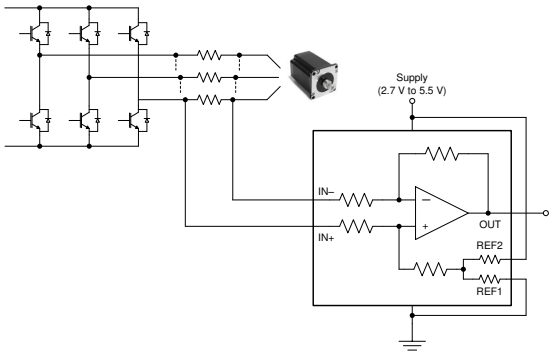
INA240 –4-V to 80-V, Bidirectional, Ultra-Precise Current Sense Amplifier With Enhanced PWM Rejection

1 Features

- Enhanced PWM Rejection
- Excellent CMRR:
  - 132-dB DC CMRR
  - 93-dB AC CMRR at 50 kHz
- Wide Common-Mode Range: –4 V to 80 V
- Accuracy:
  - Gain:
    - Gain Error: 0.20% (Maximum)
    - Gain Drift: 2.5 ppm/°C (Maximum)
  - Offset:
    - Offset Voltage: ±25 µV (Maximum)
    - Offset Drift: 250 nV/°C (Maximum)
- Available Gains:
  - INA240A1: 20 V/V
  - INA240A2: 50 V/V
  - INA240A3: 100 V/V
  - INA240A4: 200 V/V
- Quiescent Current: 2.4 mA (Maximum)

2 Applications

- Motor Controls
- Solenoid and Valve Controls
- Power Management
- Actuator Controls
- Pressure Regulators
- Telecom Equipment



Typical Application

3 Description

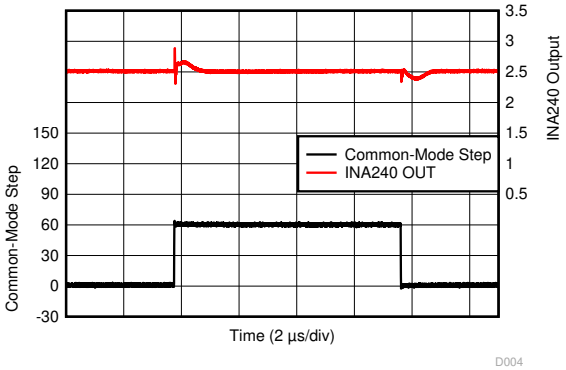
The INA240 device is a voltage-output, current-sense amplifier with enhanced PWM rejection that can sense drops across shunt resistors over a wide common-mode voltage range from –4 V to 80 V, independent of the supply voltage. The negative common-mode voltage allows the device to operate below ground, accommodating the flyback period of typical solenoid applications. Enhanced PWM rejection provides high levels of suppression for large common-mode transients (ΔV/Δt) in systems that use pulse width modulation (PWM) signals (such as motor drives and solenoid control systems). This feature allows for accurate current measurements without large transients and associated recovery ripple on the output voltage.

This device operates from a single 2.7-V to 5.5-V power supply, drawing a maximum of 2.4 mA of supply current. Four fixed gains are available: 20 V/V, 50 V/V, 100 V/V, and 200 V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10-mV full-scale. All versions are specified over the extended operating temperature range (–40°C to +125°C), and are offered in an 8-pin TSSOP and 8-pin SOIC packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA240	TSSOP (8)	3.00 mm × 4.40 mm
	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Enhanced PWM Rejection

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2017) to Revision C (December 2021)	Page
• Changed D (SOIC) package size from: 4.00 mm × 3.91 mm to: 4.90 mm × 3.91 mm	1
• Added text *or leave unconnected.* to the NC pin description	3

Changes from Revision A (October 2016) to Revision B (October 2017)	Page
• Added D (SOIC) package to *Device Information* table	1
• Added *Description (cont.)* section	1
• Added preview label to 8-pin TSSOP package	1
• Added D (SOIC) pinout diagram and table to *Pin Configuration and Functions* section	3
• Changed y-axis values in Figure 7-15	6
• Added Figure 11-2	24

Changes from Revision * (July 2016) to Revision A (October 2016)	Page
• Changed document status from Product Preview to Production Data	1

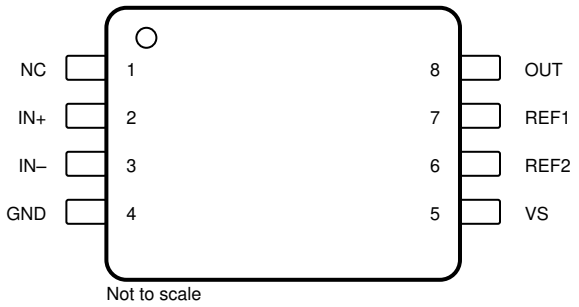
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5 Device Comparison

Table 5-1. Device Comparison

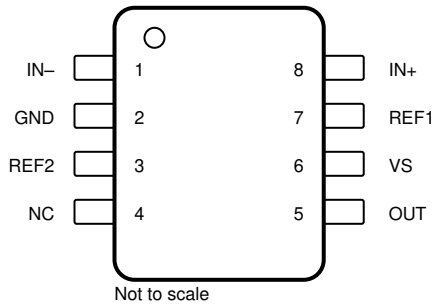
PRODUCT	GAIN (V/V)
INA240A1	20
INA240A2	50
INA240A3	100
INA240A4	200

6 Pin Configuration and Functions



NC- no internal connection

Figure 6-1. INA240 PW Package 8-Pin TSSOP Top View



NC- no internal connection

Figure 6-2. INA240 D Package 8-Pin SOIC Top View

Table 6-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	PW (TSSOP)	D (SOIC)		
GND	4	2	Analog	Ground
IN–	3	1	Analog input	Connect to load side of shunt resistor
IN+	2	8	Analog input	Connect to supply side of shunt resistor
NC	1	4	—	Reserved. Connect to ground or leave floating
OUT	8	5	Analog output	Output voltage
REF1	7	7	Analog input	Reference 1 voltage. Connect to 0 V to VS; see the *Adjusting the Output Midpoint With the Reference Pins* section for connection options
REF2	6	3	Analog input	Reference 2 voltage. Connect to 0 V to VS; see the *Adjusting the Output Midpoint With the Reference Pins* section for connection options
VS	5	6	—	Power supply, 2.7 V to 5.5 V

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage			6	V
Analog inputs, V_{IN+}, V_{IN-} (2)	Differential (V_{IN+}) – (V_{IN-})	–80	80	V
	Common-mode	–6	90	
REF1, REF2, NC inputs		GND – 0.3	V_S + 0.3	V
Output		GND – 0.3	V_S + 0.3	V
Operating free-air temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and V_{IN-} are the voltages at the IN+ and IN– pins, respectively.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	–4		80	V
V_S	Operating supply voltage	2.7		5.5	V
T_A	Operating free-air temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA240		UNIT
		PW (TSSOP)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.1	113.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.2	51.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.4	57.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	10.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.4	56.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

at T_A = 25 °C, VS = 5 V, $V_{SENSE} = V_{IN+} – V_{IN–}$, V_{CM} = 12 V, and $V_{REF1} = V_{REF2} = V_S$ / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input range	V_{IN+} = –4 V to 80 V, V_{SENSE} = 0 mV T_A = – 40°C to 125°C	–4		80	V
CMRR	Common-mode rejection ratio	V_{IN+} = –4 V to 80 V, V_{SENSE} = 0 mV T_A = –40°C to 125°C	120	132		dB
		f = 50 kHz		93		
V_{OS}	Offset voltage, input-referred	V_{SENSE} = 0 mV		±5	±25	µV
dV_{OS}/dT	Offset voltage drift	V_{SENSE} = 0 mV, T_A = –40°C to 125°C		±50	±250	nV/°C
PSRR	Power-supply rejection ratio	V_S = 2.7 V to 5.5 V, V_{SENSE} = 0 mV T_A = –40°C to 125°C		±1	±10	µV/V
I_B	Input bias current	I_{B+}, $I_{B–}$, V_{SENSE} = 0 mV		90		µA
	Reference input range		0		V_S	V
OUTPUT						
G	Gain	INA240A1		20		V/V
		INA240A2		50		
		INA240A3		100		
		INA240A4		200		
	Gain error	GND + 50 mV ≤ V_{OUT} ≤ V_S – 200 mV		±0.05%	±0.20%	
		T_A = –40°C to 125°C		±0.5	±2.5	ppm/°C
	Non-linearity error	GND + 10 mV ≤ V_{OUT} ≤ V_S – 200 mV		±0.01%		
	Reference divider accuracy	$V_{OUT} = \lvert (V_{REF1} – V_{REF2}) \rvert / 2$ at V_{SENSE} = 0 mV, T_A = –40°C to 125°C		0.02%	0.1%	
RVRR	Reference voltage rejection ratio (input-referred)	INA240A1		20		µV/V
		INA240A3		5		
		INA240A2, INA240A4		2		
	Maximum capacitive load	No sustained oscillation		1		nF
VOLTAGE OUTPUT(2)						
	Swing to V_S power-supply rail	R_L = 10 kΩ to GND T_A = –40°C to 125°C		V_S – 0.05	V_S – 0.2	V
	Swing to GND	R_L = 10 kΩ to GND, V_{SENSE} = 0 mV $V_{REF1} = V_{REF2}$ = 0 V, T_A = –40°C to 125°C		V_{GND} + 1	V_{GND} + 10	mV
FREQUENCY RESPONSE						
BW	Bandwidth	All gains, –3-dB bandwidth		400		kHz
		All gains, 2% THD+N(1)		100		
	Settling time - output settles to 0.5% of final value	INA240A1		9.6		µs
		INA240A4		9.8		
SR	Slew rate			2		V/µs
NOISE (INPUT REFERRED)						
	Voltage noise density			40		nV/√Hz
POWER SUPPLY						
V_S	Operating voltage range	T_A = –40°C to 125°C	2.7		5.5	V
I_Q	Quiescent current	V_{SENSE} = 0 mV		1.8	2.4	mA
		I_Q vs temperature, T_A = –40°C to 125°C			2.6	
TEMPERATURE RANGE						
	Specified range		–40		125	°C

(1) See the *Input Signal Bandwidth* section for more details.
(2) See Figure 7-13.

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7.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, V_{CM} = 12 V, and V_{REF} = V_S / 2 (unless otherwise noted)

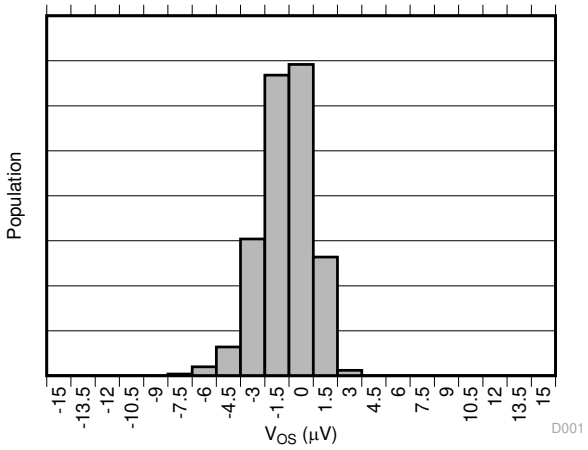


Figure 7-1. Input Offset Voltage Production Distribution

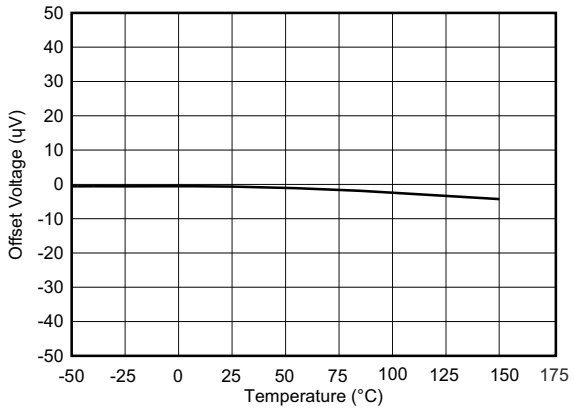


Figure 7-2. Offset Voltage vs Temperature

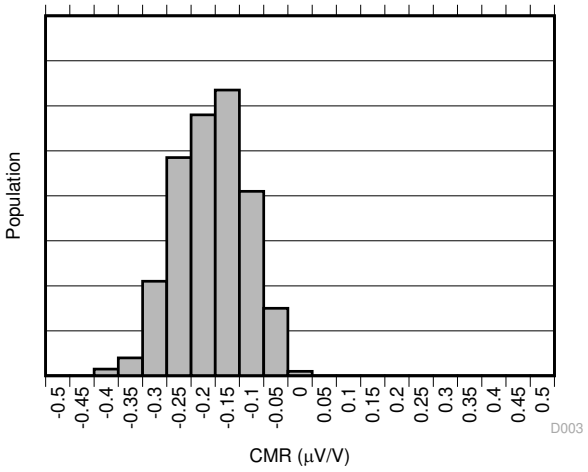


Figure 7-3. Common-Mode Rejection Production Distribution

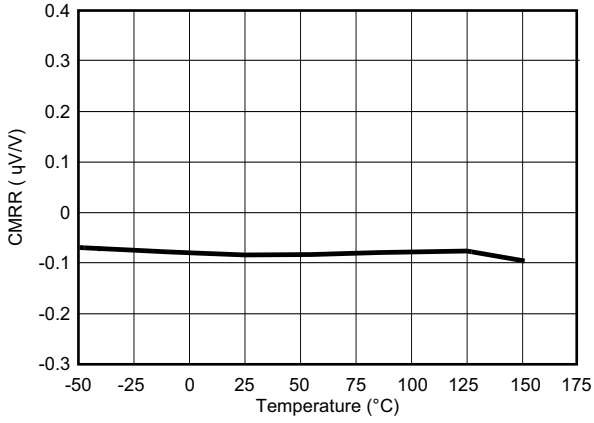


Figure 7-4. Common-Mode Rejection Ratio vs Temperature

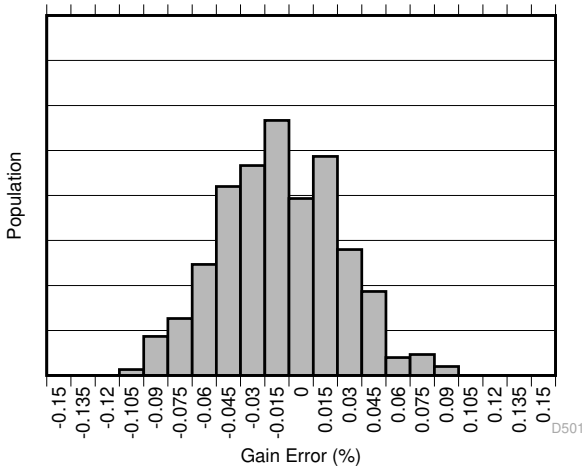


Figure 7-5. Gain Error Production Distribution

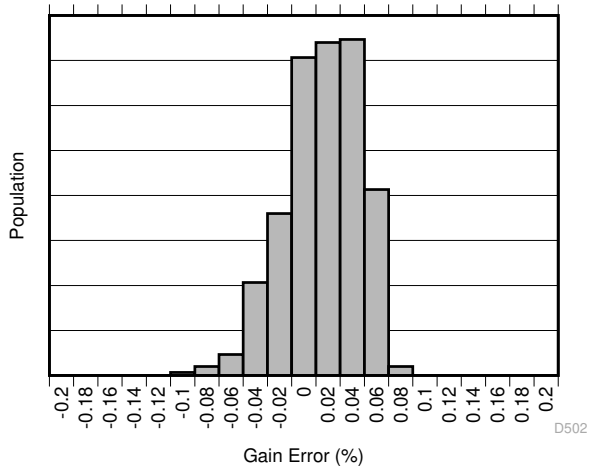


Figure 7-6. Gain Error Production Distribution

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7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{CM} = 12 V, and V_{REF} = V_S / 2 (unless otherwise noted)

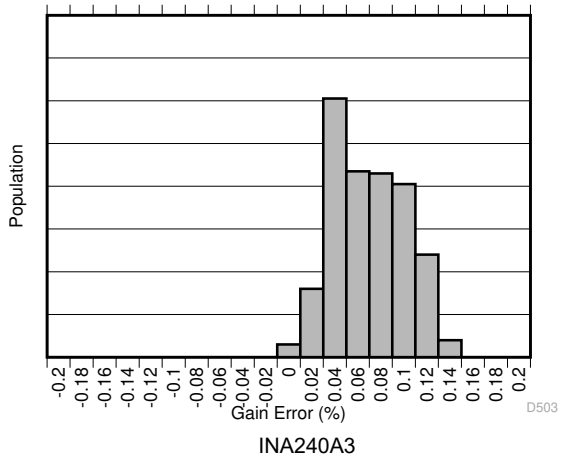


Figure 7-7. Gain Error Production Distribution

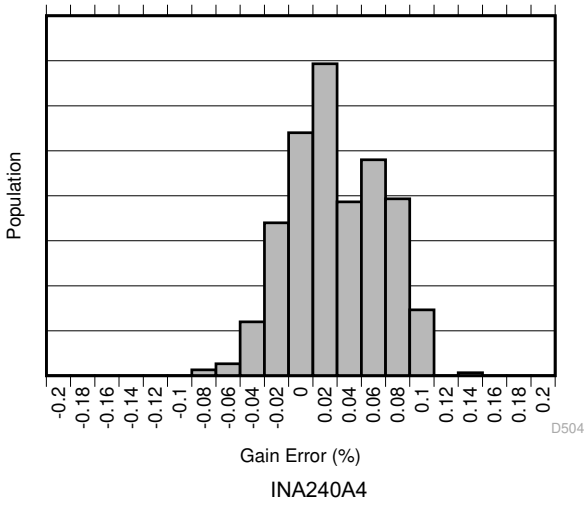


Figure 7-8. Gain Error Production Distribution

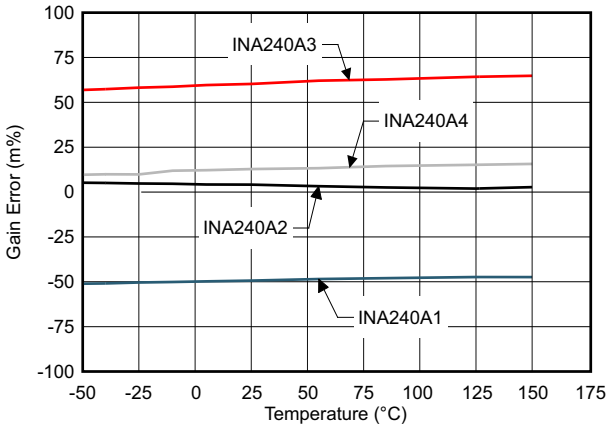


Figure 7-9. Gain Error vs Temperature

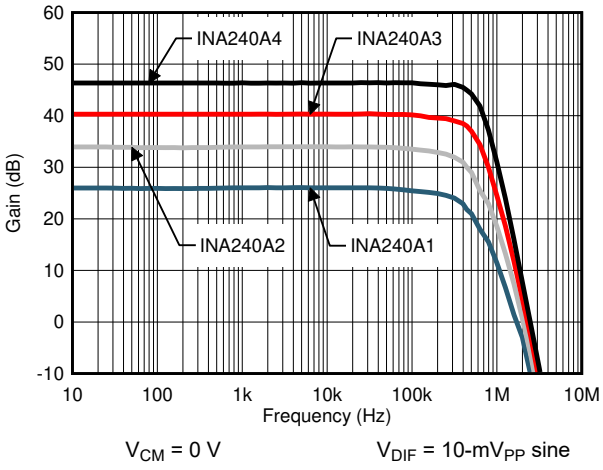


Figure 7-10. Gain vs Frequency

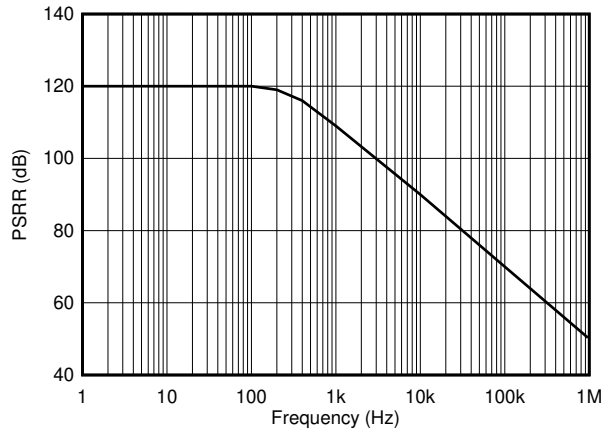


Figure 7-11. Power-Supply Rejection Ratio vs Frequency

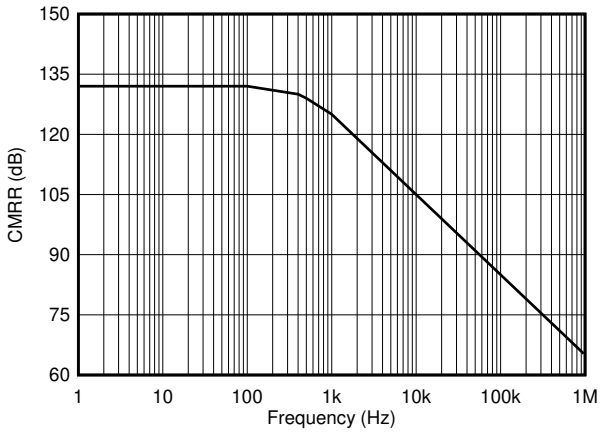


Figure 7-12. Common-Mode Rejection Ratio vs Frequency

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7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{CM} = 12 V, and V_{REF} = V_S / 2 (unless otherwise noted)

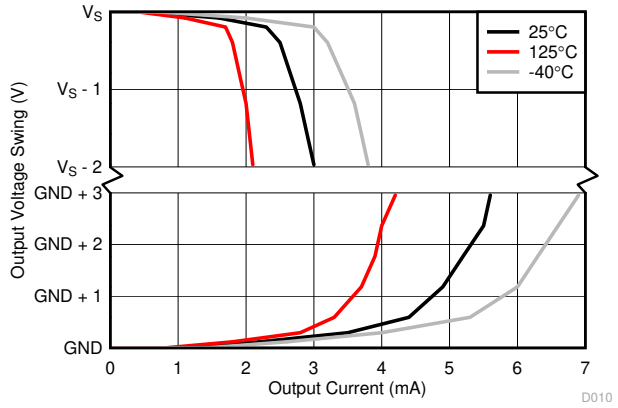
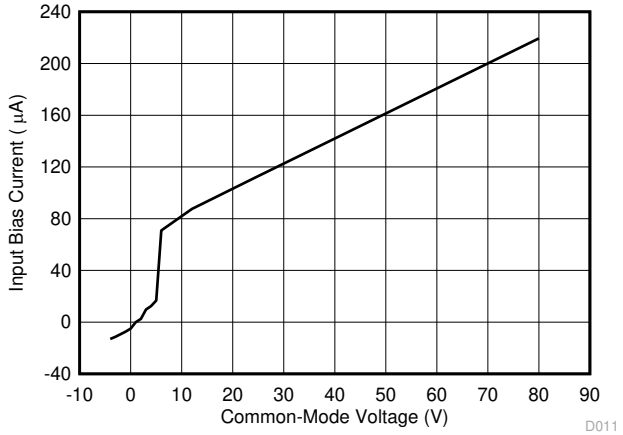
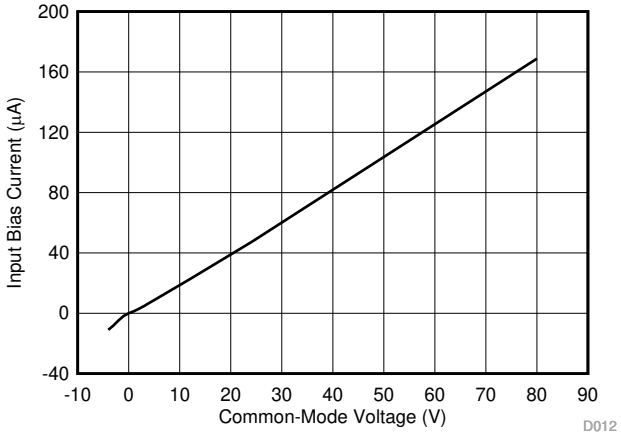


Figure 7-13. Output Voltage Swing vs Output Current



V_S = 5 V

Figure 7-14. Input Bias Current vs Common-Mode Voltage



V_S = 0 V

Figure 7-15. Input Bias Current vs Common-Mode Voltage

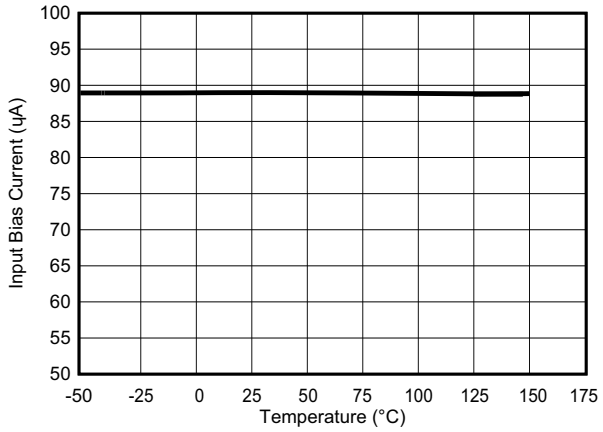


Figure 7-16. Input Bias Current vs Temperature

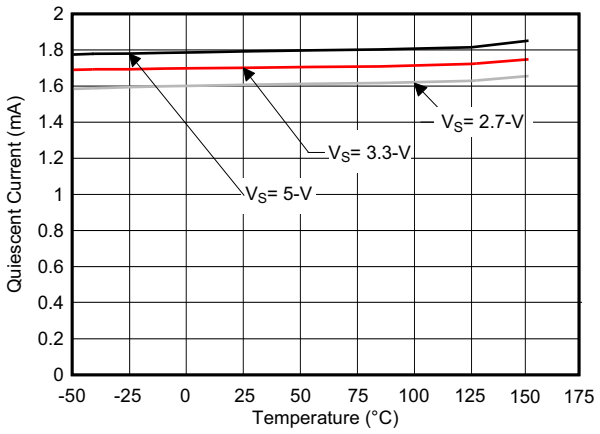


Figure 7-17. Quiescent Current vs Temperature

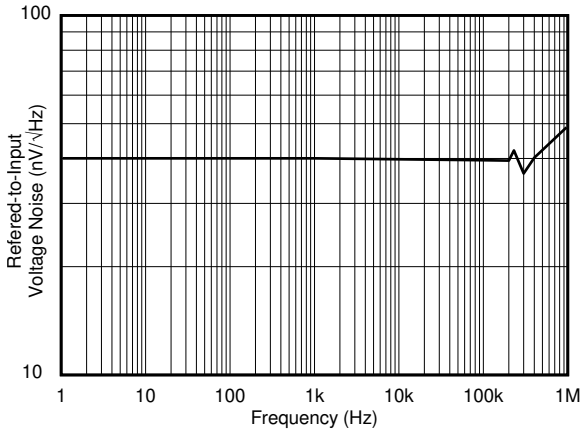
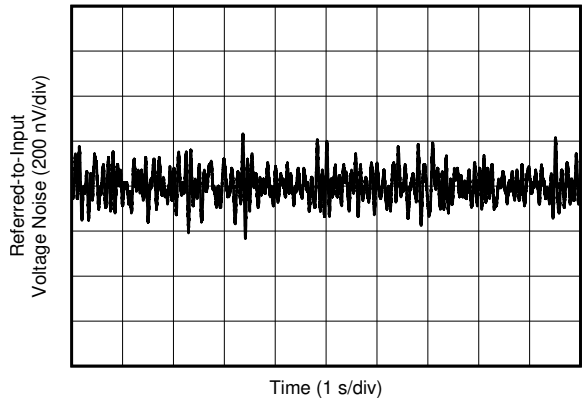


Figure 7-18. Input-Referred Voltage Noise vs Frequency

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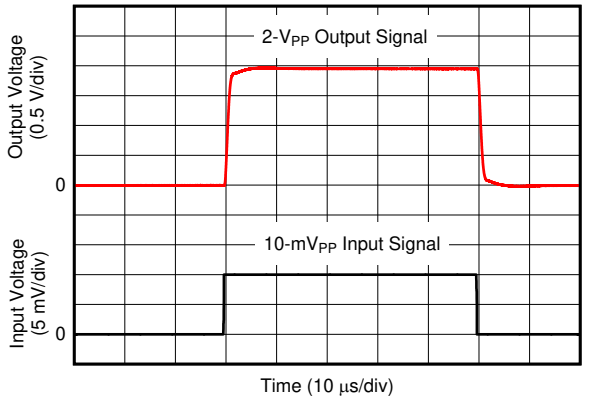
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{CM} = 12 V, and V_{REF} = V_S / 2 (unless otherwise noted)



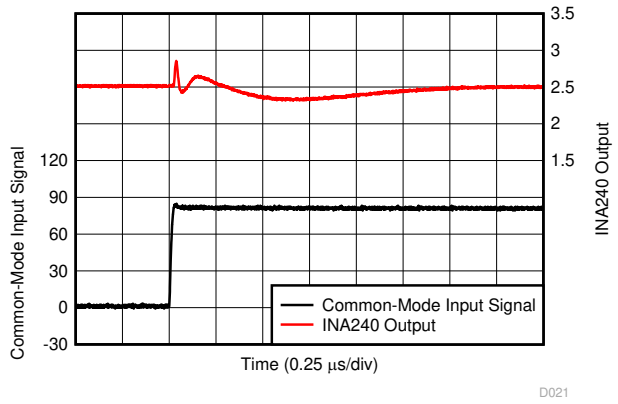
V_S = ±2.5 V V_{CM} = 0 V V_{DIF} = 0 V
V_{REF1} = V_{REF2} = 0 V Input referred

Figure 7-19. 0.1-Hz to 10-Hz Voltage Noise



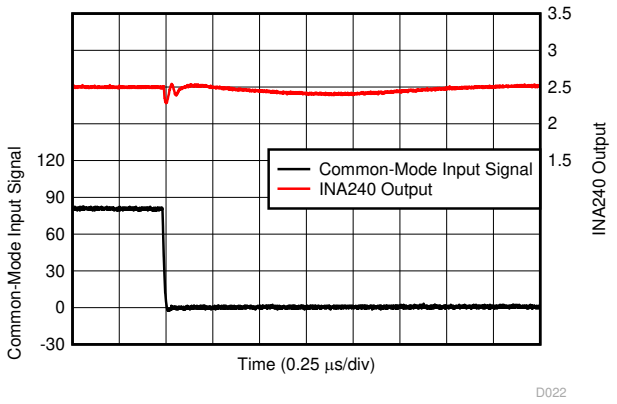
V_{REF1} = V_{REF2} = 0 V 10-mV_{PP} input step

Figure 7-20. Step Response



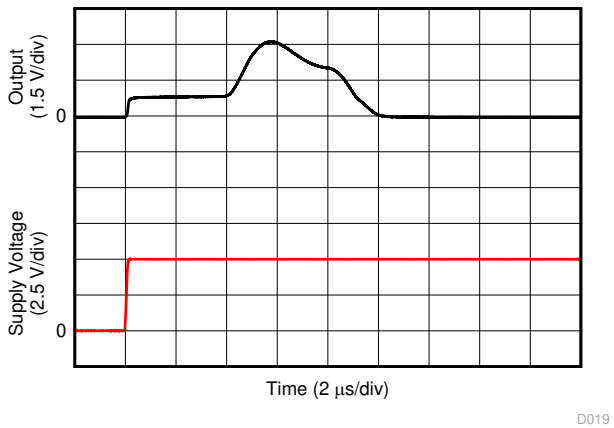
Rising edge

Figure 7-21. Common-Mode Voltage Transient Response



Falling edge

Figure 7-22. Common-Mode Voltage Transient Response



V_{REF1} = V_{REF2} = 0 V

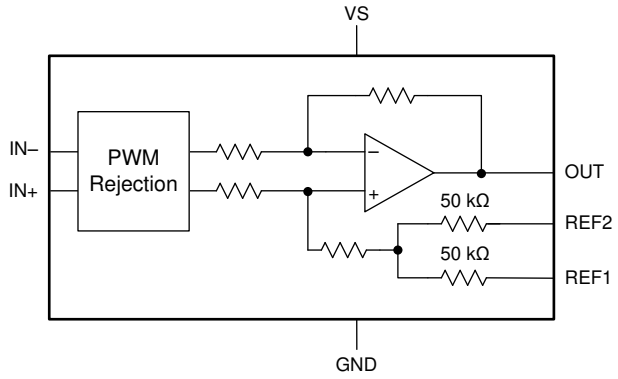
Figure 7-23. Start-Up Response

8 Detailed Description

8.1 Overview

The INA240 is a current-sense amplifier that offers a wide common-mode range, precision, zero-drift topology, excellent common-mode rejection ratio (CMRR), and features enhanced pulse width modulation (PWM) rejection. Enhanced PWM rejection reduces the effect of common-mode transients on the output signal that are associated with PWM signals. Multiple gain versions are available to allow for the optimization of the desired full-scale output voltage based on the target current range expected in the application.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Amplifier Input Signal

The INA240 is designed to handle large common-mode transients over a wide voltage range. Input signals from current measurement applications for linear and PWM applications can be connected to the amplifier to provide a highly accurate output, with minimal common-mode transient artifacts.

8.3.1.1 Enhanced PWM Rejection Operation

The enhanced PWM rejection feature of the INA240 provides increased attenuation of large common-mode ΔV/Δt transients. Large ΔV/Δt common-mode transients associated with PWM signals are employed in applications such as motor or solenoid drive and switching power supplies. Traditionally, large ΔV/Δt common-mode transitions are handled strictly by increasing the amplifier signal bandwidth, which can increase chip size, complexity and ultimately cost. The INA240 is designed with high common-mode rejection techniques to reduce large ΔV/Δt transients before the system is disturbed as a result of these large signals. The high AC CMRR, in conjunction with signal bandwidth, allows the INA240 to provide minimal output transients and ringing compared with standard circuit approaches.

8.3.1.2 Input Signal Bandwidth

The INA240 input signal, which represents the current being measured, is accurately measured with minimal disturbance from large ΔV/Δt common-mode transients as previously described. For PWM signals typically associated with motors, solenoids, and other switching applications, the current being monitored varies at a significantly slower rate than the faster PWM frequency.

The INA240 bandwidth is defined by the –3-dB bandwidth of the current-sense amplifier inside the device; see the *Electrical Characteristics* table. The device bandwidth provides fast throughput and fast response required for the rapid detection and processing of overcurrent events. Without the higher bandwidth, protection circuitry may not have adequate response time and damage may occur to the monitored application or circuit.

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Figure 8-1 shows the performance profile of the device over frequency. Harmonic distortion increases at the upper end of the amplifier bandwidth with no adverse change in detection of overcurrent events. However, increased distortion at the highest frequencies must be considered when the measured current bandwidth begins to approach the INA240 bandwidth.

For applications requiring distortion sensitive signals, Figure 8-1 provides information to show that there is an optimal frequency performance range for the amplifier. The full amplifier bandwidth is always available for fast overcurrent events at the same time that the lower frequency signals are amplified at a low distortion level. The output signal accuracy is reduced for frequencies closer to the maximum bandwidth. Individual requirements determine the acceptable limits of distortion for high-frequency, current-sensing applications. Testing and evaluation in the end application or circuit is required to determine the acceptance criteria and to validate the performance levels meet the system specifications.

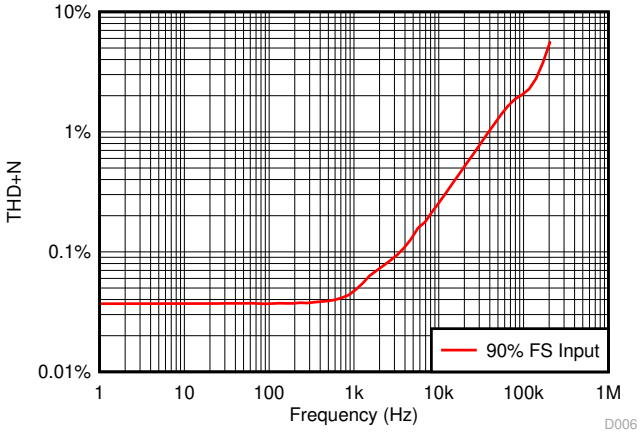


Figure 8-1. Performance Over Frequency

8.3.2 Selecting the Sense Resistor (R_{SENSE})

The INA240 determines the current magnitude from measuring the differential voltage developed across a resistor. This resistor is referred to as a *current-sensing* resistor or a *current-shunt* resistor. The flexible design of the device allows a wide input signal range across this current-sensing resistor.

The current-sensing resistor is ideally chosen solely based on the full-scale current to be measured, the full-scale input range of the circuitry following the device, and the device gain selected. The minimum current-sensing resistor is a design-based decision in order to maximize the input range of the signal chain circuitry. Full-scale output signals that are not maximized to the full input range of the system circuitry limit the ability of the system to exercise the full dynamic range of system control.

Two important factors to consider when finalizing the current-sensing resistor value are: the required current measurement accuracy and the maximum power dissipation across the resistor. A larger resistor voltage provides for a more accurate measurement, but increases the power dissipation in the resistor. The increased power dissipation generates heat, which reduces the sense resistor accuracy because of the temperature coefficient. The voltage signal measurement uncertainty is reduced when the input signal gets larger because any fixed errors become a smaller percentage of the measured signal. The design trade-off to improve measurement accuracy increases the current-sensing resistor value. The increased resistance value results in an increased power dissipation in the system which can additionally decrease the overall system accuracy. Based on these relationships, the measurement accuracy is inversely proportional to both the resistance value and power dissipation contributed by the current-shunt selection.

By increasing the current-shunt resistor, the differential voltage is increased across the resistor. Larger input differential voltages require a smaller amplifier gain to achieve a full-scale amplifier output voltage. Smaller current-shunt resistors are desired but require large amplifier gain settings. The larger gain settings often have increased error and noise parameters, which are not attractive for precision designs. Historically, the design goals for high-performance measurements forced designers to accept selecting larger current-sense resistors and the lower gain amplifier settings. The INA240 provides 100-V/V and 200-V/V gain options that offer the

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high-gain setting and maintains high-performance levels with offset values below 25 µV. These devices allow for the use of lower shunt resistor values to achieve lower power dissipation and still meet high system performance specifications.

Table 8-1 shows an example of the different results obtained from using two different gain versions of the INA240. From the table data, the higher gain device allows a smaller current-shunt resistor and decreased power dissipation in the element. The *Calculating Total Error* section provides information on the error calculations that must be considered in addition to the gain and current-shunt value when designing with the INA240.

Table 8-1. R_{SENSE} Selection and Power Dissipation(1)

PARAMETER		EQUATION	RESULTS	
			INA240A1	INA240A4
Gain		—	20 V/V	200 V/V
V_{DIFF}	Ideal maximum differential input voltage	$V_{DIFF} = V_{OUT}$ / Gain	150 mV	15 mV
R_{SENSE}	Current-sense resistor value	$R_{SENSE} = V_{DIFF} / I_{MAX}$	15 mΩ	1.5 mΩ
P_{RSENSE}	Current-sense resistor power dissipation	$R_{SENSE} \times I_{MAX}^2$	1.5 W	0.15 W

(1) Full-scale current = 10 A, and full-scale output voltage = 3 V.

8.4 Device Functional Modes

8.4.1 Adjusting the Output Midpoint With the Reference Pins

Figure 8-2 shows a test circuit for reference-divider accuracy. The INA240 output is configurable to allow for unidirectional or bidirectional operation.

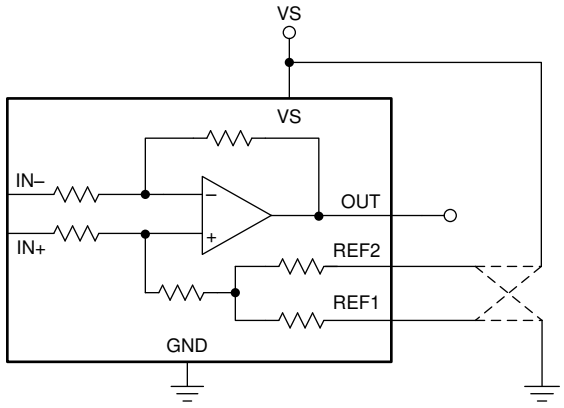


Figure 8-2. Test Circuit For Reference Divider Accuracy

Note

Do not connect the REF1 pin or the REF2 pin to any voltage source lower than GND or higher than V_S.

The output voltage is set by applying a voltage or voltages to the reference voltage inputs, REF1 and REF2. The reference inputs are connected to an internal gain network. There is no operational difference between the two reference pins.

8.4.2 Reference Pin Connections for Unidirectional Current Measurements

Unidirectional operation allows current measurements through a resistive shunt in one direction. For unidirectional operation, connect the device reference pins together and then to the negative rail (see the *Ground Referenced Output* section) or the positive rail (see the *VS Referenced Output* section). The required differential input polarity depends on the output voltage setting. The amplifier output moves away from the referenced rail proportional to the current passing through the external shunt resistor. If the amplifier reference pins are connected to the positive rail, then the input polarity must be negative to move the amplifier output down

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(towards ground). If the amplifier reference pins are connected at ground, then the input polarity must be positive to move the amplifier output up (towards supply).

The following sections describe how to configure the output for unidirectional operation cases.

8.4.2.1 Ground Referenced Output

When using the INA240 in a unidirectional mode with a ground referenced output, both reference inputs are connected to ground; this configuration takes the output to ground when there is a 0-V differential at the input (as Figure 8-3 shows).

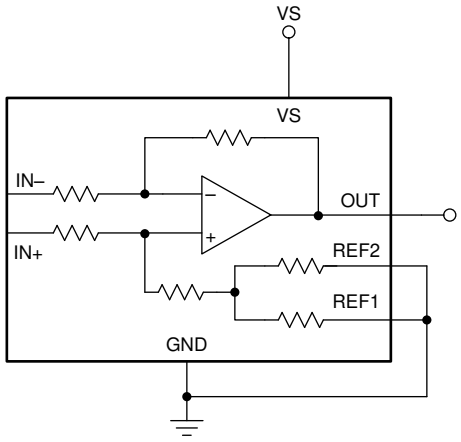


Figure 8-3. Ground Referenced Output

8.4.2.2 VS Referenced Output

Unidirectional mode with a VS referenced output is configured by connecting both reference pins to the positive supply. Use this configuration for circuits that require power-up and stabilization of the amplifier output signal and other control circuitry before power is applied to the load (as shown in Figure 8-4).

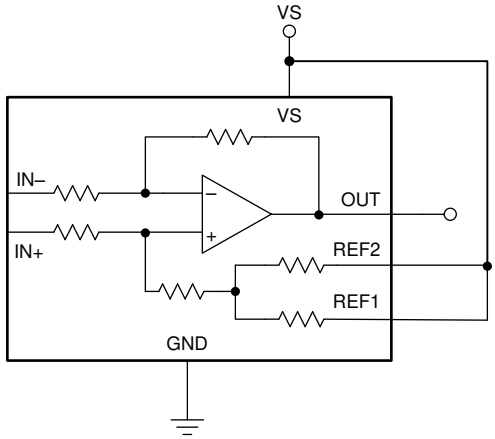


Figure 8-4. VS Referenced Output

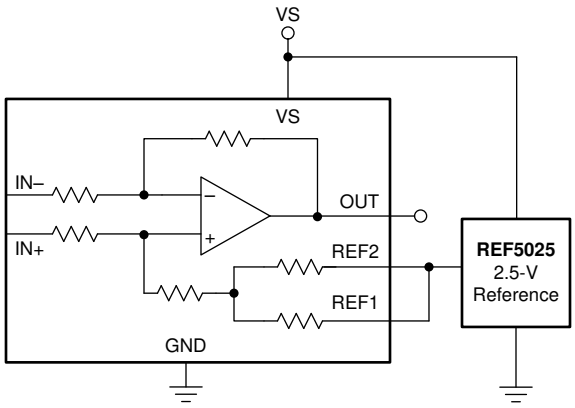
8.4.3 Reference Pin Connections for Bidirectional Current Measurements

Bidirectional operation allows the INA240 to measure currents through a resistive shunt in two directions. For this operation case, the output voltage can be set anywhere within the reference input limits. A common configuration is to set the reference inputs at half-scale for equal range in both directions. However, the reference inputs can be set to a voltage other than half-scale when the bidirectional current is non-symmetrical.

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8.4.3.1 Output Set to External Reference Voltage

Connecting both pins together and then to a reference voltage results in an output voltage equal to the reference voltage for the condition of shorted input pins or a 0-V differential input; this configuration is shown in Figure 8-5. The output voltage decreases below the reference voltage when the IN+ pin is negative relative to the IN– pin and increases when the IN+ pin is positive relative to the IN– pin. This technique is the most accurate way to bias the output to a precise voltage.



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Figure 8-5. External Reference Output

8.4.3.2 Output Set to Midsupply Voltage

By connecting one reference pin to VS and the other to the GND pin, the output is set at half of the supply when there is no differential input, as shown in Figure 8-6. This method creates a ratiometric offset to the supply voltage, where the output voltage remains at VS / 2 for 0 V applied to the inputs.

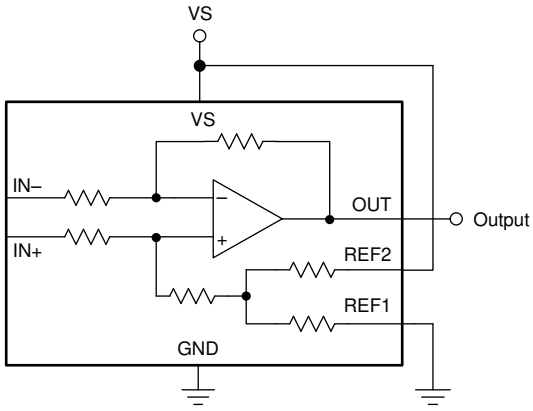
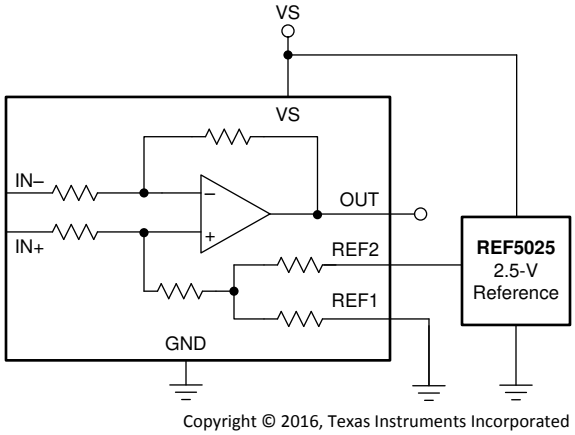


Figure 8-6. Midsupply Voltage Output

8.4.3.3 Output Set to Mid-External Reference

In this case, an external reference is divided by two by connecting one REF pin to ground and the other REF pin to the reference, as shown in Figure 8-7.

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Figure 8-7. Mid-External Reference Output

8.4.3.4 Output Set Using Resistor Divider

The INA240 REF1 and REF2 pins allow for the midpoint of the output voltage to be adjusted for system circuitry connections to analog to digital converters (ADCs) or other amplifiers. The REF pins are designed to be connected directly to supply, ground, or a low-impedance reference voltage. The REF pins can be connected together and biased using a resistor divider to achieve a custom output voltage. If the amplifier is used in this configuration, as shown in Figure 8-8, use the output as a differential signal with respect to the resistor divider voltage. Use of the amplifier output as a single-ended signal in this configuration is not recommended because the internal impedance shifts can adversely affect device performance specifications.

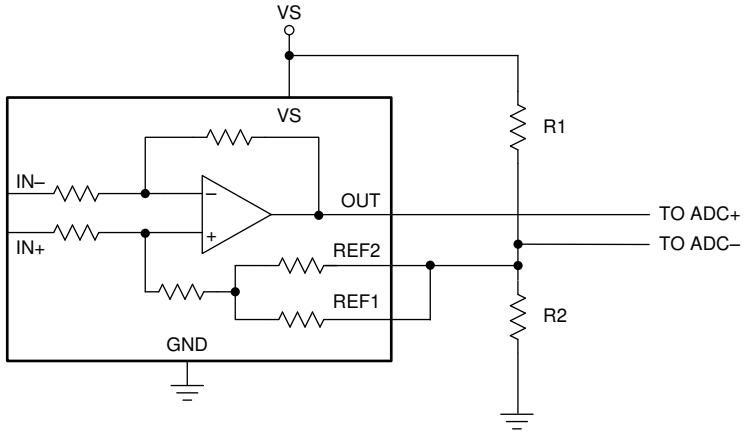


Figure 8-8. Setting the Reference Using a Resistor Divider

8.4.4 Calculating Total Error

The INA240 electrical specifications (see the *Electrical Characteristics* table) include typical individual errors terms (such as gain error, offset error, and nonlinearity error). Total error, including all of these individual error components, is not specified in the *Electrical Characteristics* table. In order to accurately calculate the expected error of the device, the device operating conditions must first be known. Some current-shunt monitors specify a total error in the product data sheet. However, this total error term is accurate under only one particular set of operating conditions. Specifying the total error at this point has limited value because any deviation from these specific operating conditions no longer yields the same total error value. This section discusses the individual error sources and how the device total error value can be calculated from the combination of these errors for specific conditions.

Two examples are provided in Table 8-2 and Table 8-3 that detail how different operating conditions can affect the total error calculations. Typical and maximum calculations are shown as well to provide the user more information on how much error variance is present from device to device.

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8.4.4.1 Error Sources

The typical error sources that have the largest effect on the total error of the device are gain error, nonlinearity, common-mode rejection ratio, and input offset voltage error. For the INA240, an additional error source (referred to as the *reference voltage rejection ratio*) is also included in the total error value.

8.4.4.2 Reference Voltage Rejection Ratio Error

Reference voltage rejection ratio refers to the amount of error induced by applying a reference voltage to the INA240 that deviates from the mid-point of the device supply voltage.

8.4.4.2.1 Total Error Example 1

Table 8-2. Total Error Calculation: Example 1(1)

TERM	SYMBOL	EQUATION	TYPICAL VALUE
Initial input offset voltage	V_{OS}	—	5 µV
Added input offset voltage because of common-mode voltage	V_{OS_CM}	$\frac{1}{10^{\left(\frac{CMRR_dB}{20}\right)}} \times (V_{CM} - 12V)$	0 µV
Added input offset voltage because of reference voltage	V_{OS_REF}	$RVRR \times \lvert V_S / 2 - V_{REF} \rvert$	0 µV
Total input offset voltage	V_{OS_Total}	$\sqrt{(V_{OS})^2 + (V_{OS_CM})^2 + (V_{OS_REF})^2}$	5 µV
Error from input offset voltage	$Error_V_{OS}$	$\frac{V_{OS_Total}}{V_{SENSE}} \times 100$	0.05%
Gain error	Error_Gain	—	0.05%
Nonlinearity error	Error_Lin	—	0.01%
Total error	—	$\sqrt{(Error_V_{OS})^2 + (Error_Gain)^2 + (Error_Lin)^2}$	0.07%

(1) The data for Table 8-2 was taken with the INA240A4, V_S = 5 V, V_{CM} = 12 V, $V_{REF1} = V_{REF2} = V_S / 2$, and V_{SENSE} = 10 mV.

8.4.4.2.2 Total Error Example 2

Table 8-3. Total Error Calculation: Example 2(1)

TERM	SYMBOL	EQUATION	TYPICAL VALUE
Initial input offset voltage	V_{OS}	—	5 µV
Added input offset voltage because of common-mode voltage	V_{OS_CM}	$\frac{1}{10^{\left(\frac{CMRR_dB}{20}\right)}} \times (V_{CM} - 12V)$	12.1 µV
Added input offset voltage because of reference voltage	V_{OS_REF}	$RVRR \times \lvert V_S / 2 - V_{REF} \rvert$	5 µV
Total input offset voltage	V_{OS_Total}	$\sqrt{(V_{OS})^2 + (V_{OS_CM})^2 + (V_{OS_REF})^2}$	14 µV
Error from input offset voltage	$Error_V_{OS}$	$\frac{V_{OS_Total}}{V_{SENSE}} \times 100$	0.14%
Gain error	Error_Gain	—	0.05%
Nonlinearity error	Error_Lin	—	0.01%

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Table 8-3. Total Error Calculation: Example 2(1) (continued)

TERM	SYMBOL	EQUATION	TYPICAL VALUE
Total error	—	$\sqrt{(\text{Error_V}_{OS})^2 + (\text{Error_Gain})^2 + (\text{Error_Lin})^2}$	0.15%

(1) The data for Table 8-3 was taken with the INA240A4, V_S = 5 V, V_{CM} = 60 V, V_{REF1} = V_{REF2} = 0 V, and V_{SENSE} = 10 mV.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The INA240 measures the voltage developed as current flows across the current-sensing resistor. The device provides reference pins to configure operation as either unidirectional or bidirectional output swing. When using the INA240 for inline motor current sense, the device is commonly configured for bidirectional operation.

9.1.1 Input Filtering

Note

Input filters are not required for accurate measurements using the INA240, and use of filters in this location is not recommended. If filter components are used on the input of the amplifier, follow the guidelines in this section to minimize the effects on performance.

Based strictly on user design requirements, external filtering of the current signal may be desired. The initial location that can be considered for the filter is at the output of the current amplifier. Although placing the filter at the output satisfies the filtering requirements, this location changes the low output impedance measured by any circuitry connected to the output voltage pin. The other location for filter placement is at the current amplifier input pins. This location satisfies the filtering requirement also, however the components must be carefully selected to minimally impact device performance. Figure 9-1 shows a filter placed at the inputs pins.

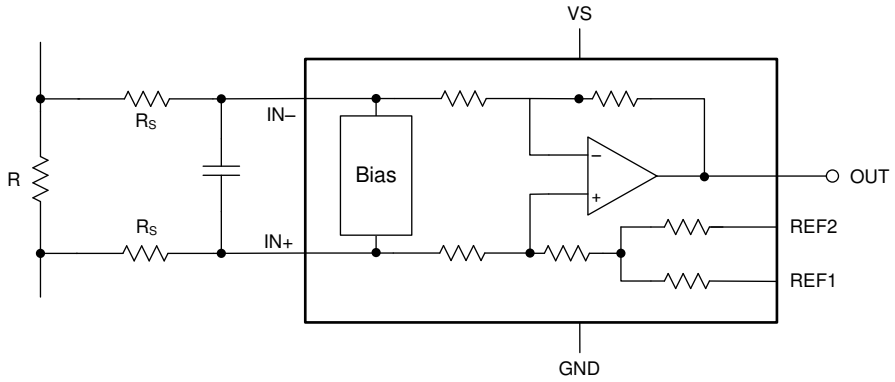


Figure 9-1. Filter at Input Pins

External series resistance provide a source of additional measurement error, so keep the value of these series resistors to 10-Ω or less to reduce loss of accuracy. The internal bias network shown in Figure 9-1 creates a mismatch in input bias currents (see Figure 9-2) when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, a mismatch is created in the voltage drop across the filter resistors. This voltage is a differential error voltage in the shunt resistor voltage. In addition to the absolute resistor value, mismatch resulting from resistor tolerance can significantly impact the error because this value is calculated based on the actual measured resistance.

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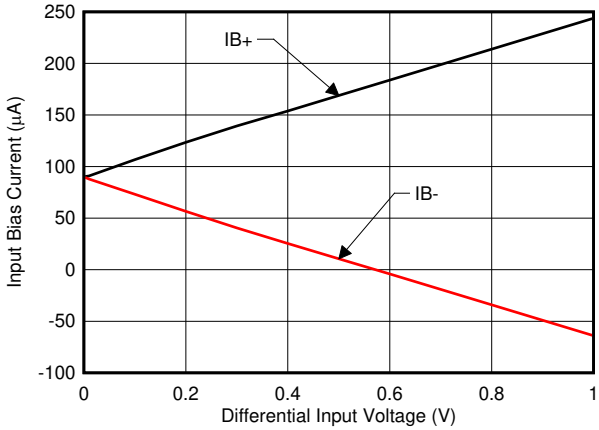


Figure 9-2. Input Bias Current vs Differential Input Voltage

The measurement error expected from the additional external filter resistors can be calculated using Equation 1, where the gain error factor is calculated using Equation 2.

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (1)$$

The gain error factor, shown in Equation 1, can be calculated to determine the gain error introduced by the additional external series resistance. Equation 1 calculates the deviation of the shunt voltage resulting from the attenuation and imbalance created by the added external filter resistance. Table 9-1 provides the gain error factor and gain error for several resistor values.

$$\text{Gain Error Factor} = \frac{3000}{R_S + 3000} \quad (2)$$

Where:

- R_S is the external filter resistance value

Table 9-1. Gain Error Factor and Gain Error For External Input Resistors

EXTERNAL RESISTANCE (Ω)	GAIN ERROR FACTOR	GAIN ERROR (%)
5	0.998	0.17
10	0.997	0.33
100	0.968	3.23

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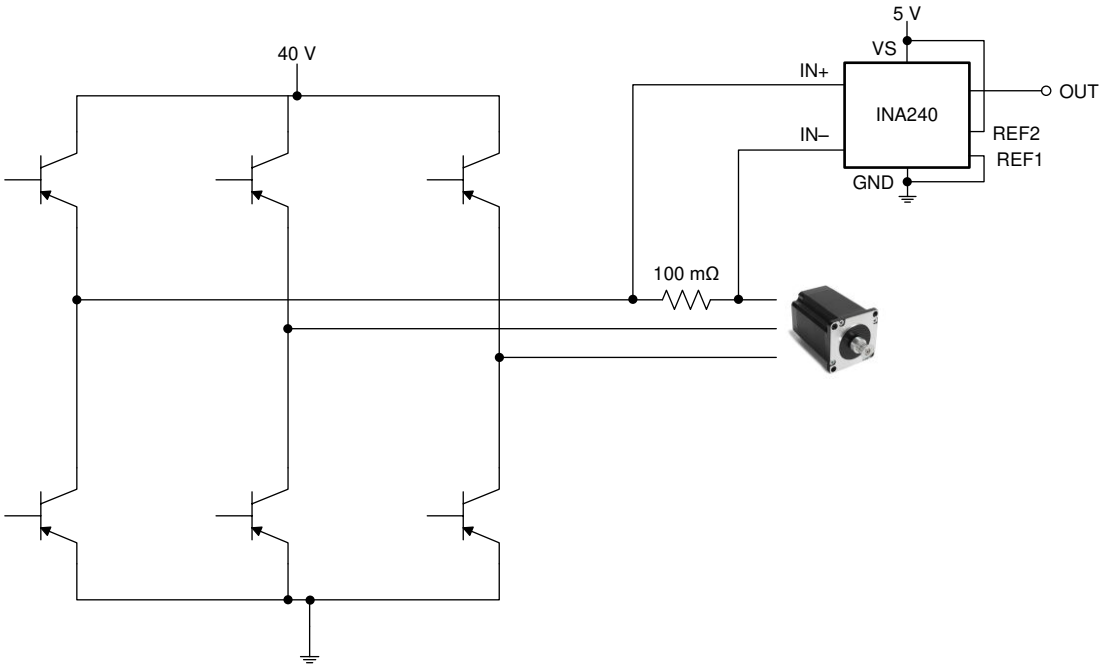
9.2 Typical Applications

The INA240 offers advantages for multiple applications including the following:

- High common-mode range and excellent CMRR enables direct inline sensing
- Ultra-low offset and drift eliminates the necessity of calibration
- Wide supply range enables a direct interface with most microprocessors

Two specific applications are provided and include more detailed information.

9.2.1 Inline Motor Current-Sense Application



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Figure 9-3. Inline Motor Application Circuit

9.2.1.1 Design Requirements

Inline current sensing has many advantages in motor control, from torque ripple reduction to real-time motor health monitoring. However, the full-scale PWM voltage requirements for inline current measurements provide challenges to accurately measure the current. Switching frequencies in the 50-kHz to 100-kHz range create higher ΔV/Δt signal transitions that must be addressed to obtain accurate inline current measurements.

With a superior common-mode rejection capability, high precision, and a high common-mode specification, the INA240 provides performance for a wide range of common-mode voltages.

9.2.1.2 Detailed Design Procedure

For this application, the INA240 measures current in the drive circuitry of a 36-V, 4000-RPM motor.

To demonstrate the performance of the device, the INA240A1 with a gain of 20 V/V was selected for this design and powered from a 5-V supply.

Using the information in the *Adjusting the Output Midpoint With the Reference Pins* section, the reference point is set to midscale by splitting the supply with REF1 connected to ground and REF2 connected to supply. This configuration allows for bipolar current measurements. Alternatively, the reference pins can be tied together and driven with an external precision reference.

The current-sensing resistor is sized so that the output of the INA240 is not saturated. A value of 100-mΩ was selected to maintain the analog input within the device limits.

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9.2.1.3 Application Curve

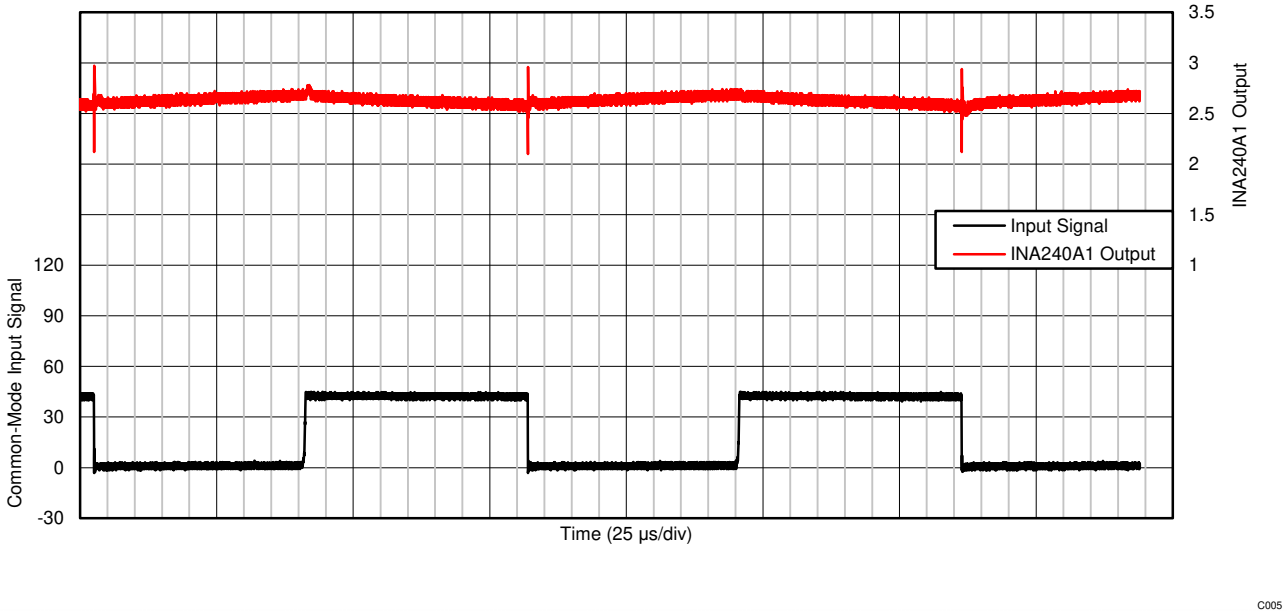
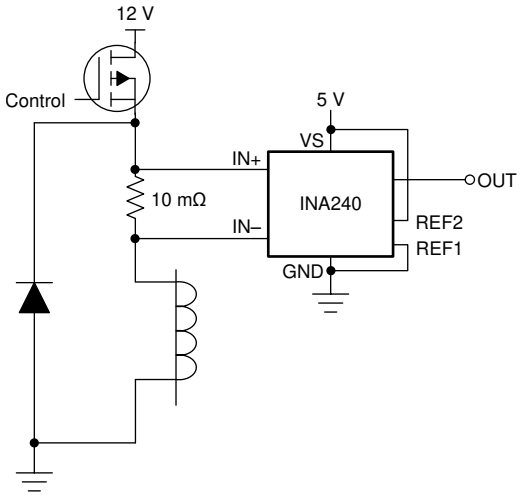


Figure 9-4. Inline Motor Current-Sense Input and Output Signals

9.2.2 Solenoid Drive Current-Sense Application



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Figure 9-5. Solenoid Drive Application Circuit

9.2.2.1 Design Requirements

Challenges exist in solenoid drive current sensing that are similar to those in motor inline current sensing. In certain topologies, the current-sensing amplifier is exposed to the full-scale PWM voltage between ground and supply. The INA240 is well suited for this type of application.

9.2.2.2 Detailed Design Procedure

For this application, the INA240 measures current in the driver circuit of a 24-V, 500-mA water valve.

To demonstrate the performance of the device, the INA240A4 with a gain of 200 V/V was selected for this design and powered from a 5-V supply.

Using the information in the *Adjusting the Output Midpoint With the Reference Pins* section, the reference point is set to midscale by splitting the supply with REF1 connected to ground and REF2 connected to supply. Alternatively, the reference pins can be tied together and driven with an external precision reference.

A value of 10 mΩ was selected to maintain the analog input within the device limits.

9.2.2.3 Application Curve

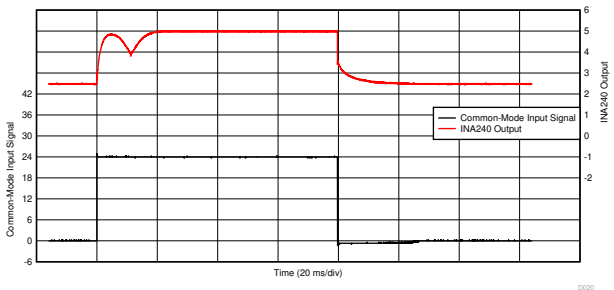


Figure 9-6. Solenoid Drive Current Sense Input and Output Signals

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9.3 What to Do and What Not to Do

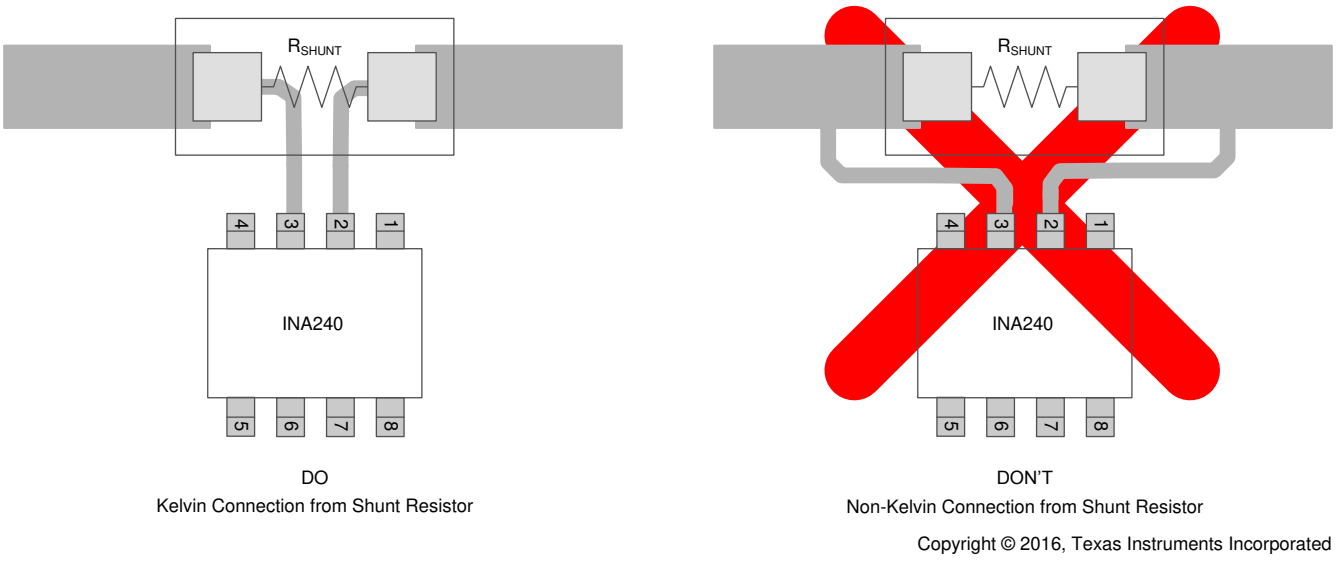
9.3.1 High-Precision Applications

For high-precision applications, verify accuracy and stability of the amplifier by:

- Providing a precision reference connected to REF1 and REF2
- Optimizing the layout of the power and sensing path of the sense resistor (see the *Layout* section)
- Providing adequate bypass capacitance on the supply pin (see the *Power Supply Decoupling* section)

9.3.2 Kelvin Connection from the Current-Sense Resistor

To provide accurate current measurements, verify the routing between the current-sense resistor and the amplifier uses a Kelvin connection. Use the information provided in Figure 9-7 and the *Connection to the Current-Sense Resistor* section during device layout.



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Figure 9-7. Shunt Connections to the INA240

10 Power Supply Recommendations

The INA240 series makes accurate measurements beyond the connected power-supply voltage (V_S) because the inputs (IN+ and IN–) operate anywhere between –4 V and 80 V independent of V_S. For example, the V_S power supply equals 5 V and the common-mode voltage of the measured shunt can be as high as 80 V.

Although the common-mode voltage of the input can be beyond the supply voltage, the output voltage range of the INA240 series is constrained to the supply voltage.

10.1 Power Supply Decoupling

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. TI recommends a bypass capacitor value of 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

11 Layout

11.1 Layout Guidelines

11.1.1 Connection to the Current-Sense Resistor

Poor routing of the current-sensing resistor can result in additional resistance between the input pins of the amplifier. Any additional high-current carrying impedance can cause significant measurement errors because the current resistor has a very-low-ohmic value. Use a Kelvin or 4-wire connection to connect to the device input pins. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins.

11.2 Layout Example

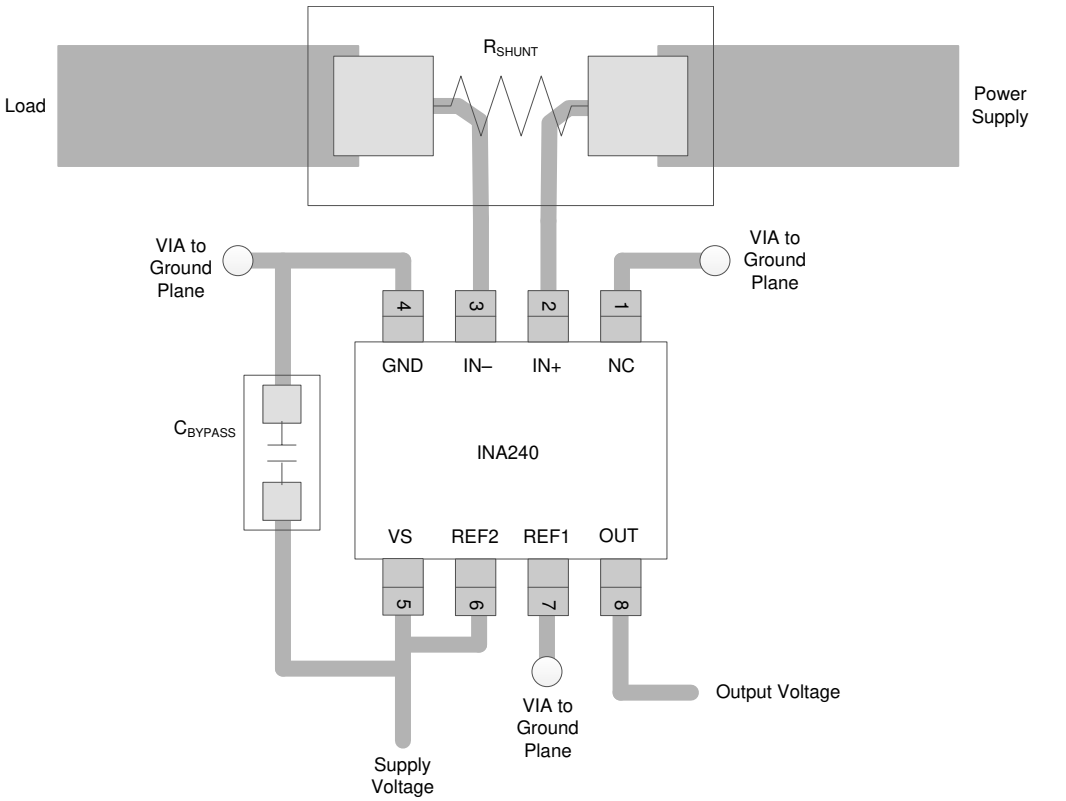


Figure 11-1. Recommended TSSOP Package Layout

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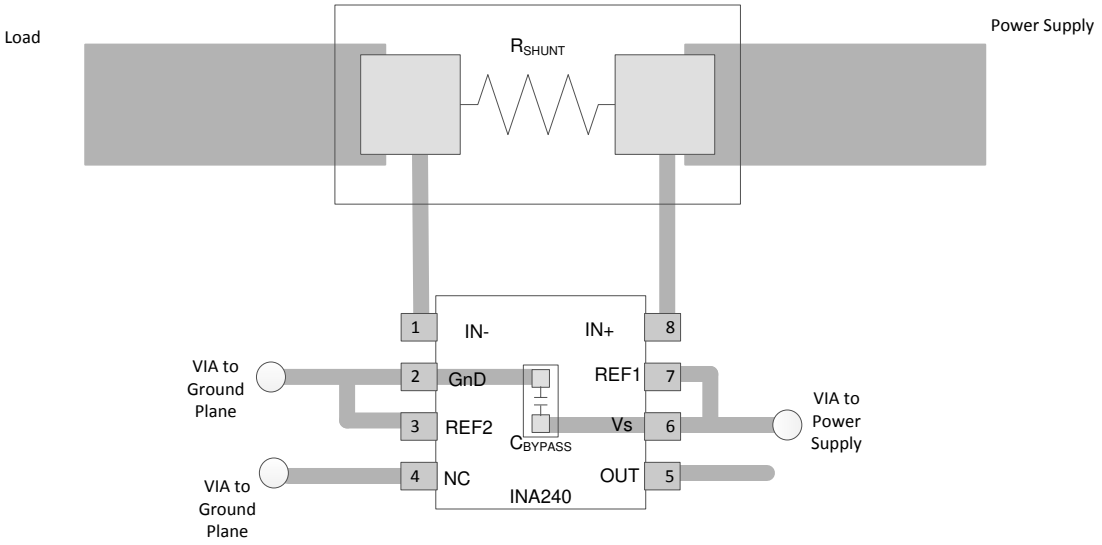


Figure 11-2. Recommended SOIC Package Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *INA240EVM User's Guide*
- Texas Instruments, *Motor Control Application Report*
- Texas Instruments, *48-V Three-Phase Inverter With Shunt-Based In-Line Motor Phase Current Sensing Reference Design*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA240A1D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1
INA240A1D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1
INA240A1DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1
INA240A1DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1
INA240A1DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1
INA240A1DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1
INA240A1PWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1
INA240A1PWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1
INA240A1PWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1
INA240A1PWRG4.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1
INA240A2DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A2
INA240A2DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A2
INA240A2DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A2
INA240A2DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A2
INA240A2PW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 125	I240A2
INA240A2PWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A2
INA240A2PWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A2
INA240A2PWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A2
INA240A2PWRG4.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A2
INA240A3D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3
INA240A3D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3
INA240A3DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3
INA240A3DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3
INA240A3DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3
INA240A3DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3
INA240A3PWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3
INA240A3PWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3
INA240A3PWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3
INA240A3PWRG4.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA240A4D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	I240A4
INA240A4DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A4
INA240A4DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A4
INA240A4PW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 125	I240A4
INA240A4PWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A4
INA240A4PWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A4
INA240A4PWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A4
INA240A4PWRG4.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A4

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF INA240 :

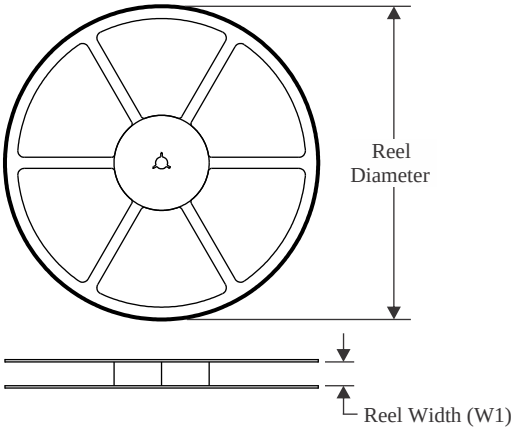
- Automotive : INA240-Q1

NOTE: Qualified Version Definitions:

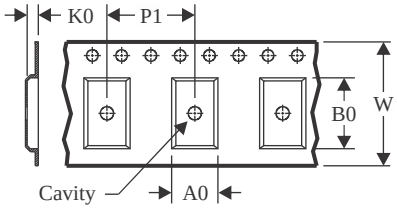
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

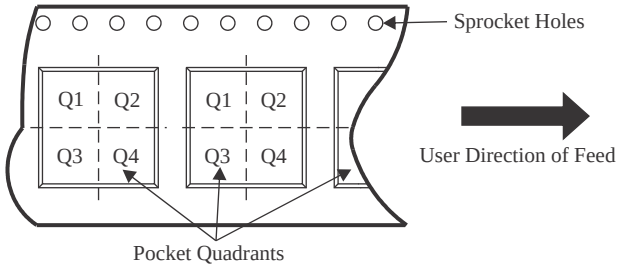


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

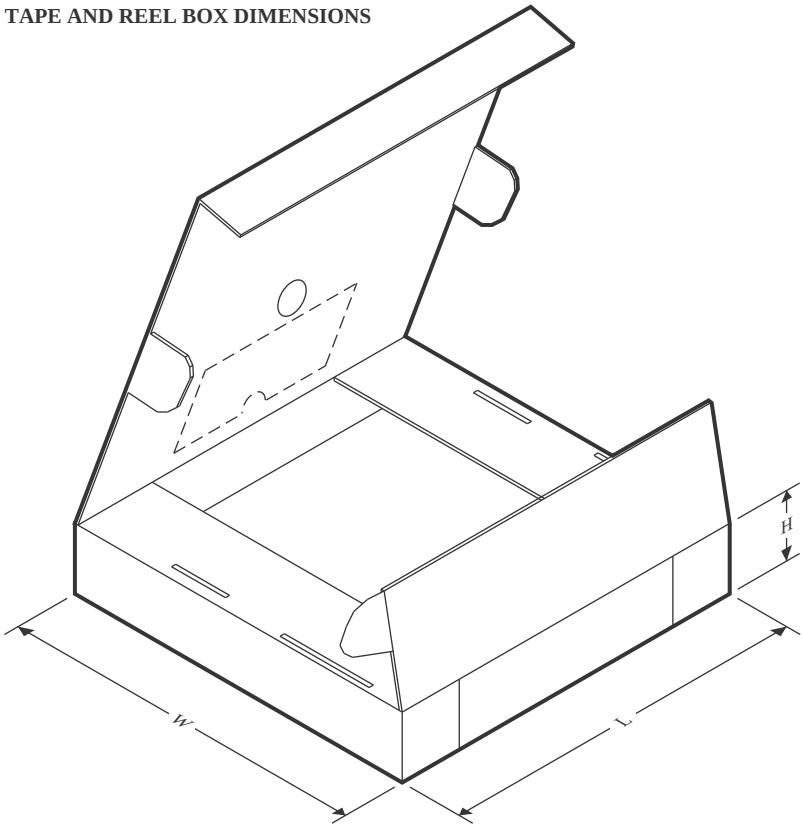
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA240A1DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA240A1DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA240A1PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
INA240A1PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
INA240A2DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA240A2DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA240A2PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
INA240A2PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
INA240A3DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA240A3DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA240A3PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
INA240A3PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
INA240A4DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA240A4PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
INA240A4PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

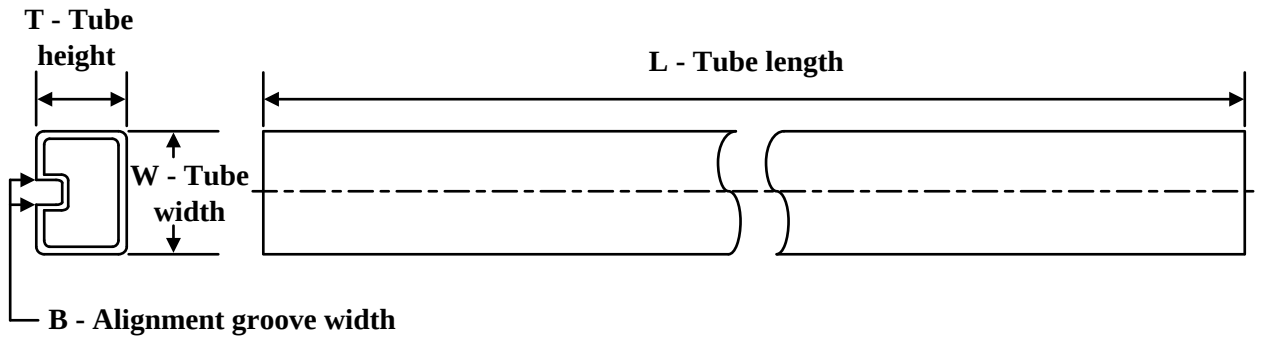
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

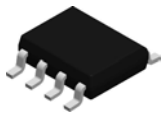
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA240A1DR	SOIC	D	8	2500	353.0	353.0	32.0
INA240A1DRG4	SOIC	D	8	2500	353.0	353.0	32.0
INA240A1PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
INA240A1PWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0
INA240A2DR	SOIC	D	8	2500	353.0	353.0	32.0
INA240A2DRG4	SOIC	D	8	2500	353.0	353.0	32.0
INA240A2PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
INA240A2PWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0
INA240A3DR	SOIC	D	8	2500	353.0	353.0	32.0
INA240A3DRG4	SOIC	D	8	2500	353.0	353.0	32.0
INA240A3PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
INA240A3PWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0
INA240A4DR	SOIC	D	8	2500	353.0	353.0	32.0
INA240A4PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
INA240A4PWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA240A1D	D	SOIC	8	75	507	8	3940	4.32
INA240A1D.A	D	SOIC	8	75	507	8	3940	4.32
INA240A3D	D	SOIC	8	75	507	8	3940	4.32
INA240A3D.A	D	SOIC	8	75	507	8	3940	4.32

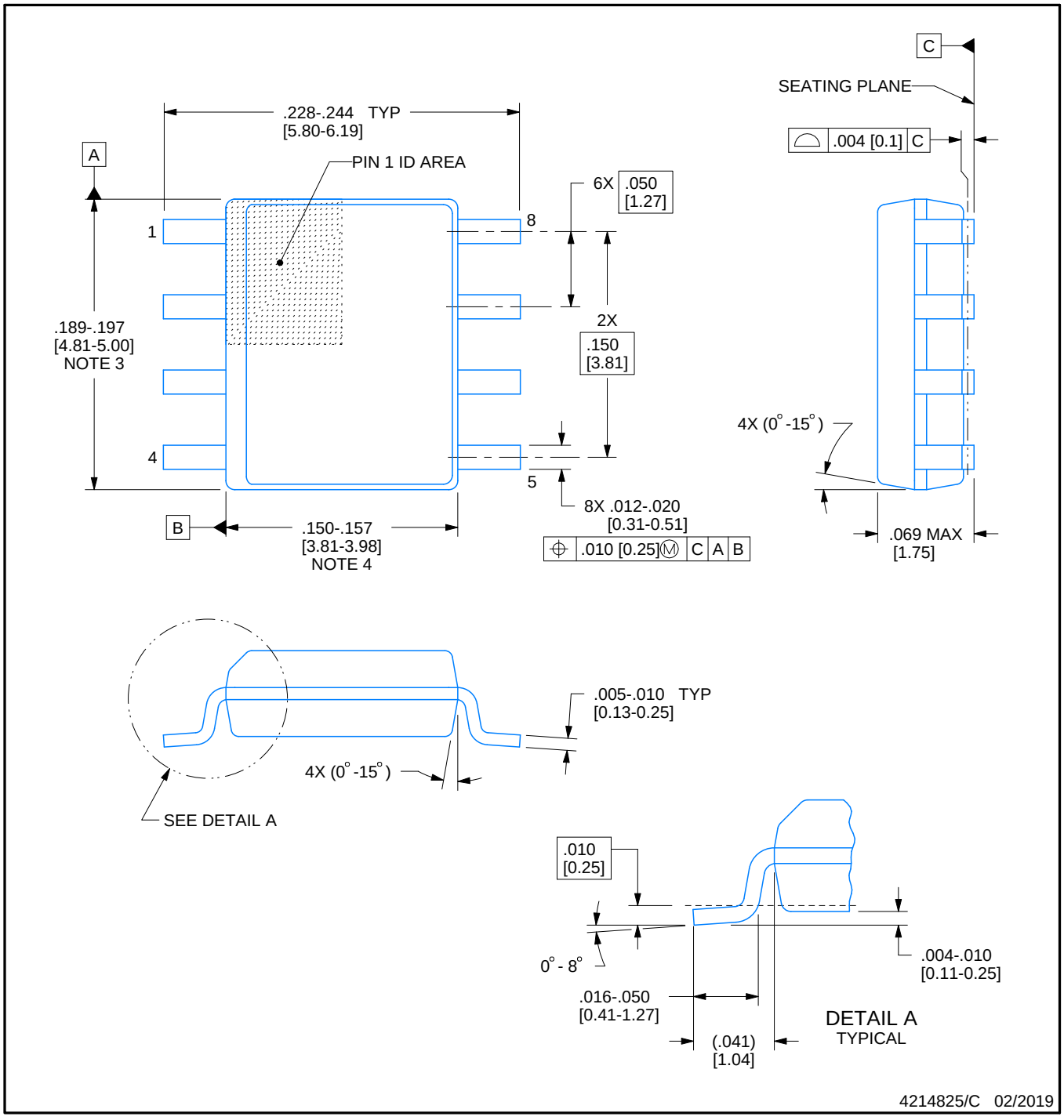


PACKAGE OUTLINE

D0008A

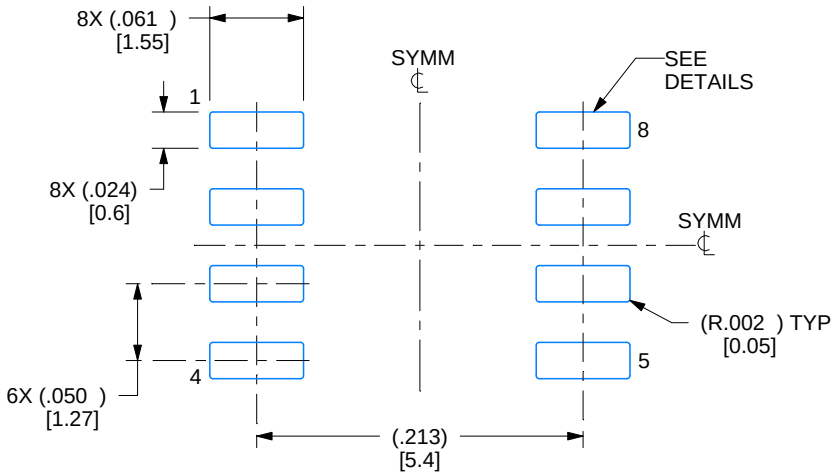
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

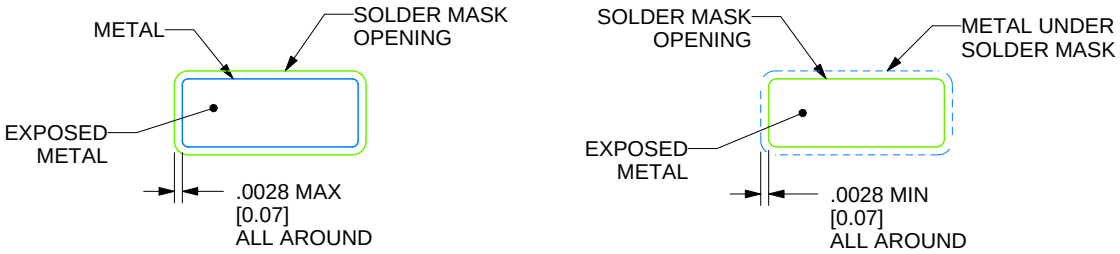


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

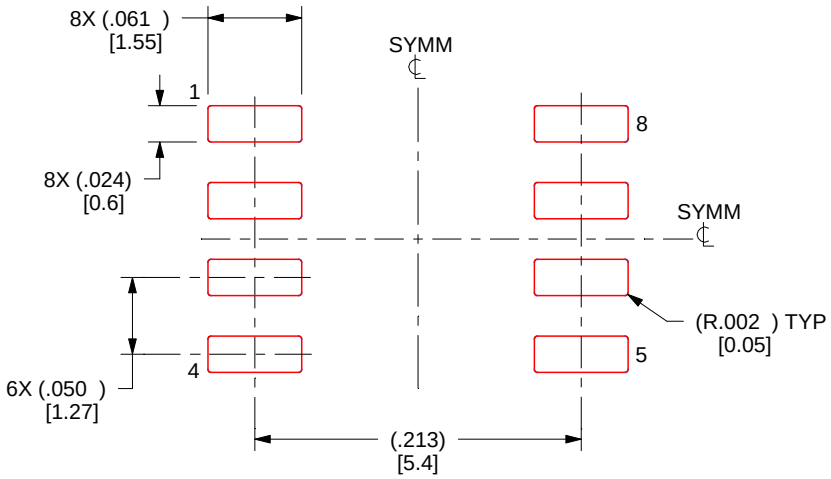
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

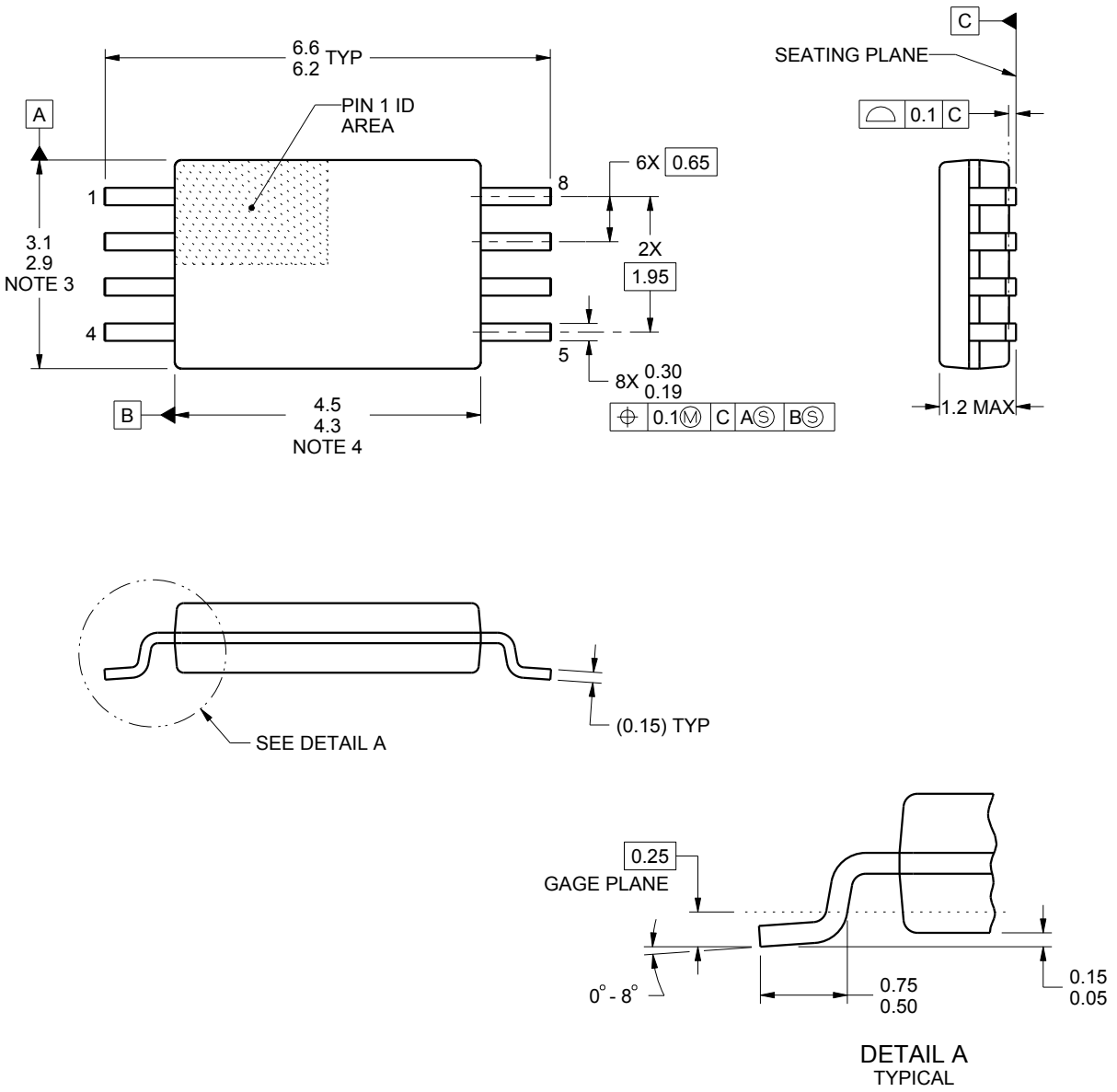
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

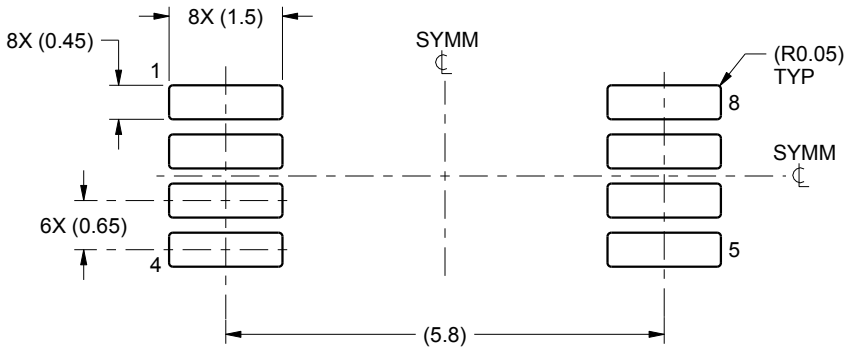
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

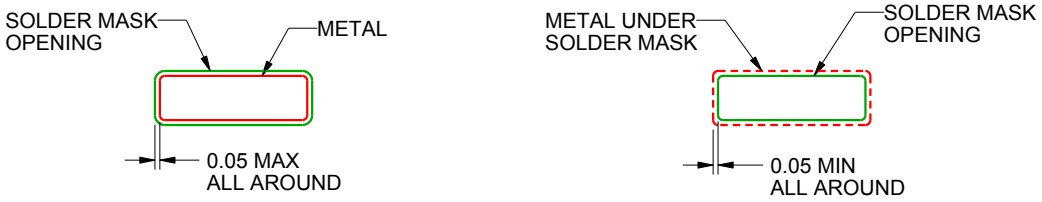


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

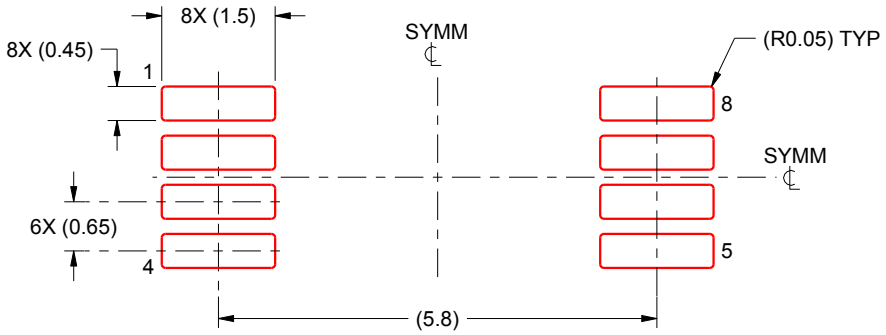


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025