ESD8x2 2-Channel, 36V ESD Protection Diode

1 Features

- Working voltage 36V
- Low leakage current 50nA (maximum)
- IEC 61000-4-2 ESD protection:
  - ±25kV contact, ±25kV air (ESD852 SOT-23)
  - ±20kV contact, ±20kV air (ESD852 DFN1110-3)
  - ±18kV contact, ±18kV air (ESD862)
- IEC 61000-4-5 (8/20µs) Protection:
  - 4.3A (ESD852 SOT-23)
  - 3.8A (ESD852 DFN1110-3)
  - 3.1A (ESD862)
- Bidirectional ESD protection
- Low I/O capacitance:
  - 2.8pF typical (ESD852 SOT-23)
  - 3.0pF typical (ESD852 DFN1110-3)
  - 2.6pF typical (ESD862)
- Leaded packages used for automatic optical inspection (AOI)

2 Applications

- Factory automation
- Communication equipments
- USB power delivery (USB-PD):
  - VBUS protection
  - IO protection (withstand short to VBUS)
- Industrial communications:
  - CAN / CAN-FD

3 Description

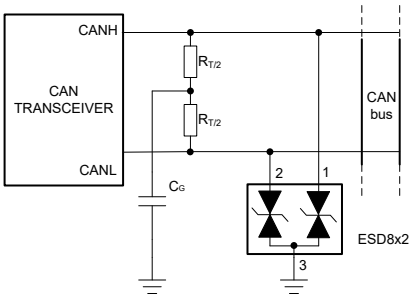
The ESD8x2 devices are bidirectional ESD protection diodes for USB power delivery (USB-PD) and industrial interfaces. The devices are rated to dissipate ESD that meets or exceeds the maximum level specified in the IEC 61000-4-2 standard (±25kV contact and airgap, ±20kV contact and airgap, or ±18kV contact and airgap). The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key because industrial systems require a high level of robustness and reliability.

These devices feature a low IO capacitance per channel and a pin-out to suit two IO lines from damage caused by electrostatic discharge (ESD) and other transients. The I_{PP} = 4.3A (8/20µs surge waveform) capability of the ESD852 makes it an excellent choice for protecting USB VBUS against transient surge events as well as industrial I/O lines. Additionally, the 2.8pF or 2.6pF line capacitance of the ESD8x2 are an excellent choice for protecting the slower speed signals for USB power delivery and IO signals for industrial applications.

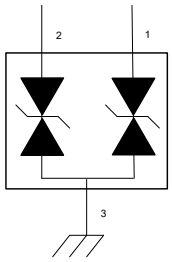
Package Information

PART NUMBER	CHANNEL	PACKAGE(1)
ESD852	2 Channels	DBZ (SOT-23, 3)
		DFN1110-3
ESD862		DBZ (SOT-23, 3)

(1) For more information, see Section 9.



ESD8x2 Typical Application



Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

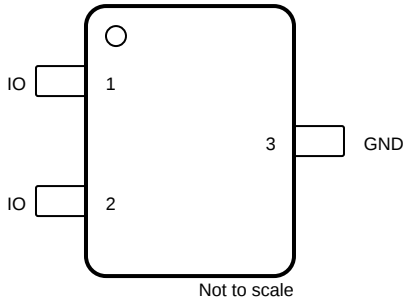


Figure 4-1. DBZ Package, SOT-23 (Top View)

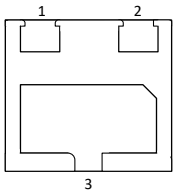


Figure 4-2. DXA Package, DFN1110-3 (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		Device	Package	MIN	MAX	UNIT
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20 µs) at 25°C	ESD852	SOT-23 & DFN1110-3		233	W
			SOT-23		4.3	A
			DFN1110-3		3.8	A
		ESD862	SOT-23		175	W
					3.1	A
T_A	Operating free-air temperature	ESD852, ESD862	SOT-23 & DFN1110-3	-55	150	°C
T_{stg}	Storage temperature	ESD852, ESD862	SOT-23 & DFN1110-3	-65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-36		36	V
T_A	Operating free-air temperature	-55		150	°C

5.3 Thermal Information

THERMAL METRIC		ESD852		ESD862	UNIT
		DBZ (SOT-23)	DXA (DFN1110-3)	DBZ (SOT-23)	
		3 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	295.8	284.2	313.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	146.3	147.9	162.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	134.0	127.4	151.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.6	12.0	43.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	133.1	126.3	150.8	°C/W

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5.4 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	Device	Package	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		ESD852, ESD862	SOT-23 & DFN1110-3	–36		36	V
V_{BRF}	Forward breakdown voltage, any IO pin to GND(1)	I_{IO} = 1mA	ESD852, ESD862	SOT-23 & DFN1110-3	37.8	40	44.2	V
V_{BRR}	Reverse breakdown voltage, any IO pin to GND(1)	I_{IO} = –1mA	ESD852, ESD862	SOT-23 & DFN1110-3	-44.2	-40	-37.8	V
V_{CLAMP}	Clamping voltage(2)	I_{PP} = 1A, t_p = 8/20µs, from IO to GND	ESD852	SOT-23		43		V
		I_{PP} = 4.3A, t_p = 8/20µs, from IO to GND				61		V
		I_{PP} = 16A, TLP, from IO to GND, both Postive & Negative				63		V
		I_{PP} = 1A, t_p = 8/20µs, from IO to GND		DFN1110-3		44		V
		I_{PP} = 3.8A, t_p = 8/20µs, from IO to GND				66		V
		I_{PP} = 16A, TLP, from IO to GND, both Postive & Negative				65		V
		I_{PP} = 1A, t_p = 8/20µs, from IO to GND	ESD862	SOT-23		47		V
		I_{PP} = 3.1A, t_p = 8/20µs, from IO to GND				61		V
		I_{PP} = 16A, TLP, from IO to GND, both Postive & Negative				64		V
I_{LEAK}	Leakage current, any IO pin to GND	V_{IO} = ±36V	ESD852, ESD862	SOT-23 & DFN1110-3			50	nA
R_{DYN}	Dynamic resistance(3)	IO to GND, GND to IO	ESD852, ESD862	SOT-23		0.49		Ω
			ESD852	DFN1110-3		0.65		Ω
C_L	Line capacitance, any IO to GND	V_{IO} = 0V, f = 1MHz, V_{p-p} = 30mV	ESD852	SOT-23		2.8	3.5	pF
				DFN1110-3		3	4	pF
			ESD862	SOT-23		2.6	2.9	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage when 1mA is applied in the positive-going direction, before the device latches into the snapback state.
(2) Device stressed with 8/20µs exponential decay waveform according to IEC 61000-4-5.
(3) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

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5.5 Typical Characteristics – ESD852 (SOT-23)

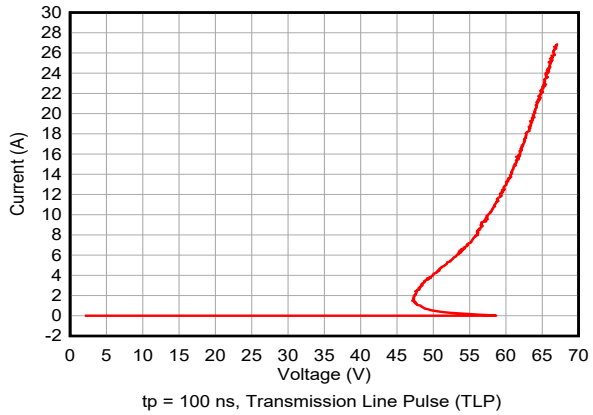


Figure 5-1. Positive TLP Curve

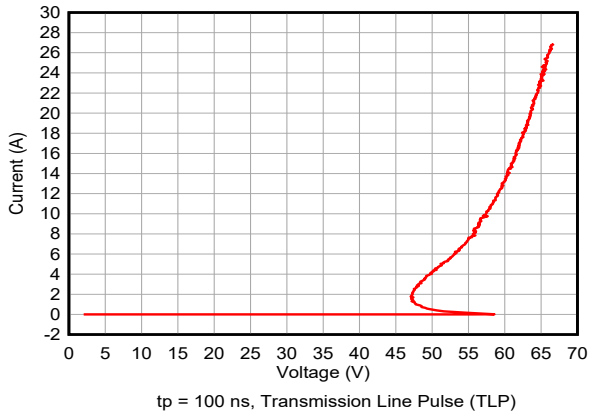


Figure 5-2. Negative TLP Curve

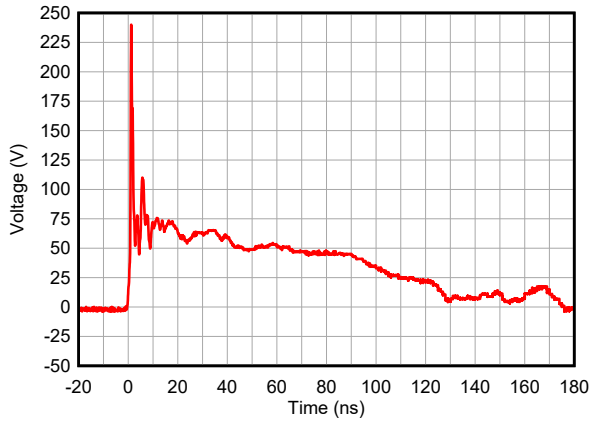


Figure 5-3. +8kV Clamped IEC Waveform

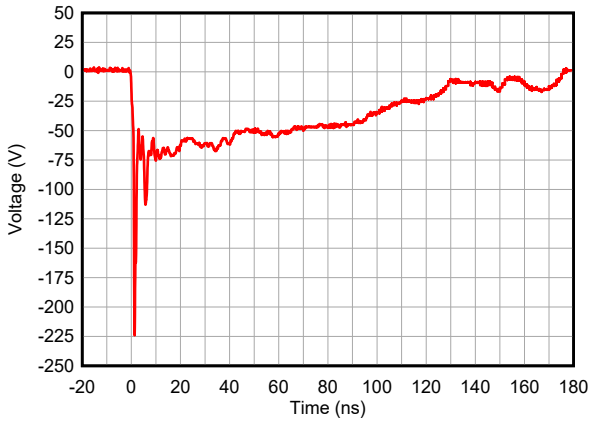


Figure 5-4. −8kV Clamped IEC Waveform

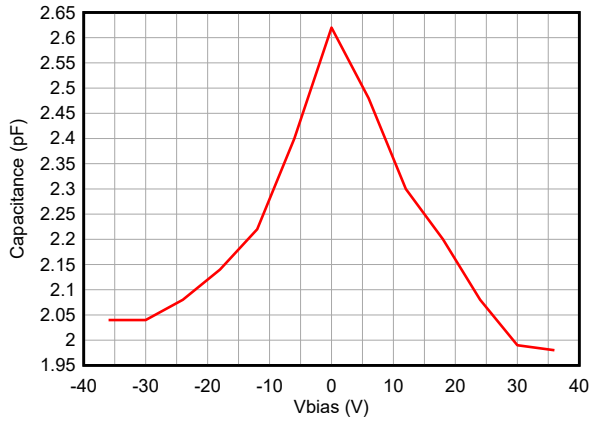


Figure 5-5. Capacitance vs. Bias Voltage

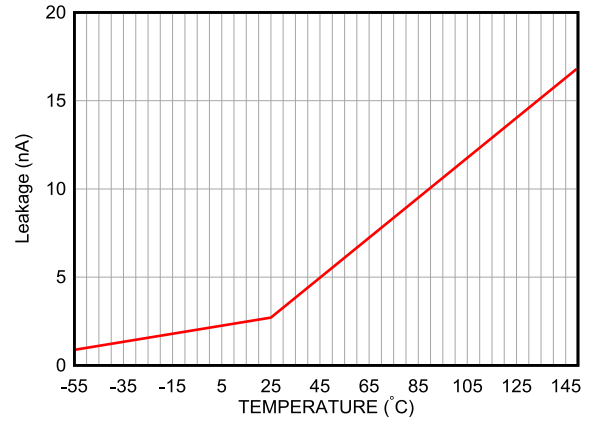


Figure 5-6. Leakage vs. Temperature

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5.6 Typical Characteristics - ESD852 (DFN1110-3)

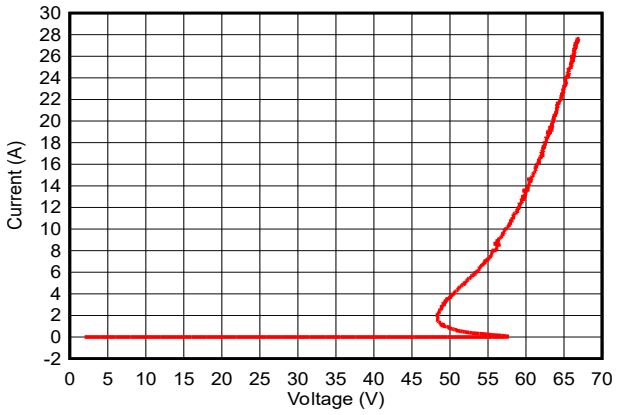


Figure 5-7. Positive TLP Curve

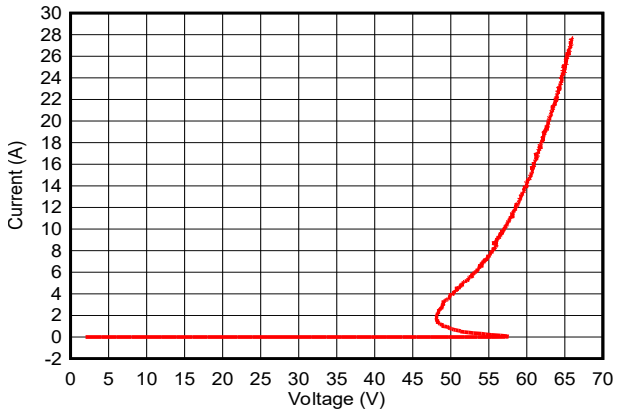


Figure 5-8. Negative TLP Curve

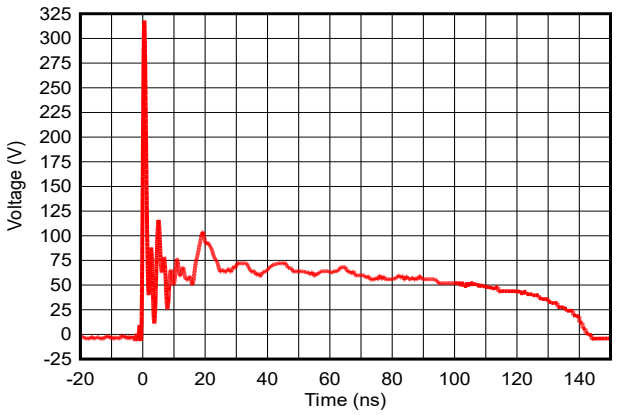


Figure 5-9. +8kV Clamped IEC Waveform

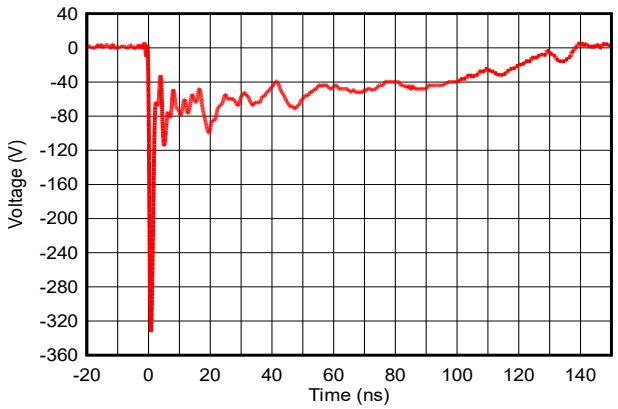


Figure 5-10. -8kV Clamped IEC Waveform

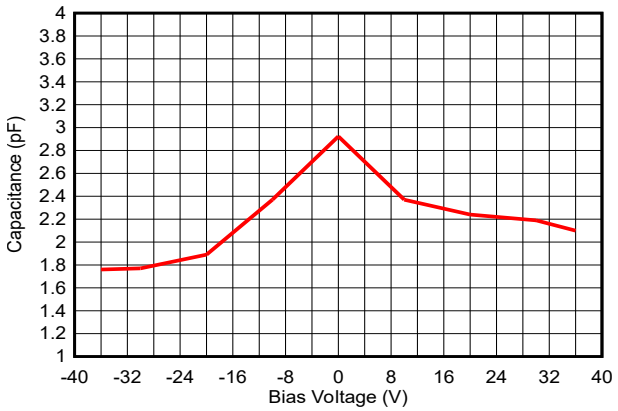


Figure 5-11. Capacitance vs. Bias Voltage

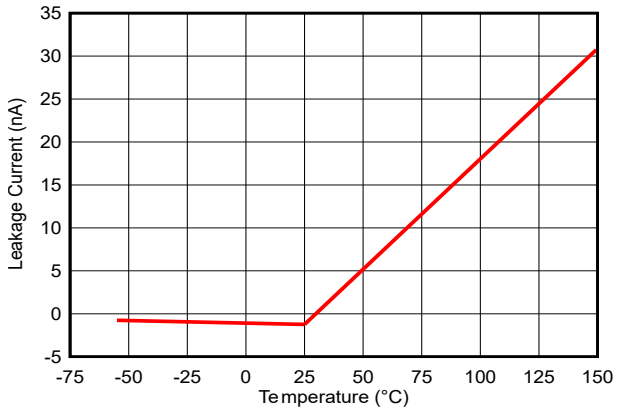


Figure 5-12. Leakage vs. Temperature

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5.7 Typical Characteristics – ESD862

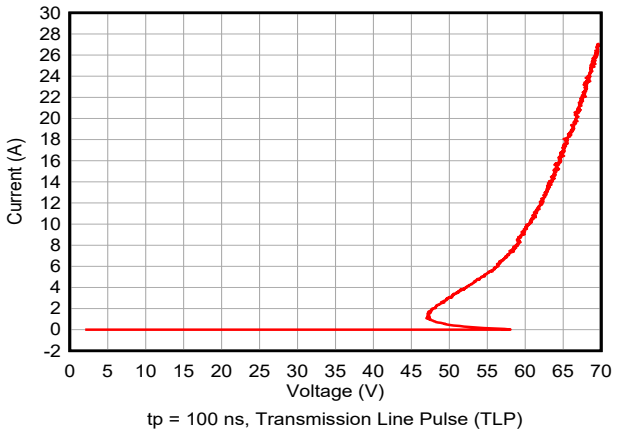


Figure 5-13. Positive TLP Curve

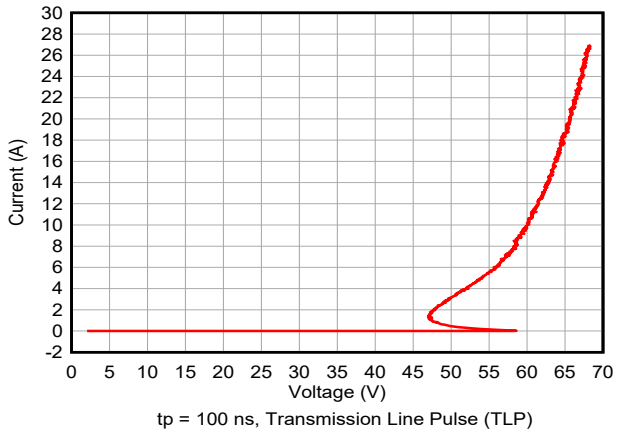


Figure 5-14. Negative TLP Curve

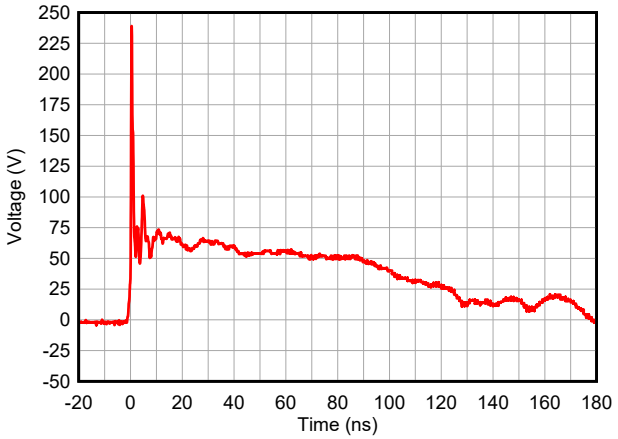


Figure 5-15. +8kV Clamped IEC Waveform

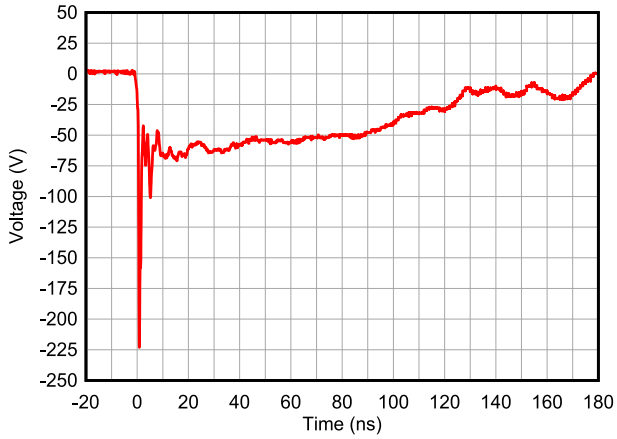


Figure 5-16. -8kV Clamped IEC Waveform

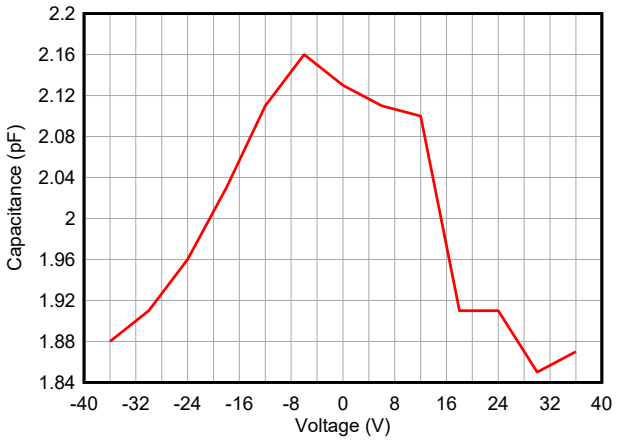


Figure 5-17. Capacitance vs. Bias Voltage

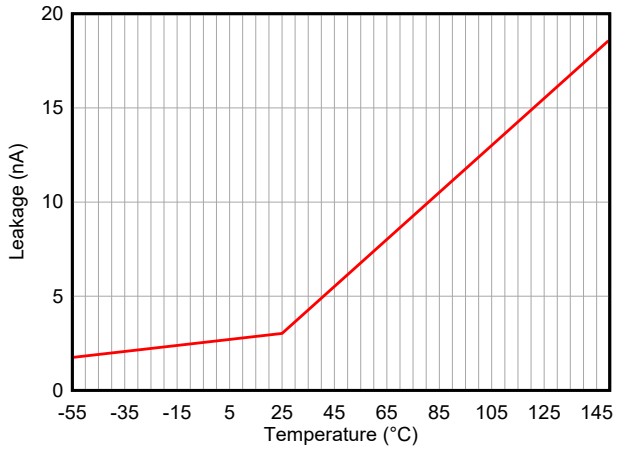


Figure 5-18. Leakage vs. Temperature

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6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The ESD8x2 devices are ESD diodes which provide a path to ground for dissipating transient voltage spikes, such as ESD or surge on signal lines and power lines. Connect the devices in parallel to the down stream circuitry they are protecting. As the current from the transient passes through the ESD device, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered ESD device holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, refer to the *ESD Packaging and Layout Guide*.

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7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD and Surge Protection for USB Interfaces* application note
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2025) to Revision B (January 2026)	Page
• Added DFN package	1

Changes from Revision * (November 2023) to Revision A (June 2025)	Page
• Added DCK package	1

DATE	REVISION	NOTES
November 2023	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD852DBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z38
ESD852DBZR.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z38
ESD852DXAR	Active	Production	USON (DXA) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	1WZ
ESD862DBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z78
ESD862DBZR.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z78

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

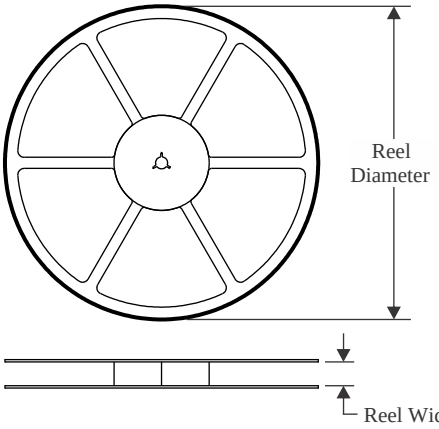
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

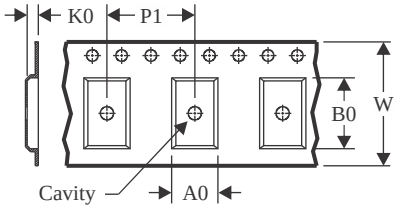
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

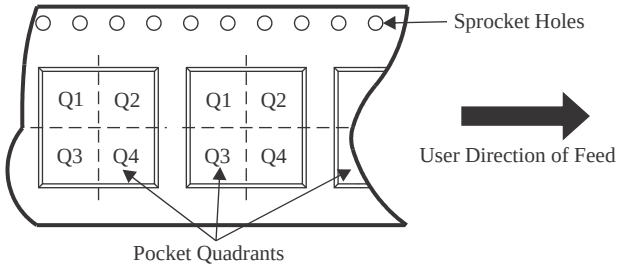


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

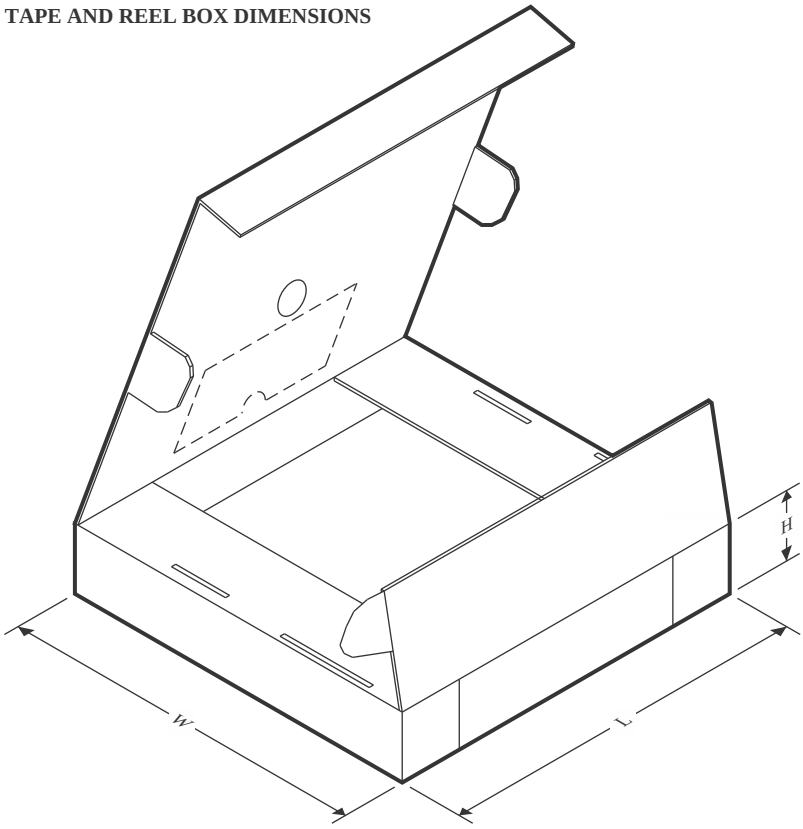
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD852DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
ESD852DXAR	USON	DXA	3	3000	180.0	8.4	1.2	1.3	0.65	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD852DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
ESD852DXAR	USON	DXA	3	3000	210.0	185.0	35.0

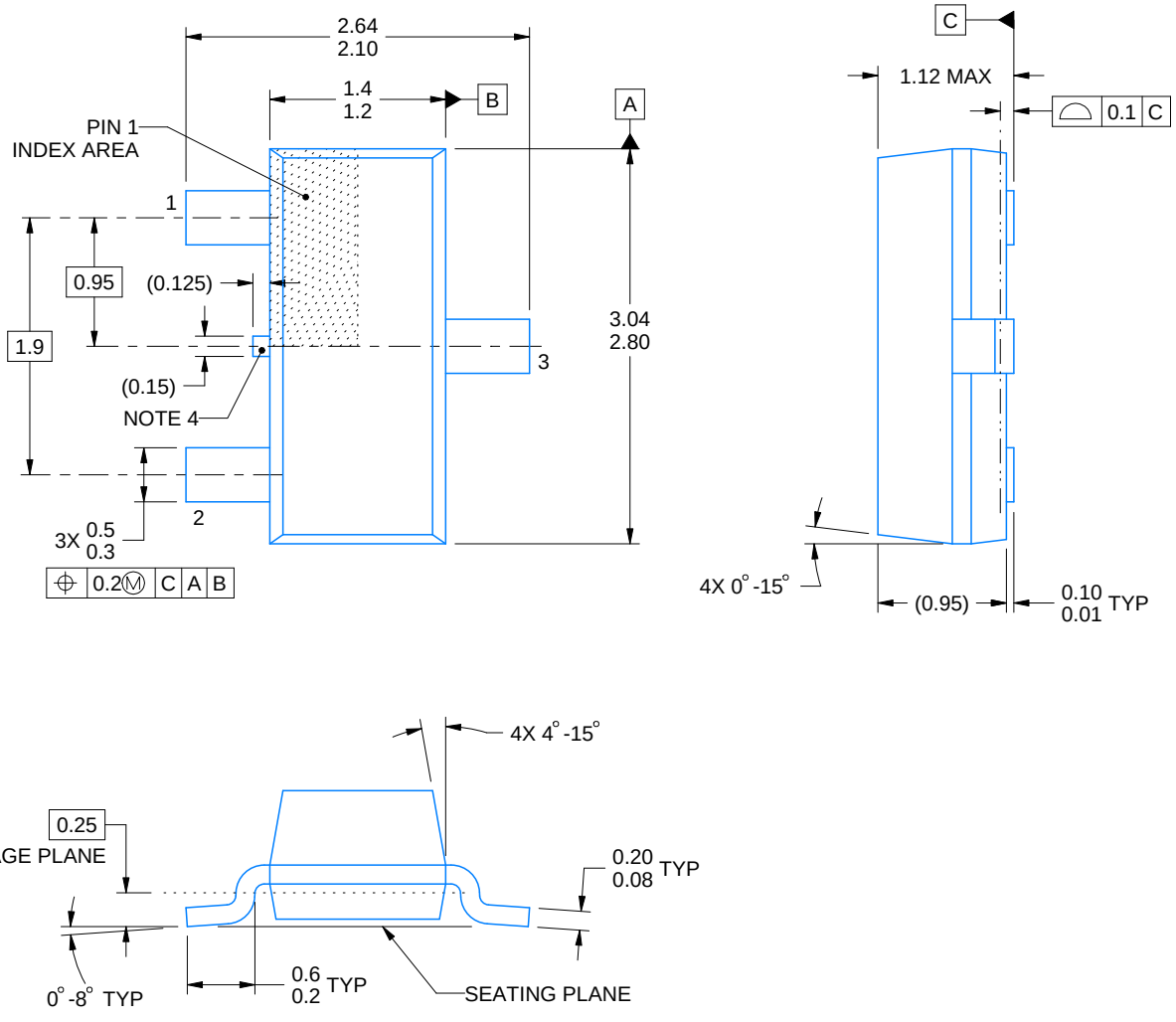
PACKAGE OUTLINE

DBZ0003A



SOT-23 - 1.12 mm max height

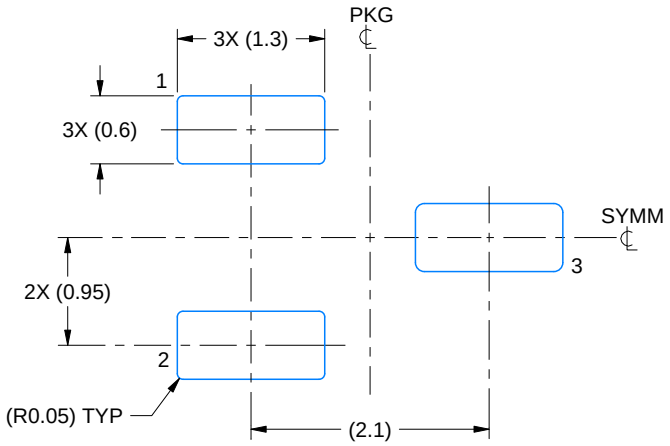
SMALL OUTLINE TRANSISTOR



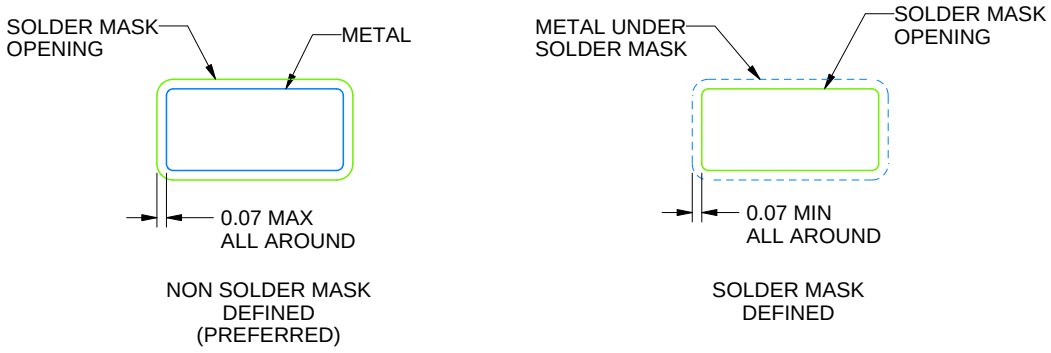
4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X

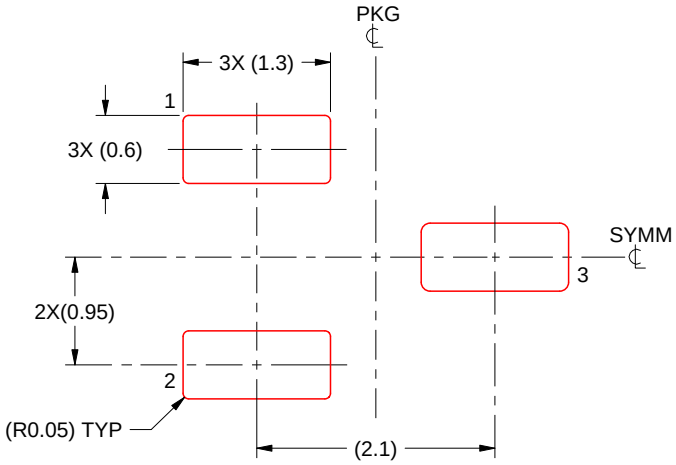


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



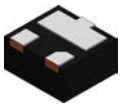
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

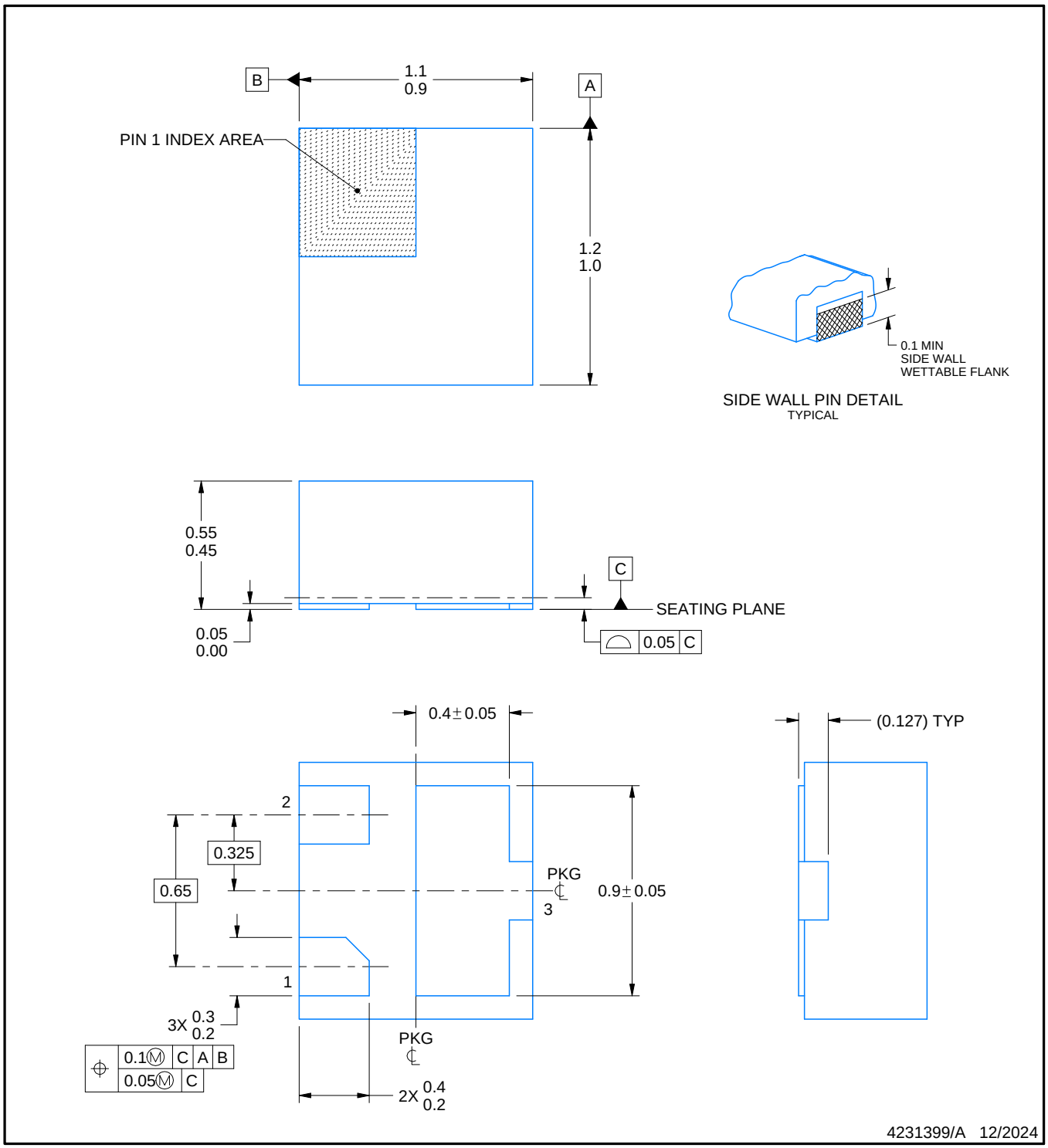
DXA0003A



PACKAGE OUTLINE

USON - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

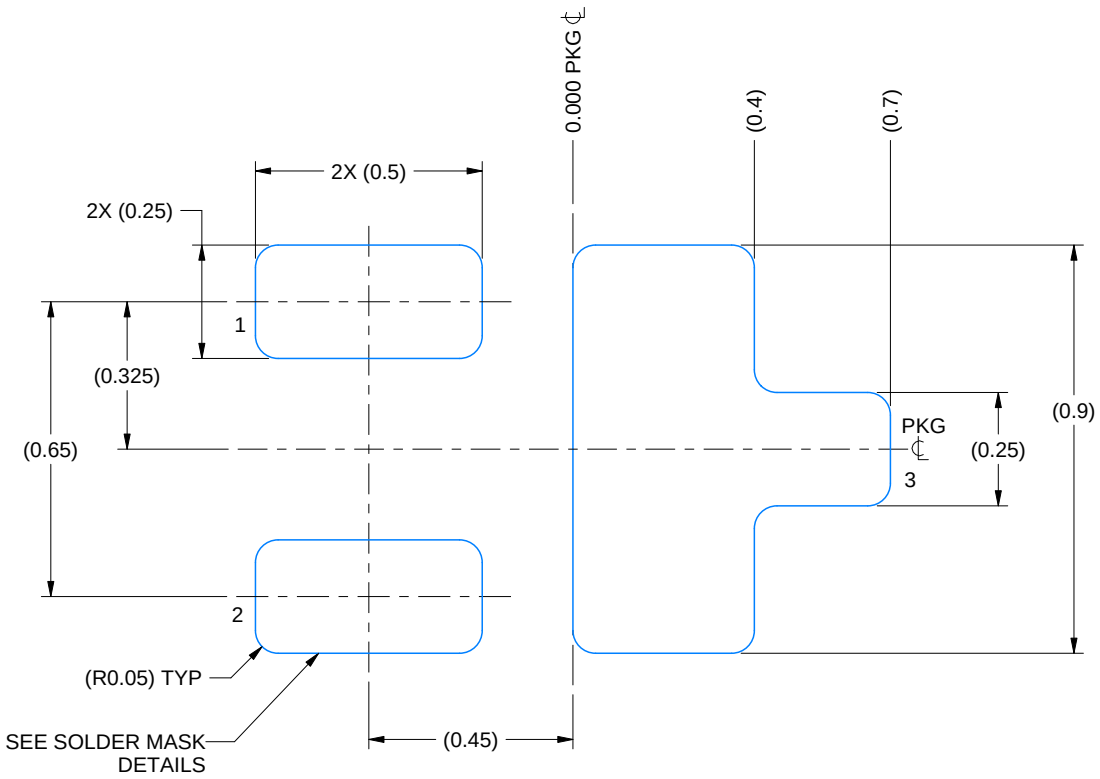
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

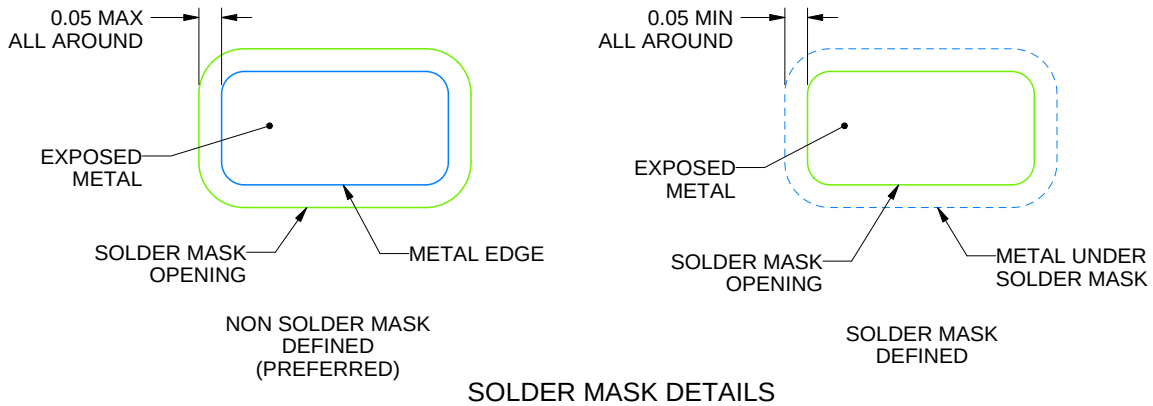
DXA0003A

USON - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 60X



SOLDER MASK DETAILS

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NOTES: (continued)

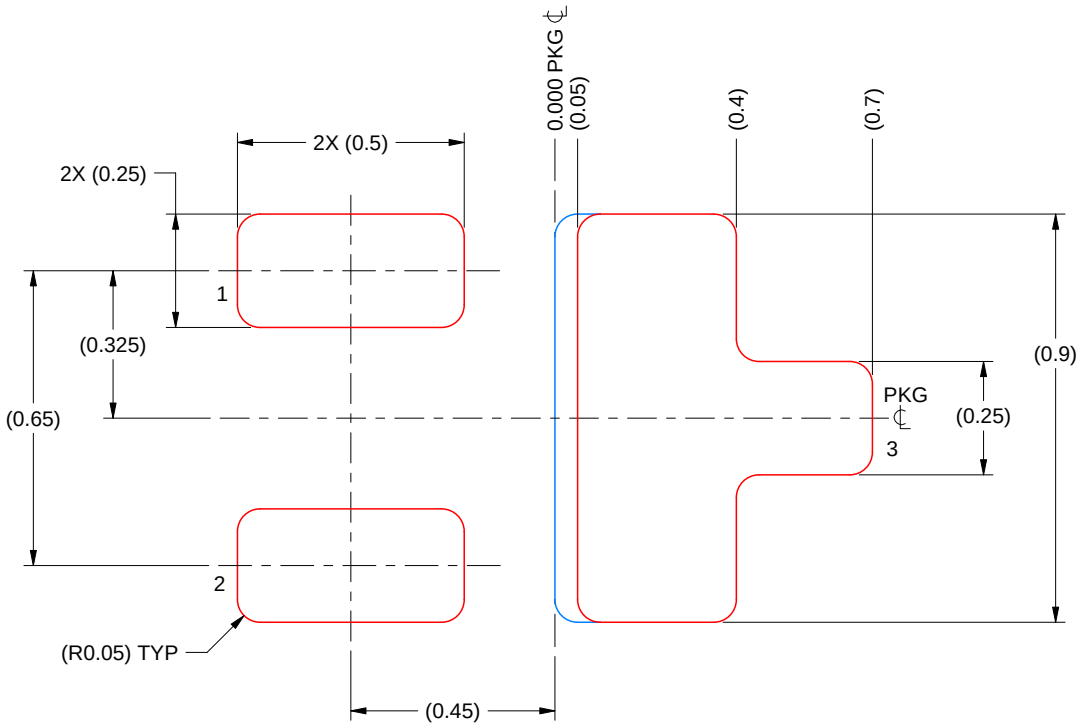
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DXA0003A

USON - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 60X

EXPOSED PAD 3
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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