ESD751 and ESD761 24-V 1-Channel ESD Protection Diodes

1 Features

- IEC 61000-4-2 level 4 ESD protection:
  - ±22-kV or ±15-kV contact discharge
  - ±22-kV or ±15-kV air-gap discharge
- Robust surge protection:
  - IEC 61000-4-5 (8/20 µs): 2.8 A or 1.8 A
- 24-V working voltage
- Bidirectional ESD protection
- Low clamping voltage protects downstream components
- Temperature range: –55°C to +150°C
- I/O capacitance = 1.6 pF or 1.1 pF (typical)
- Offered in a standard leaded package and 0402 footprint package: SOD-523 (DYA) and X1SON (DPY)
- Leaded packages used for automatic optical inspection (AOI)

2 Applications

- USB power delivery (USB-PD)
  - VBUS protection
  - I/O protection
- Industrial control networks:
  - DeviceNet
  - Smart distribution systems
  - 4/20 mA circuits
  - PLC surge protection
  - ADC surge protection

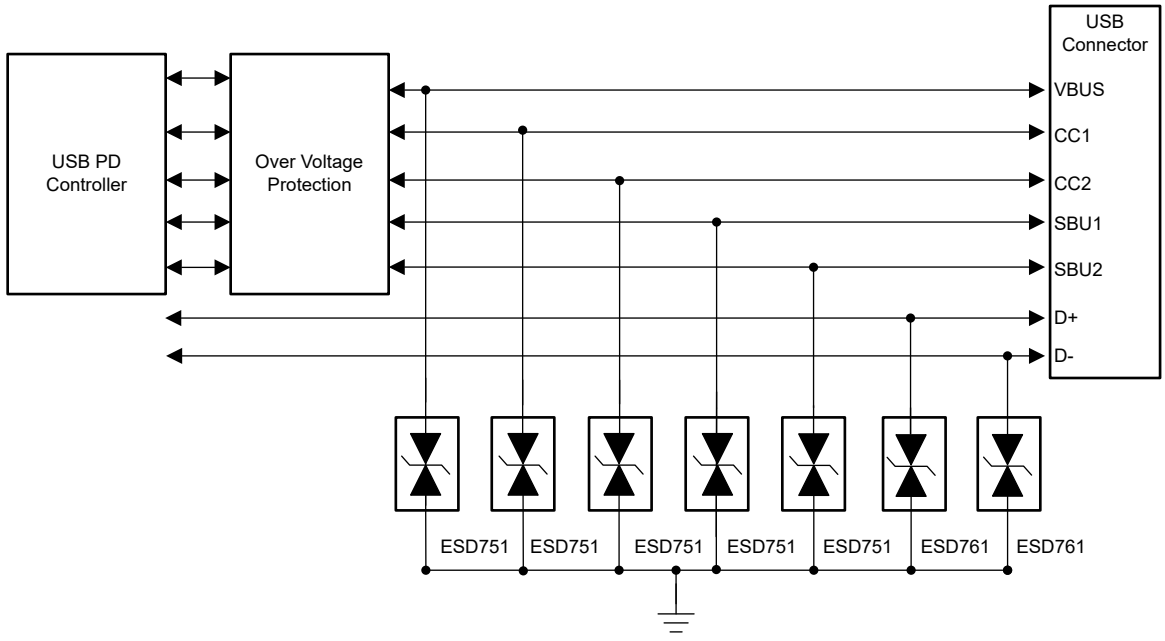
3 Description

The ESD751 and ESD761 are single-channel low capacitance bidirectional ESD protection devices for USB power delivery (USB-PD). These devices are rated to dissipate contact ESD strikes beyond the maximum level specified in the IEC 61000-4-2 international standard (±22-kV Contact, ±22-kV Airgap) and (±15-kV Contact, ±15-kV Airgap), respectively. The low dynamic resistance and low clamping voltage help protect systems against transient events. This protection is key because industrial systems require a high level of robustness and reliability.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ESD751	DYA (SOD-523, 2)	1.60 mm × 0.80 mm
ESD761	DPY (X1SON, 2)	1.00 mm × 0.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2022) to Revision C (December 2022)	Page
• Updated *Thermal Information* table	5

Changes from Revision A (November 2022) to Revision B (December 2022)	Page
• Changed the status of the ESD761 device from: *Advanced Information* to: *Production Data*	1

Changes from Revision * (November 2022) to Revision A (November 2022)	Page
• Changed the status of the ESD751 device from: *Advanced Information* to: *Production Data*	1

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5 Pin Configuration and Functions

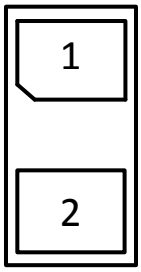


Figure 5-1. DPY Package, 2-Pin X1SON (Top View)

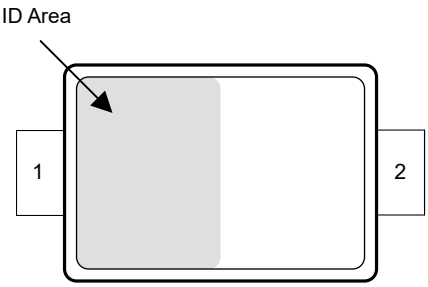


Figure 5-2. DYA Package, 2-Pin SOD523 (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD protected IO
GND	2	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		DEVICE	MIN	MAX	UNIT
P_{PP}	IEC 61000-4-5 Power (t_p - 8/20 µs) at 25°C	ESD751		102	W
		ESD761		65	
I_{PP}	IEC 61000-4-5 current (t_p - 8/20 µs) at 25°C	ESD751		2.8	A
		ESD761		1.8	
T_A	Operating free-air temperature		-55	150	°C
T_J	Junction temperature		-55	150	
T_{stg}	Storage temperature		-65	155	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002(2)	± 1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			DEVICE	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	ESD751	±22000	V
			ESD761	±15000	
		IEC 61000-4-2 Air-gap Discharge, all pins	ESD751	±22000	
			ESD761	±15000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating free-air temperature	-55		150	°C

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6.5 Thermal Information

THERMAL METRIC[1]		ESD751 DYA (SOD-523) 2 PINS	ESD761 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	746.3	282.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	301.2	150.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	509.6	98.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	81.8	9.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	503.0	97.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage			–24		24	V
V_{BRF}	Breakdown voltage[1]	I_{IO} = 10 mA, IO to GND		25.5		35.5	V
V_{BRR}		I_{IO} = –10 mA, IO to GND		–35.5		–25.5	
V_{CLAMP}	Clamping voltage[2]	I_{PP} = 2.8 A, t_p = 8/20 µs, IO to GND and GND to IO	ESD751		36.5		V
		I_{PP} = 1.8 A, t_p = 8/20 µs, IO to GND and GND to IO	ESD761		36.3		
	Clamping voltage[3]	I_{PP} = 16 A, TLP, IO to GND and GND to IO	ESD751		41.5		V
			ESD761		42.5		
I_{LEAK}	Leakage current	V_{IO} = ±24 V, IO to GND		-50	1	50	nA
R_{DYN}	Dynamic resistance[3]		ESD751		0.6		Ω
			ESD761		0.53		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, V_{pp} = 30 mV, IO to GND	ESD751		1.6	2.7	pF
			ESD761		1.1	1.8	

(1) V_{BRF} and V_{BRR} are defined as the voltage when ±10 mA is applied in the positive-going direction, before the device latches into the snapback state.
(2) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
(3) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

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6.7 Typical Characteristics – ESD751

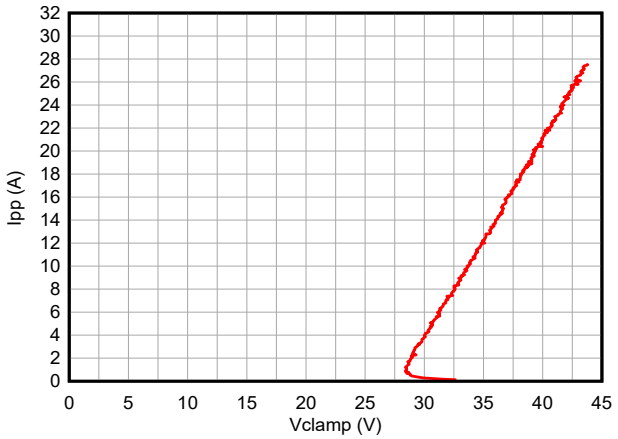


Figure 6-1. Positive TLP Curve

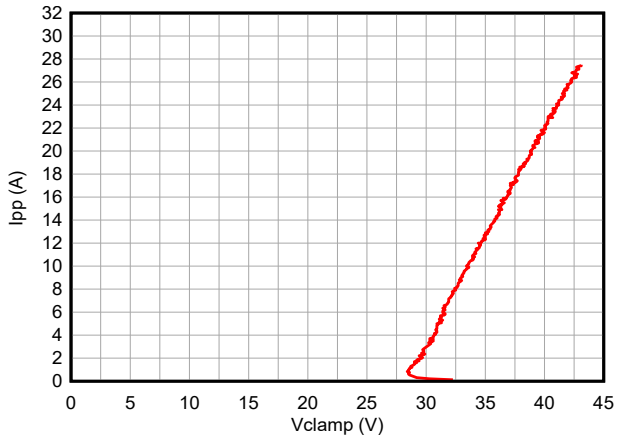


Figure 6-2. Negative TLP Curve

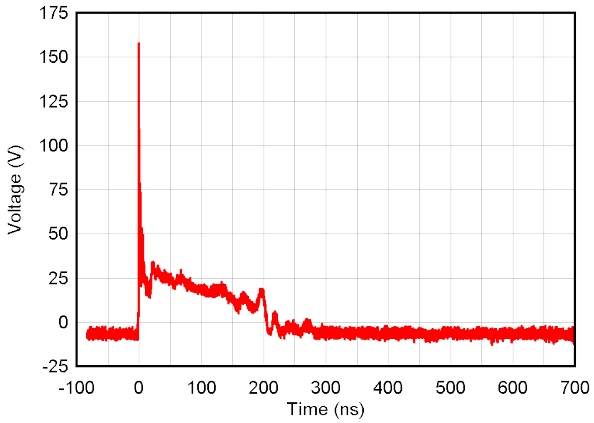


Figure 6-3. +8-kV Clamped IEC Waveform

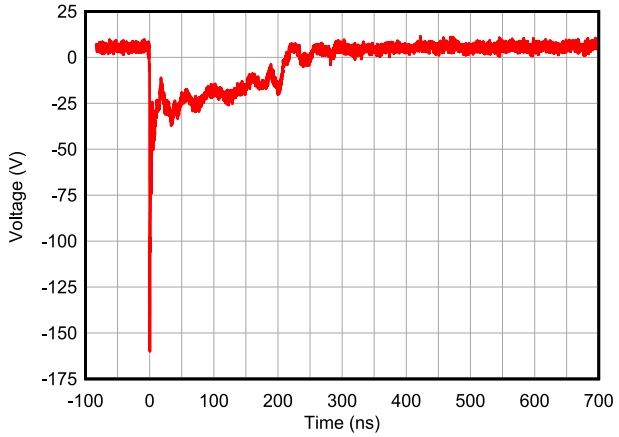


Figure 6-4. -8-kV Clamped IEC Waveform

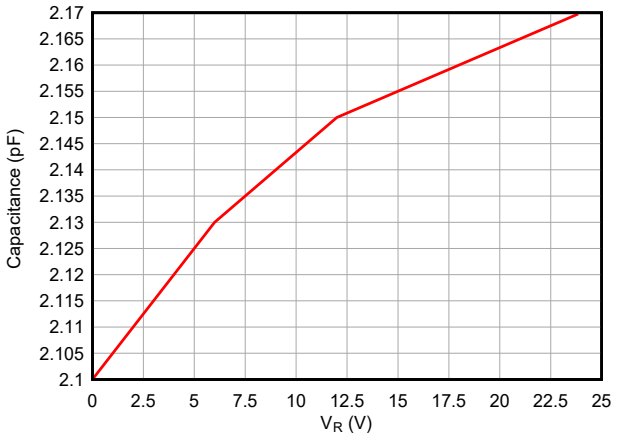


Figure 6-5. Capacitance vs. Bias Voltage

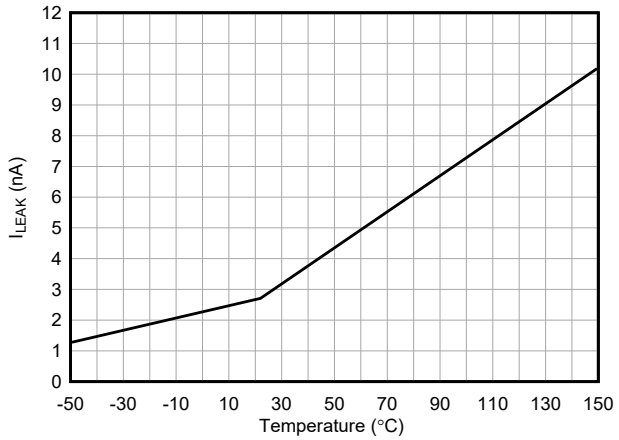


Figure 6-6. Leakage Current vs. Temperature

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6.8 Typical Characteristics - ESD761

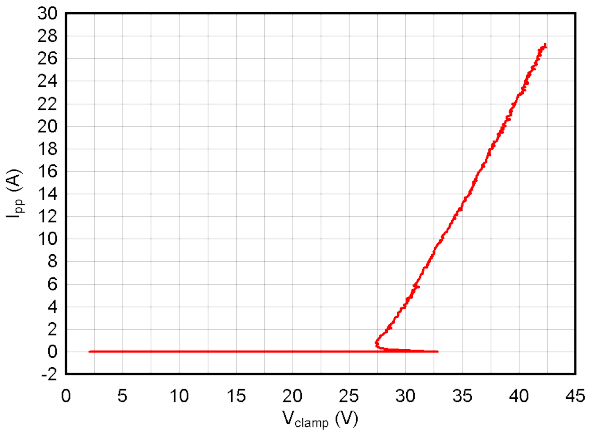


Figure 6-7. Positive TLP Curve

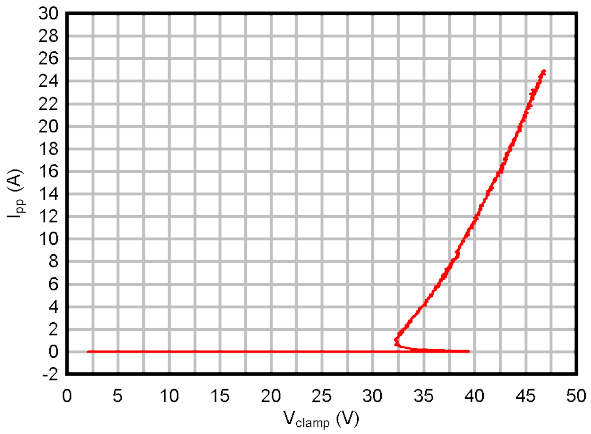


Figure 6-8. Negative TLP Curve

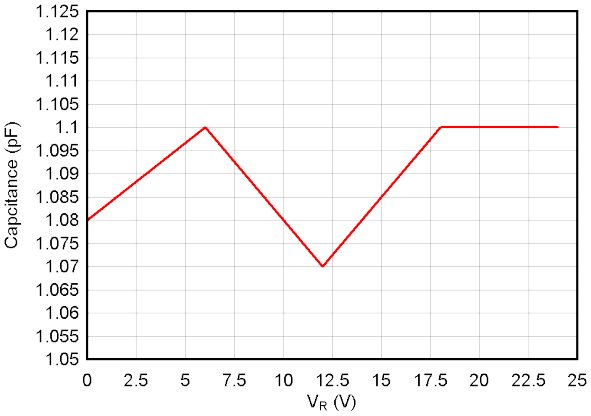


Figure 6-9. Capacitance vs. Bias Voltage

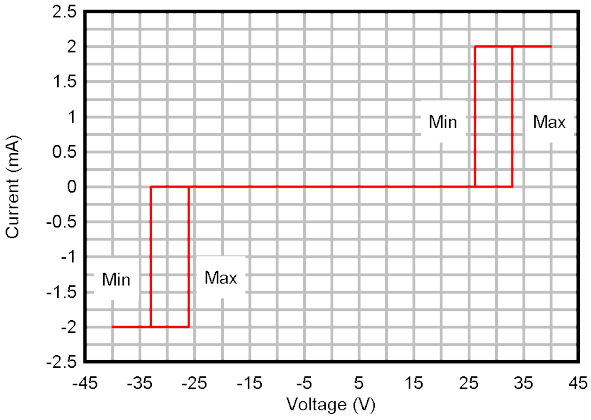


Figure 6-10. DC Voltage Sweep I-V Curve

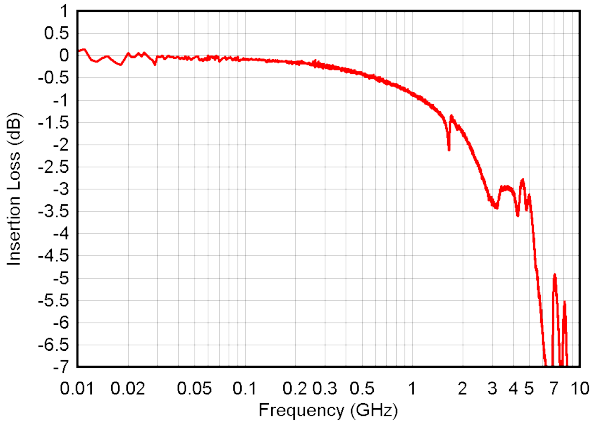


Figure 6-11. Insertion Loss

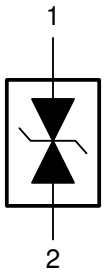
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7 Detailed Description

7.1 Overview

The ESD751 and ESD761 are single-channel bidirectional ESD diodes. These devices can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 standard. The low capacitance between the I/O pins makes these devices suitable for slower speed signals such as USB-PD or industrial I/O applications. The surge current capability is suitable for VBUS protection or industrial I/Os requiring 2.8 A of surge current protection.

7.2 Functional Block Diagram



7.3 Feature Description

These clamping devices have a small dynamic resistance, which makes the clamping voltage low when the devices are actively protecting other circuits. The breakdown is bidirectional so these protection devices are a good fit for applications requiring postive and negative polarity protection. Low leakage allows the diode to conserve power when working below the V_{RWM}. The temperature range of −55°C to +150°C makes these ESD devices work at extensive temperatures in most environments. The leaded SOD-523 package is good for applications requiring autmotic optical inspection (AOI).

7.3.1 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.8 A and 1.8 A (8/20 µs waveform) for the ESD751 and ESD761 respectively.

7.3.2 I/O Capacitance

The capacitance between the I/O pins is 1.6 pF and 1.1 pF for the ESD751 and ESD761 respectively. The capacitance of these devices support data rates up to 1 Gbps.

7.4 Device Functional Modes

The ESD751 and ESD761 are single channel passive clamps that have low leakage during normal operation when the voltage between I/O and GND is below V_{RWM}, and activate when the voltage between I/O and GND goes above V_{BR}. When the voltages on the protected lines fall below the V_{HOLD}, the device reverts back to the low leakage passive state

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ESD751 and ESD761 are single channel TVS diodes which are used to provide a path to ground for dissipating ESD events on USB-PD or industrial I/O lines. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

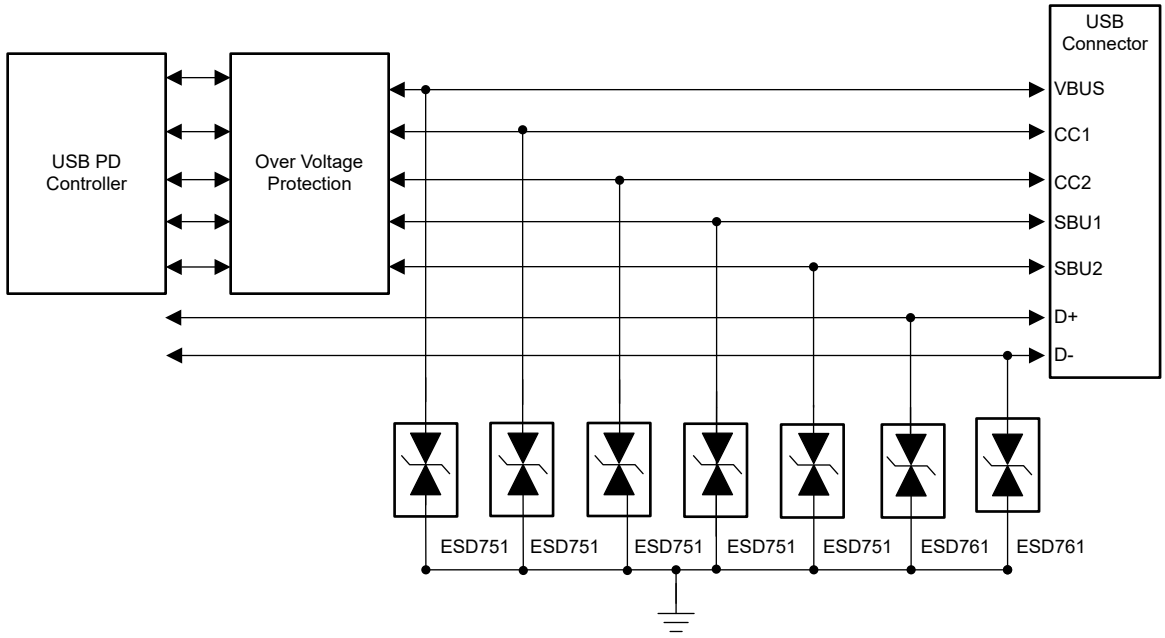


Figure 8-1. Typical Application

8.2.1 Design Requirements

For this design example, the ESD751 and ESD761 are used to provide ESD protection on a USB-PD connector. Table 8-1 lists the known design parameters for this application.

Table 8-1. Design Parameters for Typical Applications

Design Parameter	Value
Diode configuration	Bidirectional
VBUS Voltage	+ 20 V
V_{IO} differential signal range	±3.3 V
V_{RWM}	±24 V
Short to VBUS event on V_{IO}	±20 V
Data rate	Up to 480 Mbps

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8.2.2 Detailed Design Procedure

The ESD751 and ESD761 have a V_{RWM} of ±24 V to protect the diode from being damaged during a short event that can occur when one of the USB-PD slower speed lines (CC1, CC2, SBU1, SBU2, D+, and D-) is shorted to VBUS. The bidirectional characteristic ensures both positive and negative polarity are protected. The low capacitance of 1.7 pF or less permits data rates up to 480 Mbps, which allows the designer to meet the requirements for the D+ and D- signals. These devices have an IPP = 2.8 A and 1.8 A (8/20 µs), respectively. The surge current capability of these devices is suitable for protecting the VBUS power rail.

8.2.2.1 Application Curves

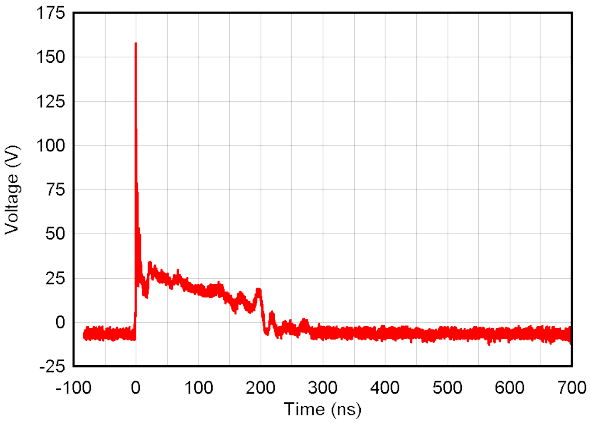


Figure 8-2. +8-kV Clamped IEC Waveform

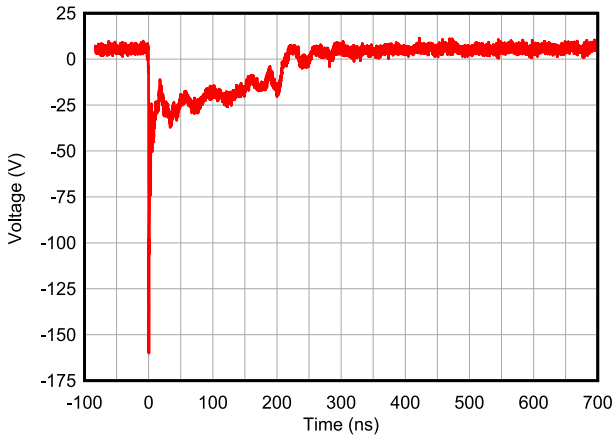


Figure 8-3. −8-kV Clamped IEC Waveform

9 Power Supply Recommendations

These devices are passive TVS diode-based ESD protection devices, therefore there is no requirement to power them. Ensure that the maximum voltage specifications for each pin is not violated.

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10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or 2 is connected to ground, use a thick and short trace for this return path.

10.2 Layout Example

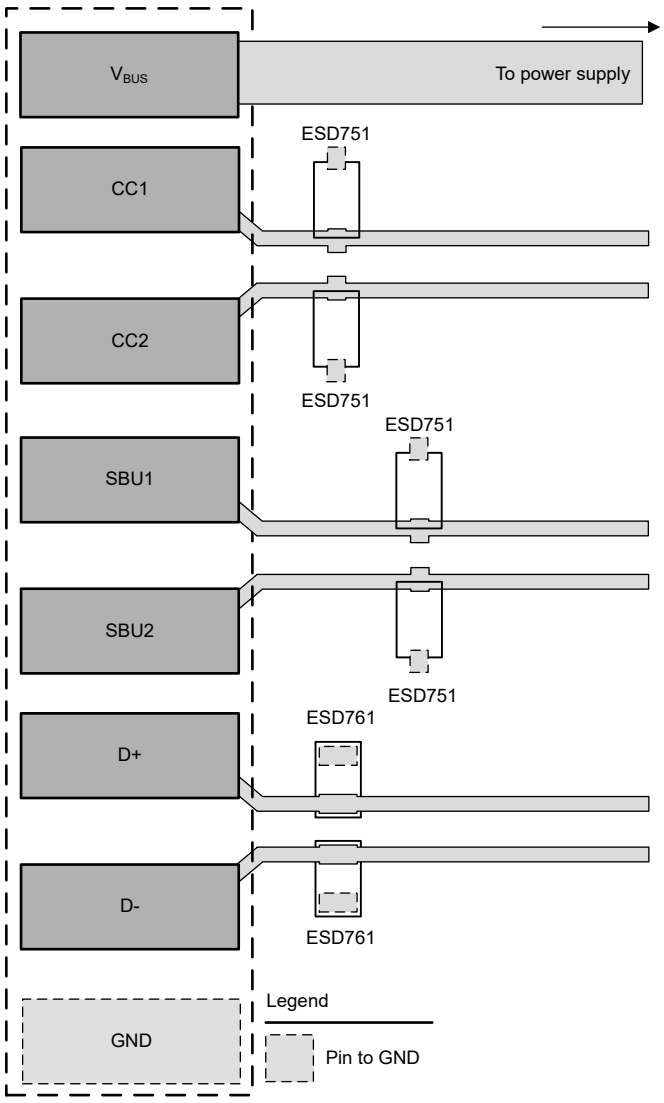


Figure 10-1. Layout Recommendation

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Picking ESD Diodes for Ultra High-Speed Data Lines* application reports
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD751DYAR	Active	Production	SOT-5X3 (DYA) | 2	8000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	1MN
ESD751DYAR.B	Active	Production	SOT-5X3 (DYA) | 2	8000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	1MN
ESD761DPYR	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-55 to 150	NE
ESD761DPYR.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	NE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ESD751, ESD761 :

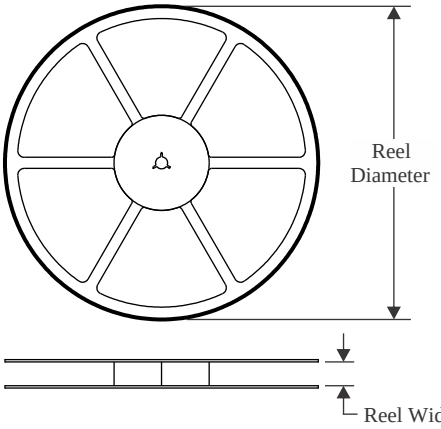
- Automotive : ESD751-Q1, ESD761-Q1

NOTE: Qualified Version Definitions:

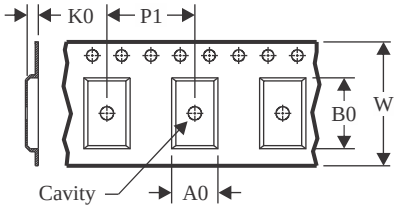
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

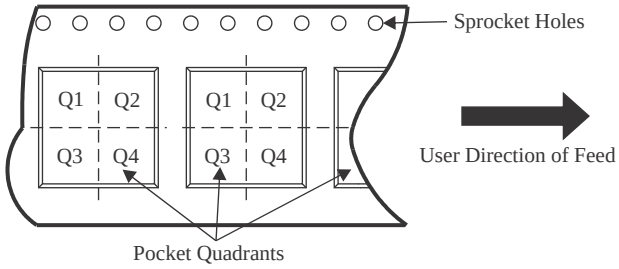


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

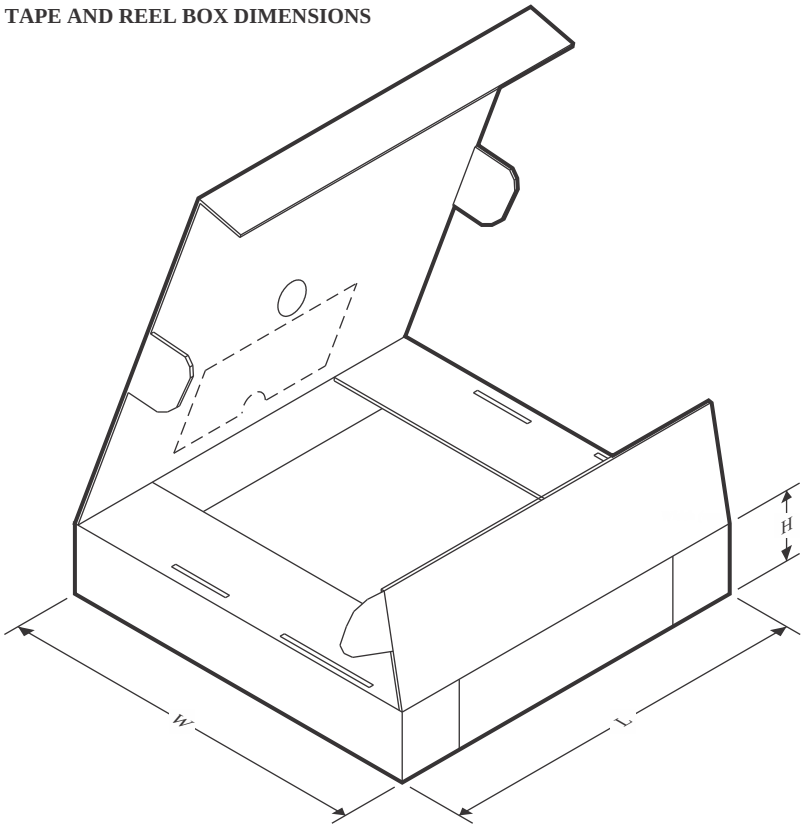
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD751DYAR	SOT-5X3	DYA	2	8000	178.0	9.5	0.5	1.94	0.73	2.0	8.0	Q1
ESD761DPYR	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD751DYAR	SOT-5X3	DYA	2	8000	210.0	200.0	42.0
ESD761DPYR	X1SON	DPY	2	10000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



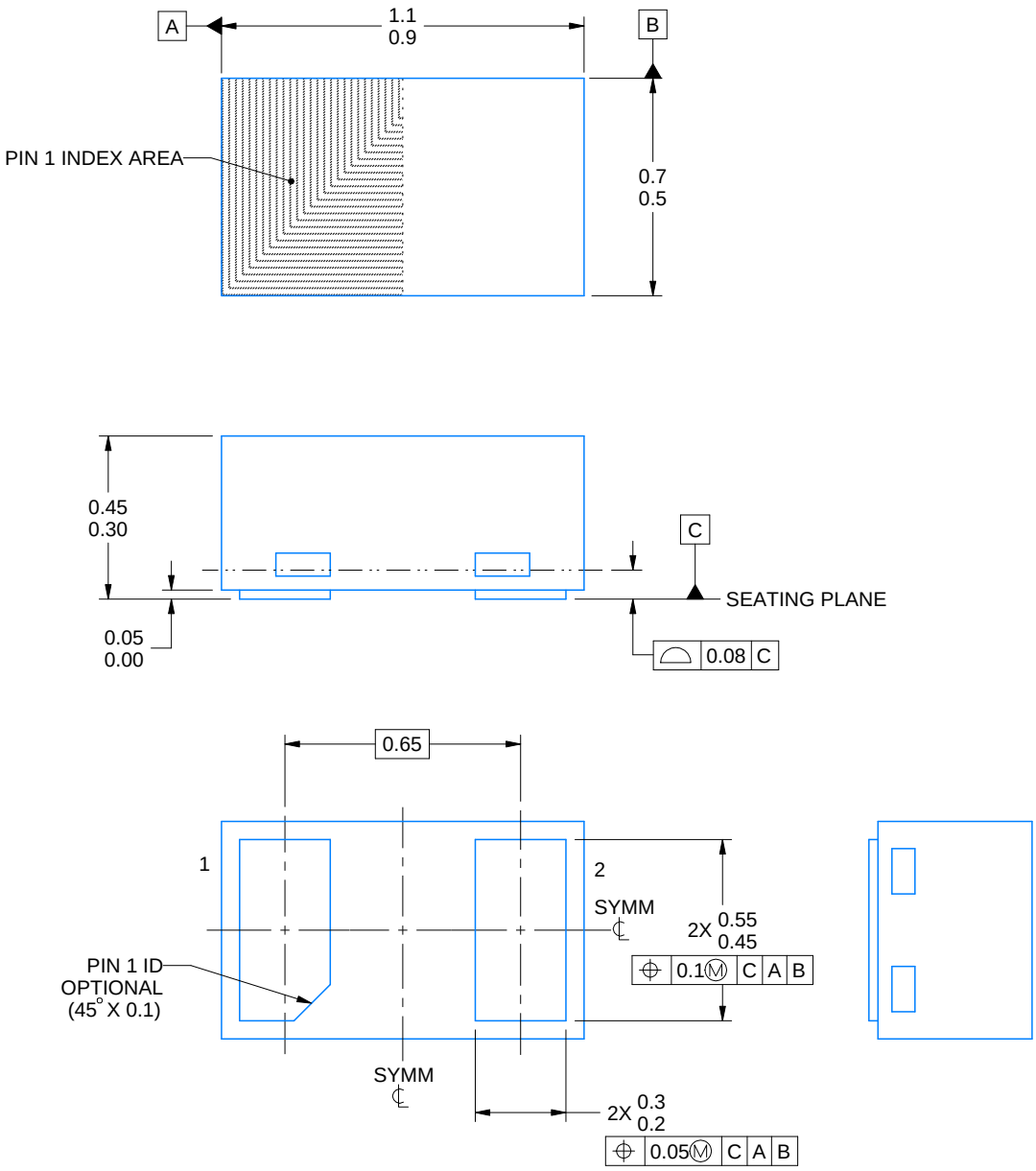
4231484/A

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

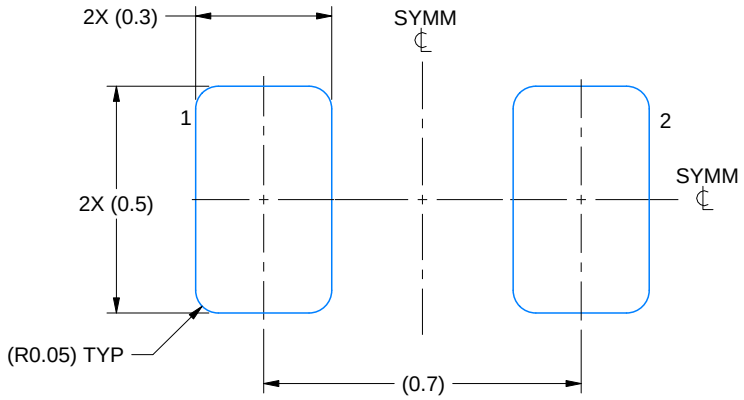
PLASTIC SMALL OUTLINE - NO LEAD



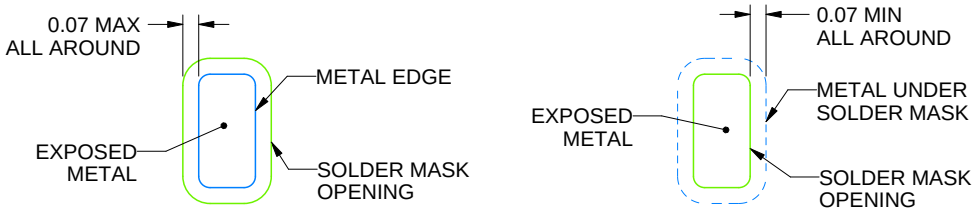
4224561/C 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

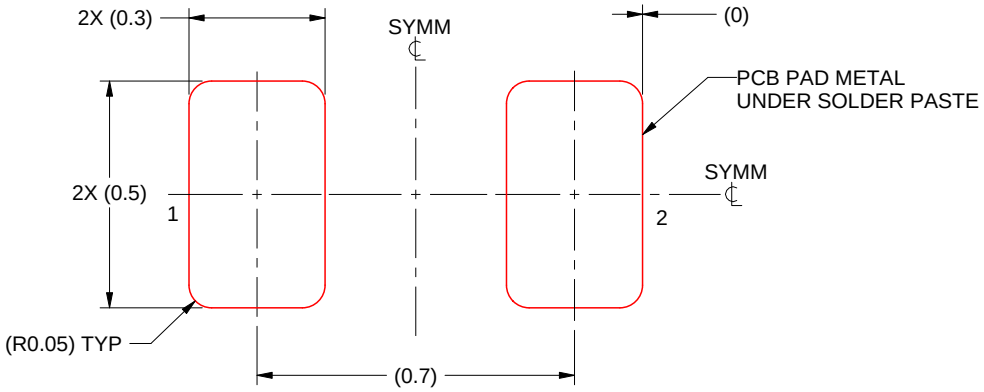


SOLDER MASK DETAILS

4224561/C 07/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/C 07/2024

NOTES: (continued)

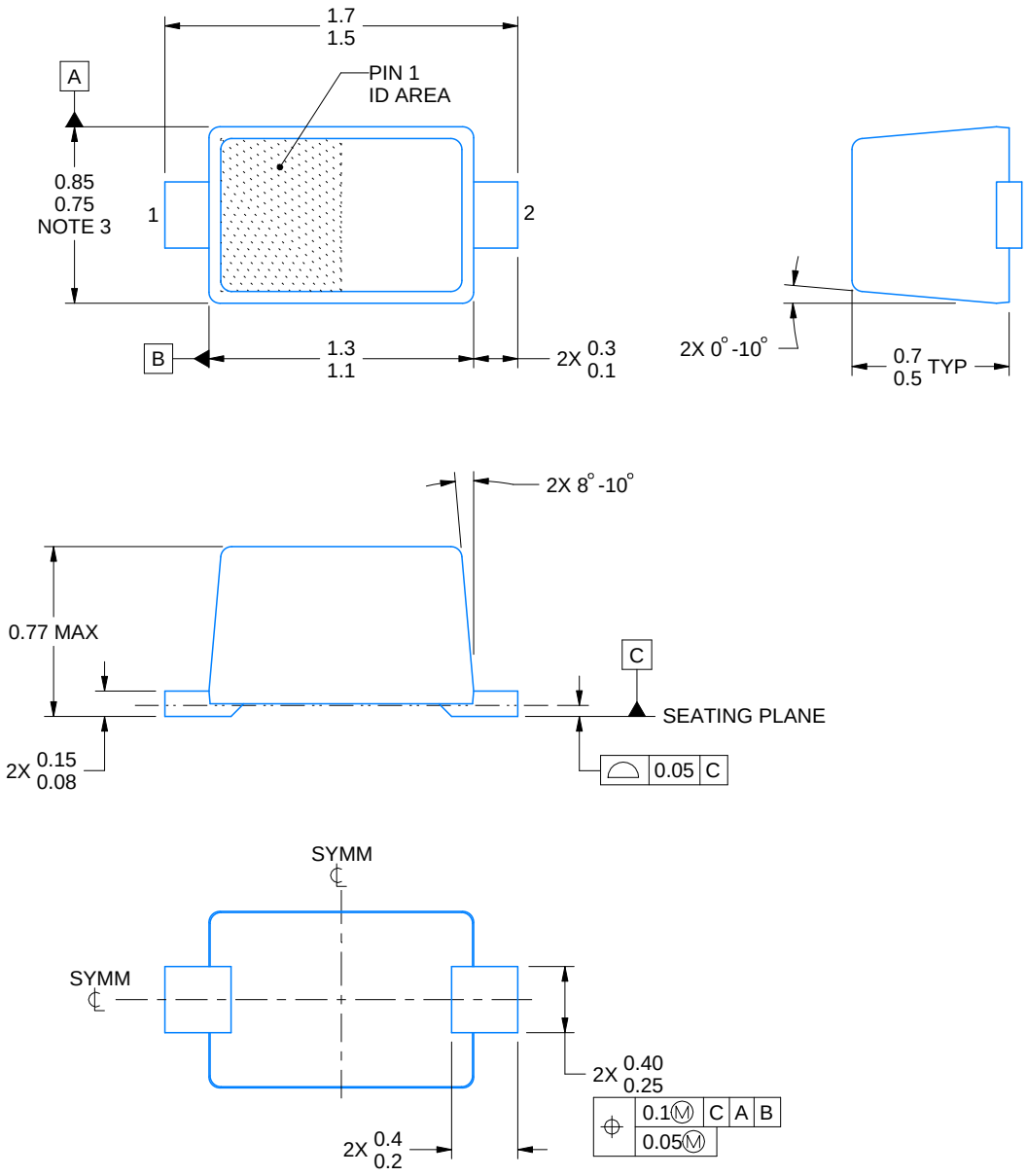
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYA0002A

SOT (SOD-523) - 0.77 mm max height

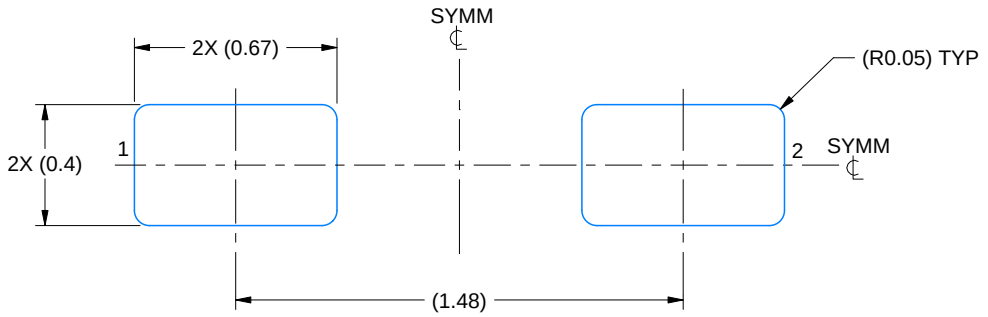
PLASTIC SMALL OUTLINE



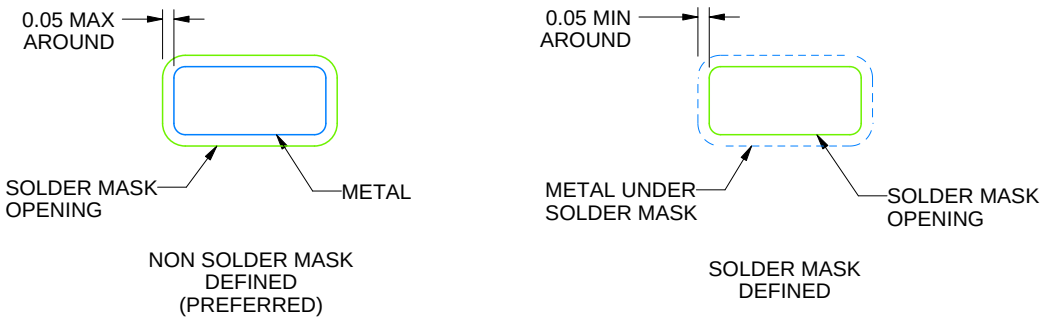
4224978/D 08/2026

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height



LAND PATTERN EXAMPLE
SCALE:40X

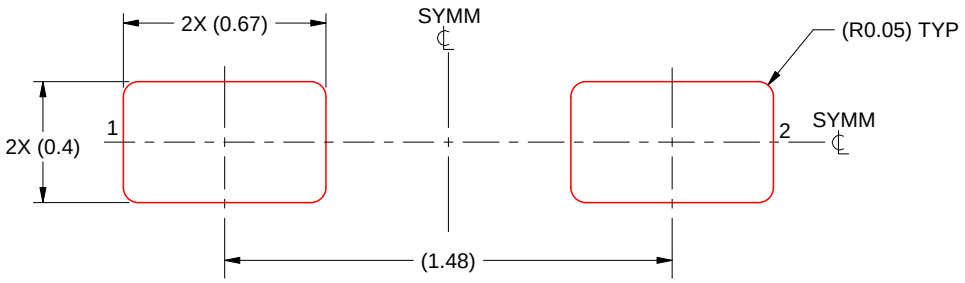


SOLDERMASK DETAILS

4224978/D 08/2026

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4224978/D 08/2026

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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