

ESD562 12V Bi-Directional ESD Protection in SOT-23

1 Features

- IEC 61000-4-5 surge protection:
 - 3.5A (8/20 μ s)
- IEC 61000-4-2 ESD protection:
 - ± 22 kV contact discharge
 - ± 30 kV air gap discharge
- 12V working voltage
- IO capacitance:
 - 1.5pF (typical)
- Bidirectional polarity to support positive and negative voltage swings
- 2 channel device provides complete ESD protection with single component
- Small, leaded SOT-23 allows low cost automatic optical inspection (AOI)
- IO capacitance:1.5

2 Applications

- End equipment:
 - [Factory automation and control](#)
 - [Building automation](#)
 - [Grid infrastructure](#)
 - [HVAC systems](#)
 - Security systems
- Interfaces:
 - RS-485
 - RS-422

3 Description

The ESD562 is a bidirectional ESD protection diode for RS-485 and RS-422 interface protection. The ESD562 is rated to dissipate ESD strikes beyond the maximum level specified in the IEC 61000-4-2 international standard (± 22 kV Contact, ± 30 kV Air-gap). The device can clamp 8/20 μ s surges with peak pulse currents up to 3A in accordance with the IEC 61000-4-5 standard.

This device features a 1.5pF (typical) IO capacitance enabling high-speed interface protection. The low clamping voltage in the positive and negative direction help protect systems against transient events. This protection is key in industrial systems which require a high level of robustness and reliability.

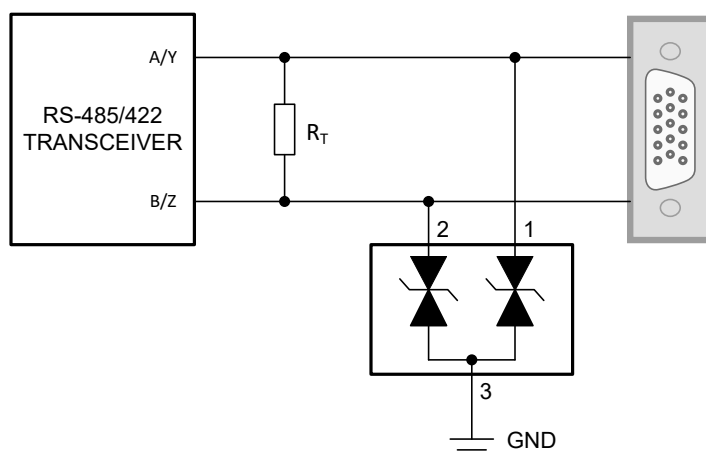
The ESD562 is available in a small leaded SOT-23 (DBZ) package.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
ESD562	DBZ (SOT-23, 3)	2.92mm × 2.37mm

(1) For more information, see [Section 9](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic



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4 Pin Configuration and Functions

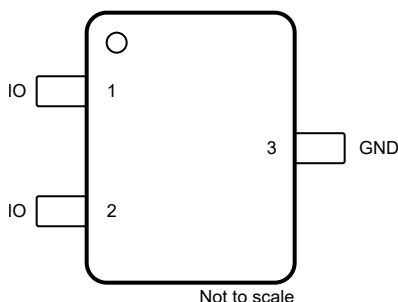


Figure 4-1. ESD562 DBZ Package, 3-Pin SOT-23 (Top View)

Table 4-1. Pin Functions for ESD562

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	Surge and ESD protected IO
GND	3	GND	Ground. Connect to ground

(1) I = Input, O = Output, I/O = Input or Output, GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
P _{pp}	IEC 61000-4-5 Surge (t _p 8/20μs) Peak Pulse Power at 25 °C		84	W
I _{pp}	IEC 61000-4-5 Surge (t _p 8/20μs) Peak Pulse Current at 25°C		3.5	A
T _A	Operating free-air temperature	-40	125	°C
T _{stg}	Storage temperature	-65	155	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings - JEDEC Specifications

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±22000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage between any 2 pins	-12		12	V
T _A	Operating Free Air Temperature	-40		125	°C

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		ESD562	UNIT
		DBZ (SOT-23)	
		3 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	250.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	136.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	84.0	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	29.5	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	83.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics

At $T_A = 25^\circ\text{C}$ unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	$I_{IO} < 50\text{nA}$	-12		12	V
$I_{LEAKAGE}$	Leakage current at V_{RWM}	$V_{IO} = \pm 12\text{V}$, I/O to GND		10	50	nA
V_{BR}	Breakdown Voltage, IO to GND and GND to IO ⁽¹⁾	$I_{IO} = \pm 1\text{mA}$	13.2		18	V
V_{CLAMP}	Surge clamping voltage, $t_p = 8/20\mu\text{s}$ ⁽²⁾	$I_{PP} = \pm 3\text{A}$, I/O to GND			21	V
	TLP clamping voltage, $t_p = 100\text{ns}$ ⁽³⁾	$I_{PP} = 16\text{A}$ (100ns TLP), I/O to GND		22		V
	TLP clamping voltage, $t_p = 100\text{ns}$ ⁽³⁾	$I_{PP} = 16\text{A}$ (100ns TLP), GND to I/O		22		V
V_{HOLD}	Holding Voltage, I/O to GND ⁽⁴⁾	TLP, IO to GND or GND to IO		16.5		V
C_{Line}	Line capacitance, IO to GND	$V_{IO} = 0\text{V}$, $f = 1\text{MHz}$		1.5		pF

(1) V_{BR} is defined as the voltage obtained at 1mA when sweeping the voltage up, before the devices latches into the snapback state

5.7 Typical Characteristics

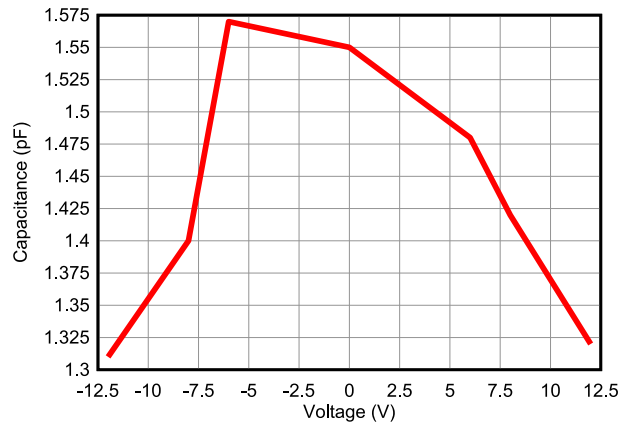


Figure 5-1. Capacitance vs. Bias Voltage

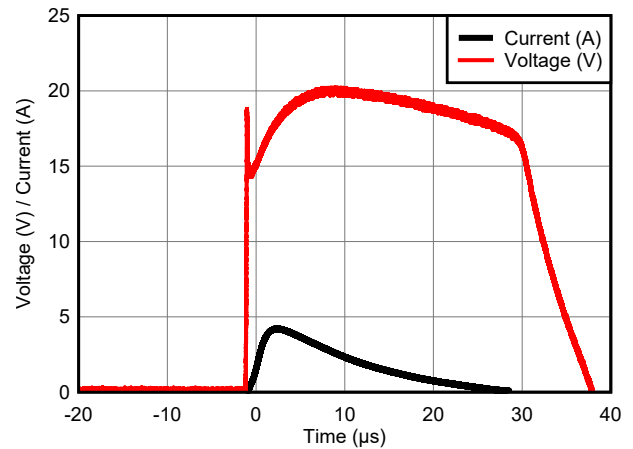


Figure 5-2. 8/20µs Surge Response

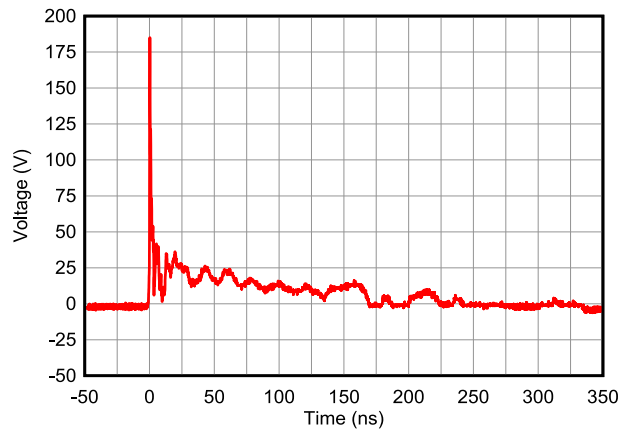


Figure 5-3. +8kV Clamped IEC Waveform

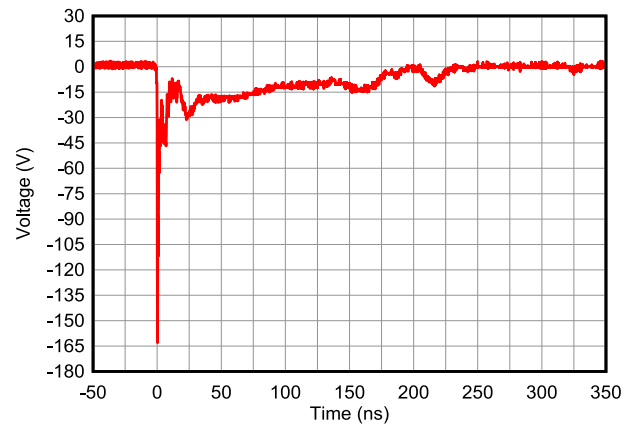


Figure 5-4. -8kV Clamped IEC Waveform

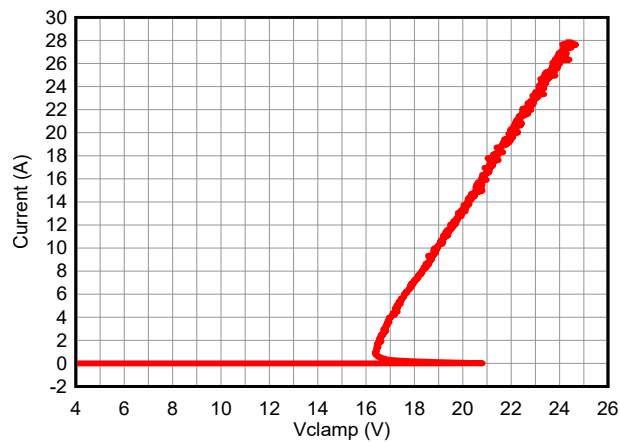


Figure 5-5. Positive TLP Curve

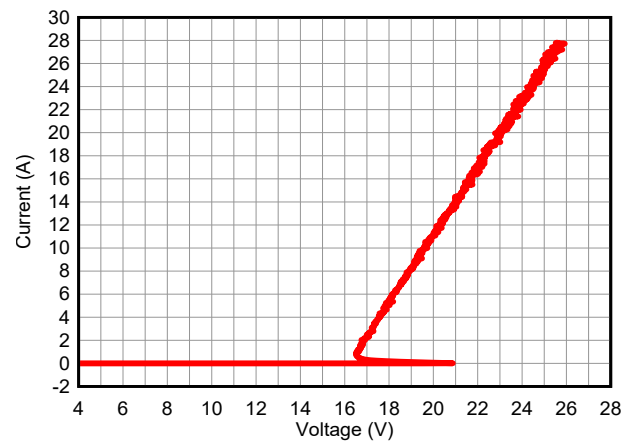


Figure 5-6. Negative TLP Curve

5.7 Typical Characteristics (continued)

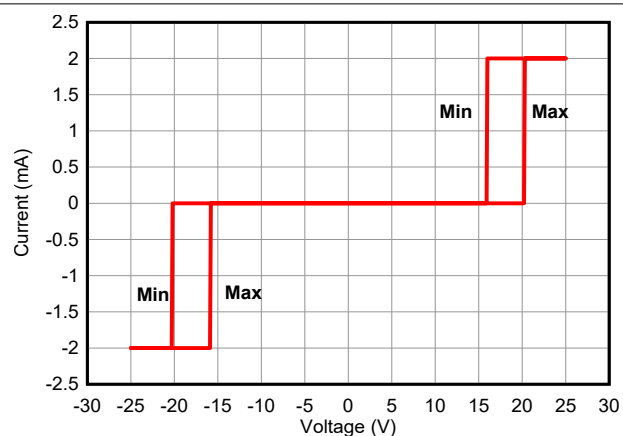


Figure 5-7. DC Voltage Sweep I-V Curve

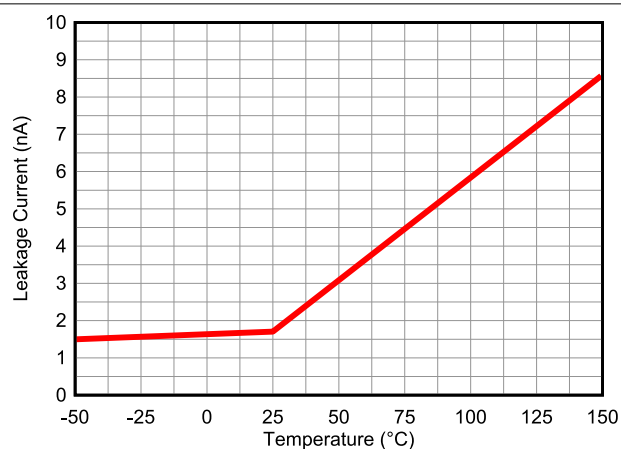


Figure 5-8. Leakage Current vs Temperature

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The ESD562 is a diode type TVS that provides a path to ground for dissipating transient voltage spikes, such as ESD or surge, on signal lines and power lines. Connect the device in parallel to the down stream circuitry for protection. As the current from the transient passes through the device, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, refer to the [ESD Packaging and Layout Guide](#) for details.

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Packaging and Layout Guide](#)
- Texas Instruments, [TI's IEC 61000-4-x Testing application note](#)
- Texas Instruments, [ESD Layout Guide user's guide](#)
- Texas Instruments, [ESD Protection Diodes EVM user's guide](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection Data Sheet user's guide](#)

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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7.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

DATE	REVISION	NOTES
February 2024	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD562DBZR	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	36X8
ESD562DBZR.B	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	36X8

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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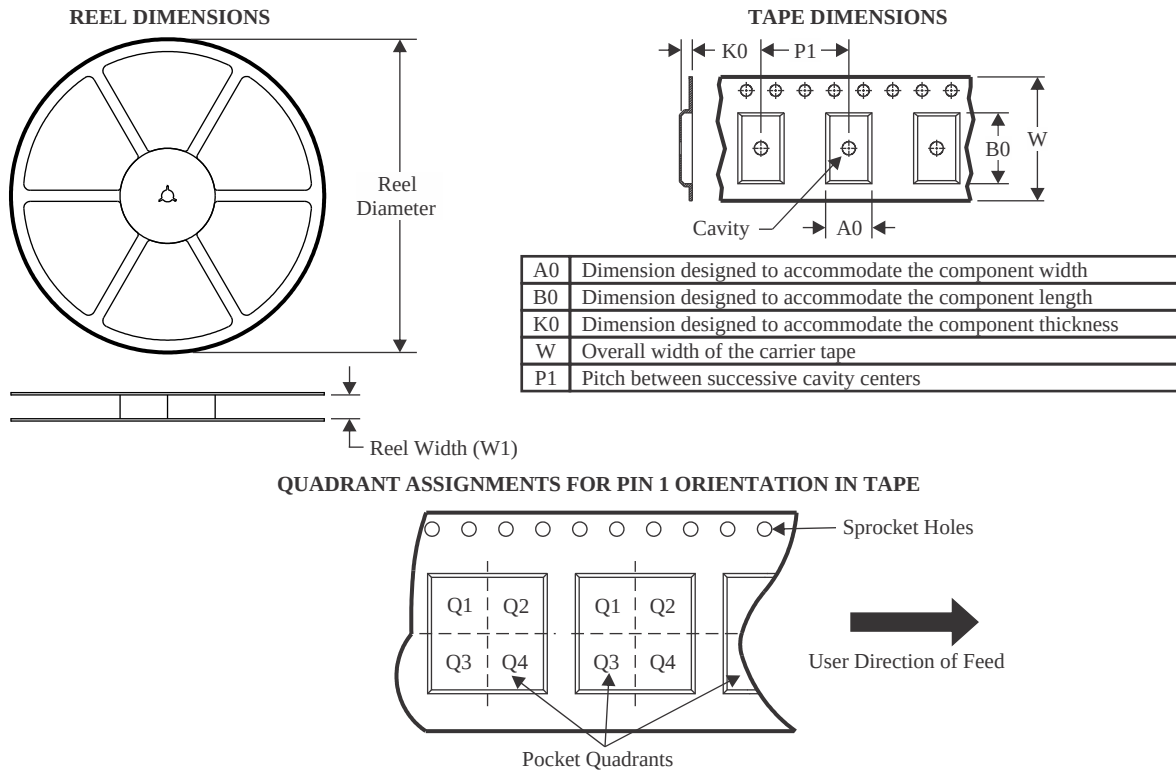
OTHER QUALIFIED VERSIONS OF ESD562 :

- Automotive : [ESD562-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD562DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

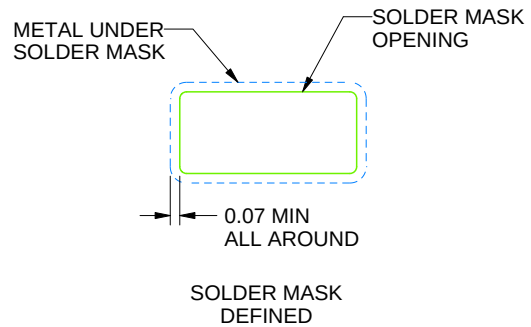
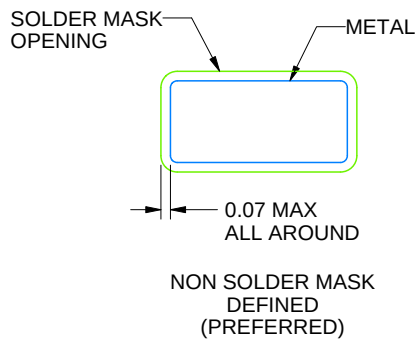
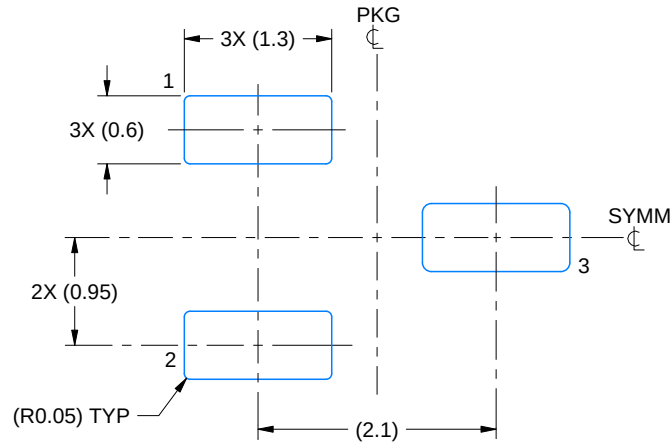
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD562DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

EXAMPLE BOARD LAYOUT

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER MASK DETAILS

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NOTES: (continued)

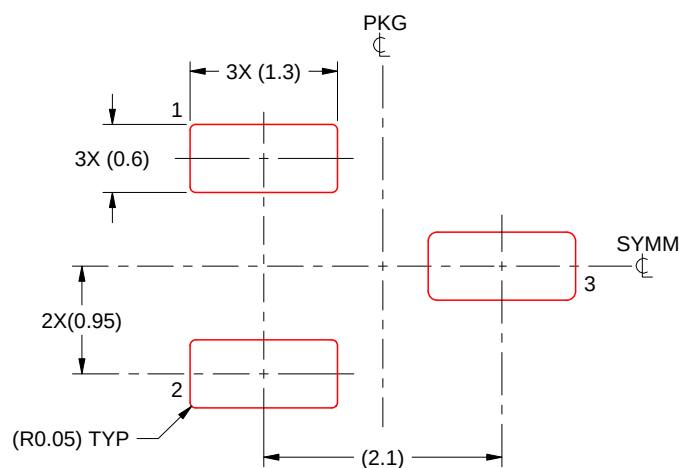
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



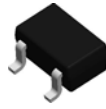
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

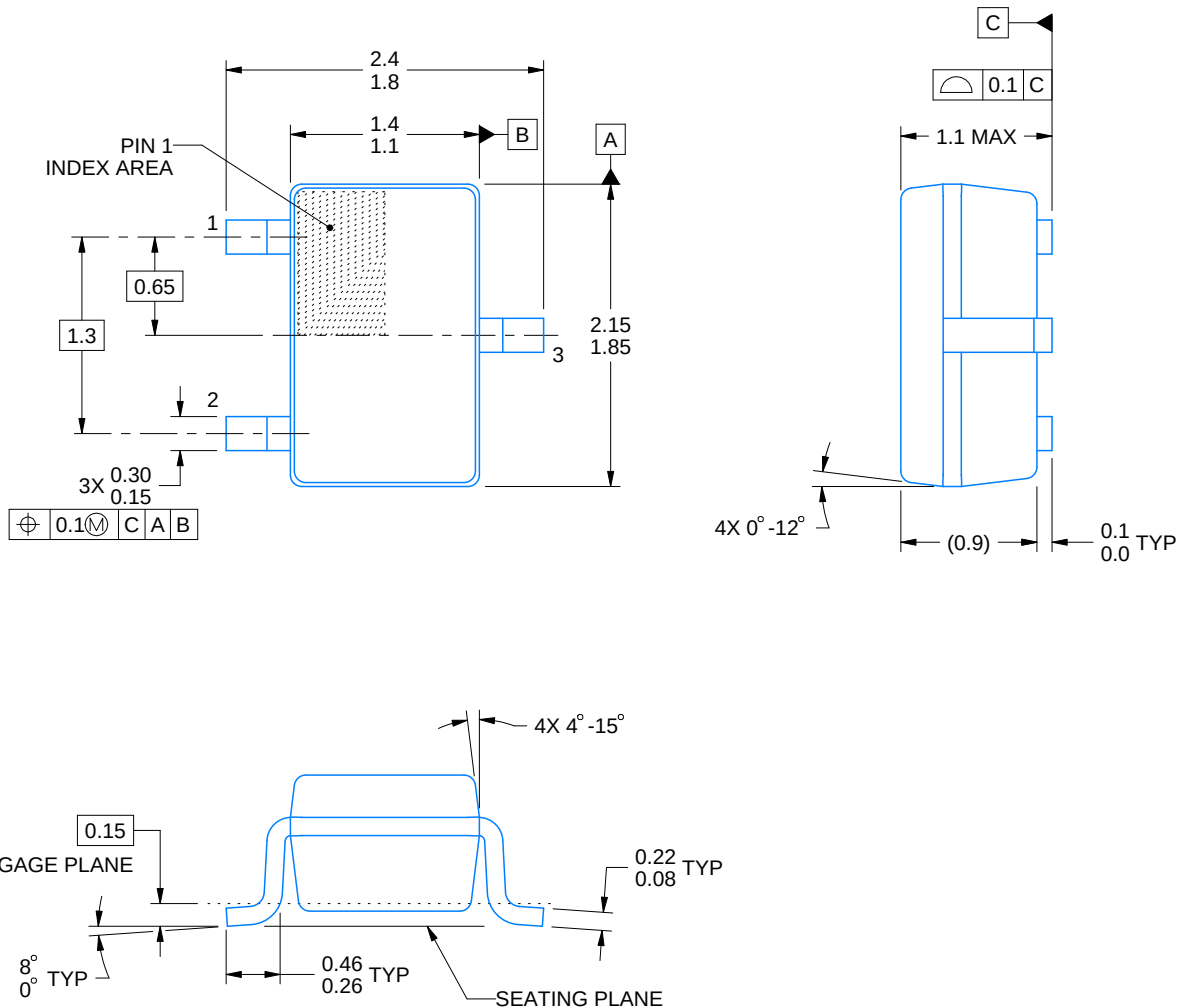
DCK0003A



PACKAGE OUTLINE

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



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NOTES:

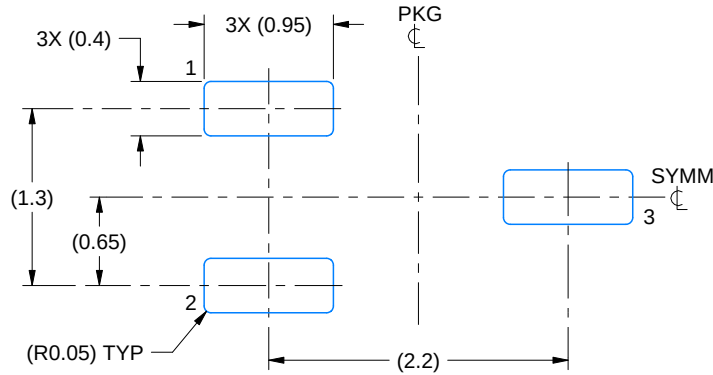
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

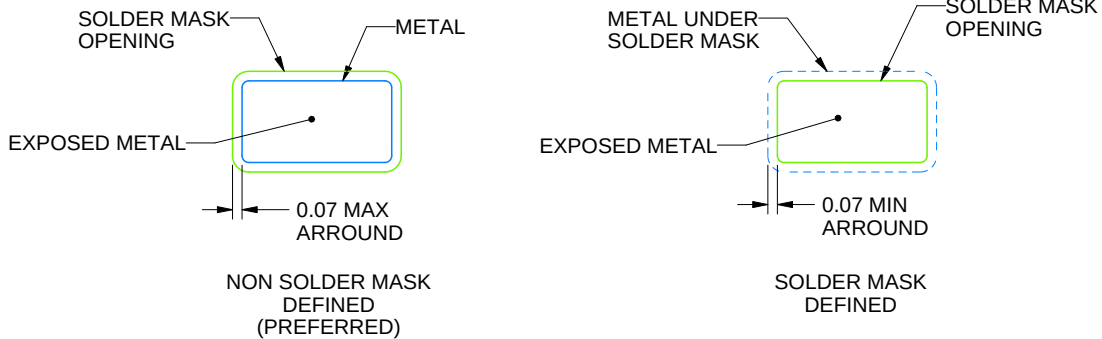
DCK0003A

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

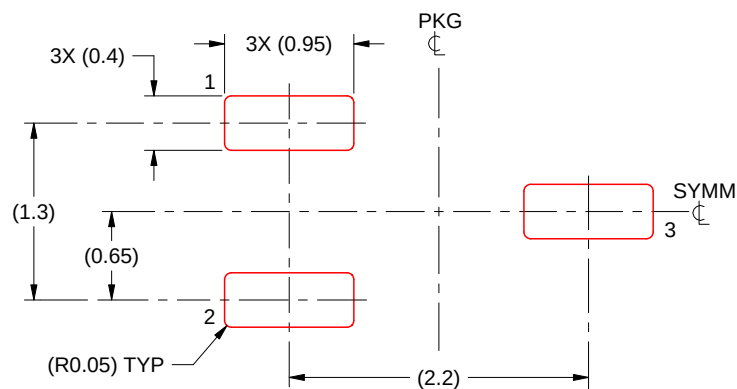
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0003A

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4220745/F 11/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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