

ESD551-Q1 1-Channel Automotive $\pm 30\text{kV}$ Bidirectional ESD Diode in an 0402 Package

1 Features

- IEC 61000-4-2 level 4 ESD protection
 - $\pm 30\text{kV}$ contact discharge
 - $\pm 30\text{kV}$ air gap discharge
- ISO 10605 (150pF, 330 Ω & 330pF, 330 Ω) ESD protection
 - $\pm 30\text{kV}$ contact discharge
 - $\pm 30\text{kV}$ air gap discharge
- IEC 61000-4-5 surge protection
 - 7A (8/20 μs)
- IO capacitance:
 - 2.8pF (typical)
- Ultra low leakage current: 100nA (maximum)
- Space-saving industry standard 0402 footprint (1.0mm $\times$ 0.6mm)
- AEC-Q101 qualified

2 Applications

- RS232
- RS485
- 12V Power Line
- GPIO

3 Description

The ESD551-Q1 is a bidirectional ESD protection diode for protecting power lines, low-speed data lines, and other I/O ports. The ESD551-Q1 is rated to dissipate ESD strikes up to $\pm 30\text{kV}$ per the IEC 61000-4-2 international standard (greater than Level 4).

This device features a 2.8pF (typical) IO capacitance enabling data line protection for protocols such as RS232/485. The extremely low dynamic resistance (0.29 Ω) and clamping voltage (22.5V at 16 TLP) is specified for system level protection against transient events.

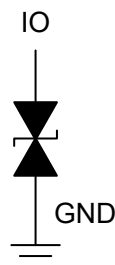
The 30kV ESD rating and 7A surge provides robust transient protection in a tiny package for protecting 12V power rails in space constrained applications.

The ESD551-Q1 is offered in the industry standard 0402 package.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
ESD551-Q1	DPY (DFN1006-2, 2)	1.0mm $\times$ 0.6mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length $\times$ width) is a nominal value and includes pins, where applicable.



Functional Block Diagram



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4 Pin Configuration and Functions

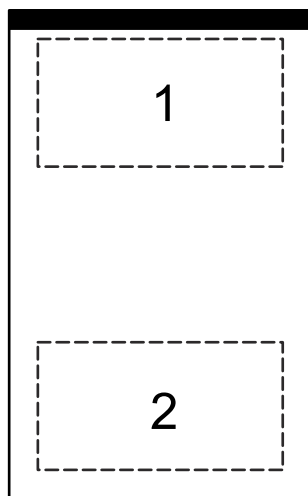


Figure 4-1. DPY Package, 2-Pin DFN1006 (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD Protected Channel. If used as ESD IO, connect pin 2 to ground
IO	2	I/O	ESD Protected Channel. If used as ESD IO, connect pin 1 to ground

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

Parameter		MIN	MAX	UNIT
P _{PPM}	IEC 61000-4-5 Surge (t _p = 8/20μs) Peak Pulse Power at 25°C ⁽²⁾		200	W
I _{PPM}	IEC 61000-4-5 Surge (t _p = 8/20μs) Peak Pulse Current at 25°C ⁽²⁾		7	A
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Voltages are with respect to GND unless otherwise noted.

5.2 ESD Ratings - AEC Specifications

Parameter		Test Conditions	VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q101-001 ⁽¹⁾	±2500	V
		Charged device model (CDM), per AEC Q101-005 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

Parameter		Test Conditions	VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30	kV
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 Air Discharge, all pins	±30	kV

5.4 ESD Ratings - ISO Specifications

Parameter		Test Conditions		VALUE	UNIT
V _(ESD)	ISO 10605 Electrostatic Discharge	C = 150pF; R = 330Ω	Contact Discharge, all pins	±30000	V
			Air-gap Discharge, all pins	±30000	
		C = 330pF; R = 330Ω	Contact Discharge, all pins	±30000	
			Air-gap Discharge, all pins	±30000	

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	-12		12	V
T _A	Operating Free Air Temperature	-55		150	°C

5.6 Thermal Information

THERMAL METRIC ⁽¹⁾		ESD551-Q1	UNIT
		DPY (DFN1006)	
		2 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	325.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	22.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	187.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	19.6	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	187.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.7 Electrical Characteristics

At TA = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{RWM}	Reverse stand-off voltage	I _{IO} < 10nA	-12		12	V
I _{LEAK}	Leakage current at V _{RWM}	V _{IO} = ±V _{RWM} V, I/O to GND			100	nA
V _{BR}	Breakdown voltage, I/O to GND ⁽¹⁾	I _{IO} = ±10mA	13.3		19	V
V _{CLAMP}	Surge clamping voltage, t _p = 8/20μs ⁽²⁾	I _{PP} = 7A, I/O to GND, GND to I/O			30.2	V
V _{CLAMP}	TLP clamping voltage, t _p = 100ns ⁽³⁾	I _{PP} = 16A (100ns TLP), I/O to GND, GND to I/O		22.5		V
R _{DYN}	Dynamic resistance ⁽⁴⁾	I/O to GND, GND to I/O		0.29		Ω
C _{LINE}	Line capacitance	V _{IO} = 0V, f = 1MHz		2.8		pF

(1) V_{BR} is defined as the voltage obtained at 10mA when sweeping the voltage up, before the device enters the snapback state

(2) Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5

(3) Non-repetitive square wave current pulse, Transmission Line Pulse (TLP); ANSI / ESD STM5.5.1-2008

(4) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10A and I = 20A

5.8 Typical Characteristics

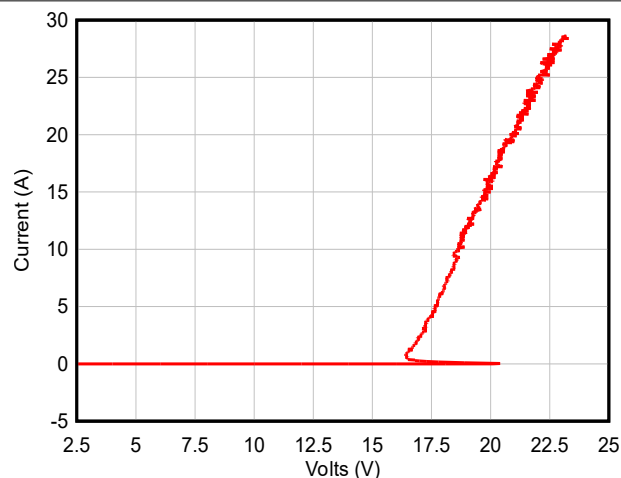


Figure 5-1. Positive TLP Curve

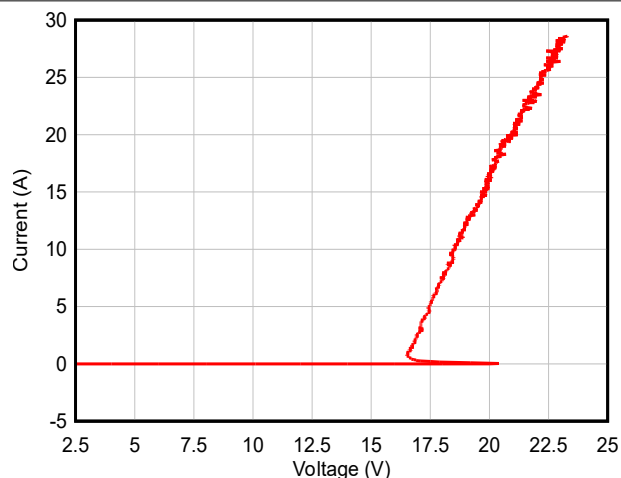


Figure 5-2. Negative TLP Curve

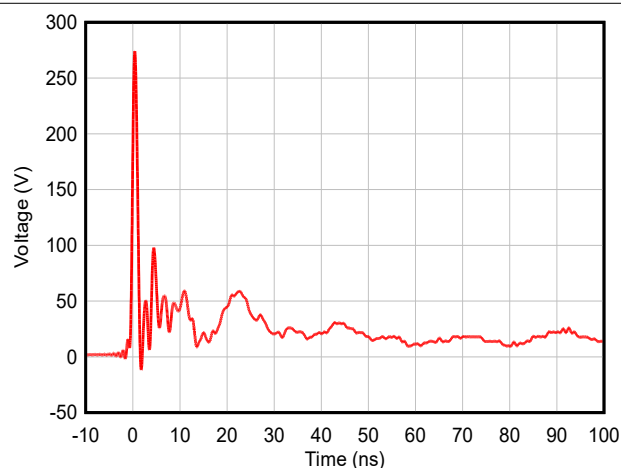


Figure 5-3. +8kV Clamped IEC Waveform

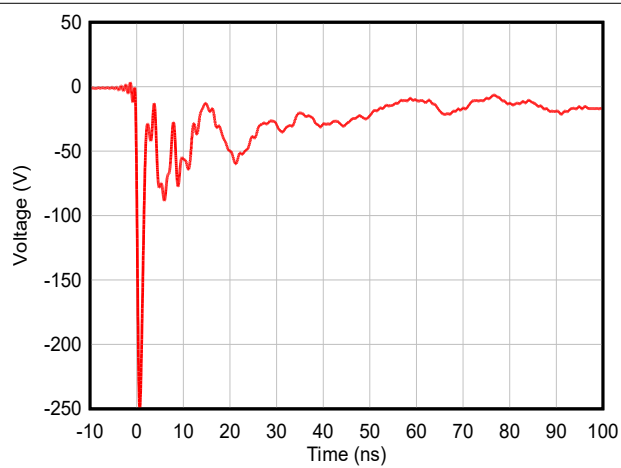


Figure 5-4. -8kV Clamped IEC Waveform

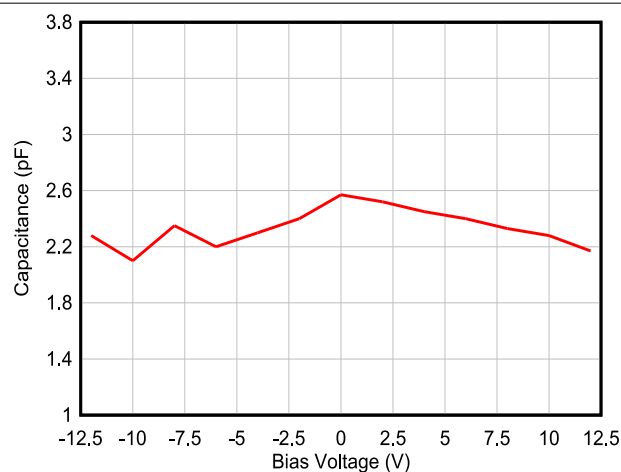


Figure 5-5. Capacitance vs Bias Voltage

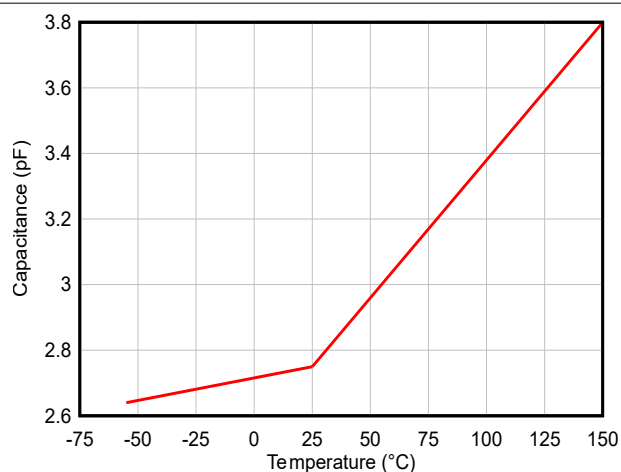
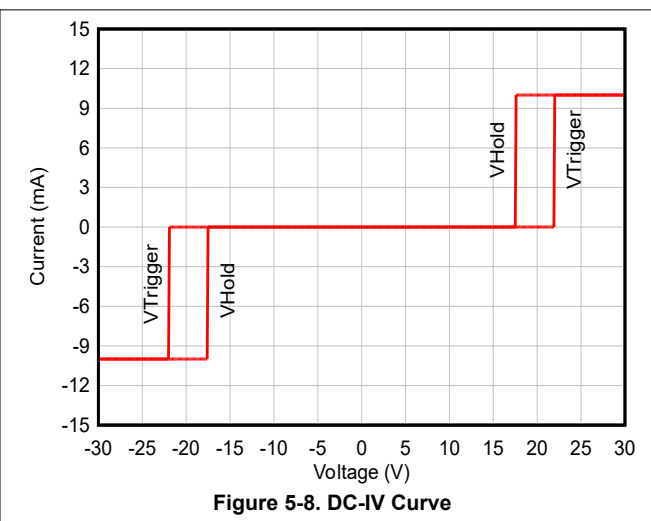
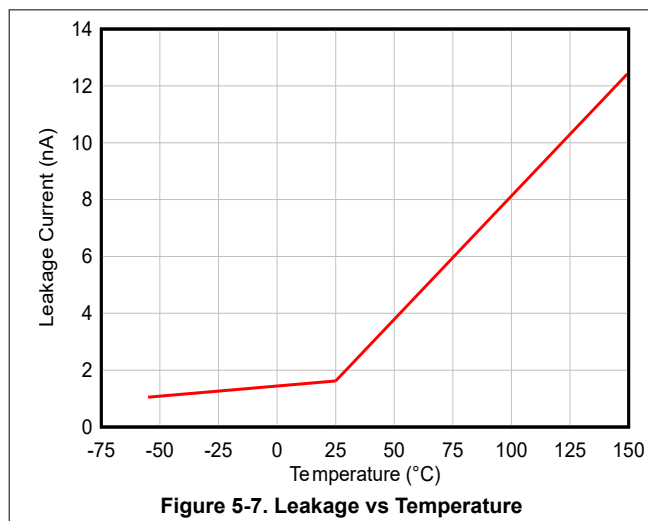


Figure 5-6. Capacitance vs Temperature

5.8 Typical Characteristics (continued)



6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Packaging and Layout Guide](#)
- Texas Instruments, [ESD Layout Guide application reports](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Picking ESD Diodes for Ultra High-Speed Data Lines application reports](#)
- Texas Instruments, [Reading and Understanding an ESD Protection data sheet](#)

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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6.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2026	*	Initial Release

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD551DPYRQ1	Active	Production	X1SON (DPY) 2	10000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-	SS

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ESD551-Q1 :

- Catalog : [ESD551](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

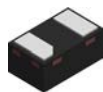
1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



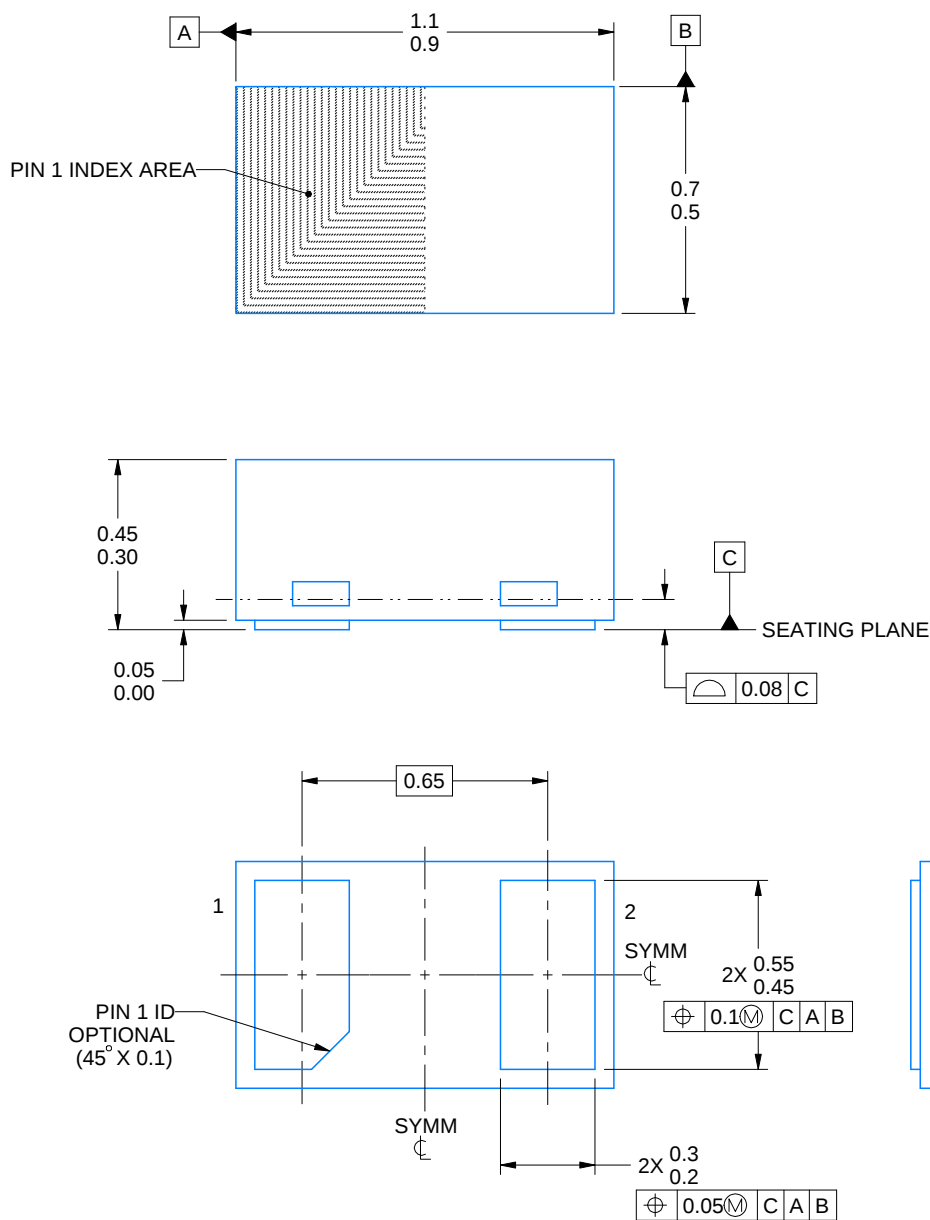
DPY0002A



PACKAGE OUTLINE

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES:

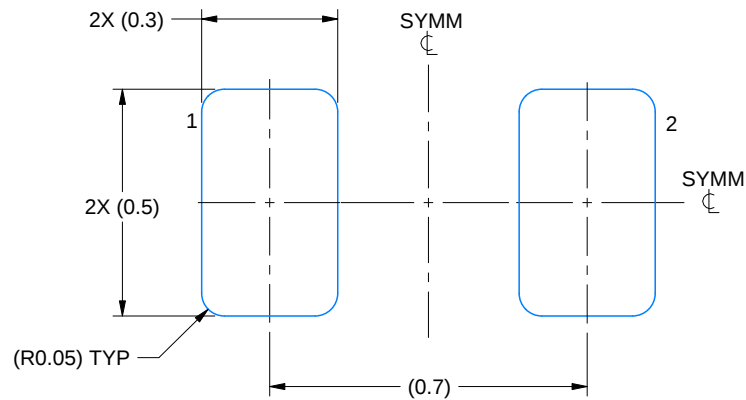
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

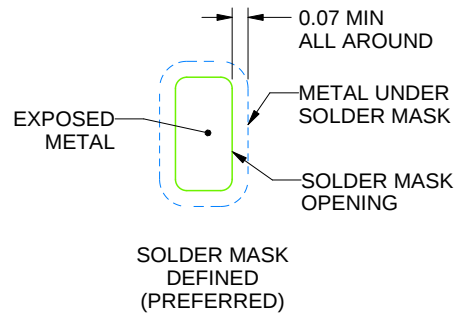
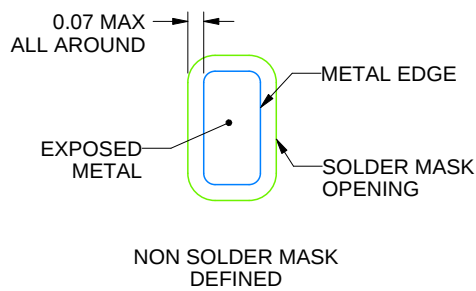
DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

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NOTES: (continued)

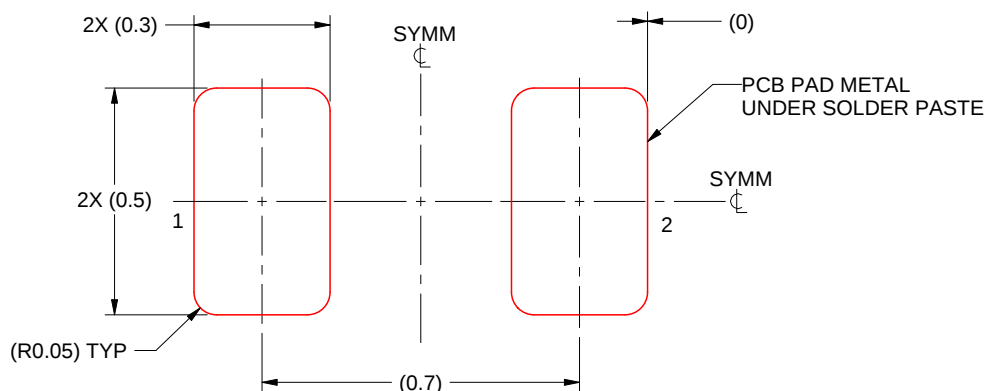
- For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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