

DS96F173MQML/DS96F175MQML EIA-485/EIA-422 Quad Differential Receivers

Check for Samples: [DS96F173MQML](#), [DS96F175MQML](#)

FEATURES

- Meets EIA-485, EIA-422A, EIA-423A Standards
- Designed for Multipoint Bus Applications
- TRI-STATE Outputs
- Common Mode Input Voltage Range: -7V to +12V
- Operates from Single +5.0V Supply
- Lower Power Version
- Input Sensitivity of ± 200 mV Over Common Mode Range
- Input Hysteresis of 50 mV Typical
- High Input Impedance
- DS96F173 and DS96F175 are Lead and Function Compatible with SN75173/175 or the AM26LS32/MC3486

DESCRIPTION

The DS96F173 and the DS96F175 are high speed quad differential line receivers designed to meet the EIA-485 standard. The DS96F173 and the DS96F175 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F173 and DS96F175 to operate at higher speeds while minimizing power consumption.

The DS96F173 and the DS96F175 have TRI-STATE outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of -7V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96F173 features an active high and active low Enable, common to all four receivers. The DS96F175 features separate active high Enables for each receiver pair.

Connection Diagrams

16-Lead Ceramic Dual-In-Line Package (Package Number NFE0016A)

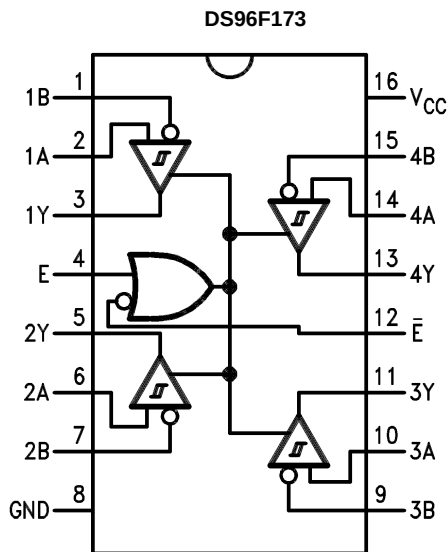


Figure 1. Top View

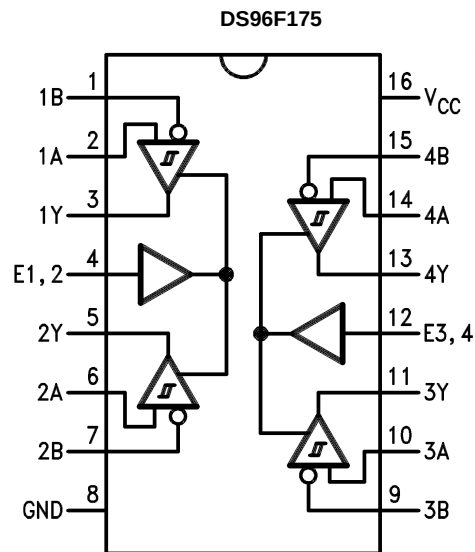


Figure 2. Top View



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

20-Lead Ceramic Leadless Chip Carrier (Package Number NAJ0020A)

*NC—No Connection

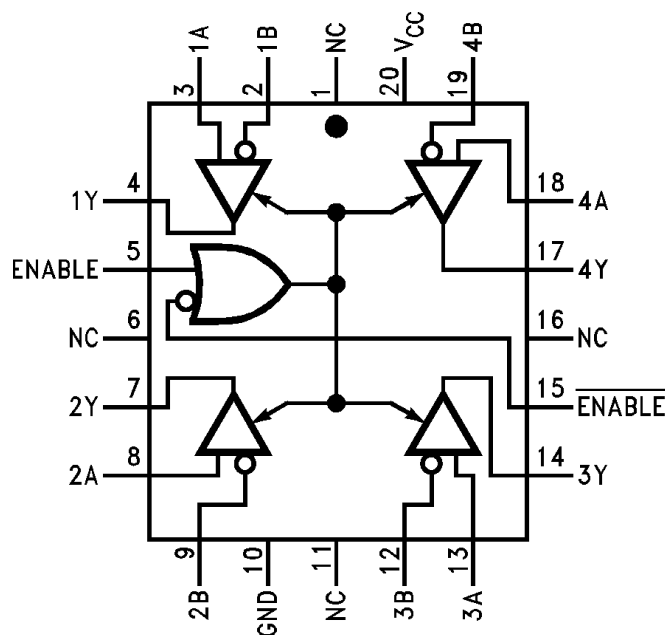


Figure 3. Top View

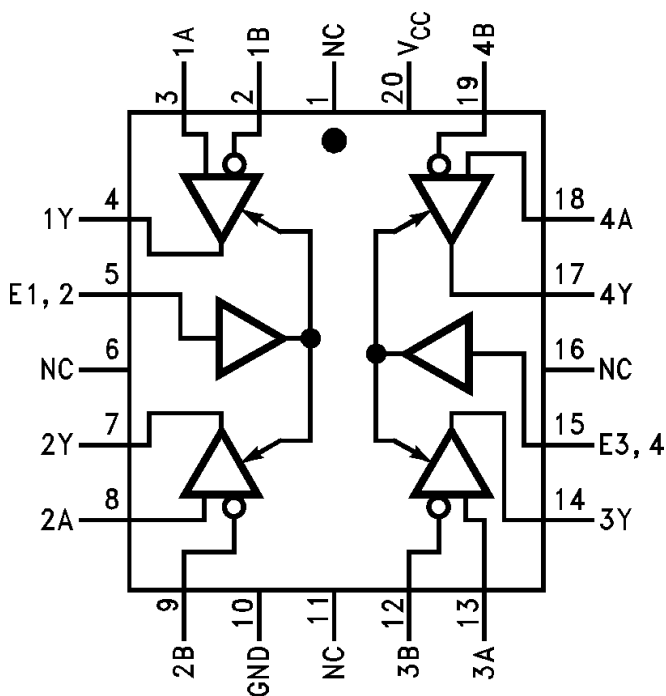
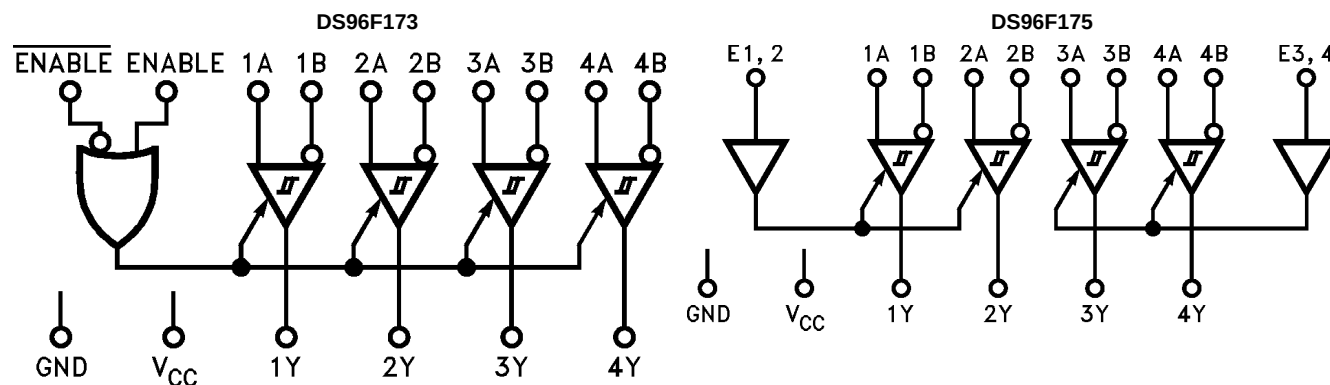


Figure 4. Top View

Logic Diagrams

Function Tables

Table 1. (Each Receiver) DS96F173⁽¹⁾

Differential Inputs A–B	Enable		Output Y
	E	$\bar{E}$	
$V_{ID} \geq 0.2V$	H	X	H
	X	L	H
$V_{ID} \leq -0.2V$	H	X	L
	X	L	L
X	L	X	Z
X	X	H	Z

(1) H = High Level
 L = Low Level
 Z = High Impedance (off)
 X = Don't Care

Table 2. (Each Receiver) DS96F175

Differential Inputs A–B	Enable E	Output Y
$V_{ID} \geq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

Storage Temperature Range (T _{Stg})		-65°C ≤ T _A ≤ +175°C
Lead Temperature (Soldering, 60 sec.)		300°C
Max. Package Power Dissipation at 25°C ⁽²⁾	CDIP (NFE)	1,500 mW
	CDIP (NAD)	1,034 mW
	LCCC (NAJ)	1,500 mW
Supply Voltage		7.0V
Input Voltage, A or B Inputs		±25V
Differential Input Voltage		±25V
Enable Input Voltage		7.0V
Low Level Output Current		50 mA

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the [Electrical Characteristics--DC Parameters](#). The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

- (2) Above T_A = 25°C derate NFE package 10 mW/°C, NAD package 6.90 mW/°C, NAJ package 11.11 mW/°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	4.50	5.50	V
Common Mode Input Voltage (V _{CM})	-7	+12	V
Differential Input Voltage (V _{ID})	-7	+12	V
Output Current HIGH (I _{OH})		-400	μA
Output Current LOW (I _{OL})		16	mA
Operating Temperature (T _A)	-55	125	°C

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

Electrical Characteristics--DC Parameters

The following conditions apply, unless otherwise specified. $V_{CC} = 5.0V$, Outputs Enabled

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
I_{CC}	Supply Current	$V_{CC} = 5.5V$, $V_{ID} = 2V$	See ⁽¹⁾		50	mA	1, 2, 3
V_{OH}	Logical "1" Output Voltage	$V_{CC} = 4.5V$, $I_{OH} = -400\mu A$, $V_{ID} = 0.2V$	See ⁽²⁾	2.5		V	1, 2, 3
V_{OL}	Logical "0" Output Voltage	$V_{CC} = 4.5V$, $I_{OL} = 8mA$, $V_{ID} = -0.2V$	See ⁽²⁾		0.45	V	1, 2, 3
V_{TH}	Differential-Input High Threshold Voltage	$V_{CC} = 4.5V$ & $5.5V$, $V_{CM} = 0V$, $V_O = 2.5V$, $I_O = -400\mu A$			0.20	V	1, 2, 3
		$V_{CC} = 4.5V$ & $5.5V$, $V_{CM} = -12V$, $V_O = 2.5V$, $I_O = -400\mu A$			0.20	V	1, 2, 3
		$V_{CC} = 4.5V$ & $5.5V$, $V_{CM} = 12V$, $V_O = 2.5V$, $I_O = -400\mu A$			0.20	V	1, 2, 3
V_{TL}	Differential-Input Low Threshold Voltage	$V_{CC} = 4.5V$ & $5.5V$, $V_{CM} = 0V$, $V_O = 0.5V$, $I_O = 16mA$		-0.20		V	1, 2, 3
		$V_{CC} = 4.5V$ & $5.5V$, $V_{CM} = -12V$, $V_O = 0.5V$, $I_O = 16mA$		-0.20		V	1, 2, 3
		$V_{CC} = 4.5V$ & $5.5V$, $V_{CM} = 12V$, $V_O = 0.5V$, $I_O = 16mA$		-0.20		V	1, 2, 3
I_I	Input Line Current	$V_{CC} = 4.5V$, $V_I = 12V$, Untested Inputs are 0V			1.0	mA	1, 2, 3
		$V_{CC} = 5.5V$, $V_I = -7V$, Untested Inputs are 0V		-0.8		mA	1, 2, 3
I_{IH}	Logical "1" Enable Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$			10	μA	1, 2, 3
I_{IL}	Logical "0" Enable Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$		-100		μA	1, 2, 3
I_{OS}	Output Short Circuit Current	$V_{CC} = 4.5V$, $V_O = 0V$	See ⁽³⁾	-85	-15	mA	1, 2, 3
		$V_{CC} = 5.5V$, $V_O = 0V$		-85	-15	mA	1, 2, 3
V_{IK}	Enable Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$		-1.5		V	1, 2, 3
I_{OZ}	High Impedance Output Current	$V_{CC} = 5.5V$, $V_{En} = 0.8V$, $V_O = 0.4V$, Outputs disabled		-20	20	μA	1, 2, 3
		$V_{CC} = 5.5V$, $V_{En} = 0.8V$, $V_O = 2.4V$, Outputs disabled		-20	20	μA	1, 2, 3
V_{IH}	Logical "1" Enable Input Voltage		See ⁽⁴⁾	2.0		V	1, 2, 3
V_{IL}	Logical "0" Enable Input Voltage		See ⁽⁵⁾		0.8	V	1, 2, 3
R_I	Input Resistance			10		k Ω	1, 2, 3

(1) I_{CC} is tested with outputs disabled (worst case), I_{CC} enabled is ensured by this test.

(2) V_{OH} & V_{OL} are tested over common mode voltage range of $\pm 12V$ via the V_{TH} / V_{TL} tests.

(3) Only one output at a time should be shorted.

(4) Ensured by V_{OL} & V_{OH} tests.

(5) Ensured by I_{OZ} test.

AC Parameters

The following conditions apply, unless otherwise specified. $V_{CC} = 5.0V$

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
t_{PHL}	Propagation Delay	$C_L = 15pF$			22	ns	1
					30	ns	2, 3
t_{PLH}	Propagation Delay	$C_L = 15pF$			22	ns	1
					30	ns	2, 3
t_{PZH}	Propagation Delay	$C_L = 15pF$			16	ns	1
					27	ns	2, 3
t_{PZL}	Propagation Delay	$C_L = 15pF$			18	ns	1
					27	ns	2, 3
t_{PHZ}	Propagation Delay	$C_L = 5pF$	See ⁽¹⁾		20	ns	1
					27	ns	2, 3
		$C_L = 20pF$			30	ns	1
					37	ns	2, 3
t_{PLZ}	Propagation Delay	$C_L = 5pF$			18	ns	1
					30	ns	2, 3
t_{PW}	Propagation Delay				3.0	ns	1
					8.0	ns	2
					5.0	ns	3

(1) Testing at 20pF assures conformance to spec at 5pF.

PARAMETER MEASUREMENT INFORMATION

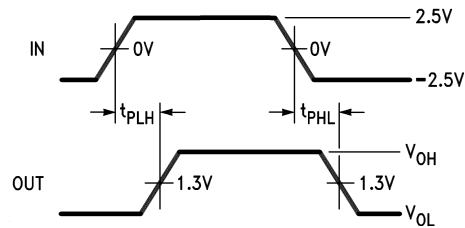
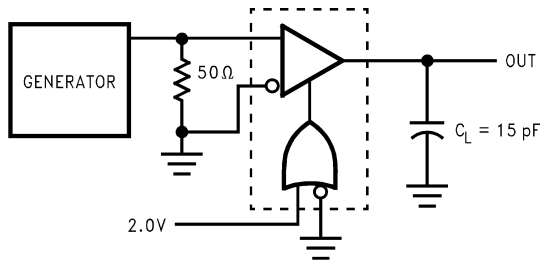


Figure 5. t_{PLH} , t_{PHL} (2)(3)

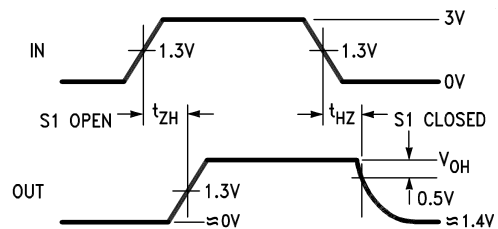
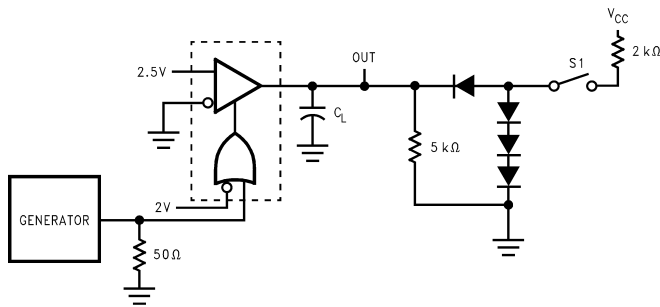


Figure 6. t_{HZ} , t_{ZH} (2)(3)(4)(5)

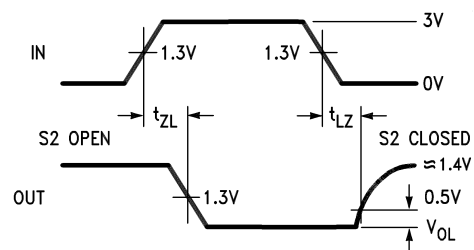
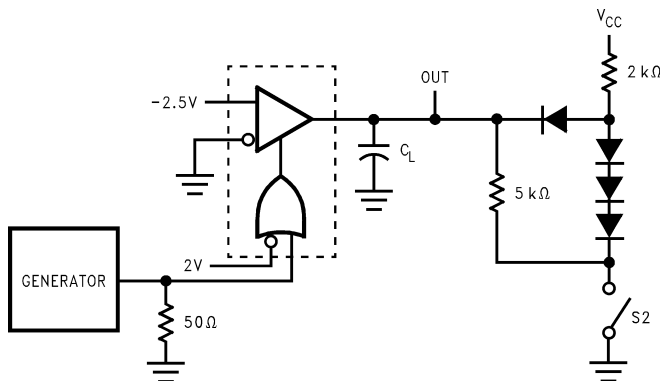


Figure 7. t_{ZL} , t_{LZ} (2)(3)(4)(5)

- (2) The input pulse is supplied by a generator having the following characteristics: $f = 1.0\text{ MHz}$, 50% duty cycle, $t_r \leq 6.0\text{ ns}$, $t_f \leq 6.0\text{ ns}$, $Z_O = 50\Omega$.
- (3) C_L includes probe and stray capacitance.
- (4) All diodes are 1N916 or equivalent.
- (5) To test the active low Enable $\bar{E}$ of DS96F173, ground E and apply an inverted input waveform to $\bar{E}$. DS96F175 has active high enable only.

Typical Application

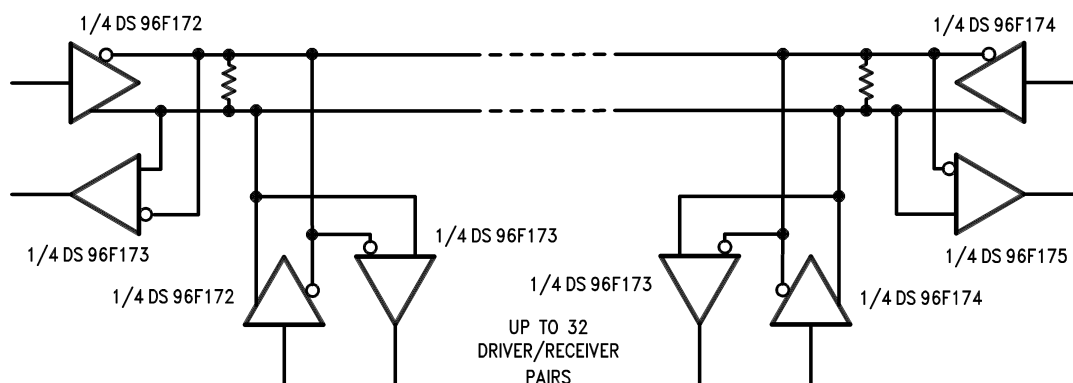


Figure 8.

NOTE

The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

REVISION HISTORY

Released	Revision	Section	Changes
28-Apr-11	A	New Release, Corporate format	2 MDS data sheets converted into one Corp. data sheet format. MNDS96F173M-X Rev 0A0 & MNDS96F175M-X Rev 0B0 will be archived.

Changes from Original (April 2013) to Revision A

Page

- Changed layout of National Data Sheet to TI format [8](#)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9076601M2A	Active	Production	LCCC (NAJ) 20	50 TUBE	No	Call TI	Call TI	-55 to 125	DS96F175ME /883 Q 5962-90766 01M2A ACO 01M2A >T
5962-9076601VEA	Active	Production	CDIP (NFE) 16	25 TUBE	No	Call TI	Call TI	-55 to 125	DS96F175MJ-QMLV 5962-9076601VEA Q
5962-9076602M2A	Active	Production	LCCC (NAJ) 20	50 TUBE	No	Call TI	Call TI	-55 to 125	DS96F173ME /883 Q 5962-90766 02M2A ACO 02M2A >T
5962-9076602MEA	Active	Production	CDIP (NFE) 16	25 TUBE	No	Call TI	Call TI	-55 to 125	DS96F173MJ/883 5962-9076602MEA Q
DS96F173ME/883	Active	Production	LCCC (NAJ) 20	50 TUBE	No	Call TI	Call TI	-55 to 125	DS96F173ME /883 Q 5962-90766 02M2A ACO 02M2A >T
DS96F173MJ/883	Active	Production	CDIP (NFE) 16	25 TUBE	No	Call TI	Call TI	-55 to 125	DS96F173MJ/883 5962-9076602MEA Q
DS96F175ME/883	Active	Production	LCCC (NAJ) 20	50 TUBE	No	Call TI	Call TI	-55 to 125	DS96F175ME /883 Q 5962-90766 01M2A ACO 01M2A >T
DS96F175MJ-QMLV	Active	Production	CDIP (NFE) 16	25 TUBE	No	Call TI	Call TI	-55 to 125	DS96F175MJ-QMLV 5962-9076601VEA Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

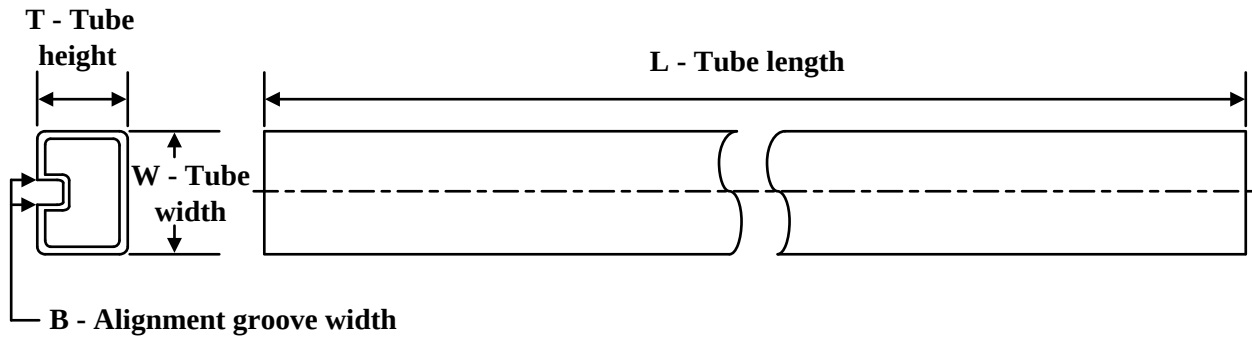
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DS96F175MQML, DS96F175MQML-SP :

- Military : [DS96F175MQML](#)
- Space : [DS96F175MQML-SP](#)

NOTE: Qualified Version Definitions:

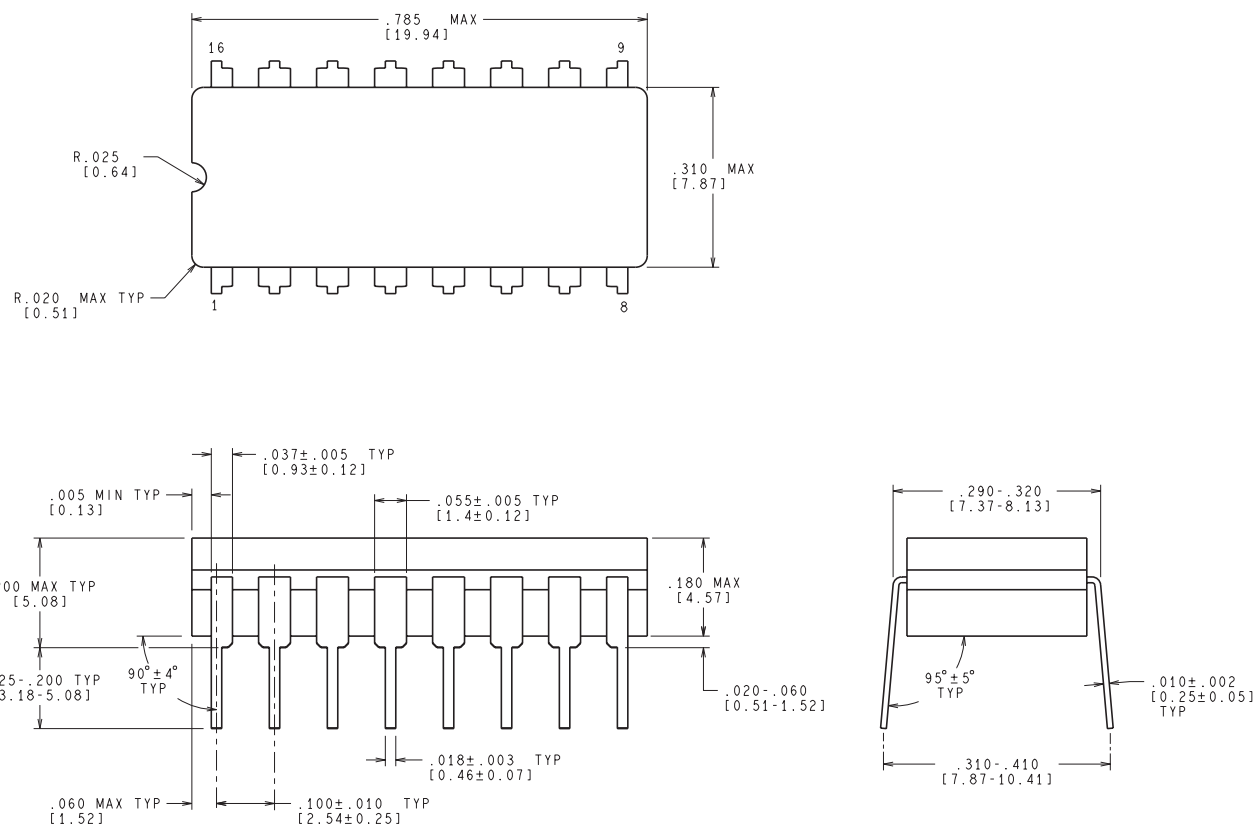
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9076601M2A	NAJ	LCCC	20	50	470	11	3810	0
5962-9076601VEA	NFE	CDIP	16	25	506.98	15.24	13440	NA
5962-9076602M2A	NAJ	LCCC	20	50	470	11	3810	0
5962-9076602MEA	NFE	CDIP	16	25	506.98	15.24	13440	NA
DS96F173ME/883	NAJ	LCCC	20	50	470	11	3810	0
DS96F173MJ/883	NFE	CDIP	16	25	506.98	15.24	13440	NA
DS96F175ME/883	NAJ	LCCC	20	50	470	11	3810	0
DS96F175MJ-QMLV	NFE	CDIP	16	25	506.98	15.24	13440	NA

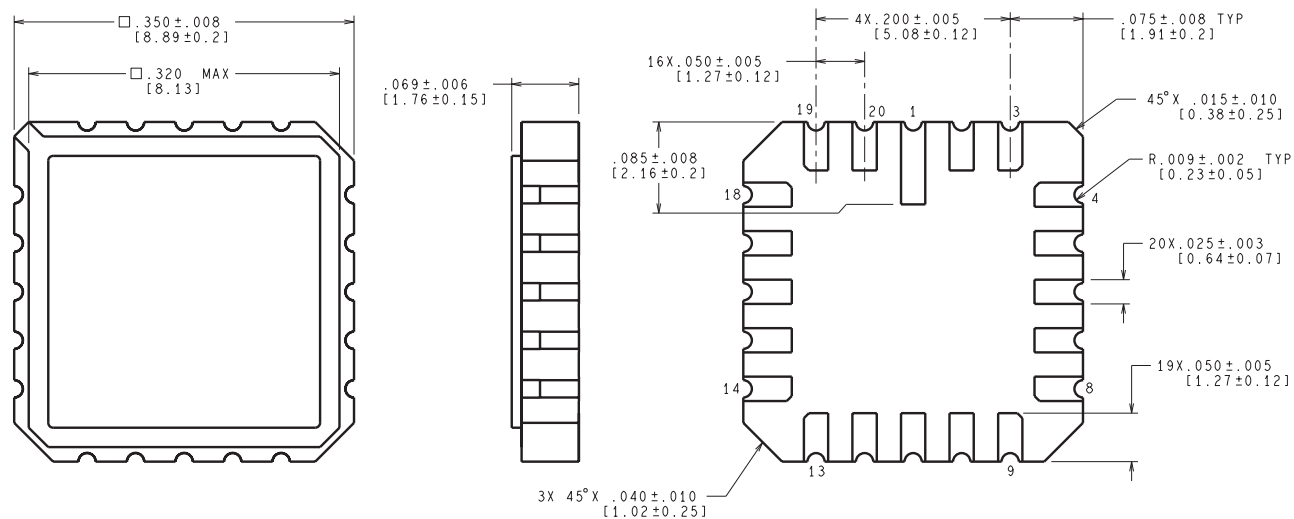
NFE0016A



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

J16A (REV L)

NAJ0020A



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

E20A (Rev F)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025