DS90C387R 85MHz Dual 12-Bit Double Pumped Input LDI Transmitter - VGA/UXGA

Check for Samples: DS90C387R

FEATURES

- **Complies with Open LDI Specification for Digital Display Interfaces**
- **25 to 85MHz Clock Support**
- **Supports VGA through UXGA Panel Resolution**
- **Up to 4.76Gbps Bandwidth in Dual 24-bit RGB In-to-Dual Pixel Out Application**
- **Dual 12-bit Double Pumped Input DVO Port**
- **Pre-Emphasis Reduces Cable Loading Effects**
- **Drives Long, Low Cost Cables**
- **DC Balance Data Transmission Provided by Transmitter Reduces ISI Distortion**
- **Transmitter Rejects Cycle-to-Cycle Jitter (±2ns of Input Bit Period)**
- **Support both LVTTL and Low Voltage Level Input (Capable of 1.0 to 1.8V)**
- **Two-Wire Serial Communication Interface up to 400 KHz**
- **Programmable Input Clock and Control Strobe Select**
- **Backward Compatible Configuration with 112MHz LDI and FPD-Link**
- **Optional Second LVDS Clock for Backward Compatibility with FPD-Link Receivers**
- **Compatible with TIA/EIA-644**

DESCRIPTION

The DS90C387R transmitter is designed to support pixel data transmission from a Host to a Flat Panel Display up to UXGA resolution. It is designed to be compatible with Graphics Memory Controller Hub (GMCH) by implementing two data per clock and can be controlled by a two-wire serial communication interface. Two input modes are supported: one port of 12-bit(two data per clock) input for 24-bit RGB, and two ports of 12-bit(two data per clock) input for dual 24-bit RGB(48-bit total). In both modes, input data will be clocked on both rising and falling edges in LVTTL level operation, or clocked on the cross over of differential clock signals in the low swing operation. Each input data width will be 1/2 of clock cycle. With an input clock at 85MHz and input data at 170Mbps, the maximum transmission rate of each LVDS line is 595Mbps, for a aggregate throughput rate of 2.38Gbps/4.76Gbps. It converts 24/48 bits (Single/Dual Pixel 24-bit color) of data into 4/8 LVDS (Low Voltage Differential Signaling) data streams. DS90C387R can be programmed via the two-wire serial communication interface. The LVDS output pin-out is identical to DS90C387. Thus, this transmitter can be paired up with DS90CF388, receiver of the 112MHz LDI chipset or FPD-Link Receivers in non-DC Balance mode operation which provides GUI/LCD panel/mother board vendors a wide choice of inter-operation with LVDS based TFT panels.

DS90C387R also comes with features that can be found on DS90C387. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. DC Balancing on a cycle-to-cycle basis is also provided to reduce ISI (Inter-Symbol Interference), control signals (VSYNC, HSYNC, DE) are sent during blanking intervals. With pre-emphasis and DC Balancing, a low distortion eye-pattern is provided at the receiver end of the cable. These enhancements allow cables 5 to 15+ meters in length to be driven depending on media characteristic and pixel clock speed. Pre-emphasis is available in both the DC Balanced and Non-DC Balanced modes. In the Non-DC Balanced mode backward compatibility with FPD-Link Receivers is obtained.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

This chip is an ideal solution to solve EMI and cable size problems for high-resolution flat panel display applications. It provides a reliable industry standard interface based on LVDS technology that delivers the bandwidth needed for high-resolution panels while maximizing bit times, and keeping clock rates low to reduce EMI and shielding requirements. For more details, please refer to the “Applications Information” section of this datasheet.

Table 1. Mode Configuration / Performance Table

Mode	One 12-bit	Two 12-bit
Mode (GUI Out/Cable)	single/single	dual/dual
Input Clock Rate (MHz)	25-85	25-85
Input Data Rate (Mbps)	50-170	50-170
LVDS data Pairs Out	4	8
Ouput Clock Rate (MHz)	25-85	25-85
Data Rate Out (Mbps) per LVDS channel	175-595	175-595
Throughput Data Rate Out	2.38Gbps	4.76Gbps

Generalized Block Diagrams

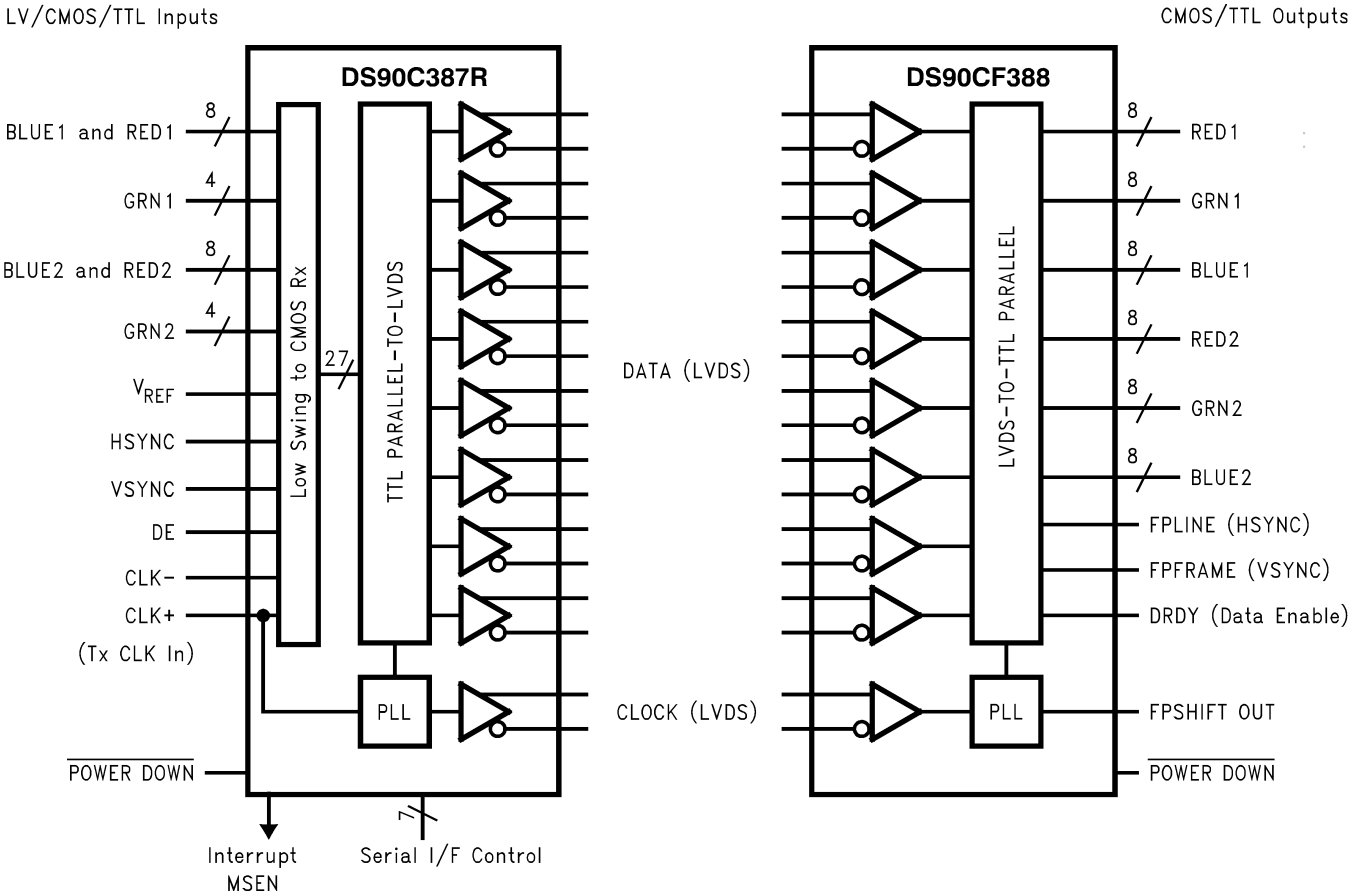

Figure 1. DS90C387R

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Absolute Maximum Ratings (1)(2)

		Min	Max	Unit
Supply Voltage (V_{CC})		−0.3	+4	V
LVCMOS/LVTTL Output Voltage		−0.3	V_{CC} + 0.3	V
LVDS Driver Output Voltage		−0.3	V_{CC} + 0.3	
LVDS Output Short Circuit Duration		Continuous		
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (Soldering, 4 seconds)			+260	°C
Maximum Package Power Dissipation Capacity at 25°C	100 TQFP Package		2.8	W
Package Derating		18.2mW/°C above +25°C		
ESD Rating	HBM, 1.5kΩ, 100pF		> 2	kV
	EIAJ, 0Ω, 200pF		> 300	V

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Nom	Max	Unit
All Supply Voltage	3.0	3.3	3.6	V
Operating Free Air Temperature ($T_{A)}$)	−10	+25	+70	°C
Supply Noise Voltage (V_{CC}) up to 33MHz			100	mV_{p-p}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LVCMOS/LVTTL DC SPECIFICATIONS (All pins, except output pins AnP, AnM, CLKnP and CLKnM, BAL, $\overline{PD}$ pins)						
V_{IH}	High Level Input Voltage	$V_{REF} = V_{CC3V} = V_{CC}$	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage	$V_{REF} = V_{CC3V} = V_{CC}$	GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = 18 mA		-0.8	-1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, or V_{CC}		+1.8	+15	µA
		V_{IN} = GND	−15	0		µA
V_{OL}	Low level Open Drain Output Voltage	I_{OL} = 2 mA		0.1	0.3	V
LVCMOS DC SPECIFICATIONS ($\overline{PD}$ pin)						
V_{IH}	High Level Input Voltage	$V_{REF} = V_{CC3V} = V_{CC}$	2.9		V_{CC}	V
V_{IL}	Low Level Input Voltage	$V_{REF} = V_{CC3V} = V_{CC}$	GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = 18 mA		-0.8	-1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, or V_{CC}		+1.8	+15	µA
		V_{IN} = GND	−15	0		µA
LVDS DRIVER DC SPECIFICATIONS (output pins AnP, AnM, CLKnP and CLKnM)						
V_{OD}	Differential Output Voltage	R_L = 100Ω	247	345	550	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	mV
V_{OS}	Offset Voltage		1.125	1.25	1.475	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω		−3.5	−11	mA
I_{OZ}	Output TRI-STATE Current	$\overline{PD}$ = 0V, V_{OUT} = 0V or V_{CC}		±1	±10	µA

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C. Device tested in Non-Balanced mode only.

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Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Low Voltage Mode DC SPECIFICATIONS(pins D0 to D23, CLKINP, CLKINM, DE, HSYNC,VSYNC)							
V_{IHLS}	Low Swing High Level Input Voltage, V_{CC} = 3V	(2)		V_{REF} +100mV		1.8	V
V_{ILLS}	Low Swing Low Level Input Voltage,V_{CC} = 3V			GND		V_{REF} - 100mV	V
V_{REF}	Differential Input Reference Voltage, V_{CC} = 3V	Low Swing,V_{REF} = ½V_{DDQ}		0.45	0.5*V_{DDQ}	1	V
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern (Figure 4), BAL=High (enabled), V_{CC} = 3.6V	f = 32.5 MHz, DUAL = V_{CC}		115	180	mA
			f = 32.5 MHz, DUAL = Gnd		75		mA
			f = 65 MHz, DUAL = V_{CC}		150	215	mA
			f = 65 MHz, DUAL = Gnd		95		mA
			f = 85 MHz, DUAL = V_{CC}		175	235	mA
			f = 85 MHz, DUAL = Gnd		110		mA
ICCTG	Transmitter Supply Current, 16 Grayscale Case	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern (Figure 3), BAL = High (enabled), V_{CC} = 3.6V	f = 32.5 MHz, DUAL = V_{CC}		110	170	mA
			f = 32.5 MHz, DUAL = Gnd		70		mA
			f = 65 MHz, DUAL = V_{CC}		135	205	mA
			f = 65 MHz, DUAL = Gnd		90		mA
			f = 85 MHz, DUAL = V_{CC}		155	225	mA
			f = 85 MHz, DUAL = Gnd		100		mA
ICCTZ	Transmitter Supply Current, Power Down	$\overline{PD}$ = Low Driver Outputs in TRI-STATE under Powerdown Mode			4.8	85	µA

(2) Low Swing DC threshold testing is preformed on data and control inputs only. Clock inputs tested by functional testing only.

DIGITAL DC CHARACTERISTICS for Two-Wire Serial Communication Interface

Over recommended operating supply and temperature ranges unless otherwise specified.(1)
Parameters list below only valid when I2CSEL pin = Vcc.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}(1)	Logical " 1 " input voltage		2.1			V
V_{IN}(0)	Logical " 0 " input voltage				0.8	V
V_{OL}	Serial Bus Low level output voltage	I_{OL}= 3mA			0.4	V
		I_{OL}= 6mA			0.6	V

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C. Device tested in Non-Balanced mode only.

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Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. Device driving the transmitter inputs should comply to this table of recommendations.

Symbol	Parameter		Min	Typ	Max	Unit
TCIT	TxCLK IN Transition Time (Figure 6)	DUAL = Gnd or V_{CC}	0.8	1.2	2.4	ns
TCIP	TxCLK IN Period (Figure 7)	DUAL = Gnd or V_{CC}	11.76	T	40	ns
TCIH	TxCLK in High Time (Figure 7)		0.4T	0.5T	0.6T	ns
TCIL	TxCLK in Low Time (Figure 7)		0.4T	0.5T	0.6T	ns
VDDQ	Low Swing Voltage Amplitude from GMCH		1.0		1.8	V

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.(1)

Symbol	Parameter		Min	Typ	Max	Unit
LLHT	LVDS Low-to-High Transition Time (Figure 5), PRE = no connect (minimum pre-empahsis).			0.14	0.9	ns
	LVDS Low-to-High Transition Time (Figure 5), PRE = V_{CC} (max. pre-empahsis).			0.11	0.7	ns
LHLT	LVDS High-to-Low Transition Time (Figure 5), PRE = no connect (mini. pre-empahsis).			0.16	0.9	ns
	LVDS High-to-Low Transition Time (Figure 5), PRE = V_{CC} (max. pre-empahsis).			0.11	0.7	ns
TCCS	TxOUT Channel to Channel Skew			100		ps
TPPOS0	Transmitter Output Pulse Position for Bit0 from TxCLKout rising edge.	f = 85MHz (2)	-300	0	+300	ps
TPPOS1	Transmitter Output Pulse Position for Bit1 from TxCLKout rising edge.		1.38	1.68	1.98	ns
TPPOS2	Transmitter Output Pulse Position for Bit2 from TxCLKout rising edge.		3.06	3.36	3.66	ns
TPPOS3	Transmitter Output Pulse Position for Bit3 from TxCLKout rising edge.		4.74	5.04	5.34	ns
TPPOS4	Transmitter Output Pulse Position for Bit4 from TxCLKout rising edge.		6.42	6.72	7.02	ns
TPPOS5	Transmitter Output Pulse Position for Bit5 from TxCLKout rising edge.		8.10	8.40	8.70	ns
TPPOS6	Transmitter Output Pulse Position for Bit6 from TxCLKout rising edge.		9.78	10.08	10.38	ns
TSTC	TxIN Setup to TxCLK IN in low swing mode at 85 MHz (Figure 8)		1.8			ns
THTC	TxIN Hold to TxCLK IN in low swing mode at 85 MHz (Figure 8)		2			ns
TJCC	Transmitter Jitter Cycle-to-cycle (Figure 13 Figure 14) (3), DUAL = Gnd, V_{CC} = 3V	f = 85 MHz		110	150	ps
		f = 65 MHz		80	120	ps
		f = 32.5 MHz		75	115	ps
TPLLS	Transmitter Phase Lock Loop Set (Figure 9)				10	ms
TPDD	Transmitter Powerdown Delay (Figure 10)				100	ns
TPDL	Transmitter Input to Output Latency (Figure 11)	f = 32.5/65/85 MHz (4)		1.5TCIP +4.1		ns

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C. Device tested in Non-Balanced mode only.
(2) The parameters are guaranteed by design. The limits are based on statistical analysis of the device performance over PVT(process, voltage and temperature) range.
(3) The limits are based on bench characterization of the device's jitter response over the power supply voltage range. Output clock jitter is measured with a cycle-to-cycle jitter of ±2ns applied to the input clock signal while data inputs are switching (see Figure 13 and Figure 14). A jitter event of 2ns, represents worse case jump in the clock edge from most graphics VGA chips currently available. This parameter is used when calculating system margin as described in AN-1059.
(4) From V = 1.5V of CLKINP to V_{DIFF}= 0V of CLK1P when R_FB = High, DUAL = Low or High, BAL = Low.

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DIGITAL SWITCHING CHARACTERISTICS for Two-Wire Serial Communication Interface

Unless otherwise noted, below specifications apply for V_{CC}=+3.3V, load capacitance on output lines = 80 pF. Load capacitance on output lines can be up to 400 pF provided that external pull-up switch is on board. The following parameters are the timing relationships between SCL and SDA signals related to the DS90C387R.

Symbol	Parameter	Min	Typ	Max	Unit
t_1	SCL (Clock) Period	2.5			µs
t_2	Data in Set-Up Time to SCL High	100			ns
t_3	Data Out Stable after SCL Low	0			ns
t_4	SDA Low Set-Up Time to SCL Low (Start Condition)	100			ns
t_5	SDA High Hold Time after SCL High (Stop Condition)	100			ns

AC Timing Diagrams

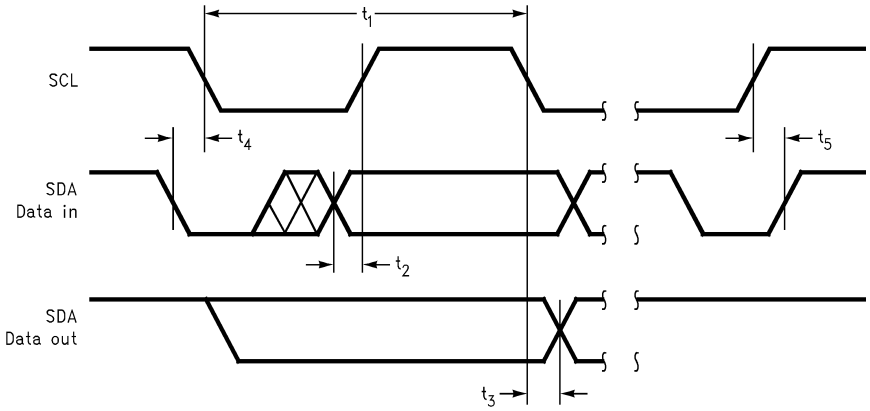

Figure 2. Two-Wire Serial Communication Interface Timing Diagram when I2CSEL = Vcc

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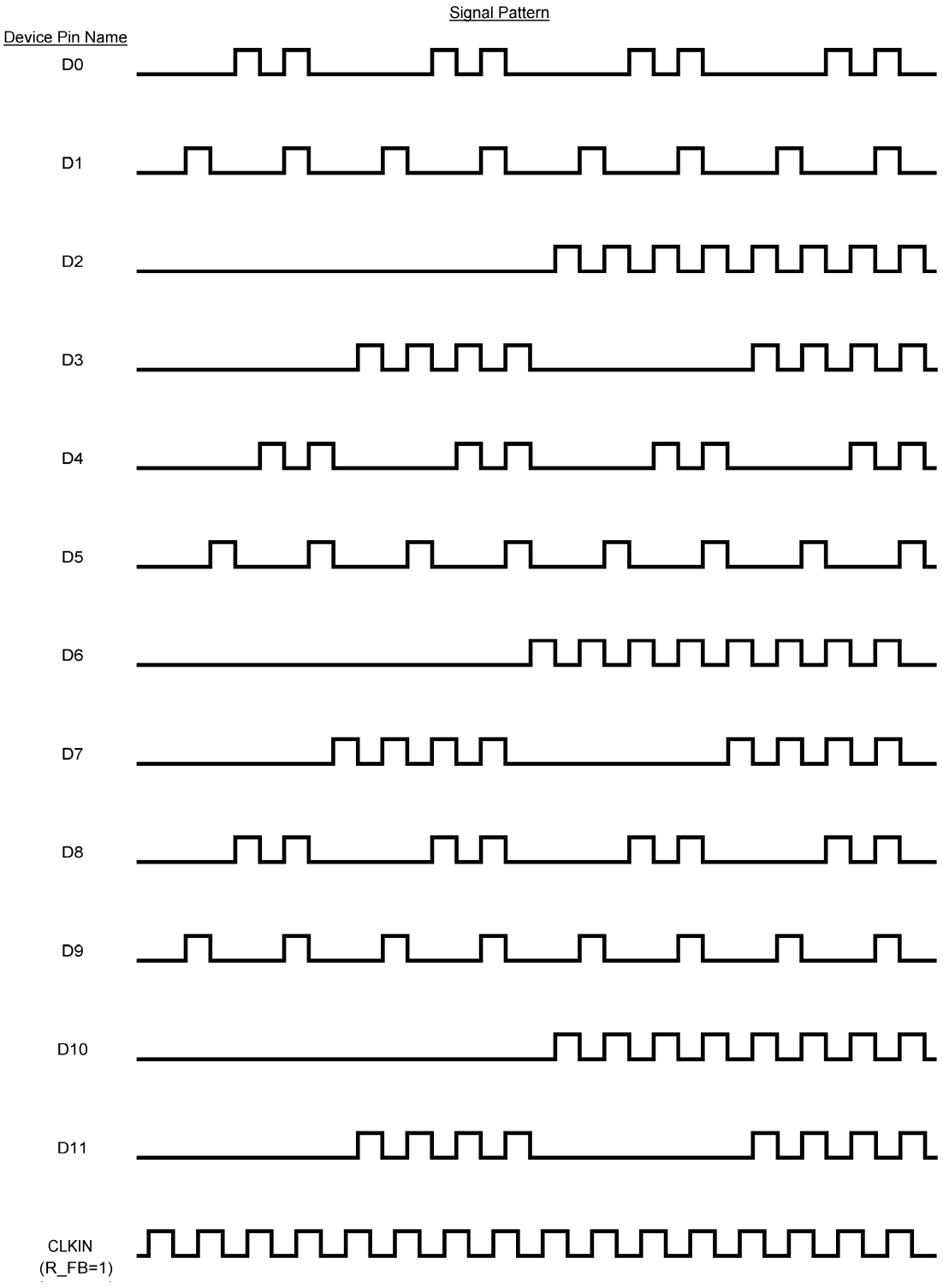

The 16 grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Figure 3. “16 Grayscale” Test Pattern

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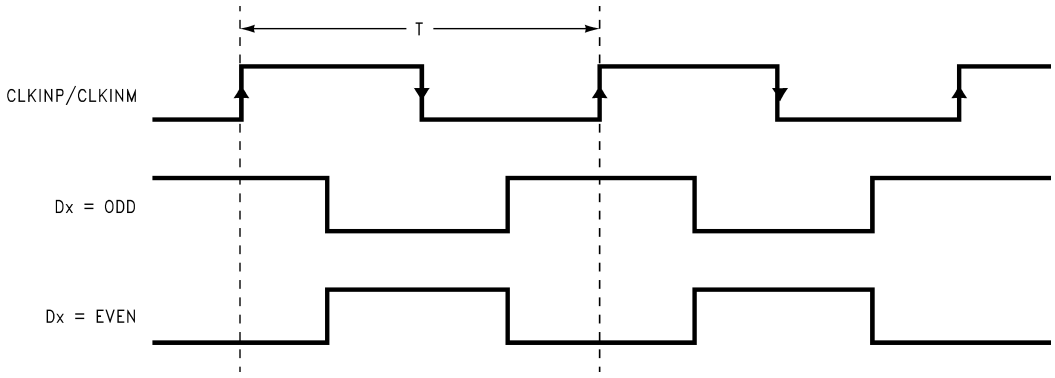

The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Figure 4. "Worst Case" Test Pattern

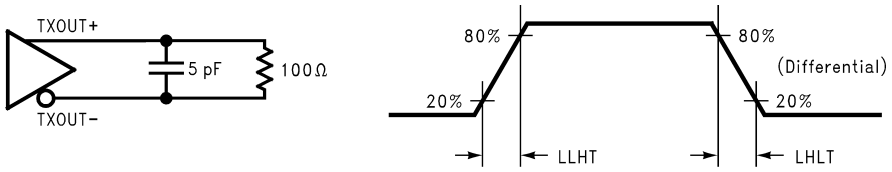

Figure 5. DS90C387R LVDS Output Load and Transition Times

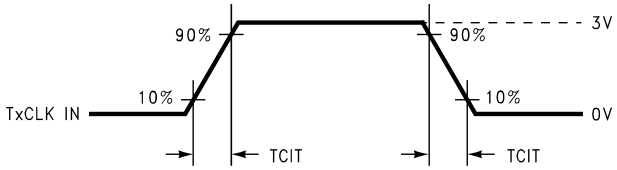

Figure 6. DS90C387R Input Clock Transition Time

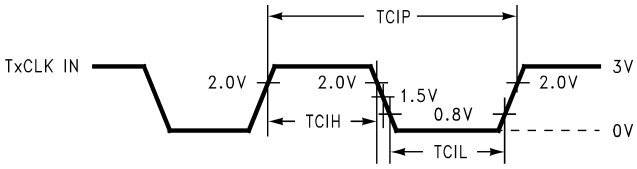

Figure 7. DS90C387R TxCLK IN Period, and High/Low Time (Falling Edge Strobe)

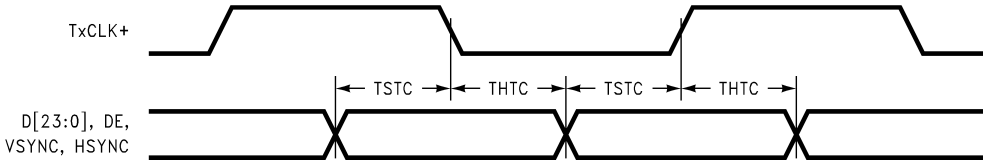

Figure 8. DS90C387R Setup/Hold (Falling Edge Strobe First)

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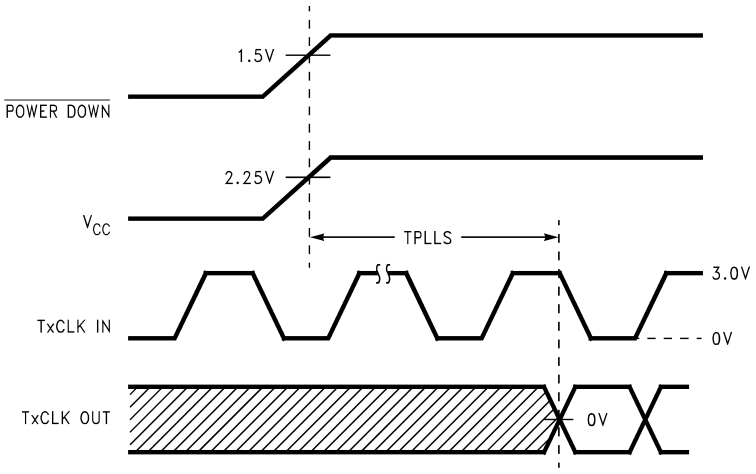


Figure 9. DS90C387R Phase Lock Loop Set Time

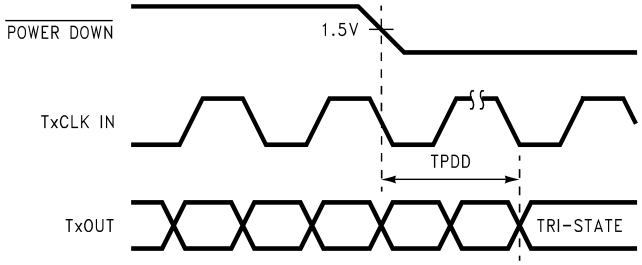
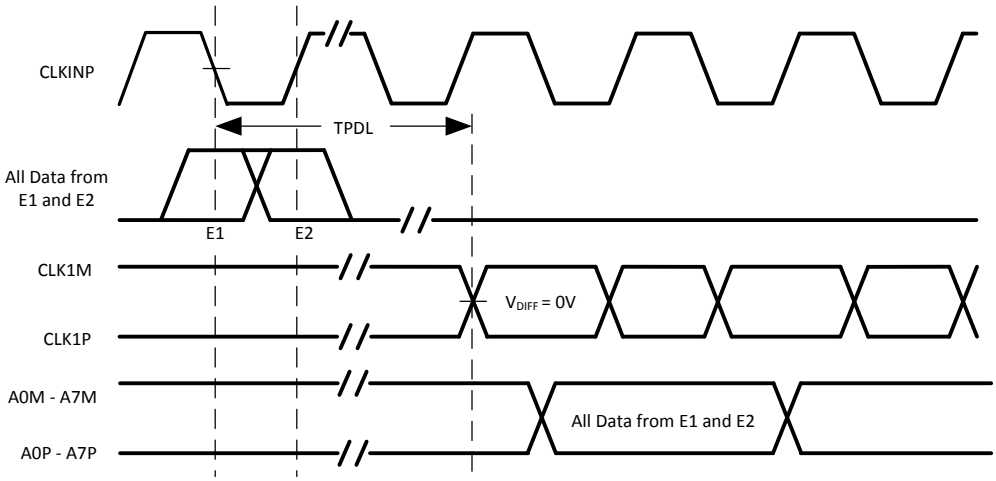
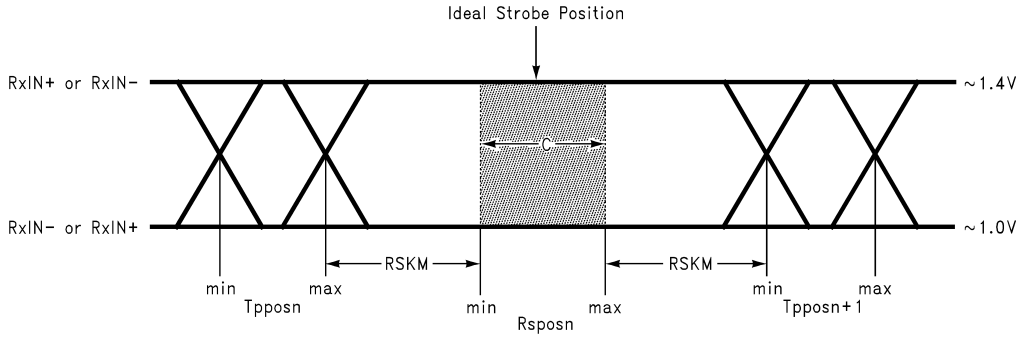


Figure 10. DS90C387R Power Down Delay



NOTE: From V = 1.5V of CLKINP to V_{DIFF}= 0V of CLK1P when R_FB = High, DUAL = Low or High, BAL = Low.

Figure 11. DS90C387R Input to Output Latency



C—Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max
Tppos—Transmitter output pulse position (min and max)
RSKM = Cable Skew (type, length) + Source Clock Jitter (cycle to cycle) + ISI (Inter-symbol interference)
Cable Skew—typically 10 ps–40 ps per foot, media dependent

A. Cycle-to-cycle jitter is less than 150 ps at 85 MHz

B. ISI is dependent on interconnect length; may be zero

Figure 12. Receiver Skew Margin

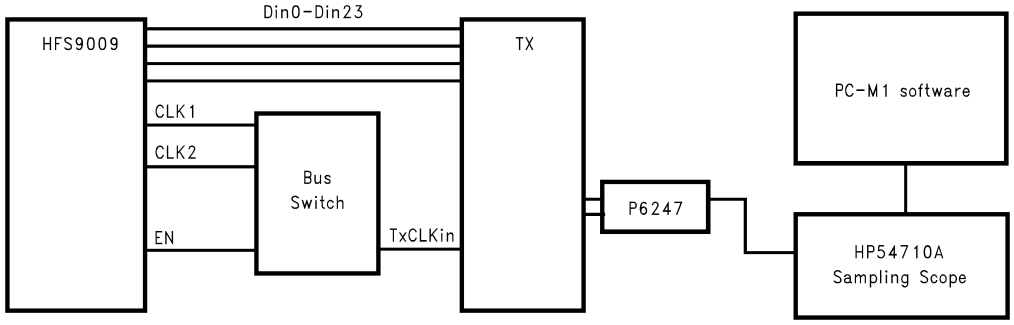


Figure 13. TJCC Test Setup - DS90C387R

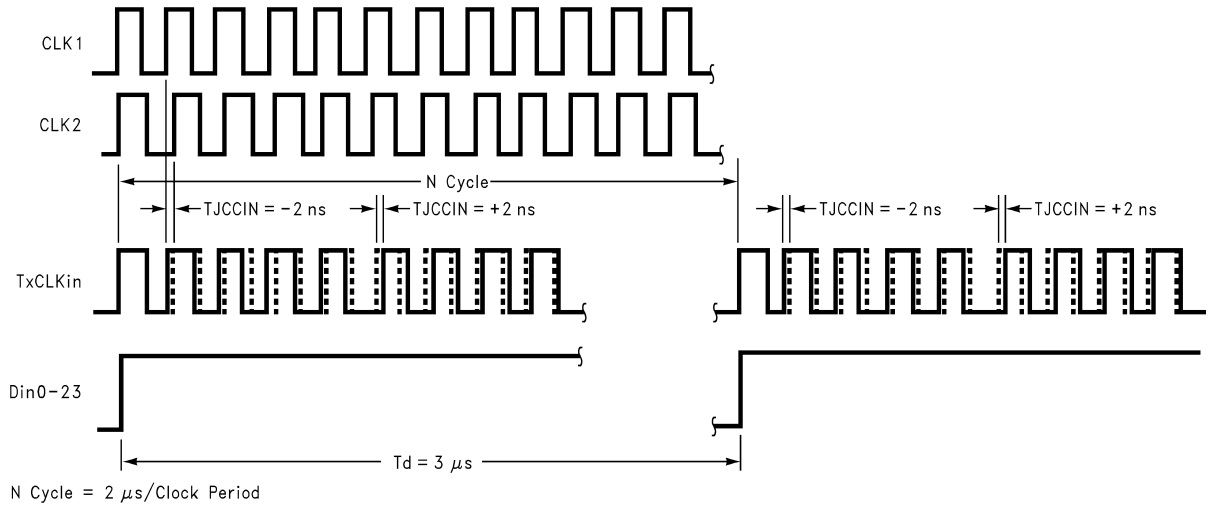


Figure 14. Timing Diagram of the Input Cycle-to-Cycle Clock Jitter

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DS90C387R PIN DESCRIPTION—LDI TRANSMITTER

Pin Name	I/O	No.	Description
D0-D23	I	24	LVTTL level single-ended inputs or low swing pseduo differential inputs. Reference to V_{REF} pin.
			D0-D11 are for 12-bit input mode (24 RGB data); D0-D11 (first 12-bit port) and D12-D23 (second 12-bit port) are for two 12-bit input mode (48 RGB data).
DE	I	1	LVTTL level or low swing level inputs for data enable. This signal is HIGH when input pixel data is valid to DS90C387R provided that R_FDE = HIGH.
HSYNC	I	1	Horizontal Sync input control signal. LVTTL level or low swing level.
VSYNC	I	1	Vertical Horizontal Sync input control signal. LVTTL level or low swing level.
AnP	O	8	Positive LVDS differential data output.
AnM	O	8	Negative LVDS differential data output.
CLKINP	I	1	In LVTTL level operation, this is a single-ended clock. In low swing operation, this is the positive differential clock input .
CLKINM	I	1	In LVTTL level operation, no connect or connect to V_{REF} pin. Do not connect to GND under any condition. In low swing operation, this is negative differential clock input .
R_FB	I	1	LVTTL level input for selecting the Primary clock edge E1. Falling clock edge selected when input is HIGH; Rising clock edge selected when input is LOW.(1)
R_FDE	I	1	LVTTL level input. Programmable control (DE) strobe select. Tie HIGH for data active when DE is HIGH. (1)
CLK1P	O	1	Positive LVDS differential clock output.
CLK1M	O	1	Negative LVDS differential clock output.
$\overline{PD}$	I	1	LVCMOS level input. Input = LOW will place the entire device in power down mode. Outputs of the device will be in TRI-STATE mode to ensure low current at power down. (1)
			Input = HIGH for normal operation.
PLLSEL	I	1	LVTTL level in. Tie to Vcc for normal operation. (1)
BAL	I	1	LVTTL level input. Mode select for dc balanced or non-dc balanced interface. DC balance is active when input is high. (1)
PRE	I	1	Pre-emphasis level select. Pre-emphasis is active when input is tied to V_{CC} through external pull-up resistor. Resistor value determines pre-emphasis level (see table in application section). For normal LVDS drive level (minimum pre-emphasis) leave this pin open (do not tie to ground).(1)
DUAL	I	1	LVTTL level input. Input = LOW for one 12-bit input mode, 24 RGB data in, 24 RGB data out.(1)
			LVTTL level input. Input = V_{CC} for two 12-bit input mode, 48 RGB data in, 48 RGB data out.(1)
V_{CC}	I	1	Connect to power supply with voltage stated under Recommended Operating Conditions. Power supply pin for LVTTL inputs and digital circuitry, pin53.
GND	I	4	Ground pins for LVTTL inputs and digital circuitry, pins 9, 11, 52, 77.
$I2V_{CC}$	I	1	Connect to power supply with voltage stated under Recommended Operating Conditions, pin 68.
V_{CC3V}	I	3	Connect to power supply with voltage stated under Recommended Operating Conditions, pins 70, 79, 95.
GND_{3V}	I	3	Ground pin(s) for powering the data inputs, pins 71, 80, 96.
SGND	I	1	Connect to ground, pin 69.
$PLLV_{CC}$	I	2	Connect to power supply with voltage stated under Recommended Operating Conditions. Power supply pins for PLL circuitry, pin 10, 16.
PLLGND	I	3	Ground pins for PLL circuitry, pins 14, 15, 17.
$LVDSV_{CC}$	I	3	Connect to power supply with voltage stated under Recommended Operating Conditions. Power supply pins for LVDS outputs, pins 30, 40, 48.
LVDSGND	I	4	Ground pins for LVDS outputs, pins 25, 35, 43, 51.
CLK2P/NC	O	1	Additional positive LVDS differential clock output identical to CLK1P. No connect if not used.
CLK2M/NC	O	1	Additional negative LVDS differential clock output identical to CLK1M. No connect if not used.

(1) Inputs default to “low” when left open due to internal pull-down resistor.

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DS90C387R PIN DESCRIPTION—LDI TRANSMITTER (continued)

Pin Name	I/O	No.	Description
V_{REF}	I	1	V_{REF}= 1/2 V_{DDQ}, a "Fixed " line of differential input.
			If V_{REF} ≥ 1.8V, indicates input data is in LVTTL mode.
			If V_{REF} < 1.1V, indicates input data is in low voltage swing mode.
			In low voltage swing mode, input data = logic HIGH = V_{REF} + 100mV.
			In low voltage swing mode, input data = logic LOW = V_{REF} - 100mV.
			This pin is not to be left floating. When not use in LVTTL mode, tie to V_{cc}
I2CSEL	I	1	HIGH to enable two-wire serial communication interface; LOW to disable the interface.
DDREN/I2Cclk	I	1	Always HIGH for one 12-bit port and two 12-bit ports operation. When I2CSEL = HIGH, this is the clock line for the two-wire serial communication interface.
DSEL/I2Cdat	I/O	1	Differential select pin for CLKIN (HIGH = single-ended, LOW = differentail) or when I2CSEL = HIGH, this is the Bidirectional Data line for the two-wire serial communication interface.
A0	I	1	when I2CSEL = HIGH, this is one of the Slave Device Address Lower Bits.
A1	I	1	when I2CSEL = HIGH, this is one of the Slave Device Address Lower Bits.
A2	I	1	when I2CSEL = HIGH, this is one of the Slave Device Address Lower Bits.
MSEN	O	1	Interrupt signal. This is an open drain output, pull-up resistor is required.
TST1		1	Test pin, tie to Vcc.
TST2		1	Test pin, no connect. Do not tie to ground.
RESERVED1		1	Reserved pin, tie to ground.
RESERVED2		1	Reserved pin, tie to ground.
RESERVED3		1	Reserved pin, no connect. Do not tie to ground.
RESERVED4		1	Reserved pin, tie to ground.
RESERVED5		1	Reserved pin, tie to ground.
RESERVED6		1	Reserved pin, tie to ground.
RESERVED7		1	Reserved pin, tie to ground.
RESERVED8		1	Reserved pin, tie to ground.
RESERVED9		1	Reserved pin, tie to ground.

Table 2. Control Settings for mode selection

Mode	12bit	Two 12-bit
DUAL	L	H
BAL	L/H	L/H
I2CSEL	L	L
DDREN/I2Cclk	H	H
CLKIN polarity	R_FB	R_FB
CLKIN,single-ended/ differentail	DSEL	DSEL
Description	12-bit in, 24-bit pixel out, non-DC Balanced or DC-Balanced	Two 12-bit in, two 24-bit pixels out, non-DC Balanced or DC-Balanced.

Table 3. Relationship between R_FB, DE, HSYNC and VSYNC pins

R_FB	Primary Edge	Secondary Edge	DE latches on	HSYNC latches on	VSYNC latches on
VCC	Falling	Rising	Rising	Falling	Falling
GND	Rising	Falling	Falling	Rising	Rising

Two-Wire Serial Communication Interface Description

The DS90C387R operates as a slave on the Serial Bus, so the SCL line is an input (no clock is generated by the DS90C387R) and the SDA line is bi-directional. DS90C387R has a 7-bit slave address. The address bits are controlled by the state of the address select pins A2, A1 and A0, and are set by connecting these pins to ground for a LOW, (0) , to V_{CC} for a HIGH, (1).

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Therefore, the complete slave address is:

A6	A5	A4	A3	A2	A1	A0
MSB						LSB

and is selected as follows:

Address Select Pin State			DS90C387R Serial Bus Slave Address
A2	**A1**	**A0**	**A6:A0 binary**
0	0	0	0111000
0	0	1	0111001
0	1	0	0111010
0	1	1	0111011
1	0	0	0111100
1	0	1	0111101
1	1	0	0111110
1	1	1	0111111

The DS90C387R latches the state of the address select pins during the first read or write on the Serial Bus. Changing the state of the address select pins after the first read or write to any device on the Serial Bus will not change the slave address of the DS90C387R.

A zero in front of the register address is required as the most left column shown in Table 4. For example, to access register F, “0F” is the correct way of accessing the register.

Table 4. Register Mapping

Addr	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
000	VND_IDL(RO)							
001	VND_IDH(RO)							
002	DEV_IDL(RO)							
003	DEV_IDH(RO)							
004	DEV_REV(RO)							
005	RSVD[7:0](RO)							
006	FRQ_LOW[7:0](RO)							
007	FRQ_HIGH[7:0](RO)							
008	RSVD[1:0]		VEN(RW)	HEN(RW)	DSEL(RW)	BSEL(RW)	EDGE(RW)	PD(RW)
009	VLOW(RO)	MSEL[2:0](RW)			TSEL(RW)	RSEN(RO)	HTPLG(RO)(1)	MDI(RW)
00A	DK[3:1](RW)(1)			DKEN(RW)(1)	CTL[3:1](RW)			RSVD(RW)
00B	CFG[7:0](RO)(1)							
00C	VDJK[7:0](RW)(1)							
00D	RSVD[3:0](RW)				RSVD[3:0](RO)			
00E	RSVD[7:0](RW)							
00F	RSVD[7:0](RW)							

(1) Features not implemented on DS90C387R

Table 5. Register Field Definitions

Field	Access	Description
VND_IDL	RO	Vendor ID low byte, value is 05h.
VND_IDH	RO	Vendor ID high byte, value is 13h.
DEV_IDL	RO	Device ID low byte, value is 24h.
DEV_IDH	RO	Device ID high byte, value is 67h.
DEV_REV	RO	Device revision, value is 00h.

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Table 5. Register Field Definitions (continued)

Field	Access	Description
FRQ_LOW	RO	25 MHz is Low frequency limit for the current mode, value is 19h.
FRQ_HIGH	RO	85 MHz is High frequency limit for the current mode, value is 55h.
PD	RW	Power down mode, default = 1.
		0 - power down only the LVDS drivers. Output of this device will be in TRI-STATE mode. Other circuitry are still active.
		1 - normal operation.
EDGE	RW	Edge select (same function as R_FB pin), default = 1.
		0 - input data is rising edge latched (rising edge latched first in 12-bit and two 12-bit mode).
		1 - input data is falling edge latched (falling edge latched first in 12-bit and two 12-bit mode).
BSEL	RW	Input bus select (same as DUAL pin), default = 0.
		0 - one 12-bit bus.
		1 - two 12-bit bus.
DSEL	RW	Dual level clock select (same function as DSEL pin), default = 1.
		0 - input clock is differential.
		1 - input clock is single-ended (up to 65MHz). CLKINM and V_{REF} pin are internally connected.
HEN	RW	Horizontal sync enable, default = 1.
		0 - HSYNC input is transmitted as fixed LOW.
		1 - HSYNC input is transmitted as it is.
VEN	RW	Vertical sync enable, default = 1.
		0 - VSYNC input is transmitted as fixed LOW.
		1 - VSYNC input is transmitted as it is.
MDI	RW	Monitor Detect Interrupt, default = 1.
		0 - Detection signal has changed logical level (write "1" to this bit to clear).
		1 - Detection signal has not changed state.
HTPLG(1)	RO	Feature not implemented.
RSEN	RO	This bit is a ”1 “ if a powered on receiver is connected to the transmitter outputs, ” 0 “ otherwsie. This function is only available for use in DC-coupled systems. Default=0.
TSEL	RW	Interrupt generation method, default=0.
		0 - Interrupt bit (MDI) is generated by monitoring RSEN.
		1 - Interrupt bit (MDI) is generated by monitoring HTPLG.
MSEL [2:0]	RW	Select source for the MSEN output pin. Default valus is 001.
		000 - Force MSEN output HIGH (disabled).
		001 - Output the value of MDI bit (interrupt). This is default.
		010 - Output the value of RSEN bit (receiver detect).
		011 - Output the value of HTPLG bit (hot plug detect).
		1xx - Reserved.
VLOW	RO	This bit is an 1 if the VREF signal indicates low swing inputs. Default=1.
		It is a 0 if VREF indicates high swing inputs.
CTL [3:1]	RW	General purpose inputs.
CFG [7:0](1)	RO	Feature not implemented.
VDJK [7:0](1)	RW	Reserved.
DK [3:1](1)	RW	Feature not implemented.
DKEN(1)	RW	Feature not implemented.

(1) Features not implemented on DS90C387R

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Communicating with the DS90C387R through Registers

There are 31 data registers in the DS90C387R, and can be accessed through sixteen register addresses. All registers are predefined as read only, or read and write. The device will always attempt to detect if a LCD panel/monitor is connected.

A **Write** to the DS90C387R will always include the slave address byte, data register address byte, a data byte.

Reading the DS90C387R can take place either of two ways:

1. If the location latched in the data register addresses is correct , then the read can simply consist of a slave address byte, followed by retrieving the data byte.
2. If the data register address needs to be set, then a slave address byte, data register address will be sent first, then the master will repeat start, send the slave address byte and data byte to accomplish a read.

The data byte has the most significant bit first. At the end of a read, the DS90C387R can accept either Acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).

Two-Wire Serial Communication Interface for Slave

The DS90C387R slave state machine does not require an internal clock and it supports only byte read and write. Page mode is not supported. The 7-bit binary address is "0111$A_2A_1A_0$", where $A_2A_1A_0$ are pin programmable to " 1" or " 0 " and the " 0111 " is hardwired internally.

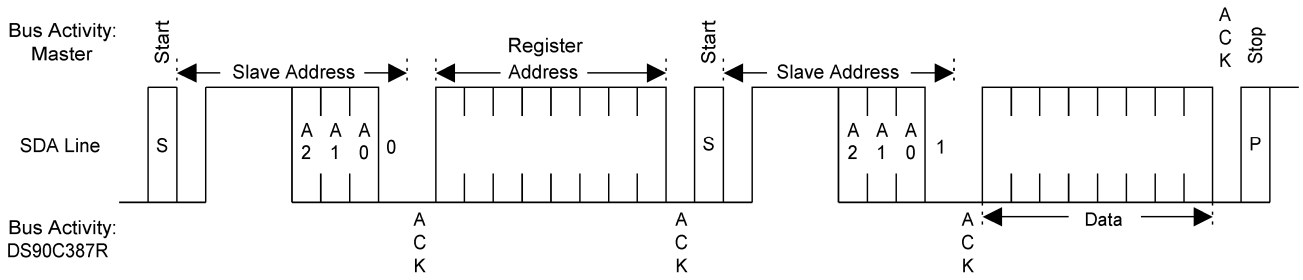

Figure 15. Byte Read

The master must generate a " Start " by sending the 7-bit slave address plus a 0 first, and wait for acknowledge from DS90C387R. When DS90C387R acknowledges (the 1st ACK) that the master is calling, the master then sends the data register address byte and waits for acknowledge from the slave. When the slave acknowledges (the 2nd ACK), the master repeats the " Start " by sending the 7-bit slave address plus a 1 (indicating that READ operation is in progress) and waits for acknowledge from DS90C387R. After the slave responds (the 3rd ACK), the slave sends the data to the bus and waits for acknowledge from the master. When the master acknowledges (the 4th ACK), it generates a " Stop ". This completes the " READ ".

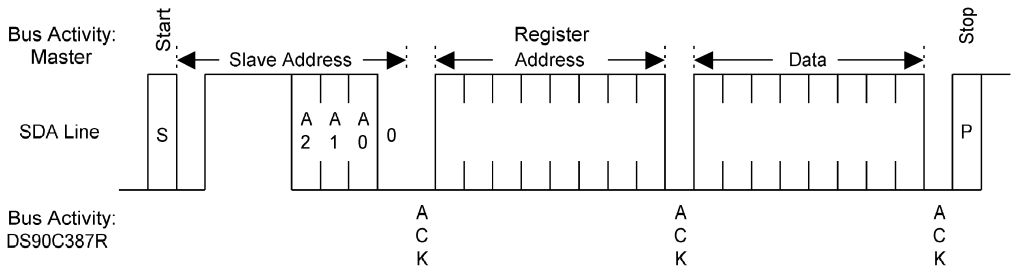

Figure 16. Byte Write

The master must generate a " Start ", by sending the 7-bit slave address plus a 0 and wait for acknowledge from DS90C387R. When DS90C387R acknowledges (the 1st ACK) that the master is calling, the master then sends the data register address byte and waits for acknowledge from the slave. When the slave acknowledges (the 2nd ACK), the master sends the data byte and wait for acknowledge from the slave. When the slave acknowledges (the 3rd ACK), the master generates a " Stop ". This completes the " WRITE ".

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LVDS Interface

Table 6. LVDS data bit naming convention(1)

X	Y	Z	Description
X=R			Red
X=G			Green
X=B			Blue
	Y=1		Odd (First) Pixel
	Y=2		Even (Second) Pixel
		Z=0-7	LVDS bit number (not VGA controller LSB to MSB)

(1) For a 48-bit dual pixel application - LSB (Less Significant Bit) = R16,G16,B16,R26,G26,B26 and MSB (Most Significant Bit) = R15,G15,B15,R25,G25,B25.

Table 7. 12-bit (two data per clock) data mapping(1)

VGA - TFT Data Signals Color Bits		Transmitter input pin names	Receiver output pin names	TFT Panel Data Signals	
	24-bit	DS90C387R	DS90CF388	18-bit	24-bit
LSB	R0	E2-D4	R16		R0
	R1	E2-D5	R17		R1
	R2	E2-D6	R10	R0	R2
	R3	E2-D7	R11	R1	R3
	R4	E2-D8	R12	R2	R4
	R5	E2-D9	R13	R3	R5
	R6	E2-D10	R14	R4	R6
MSB	R7	E2-D11	R15	R5	R7
LSB	G0	E1-D8	G16		G0
	G1	E1-D9	G17		G1
	G2	E1-D10	G10	G0	G2
	G3	E1-D11	G11	G1	G3
	G4	E2-D0	G12	G2	G4
	G5	E2-D1	G13	G3	G5
	G6	E2-D2	G14	G4	G6
MSB	G7	E2-D3	G15	G5	G7
LSB	B0	E1-D0	B16		B0
	B1	E1-D1	B17		B1
	B2	E1-D2	B10	B0	B2
	B3	E1-D3	B11	B1	B3
	B4	E1-D4	B12	B2	B4
	B5	E1-D5	B13	B3	B5
	B6	E1-D6	B14	B4	B6
MSB	B7	E1-D7	B15	B5	B7

(1) DUAL=GND, BAL=Vcc/GND, only A0-A3 are used

Table 8. Two 12-bit (two data per clock) data mapping(1)

VGA - TFT Data Signals Color Bits		Transmitter input pin names	Receiver output pin names	TFT Panel Data Signals	
	24-bit	DS90C387R	DS90CF388	18-bit	24-bit
Port 1-Primary (odd pixel/first RGB pixel)					
LSB	R0	E2-D4	R16		R0

(1) DUAL=GND, BAL=Vcc/GND, only A0-A3 are used

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Table 8. Two 12-bit (two data per clock) data mapping[1] (continued)

VGA - TFT Data Signals Color Bits		Transmitter input pin names	Receiver output pin names	TFT Panel Data Signals	
	R1	E2-D5	R17		R1
	R2	E2-D6	R10	R0	R2
	R3	E2-D7	R11	R1	R3
	R4	E2-D8	R12	R2	R4
	R5	E2-D9	R13	R3	R5
	R6	E2-D10	R14	R4	R6
MSB	R7	E2-D11	R15	R5	R7
LSB	G0	E1-D8	G16		G0
	G1	E1-D9	G17		G1
	G2	E1-D10	G10	G0	G2
	G3	E1-D11	G11	G1	G3
	G4	E2-D0	G12	G2	G4
	G5	E2-D1	G13	G3	G5
	G6	E2-D2	G14	G4	G6
MSB	G7	E2-D3	G15	G5	G7
LSB	B0	E1-D0	B16		B0
	B1	E1-D1	B17		B1
	B2	E1-D2	B10	B0	B2
	B3	E1-D3	B11	B1	B3
	B4	E1-D4	B12	B2	B4
	B5	E1-D5	B13	B3	B5
	B6	E1-D6	B14	B4	B6
MSB	B7	E1-D7	B15	B5	B7
Port 2-Secondary (even pixel/second RGB pixel)					
LSB	R0	E2-D16	R26		R0
	R1	E2-D17	R27		R1
	R2	E2-D18	R20	R0	R2
	R3	E2-D19	R21	R1	R3
	R4	E2-D20	R22	R2	R4
	R5	E2-D21	R23	R3	R5
	R6	E2-D22	R24	R4	R6
MSB	R7	E2-D23	R25	R5	R7
LSB	G0	E1-D20	G26		G0
	G1	E1-D21	G27		G1
	G2	E1-D22	G20	G0	G2
	G3	E1-D23	G21	G1	G3
	G4	E2-D12	G22	G2	G4
	G5	E2-D13	G23	G3	G5
	G6	E2-D14	G24	G4	G6
MSB	G7	E2-D15	G25	G5	G7
LSB	B0	E1-D12	B26		B0
	B1	E1-D13	B27		B1
	B2	E1-D14	B20	B0	B2
	B3	E1-D15	B21	B1	B3
	B4	E1-D16	B22	B2	B4
	B5	E1-D17	B23	B3	B5
	B6	E1-D18	B24	B4	B6

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Table 8. Two 12-bit (two data per clock) data mapping[1] (continued)

VGA - TFT Data Signals Color Bits		Transmitter input pin names	Receiver output pin names	TFT Panel Data Signals	
MSB	B7	E1-D19	B25	B5	B7

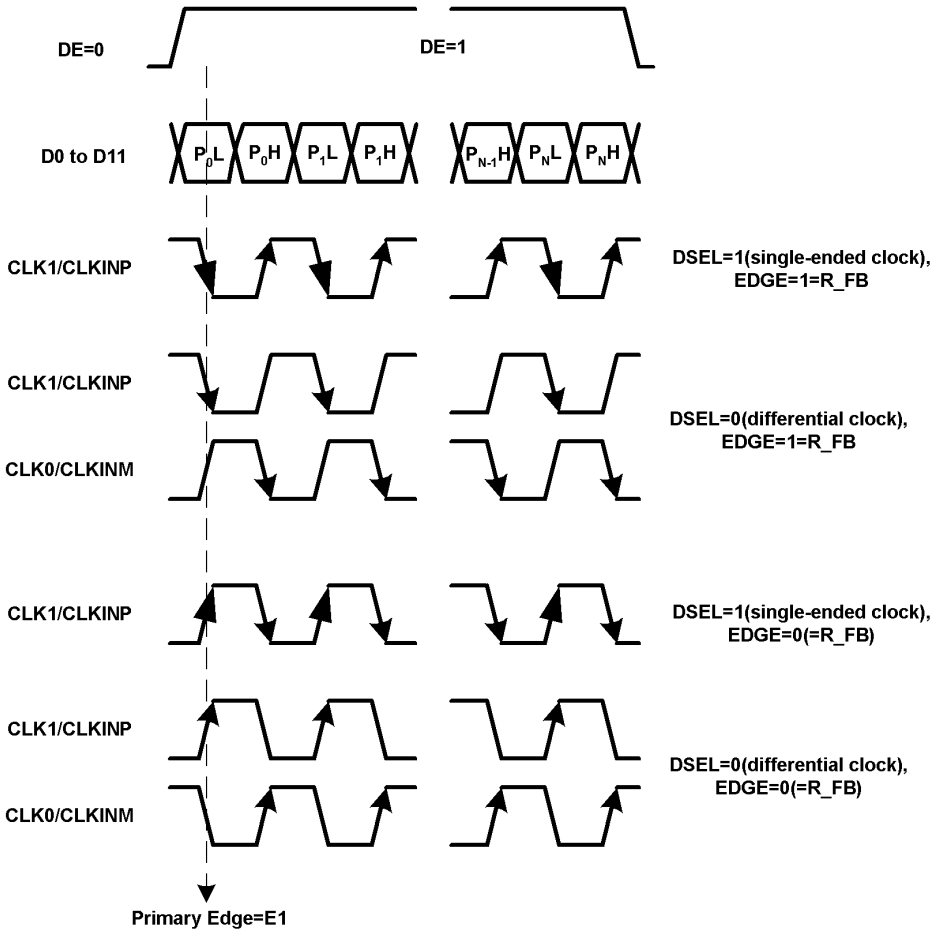

Figure 17. How ds90c387r Latch Data

Table 9. 12-bit (two data per clock) input application data mapping with GMCH.

	P0		P1		P2	
	P0L	P0H	P1L	P1H	P2L	P2H
Pin Name	Low	High	Low	High	Low	High
D11	G0[3]	R0[7]	G1[3]	R1[7]	G2[3]	R2[7]
D10	G0[2]	R0[6]	G1[2]	R1[6]	G2[2]	R2[6]
D9	G0[1]	R0[5]	G1[1]	R1[5]	G2[1]	R2[5]
D8	G0[0]	R0[4]	G1[0]	R1[4]	G2[0]	R2[4]
D7	B0[7]	R0[3]	B1[7]	R1[3]	B2[7]	R2[3]
D6	B0[6]	R0[2]	B1[6]	R1[2]	B2[6]	R2[2]
D5	B0[5]	R0[1]	B1[5]	R1[1]	B2[5]	R2[1]
D4	B0[4]	R0[0]	B1[4]	R1[0]	B2[4]	R2[0]
D3	B0[3]	G0[7]	B1[3]	G1[7]	B2[3]	G2[7]
D2	B0[2]	G0[6]	B1[2]	G1[6]	B2[2]	G2[6]
D1	B0[1]	G0[5]	B1[1]	G1[5]	B2[1]	G2[5]

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Table 9. 12-bit (two data per clock) input application data mapping with GMCH. (continued)

	P0		P1		P2	
	P0L	P0H	P1L	P1H	P2L	P2H
Pin Name	Low	High	Low	High	Low	High
D0	B0[0]	G0[4]	B1[0]	G1[4]	B2[0]	G2[4]

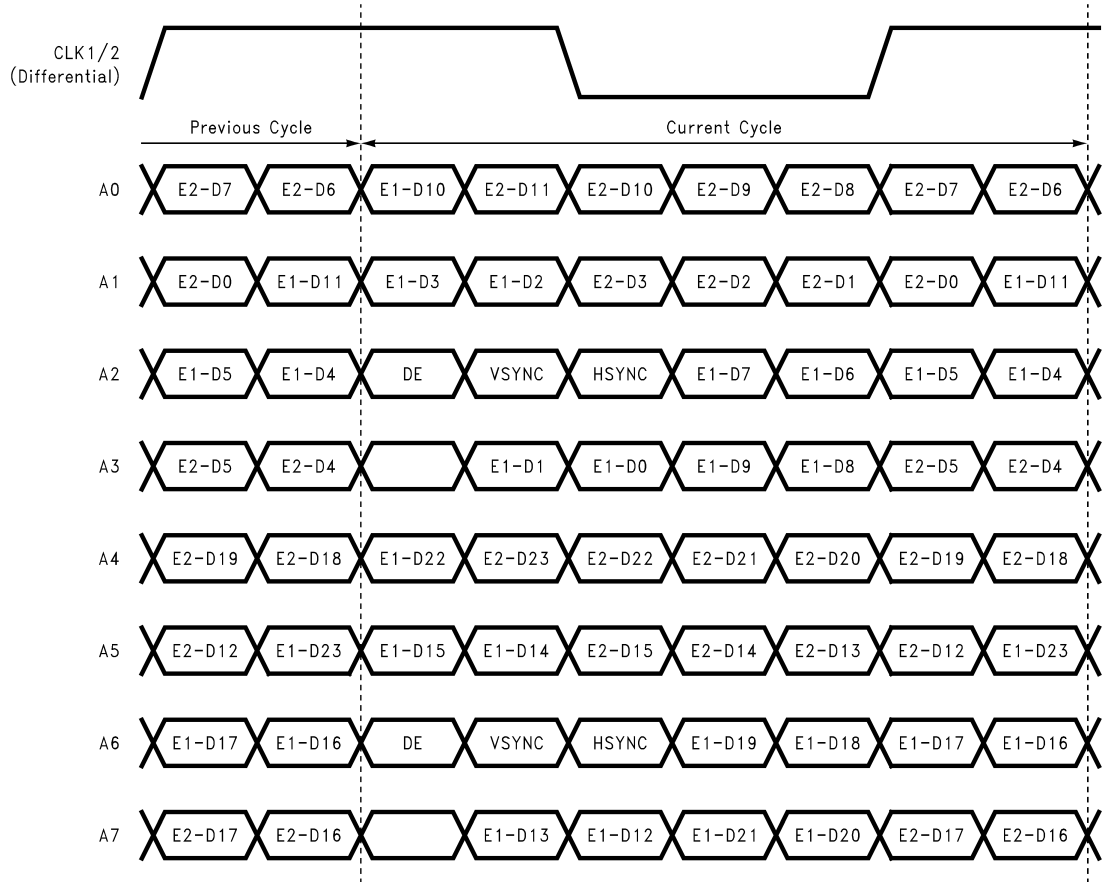

Figure 18. TTL Data Inputs Mapped to LVDS Outputs
Non-DC Balanced Mode (Backward Compatible, BAL=Low, A0 to A3 for Port1, A4 to A7 for Port2)

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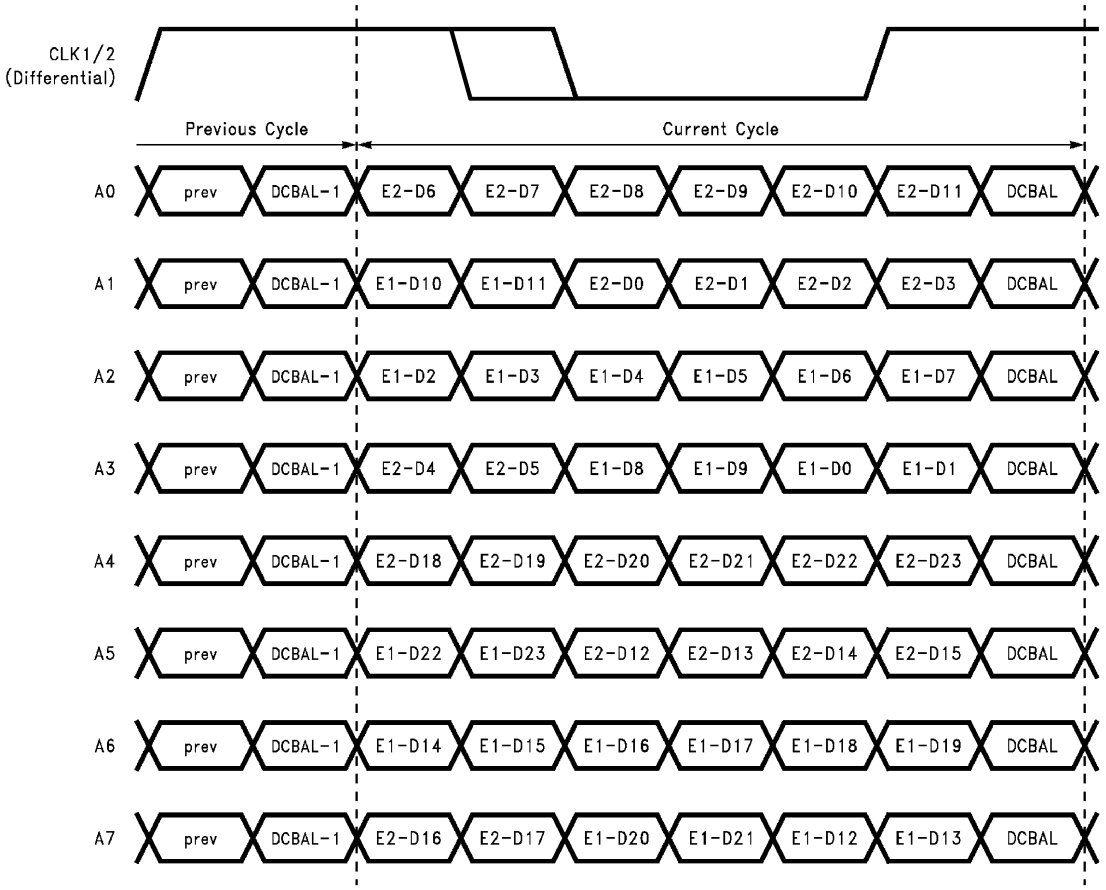

Figure 19. 48 Parallel TTL Data Inputs Mapped to LVDS Outputs DC Balanced Mode (Data Enabled, BAL=High, A0 to A3 for Port1, A4 to A7 for Port2)

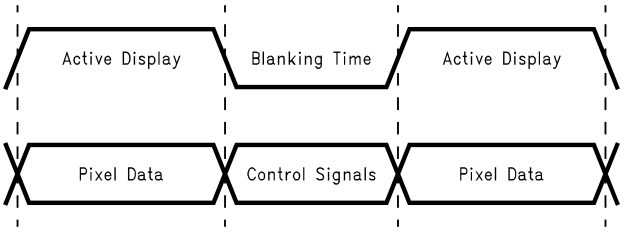

Figure 20. Control Signals Transmitted During Blanking in DC-Balance mode

Table 10. Control Signals Transmitted During Blanking in DC-Balance mode

Control Signal	Signal Level	Channel	Pattern
DE	HIGH	CLK1	1111000 or 1110000
	LOW		1111100 or 1100000
HSYNC	HIGH	A0	1100000 or 1111100
	LOW		1110000 or 1111000
VSYNC	HIGH	A1	1100000 or 1111100
	LOW		1110000 or 1111000

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APPLICATIONS INFORMATION

How to configure the DS90C387R to work with DS90CF384/DS90CF384A/DS90CF386 or DS90CF388 for most common application:

1. To configure for single pixel application using the DS90C387R to interface with GMCH host, please see table below for reference pin connection and configuration. Due to the implementation differences among various GMCH vendors, the table is using the GMCH vendor located in Santa Clara, California, USA as an example. A two-wire serial communication interface based EEPROM containing EDID 128 bytes LCD timing information may be required depending on device driver implementation.

From DS90C387R	To GMCH
data signal connection	
D0	D0
D1	D1
D2	D2
D3	D3
D4	D4
D5	D5
D6	D6
D7	D7
D8	D8
D9	D9
D10	D10
D11	D11
CLKINP	CLK1
CLKINM	CLK0
DE	BLANK
HSYNC	HSYNC
VSYNC	VSYHC
configuration for other pins	
DDRENI2Cclk	I2CCLK
DSELI2Cdat	I2CDATA
A0	GND
A1	GND
A2	GND
PLLSEL	Vcc
DUAL	GND
BAL	GND
D12 to D23	No connect
RESERVED1	GND
RESERVED2	GND
RESERVED3	No connect
RESERVED4	GND
RESERVED5	GND
RESERVED6	GND
RESERVED7	GND
RESERVED8	GND
RESERVED9	GND
TST1	Vcc
TST2	No connect
VREF	VREF

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From DS90C387R	To GMCH
MSEN	INT#

2. To configure for single pixel application using the DS90C387R with single DS90CF384 or DS90CF384A or DS90CF386 LVDS based LCD panel or monitor, the “DUAL” pin must be set to Gnd (single RGB), and “BAL” pin must be set to Gnd to disable the feature for DS90CF384/DS90CF386 doesn't support DC balance function. For cable length more than two meters, pre-emphasis feature is recommended. Please see table below for reference pin connection.

From DS90C387R Output Pins	To LVDS based LCD monitor
data signal connection	
A0M	RxIN0−
A0P	RxIN0+
A1M	RxIN1−
A1P	RxIN1+
A2M	RxIN2−
A2P	RxIN2+
CLK1M	RxCLKIN0−
CLK1P	RxCLKIN0+
A3M(valid for 8-bit LCD only; no connect for 6-bit LCD)	RxIN3−(valid for 8-bit LCD only; no connect for 6-bit LCD)
A3P(valid for 8-bit LCD only; no connect for 6-bit LCD)	RxIN3+(valid for 8-bit LCD only; no connect for 6-bit LCD)
A4M	No connect
A4P	No connect
A5M	No connect
A5P	No connect
A6M	No connect
A6P	No connect
A7M	No connect
A7P	No connect
CLK2M	No connect
CLK2P	No connect

3. To configure for single pixel or dual pixel application using the DS90C387R with DS90CF388, the “DUAL” pin must be set to Vcc (dual RGB) or Gnd (single RGB). Also, “BAL” pins on both devices have to in the same logic state. For cable length more than two meters, pre-emphasis feature is recommended.

4. In dual mode, DS90C387R has two LVDS clock outputs enabling an interface to two FPD-Link 'notebook' receivers (DS90CF384/DS90CF386). “BAL” pin must be set to Gnd to disable DC balance function for DS90CF384/DS90CF386 doesn't support DC balance function. In single mode, outputs A4-to-A7 and CLK2 are disabled which reduces power dissipation. For cable length more than two meters, pre-emphasis feature is recommended.

The DS90CF388 is able to support single or dual pixel interface up to 112MHz operating frequency. This receiver may also be used to interface to a VGA controller with an integrated LVDS transmitter without DC balance data transmission. In this case, the receivers “BAL” pin must be tied low (DC balance disabled).

Features Description:

1. Pre-emphasis: adds extra current during LVDS logic transition to reduce the cable loading effects. Pre-emphasis strength is set via a DC voltage level applied from min to max (0.75V to Vcc) at the “PRE” pin. A higher input voltage on the ”PRE” pin increases the magnitude of dynamic current during data transition. The “PRE” pin requires one pull-up resistor (Rpre) to Vcc in order to set the DC level. There is an internal resistor network, which cause a voltage drop. Please refer to the tables below to set the voltage level.

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Table 11. Pre-emphasis DC voltage level with (Rpre)

Rpre	Resulting PRE Voltage	Effects
1MΩ or NC	0.75V	Standard LVDS
50kΩ	1.0V	
9kΩ	1.5V	50% pre-emphasis
3kΩ	2.0V	
1kΩ	2.6V	
100Ω	Vcc	100% pre-emphasis

Table 12. Pre-emphasis needed per cable length

Frequency	PRE Voltage	Typical cable length
85MHz	1.5V	7 meters
65MHz	1.5V	10 meters

2. DC Balance: In the balanced operating modes, in addition to pixel and control information an additional bit is transmitted on every LVDS data signal line during each cycle of active data as shown in Figure 19. This bit is the DC balance bit (DCBAL). The purpose of the DC Balance bit is to minimize the short- and long-term DC bias on the signal lines. This is achieved by selectively sending the pixel data either unmodified or inverted.

The value of the DC balance bit is calculated from the running word disparity and the data disparity of the current word to be sent. The data disparity of the current word shall be calculated by subtracting the number of bits of value 0 from the number of bits value 1 in the current word. Initially, the running word disparity may be any value between +7 and −6. The running word disparity shall be calculated as a continuous sum of all the modified data disparity values, where the unmodified data disparity value is the calculated data disparity minus 1 if the data is sent unmodified and 1 plus the inverse of the calculated data disparity if the data is sent inverted. The value of the running word disparity shall saturate at +7 and −6.

The value of the DC balance bit (DCBAL) shall be 0 when the data is sent unmodified and 1 when the data is sent inverted. To determine whether to send pixel data unmodified or inverted, the running word disparity and the current data disparity are used. If the running word disparity is positive and the current data disparity is positive, the pixel data shall be sent inverted. If the running word disparity is positive and the current data disparity is zero or negative, the pixel data shall be sent unmodified. If the running word disparity is negative and the current data disparity is positive, the pixel data shall be sent unmodified. If the running word disparity is negative and the current data disparity is zero or negative, the pixel data shall be sent inverted. If the running word disparity is zero, the pixel data shall be sent inverted.

Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference). With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable. These enhancements allow cables 5 to 10+ meters in length to be driven. Quality of the cable can affect the length.

The data enable control signal (DE) is used in the DC balanced mode to distinguish between pixel data and control information being sent. It must be continuously available to the device in order to correctly separate pixel data from control information. For this reason, DE shall be sent on the clock signals, LVDS CLK1 and CLK2, when operating in the DC balanced mode. If the value of the control to be sent is 1 (active display), the value of the control word sent on the clock signals shall be 1111000 or 1110000. If the value of the control to be sent is 0 (blanking time), the value of the control word sent on the clock signals shall be 1111100 or 1100000.

The control information, such as HSYNC and VSYNC, is always sent unmodified. The value of the control word to send is determined by the running word disparity and the value of the control to be sent. If the running word disparity is positive and the value of the control to be sent is 0, the control word sent shall be 1110000. If the running word disparity is zero or negative and the control word to be sent is 0, the control word sent shall be 1111000. If the running word disparity is positive and the value of the control to be sent is 1, the control word sent shall be 1100000. If the running word disparity is zero or negative and the value of the control to be sent is 1, the control word sent shall be 1111100. The DC Balance bit shall be sent as 0 when sending control information during blanking time. See Figure 20.

In backward compatible mode (BAL=low) control and data is sent as regular LVDS data. See Figure 18.

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Backwards Compatible Mode with FPD-Link

The transmitter provides a second LVDS output clock. Both LVDS clocks will be identical in 'Dual pixel mode'. This feature supports backward compatibility with the previous generation of devices - the second clock allows the transmitter to interface to panels using a 'dual pixel' configuration of two 24-bit or 18-bit 'notebook' receivers.

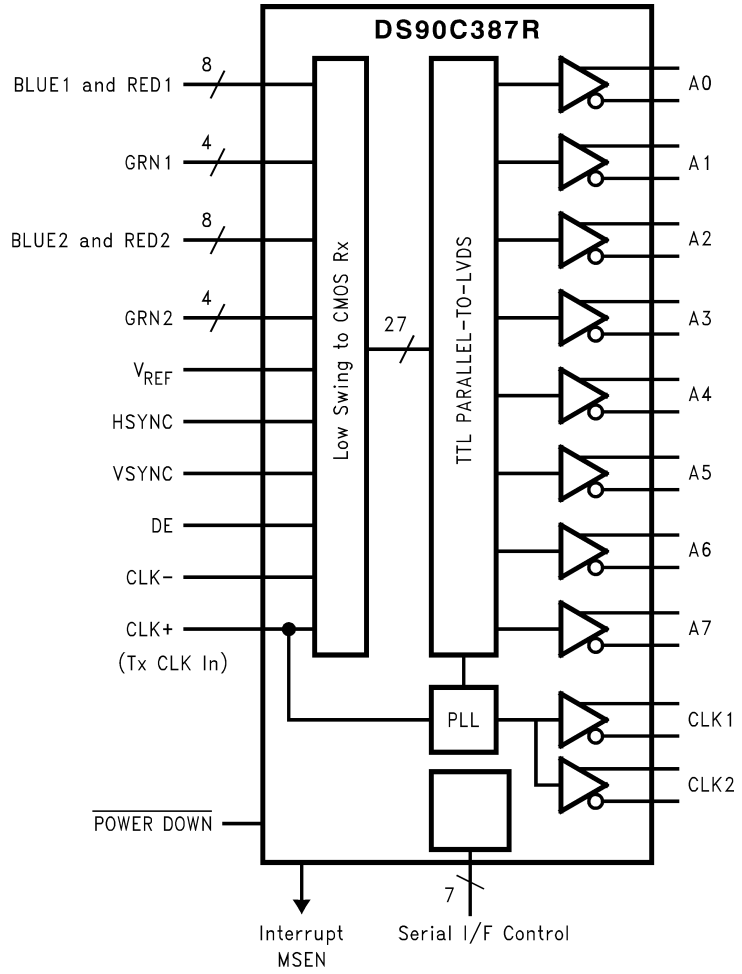
Pre-emphasis feature is available for use in both the DC balanced and non-DC balanced (backwards compatible) modes.

Information on Jitter Rejection:

The transmitter is designed to reject cycle-to-cycle jitter which may be seen at the transmitter input clock. Very low cycle-to-cycle jitter is passed on to the transmitter outputs. This significantly reduces the impact of jitter provided by the input clock source, and improves the accuracy of data sampling. Data sampling is further enhanced by automatically calibrated data sampling strobes at the receiver inputs. Timing and control signals (VSYNC, HSYNC, DE) are sent during blanking intervals to guarantee correct reception of these critical signals.

The transmitter is offered with programmable primary clock edge for convenient interface with a variety of graphics controllers. The transmitter can be programmed for rising edge strobe or falling edge strobe through a dedicated pin. A rising edge transmitter will inter-operate with a falling edge receiver without any translation logic.

Transmitter Block Diagram



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Configuration Table

Table 13. Transmitter / DS90CF388 Receiver configuration table

Pin	Condition	Configuration
R_FB (Tx only)	R_FB = V_{CC}	Primary clock edge selected as Falling Edge
	R_FB = GND	Primary clock edge selected as Rising Edge
R_FDE (both Tx and Rx)	R_FDE = V_{CC}	Active data DE = High
	R_FDE = GND	Active data DE = Low
BAL (both Tx and Rx)	BAL=V_{CC}	DC Balanced enabled
	BAL=Gnd	DC Balanced disabled (backward compatible to FPD-Link)
DUAL (Tx only)	DUAL=V_{CC}	48-bit color (dual pixel) support
	DUAL=Gnd	24-bit color (single pixel) support

Pin Diagram

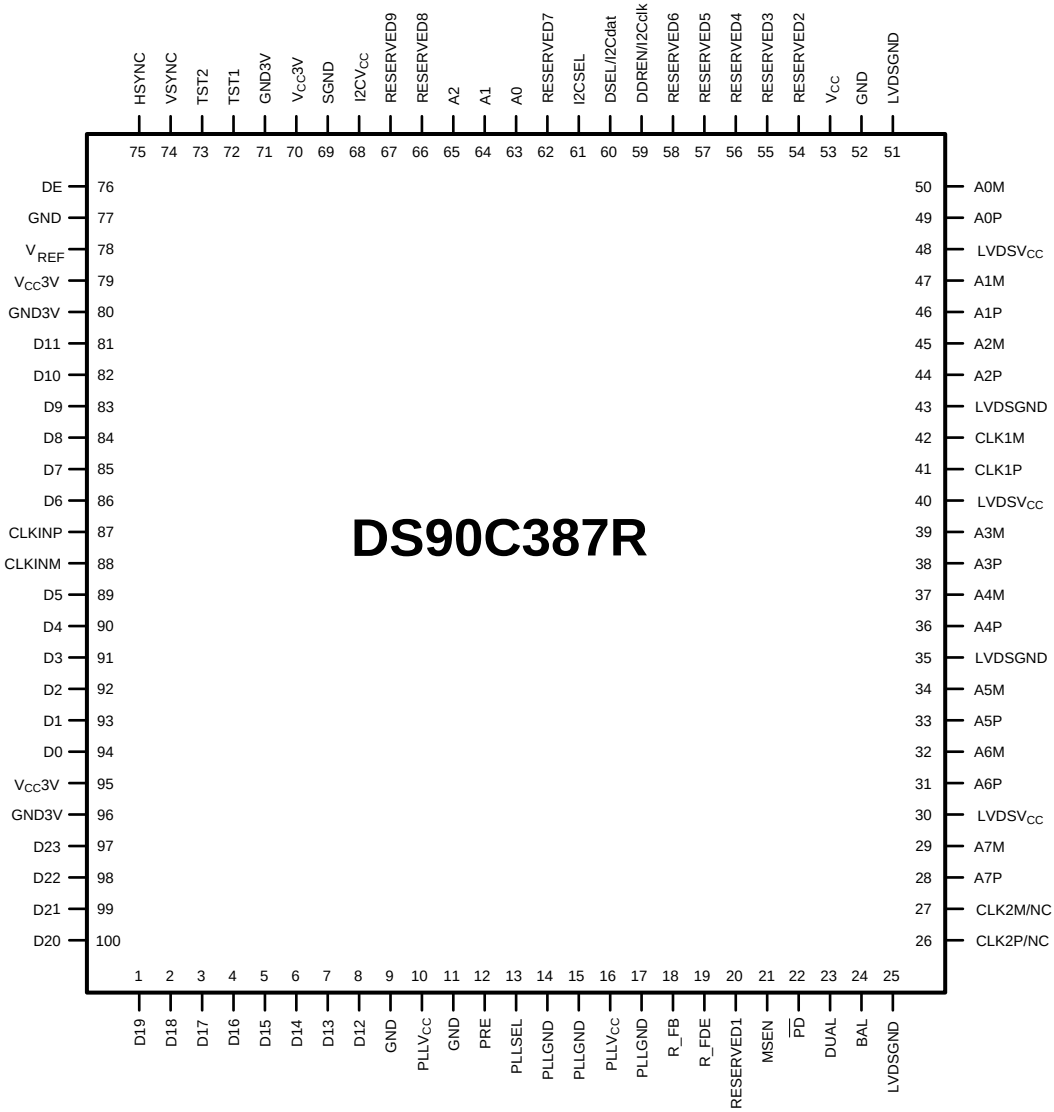

Figure 21. Transmitter-DS90C387R
See Package Number NEZ100A

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	25

Changes from Revision F (April 2013) to Revision G	Page
• Corrected the pin names in Figure 21	25

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90C387RVJD/NOPB	Active	Production	TQFP (NEZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-10 to 70	DS90C387RVJD >B
DS90C387RVJD/NOPB.B	Active	Production	TQFP (NEZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-10 to 70	DS90C387RVJD >B
DS90C387RVJDX/NOPB	Active	Production	TQFP (NEZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-10 to 70	DS90C387RVJD >B
DS90C387RVJDX/NOPB.B	Active	Production	TQFP (NEZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-10 to 70	DS90C387RVJD >B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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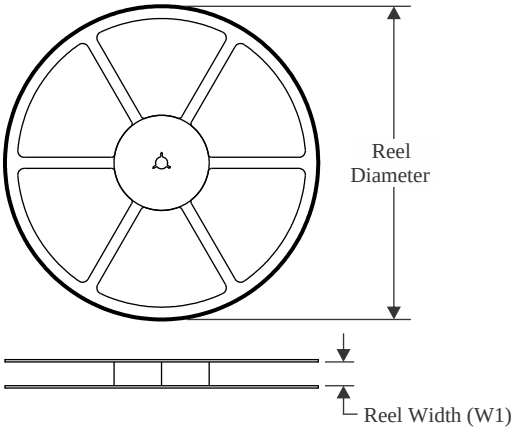
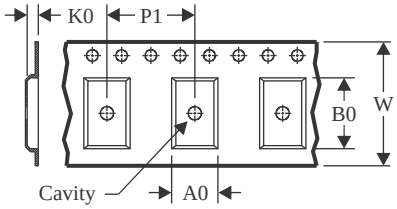
TAPE AND REEL INFORMATION

REEL DIMENSIONS

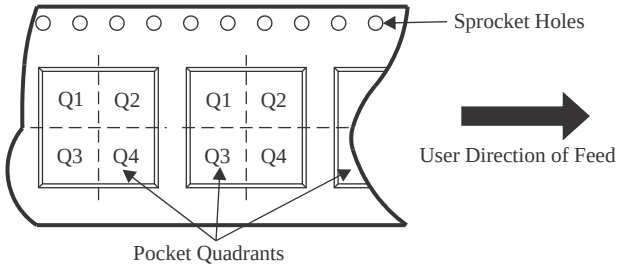


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

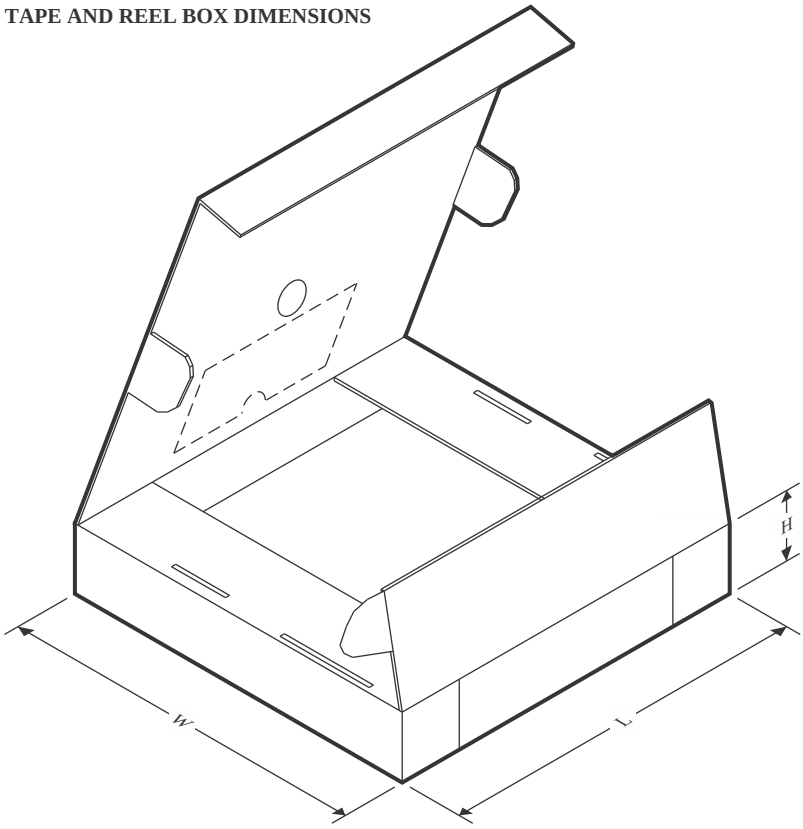
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90C387RVJDX/NOPB	TQFP	NEZ	100	1000	330.0	32.4	18.0	18.0	1.6	24.0	32.0	Q2

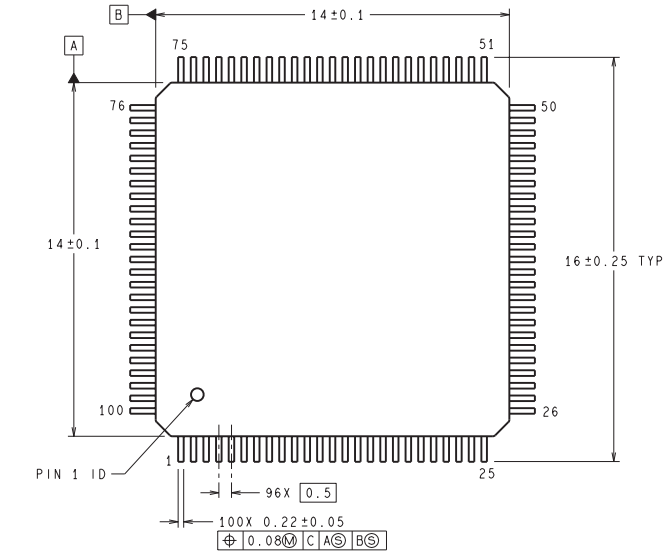
TAPE AND REEL BOX DIMENSIONS

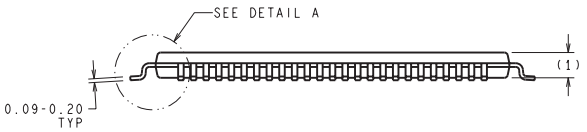


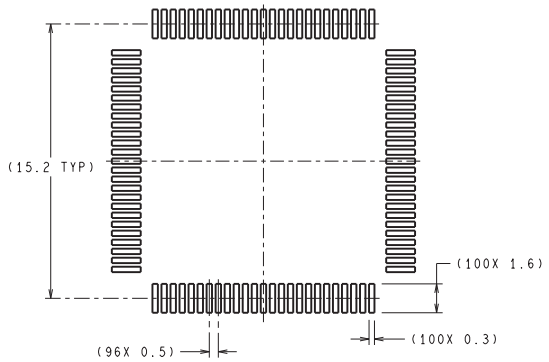
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90C387RVJDX/NOPB	TQFP	NEZ	100	1000	367.0	367.0	55.0

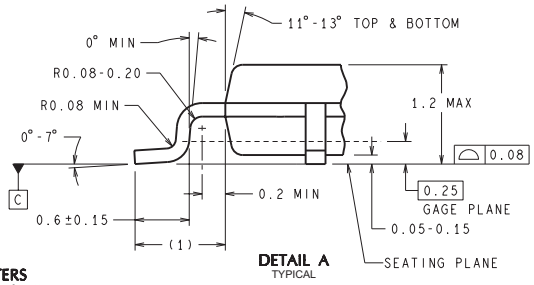
NEZ0100A







RECOMMENDED LAND PATTERN



DETAIL A
TYPICAL

DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN ( ) FOR REFERENCE ONLY

VJD100A (Rev C)

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