DRV8837C 1-A Low-Voltage H-Bridge Driver

1 Features

- H-Bridge Motor Driver
  - Drives a DC Motor or Other Loads
  - Low MOSFET On-Resistance: HS + LS 1 Ω
- 1-A Maximum Drive Current
- 0- to 11-V Operating Supply-Voltage Range
- Standard PWM Interface (IN1/IN2)
- Low-Power Sleep Mode With 120-nA Maximum Sleep Current
  - nSLEEP pin
- Small Package and Footprint
  - 8 WSON (With Thermal Pad)
  - 2.0 × 2.0 mm
- Protection Features
  - VCC Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)

2 Applications

- Cameras
- DSLR Lenses
- Consumer Products
- Toys
- Robotics
- Medical Devices

3 Description

The DRV8837C device provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device can drive one DC motor or other devices like solenoids. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding. An internal charge pump generates needed gate drive voltages.

The DRV8837C device can supply up to 1 A of output current. The device operates on a motor power supply voltage from 0 to 11 V, and control logic can operate on 1.8-V to 5-V rails.

The DRV8837C device has a PWM (IN/IN) input interface.

Internal shutdown functions are provided for overcurrent protection, short circuit protection, undervoltage lockout, and overtemperature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8837C	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

DRV8837C Simplified Diagram

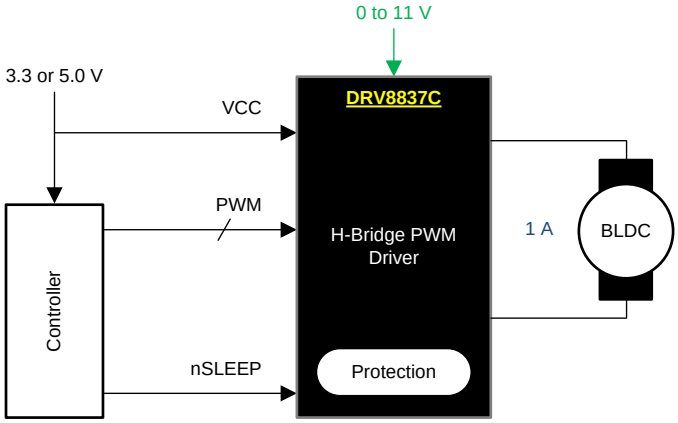

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Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Timing Requirements ... 6
6.7 Typical Characteristics ... 7
7 Detailed Description ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 Feature Description ... 9
7.4 Device Functional Modes ... 10
8 Application and Implementation ... 11
8.1 Application Information ... 11
8.2 Typical Application ... 11
9 Power Supply Recommendations ... 12
9.1 Bulk Capacitance ... 12
10 Layout ... 14
10.1 Layout Guidelines ... 14
10.2 Layout Example ... 14
10.3 Power Dissipation ... 14
11 Device and Documentation Support ... 15
11.1 Documentation Support ... 15
11.2 Receiving Notification of Documentation Updates ... 15
11.3 Community Resources ... 15
11.4 Trademarks ... 15
11.5 Electrostatic Discharge Caution ... 15
11.6 Glossary ... 15
12 Mechanical, Packaging, and Orderable Information ... 15

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2016) to Revision A	Page
• Changed the device status from *Product Preview* to *Production Data*	1

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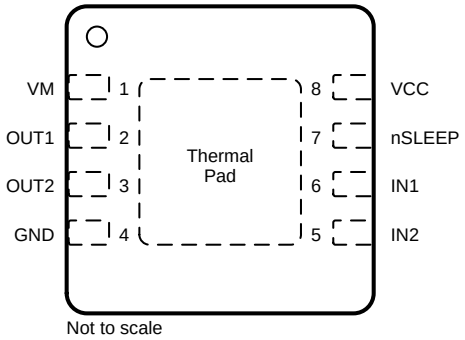
5 Pin Configuration and Functions

DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
POWER AND GROUND			
GND	4	PWR	Device ground This pin must be connected to the PCB ground.
VCC	8	PWR	Logic power supply Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor rated for VCC.
VM	1	PWR	Motor power supply Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor rated for VM.
CONTROL			
IN1	6	I	IN1 input
IN2	5	I	IN2 input
nSLEEP	7	I	Sleep mode input When this pin is in logic low, the device enters low-power sleep mode. The device operates normally when this pin is logic high. The pin has an internal pulldown resistor to GND.
OUTPUT			
OUT1	2	O	Motor output Connect this pin to the motor winding.
OUT2	3	O	

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)(2)]

		MIN	MAX	UNIT
Motor power-supply voltage	VM	–0.3	12	V
Logic power-supply voltage	V_{CC}	–0.3	7	V
Control pin voltage	IN1, IN2, nSLEEP	–0.5	7	V
Peak drive current	OUT1, OUT2	Internally limited		A
Operating virtual junction temperature, T_J		–40	150	ºC
Storage temperature, T_{stg}		–60	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Motor power-supply voltage	0	11	V
V_{CC}	Logic power-supply voltage	1.8	7	V
I_{OUT}	Motor peak current	0	1	A
f_{PWM}	Externally applied PWM frequency	0	250	kHz
V_{LOGIC}	Logic level input voltage	0	5.5	V
T_A	Operating ambient temperature	–40	85	°C

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC [(1)]		DRV8837C DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, V_{CC})						
V_{VM}	VM operating voltage		0		11	V
I_{VM}	VM operating supply current	V_{VM} = 5 V; V_{CC} = 3 V; No PWM		40	100	µA
		V_{VM} = 5 V; V_{CC} = 3 V; 50 kHz PWM		0.8	1.5	mA
I_{VMQ}	VM sleep mode supply current	V_{VM} = 5 V; V_{CC} = 3 V; nSLEEP = 0		30	95	nA
V_{CC}	V_{CC} operating voltage		1.8		7	V
I_{VCC}	V_{CC} operating supply current	V_{VM} = 5 V; V_{CC} = 3 V; No PWM		300	500	µA
		V_{VM} = 5 V; V_{CC} = 3 V; 50 kHz PWM		0.7	1.5	mA
I_{VCCQ}	V_{CC} sleep mode supply current	V_{VM} = 5 V; V_{CC} = 3 V; nSLEEP = 0		5	25	nA
CONTROL INPUTS (IN1/PH, IN2/EN, nSLEEP)						
V_{IL}	Input logic-low voltage				0.25 × V_{CC}	V
V_{IH}	Input logic-high voltage		0.5 × V_{CC}			V
V_{HYS}	Input logic hysteresis			0.08 × V_{CC}		V
I_{IL}	Input logic-low current	V_{INx} = 0 V	–5		5	µA
I_{IH}	Input logic-high current	V_{INx} = 3.3 V			50	µA
R_{PD}	Pulldown resistance			100		kΩ
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
$R_{DS(ON)}$	HS + LS FET on-resistance	V_{VM} = 5 V; V_{CC} = 3.3 V; I_O = 200 mA; T_J = 25°C		1000		mΩ
I_{OFF}	Off-state leakage current	V_{OUTx} = 0 V	–200		200	nA
PROTECTION CIRCUITS						
V_{UVLO}	V_{CC} undervoltage lockout	V_{CC} falling			1.7	V
		V_{CC} rising			1.8	V
I_{OCP}	Overcurrent protection trip level		1.2			A
t_{DEG}	Overcurrent deglitch time			1		µs
t_{RETRY}	Overcurrent retry time			1		ms
T_{TSD} (1)	Thermal shutdown temperature	Die temperature T_J	150	160	180	°C

(1) Not tested in production; limits are based on characterization data

6.6 Timing Requirements

T_A = 25°C, V_{VM} = 5 V, V_{CC} = 3 V, RL = 20 Ω

NO.				MIN	MAX	UNIT
1	t_7	Output enable time	See Figure 1.		300	ns
2	t_8	Output disable time			300	ns
3	t_9	Delay time, INx high to OUTx high			160	ns
4	t_{10}	Delay time, INx low to OUTx low			160	ns
5	t_{11}	Output rise time		20	188	ns
6	t_{12}	Output fall time		20	188	ns
—	t_{wake}	Wake time, nSLEEP rising edge to part active			30	µs

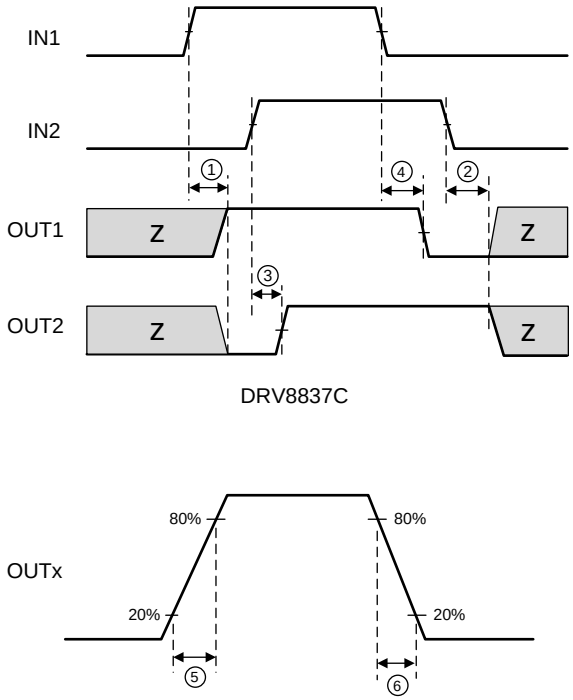

Figure 1. Input and Output Timing for DRV8837C

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6.7 Typical Characteristics

Plots generated using characterization data.

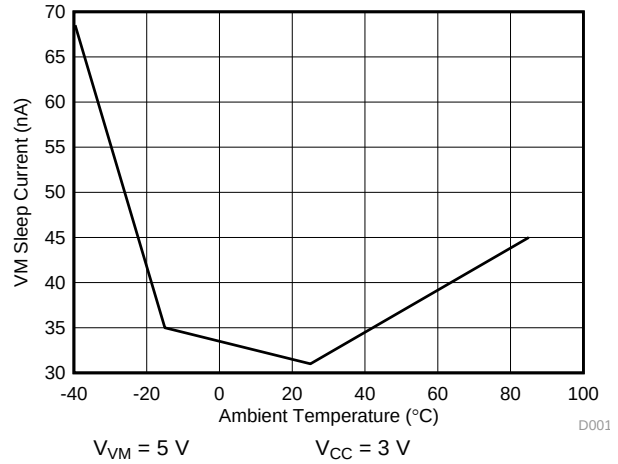


Figure 2. VM Sleep Current vs Ambient Temperature

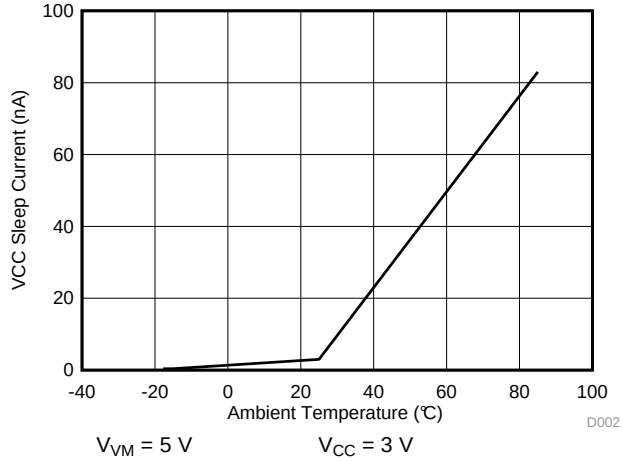


Figure 3. VCC Sleep Current vs Ambient Temperature

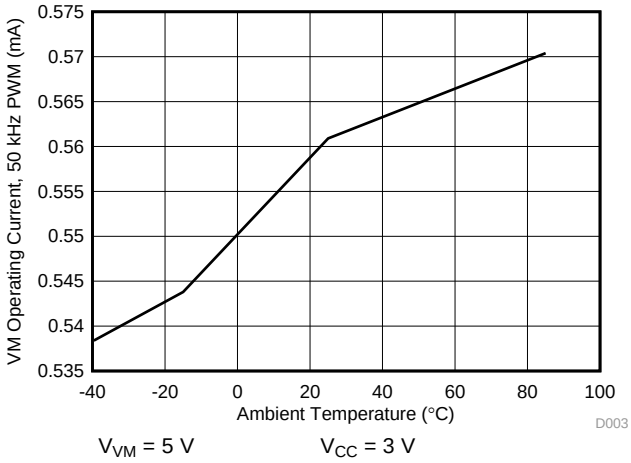


Figure 4. VM Operating Current vs Ambient Temperature

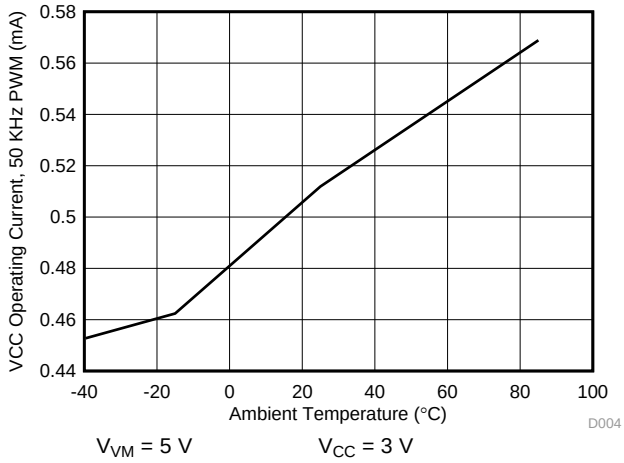


Figure 5. VCC Operating Current vs Ambient Temperature

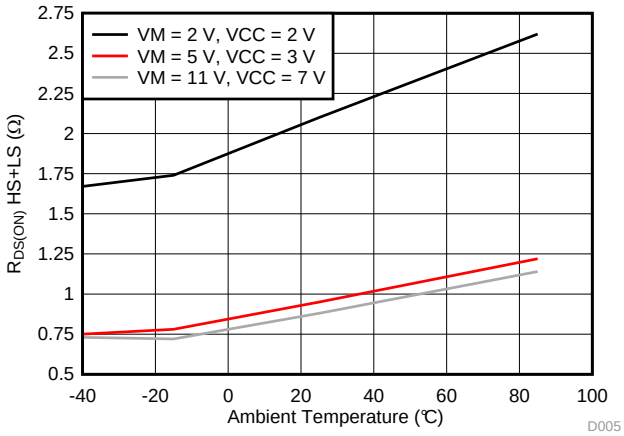


Figure 6. HS + LS $R_{DS(ON)}$ vs Ambient Temperature

7 Detailed Description

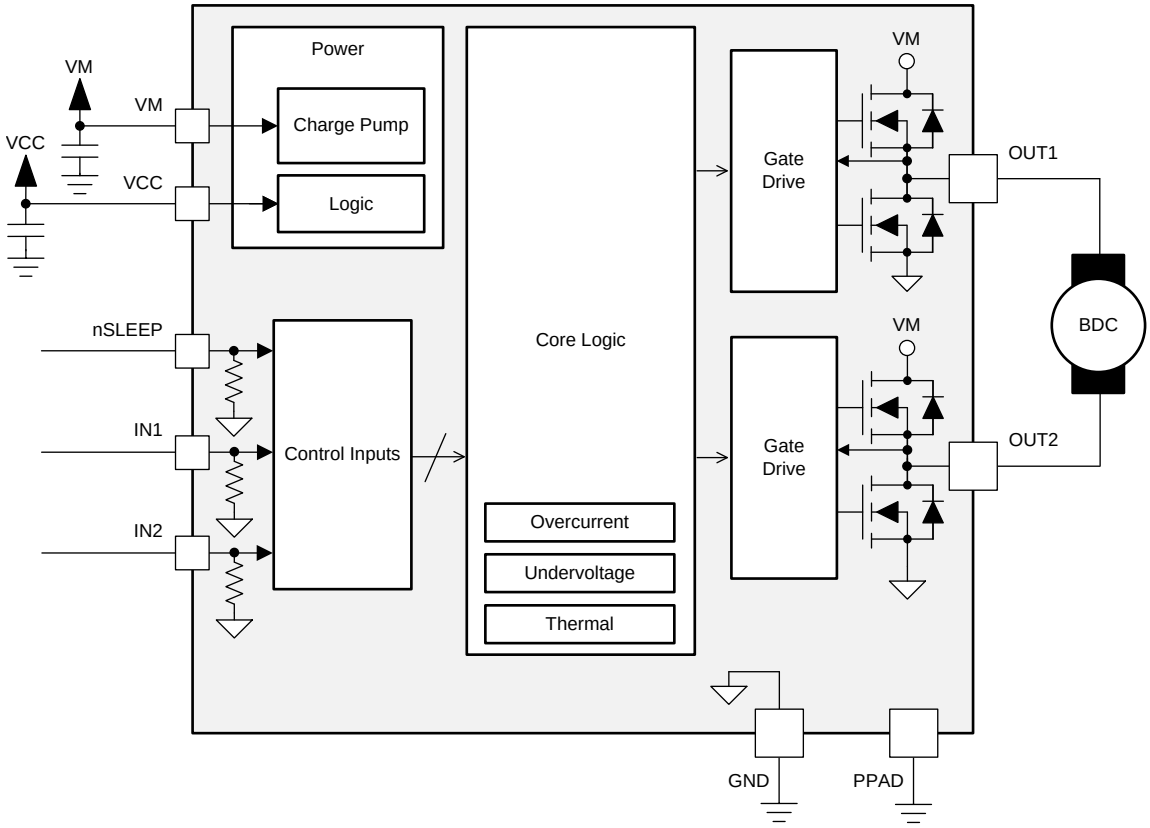
7.1 Overview

The DRV8837C device is an H-bridge driver that can drive one DC motor or other devices like solenoids. The outputs are controlled using a PWM interface (IN1/IN2).

A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

This device greatly reduces the component count of motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single device. In addition, the DRV8837C device adds protection features beyond traditional discrete implementations: undervoltage lockout, overcurrent protection, and thermal shutdown.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Bridge Control

The DRV8837C device is controlled using a PWM input interface, also called an IN/IN interface. Each output is controlled by a corresponding input pin.

Table 1 shows the logic for the DRV8837C device.

Table 1. DRV8837C Device Logic

nSLEEP	IN1	IN2	OUT1	OUT2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

7.3.2 Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the DRV8837C device enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

7.3.3 Power Supplies and Input Pins

The input pins can be driven within the recommended operating conditions with or without the VCC, VM, or both power supplies present. No leakage current path exists to the supply. Each input pin has a weak pulldown resistor (approximately 100 kΩ) to ground.

The VCC and VM supplies can be applied and removed in any order. When the VCC supply is removed, the device enters a low-power state and draws very little current from the VM supply. The VCC and VM pins can be connected together if the supply voltage is between 1.8 and 7 V.

The VM voltage supply does not have any undervoltage-lockout protection (UVLO). As long as V_{CC} > 1.8 V, the internal device logic remains active which means that the VM pin voltage can drop to 0 V, however, the load may not be sufficiently driven at low VM voltages.

7.3.4 Protection Circuits

The DRV8837C is fully protected against VCC undervoltage, overcurrent, and overtemperature events.

VCC undervoltage lockout If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when the VCC pin voltage rises above the UVLO threshold.

Overcurrent protection (OCP) An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{DEG}, all FETs in the H-bridge are disabled. Operation resumes automatically after t_{RETRY} has elapsed. Overcurrent conditions are detected on both the high-side and low-side devices. A short to the VM pin, GND, or from the OUT1 pin to theOUT2 pin results in an overcurrent condition.

Thermal shutdown (TSD) If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, operation automatically resumes.

Table 2. Fault Behavior

FAULT	CONDITION	H-BRIDGE	RECOVERY
VCC undervoltage (UVLO)	VCC < 1.7 V	Disabled	VCC > 1.8 V
Overcurrent (OCP)	I_{OUT} > 1.2 A (MIN)	Disabled (retries automatically)	t_{RETRY} elapses
Thermal Shutdown (TSD)	T_J > 150°C (MIN)	Disabled (retries automatically)	T_J < 150°C

7.4 Device Functional Modes

The DRV8837C device is active unless the nSLEEP pin is brought logic low. In sleep mode the H-bridge FETs are disabled Hi-Z. The DRV8837C device is brought out of sleep mode automatically if nSLEEP is brought logic high.

The H-bridge outputs are disabled during undervoltage lockout, overcurrent, and overtemperature fault conditions.

Table 3. Operation Modes

MODE	CONDITION	H-BRIDGE
Operating	nSLEEP pin = 1	Operating
Sleep mode	nSLEEP pin = 0	Disabled
Fault encountered	Any fault condition met	Disabled (retries automatically)

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8837C device is device is used to drive one DC motor or other devices like solenoids. The following design procedure can be used to configure the DRV8837C device.

8.2 Typical Application

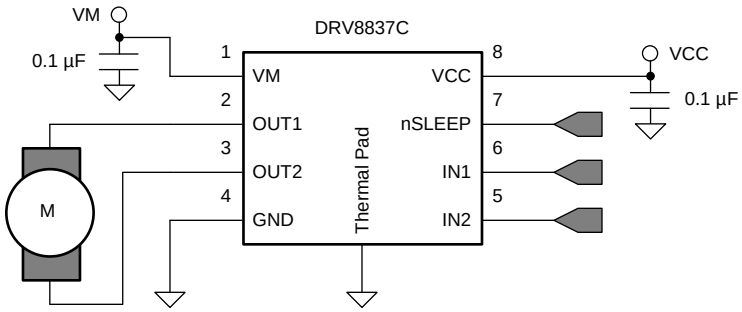

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Figure 7. Schematic of DRV8837C Application

8.2.1 Design Requirements

Table 4 lists the required parameters for a typical usage case.

Table 4. System Design Requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	VM	9 V
Logic supply voltage	VCC	3.3 V
Target RMS current	I_{OUT}	0.8 A

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed dc motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Low-Power Operation

When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power.

8.2.3 Application Curves

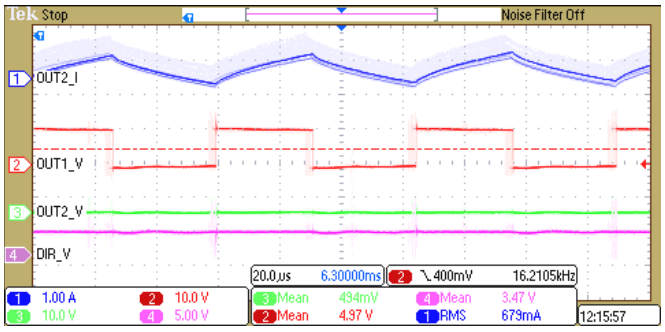

Figure 8. 50% Duty Cycle, Forward Direction

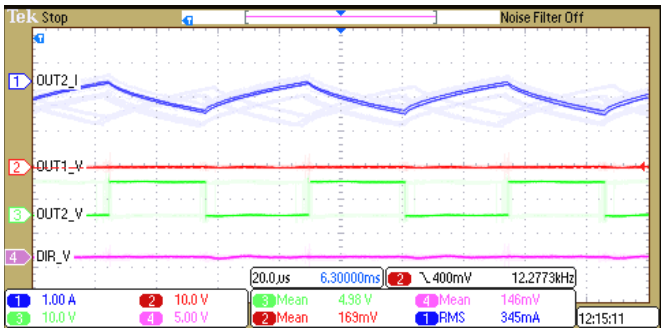

Figure 9. 50% Duty Cycle, Reverse Direction

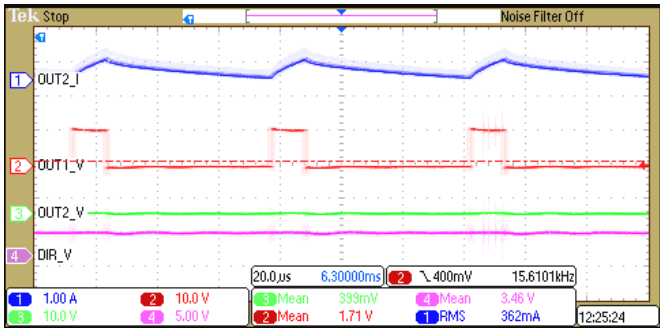

Figure 10. 20% Duty Cycle, Forward Direction

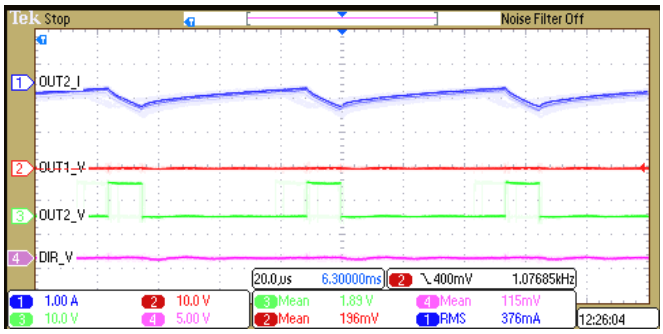

Figure 11. 20% Duty Cycle, Reverse Direction

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power-supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.

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Bulk Capacitance (continued)

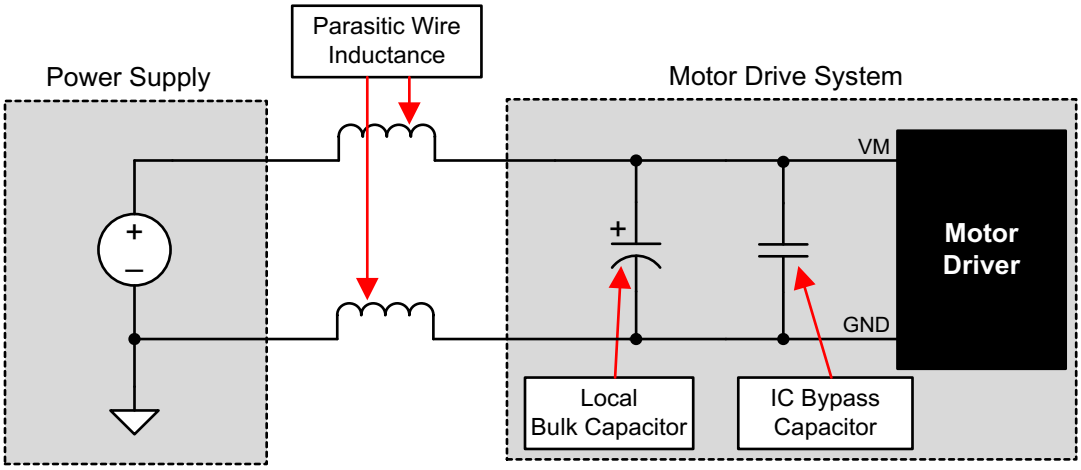

Figure 12. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply

10 Layout

10.1 Layout Guidelines

The VM and VCC pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 µF rated for the VM and VCC supplies. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin. In addition bulk capacitance is required on the VM pin.

10.2 Layout Example

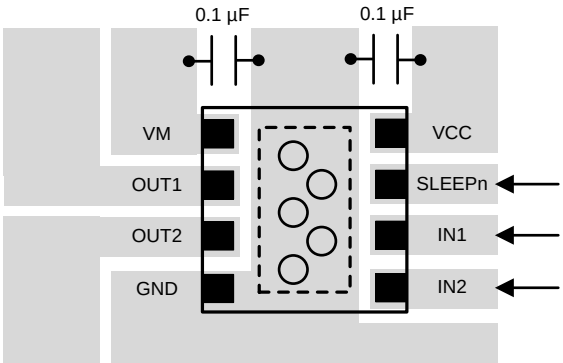

Figure 13. Simplified Layout Example

10.3 Power Dissipation

Power dissipation in the DRV8837C device is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Use Equation 1 to estimate the average power dissipation when running a brushed-DC motor.

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2$$

where

- P_{TOT} is the total power dissipation
- $R_{DS(ON)}$ is the resistance of the HS plus LS FETs
- $I_{OUT(RMS)}$ is the RMS or DC output current being supplied to the load (1)

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

NOTE

The value of $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

The DRV8837C device has thermal shutdown protection. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Calculating Motor Driver Power Dissipation* (SLVA504)
- *DRV8837C Evaluation Module User's Guide* (SLVUAS3)
- *Understanding Motor Driver Current Ratings* (SLVA505)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8837CDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837C
DRV8837CDSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837C
DRV8837CDSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837C
DRV8837CDSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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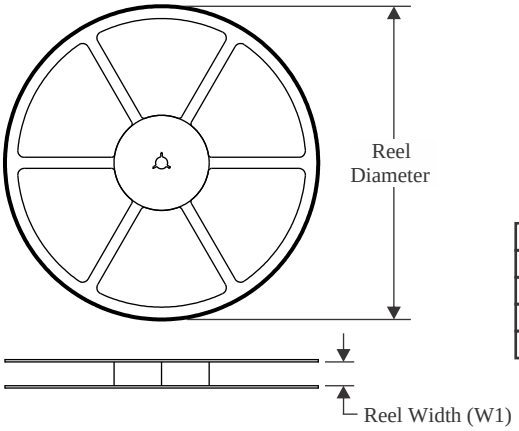
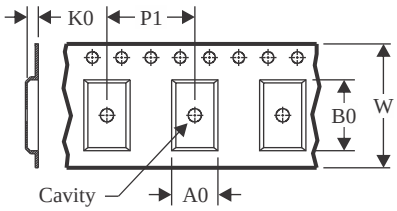
TAPE AND REEL INFORMATION

REEL DIMENSIONS

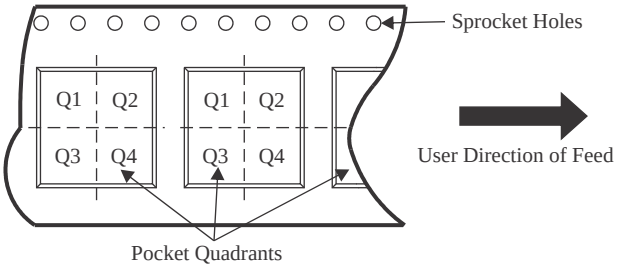


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

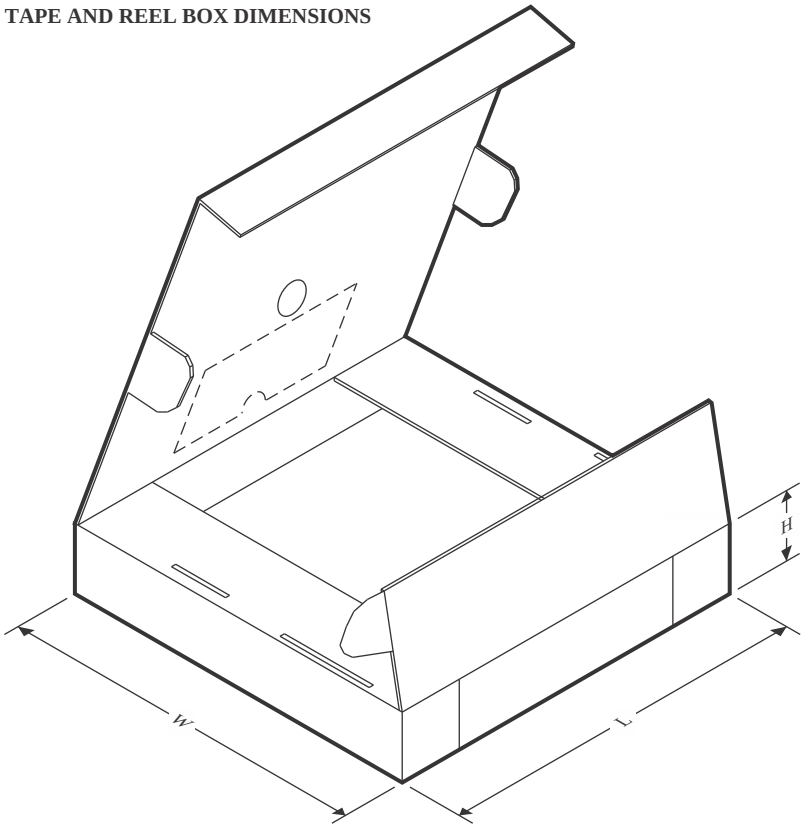
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8837CDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8837CDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8837CDSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8837CDSGR	WSON	DSG	8	3000	182.0	182.0	20.0
DRV8837CDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
DRV8837CDSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

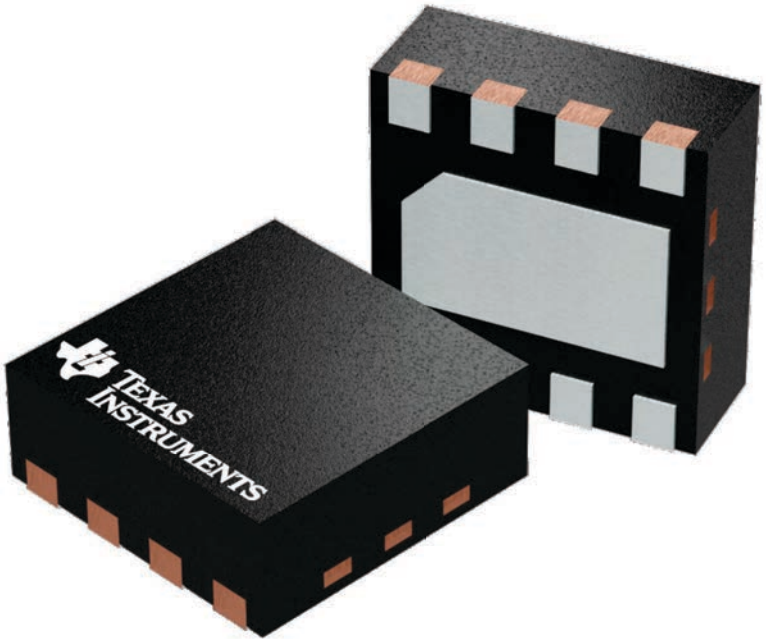
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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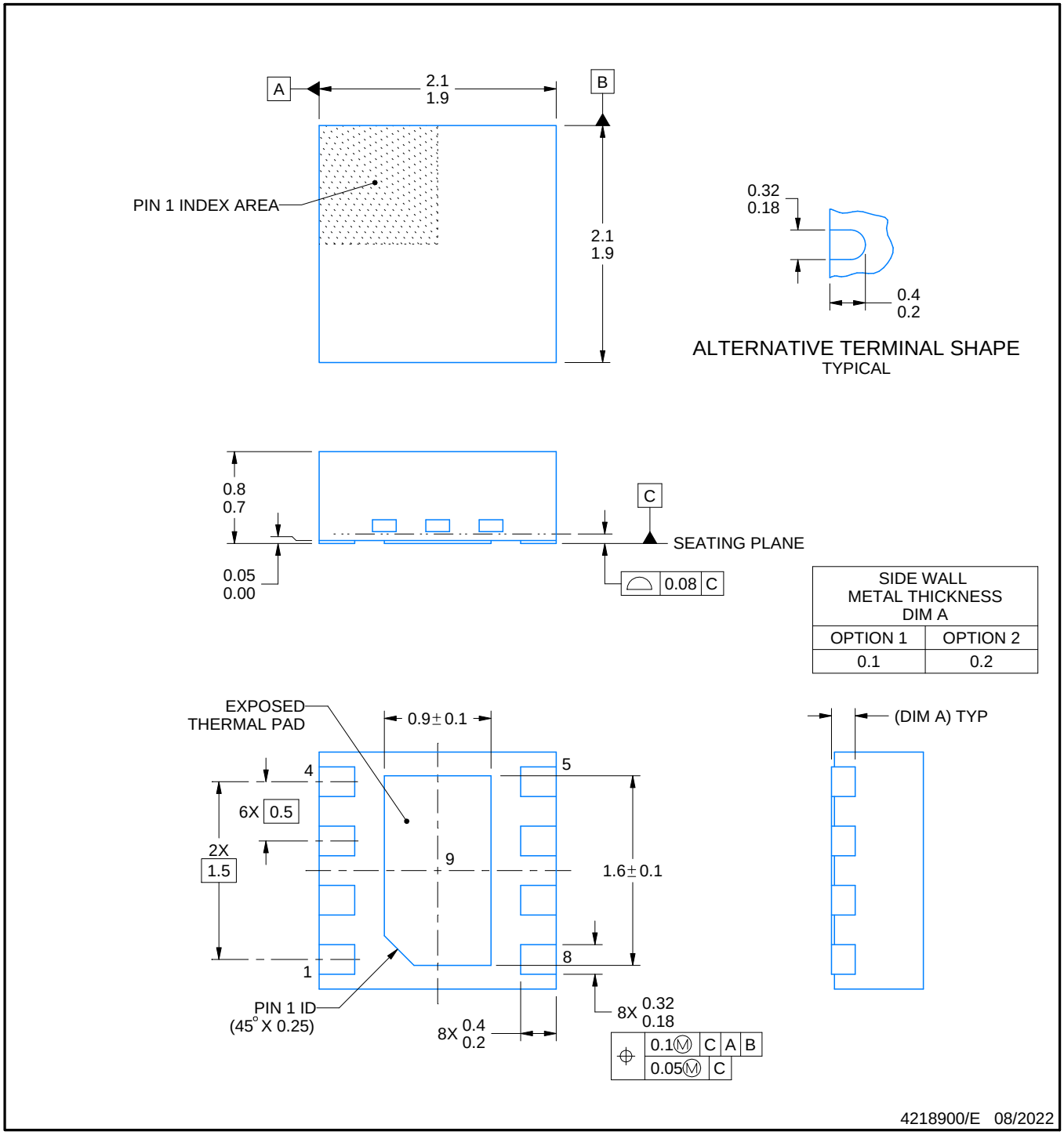
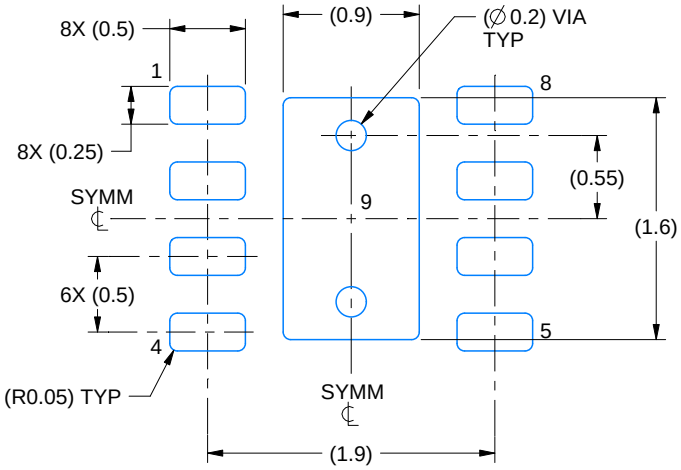
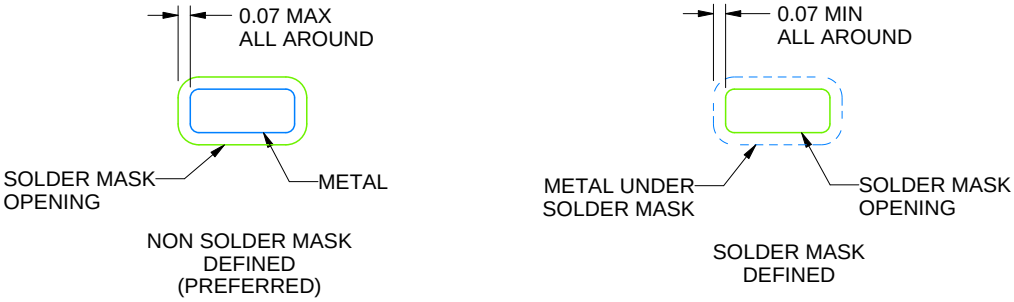


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

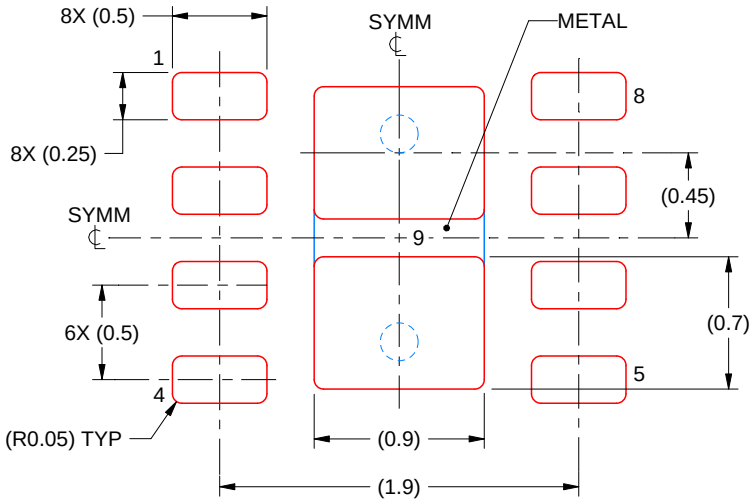


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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