DRV7167A 100-V, 60A Half-Bridge GaN Motor Driver Power Stage

1 Features

- 100V, Half-bridge GaN Motor Driver power stage with integrated driver supporting 48V systems
- Low GaN on-state resistance
  - 2.2 mΩ $R_{DS(ON)}$ (per FET) at T_A=25°C
- Enables efficient and high density power conversion
  - High output current capability: 60A_{rms}
  - Supports upto 500 kHz PWM switching frequency
  - Ultra-low propagation delay (20ns typical) and matching (2ns typical)
  - Configurable slew rate of GaN FETs
  - Zero-voltage detection (ZVD) reporting for dead-time optimization.
  - Independent input mode (IIM) control
  - Single PWM input with resistor programmable dead-time option for IO-limited controllers
- 5V external bias power supply
  - Supports 3.3V and 5V input logic levels
- Robust protection
  - Interlock protection in Independent Input Mode (IIM)
  - Internal bootstrap supply voltage regulation to prevent GaN FET Overdrive
  - V_{DS} monitoring based cycle-by-cyle short-circuit protection
  - Fault indication for over-temperature, supply under-voltage and short-circuit events
- Parasitic optimized QFN package with exposed top pad to support top-side cooling.

2 Applications

- Humanoid Robots
- Collaborative robots
- Mobile Robots (AGV/AMR)
- 48V Servo Drives
- Drones
- E-bikes, E-Scooters, E-Mobility
- Power tools

3 Description

The DRV7167A device is a family of 100V half-bridge power stages, with integrated gate-driver and enhancement-mode gallium nitride (GaN) FETs. The devices consist of a high-frequency GaN FET driver in a half-bridge configuration, that drives two 100V GaN FETs.

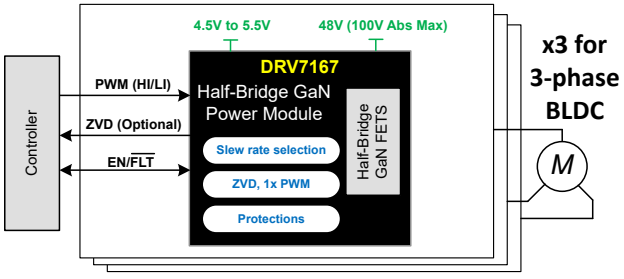
GaN FETs provide significant advantages for power conversion as GaN FETs have zero reverse recovery and very small input capacitance (C_{ISS}) and output capacitance (C_{OSS}). All the devices are mounted on a completely bond-wire free package platform with minimized package parasitic elements, which can be easily mounted on PCBs.

The TTL logic compatible inputs support 3.3V and 5V logic levels, regardless of the GVDD voltage. A proprietary bootstrap voltage control technique regulates the gate voltages of the enhancement mode GaN FETs within the safe operating range. The device extends advantages of discrete GaN FETs by offering a more user-friendly interface. The device is an excellent option for applications requiring high-frequency, high-efficiency operation in a small form factor.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (3)(NOM)
DRV7167A(2)	VBN (VQFN, 18)	7.00mm × 4.50mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Advance information. The products are in sampling and preproduction phase.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



DRV7167 Simplified Schematic

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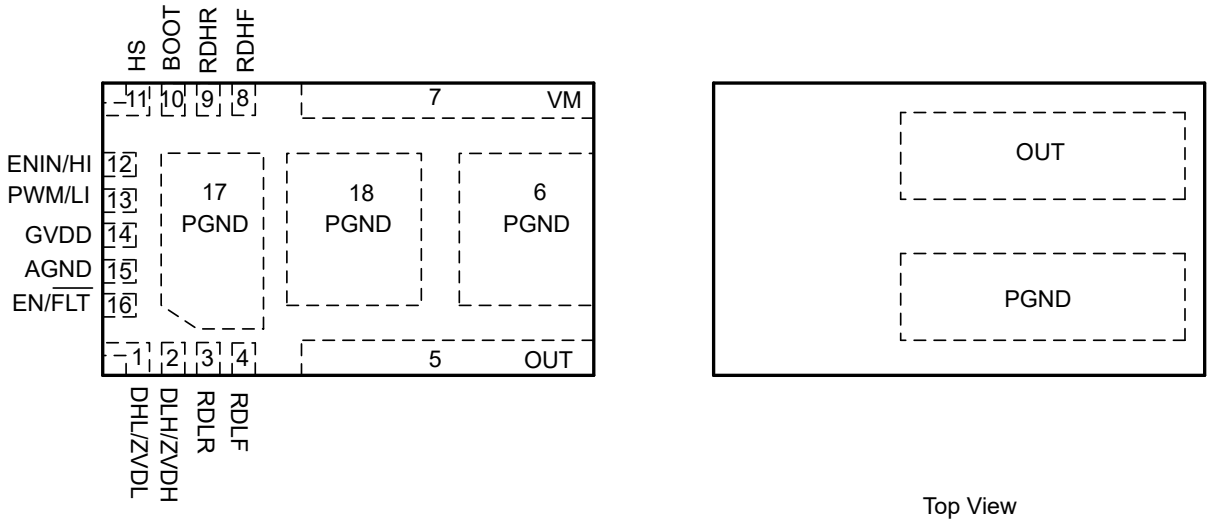
4 Pin Configuration and Functions



Transparent Top View
(Shows Pin Locations)

Top View
(Shows Exposed GaN dies
for heatsink connection)

Figure 4-1. VBN Package, 18-Pin VQFN (Top View)

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Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
DHL/ZVDL	1	IO	In PWM mode, sets the dead time for high-to-low transition by connecting a resistor to AGND. In IIM mode, zero-voltage detection output signal to indicate if low-side FET achieves zero-voltage switching in current switching cycle. Note: Do not Tie ZVDL to GVDD.
DLH/ZVDH	2	IO	In PWM mode, sets the dead time for low-to-high transition by connecting a resistor to AGND. In IIM mode, zero-voltage detection output signal to indicate if high-side FET achieves zero-voltage switching in current switching cycle.
RDLR	3	I	Sets the slew-rate control for LS FET turn-on through resistor to AGND.
RDLF	4	I	Sets the slew-rate control for LS FET turn-off through resistor to AGND. Float this pin to enable PWM mode.
OUT	5	P	Switching node. Internally connected to HS pin.
PGND	6, 17, 18	G	Power ground. Low-side GaN FET source. Internally connected to low-side GaN FET source.
VM	7	P	Input voltage pin. Internally connected to high-side GaN FET drain.
RDHF	8	I	Sets the slew-rate control for HS FET turn-off through resistor to HS.
RDHR	9	I	Sets the slew-rate control for HS FET turn-on through resistor to HS. Note: Do not float RDHR pin.
BOOT	10	P	High-side gate driver bootstrap rail. Connect bypass capacitor to HS.
HS	11	P	High-side GaN FET source connection.
ENIN/HI	12	I	In PWM mode, enables gate-drive for both high-side and low-side FETs. In IIM mode, high-side gate driver control input.
PWM/LI	13	I	In PWM mode, PWM input. In IIM mode, low-side gate driver control input.
GVDD	14	P	5V device power supply.
AGND	15	G	Analog ground. Internally connected to low-side GaN FET source.
EN/$\overline{\text{FLT}}$	16	IO	Chip enable and Fault output pin. Connect to microcontoller output or to GVDD through 4.7 kΩ resistor.

(1) I = Input, O = Output, IO = Input/Output, G = Ground, P = Power

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5 Specifications

5.1 Absolute Maximum Ratings

See(1)

PARAMETER	MIN	MAX	UNIT
VM to PGND (2)	0	100	V
VM to PGND (T_J = 125°C, Repetitive Transient) (2) (3)		120	V
BOOT to AGND (2)		106	V
HS to AGND (2)		100	V
HS to PGND(T_J = 125°C, Repetitive Transient)(2) (3)		120	V
HI to AGND	-0.3	6	V
LI to AGND	-0.3	6	V
HI to AGND, 20ns transients, < 1Mhz frequency	-2	6	V
LI to AGND, 20ns transients, < 1Mhz frequency	-2	6	V
GVDD to AGND	-0.3	6	V
BOOT to GVDD (2)	0	100	V
BOOT to HS	-0.3	6	V
OUT to PGND (2)		100	V
IOUT from OUT pin (Continuous), T_J = 125℃		60	A
Junction Temperature, T_J	-40	150	°C
Storage Temperature, T_{stg}	-40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) This is a DC voltage rating applicable only under non switching conditions.
(3) Pulsed repetitively with duty cycle ≤ 1%.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001(1)	±1000	V
$V_{(ESD)}$	Electrostatic Discharge	Charged-device model (CDM), per ANSI/ESDA/ JEDEC JS-002(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

Unless otherwise noted, voltages are with respect to AGND

		MIN	NOM	MAX	UNIT
VM to PGND(1)				80	V
GVDD to AGND		4.5	5	5.5	V
GVDD to AGND, 20ns transients, < 1MHz frequency				5.8	V
PWM/LI, ENIN/HI, EN/$\overline{FLT}$ Low Level Input		0		1.2	V
PWM/LI, ENIN/HI, EN/$\overline{FLT}$ High Level Input	PWM/LI, ENIN/HI, EN/$\overline{FLT}$ High Level Input	2.1		GVDD	V
BOOT to HS	BOOT to HS	V_{HS}+ 4.5		V_{HS}+ 5.5	V
f_{MAX}				500	kHz
t_{PW}	Minimum input pulse width supported	10			ns
Dead time control resistor	RDLH, RDLH	0		100	kΩ
Slew rate control resistor	RDHR, RDHF, RDLR, RDLF	4		32	kΩ
IOUT from OUT pin (Continuous), T_J = 125°C				60 (2)	A
HS, OUT Slew rate (3)	HS, OUT Slew rate (3)			50	V/ns
Junction Temperature, T_J	Junction Temperature, T_J			150	°C

(1) During soft-switching operation the recommended operating input voltage is 80V. During hard-switching operation the recommended input voltage is 60V.
(2) Output current in end application depends on thermal design.
(3) Determined through design and characterization. Not tested in production.

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5.4 Thermal Information_DRV7167A

THERMAL METRIC (1)		DRV7167 QFN 18 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)	26.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JC(Bot)}$	Junction-to-case (bottom) thermal resistance, low-side FET to PGND	3.5	°C/W
	Junction-to-case (bottom) thermal resistance, high-side FET to VM	6.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

GVDD = 5V, C_{GVDD} = 1uF + 220nF, $C_{BOOT-HS}$ = 200nF, EN/$\overline{FLT}$ is pulled up to GVDD with 4.7KΩ resistor, voltages are with respect to AGND and typical specifications are at 25°C (1); –40°C ≤ T_J≤125°C, (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER STAGE_DRV7167A						
$R_{DS(ON)HS}$	High-side GaN FET on-resistance	LI=0V, HI=GVDD=5V, BOOT-HS=5V, $I_{(VM-OUT)}$=16A, T_J = 25°C		2.2	3.1	mΩ
$R_{DS(ON)LS}$	Low-side GaN FET on-resistance	LI=GVDD=5V, HI=0V, BOOT-HS=5V, $I_{(OUT-PGND)}$=16A, T_J = 25°C		2.1	3	mΩ
V_{SD}	GaN source to drain 3rd quadrant conduction drop	I_{SD} = 500 mA, V_M floating, V_{GVDD} = 5 V, HI = LI = 0V		1.2		V
$I_{L-VM-OUT}$	Leakage from VM to OUT when the high-side GaN FET and low-side GaN FET are off	VM = 80V, OUT=0V, HI = LI = 0V, V_{GVDD} = 5V, T_J=25°C		8	300	µA
$I_{L-OUT-GND}$	Leakage from OUT to GND when the high-side GaN FET and low-side GaN FET are off	OUT = 80V, HI = LI = 0V, V_{GVDD} = 5V, T_J=25°C		37	300	µA
C_{ISS}	Input capacitance of high side or low side GaN FET	V_{DS} = 50V, V_{GS} = 0V, T_J = 25°C		1800		pF
C_{OSS}	Output capacitance of high-side or low-side GaN FET			400		pF
$C_{OSS(ER)}$	Energy related output capacitance of high-side or low-side GaN FET			496		pF
$C_{OSS(TR)}$	Time related output capacitance of high-side GaN FET or low-side GaN FET			618		pF
C_{RSS}	Reverse transfer capacitance of high-side or low-side GaN FET			26		pF
Q_G	Total gate charge of high-side or low-side GaN FET	V_{DS}=50V, I_D= 16A, V_{GS} = 5V, T_J=25°C		18		nC
Q_{OSS}	Output charge of high-side or low-side GaN FET	V_{DS}=50V, V_{GS}= 0V, T_J=25°C		30		nC
Q_{RR}	Source to Drain Reverse Recovery Charge of high-side or low-side GaN FET			0		nC
E_{ON_LS}	Turn-ON switching energy of low-side GaN FET	LI = 0 to 5V, V_{SW} = 48V to 0V, RDLR = 2k, I_D= 20A		2.8		µJ
E_{OFF_LS}	Turn-OFF switching energy of low-side GaN FET	LI = 5 to 0V, V_{SW} = 0V to 48V, RDLF = 2k, I_D= 20A		0.78		µJ
E_{ON_HS}	Turn-ON switching energy of high-side GaN FET	HI = 0 to 5V, V_{SW} = 0V to 48V, RDHR = 2k, I_D= 20A		2.8		µJ
E_{OFF_HS}	Turn-OFF switching energy of high-side GaN FET	HI = 5 to 0V, V_{SW} = 48V to 0V, RDHF = 2k, I_D= 20A		0.78		µJ
t_{HIPLH} (2) (3)	Propagation delay: HI Rising	LI = 0V, GVDD = 5V, BOOT-HS = 5V, VM = 48V		20	36	ns

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GVDD = 5V, C_{GVDD} = 1uF + 220nF, $C_{BOOT-HS}$ = 200nF, EN/$\overline{FLT}$ is pulled up to GVDD with 4.7KΩ resistor, voltages are with respect to AGND and typical specifications are at 25℃ (1); –40℃ ≤ T_J≤125℃, (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{HIPHL} (2) (3)	Propagation delay: HI Falling	LI = 0V, GVDD = 5V, BOOT-HS = 5V, VM = 48V		20	35	ns
t_{LIPLH} (2) (3)	Propagation delay: LI Rising	HI = 0V, GVDD = 5V, BOOT-HS = 5V, VM = 48V		20	32	ns
t_{LIPHL} (2) (3)	Propagation delay: LI Falling	HI = 0V, GVDD = 5V, BOOT-HS = 5V, VM = 48V		20	32	ns
t_{MON} (2) (3)	Delay Matching: LI high & HI low			1	5	ns
t_{MOFF} (2) (3)	Delay Matching: LI low & HI high			1	5	ns
$t_{MHIR(P-P)}$ (2) (3)	Part to part Delay Matching: HI rising	LI = 0V, GVDD = 5V, BOOT-HS = 5V, VM = 48V		7	14	ns
$t_{MHIF(P-P)}$ (2) (3)	Part to part Delay Matching: HI falling	LI = 0V, GVDD = 5V, BOOT-HS = 5V, VM = 48V		7	14	ns
$t_{MLIR(P-P)}$ (2) (3)	Part to part Delay Matching: LI rising	HI = 0V, GVDD = 5V, BOOT-HS = 5V, VM = 48V		9	14	ns
$t_{MLIF(P-P)}$ (2) (3)	Part to part Delay Matching: LI falling	HI = 0V, GVDD = 5V, BOOT-HS = 5V, VM = 48V		9	14	ns
t_{PW}	Minimum Input Pulse Width that Changes the Output			8		ns
INPUT PINS (ENIN/HI, PWM/LI, EN)						
V_{IH}	High-Level Input Voltage Threshold	Rising Edge			2.1	V
V_{IL}	Low-Level Input Voltage Threshold	Falling Edge	1.2			V
V_{HYS}	Hysteresis between rising and falling threshold			300		mV
R_I	Input pull down resistance		200	300	500	kΩ
OUTPUT PINS (ZVDx)						
V_{OL}	Low level output voltage	I_{OL} = 3 mA			0.25	V
V_{OH}	High level output voltage	I_{OL} = -1.5 mA to 0 mA	2.6		3.5	V
UNDER/OVER VOLTAGE PROTECTION						
V_{GVDDR}	V_{GVDD} UVLO Rising edge threshold	Rising	3.3	3.7	4.0	V
V_{GVDDF}	V_{GVDD} UVLO Falling edge threshold		3.1	3.5	3.8	V
$V_{GVDD(hyst)}$	V_{GVDD} UVLO threshold hysteresis			200		mV
$V_{GVDD(Deglitch)}$	V_{GVDD} UVLO glitch immunity			1		µs
V_{BOOTR}	BOOT UVLO Rising edge threshold	Rising	3.3	3.7	4.0	V
V_{BOOTF}	BOOT UVLO Falling edge threshold		3.1	3.5	3.8	V
$V_{BOOT(hyst)}$	BOOT UVLO threshold hysteresis			200		mV
$V_{BOOT(Deglitch)}$	BOOT UVLO glitch immunity			1		µs
$t_{start-up}$	Time from VGVDD> V_{GVDDR} to device ready for PWM input				180	µs
SYNCRONOUS BOOTSTRAP						
V_{DH}	Forward voltage drop	$I_{VDD-BOOT}$ = 5mA		25		mV
		$I_{VDD-BOOT}$ = 50mA		250		mV
t_{SS}	BOOT power up time (With LI=High)	C_{BOOT} = 220 nF		2.2		µs
t_{SS}	BOOT power up time (With LI=High)	C_{BOOT} = 1 µF		12		µs
Q_{RR}	Bootstrap reverse recovery charge	VM = 50 V		0		nC
V_{BOOTth_U}	Rising threshold when boot cap charging is stopped.	VM = 5V, LI = 5V	4.8	5	5.2	V
V_{BOOTth_L}	Falling threshold when boot cap charging is started again	VM = 5V, LI = 5V	4.6	4.8	5	V
SUPPLY CURRENTS						
I_{GVDD}	GVDD Quiescent Current	LI = HI = 0V, GVDD = 5V, EN=0		0.4		mA
I_{GVDD}	GVDD Quiescent Current	LI = HI = 0V, GVDD = 5V		1	1.5	mA

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GVDD = 5V, C_{GVDD} = 1uF + 220nF, $C_{BOOT-HS}$ = 200nF, EN/$\overline{FLT}$ is pulled up to GVDD with 4.7KΩ resistor, voltages are with respect to AGND and typical specifications are at 25℃ (1); –40℃ ≤ T_J≤125℃, (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{GVDD}	GVDD Quiescent Current	LI=GVDD=5V, HI=0V		1.8	4.5	mA
I_{GVDDO}	Total GVDD Operating Current	f = 500 kHz, 50% Duty cycle, V_M = 48V		18	24	mA
I_{BOOT}	BOOT Quiescent Current	LI = HI = 0V, GVDD = 5V, BOOT-HS = 5V		0.5	1	mA
I_{BOOT}	BOOT Quiescent Current	LI=0V, HI=GVDD=5V, BOOT-HS=5V, VM=48V		1.8	4.5	mA
I_{BOOTO}	BOOT Operating Current	f = 500 kHz, 50% Duty cycle, GVDD = 5V, BOOT-HS = 5V, V_M = 48V		12	15	mA
SLEW RATE CONTROL (EFFECTIVE GATE RESISTANCE)						
Rgfh	RDHF = 0 Ω	Voltage across driver FET = 1.2V		0.3		Ω
	RDHF = 4 kΩ			1.3		
	RDHF = 8 kΩ			2.6		
	RDHF =16 kΩ			5.3		
Rgfl	RDLF = 0 Ω	Voltage across driver FET = 1.2V		0.3		Ω
	RDLF = 4 kΩ			1.3		
	RDLF = 8 kΩ			2.6		
	RDLF =16 kΩ			5.3		
Rgrh	RDHR = 0 Ω	Voltage across driver FET = 1.2V		0.8		Ω
	RDHR = 4 kΩ			3.6		
	RDHR = 8 kΩ			7		
	RDHR =16 kΩ			14		
Rgrl	RDLR = 0 Ω	Voltage across driver FET = 1.2V		0.8		Ω
	RDLR = 4 kΩ			3.6		
	RDLR = 8 kΩ			7		
	RDLR =16 kΩ			14		
DEAD TIME CONTROL						
t_{DEAD_MIN}	Minimum Dead Time	DLH, DHL = 0Ω; Minimum Slew rate setting.	5	7.5	10	ns
t_{DEAD_MAX}	Maximum Dead Time	DLH, DHL = 100kΩ; Maximum Slew rate setting.	32	40	48	ns
OCP						
V_{DSAT}	Saturation protection voltage threshold			0.75		V
t_{BLANK}	Blanking time for V_{DSAT} detection		38	60	88	ns
t_{SATFLT}	Time to indicate FLT upon V_{DS} overvoltage detection after blanking time			30		ns
ZVD Output (Active Low)						
V_{THRESH_ZVD}	ZVD Detector Threshold		0.32		0.85	V
t_{3RD_ZVD}	Minimum third quadrant time that can be detected by ZVD detector (Low Side)	For a 0 to -1.5V to 0 pulse with 100ps rise/ fall time	6	10	14	ns
t_{3RD_ZVD}	Minimum third quadrant time that can be detected by ZVD detector (High Side)	For a 0 to -1.5V to 0 pulse with 100ps rise/ fall time	6	10	14	ns
$t_{DLY_ZVD_L}$	Delay between V_{THRESH_ZVD} cross vs ZVD output going low	For a 0 to -1.5V to 0 pulse with 100ps rise/ fall time		15	30	ns
$t_{DLY_ZVD_H}$	Delay between V_{THRESH_ZVD} cross vs ZVD output going low	For a 0 to -1.5V to 0 pulse with 100ps rise/ fall time		20	30	ns
t_{WD_ZVD}	ZVD pulse width	For a 0 to -1.5V to 0 pulse with 100ps rise/ fall time	40	65	110	ns
OTD						
OTD+	Over Temperature Detect high threshold			170		℃
OTD-	Over Temperature Detect high threshold			154		℃
OTD_{HYS}	Over Temperature Detect high threshold			16		℃
FAULT						

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GVDD = 5V, C_{GVDD} = 1uF + 220nF, $C_{BOOT-HS}$ = 200nF, EN/$\overline{FLT}$ is pulled up to GVDD with 4.7KΩ resistor, voltages are with respect to AGND and typical specifications are at 25℃ (1); –40℃ ≤ T_J≤125℃, (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{FLT}	Fault pin pull down current	V_{FLT} = 0.4 V	3			mA
t_{FLTDLY_1}	Time to indicate FLT after fault occurs for OCP and OTD			20		ns
t_{FLTDLY_2}	Time to indicate FLT after fault occurs for GVDD UVLO			1		µs
t_{FLT}	Min fault indication time		6	14	24	µs
t_{ENBLK}	Time after FLT release, after which EN=0 is effective			1		µs

(1) Parameters that show only a typical value are determined by design and can not be tested in production.
(2) See *Propagation Delay and Mismatch Measurement* section.
(3) Measured at fastest slew rate.

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6 Typical Characteristics

At T_A = 25°C, GVDD = 5V, C_{GVDD} = 1µF, $C_{BOOT-HS}$ = 220nF (Unless otherwise noted)

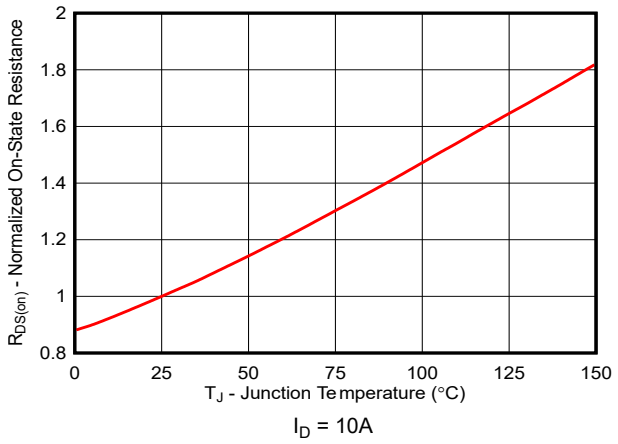

Figure 6-1. DRV7167 Normalized On-State Resistance vs Temperature

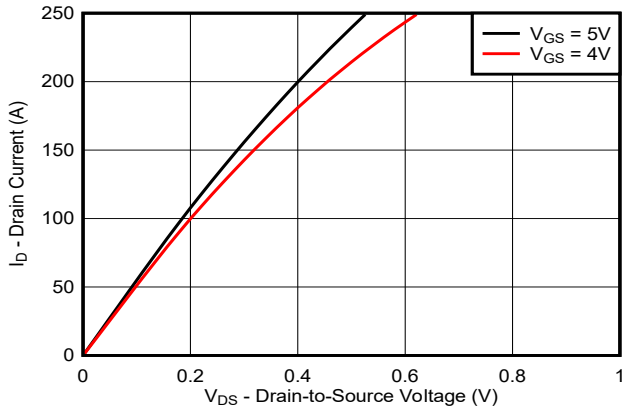

Figure 6-2. DRV7167 Typical Output Characteristics

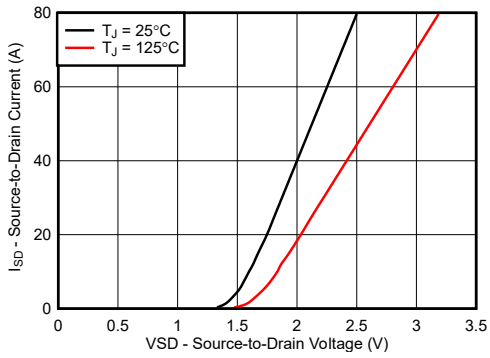

Figure 6-3. DRV7167 Reverse Drain-Source Characteristics

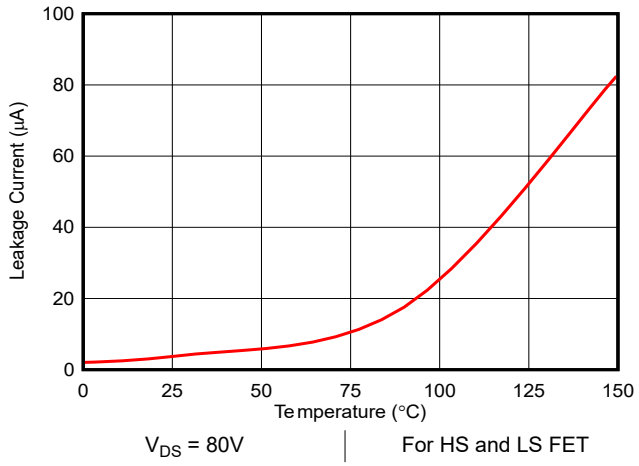

Figure 6-4. DRV7167: Drain Leakage Current

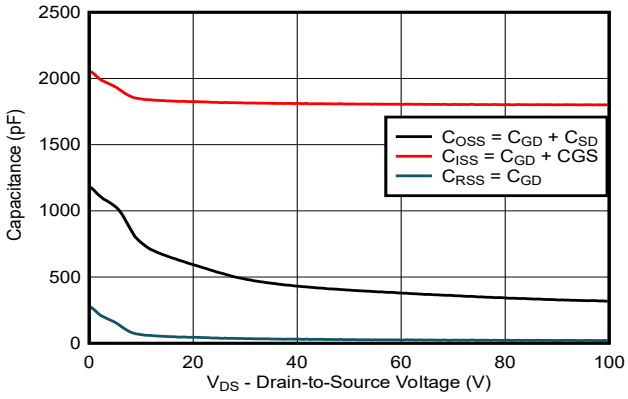

Figure 6-5. DRV7167: Typical Capacitance

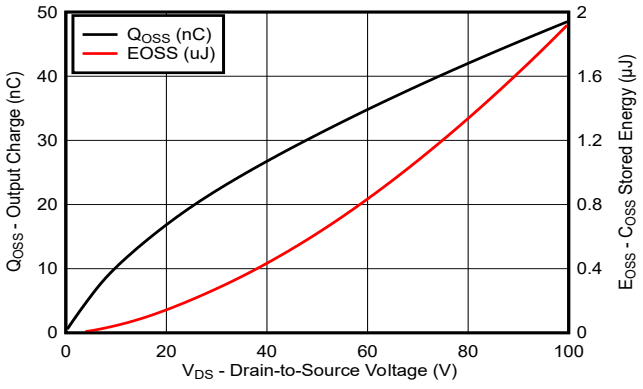

Figure 6-6. DRV7167 Typical Output Charge and Stored Energy

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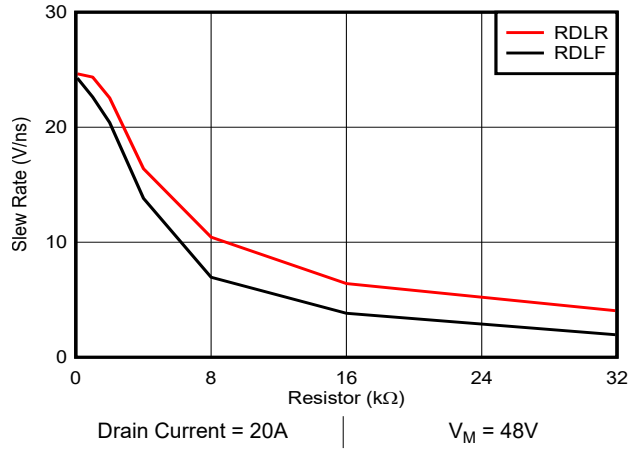

Figure 6-7. DRV7167: Slew Rate Control - Current entering into OUT pin

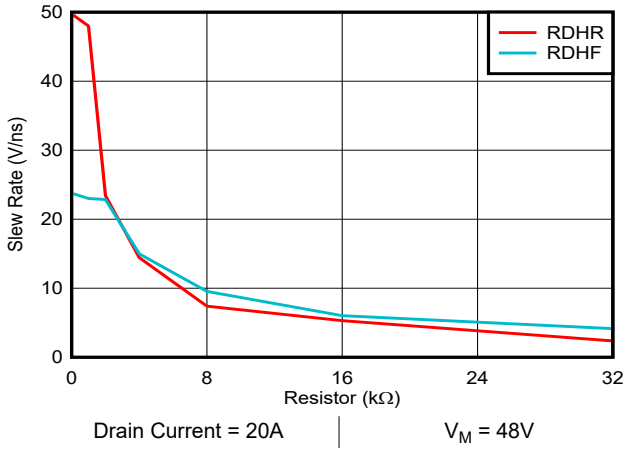

Figure 6-8. DRV7167: Slew Rate Control - Current leaving OUT pin

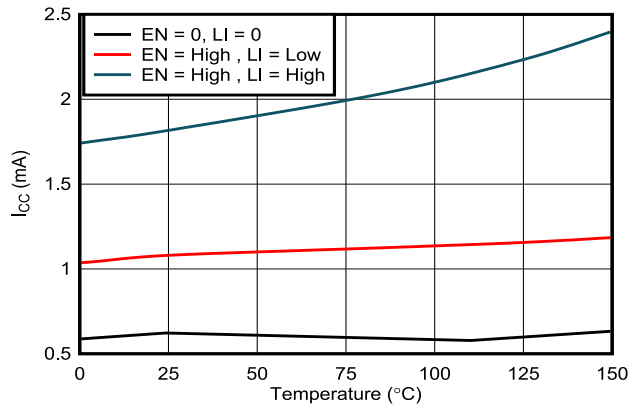

Figure 6-9. GVDD-AGND Current

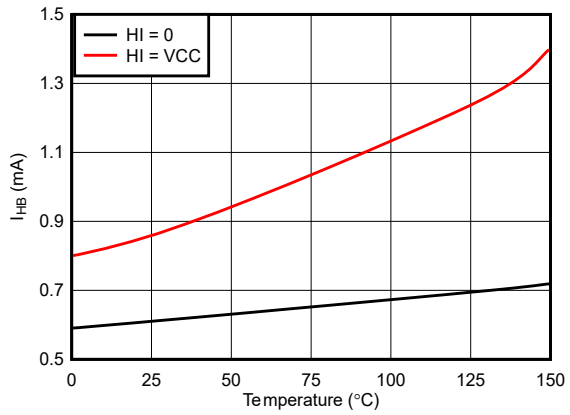

Figure 6-10. BOOT-HS Current

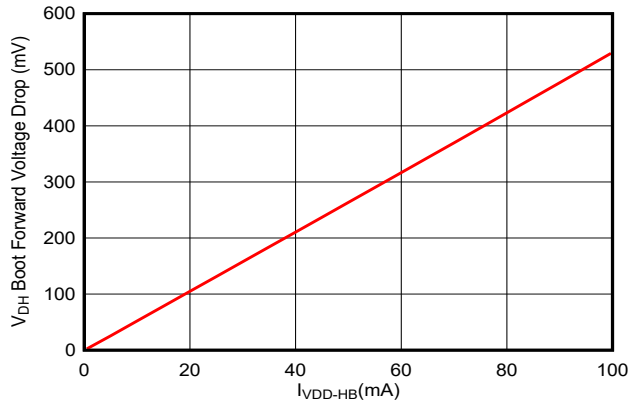

Figure 6-11. Bootstrap Forward Voltage versus Current

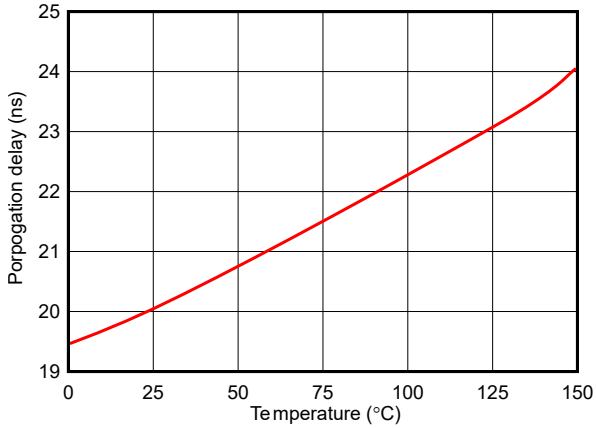

Figure 6-12. HI/LI Propagation Delay

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7 Parameter Measurement Information

7.1 Propagation Delay and Mismatch Measurement

The Figure 7-1 and Figure 7-2 are used to measure the propagation delay from the driver input to OUT node output and the delay mismatch. HI signal propagation delays, t_{HIPLH} and t_{HIPHL} are measured with 0Ω RDHR and RDHF resistor in "current leaving OUT pin" mode as shown in Figure 7-3. LI signal propagation delays t_{LIPLH} and t_{LIPHL} are measured with 0Ω RDLR and RDLF resistor in "current entering OUT pin" mode as shown in Figure 7-4. Propagation delay mismatch parameters are defined as

$$t_{MON} = |t_{HIPLH} - t_{LIPHL}| \quad (1)$$

$$t_{MOFF} = |t_{LIPLH} - t_{HIPHL}| \quad (2)$$

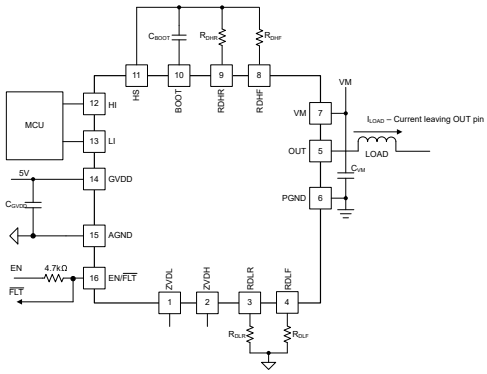

Figure 7-1. Propagation delay - Current leaving OUT pin

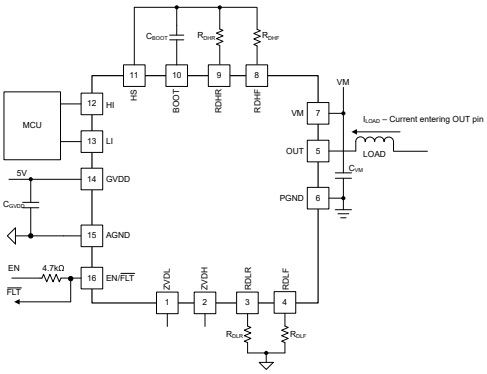

Figure 7-2. Propagation delay - Current entering OUT pin

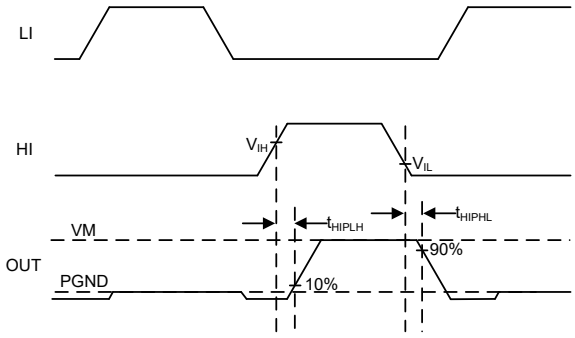

Figure 7-3. t_{PHILH} and t_{PHIHL} Measurement

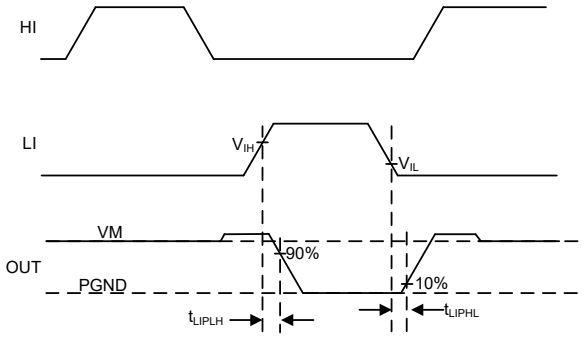

Figure 7-4. t_{PLILH} and t_{PLIHL} Measurement

7.2 Slew Rate Measurement

Figure 7-1 measures OUT node rising and falling slew rate corresponding to HI pulse for selected RDHR and RDHF resistors as shown in Figure 7-5. Slew is calculated from 20% to 80% rise or fall time of the OUT node as per Equation 3.

$$Slew_{RDXX} = (0.6 \times VM) / t_{RDXX} \quad (3)$$

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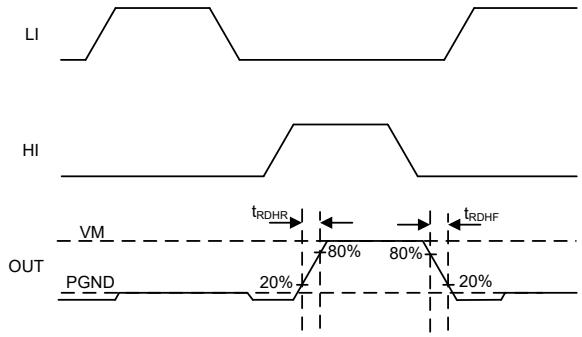

Figure 7-5. Slew Rate Measurement for RDHR and RDHF

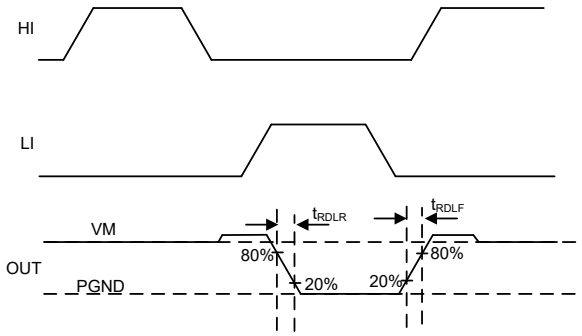

Figure 7-6. Slew Rate Measurement for RDLR and RDLF

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8 Detailed Description

8.1 Overview

DRV7167A is a highly-integrated, half-bridge GaN power stage incorporating high-side and low-side gate drivers, along with two GaN FETs in a half bridge configuration. The device supports use in isolated and non-isolated power architectures, and simplifies the design through driver and power stage integration. The optimized package layout minimizes parasitic inductance and simplifies PCB design. The driver supports programmable turn-on and turn-off control to optimize the EMI performance. The device includes several features to improve system performance, efficiency and protection, making the device prime for high power density BLDC applications.

8.2 Functional Block Diagram

Figure 8-1 shows the functional block diagram of the DRV7167A device with integrated high-side and low-side GaN FETs.

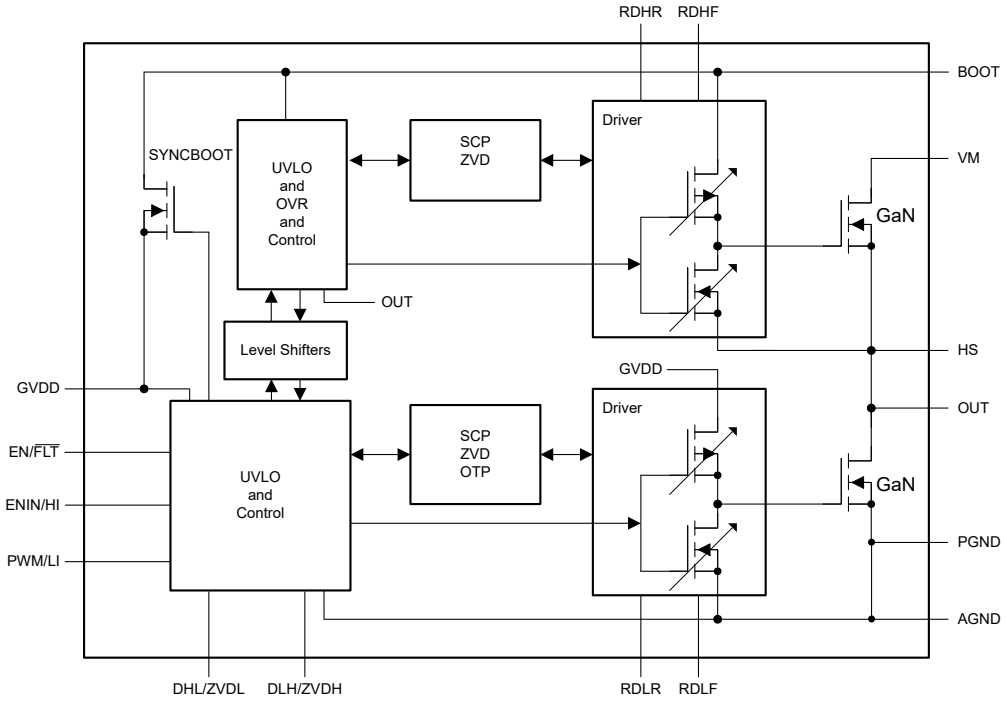

Figure 8-1. Functional Block Diagram

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8.3 Feature Description

The DRV7167A device simplifies the design of high-power-density PCBs by eliminating the need for underfill while maintaining required creepage and clearance distances. The device provides tightly matched propagation delays between the high-side and low-side gate drivers, enabling precise dead-time control, a factor that is critical in achieving high efficiency in GaN FET-based applications. Both HI and LI inputs are independently controllable to minimize third-quadrant conduction time. The propagation delay mismatch between the HI and LI channels, for both rising and falling edges, is typically 2ns, allowing extremely tight dead-time optimization. The device also supports a single PWM input mode with resistor-programmable dead-time adjustment for use with controllers that have limited I/O capability. By co-packaging the GaN FET half-bridge with the driver, the DRV7167A achieves optimized gate-loop inductance, significantly improving performance in hard-switched topologies.

An integrated bootstrap circuit with overvoltage regulation establishes that the high-side gate-to-source voltage (V_{GS}) remains within the safe operating limit of the GaN FET, eliminating the need for external protection components. The built-in driver includes undervoltage lockout (UVLO) protection on both the GVDD and BOOT–HS rails. When either rail voltage falls below the UVLO threshold, the device ignores HI and LI commands to prevent partial FET turn-on. If GVDD remains above 2.5V and below UVLO threshold, the driver actively pulls both gate driver outputs low. Hysteresis on the UVLO threshold prevents chatter and false triggering due to supply noise or transients

The DRV7167A integrates V_{DS}-based short-circuit protection for both FETs, along with over-temperature reporting. Additional features include zero-voltage detection (ZVD) which enables dead-time optimization and minimize third-quadrant conduction losses.

8.3.1 Control Inputs

DRV7167A supports IIM mode and single PWM Mode. In Independent Input Mode (IIM), the DRV7167A input pins are independently controlled with TTL input thresholds and support 3.3V and 5V logic levels. Table 8-1 describes the configuration for single PWM mode and IIM mode.

Table 8-1. Control Input Configuration

MODE	CONFIGURATION
IIM Mode	• Connect resistor on RDLF pin (pin 4) to AGND pin (pin 15). • ENIN/HI (pin 12) is the control input for high side gate drive and PWM/LI (Pin 13) is the control input for low side gate drive.
Single PWM Mode	• Float RDLF pin (pin 4) to enable the Single PWM mode, to confirm float detection, verify that the RDLF pin has less than 10pF parasitic capacitance. • Keep ENIN/HI (pin 12) high to enable the gate drive for both high side and low side FET. • PWM/LI (pin 13) is the control input for PWM. Low side FET turns on, when PWM is high and high-side FET turns on when PWM FET is low.

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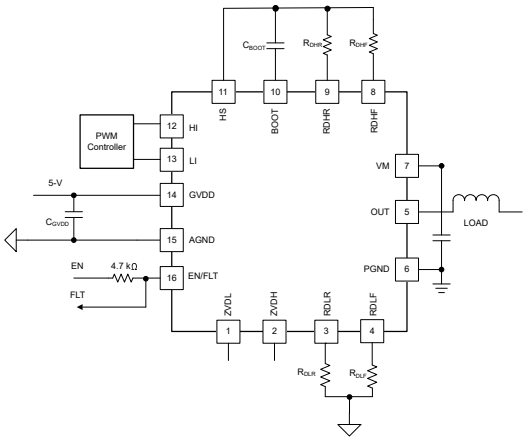

Figure 8-2. IIM Mode

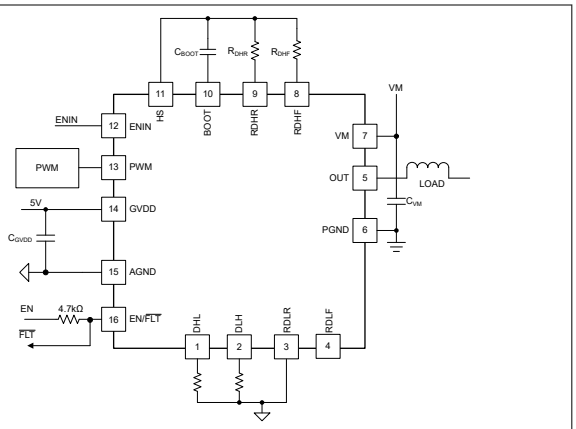

Figure 8-3. Single PWM Mode

DRV7167A implements overlap protection functionality (interlock), to prevent a shoot-through condition if both HI and LI are asserted high. If both HI and LI are asserted, both the high-side and low-side GaN FETs are turned off.

When used in single PWM mode, the DRV7167A operates from a single PWM input, with the dead-times between low-to-high set by the external resistors on the pins DLH and high-to-low transitions set by external resistors on the DHL pins, as specified in Section 8.3.2.

8.3.1.1 EN/$\overline{\text{FLT}}$ Control

EN/$\overline{\text{FLT}}$ is a multiplexed device enable and fault indicator pin. Keep the EN/$\overline{\text{FLT}}$ pin high to keep the device functionality enabled. In the event of a fault condition, the device pulls the EN/$\overline{\text{FLT}}$ pin low in an open-drain configuration for a duration of t_{FLT} as described in Section 8.3.8. An enable resistor is required to limit the current into the EN/$\overline{\text{FLT}}$ pin during this period. The enable functionality is masked and the device remains enabled during the fault condition, as described in Figure 8-4. Place a decoupling capacitor close to the device to avoid noise coupling on EN/$\overline{\text{FLT}}$ pin. The enable signal is masked for t_{ENBLK} time after fault is released. Establish that the EN/$\overline{\text{FLT}}$ pin has low parasitic capacitance to support faster rise after the fault is released. Pull EN/$\overline{\text{FLT}}$ low externally to disable the device.

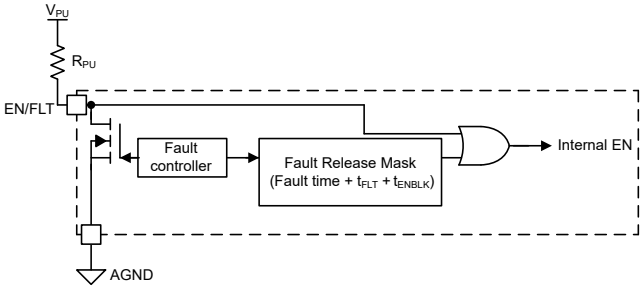

Figure 8-4. EN/$\overline{\text{FLT}}$ Pin Block Diagram

8.3.2 Dead Time Setting in Single PWM Mode

DRV7167A supports single PWM mode for IO limited controllers. Float the RDLF pin to enable the single PWM mode. Keep the ENIN/HI pin high to enable the driver. Resistors (0Ω to 100kΩ) on DHL and DLH set the dead time for high to low transition and low to high transition at switch node as per Equation 4 and Equation 5. Figure 8-5 explains how the PWM inputs from the high side (HS) and low side (LS) GaN FET derive from the single PWM input. DRV7167A generates a complimentary PWM, which is 180° phase shifted signal of the PWM input. The device generates the LS FET PWM input by delaying the rising edge of PWM input by t_{DHL} time to provide dead time and HS FET PWM input by delaying the rising edge of complimentary PWM input by t_{DLH} time to

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provide dead time. TI recommends choosing sufficient dead time for the selected slew rate setting to avoid any shoot through.

$$t_{DHL}(ns) = 1/3 \times R_{DHL}(k\Omega) + 7.5 \quad (4)$$

$$t_{DLH}(ns) = 1/3 \times R_{DLH}(k\Omega) + 7.5 \quad (5)$$

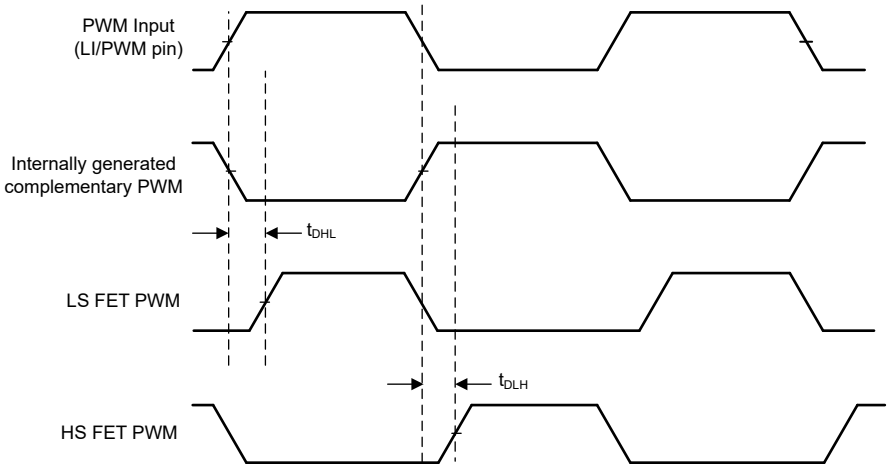

Figure 8-5. PWM Mode Operation

8.3.3 Start-up and UVLO

The DRV7167A ignores HI and LI inputs at the time of start-up for $t_{start-up}$ duration. The device has UVLO protection on both the GVDD and BOOT (bootstrap) supplies. Post start-up, when the GVDD voltage falls below GVDD falling edge threshold (V_{GVDDF}) both the HI and LI inputs are ignored, and gates of high side and low side GaN FETs are actively pulled low to prevent the GaN FETs from partially turning on. When the BOOT to HS bootstrap voltage is below the UVLO threshold V_{BOOTF}, only the high-side GaN FET gate is pulled low. Both UVLO threshold voltages have 200mV of hysteresis to avoid chattering. A deglitch filter of 1µs is implemented on UVLO detect circuit to avoid false trigger due to noise. The device reports fault for GVDD UVLO as shown in Figure 8-14.

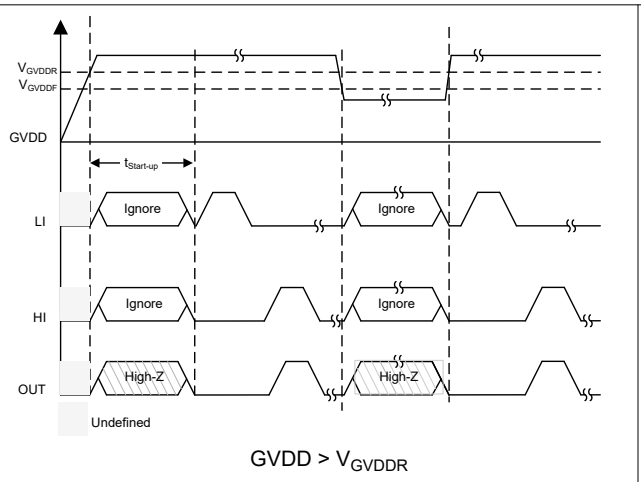

Figure 8-6. GVDD UVLO

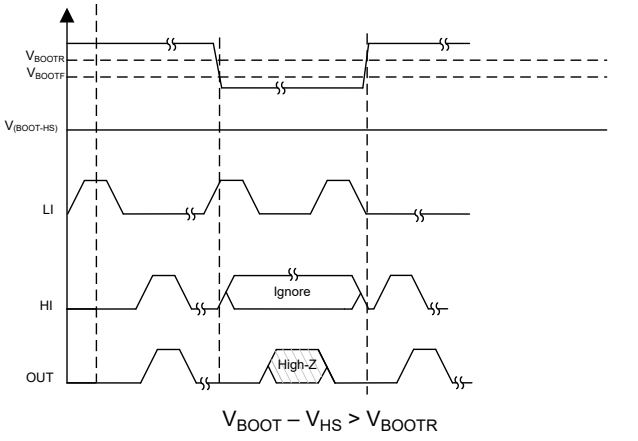

Figure 8-7. BOOT UVLO

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8.3.4 Synchronous Bootstrap

The DRV7167A incorporates a synchronous bootstrap circuit from GVDD to BOOT, providing a bias ($V_{BOOT-HS}$) for the high-side driver. The regulated supply makes sure that the gate voltage does not exceed the maximum gate-to-source voltage (V_{BOOTth_R}) rating of enhancement-mode GaN FETs due to third quadrant conduction. The integrated bootstrap FET offers fast recovery, low on-resistance of 5Ω, and sufficient voltage margin to establish efficient and reliable bootstrap operation. Figure 8-8 explains the control mechanism of bootstrap. An external capacitor connected between the BOOT and HS pins recharges during every switching cycle when the LI input goes high. Boot regulator verifies that the boot cap charges between V_{BOOTth_U} and V_{BOOTth_L}, as described in Figure 8-9. TI recommends providing a sufficient LI pulse to charge the boot capacitor as per t_{ss} time during start-up. DRV7167A has inrush current control while charging the bootstrap at the time of start-up to avoid voltage droop on GVDD pin. The boot control mechanism avoids reverse recovery of the synchronous bootstrap FET body diode to couple on GVDD and BOOT pins, therefore, the effective Q_{RR} is 0 for synchronous bootstrap. The boot control mechanism reduces the ripple on GVDD and HS caps and eases the sizing constraint of GVDD-AGND and BOOT-HS caps. TI recommends an isolated supply with respect to HS node for the applications where sufficient LI pulse is not possible to charge the boot capacitor. Note that the gate voltage of the high-side GaN FET is not clamped internally. Hence, to prevent exceeding the high-side GaN transistor gate breakdown voltage, keep the external isolated bias supply within the recommended operating conditions. Refer to Section 9.2.2.1 for the bootstrap capacitor value recommendation.

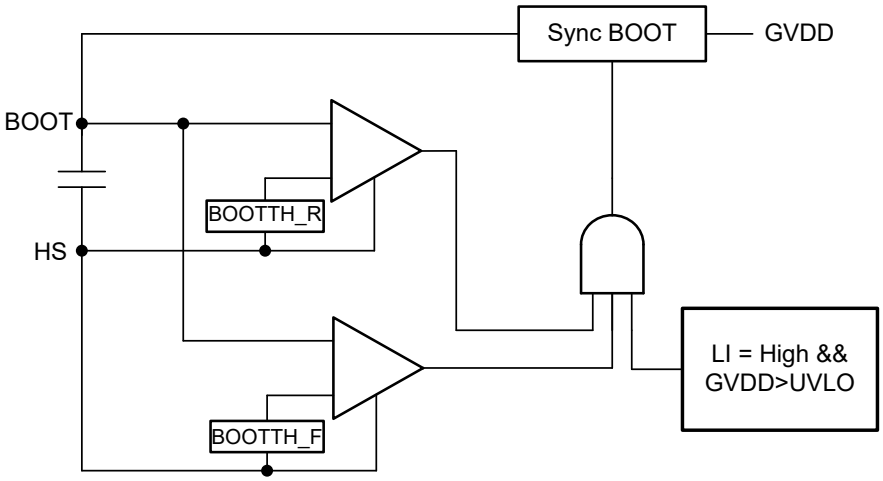

Figure 8-8. Synchronous Bootstrap Control Logic

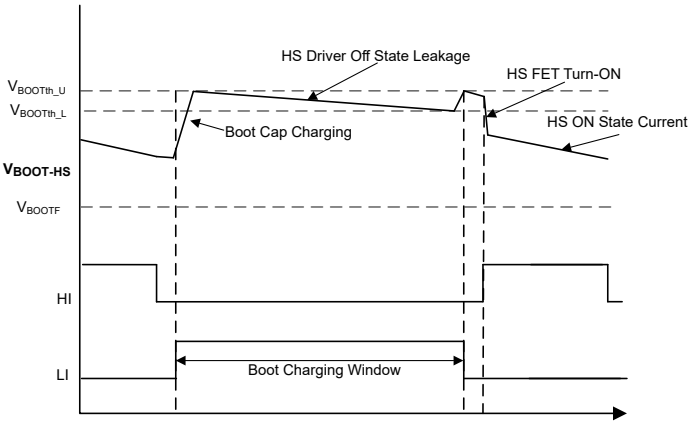

Figure 8-9. Boot Capacitor Charging Profile

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8.3.5 Level Shift

The level-shift circuit is the interface from the high-side input HI to the high-side driver stage, which is referenced to the switch node (HS). The level shift allows control of the high-side GaN FET gate driver output, which is referenced to the HS pin and provides excellent delay matching with the low-side driver.

8.3.6 Zero Voltage Detection (ZVD) Reporting

The DRV7167A supports zero voltage detection (ZVD) to indicate whether the high-side and low-side FETs transitioned to third-quadrant for more than t_{3RD_ZVD} time in any switching cycle. ZVD information is reported on ZVDH (for high-side FET) and ZVDL (for low-side FET) pins. The ZVD feature is only available in IIM mode.

For the low-side FET, if in a particular transition the switch node falls V_{THRESH_ZVD} below AGND for a time period greater than t_{3RD_ZVD}, a low pulse of t_{WD_ZVD} generates with a delay of $t_{DLY_ZVD_L}$.

For the high-side FET, if in a particular transition the switch node rises V_{THRESH_ZVD} above VM for a time period greater than t_{3RD_ZVD}, a low pulse of t_{WD_ZVD} generates after a one PWM cycle, with a delay of $t_{DLY_ZVD_H}$ from the corresponding LI transition.

A controller interfacing DRV7167A can use the ZVD information to adjust dead-times and minimize the third quadrant conduction time of the high-side and low-side FETs.

Figure 8-10 shows the ZVDL signals when DRV7167A is actively sourcing current into the motor winding (phase current flows out of the OUT pin toward the motor). During the dead-time, when both FETs are off, the switch node transitions below AGND, and the low-side FET enters third-quadrant conduction. This information is reported on ZVDL. Ignore the ZVDH signal when only low side GaN is soft switched.

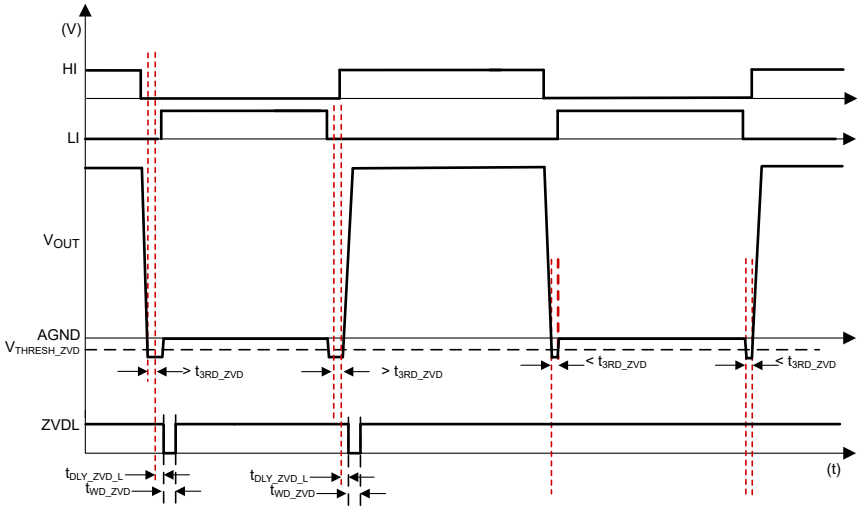

Figure 8-10. ZVD Reporting - Current flowing out of the OUT pin

Figure 8-11 shows the ZVDH signals when DRV7167A is sinking current out of the motor winding (phase current flows into the OUT pin). During the dead-time, when both FETs are off, the switch node transitions above VM, and the high-side FET enters third-quadrant conduction. This information is reported on ZVDH with a one-PWM cycle delay. Ignore the ZVDL signal when only high side GaN is soft switched.

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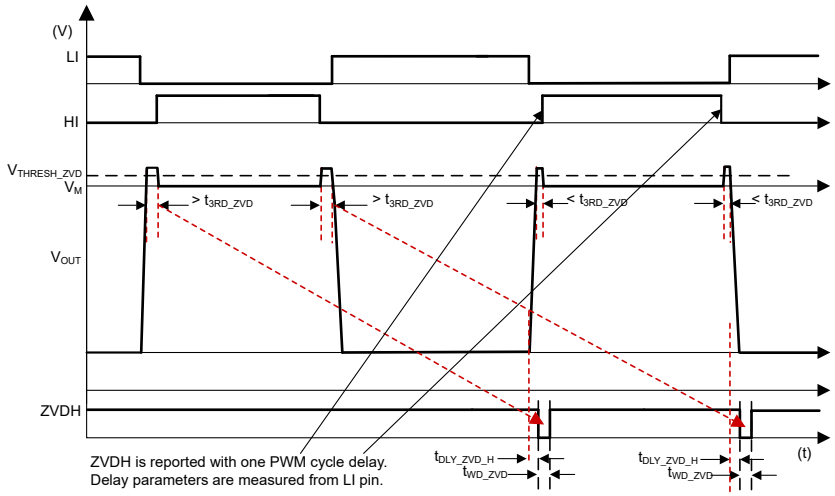

Figure 8-11. ZVD Reporting - Current flowing into the OUT pin

8.3.7 Slew Rate Control

As described in Pin Functions, turn-on and turn-off drive strength of HS and LS FETs are controlled independently through:

- RDHF pin controls the falling gate drive strength of the high side FET.
- RDHR pin controls the rising gate drive strength of the high side FET.
- RDLF pin controls falling gate drive strength of the low side FET.
- RDLR pin controls the rising gate drive strength of the low side FET.

Using the above listed resistors allows users to optimize the tradeoff between higher efficiency (faster slew rates) and lower ringing (slower slew rates). Figure 8-12 and Figure 8-13 shows the typical variation of slew rate with resistor. The circuitry in the device adjusts drive strength versus temperature to keep constant slew rate across the temperature. Therefore, overall gate loop remains small because RDxx is not in main gate drive loop, achieving better performance than a discrete gate driver with an external gate resistor.

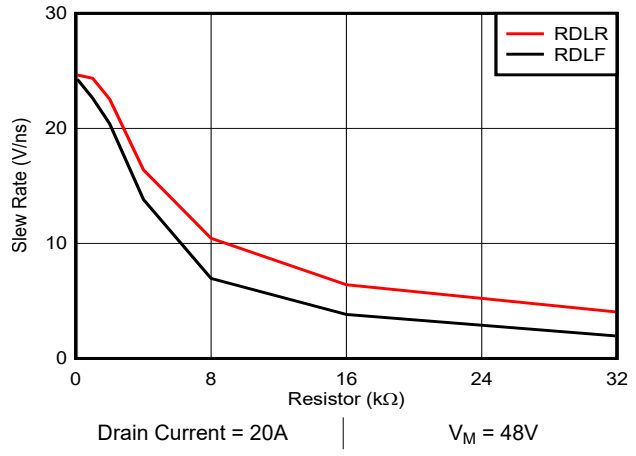

Figure 8-12. DRV7167: Slew Rate Control - Current entering into OUT pin

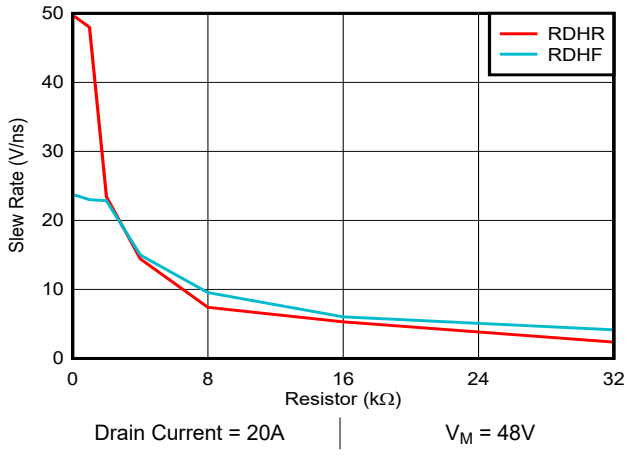

Figure 8-13. DRV7167: Slew Rate Control - Current leaving OUT pin

8.3.8 Fault Indication

The DRV7167A indicates three types of faults on the EN/$\overline{\text{FLT}}$ pin:

- UVLO event on the GVDD supply

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- Short-circuit event on the low-side GaN FET
- Overtemperature event on the driver

After asserted, the active low fault signal remains asserted as long any of the three faults exist, and for t_{FLT} after all faults cease to exist.

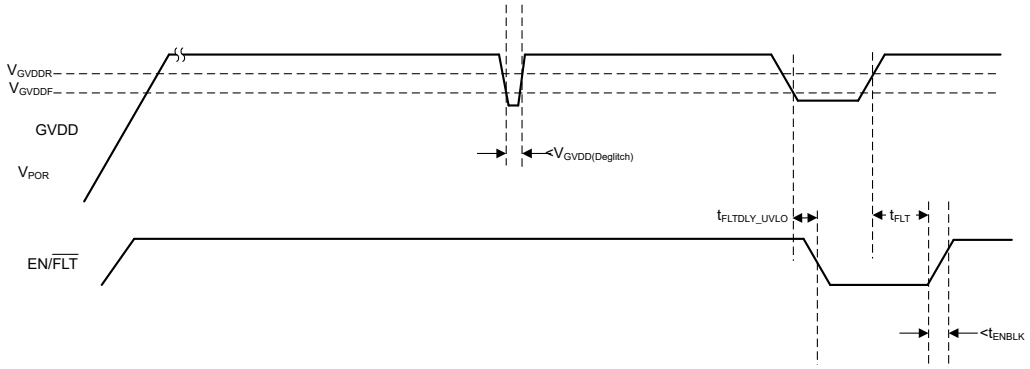

Figure 8-14. UVLO Fault Reporting

8.3.9 Overcurrent Protection (OCP)

The DRV7167A implements drain-to-source voltage (V_{DS}) monitoring-based Overcurrent/short-circuit protection on both FETs. After either FET turns on through HI/LI = high, the device waits for a time t_{BLANK}. After the wait, the V_{DS} voltage of the FET is sensed, if the voltage is greater than V_{DSAT}, a short circuit is inferred. Thereafter, the FET turns off within ≅10ns to prevent damage. Overcurrent protection operates on a cycle-by-cycle basis, every HI/LI logic low-to-high cycle turns on the FET. If the V_{DS} exceeds the set threshold, the OCP turns off the FET for the remainder of the HI/LI logic-high duration. The OCP protection is implemented only for current flowing from drain to source. DRV7167A triggers fault only for low side FET OCP event, as shown in Figure 8-15, HS FET OCP event turns off the FET for the given cycle and does not change the EN/$\overline{FLT}$ status, as shown in Figure 8-16.

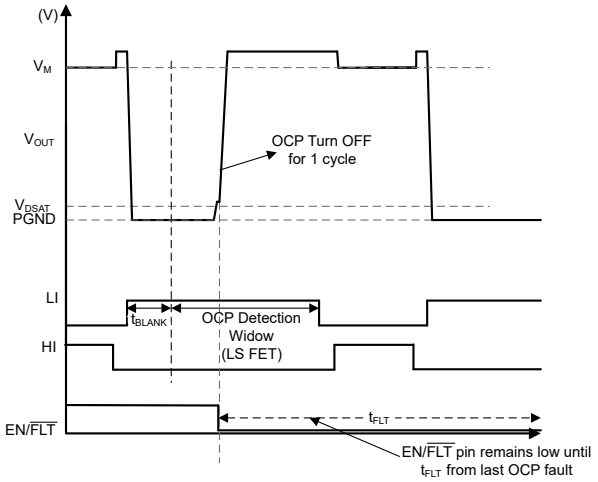

Figure 8-15. LS FET OCP Event - Current flowing into OUT pin

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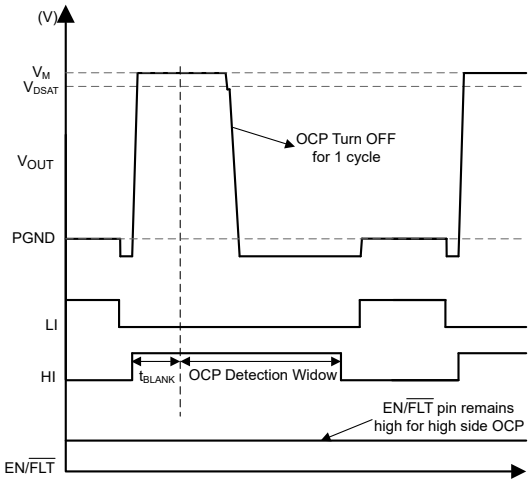

Figure 8-16. HS FET OCP Event - Current flowing out of OUT pin

8.3.10 Over Temperature Detection (OTD)

The DRV7167A monitors the die temperature of the integrated gate-driver and indicates a fault when the OTD+ threshold is exceeded. The device does not take any other action, for example, the device does not turn-off the GaN FETs upon detecting over-temperature, leaving any such protection action to the external PWM controller.

Depending on the operating conditions, and system thermal design, a temperature difference between the GaN FETs and the integrated driver is possible.

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8.4 Device Functional Modes

The DRV7167A operates in normal mode when the GVDD-AGND and BOOT-HS are above UVLO. Refer to *Section 8.3.3* for information on UVLO operation mode. In the normal mode, the output state is dependent on the states of the HI and LI pins.

Table 8-2 lists the output states for different input pin combinations for DRV7167A in IIM mode. This device supports overlap protection/interlock functionality. If both HI and LI are asserted, both GaN FETs in the power stage are turned off.

Table 8-2. Truth Table (DRV7167A)

HI	LI	HIGH-SIDE GaN FET	LOW-SIDE GaN FET	OUT
L	L	OFF	OFF	Hi-Z
L	H	OFF	ON	PGND
H	L	ON	OFF	VM
H	H	OFF	OFF	Hi-Z

Table 8-3 lists the output states for different input pin combinations for DRV7167A in single PWM mode.

Table 8-3. Single PWM Mode Truth Table

ENIN	PWM	HIGH-SIDE GaN FET	LOW-SIDE GaN FET	OUT
L	L	OFF	OFF	Hi-Z
L	H	OFF	OFF	Hi-Z
H	L	ON	OFF	VM
H	H	OFF	ON	PGND

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The DRV7167A GaN power stage is a versatile building block for Motor Driver applications. The high-performance gate driver with GaN FETs integration minimizes parasitics and enables extremely fast and efficient switching of the GaN FETs.

9.2 Typical Application

Figure 9-1 shows a BLDC Motor Driver application with GVDD connected to a 5V supply. Optimizing the power loop (loop impedance from VM capacitor to PGND) is critical. Having a high power loop inductance causes significant ringing in the OUT node and also causes the associated power loss. The DRV7167A has VM and PGND pins next to each other. This enables the VM capacitor to be placed very close to DRV7167A on the top layer of the PCB, minimizing power loop inductance.

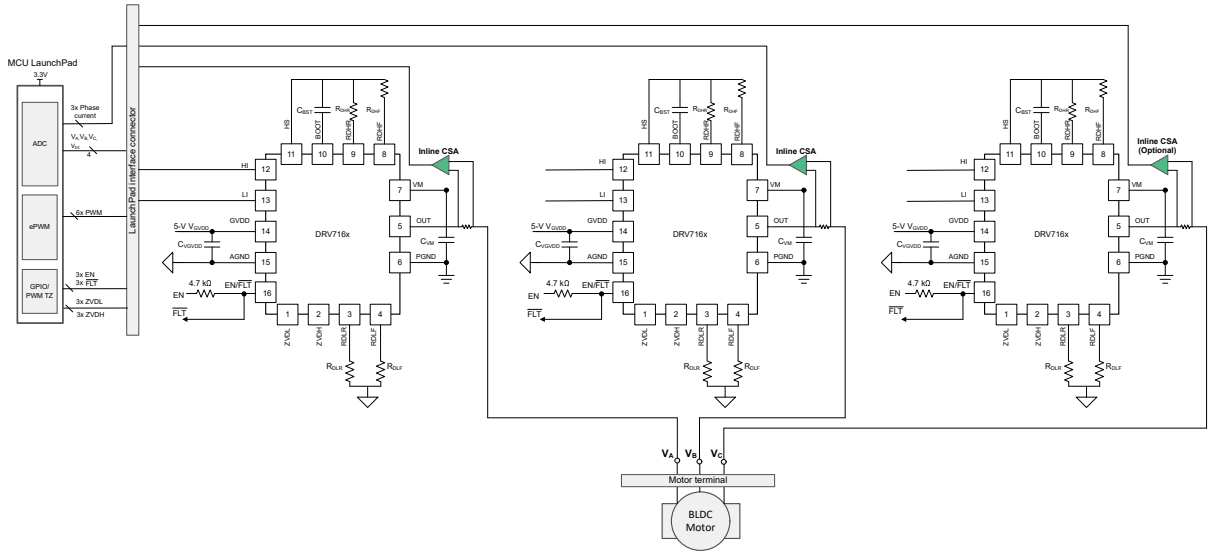

Figure 9-1. Typical Connection Diagram for a BLDC Motor in IIM Mode

9.2.1 Design Requirements

Table 9-1 lists the example input parameters for the system design.

Table 9-1. Design Parameters

PARAMETER	SAMPLE VALUE
Half-bridge input supply voltage, V_M	48 V
Motor rms current	20A
Motor peak current	60 A
V_{BOOT}-V_{HS} bootstrap capacitor	0.22 uF, X5R
Switching frequency	100 kHz
Dead time	15 ns
Slew rate setting	10 V/ns

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9.2.2 Detailed Design Procedure

This procedure outlines the design considerations of DRV7167A in a BLDC Motor Application. For additional design help, see Section 10.1.1.

9.2.2.1 Bootstrap Capacitor

The bootstrap capacitor provides the gate charge for the high-side gate drive, dc bias power for BOOT UVLO circuit, and the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated using Equation 6.

$$C_{BST} = (Q_G + Q_{RR} + I_{BOOT} * t_{ON(max)}) / \Delta V \quad (6)$$

where

- I_{BOOT} is the quiescent current of the high-side gate driver
- t_{ON}(maximum) is the maximum on-time period of the high-side gate driver
- Q_{RR} is the reverse recovery charge of the bootstrap diode
- Q_G is the gate charge of the high-side GaN FET
- ΔV is the permissible ripple in the bootstrap capacitor (< 100 mV, typical)

A 0.22-µF, 16-V, 0402 ceramic capacitor is suitable for most applications. Place the bootstrap capacitor as close as possible to the BOOT and HS pins.

9.2.2.2 GVDD Bypass Capacitor

The GVDD bypass capacitor provides the gate charge for the low-side and high-side GaN FETs. Calculate the required bypass capacitance using Equation 7.

$$C_{GVDD} = (2 \times Q_G) / \Delta V \quad (7)$$

where

- Q_G = individual and equal gate charge of the high-side and low-side GaN FETs
- ΔV = maximum allowable voltage drop across the bypass capacitor

A 1µF or larger value capacitor along with high frequency, good-quality, small package ceramic capacitor of 100nF is recommended. Place the high frequency bypass capacitor as close as possible to the GVDD and AGND pins of the device to minimize the parasitic inductance in low side gate drive loop.

9.2.2.3 Power Dissipation

The total power dissipation of the DRV7167A device is the sum of the high side and low side gate driver losses, the boot strap power loss, and the switching and conduction losses in the GaN FETs.

The gate driver losses are incurred by charge and discharge of the of the parasitic capacitance of GaN FET. Approximate the loss using Equation 8.

$$P = Q_G \times f_{SW} \times (GVDD + V_{BOOT}) \quad (8)$$

where

- Q_G = gate charge
- f_{SW} = switching frequency
- GVDD = bias supply at GVDD pin
- V_{BOOT} = voltage across BOOT-HS pins

The bootstrap circuit dissipates power while charging the boot strap capacitor through boot FET turn-on resistor. This loss is proportional to the frequency. There are some additional losses in the gate driver due to the internal driver stage.

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The power losses due to the GaN FETs is divisible into conduction losses and switching losses. Conduction losses are resistive losses and are calculated using Equation 9.

$$P_{COND} = \left[\left(I_{RMS(HS)}\right)^2 \times RDS_{(on)HS}\right] + \left[\left(I_{RMS(LS)}\right)^2 \times RDS_{(on)LS}\right] \quad (9)$$

where

- $R_{DS(on)HS}$ = high-side GaN FET on-resistance at operating T_J.
- $R_{DS(on)LS}$ = low-side GaN FET on-resistance at operating T_J.
- $I_{RMS(HS)}$ = high-side GaN FET RMS current.
- $I_{RMS(LS)}$ = low-side GaN FET RMS current.

Compute the switching losses to a first order using Equation 10, where t_{TR} can be approximated by dividing V_M by slew rate (V/ns) set by RDXX resistor for hard switched FET.

$$P_{SW} = 0.5 \times V_M \times I_{OUT} \times (t_{TR_R} + t_{TR_F}) \times f_{SW} + (V_M \times V_M \times C_{OSS(TR)} \times f_{SW}) \quad (10)$$

where

- t_{TR_R} = sum of the switch node transition times from ON to OFF and from OFF to ON.
- $C_{OSS(TR)}$ = output capacitance of each GaN FET.

Refer to the E_{ON} and E_{OFF} values for detailed calculation of swiitching loss. The soft switched GaN FET enters into the third quadrant during the dead time. Compute the third quadrant loss using Equation 11.

$$P = 2 \times V_{SD} \times I_{LOAD} \times f_{SW} \times t_{3rd} \quad (11)$$

where

- V_{SD} = third quadrant voltage.
- I_{LOAD} = current in soft switched FET.
- f_{SW} = switching frequency.
- t_{3rd} = time for which GaN FET stays in 3rdquadrant. This equation assumes that the third quadrant time before LS FET turns on and after LS FET turns off are same.

Switching frequency directly effects device power dissipation. Although the gate driver of the DRV7167A device is capable of driving the GaN FETs at frequencies up to 500 kHz, carefully consider the running conditions for the device to verify that the conditions meet the recommended operating temperature specifications. Hard-switched topologies like BLDC Motor drivers tend to generate more losses and self-heating than soft-switched applications.

The sum of the driver loss, the bootstrap loss, and the switching and conduction losses in the GaN FETs is the total power loss of the device. Careful board layout with an adequate amount of thermal vias close to the power pads (VM and PGND) allows for optimum power dissipation from the package. A top-side mounted heat sink with airflow can also improve the package power dissipation. Verify that the power loss in the driver and the GaN FETs is maintained below the maximum power dissipation limit of the package at the operating temperature.

9.2.3 Application Curves

9.2.3.1 Slew rate plots

Figure 9-2 through Figure 9-5 outline the switching transient voltage, propagation delay, and the configurable slew rate (20% to 80%) for both rising and falling edge with the output phase current at 10A_{RMS} and 80kHz PWM frequency. Overshoot voltage is around 14V when 0Ω control resistors are implemented.

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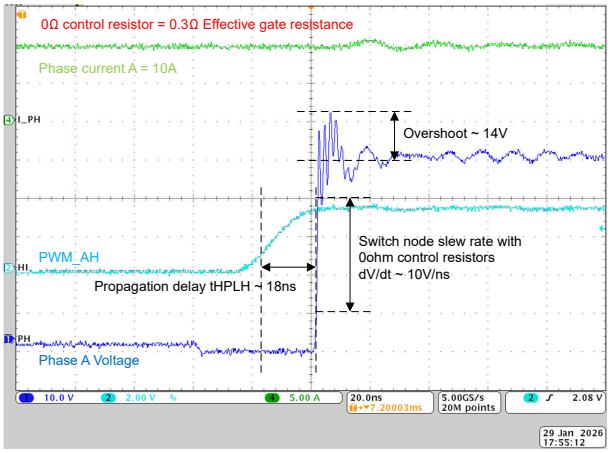

Figure 9-2. Rising Slew Rate With 0Ω Control Resistor

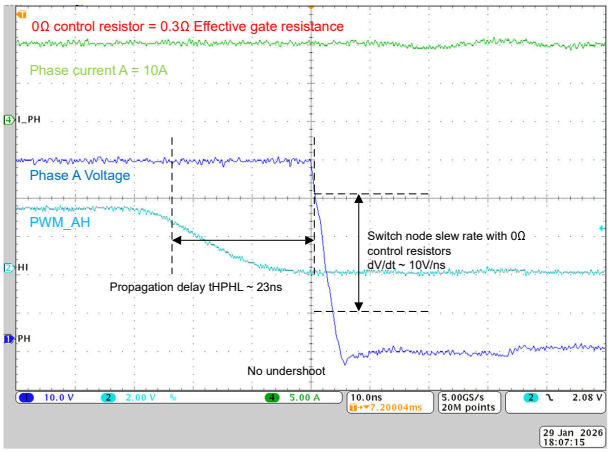

Figure 9-3. Falling Slew Rate With 0Ω Control Resistor

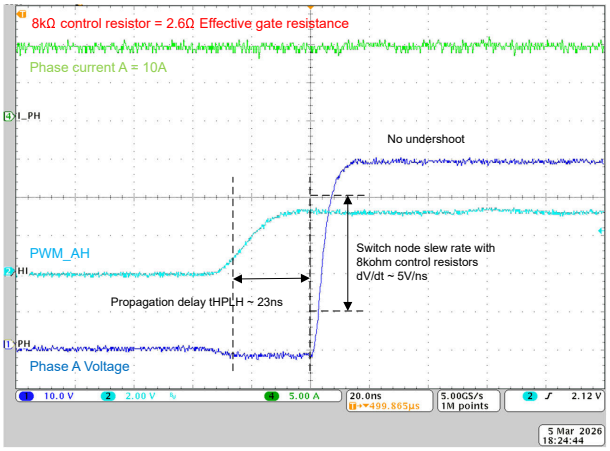

Figure 9-4. Rising Slew Rate With 8kΩ Control Resistor

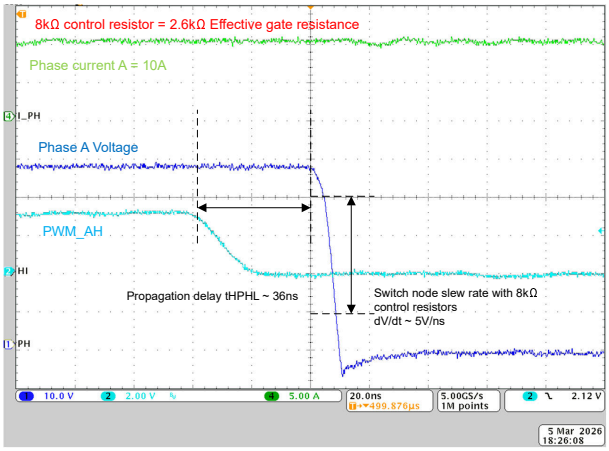

Figure 9-5. Falling Slew Rate With 8kΩ Control Resistor

9.3 Power Supply Recommendations

The recommended bias supply voltage range for DRV7167A is from 4.5 V to 5.5 V. Note that the gate voltage of the low-side GaN FET is not clamped internally. Hence, it is important to keep the GVDD bias supply within the recommended operating range to prevent exceeding the low-side GaN transistor gate breakdown voltage.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the GVDD voltage drops, the device continues to operate in normal mode as far as the voltage drop does not exceeds the hysteresis specification, $V_{GVDD(hyst)}$. If the voltage drop is more than hysteresis specification, the device shuts down. Therefore, while operating at or near the 4.5 V range, the voltage ripple on the auxiliary power supply output must be smaller than the hysteresis specification of DRV7167A to avoid triggering device-shutdown.

Place a local bypass capacitor between the GVDD and AGND pins. This capacitor must be located as close as possible to the device. A low ESR, ceramic surface-mount capacitor is recommended. TI recommends using 2 capacitors across GVDD and AGND: a 100 nF ceramic surface-mount capacitor for high frequency filtering placed very close to GVDD and AGND pin, and another surface-mount capacitor, 1 µF to 10 µF, for IC bias requirements.

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9.4 Layout

9.4.1 Layout Guidelines

To maximize the efficiency benefits of fast switching, it is extremely important to optimize the board layout such that the power loop impedance is minimal. When using a multilayer board (more than 2 layers), power loop parasitic impedance is minimized by having the return path to the input capacitor (between VM and PGND), small and directly underneath the first layer as shown in Figure 9-6 and Figure 9-7. Loop inductance is reduced due to flux cancellation as the return current is directly underneath and flowing in the opposite direction.

Insufficient attention to the above power loop layout guidelines can result in excessive overshoot and undershoot on the switch node.

It is also critical that the GVDD capacitors and the bootstrap capacitors are as close as possible to the device and in the first layer. Carefully consider the AGND connection of DRV7167A device. It must NOT be directly connected to PGND so that PGND noise does not directly shift AGND and cause spurious switching events due to noise injected in HI and LI signals.

Refer DRV7167A EVM for an actual layout based on these recommendations.

9.4.2 Layout Examples

Placements shown in Figure 9-6 and in the cross section of Figure 9-7 show the suggested placement of the device with respect to sensitive passive components, such as VM, bootstrap capacitors (HS and BOOT) and GVDD capacitors. Use appropriate spacing in the layout to reduce creepage and maintain clearance requirements in accordance with the application pollution level. Inner layers if present can be more closely spaced due to negligible pollution.

The layout must be designed to minimize the capacitance at the OUT node. Use as small an area of copper as possible to connect the device OUT pin to the inductor, or transformer, or other output load. Furthermore, ensure that the ground plane or any other copper plane has a cutout so that there is no overlap with the OUT node, as this would effectively form a capacitor on the printed circuit board. Additional capacitance on this node reduces the advantages of the advanced packaging approach of the DRV7167A and may result in reduced performance.

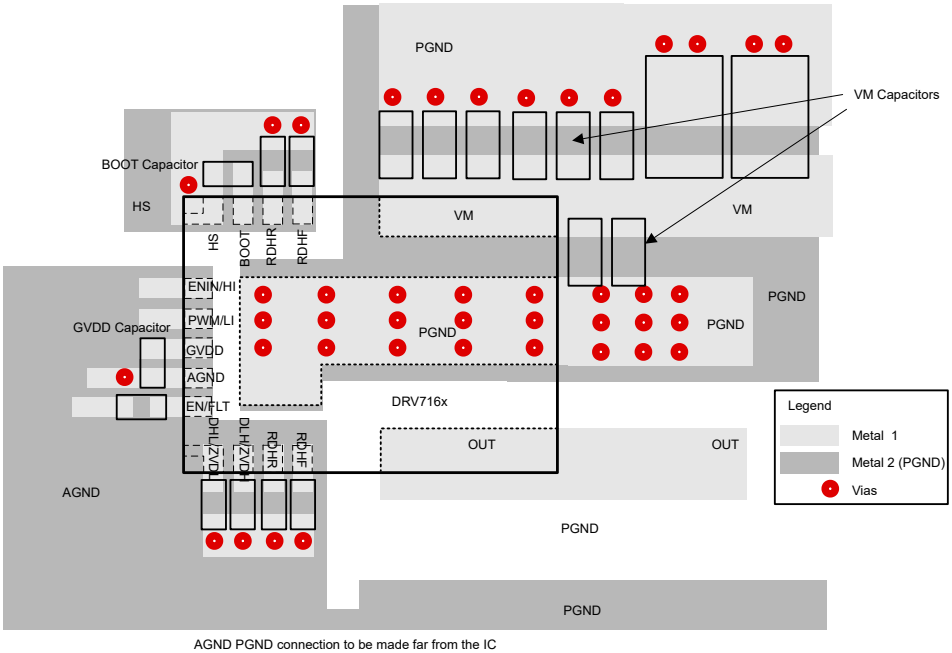

Figure 9-6. External Component Placement (Multi-layer PCB)

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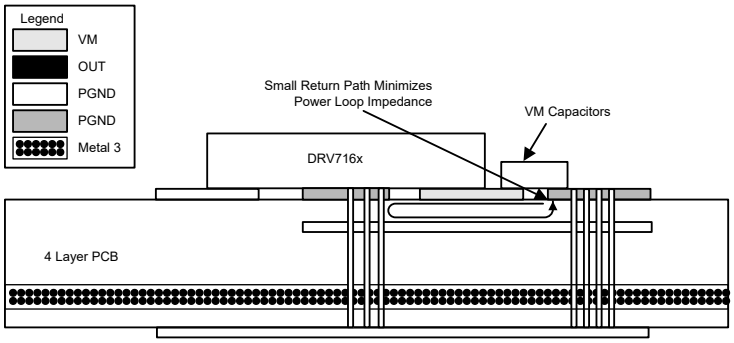

Figure 9-7. Four-Layer Board Cross Section With Return Path Directly Underneath for Power Loop

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- Texas Instruments, *Motor Control in Humanoid Robots*
- Texas Instruments, *48V 1kW Robot Joint Motor control with Industrial Communication reference design*
- Texas Instruments, *Layout Guidelines for LMG2100R044 GaN Power Stage Module*
- Texas Instruments, *LMG2100 Evaluation Module*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2025) to Revision A (July 2026)	Page
• Corrected typographical error in the *Description*	1
• Corrected typographical error in	13
• Corrected typographical error in Figure 8-1	15
• Corrected typographical error in Figure 9-1	25

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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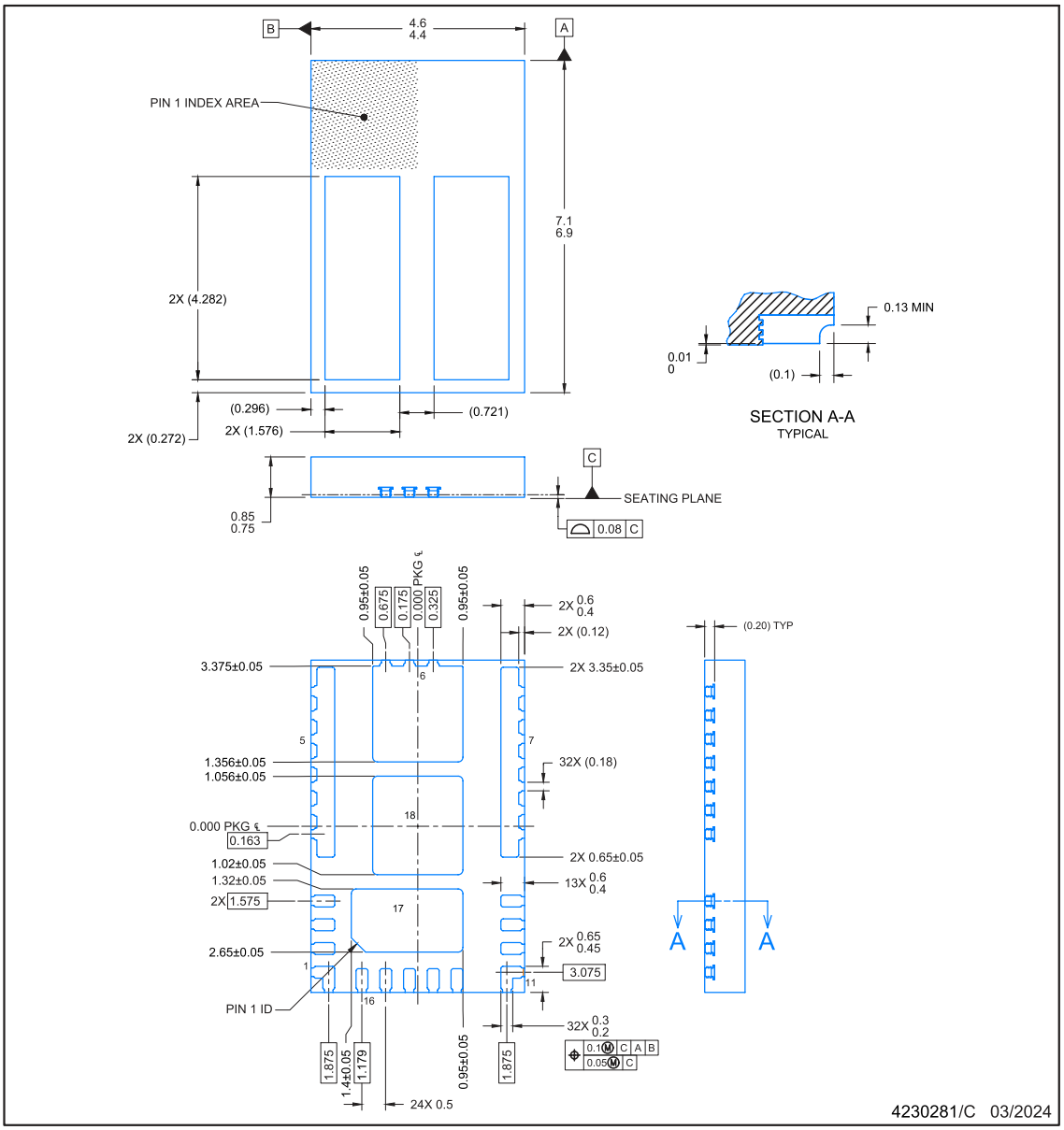
12.1 Package Information

12.1.1 Mechanical Data

PACKAGE OUTLINE

VBN0018A — **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

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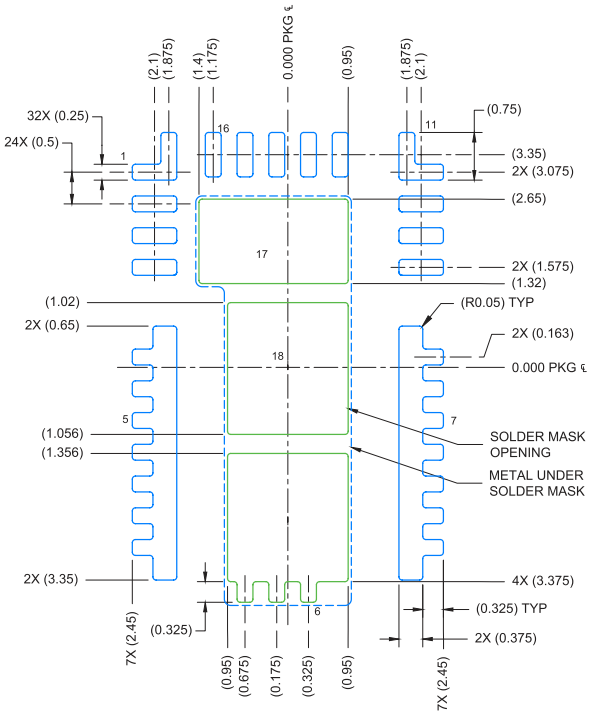
EXAMPLE BOARD LAYOUT

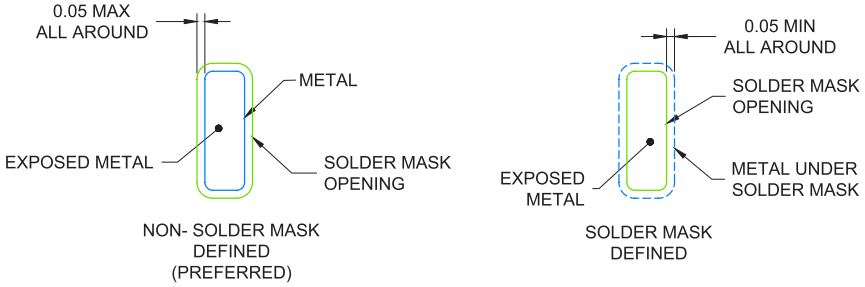
VBN0018A

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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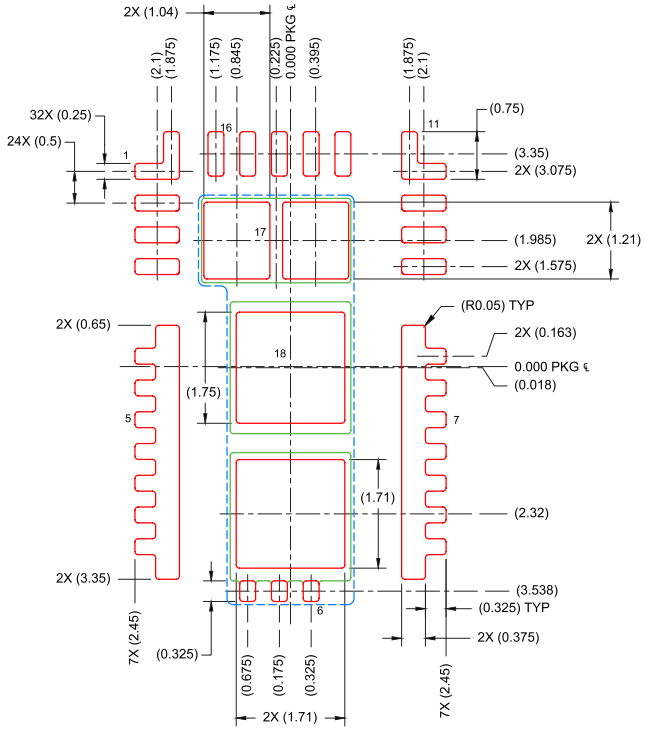
EXAMPLE STENCIL DESIGN

VBN0018A

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 6: 78%
PAD 17: 81%
PAD 18: 76%

4230281/C 03/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PDRV7167AVBNR	Active	Preproduction	VQFN-FCRLF (VBN) | 18	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

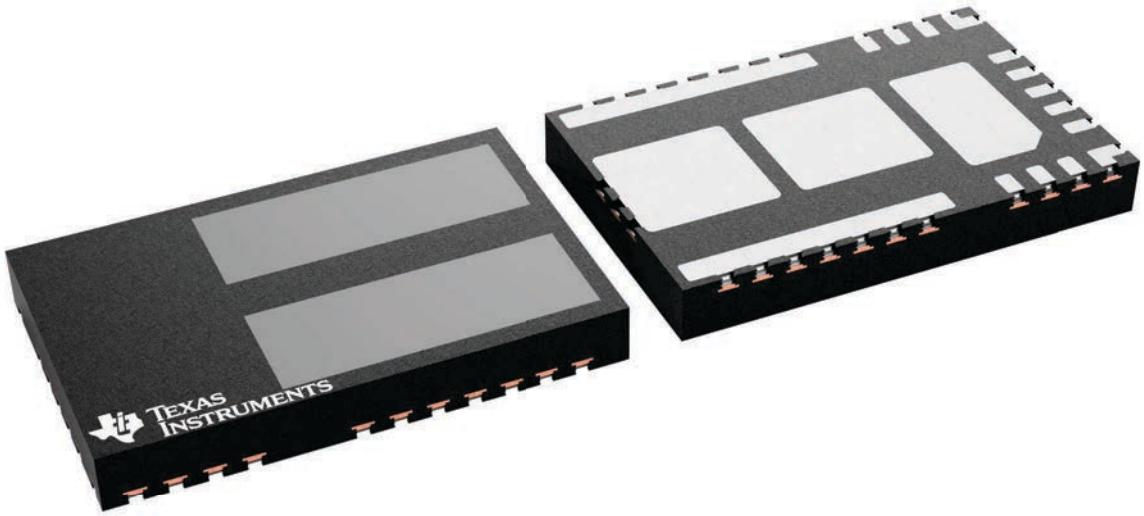
VBN 18

VQFN-FCRLF - 0.85 mm max height

4.5 x 7, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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