DirectPath™, Pop-Free 3Vrms Line Driver with Adjustable Gain

Check for Samples: DRV602

FEATURES

- **DirectPath™**
  - **Eliminates Pop/Clicks**
  - **Eliminates Output DC-Blocking Capacitors**
  - **Provides Flat Frequency Response 20Hz–20kHz**
- **Low Noise and THD**
  - **SNR > 102 dB**
  - **Typical V_N < 15 μVms**
  - **THD+N < 0.05% 20 Hz–20 kHz**
- **Output Voltage into 2.5-kΩ Load**
  - **2 Vrms with 3.3-V Supply Voltage**
  - **3 Vrms with 5-V Supply Voltage**
- **3Vrms Output Voltage into 2.5 kΩ Load With 5V Supply Voltage**
- **Differential Input**

APPLICATIONS

- **Set-Top Boxes**
- **PDP / LCD TV**
- **Blu-ray Disc™, DVD-Players**
- **Home Theater in a Box**

DESCRIPTION

The DRV602PW is a 3Vrms pop-free stereo line driver designed to allow the removal of the output dc-blocking capacitors for reduced component count and cost. The device is ideal for single supply electronics where size and cost are critical design parameters.

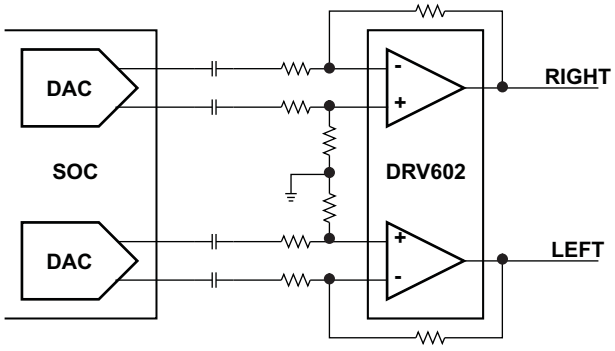
Designed using TI's patented DirectPath™ technology, the DRV602 is capable of driving 3Vrms into a 2.5kΩ load with 5V supply voltage. The device has differential inputs and uses external gain setting resistors, that supports a gain range of ±1V/V to ±10V/V. The use of external gain resistors also allows the implementation of a 2nd order low pass filter to compliment DAC's and SOC converters. The line output of the DRV602 has ±8kV IEC ESD protection. The DRV602 (referred to as the '602) has built-in shutdown control for pop-free on/off control.

Using the DRV602 in audio products can reduce component count compared to traditional methods of generating a 3Vrms output. The DRV602 doesn't require a power supply greater than 5V to generate its $8.5V_{PP}$ output, nor does it require a split rail power supply. The DRV602 integrates its own charge pump to generate a negative supply rail that provides a clean, pop-free ground biased 3Vrms output.

The DRV602 is available in a 14 pin TSSOP package.

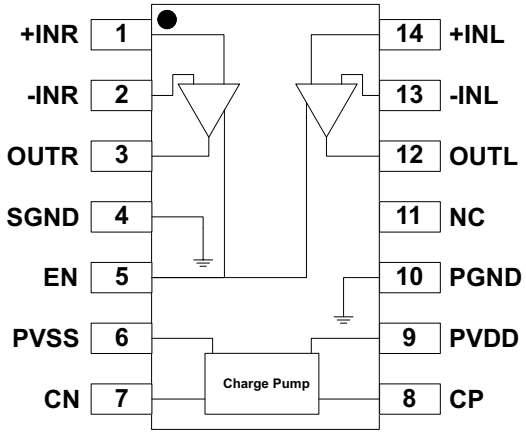
If higher SNR, trimmed DC-offset and external undervoltage-mute functions are beneficial in the application, TI recommends the footprint compatible DRV603 (SLOS617).

For a stereo line and stereo HP driver see DRV604 (SLOS659).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PW (TSSOP) PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O(1)	DESCRIPTION
NAME	TSSOP (PW)		
+INR	1	I	Right channel OPAMP positive input
–INR	2	I	Right channel OPAMP negative input
OUTR	3	O	Right channel OPAMP output
SGND	4	I	Signal ground
EN	5	I	Enable input, active high
PVSS	6	O	Supply voltage
CN	7	I/O	Charge pump flying capacitor negative terminal
CP	8	I/O	Charge pump flying capacitor positive terminal
PVDD	9	I	Positive supply
PGND	10	I	Power ground
NC	11		No internal connection
OUTL	12	O	Left channel OPAMP output
–INL	13	I	Left channel OPAMP negative input
+INL	14	I	Left channel OPAMP positive input

(1) I = input, O = output, P = power

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range

		VALUE	UNIT
	Supply voltage, VDD to GND	–0.3 V to 5.5	V
V_I	Input voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
R_L	Minimum load impedance	> 600	Ω
	EN to GND	–0.3 to V_{DD} +0.3	V
T_J	Maximum operating junction temperature range,	–40 to 150	°C
T_{stg}	Storage temperature range	–40 to 150	°C
ESD	IEC Contact ESD Protection per IEC6100-4-2, on output pins measured on DRV602EVM	±8	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represents the DC voltage + peak AC waveform measured at the terminal of the device in all conditions.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°/W)	θ_{JA} (°/W)	POWER RATING(1) AT $T_A \le 25°C$	POWER RATING(1) AT $T_A \le 70°C$
TSSOP-14 (PW)	35	115(2)	870mW	348mW

(1) Power rating is determined with a junction temperature of 125°C. This is the point where performance starts to degrade and long-term reliability starts to be reduced. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and reliability.
(2) These data were taken with the JEDEC High-K test printed circuit board (PCB). For the JEDEC low-K test PCB, the θ_{JA} is 185°C.

ORDERING INFORMATION

T_A	PACKAGE(1)	DESCRIPTION
-40°C to 85°C	DRV602PW	14-Pin TSSOP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage,	DC Supply Voltage	3	3.3	5.5	V
V_{IH}	High-level input voltage	EN		60		% of VDD
V_{IL}	Low-level input voltage	EN		40		% of VDD
T_A	Operating free-air temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

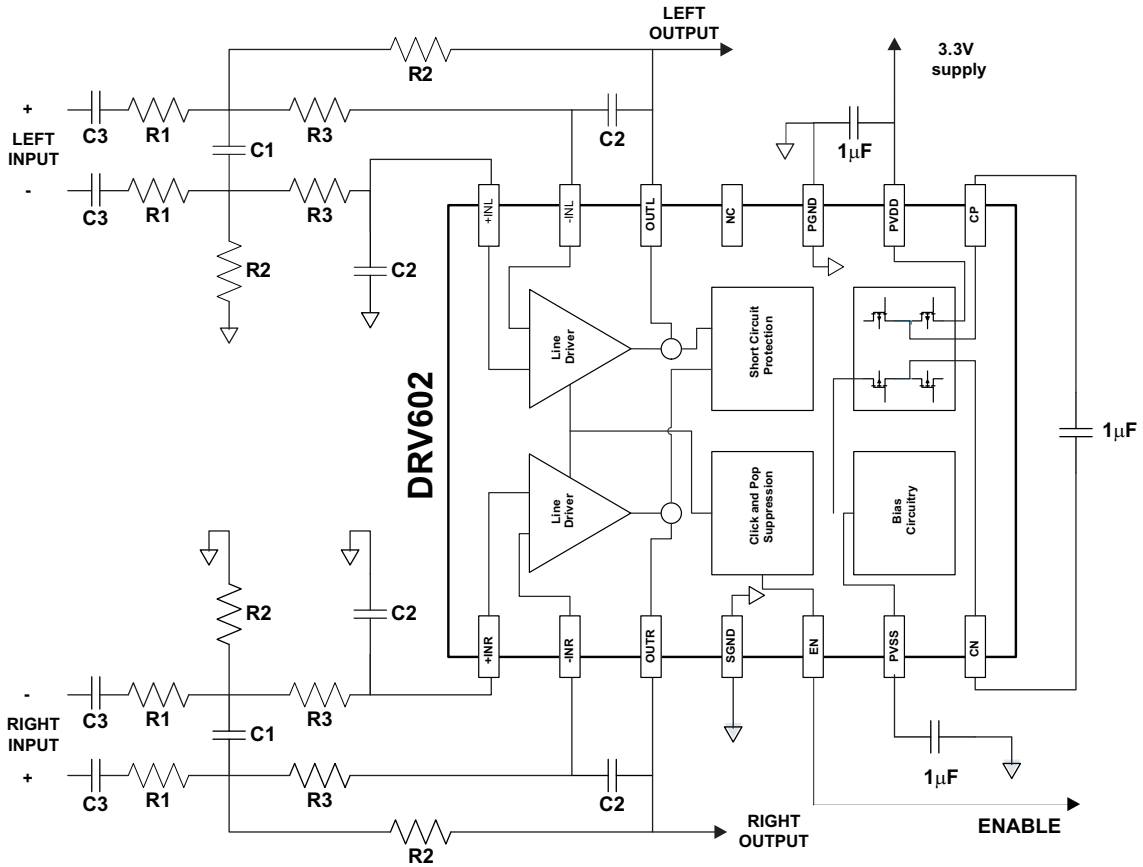
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage	V_{DD} = 3 V to 5 V, Voltage follower - gain = 1			5	mV
PSRR	Supply Rejection Ratio	V_{DD} = 3.3 V to 5 V		88		dB
V_{OH}	High-level output voltage	V_{DD} = 3.3 V, R_L = 2.5 kΩ	3.10			V
V_{OL}	Low-level output voltage	V_{DD} = 3.3 V, R_L = 2.5 kΩ			–3.05	V
$\|I_{IH}\|$	High-level input current (EN)	V_{DD} = 5 V, V_I = V_{DD}			1	µA
$\|I_{IL}\|$	Low-level input current (EN)	V_{DD} = 5 V, V_I = 0 V			1	µA
I_{DD}	Supply Current	V_{DD} = 3.3 V, No load, EN = V_{DD}	8	11		mA
		V_{DD} = 5 V, No load, EN = V_{DD}		12.5	20	
		Shutdown mode, Vdd = 3 V to 5 V			2	mA

OPERATING CHARACTERISTICS

V_{DD} = 3.3 V , T_A = 25°C, R_L = 2.5kΩ, $C_{(PUMP)}$ = $C_{(PVSS)}$ = 1 µF , C_{IN} = 1 µF, R_{IN} = 33 kΩ, R_{fb} = 68kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output Voltage (Outputs In Phase)	THD = 1%, V_{DD} = 3.3 V, f = 1 kHz		2.05		Vrms
		THD = 1%, V_{DD} = 5 V, f = 1 kHz		3.01		
THD+N	Total harmonic distortion plus noise	V_O = 2 Vrms, f = 1 kHz V_O = 2 Vrms, f = 6.8 kHz		0.01% 0.05%		
	Crosstalk	V_O = 2 Vrms, f = 1 kHz		–100		dB
I_O	Output current limit	V_{DD} = 3.3 V		20		mA
R_{IN}	Input resistor range		1	10	47	kΩ
R_{fb}	Feedback resistor range		4.7	20	100	kΩ
	Slew rate			4.5		V/µs
	Maximum capacitive load			220		pF
V_N	Noise output voltage	A-weighted, BW 20Hz–22kHz		15		µVrms
SNR	Signal to noise ratio	V_O = 2 Vrms, THD+N = 0.1%, 22 kHz BW, A-weighted		102		dB
G_{BW}	Unity Gain Bandwidth			8		MHz
A_{VO}	Open-loop voltage gain			150		dB
Fcp	Charge Pump frequency		225	450	675	kHz

APPLICATION CIRCUIT



R1 = 33kΩ, R2 = 68kΩ, R3 = 100kΩ, C1 = 150pF, C2 = 15pF, C3 = 1 µF

Differential input, single ended output, 2nd order filter. 40kHz –3dB frequency, Gain 2.06.

TYPICAL CHARACTERISTICS

V_{DD} = 3.3V , T_A = 25°C, $C_{(PUMP)}$ = $C_{(PVSS)}$ = 1 µF , C_{IN} = 1 µF, R_{IN} = 33 kΩ, R_{fb} = 68 kΩ, R_L = 2.5 kΩ (unless otherwise noted)

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE

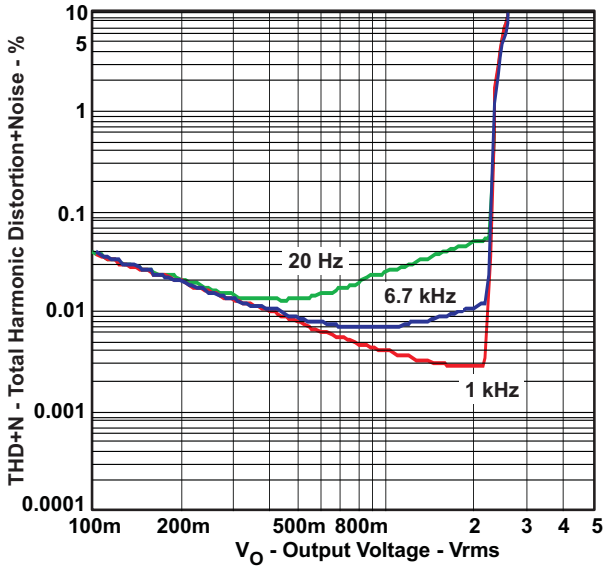


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

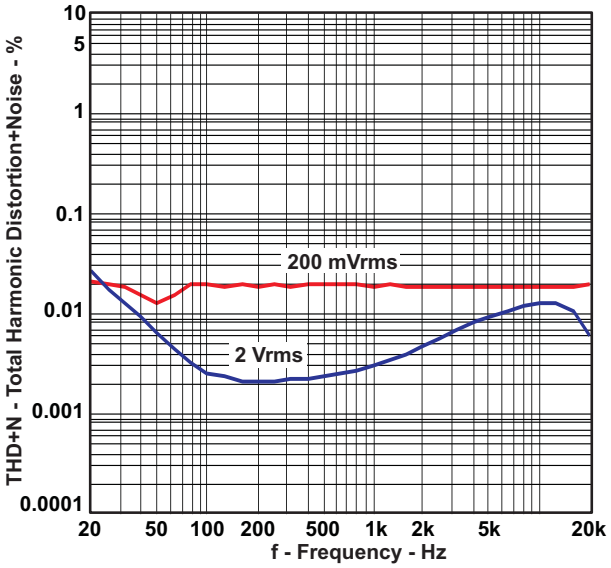


Figure 2.

FFT vs FREQUENCY

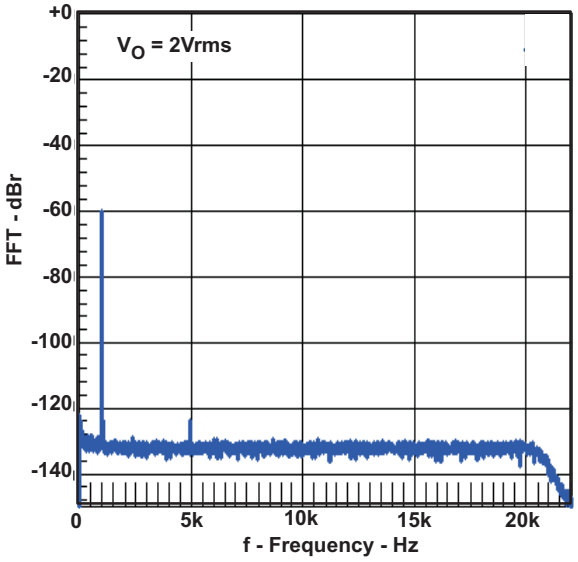


Figure 3.

QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

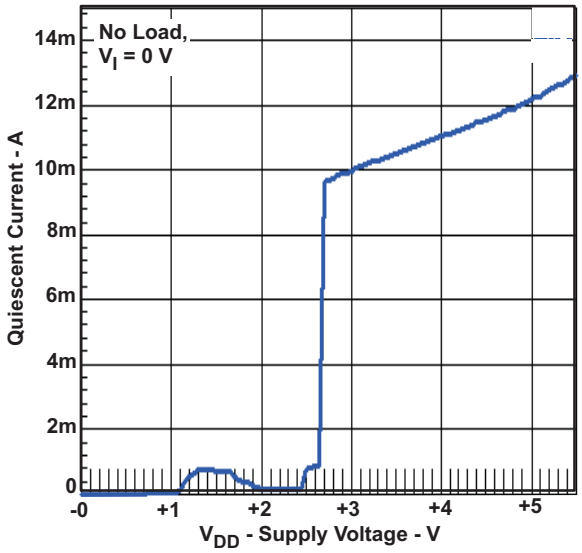


Figure 4.

APPLICATION INFORMATION

Line Driver Amplifiers

Single-supply line driver amplifiers typically require dc-blocking capacitors. The top drawing in Figure 5 illustrates the conventional line driver amplifier connection to the load and output signal.

DC blocking capacitors are often large in value, and a mute circuit is needed during power up to minimize click & pop. The output capacitor and mute circuit consume PCB area and increase cost of assembly, and can reduce the fidelity of the audio output signal.

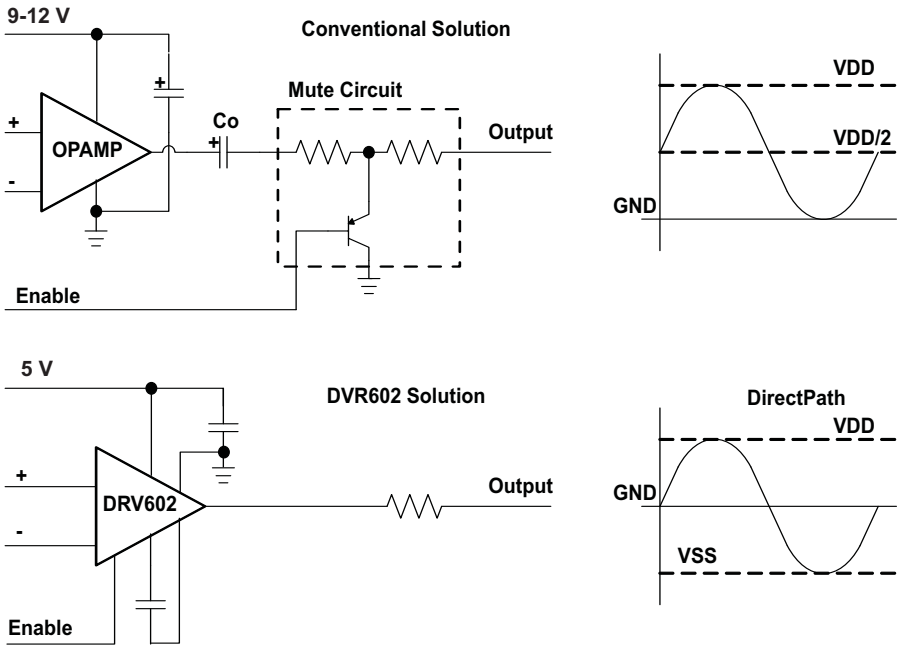


Figure 5. Conventional and DirectPath Line Driver

The DirectPath™ amplifier architecture operates from a single supply, but makes use of an internal charge pump to provide a negative voltage rail.

Combining the user provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode.

The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. The DirectPath amplifier requires no output dc blocking capacitors.

The bottom block diagram and waveform of Figure 5 illustrate the ground-referenced Line Driver architecture. This is the architecture of the DRV602.

Charge Pump Flying Capacitor and PVSS Capacitor

The charge pump flying capacitor, C_{PUMP}, serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1µF is typical. Capacitor values that are smaller than 1µF can be used, but the maximum output voltage may be reduced and the device may not operate to specifications.

Decoupling Capacitors

The DRV602 is a DirectPath Line Driver amplifier that require adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1µF, placed as close as possible to the device PV_{DD} lead works best. Placing this decoupling capacitor close to the DRV602 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Gain setting resistors ranges

The gain setting resistors, R_{IN} and R_{fb}, must be chosen so that noise, stability and input capacitor size of the DRV602 is kept within acceptable limits. Voltage gain is defined as R_{fb} divided by R_{IN}.

Selecting values that are too low demands a large input ac-coupling capacitor, C_{IN} . Selecting values that are too high increases the noise of the amplifier. Table 1 lists the recommended resistor values for different gain settings.

Table 1. Recommended Resistor Values

INPUT RESISTOR VALUE, R_{IN}	FEEDBACK RESISTOR VALUE, R_{fb}	DIFFERENTIAL INPUT GAIN	INVERTING INPUT GAIN	NON INVERTING INPUT GAIN
22 kΩ	22 kΩ	1.0 V/V	–1.0 V/V	2.0 V/V
15 kΩ	30 kΩ	1.5 V/V	–1.5 V/V	2.5 V/V
33 kΩ	68 kΩ	2.1 V/V	–2.1 V/V	3.1 V/V
10 kΩ	100 kΩ	10.0 V/V	–10.0 V/V	11.0 V/V

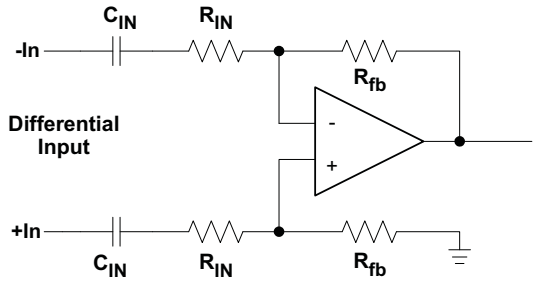


Figure 6. Differential Input

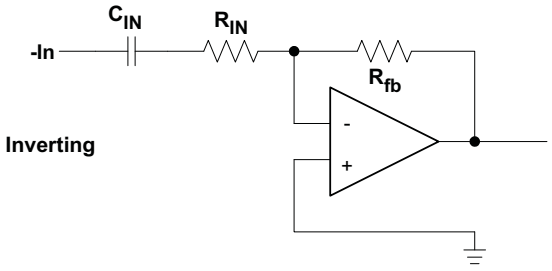


Figure 7. Inverting

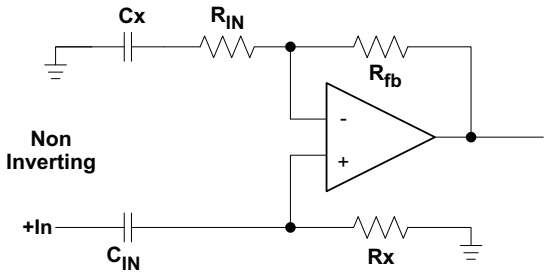


Figure 8. Non-Inverting

Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the DRV602. These capacitors block the DC portion of the audio source and allow the DRV602 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the DC gain to 1, limiting the DC-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 1, then the frequency and/or capacitance can be determined when one of the two values are given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}} \tag{1}$$

Using the DRV602 as 2nd Order Filter

Several audio DACs used today require an external low-pass filter to remove out of band noise. This is possible with the DRV602 as it can be used like a standard OPAMP.

Several filter topologies can be implemented both single ended and differential. In Figure 9, a Multi FeedBack - MFB, with differential input and single ended input is shown.

An ac-coupling capacitor to remove dc-content from the source is shown, it serves to block any dc content from the source and lowers the dc-gain to 1 helping reducing the output dc-offset to minimum.

The component values can be calculated with the help of the TI FilterPro™ program available on the TI website at: http://focus.ti.com/docs/toolsw/folders/print/filterpro.html

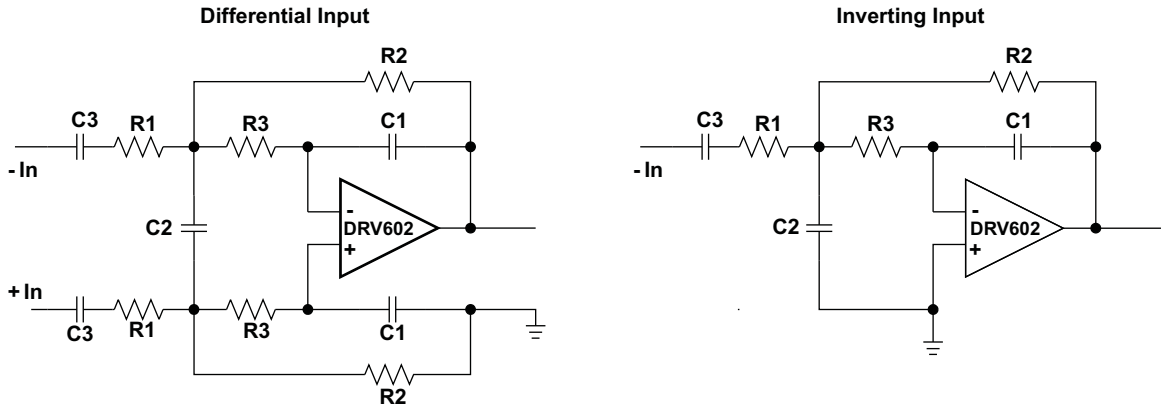


Figure 9. 2nd Order Active Low Pass Filter

The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small size ac-coupling cap. With the proposed values, 33k, 68k, 100k, a DNR of 102dB can be achieved with a small 1μF input ac-coupling capacitor.

Pop-Free Power Up

Pop-free power up is ensured by keeping the EN (enable pin) low during power supply ramp up and down. The EN pin should be kept low until the input ac-coupling capacitors are fully charged before asserting the EN pin high; this way, proper precharge of the ac-coupling is performed, and pop-free power-up is achieved. Figure 10 illustrates the preferred sequence.

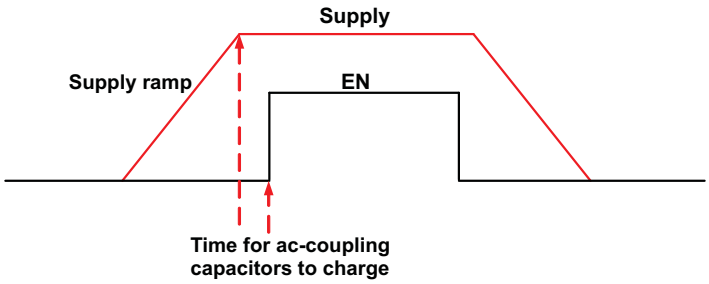


Figure 10. Power-Up Sequence

Capacitive Load

The DRV602 has the ability to drive a high capacitive load up to 220pF directly, higher capacitive loads can be accepted by adding a series resistor of 10Ω or larger.

Layout Recommendations

A proposed layout for the DRV602 can be seen in the DRV602EVM user's guide (SLOU248) and the Gerber files can be downloaded on www.ti.com, open the DRV602 product folder and look in the Tools and Software folder.

The gain setting resistors, R_{IN} and R_{fb} , must be placed close to the input pins to minimize the capacitive loading on these input pins and to ensure maximum stability of the DRV602. For the recommended PCB layout, see the DRV602EVM user's guide.

REVISION HISTORY

NOTE: Page numbers of current version may differ from previous versions.

Changes from Revision A (December 2008) to Revision B **Page**

- Changed crosstalk spec from -80dB to -100dB 4

Changes from Revision B (October 2009) to Revision C **Page**

- Added "Pop-Free" to title and changed "pop-less" to "pop-free in description text strings. 1
- Added Output Voltage Feature bullet: "3Vrms With 5-V Supply Voltage" 1
- Changed "2Vrms" to "3Vrms" in Description Section 1
- Changed "$5V_{PP}$" to "$8.5V_{PP}$" in Description Section 1
- Changed Recommended Operating Conditions T_A range from "0 to 70 °C" to "–40 to 85°C" 3
- Changed Electrical Characteristics Test Conditions V_{DD} from "4.5 V" to "5 V" 3
- Added "V_O" spec. for "V_{DD} = 5 V" to Operating Characteristics table 4

Changes from Revision May 2010 (C) to Revision D **Page**

- Changed Abs Max Table (T_J) From: -40°C to 85°C to -40°C to 150 3
- Changed RIGHT INPUT From: + / - To: - / + in the Application Circuit 4
- Added R_L = 2.5 kΩ to the TYPICAL CHARACTERISTICS conditions statement 5
- Added , C_{PUMP}, to the first sentence of the Charge Pump Flying Capacitor and PVSS Capacitor section 7
- Changed V_{DD} To: PV_{DD} in Decoupling Capacitors section 7
- Changed SD (shutdown pin) to EN (enable pin) in the Pop-Free Power Up section 9
- Deleted last sentence in the Capacitive Load section 9

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV602PW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV602
DRV602PW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV602
DRV602PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV602
DRV602PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV602
DRV602PWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV602

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

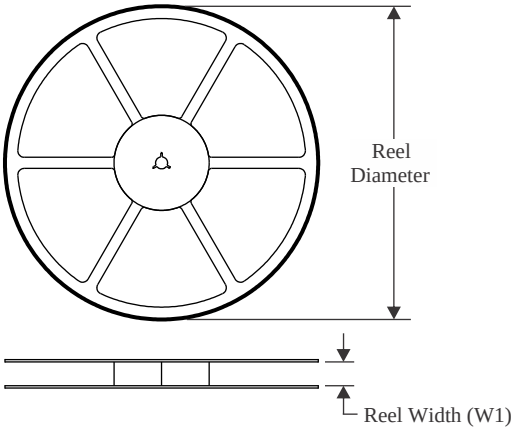
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

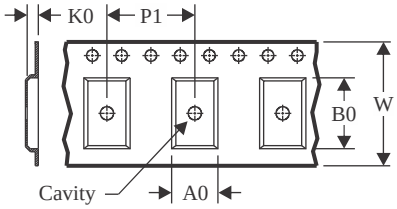
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

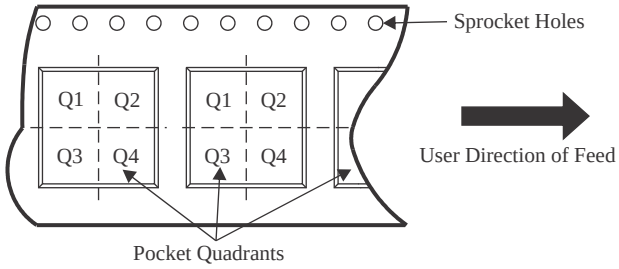


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

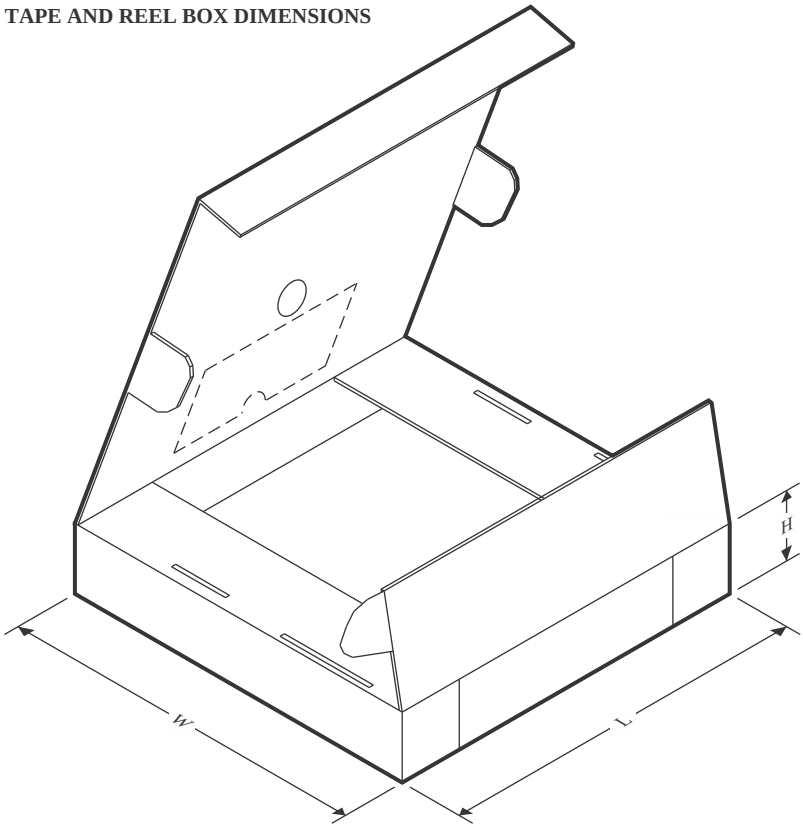
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV602PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

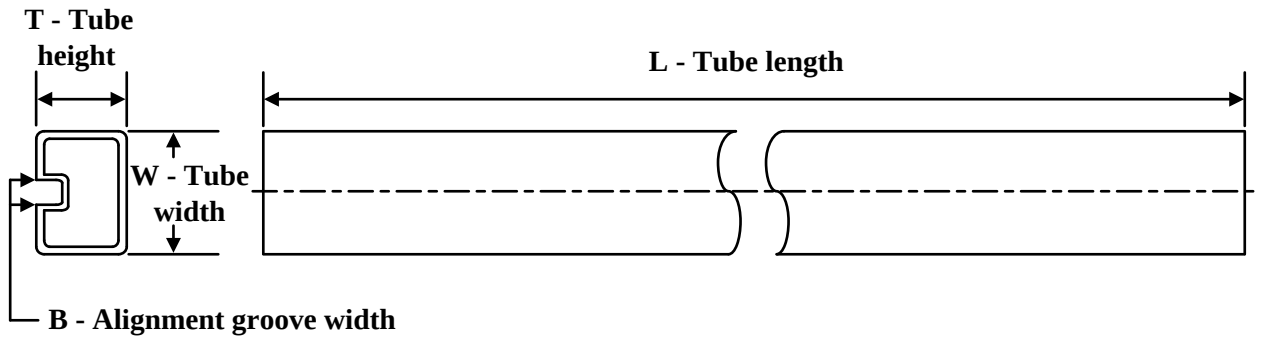
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV602PWR	TSSOP	PW	14	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

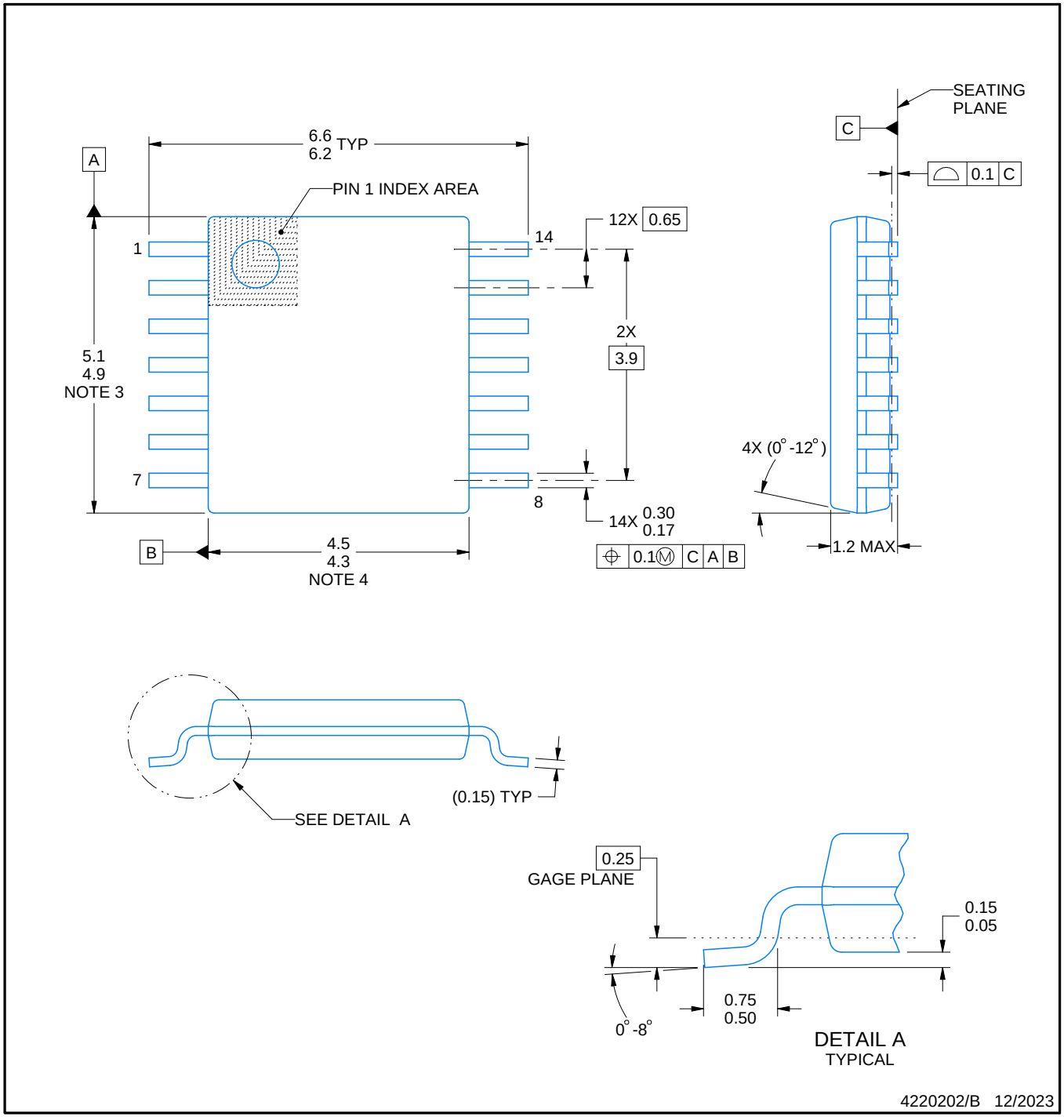
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV602PW	PW	TSSOP	14	90	530	10.2	3600	3.5
DRV602PW.B	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0014A

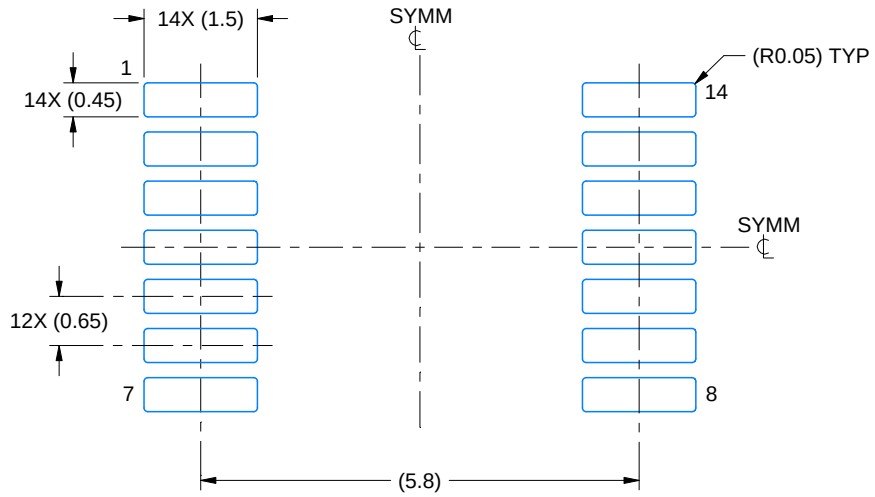
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

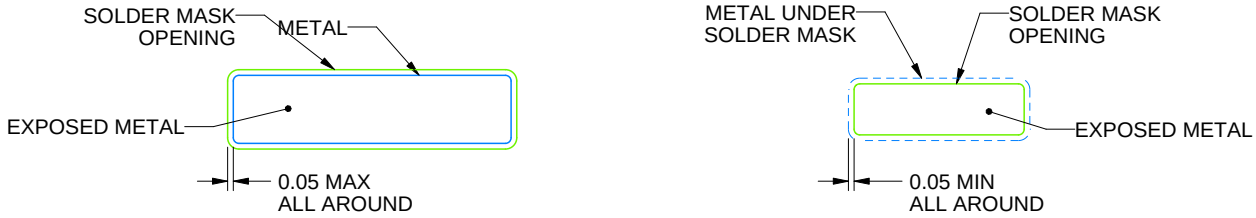


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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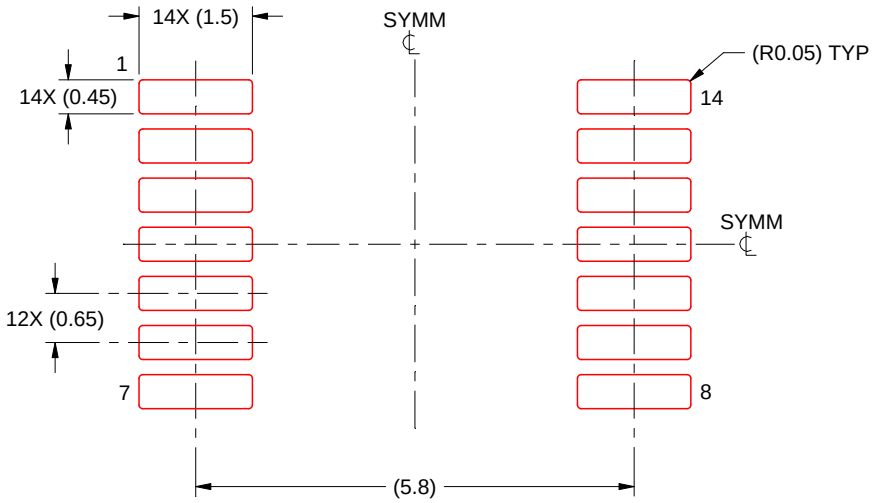
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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