

CSD18534KCS 60V N-Channel NexFET™ Power MOSFET

1 Features

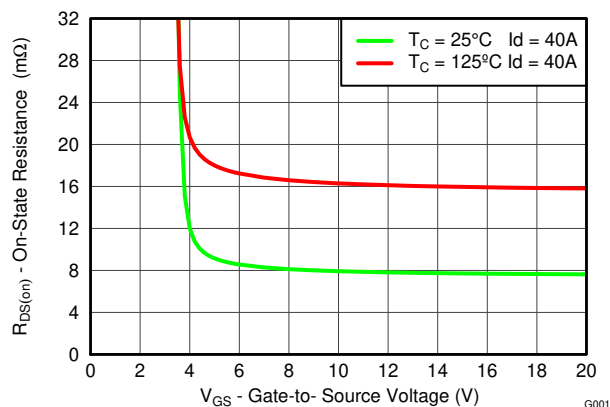
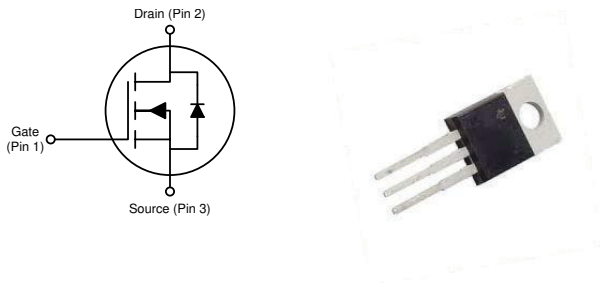
- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Logic level
- Pb-Free terminal plating
- RoHS compliant
- Halogen free
- TO-220 plastic package

2 Applications

- DC-DC conversion
- Secondary side synchronous rectifier
- Motor control

3 Description

This 7.6m Ω , 60V TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



$R_{DS(on)}$ vs V_{GS}

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
Q_g	Gate Charge Total (10V)	19	nC
Q_{gd}	Gate Charge Gate-to-Drain	3.1	nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{V}$	10.2 m Ω
		$V_{GS} = 10\text{V}$	7.6 m Ω
$V_{GS(th)}$	Threshold Voltage	1.9	V

Ordering Information⁽¹⁾

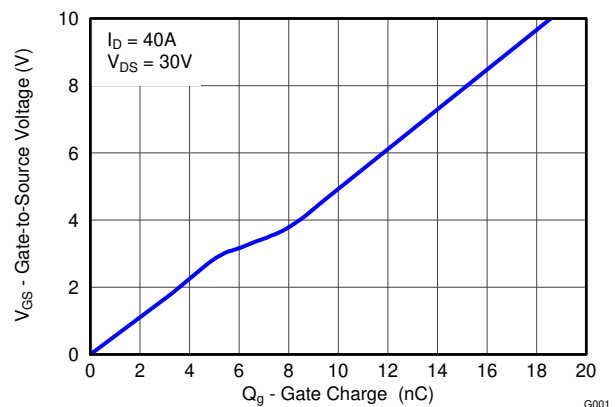
Device	Package	Media	Qty	Ship
CSD18534KCS	TO-220 Plastic Package	Tube	50	Tube

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current (Package limited)	100	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	73	
	Continuous Drain Current (Silicon limited), $T_C = 100^\circ\text{C}$	52	
I_{DM}	Pulsed Drain Current ⁽¹⁾	164	A
P_D	Power Dissipation	107	W
T_J , T_{stg}	Operating Junction and Storage Temperature Range	-55 to 175	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 38\text{A}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$	72	mJ

- (1) Max $R_{\theta JC} = 1.3^\circ\text{C/W}$, pulse duration $\leq 100\mu\text{s}$, duty cycle $\leq 1\%$



Gate Charge



Table of Contents

1 Features	1	5.1 Third-Party Products Disclaimer.....	7
2 Applications	1	5.2 Receiving Notification of Documentation Updates.....	7
3 Description	1	5.3 Support Resources.....	7
4 Specifications	3	5.4 Trademarks.....	7
4.1 Electrical Characteristics.....	3	5.5 Electrostatic Discharge Caution.....	7
4.2 Thermal Information.....	3	5.6 Glossary.....	7
4.3 Typical MOSFET Characteristics.....	4	6 Revision History	8
5 Device and Documentation Support	7	7 Mechanical, Packaging, and Orderable Information	9

4 Specifications

4.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
STATIC CHARACTERISTICS							
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0V, I _D = 250μA	60			V	
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0V, V _{DS} = 48V	1			μA	
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0V, V _{GS} = 20V	100			nA	
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1.5	1.9	2.3	V	
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 4.5V, I _D = 40A	10.2			13.3	mΩ
		V _{GS} = 10V, I _D = 40A	7.6			9.5	mΩ
g _{fs}	Transconductance	V _{DS} = 30V, I _D = 40A	100			S	
DYNAMIC CHARACTERISTICS							
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 30V, f = 1MHz	1500			1880	pF
C _{oss}	Output Capacitance		164			205	pF
C _{rss}	Reverse Transfer Capacitance		5.0			6.5	pF
R _G	Series Gate Resistance		1.5			3.0	Ω
Q _g	Gate Charge Total (4.5V)	V _{DS} = 30V, I _D = 40A	9.3			12	nC
Q _g	Gate Charge Total (10V)		19			24	nC
Q _{gd}	Gate Charge Gate-to-Drain		3.1				nC
Q _{gs}	Gate Charge Gate-to-Source		4.8				nC
Q _{g(th)}	Gate Charge at V _{th}		3.3				nC
Q _{oss}	Output Charge		18				nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 30V, V _{GS} = 10V, I _{DS} = 40A, R _G = 0Ω	4.2				ns
t _r	Rise Time		4.8				ns
t _{d(off)}	Turn Off Delay Time		10.4				ns
t _f	Fall Time		2.4				ns
DIODE CHARACTERISTICS							
V _{SD}	Diode Forward Voltage	I _{SD} = 40A, V _{GS} = 0V	0.8			1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 30V, I _F = 40A, di/dt = 300A/μs	68				nC
t _{rr}	Reverse Recovery Time		49				ns

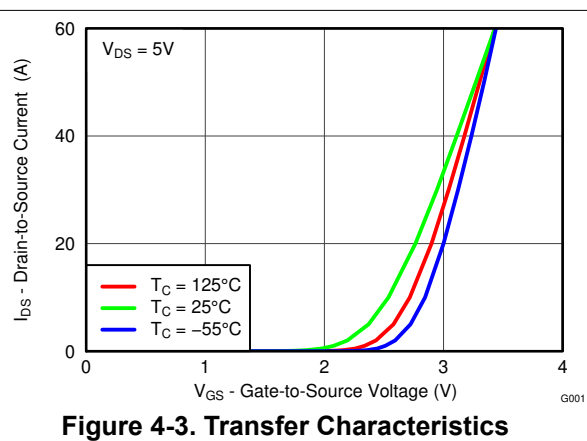
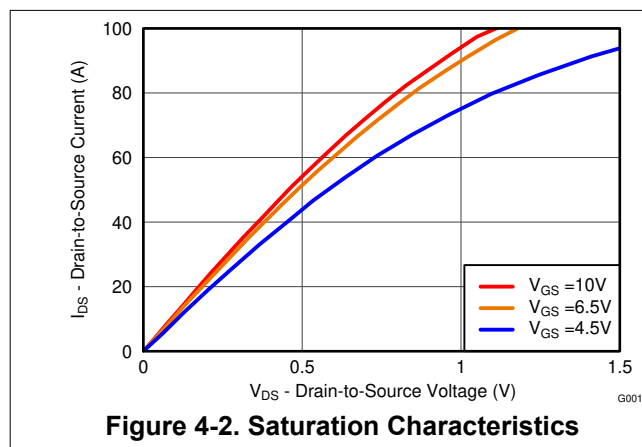
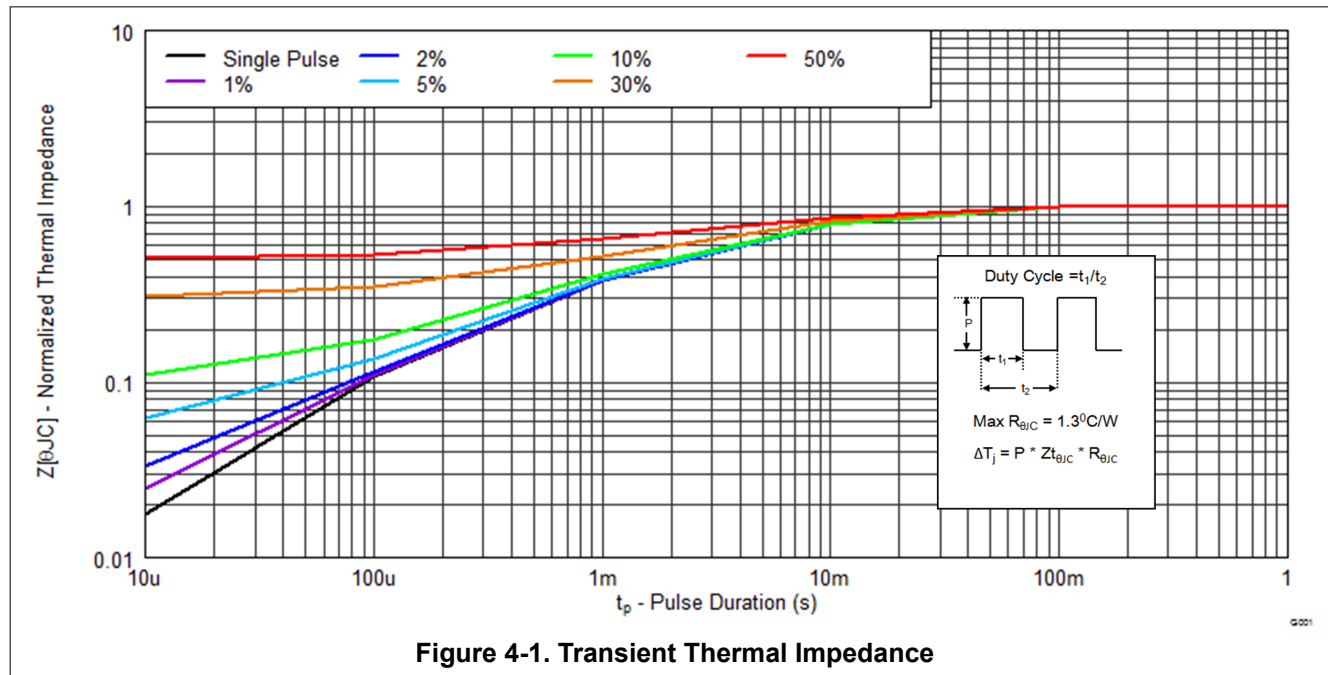
4.2 Thermal Information

$T_A = 25^\circ\text{C}$ unless otherwise stated

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance			1.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance			62	

4.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$, unless otherwise stated



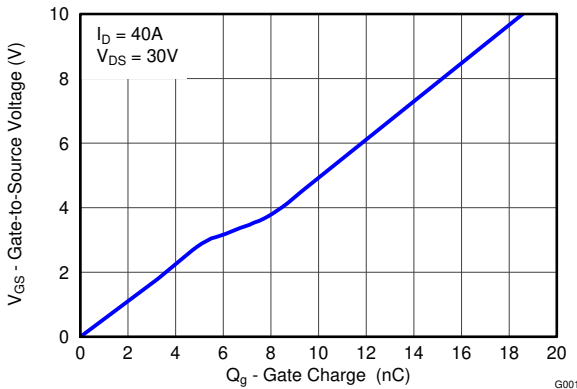


Figure 4-4. Gate Charge

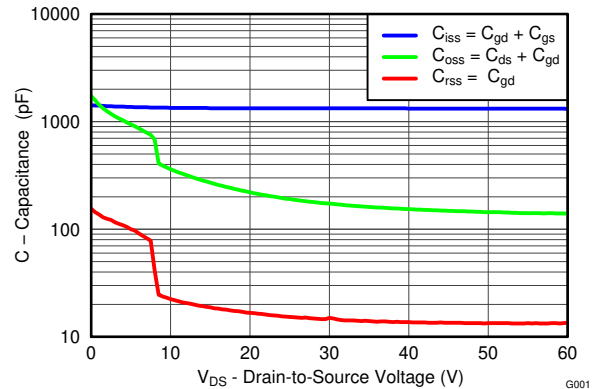


Figure 4-5. Capacitance

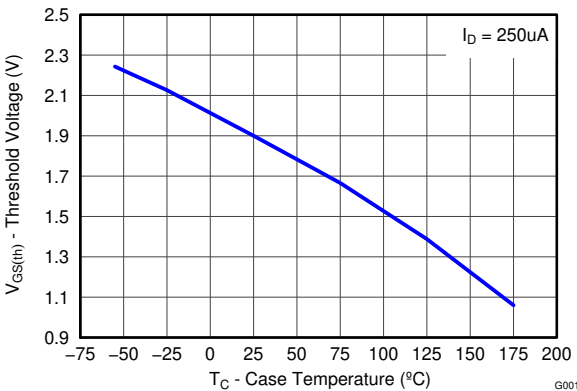


Figure 4-6. Threshold Voltage vs Temperature

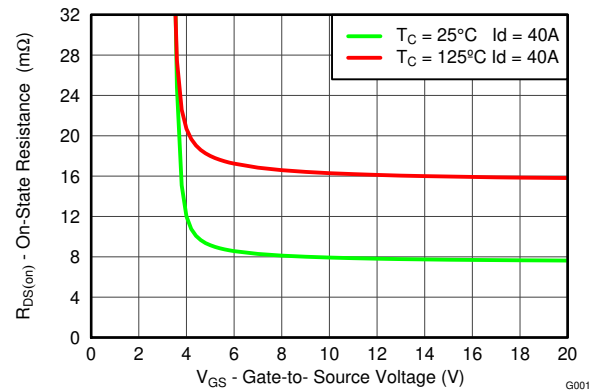


Figure 4-7. On-State Resistance vs Gate-to-Source Voltage

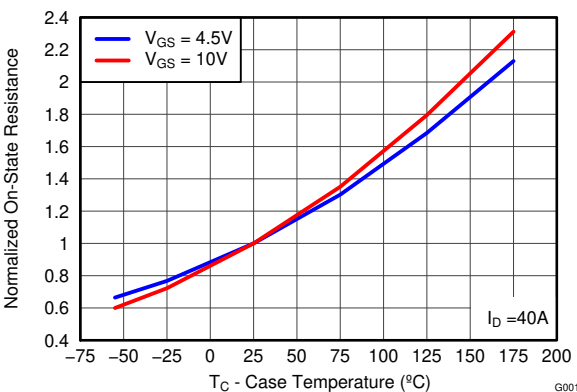


Figure 4-8. Normalized On-State Resistance vs Temperature

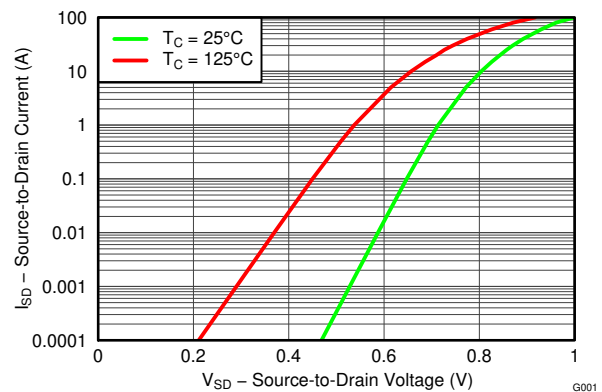


Figure 4-9. Typical Diode Forward Voltage

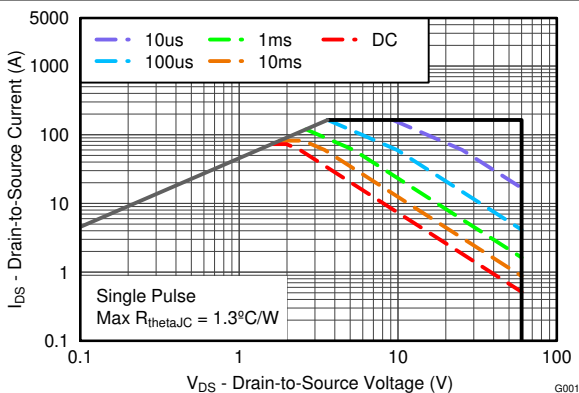


Figure 4-10. Maximum Safe Operating Area

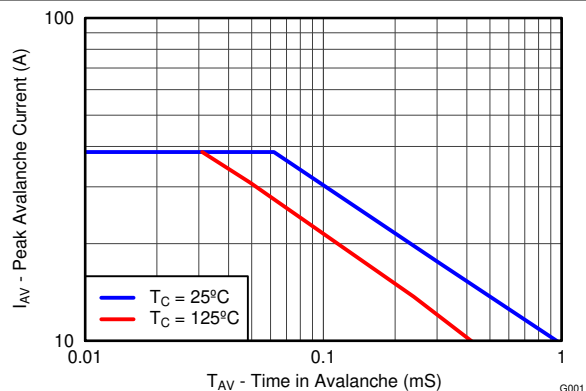


Figure 4-11. Single Pulse Unclamped Inductive Switching

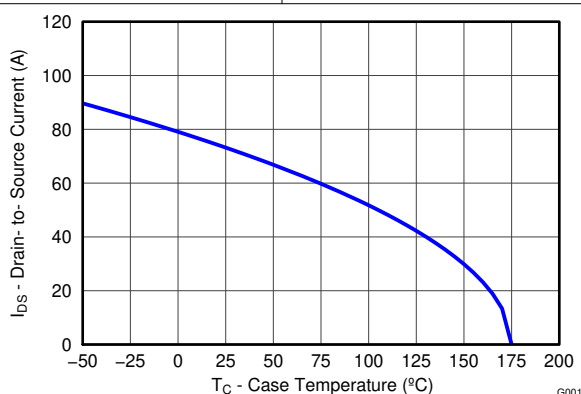


Figure 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

5.4 Trademarks

NexFET™ is a trademark of Texas Instruments.

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

5.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

Changes from Revision B (October 2014) to Revision C (March 2024) Page

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1

Changes from Revision A (April 2014) to Revision B (October 2014) Page

- Increased I_{DM} to 164 A 1
- Updated pulsed current conditions 1
- Updated [Figure 4-1](#) from a normalized $R_{\theta JA}$ to a normalized $R_{\theta JC}$ curve 4
- Updated the SOA in [Figure 4-10](#) 4

Changes from Revision A (April 2014) to Revision B (October 2014) Page

- Increased I_{DM} to 164 A 1
- Updated pulsed current conditions 1
- Updated [Figure 4-1](#) from a normalized $R_{\theta JA}$ to a normalized $R_{\theta JC}$ curve 4
- Updated the SOA in [Figure 4-10](#) 4

Changes from Revision * (September 2012) to Revision A (April 2014) Page

- Updated document title 1
- Updated description 1
- Adjusted currents to reflect higher temperature capability in Absolute Maximum Ratings..... 1
- Adjusted max power to reflect higher temperature capability in Absolute Maximum Ratings..... 1
- Increased maximum temperature to 175°C in Absolute Maximum Ratings..... 1
- Updated [Figure 4-6](#) to extend to 175°C 4
- Updated [Figure 4-8](#) to extend to 175°C 4
- Updated [Figure 4-12](#) to extend to 175°C 4

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD18534KCS	Active	Production	TO-220 (KCS) 3	50 TUBE	ROHS Exempt	SN	N/A for Pkg Type	-55 to 175	CSD18534KCS
CSD18534KCS.B	Active	Production	TO-220 (KCS) 3	50 TUBE	ROHS Exempt	SN	N/A for Pkg Type	-55 to 175	CSD18534KCS

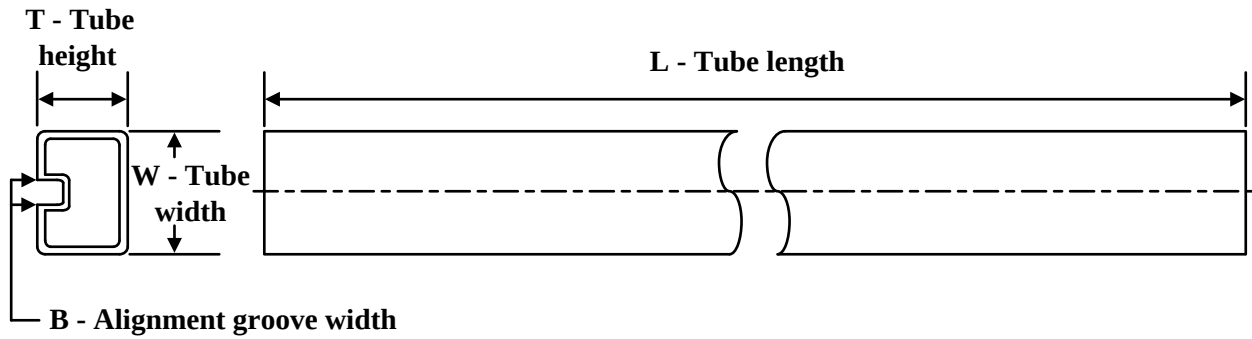
- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

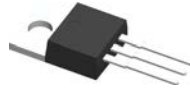
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CSD18534KCS	KCS	TO-220	3	50	532	34.1	700	9.6
CSD18534KCS.B	KCS	TO-220	3	50	532	34.1	700	9.6

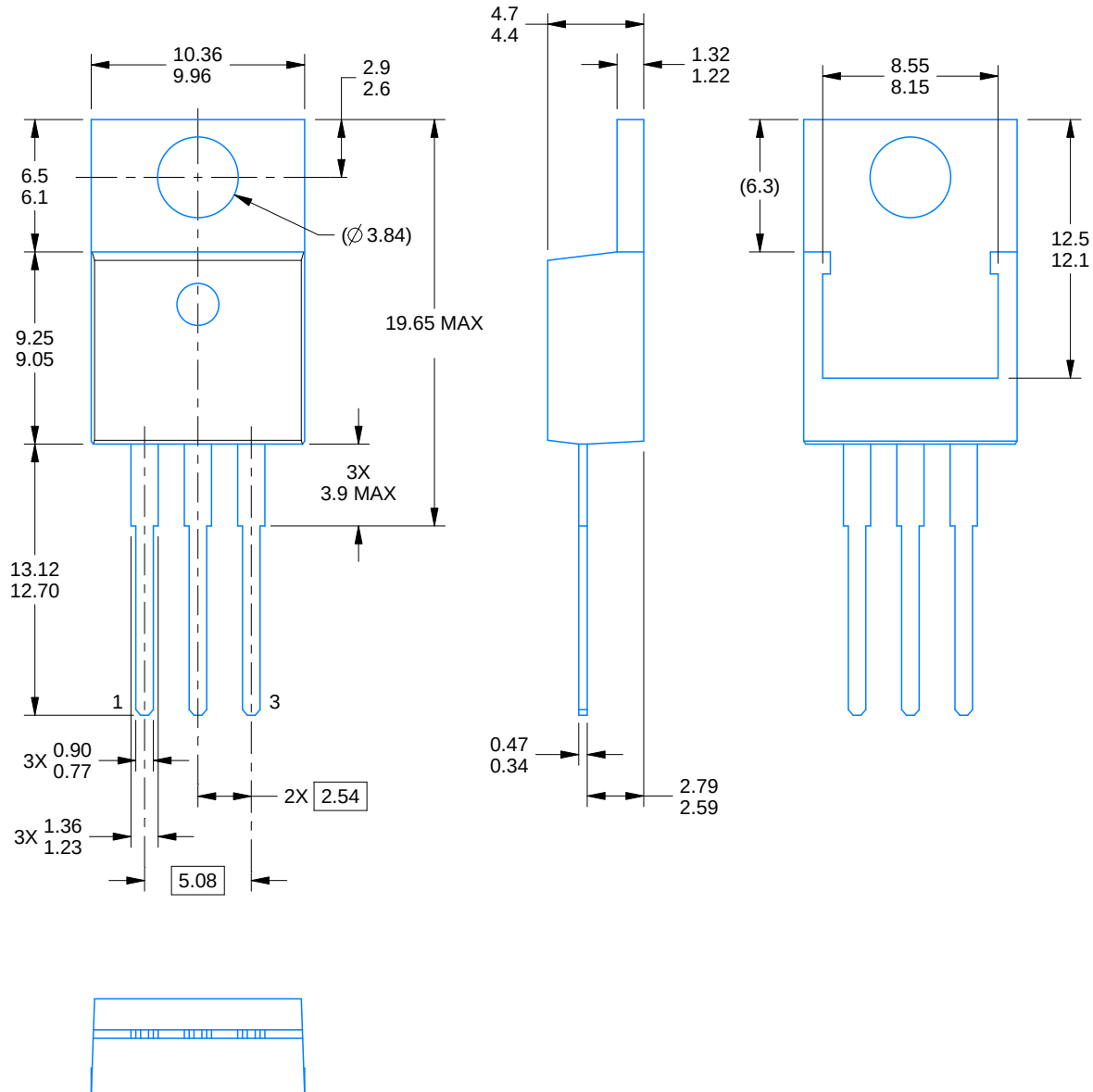


PACKAGE OUTLINE

KCS0003B

TO-220 - 19.65 mm max height

TO-220



4222214/B 08/2018

NOTES:

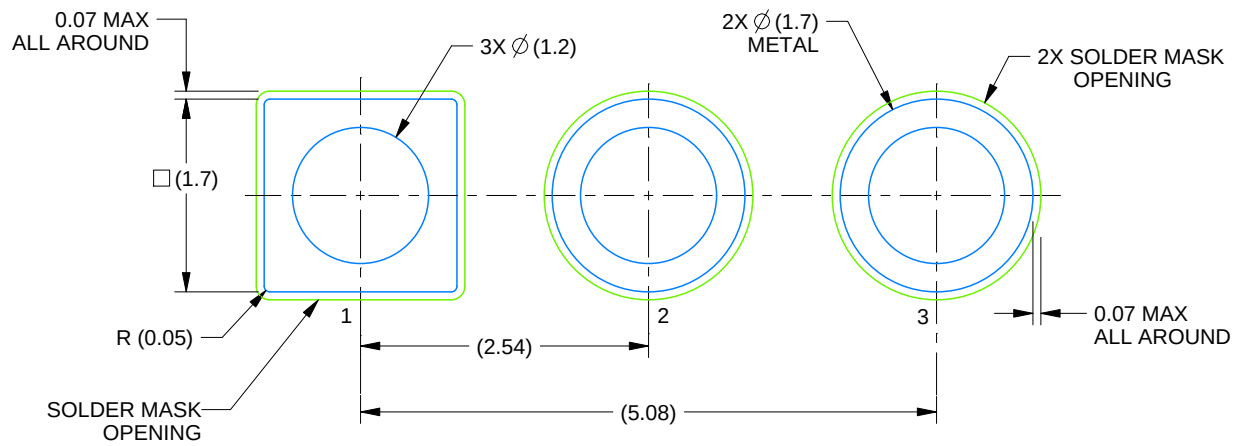
1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.

EXAMPLE BOARD LAYOUT

KCS0003B

TO-220 - 19.65 mm max height

TO-220



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B 08/2018

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025