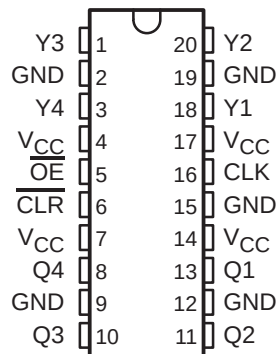


# CDC337 CLOCK DRIVER WITH 3-STATE OUTPUTS

SCAS330B – DECEMBER 1990 – REVISED OCTOBER 1998

- Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications
- TTL-Compatible Inputs and CMOS-Compatible Outputs
- Distributes One Clock Input to Eight Outputs
  - Four Same-Frequency Outputs
  - Four Half-Frequency Outputs
- Distributed  $V_{CC}$  and Ground Pins Reduce Switching Noise
- High-Drive Outputs ( $-48\text{-mA } I_{OH}$ ,  $48\text{-mA } I_{OL}$ )
- State-of-the-Art *EPIC-II B*<sup>™</sup> BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline (DW)

DW PACKAGE  
(TOP VIEW)



## description

The CDC337 is a high-performance, low-skew clock driver. It is specifically designed for applications requiring synchronized output signals at both the clock frequency and one-half the clock frequency. The four Y outputs switch in phase and at the same frequency as the clock (CLK) input. The four Q outputs switch at one-half the frequency of CLK.

When the output-enable ( $\overline{OE}$ ) input is low and the clear ( $\overline{CLR}$ ) input is high, the Y outputs follow CLK and the Q outputs toggle on low-to-high transitions at CLK. Taking  $\overline{CLR}$  low asynchronously resets the Q outputs to the low level. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The CDC337 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

| INPUTS          |                  |            | OUTPUTS |                            |
|-----------------|------------------|------------|---------|----------------------------|
| $\overline{OE}$ | $\overline{CLR}$ | CLK        | Y1-Y4   | Q1-Q4                      |
| H               | X                | X          | Z       | Z                          |
| L               | L                | L          | L       | L                          |
| L               | L                | H          | H       | L                          |
| L               | H                | L          | L       | $Q_0^{\dagger}$            |
| L               | H                | $\uparrow$ | H       | $\overline{Q_0}^{\dagger}$ |

<sup>†</sup> The level of the Q outputs before the indicated steady-state input conditions were established



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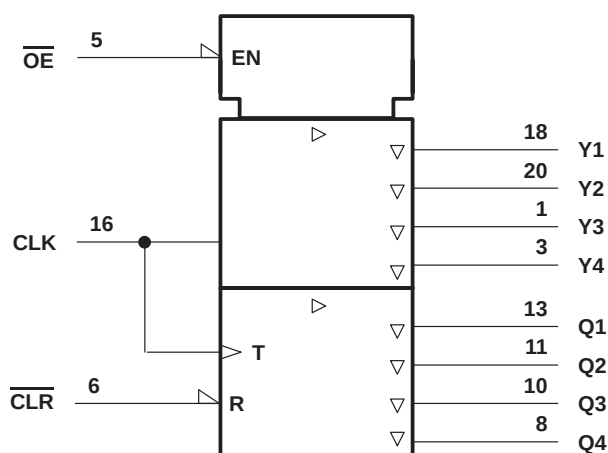
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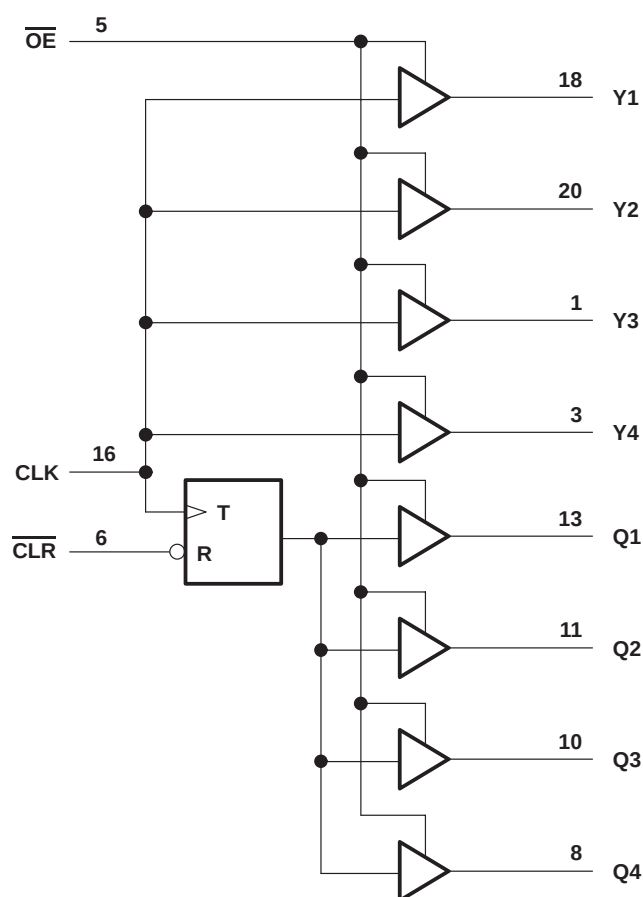
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|                                                                                              |                            |
|----------------------------------------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$                                                               | –0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1)                                                      | –0.5 V to 7 V              |
| Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, $I_O$                                              | 96 mA                      |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                                                  | –18 mA                     |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2)            | 1.6 W                      |
| Storage temperature range, $T_{stg}$                                                         | –65°C to 150°C             |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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**recommended operating conditions (see Note 3)**

|             |                                | MIN  | MAX      | UNIT |
|-------------|--------------------------------|------|----------|------|
| $V_{CC}$    | Supply voltage                 | 4.75 | 5.25     | V    |
| $V_{IH}$    | High-level input voltage       | 2    |          | V    |
| $V_{IL}$    | Low-level input voltage        |      | 0.8      | V    |
| $V_I$       | Input voltage                  | 0    | $V_{CC}$ | V    |
| $I_{OH}$    | High-level output current      |      | -48      | mA   |
| $I_{OL}$    | Low-level output current       |      | 48       | mA   |
| $f_{clock}$ | Input clock frequency          |      | 80       | MHz  |
| $T_A$       | Operating free-air temperature | -40  | 85       | °C   |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER       | TEST CONDITIONS                                                                       |                  | MIN  | TYP <sup>†</sup> | MAX  | UNIT |
|-----------------|---------------------------------------------------------------------------------------|------------------|------|------------------|------|------|
| V <sub>IK</sub> | V <sub>CC</sub> = 4.75 V, I <sub>I</sub> = −18 mA                                     |                  |      |                  | −1.2 | V    |
| V <sub>OH</sub> | V <sub>CC</sub> = 4.75 V, I <sub>OH</sub> = − 32 mA                                   |                  | 3.75 |                  |      | V    |
| V <sub>OL</sub> | V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 32 mA                                     |                  |      |                  | 0.55 | V    |
| I <sub>IH</sub> | V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V                                      |                  |      |                  | 50   | μA   |
| I <sub>IL</sub> | V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.5 V                                      |                  |      |                  | −50  | μA   |
| I <sub>OZ</sub> | V <sub>CC</sub> = 5.25 V, V <sub>O</sub> = V <sub>CC</sub> or GND                     |                  |      |                  | ±50  | μA   |
| I <sub>CC</sub> | V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | Outputs high     |      |                  | 70   | mA   |
|                 |                                                                                       | Outputs low      |      |                  | 85   |      |
|                 |                                                                                       | Outputs disabled |      |                  | 70   |      |
| C <sub>i</sub>  | V <sub>I</sub> = 2.5 V or 0.5 V                                                       |                  |      | 3                |      | pF   |
| C <sub>O</sub>  | V <sub>O</sub> = V <sub>CC</sub> or GND                                               |                  |      | 10               |      | pF   |

<sup>†</sup> All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

|             |                                                                      | MIN                         | MAX | UNIT |
|-------------|----------------------------------------------------------------------|-----------------------------|-----|------|
| $f_{clock}$ | Clock frequency                                                      |                             | 80  | MHz  |
| $t_w$       | Pulse duration                                                       | $\overline{\text{CLR}}$ low | 4   | ns   |
|             |                                                                      | CLK low                     | 4   |      |
|             |                                                                      | CLK high                    | 4   |      |
| $t_{su}$    | Setup time, $\overline{\text{CLR}}$ inactive before CLK <sup>↑</sup> |                             | 2   | ns   |
|             | Clock duty cycle                                                     | 40%                         | 60% |      |

# CDC337

## CLOCK DRIVER

### WITH 3-STATE OUTPUTS

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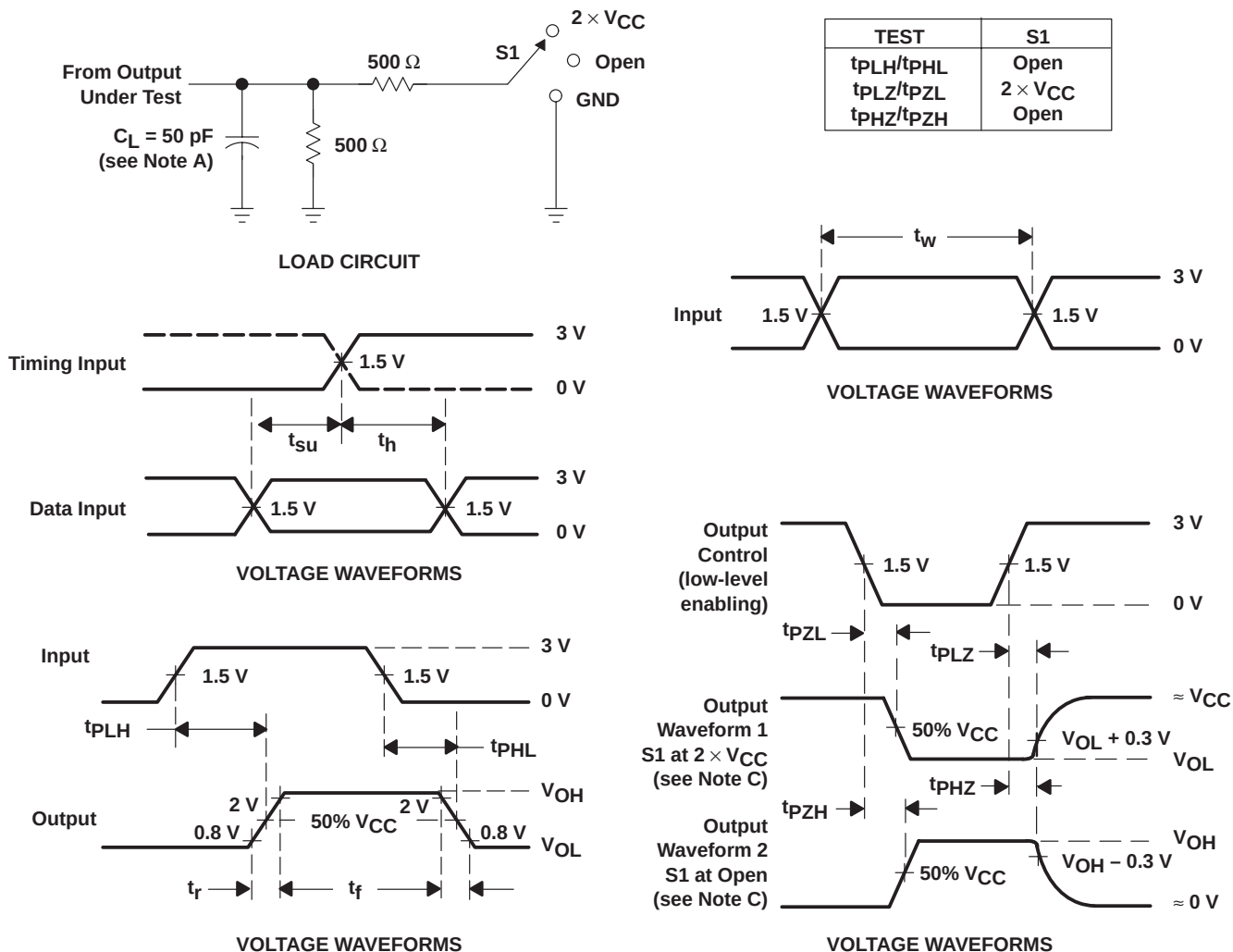
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Note 4 and Figures 1 and 2)

| PARAMETER   | FROM<br>(INPUT)  | TO<br>(OUTPUT) | MIN | TYP† | MAX  | UNIT |
|-------------|------------------|----------------|-----|------|------|------|
| $f_{max}$   |                  |                | 80  |      |      | MHz  |
| $t_{PLH}$   | CLK              | Any Y or Q     | 4   |      | 9    | ns   |
| $t_{PHL}$   |                  |                | 4   |      | 9    |      |
| $t_{PHL}$   | $\overline{CLR}$ | Any Q          | 4   |      | 10   | ns   |
| $t_{PZH}$   | $\overline{OE}$  | Any Y or Q     | 3   |      | 7    | ns   |
| $t_{PZL}$   |                  |                | 3   |      | 7    |      |
| $t_{PHZ}$   | $\overline{OE}$  | Any Y or Q     | 2   |      | 7    | ns   |
| $t_{PLZ}$   |                  |                | 2   |      | 7    |      |
| $t_{sk(o)}$ | CLK↑             | Y↑             |     |      | 0.75 | ns   |
|             |                  | Q↑             |     |      | 0.9  |      |
|             |                  | Y↑ and Q↑      |     |      | 0.9  |      |
| $t_r$       |                  |                |     | 0.9  |      | ns   |
| $t_f$       |                  |                |     | 0.7  |      | ns   |

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

NOTE 4: All specifications are valid only for all outputs switching.

## PARAMETER MEASUREMENT INFORMATION



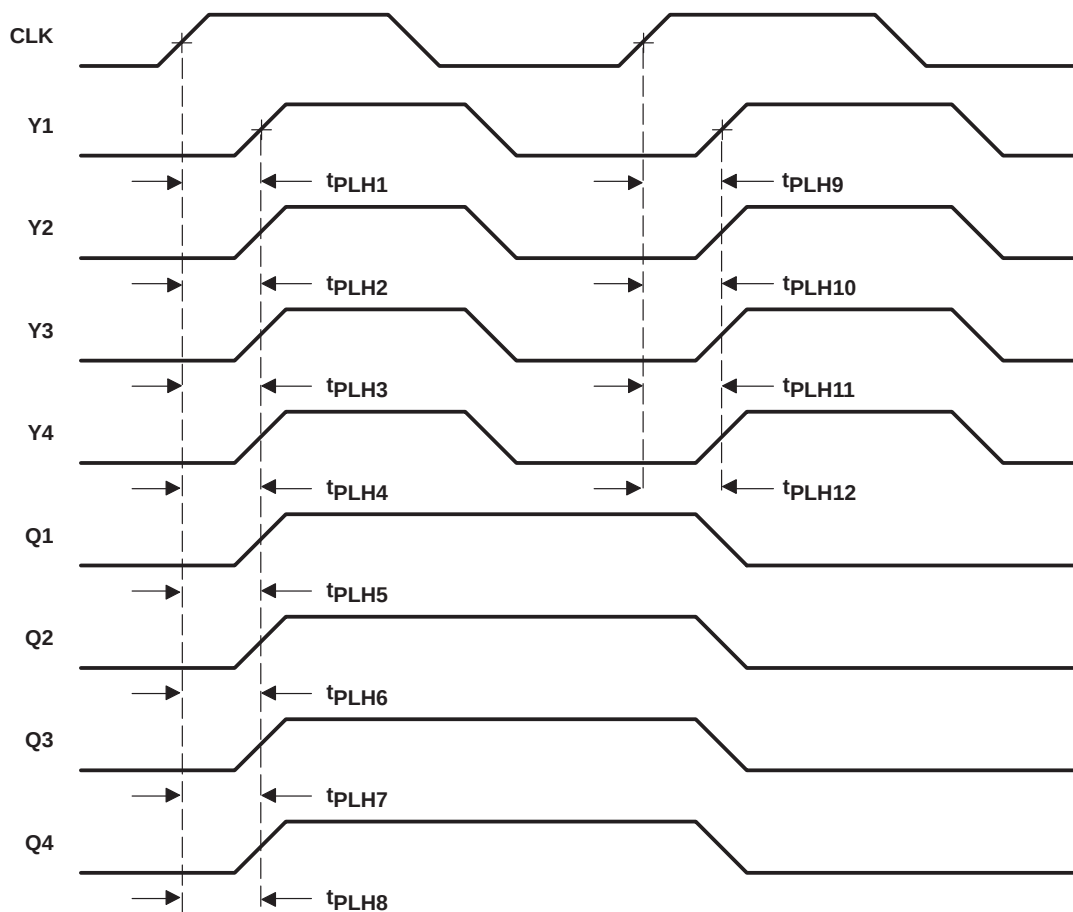
- NOTES:
- $C_L$  includes probe and jig capacitance.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A. Output skew,  $t_{sk(o)}$ , from  $CLK\uparrow$  to  $Y\uparrow$ , is calculated as the greater of the difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 1, 2, 3, 4$ ) or  $t_{PLHn}$  ( $n = 9, 10, 11, 12$ ).
- B. Output skew,  $t_{sk(o)}$ , from  $CLK\uparrow$  to  $Q\uparrow$ , is calculated as the greater of the difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 5, 6, 7, 8$ ).
- C. Output skew,  $t_{sk(o)}$ , from  $CLK\uparrow$  to  $Y\uparrow$  and  $Q\uparrow$ , is calculated as the greater of the difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 1, 2, \dots, 8$ ).

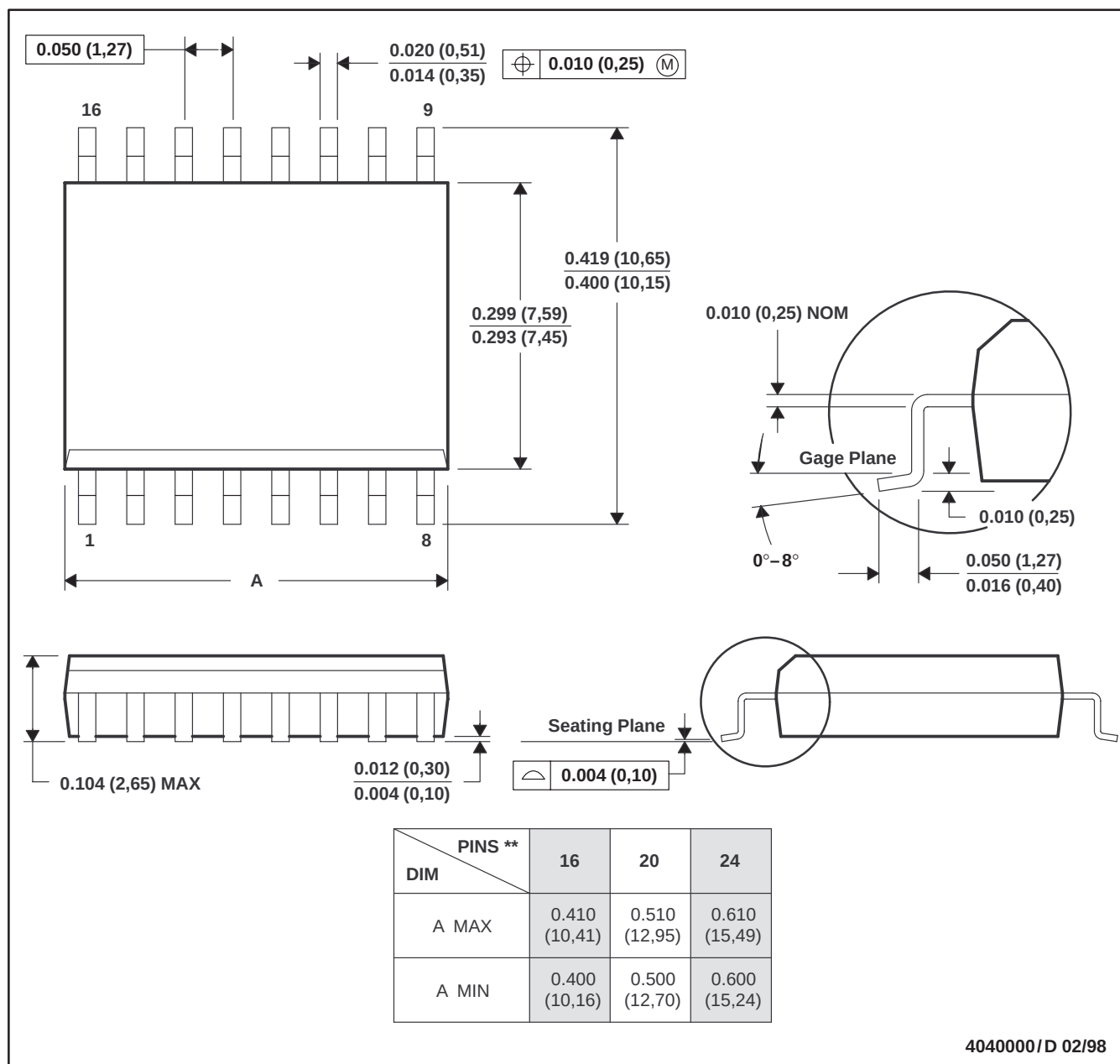
**Figure 2. Waveforms for Calculation of  $t_{sk(o)}$**

## MECHANICAL INFORMATION

**DW (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-013

## PACKAGING INFORMATION

| Orderable part number    | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CDC337DW</a> | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDC337              |
| CDC337DW.B               | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDC337              |
| CDC337DWG4               | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDC337              |
| CDC337DWG4.B             | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CDC337              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TUBE



\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CDC337DW     | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| CDC337DW.B   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| CDC337DWG4   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| CDC337DWG4.B | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |

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