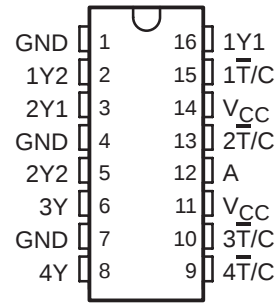


CDC328A 1-LINE TO 6-LINE CLOCK DRIVER WITH SELECTABLE POLARITY

SCAS327B – DECEMBER 1992 – REVISED NOVEMBER 1995

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- TTL-Compatible Inputs and Outputs
- Distributes One Clock Input to Six Clock Outputs
- Polarity Control Selects True or Complementary Outputs
- Distributed V_{CC} and GND Pins Reduce Switching Noise
- High-Drive Outputs ($-48\text{-mA } I_{OH}$, $48\text{-mA } I_{OL}$)
- State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages

D OR DB PACKAGE
(TOP VIEW)



description

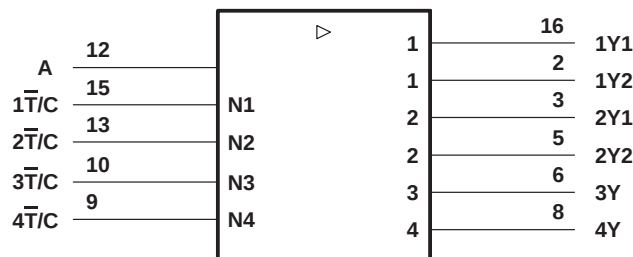
The CDC328A contains a clock-driver circuit that distributes one input signal to six outputs with minimum skew for clock distribution. Through the use of the polarity-control inputs ($\overline{T/C}$), various combinations of true and complementary outputs can be obtained.

The CDC328A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS		OUTPUT Y
$\overline{T/C}$	A	
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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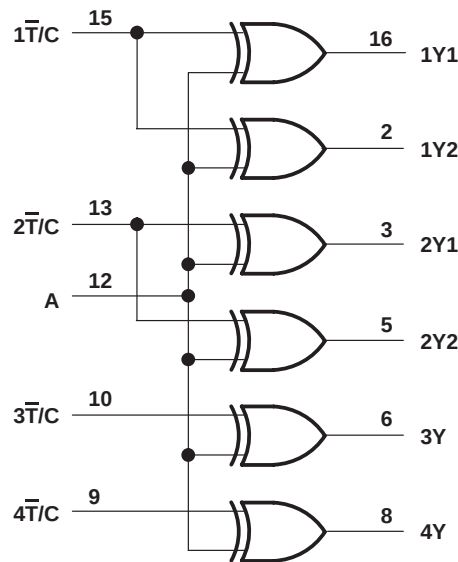
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O	96 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	0.77 W
DB package	0.6 W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 300 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

CDC328A
1-LINE TO 6-LINE CLOCK DRIVER
WITH SELECTABLE POLARITY

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recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0	V_{CC}		V
I_{OH}	High-level output current			-48	mA
I_{OL}	Low-level output current			48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
f_{clock}	Input clock frequency			100	MHz
T_A	Operating free-air temperature	-40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



CDC328A

1-LINE TO 6-LINE CLOCK DRIVER WITH SELECTABLE POLARITY

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IK}	$V_{CC} = 4.75 \text{ V}$,	$I_I = -18 \text{ mA}$			-1.2	V
V_{OH}	$V_{CC} = 4.75 \text{ V}$,	$I_{OH} = -48 \text{ mA}$	2			V
V_{OL}	$V_{CC} = 4.75 \text{ V}$,	$I_{OL} = 48 \text{ mA}$			0.5	V
I_I	$V_{CC} = 5.25 \text{ V}$,	$V_I = V_{CC} \text{ or GND}$			± 1	μA
$I_{O\ddagger}$	$V_{CC} = 5.25 \text{ V}$,	$V_O = 2.5 \text{ V}$	-15		-100	mA
I_{CC}	$V_{CC} = 5.25 \text{ V}$, $V_I = V_{CC} \text{ or GND}$	$I_O = 0$,			10	mA
		Outputs high			40	
C_i	$V_I = 2.5 \text{ V or } 0.5 \text{ V}$				3	pF

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

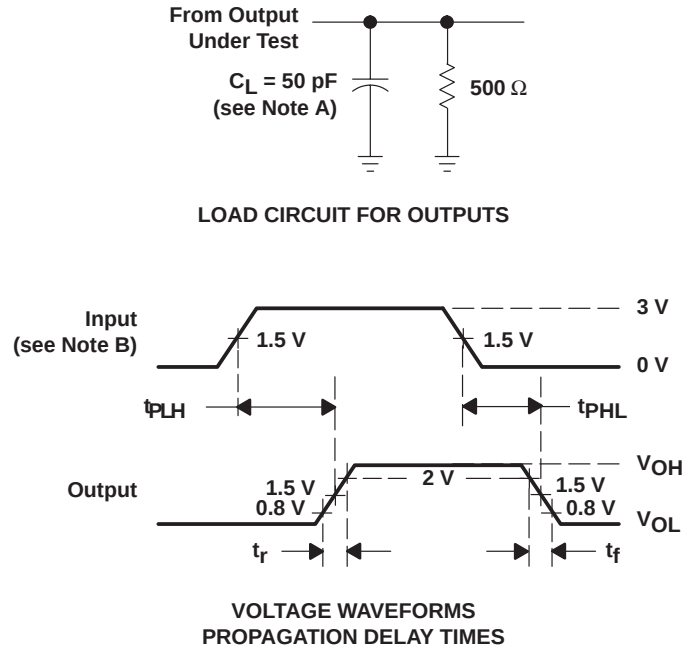
[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{PLH}	A	Any Y	1.7	5	ns
t _{PHL}			1.5	5	
t _{PLH}	T̄/C	Any Y	1.5	5	ns
t _{PHL}			1.4	5	
t _{sk(o)}	A	Any Y (same phase)	0.5		ns
		Any Y (any phase)	1		
t _{sk(p)}	A	Any Y	1		ns
t _r		Any Y	1.5		ns
t _f		Any Y	1.5		ns



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

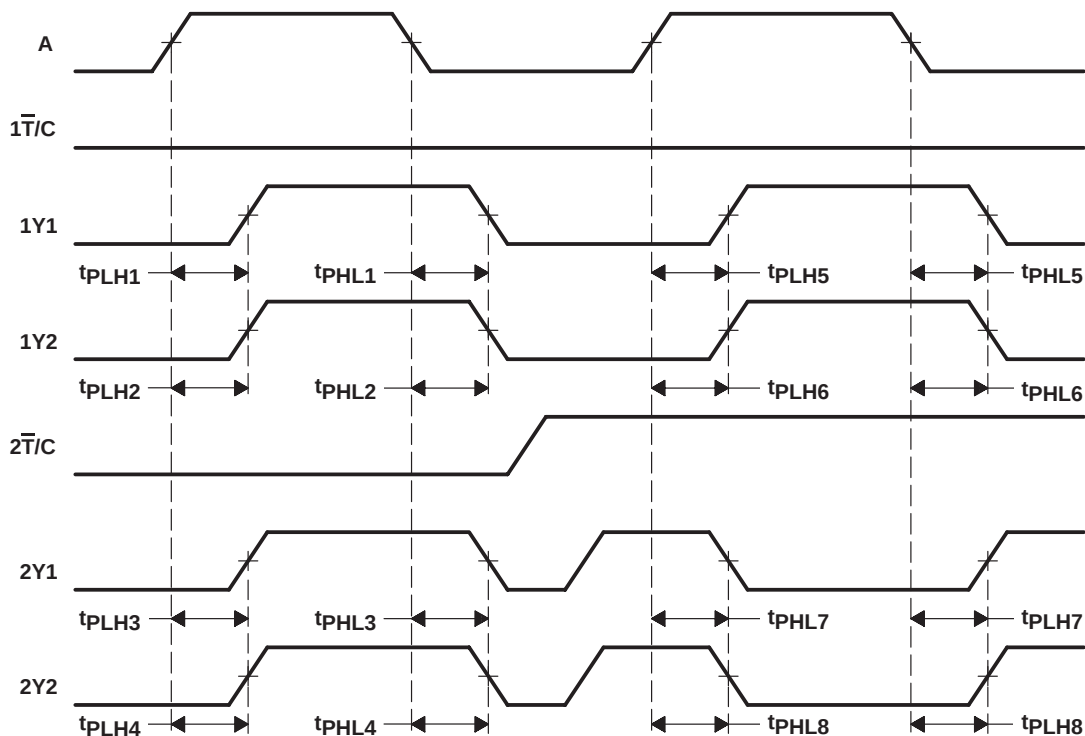
Figure 1. Load Circuit and Voltage Waveforms

CDC328A

1-LINE TO 6-LINE CLOCK DRIVER WITH SELECTABLE POLARITY

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output skew, $t_{sk(o)}$, from A to any Y (same phase), can be measured only between outputs for which the respective polarity-control inputs ($\overline{T/C}$) are at the same logic level. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from $A\uparrow$ to any Y (e.g., t_{PLHn} , $n = 1$ to 4; or t_{PLHn} , $n = 5$ to 6)
 - The difference between the fastest and slowest of t_{PHL} from $A\downarrow$ to any Y (e.g., t_{PHLn} , $n = 1$ to 4; or t_{PHLn} , $n = 5$ to 6)
 - The difference between the fastest and slowest of t_{PLH} from $A\downarrow$ to any Y (e.g., t_{PLHn} , $n = 7$ to 8)
 - The difference between the fastest and slowest of t_{PHL} from $A\uparrow$ to any Y (e.g., t_{PHLn} , $n = 7$ to 8)
- B. Output skew, $t_{sk(o)}$, from A to any Y (any phase), can be measured between outputs for which the respective polarity-control inputs ($\overline{T/C}$) are at the same or different logic levels. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from $A\uparrow$ to any Y or t_{PHL} from $A\uparrow$ to any Y (e.g., t_{PLHn} , $n = 1$ to 4; or t_{PLHn} , $n = 5$ to 6, and t_{PHLn} , $n = 7$ to 8)
 - The difference between the fastest and slowest of t_{PHL} from $A\downarrow$ to any Y or t_{PLH} from $A\downarrow$ to any Y (e.g., t_{PHLn} , $n = 1$ to 4; or t_{PHLn} , $n = 5$ to 6, and t_{PLHn} , $n = 7$ to 8)
- C. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ ($n = 1, 2, 3, 4, 5, 6, 7, 8$).

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC328AD	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC328A
CDC328AD.B	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC328A
CDC328ADBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK328A
CDC328ADBR.B	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK328A
CDC328ADG4	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC328A
CDC328ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC328A
CDC328ADR.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC328A
CDC328ADRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC328A
CDC328ADRG4.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC328A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC328ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
CDC328ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CDC328ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC328ADBR	SSOP	DB	16	2000	353.0	353.0	32.0
CDC328ADR	SOIC	D	16	2500	350.0	350.0	43.0
CDC328ADRG4	SOIC	D	16	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CDC328AD	D	SOIC	16	40	505.46	6.76	3810	4
CDC328AD.B	D	SOIC	16	40	505.46	6.76	3810	4
CDC328ADG4	D	SOIC	16	40	505.46	6.76	3810	4

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