CDx4HC85, CDx4HCT85 High-Speed CMOS Logic 4-Bit Magnitude Comparator

1 Features

- Buffered inputs and outputs
- Typical propagation delay: 13 ns (data to output at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C)
- Serial or parallel expansion without external gating
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temperature range: –55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- HC types
  - 2 V to 6 V operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5 V
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility, V_{IL} = 0.8 V (max), V_{IH} = 2 V (min)
  - CMOS input compatibility, $I_I \leq 1$ µA at V_{OL}, V_{OH}

2 Description

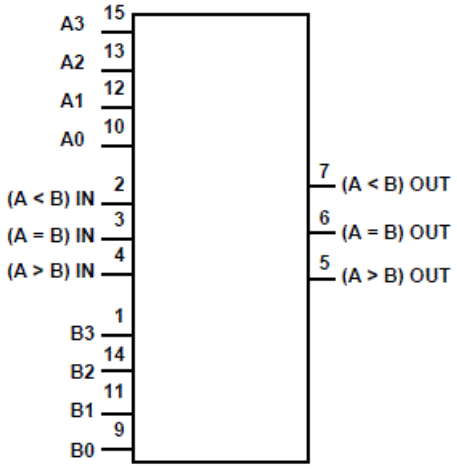
The ’HC85 and ’HCT85 are high speed magnitude comparators that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These 4-bit devices compare two binary, BCD, or other monotonic codes and present the three possible magnitude results at the outputs (A > B, A < B, and A = B). The 4-bit input words are weighted (A0 to A3 and B0 to B3), where A3 and B3 are the most significant bits.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD54HC85F3A	CDIP (16)	24.38 mm × 6.92 mm
CD54HCT85F3A	CDIP (16)	24.38 mm × 6.92 mm
CD74HC85M	SOIC (16)	9.90 mm × 3.90 mm
CD74HCT85M	SOIC (16)	9.90 mm × 3.90 mm
CD74HC85E	PDIP (16)	19.31 mm × 6.35 mm
CD74HCT85E	PDIP (16)	19.31 mm × 6.35 mm
CD74HC85NS	SO (16)	6.20 mm × 5.30 mm
CD74HC85PW	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Diagram

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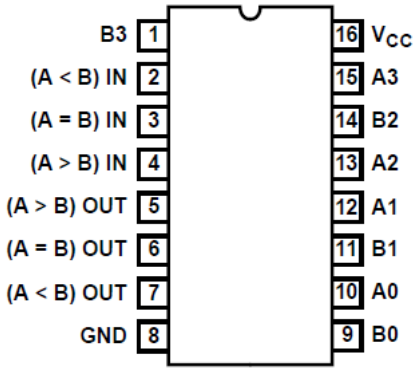
3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2003) to Revision F (February 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards	1

4 Pin Configuration and Functions



J, N, D, NS, or PW package
16-Pin CDIP, PDIP, SOIC, SO, or TSSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input diode current	For $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output diode current	For $V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Output source or sink current per output pin	For $V_O > –0.5$ V or $V_O < V_{CC} + 0.5$ V		±25	mA
I_{CC}	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C
	Lead temperature (Soldering 10s) (SOIC - lead tips only)			300	°C

(1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V_I, V_O	Input or output voltage		0	V_{CC}	V
	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T_A	Temperature range		–55	125	℃

5.3 Thermal Information

THERMAL METRIC		D (SOIC) 16 PINS	N (PDIP) 16 PINS	NS (SO) 16 PINS	PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	73	67	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS(1)	V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High level output voltage	I_{OH} = – 20 µA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		
		I_{OH} = – 20 µA	6	5.9			5.9		5.9		
	High level output voltage	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		
		I_{OH} = – 5.2 mA	6	5.48			5.34		5.2		
V_{OL}	Low level output voltage	I_{OL} = 20 µA	2			0.1		0.1		0.1	V
		I_{OL} = 20 µA	4.5			0.1		0.1		0.1	
		I_{OL} = 20 µA	6			0.1		0.1		0.1	
	Low level output voltage	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	
		I_{OL} = 5.2 mA	6			0.26		0.33		0.4	V
I_I	Input leakage current		6			±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	6			8		80		160	µA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage	I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
	High level output voltage	I_{OH} = – 4 µA	4.5	3.98			3.84		3.7		
V_{OL}	Low level output voltage	I_{OL} = 20 µA	4.5			0.1		0.1		0.1	V
	Low level output voltage	I_{OL} = 4 µA	4.5			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	5.5			±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	5.5			8		80		160	µA
ΔI_{CC} (2)	Additional supply current per input pin	A_0 - A_3, B_0 - B_3 and (A = B) IN(3)	4.5 to 5.5		100	540		675		735	µA
		(A > B) IN, (A < B) IN(3)	4.5 to 5.5		100	360		450		490	µA

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.
(2) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
(3) Inputs held at V_{CC} – 2.1.

5.5 Switching Specifications

Input t_r, t_f = 6 ns

PARAMETER		V_{CC} (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t_{PLH}, t_{PHL}	Propagation delay, A_n, B_n to (A > B) OUT, (A < B) OUT	2			195		245		295	ns
		4.5		16[3]	39		47		59	
		6			33		42		50	
t_{PLH}, t_{PHL}	A_n, B_n to (A = B) OUT	2			175		240		265	ns
		4.5		14[3]	35		44		53	
		6			30		37		45	
t_{PLH}, t_{PHL}	(A > B) IN, (A < B) IN, (A = B) IN to (A > B) OUT, (A < B) OUT	2			140		175		210	ns
		4.5		11[3]	28		35		42	
		6			24		30		36	
t_{PLH}, t_{PHL}	(A > B) IN to (A = B) OUT	2			120		150		180	ns
		4.5		9[3]	24		30		36	
		6			20		26		31	
C_{PD}	Power dissipation capacitance[1] [2]	5		24						pF
t_{TLH}, t_{THL}	Output transition times (Figure 6-1)	2			75		95		110	ns
		4.5			15		19		22	
		6			13		16		19	
C_{IN}	Input capacitance				10		10		10	pF
HCT TYPES										
t_{PLH}, t_{PHL}	Propagation delay, A_n, B_n to (A > B) OUT, (A < B) OUT	4.5		15[3]	37		46		56	ns
t_{PLH}, t_{PHL}	A_n, B_n to (A = B) OUT	4.5		17[3]	40		50		60	ns
t_{PLH} t_{PHL}	(A > B) IN, (A < B) IN, (A = B) IN to (A > B) OUT, (A < B) OUT	4.5		12[3]	30		38		45	ns
t_{PLH}, t_{PHL}	(A > B) IN to (A = B) OUT	4.5		13[3]	31		39		47	ns
t_{TLH}, t_{THL}	Output transition times (Figure 6-1)	4.5			15		19		22	ns
C_{PD}	Power dissipation capacitance[1] [2]	5		26						pF
C_{IN}	Input capacitance				10		10		10	pF

(1) C_{PD} is used to determine the dynamic power consumption, per gate/package.
(2) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.
(3) C_L = 15 pF and V_{CC} = 5 V.

6 Parameter Measurement Information

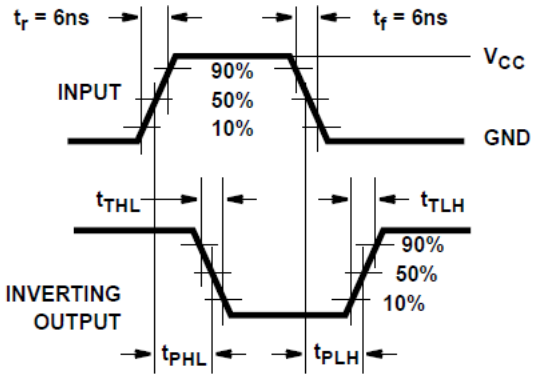


Figure 6-1. HC and HCU Transition Times and Propagation Delay Times, Combination Logic

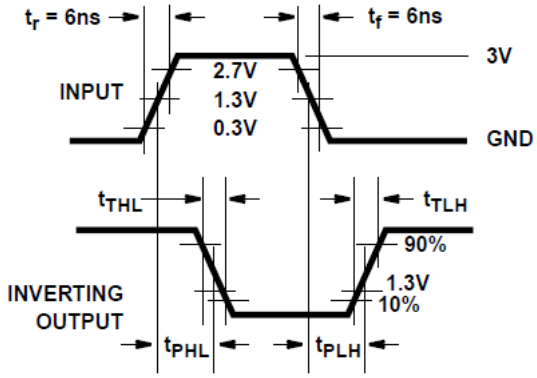


Figure 6-2. HCT Transition Times and Propagation Delay Times, Combination Logic

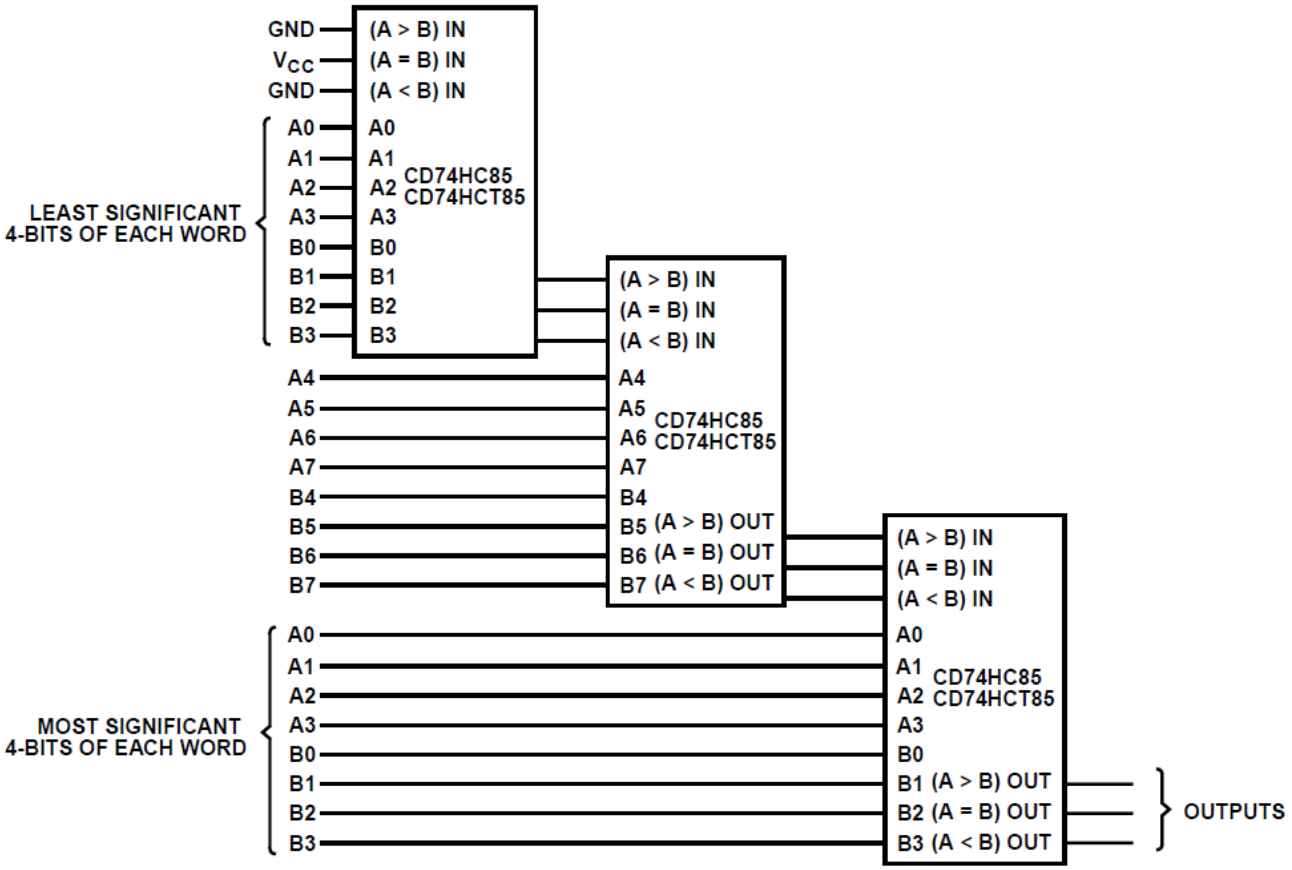


Figure 6-3. Series Cascading - Comparing 12-Bit Words

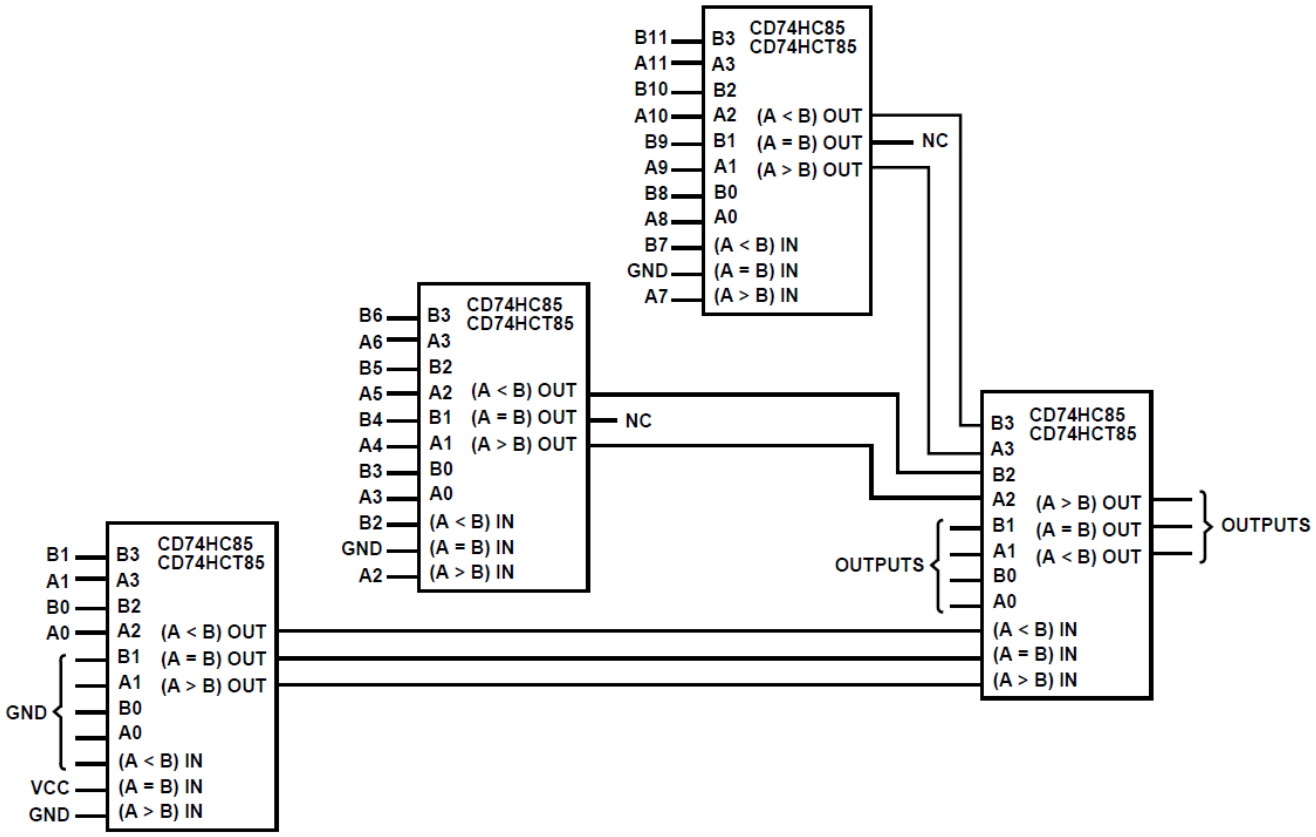


Figure 6-4. Parallel Cascading - Comparing 12-Bit Words

7 Detailed Description

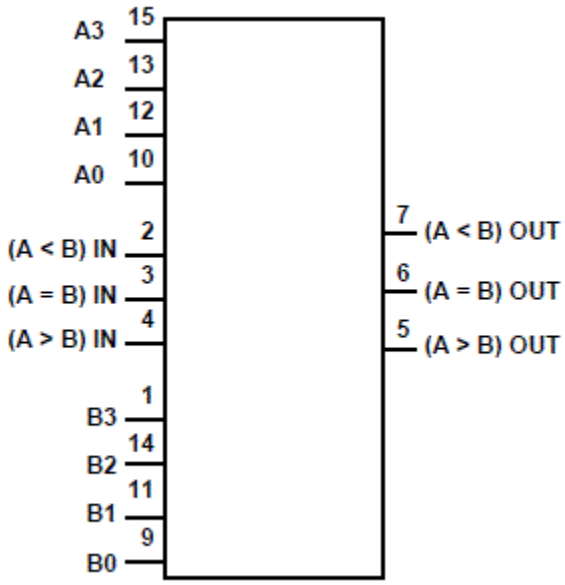
7.1 Overview

The ’HC85 and ’HCT85 are high speed magnitude comparators that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These 4-bit devices compare two binary, BCD, or other monotonic codes and present the three possible magnitude results at the outputs (A > B, A < B, and A = B). The 4-bit input words are weighted (A0 to A3 and B0 to B3), where A3 and B3 are the most significant bits.

The devices are expandable without external gating, in both serial and parallel fashion. The upper part of the truth table indicates operation using a single device or devices in a serially expanded application. The parallel expansion scheme is described by the last three entries in the truth table.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Truth Table(1)

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
SINGLE DEVICE OR SERIES CASCADING									
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 >B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
PARALLEL CASCADING									
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

(1) H = high voltage level, L = low voltage level, X = don’t care

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

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All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8867201EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8867201EA CD54HCT85F3A
8601301EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8601301EA CD54HC85F3A
CD54HC85F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8601301EA CD54HC85F3A
CD54HC85F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8601301EA CD54HC85F3A
CD54HCT85F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8867201EA CD54HCT85F3A
CD54HCT85F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8867201EA CD54HCT85F3A
CD74HC85E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC85E
CD74HC85E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC85E
CD74HC85EE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC85E
CD74HC85M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC85M
CD74HC85M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC85M
CD74HC85M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC85M
CD74HC85MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC85M
CD74HC85NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC85M
CD74HC85NSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC85M
CD74HC85PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ85
CD74HC85PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HJ85
CD74HC85PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ85
CD74HC85PWT	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ85
CD74HCT85E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT85E
CD74HCT85E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT85E
CD74HCT85M	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT85M
CD74HCT85M.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT85M
CD74HCT85MT	NRND	Production	SOIC (D) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT85M
CD74HCT85MT.A	NRND	Production	SOIC (D) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT85M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD54HC85, CD54HCT85, CD74HC85, CD74HCT85 :

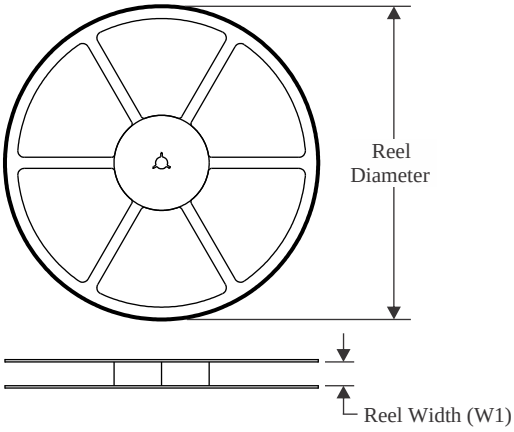
- Catalog : CD74HC85, CD74HCT85
- Military : CD54HC85, CD54HCT85

NOTE: Qualified Version Definitions:

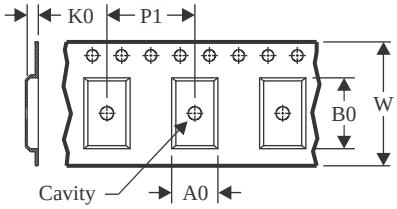
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

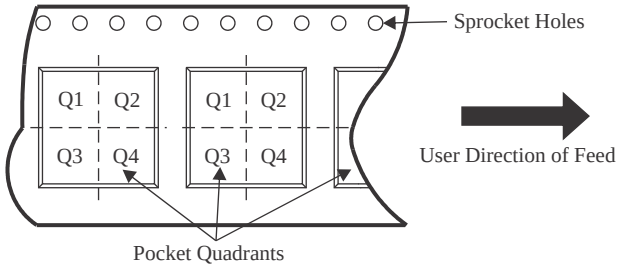


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

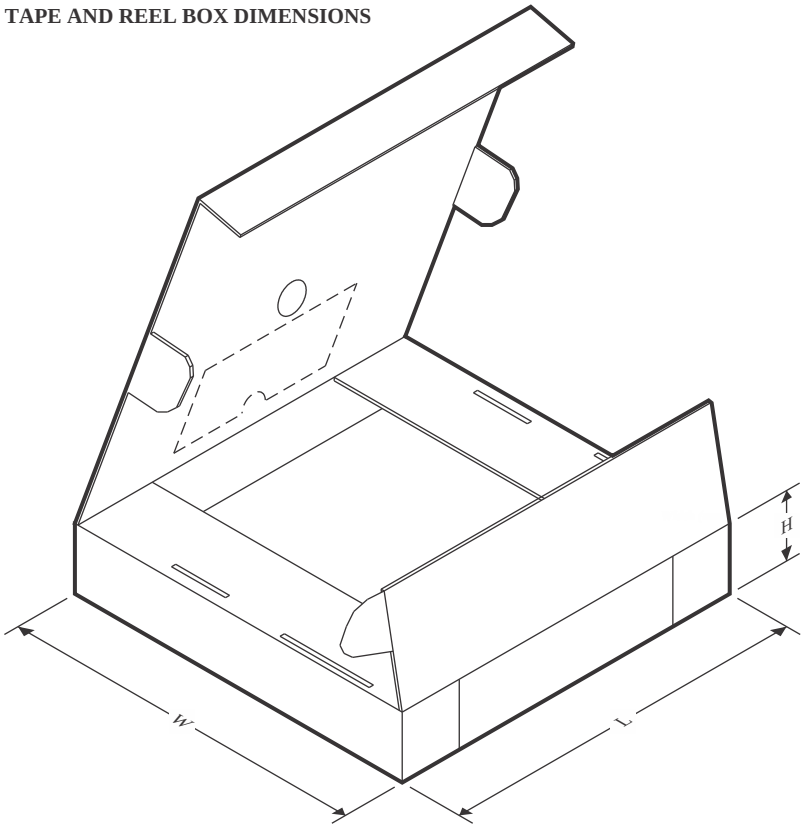
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC85M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC85NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD74HC85PWR	TSSOP	PW	16	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
CD74HC85PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC85PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

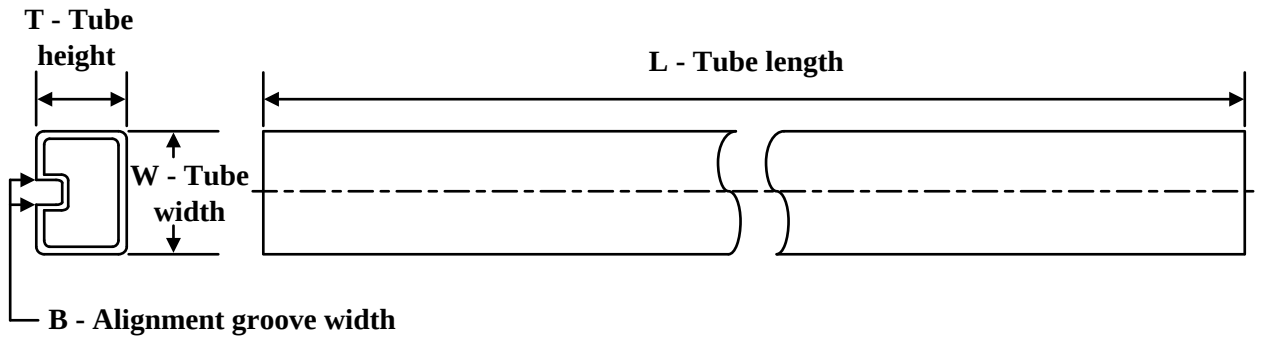
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

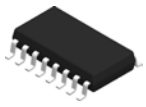
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC85M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC85NSR	SOP	NS	16	2000	353.0	353.0	32.0
CD74HC85PWR	TSSOP	PW	16	2000	366.0	364.0	50.0
CD74HC85PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD74HC85PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC85E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC85E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC85E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC85E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC85EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC85EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT85E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT85E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT85E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT85E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT85M	D	SOIC	16	40	507	8	3940	4.32
CD74HCT85M.A	D	SOIC	16	40	507	8	3940	4.32

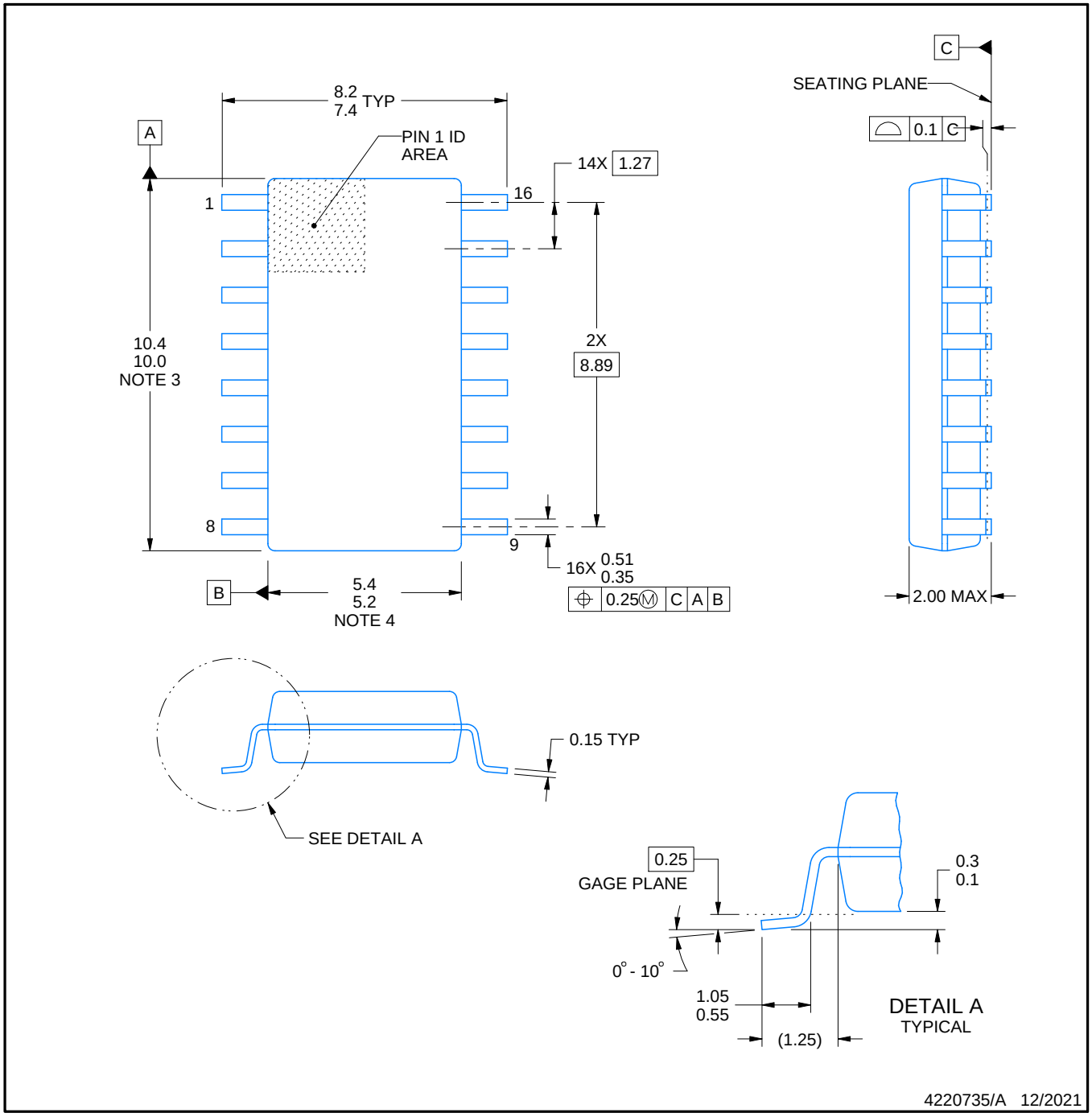


PACKAGE OUTLINE

NS0016A

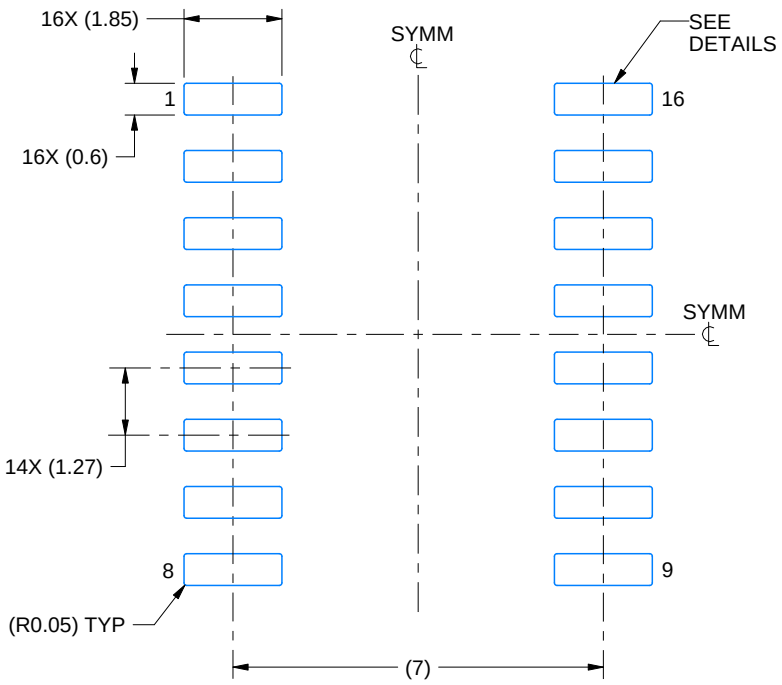
SOP - 2.00 mm max height

SOP

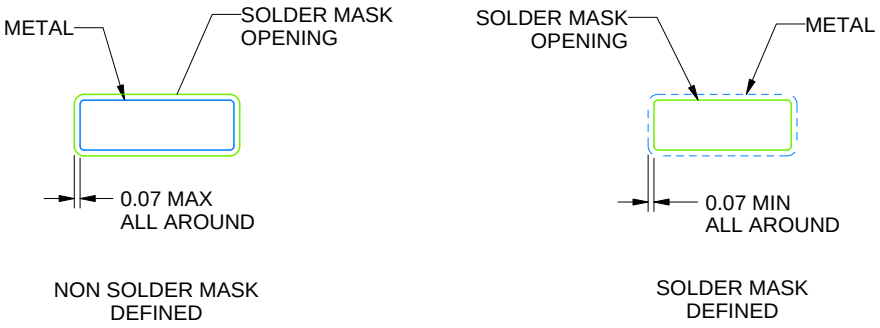


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

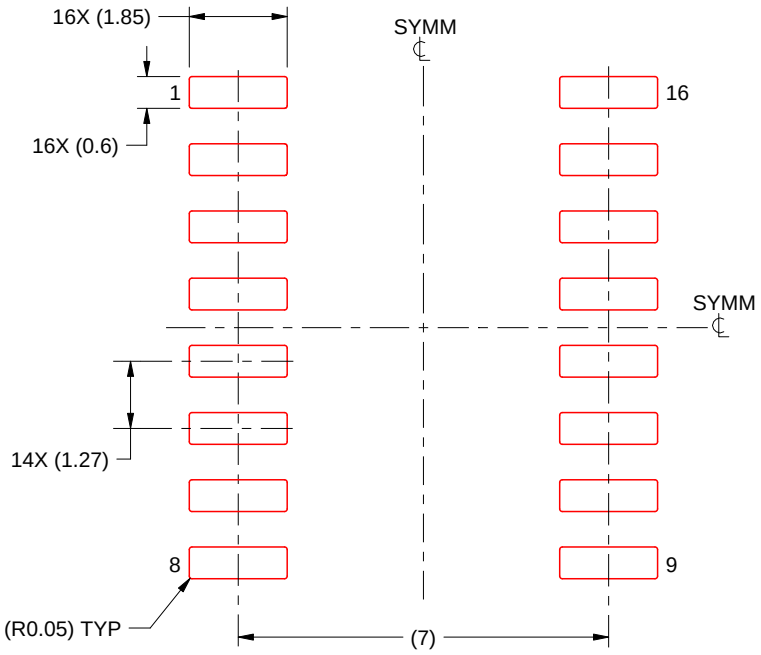
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



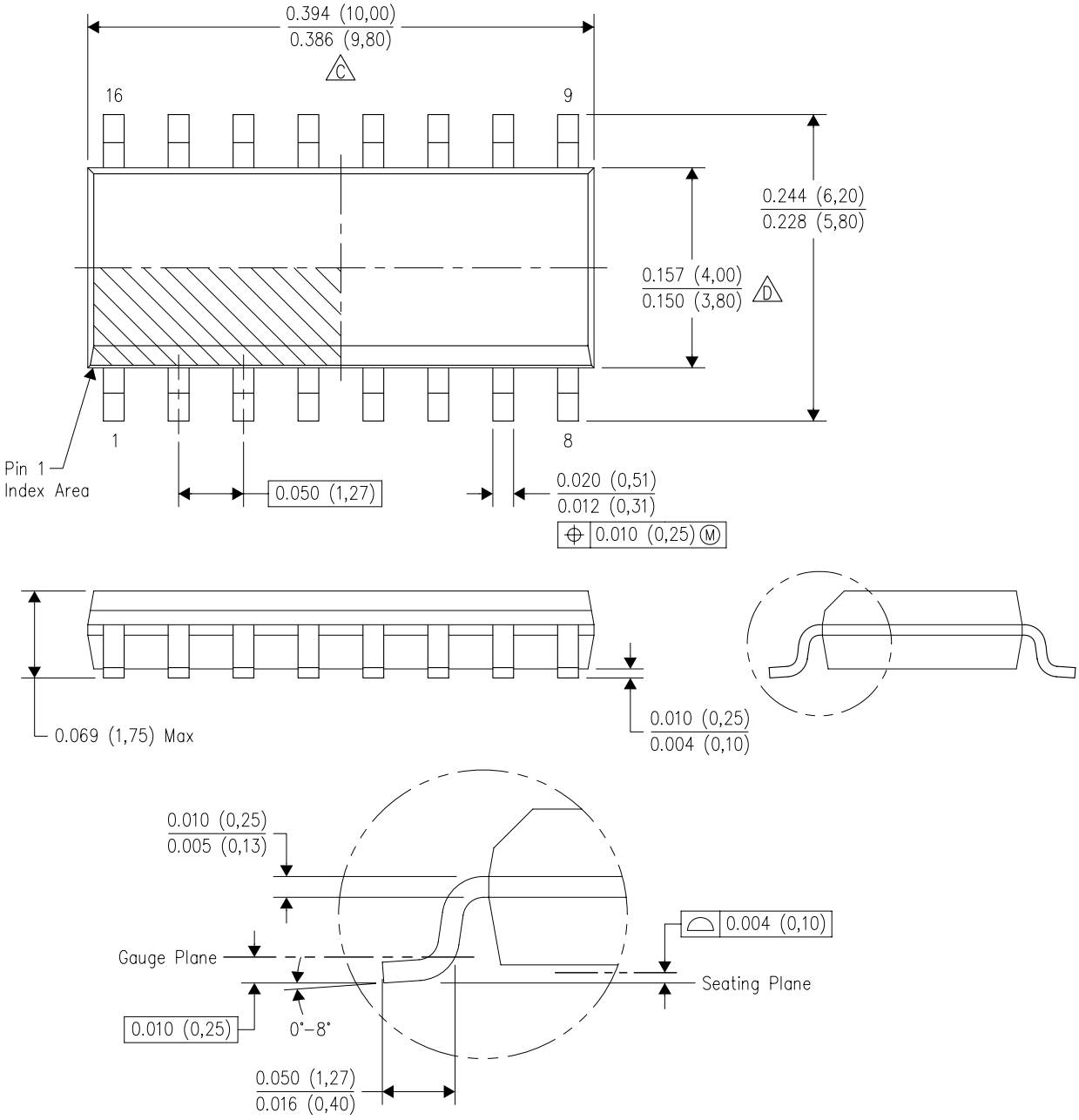
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

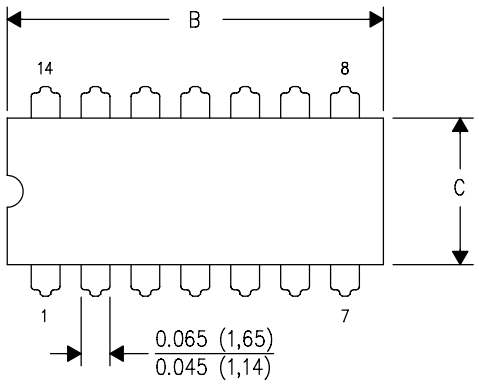


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

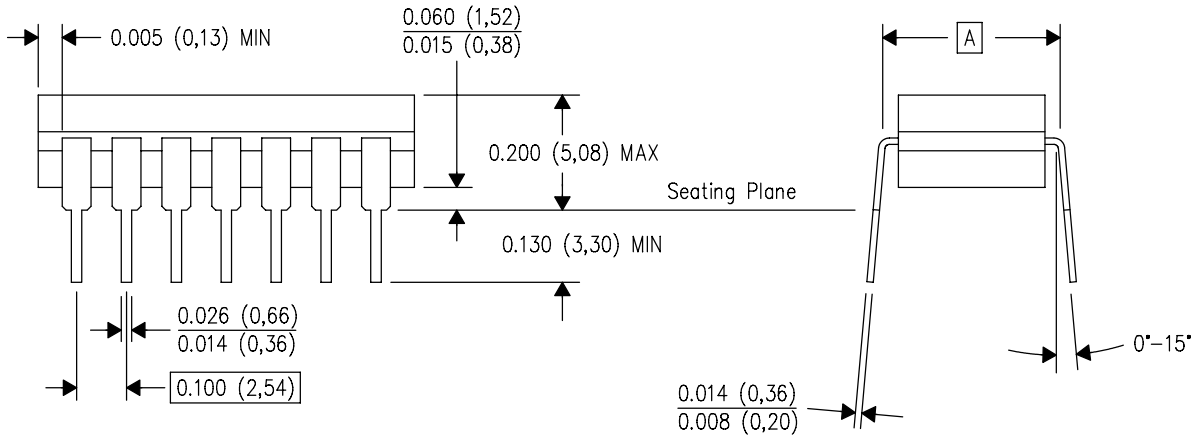
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

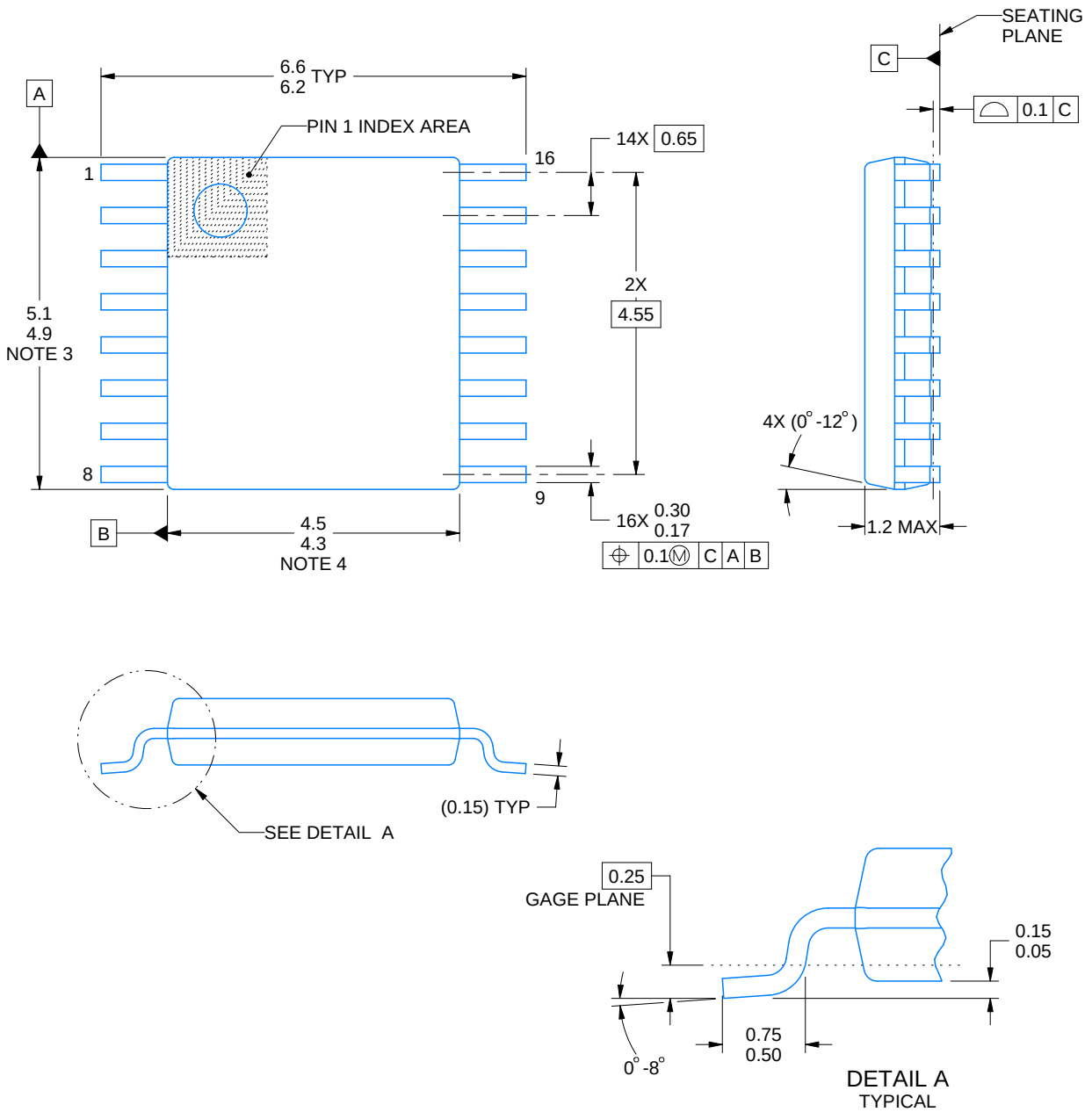
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PACKAGE OUTLINE

PW0016A

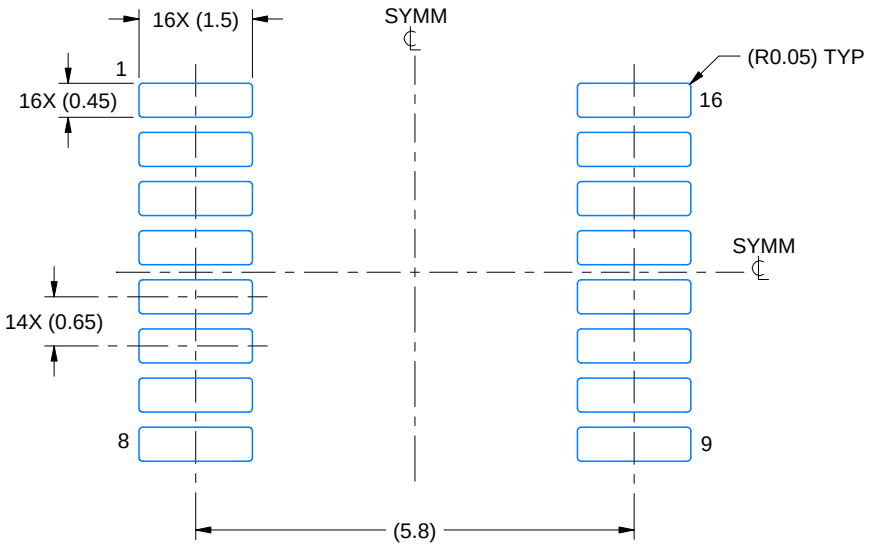
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



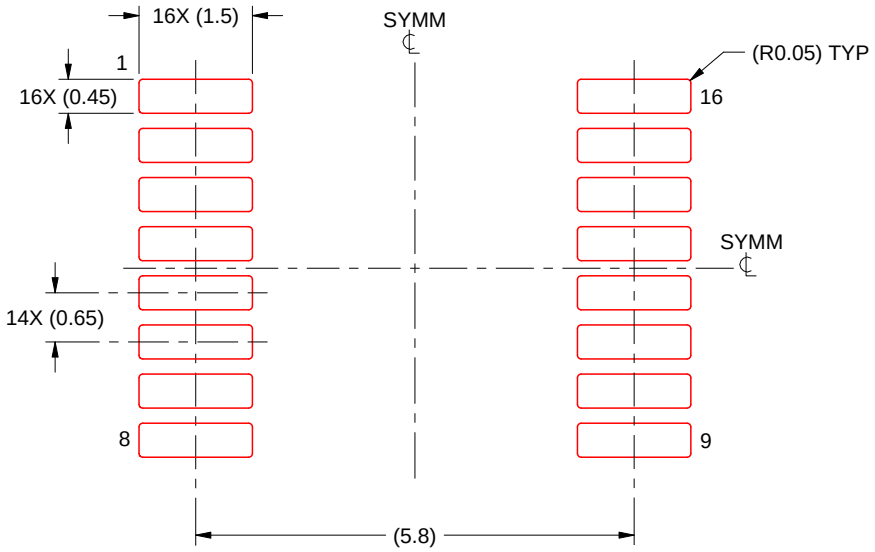
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

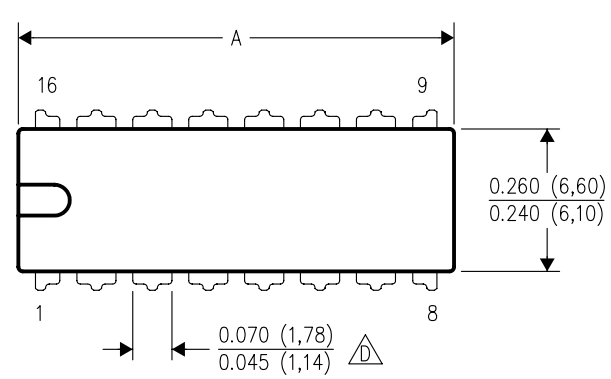
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

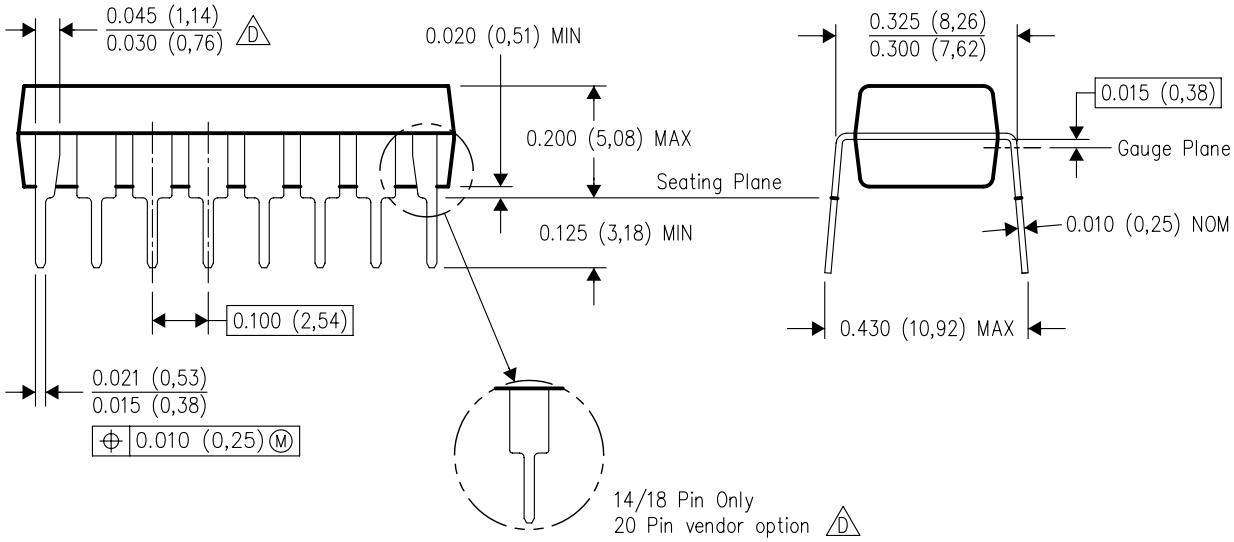
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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