

High-Speed CMOS Logic Octal-Bus Transceiver/Registers, Three-State

Features

- CD74HC652, CD74HCT652 Non-Inverting
- Independent Registers for A and B Buses
- Three-State Outputs
- Drives 15 LSTTL Loads
- Typical Propagation Delay = 12ns at $V_{CC} = 5V$, $C_L = 15pF$
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The CD74HC652 and CD74HCT652 three-state, octal-bus transceiver/registers use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits. The CD74HC652 and CD74HCT652 have non-inverting outputs. These devices consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OE_{AB} and OE_{BA} are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrates the four fundamentals bus-management functions that can be performed with the octal-bus transceivers and registers.

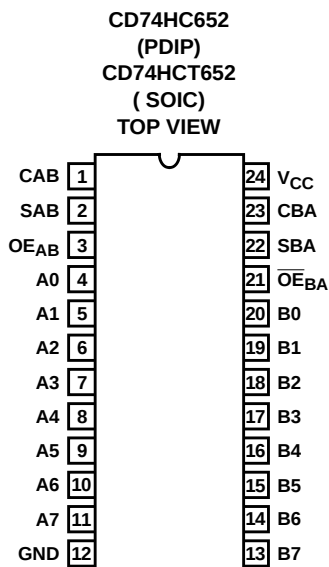
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select of the control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the D-type flip-flops by simultaneously enabling OE_{AB} and OE_{BA} . In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD74HC652EN	-55 to 125	24 Ld PDIP
CD74HCT652M	-55 to 125	24 Ld SOIC
CD74HCT652M96	-55 to 125	24 Ld SOIC

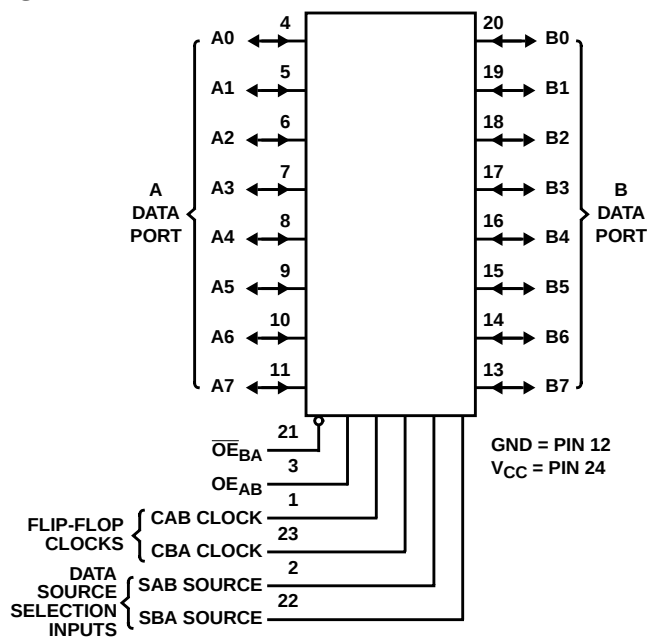
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

Pinout



CD74HC652, CD74HCT652

Functional Diagram



FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
OE _{AB}	OE _{BA}	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	651	652
L	H	H or L	H or L	X	X	Input	Input	Isolation (Note 1)	Isolation (Note 1)
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified (Note 2)	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X (Note 3)	X	Input	Output	Store A in Both Registers	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified (Note 2)	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X (Note 3)	Output	Input	Store B in Both Registers	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and	Stored A Data to B Bus
								Stored B Data to A Bus	Stored B Data to A Bus

NOTES:

- To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.
- The data output functions may be enabled or disabled by various signals at the OE_{AB} or OE_{BA} inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
- Select Control = L: Clocks can occur simultaneously.
Select Control = H: Clocks must be staggered in order to load both registers.

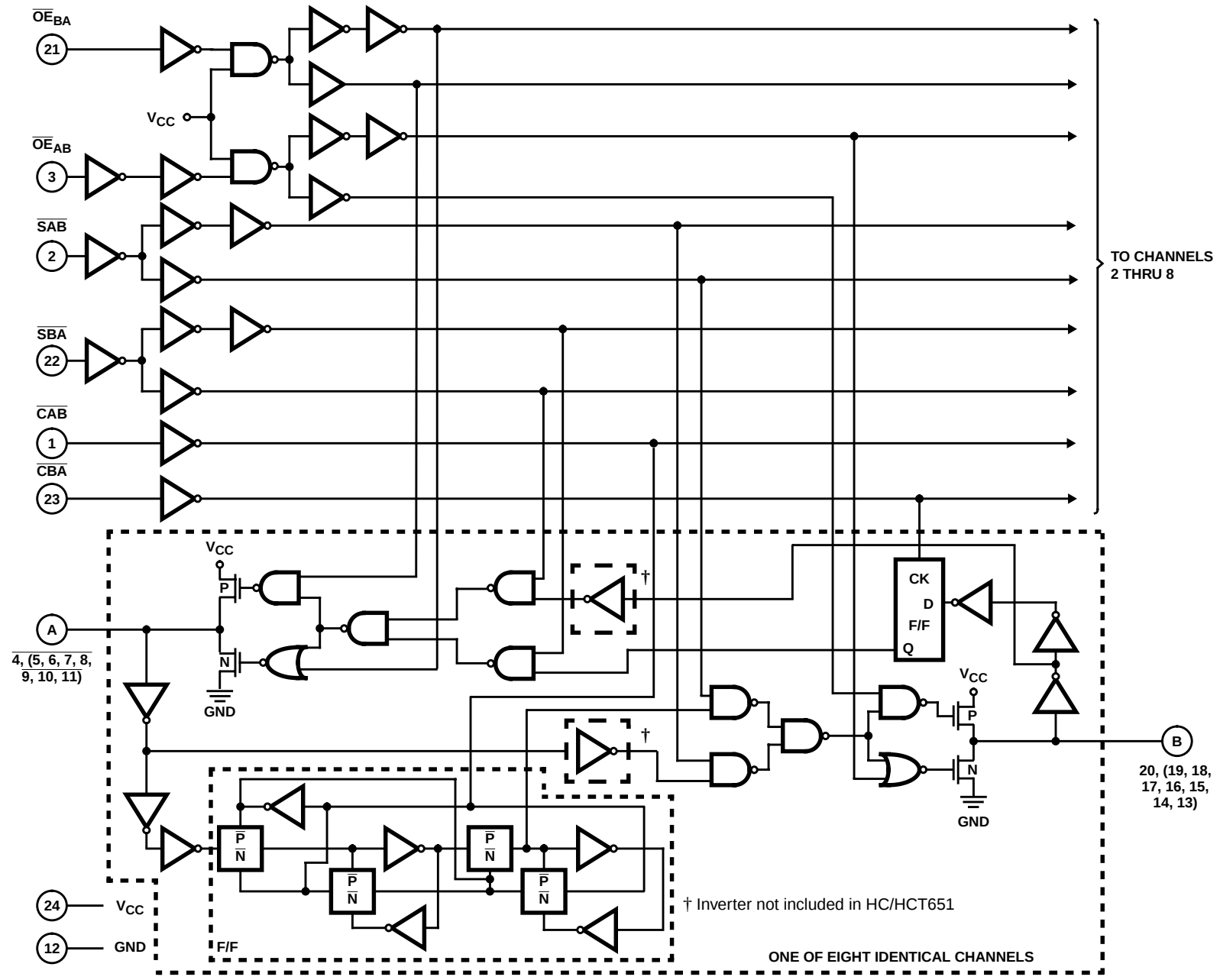


FIGURE 1. LOGIC BLOCK DIAGRAM

CD74HC652, CD74HCT652

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} (Voltages Referenced to Ground)	-0.5V to 7V
DC Input Diode Current, I_{IK} For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Drain Current, I_O For $-0.5V < V_O < V_{CC} + 0.5V$	$\pm 35mA$
DC Output Diode Current, I_{OK} For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^{\circ}C/W$)
EN (PDIP) Package (Note 4)	67
M (SOIC) Package (Note 5)	46
Maximum Junction Temperature (Hermetic Package or Die)	175 $^{\circ}C$
Maximum Junction Temperature (Plastic Package)	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$ (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range, T_A	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types	.2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I , V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- The package thermal impedance is calculated in accordance with JESD 51-3.
- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	V _{IS} (V)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.3	-	0.3	-	0.3	V
				4.5	-	-	0.9	-	0.9	-	0.9	V
				6	-	-	1.2	-	1.2	-	1.2	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V

CD74HC652, CD74HCT652

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	μA
Three- State Leakage Current	V_{IL} or V_{IH}	$V_O = V_{CC}$ or GND	-	6	-	-	± 0.5	-	± 5.0	-	± 10	μA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-	-	± 0.1	-	± 1	-	± 1	μA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Three- State Leakage Current	V_{IL} or V_{IH}	$V_O = V_{CC}$ or GND	-	5.5	-	-	± 0.5	-	± 5.0	-	± 10	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 6)	$V_{CC} - 2.1$	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

- For dual-supply systems theoretical worst case ($V_I = 2.4V$, $V_{CC} = 5.5V$) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
$\overline{OE}_{BA}$	1.3
OE_{AB}	0.75
Clock A to B, B to A	0.6
Select A, Select B	0.45
Inputs A_0 - A_7 , B_0 - B_7	0.3

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360 μA max at 25°C.

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Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
Maximum Clock Frequency	f _{MAX}	2	6	-	-	5	-	-	4	-	-	MHz
		4.5	30	-	-	25	-	-	20	-	-	MHz
		6	35	-	-	29	-	-	23	-	-	MHz
Setup Time Data to Clock	t _{SU}	2	60	-	-	75	-	-	90	-	-	ns
		4.5	12	-	-	15	-	-	18	-	-	ns
		6	10	-	-	13	-	-	15	-	-	ns
Hold Time Data to Clock	t _H	2	35	-	-	45	-	-	55	-	-	ns
		4.5	7	-	-	9	-	-	11	-	-	ns
		6	6	-	-	8	-	-	9	-	-	ns
Clock Pulse Width	t _W	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
HCT TYPES												
Maximum Clock Frequency	f _{MAX}	4.5	25	-	-	20	-	-	17	-	-	MHz
Setup Time Data to Clock	t _{SU}	4.5	12	-	-	15	-	-	18	-	-	ns
Hold Time Data to Clock	t _H	4.5	5	-	-	5	-	-	5	-	-	ns
Clock Pulse Width	t _W	4.5	25	-	-	31	-	-	38	-	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, Store A Data to B Bus Store B Data to A Bus	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	220	-	275	-	300	ns
			4.5	-	-	44	-	55	-	66	ns
			6	-	-	37	-	47	-	5.6	ns
		C _L = 15pF	5	-	18	-	-	-	-	-	ns
Propagation Delay, A Data to B Bus B Data to A Bus	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	135	-	170	-	205	ns
			4.5	-	-	27	-	34	-	41	ns
			6	-	-	23	-	29	-	35	ns
		C _L = 15pF	5	-	12	-	-	-	-	-	ns
Propagation Delay, Select to Data	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	170	-	215	-	255	ns
			4.5	-	-	34	-	43	-	51	ns
			6	-	-	29	-	37	-	43	ns
		C _L = 15pF	5	-	14	-	-	-	-	-	ns

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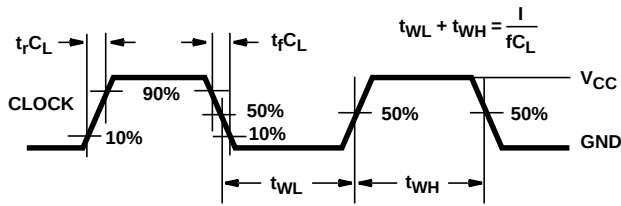
Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Three-State Disabling Time Bus to Output or Register to Output	t_{PLZ}, t_{PHZ}	$C_L = 50\text{pF}$	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
			6	-	-	30	-	37	-	45	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
Three-State Enabling Time Bus to Output or Register to Output	t_{PZL}, t_{PZH}	$C_L = 50\text{pF}$	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
			6	-	-	30	-	37	-	45	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
			6	-	-	10	-	13	-	15	ns
Three-State Output Capacitance	C_O	-	-	-	-	20	-	20	-	20	pF
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Maximum Frequency	f_{MAX}	$C_L = 15\text{pF}$	5	-	60	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 7, 8)	C_{PD}	-	5	-	52	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay, Store A Data to B Bus Store B Data to A Bus	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	44	-	55	-	66	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
Propagation Delay, A Data to B Bus B Data to A Bus	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	37	-	46	-	56	ns
		$C_L = 15\text{pF}$	5	-	15	-	-	-	-	-	ns
Propagation Delay, Select to Data	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	46	-	58	-	69	ns
		$C_L = 15\text{pF}$	5	-	19	-	-	-	-	-	ns
Three-State Disabling Time Bus to Output or Register to Output	t_{PLZ}, t_{PHZ}	$C_L = 50\text{pF}$	4.5	-	-	35	-	44	-	53	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
Three-State Enabling Time Bus to Output or Register to Output	t_{PZL}, t_{PZH}	$C_L = 50\text{pF}$	4.5	-	-	45	-	56	-	68	ns
		$C_L = 15\text{pF}$	5	-	19	-	-	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	4.5	-	-	12	-	15	-	18	ns
Three-State Output Capacitance	C_O	-	-	-	-	20	-	20	-	20	pF
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Maximum Frequency	f_{MAX}	$C_L = 15\text{pF}$	5	-	45	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 7, 8)	C_{PD}	-	5	-	52	-	-	-	-	-	pF

NOTES:

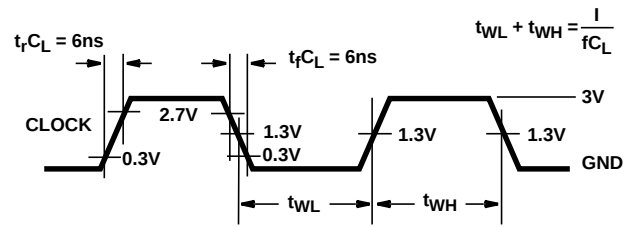
- C_{PD} is used to determine the dynamic power consumption, per package.
- $P_D = V_{CC}^2 C_{PD} f_i + \sum V_{CC}^2 C_L f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 3. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

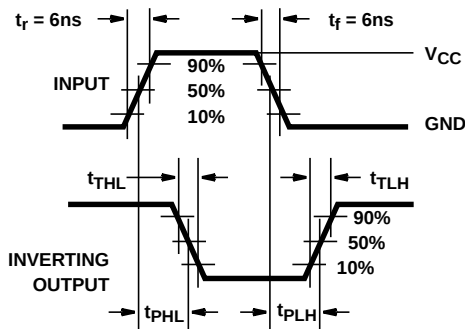


FIGURE 4. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

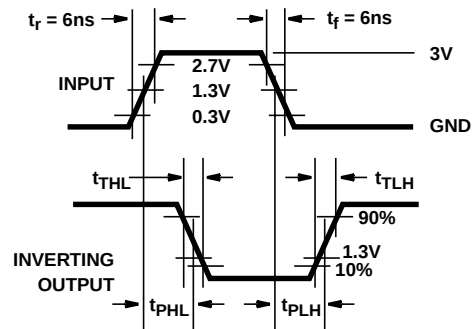


FIGURE 5. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Test Circuits and Waveforms (Continued)

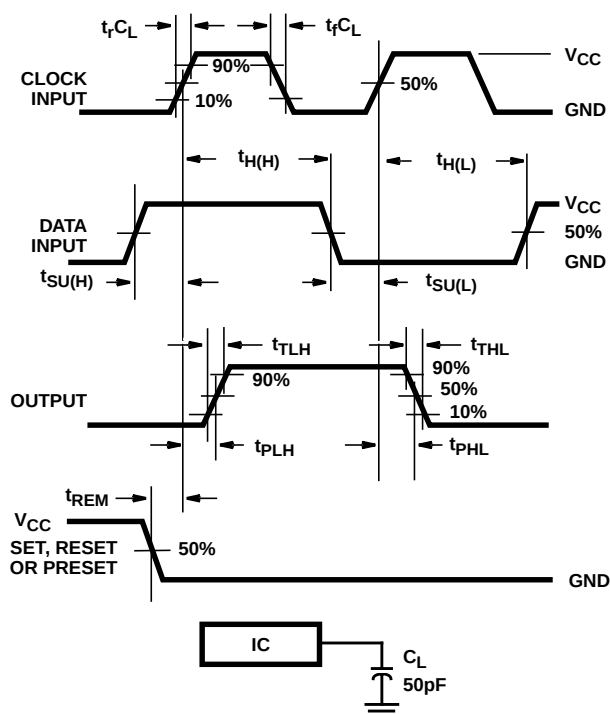


FIGURE 6. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

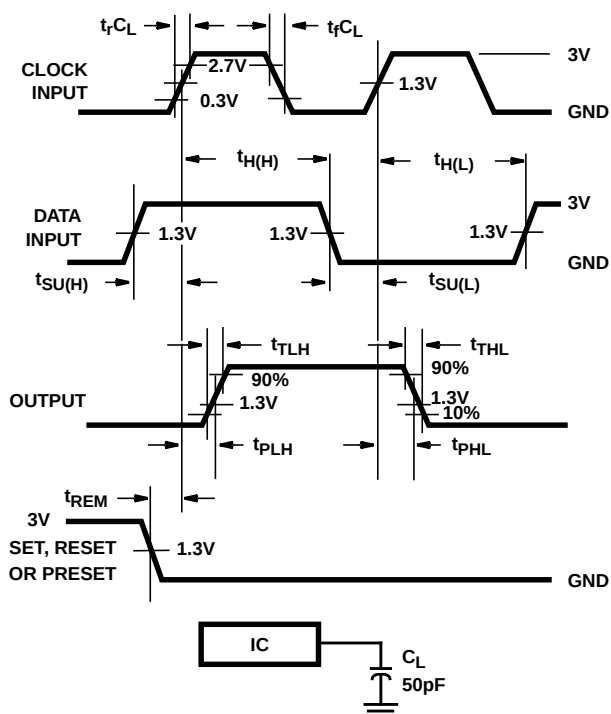


FIGURE 7. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

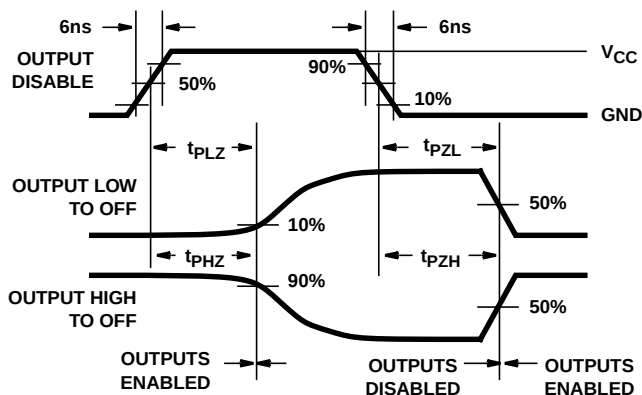


FIGURE 8. HC THREE-STATE PROPAGATION DELAY WAVEFORM

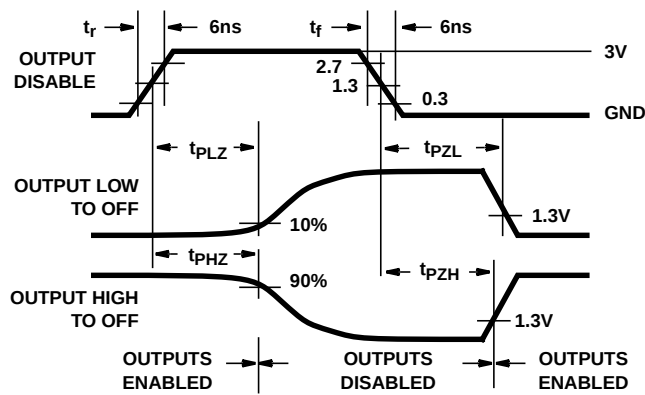
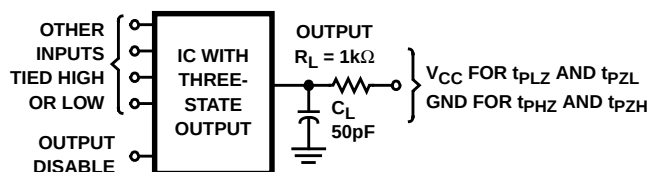


FIGURE 9. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

FIGURE 10. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HCT652M	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT652M
CD74HCT652M.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT652M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE

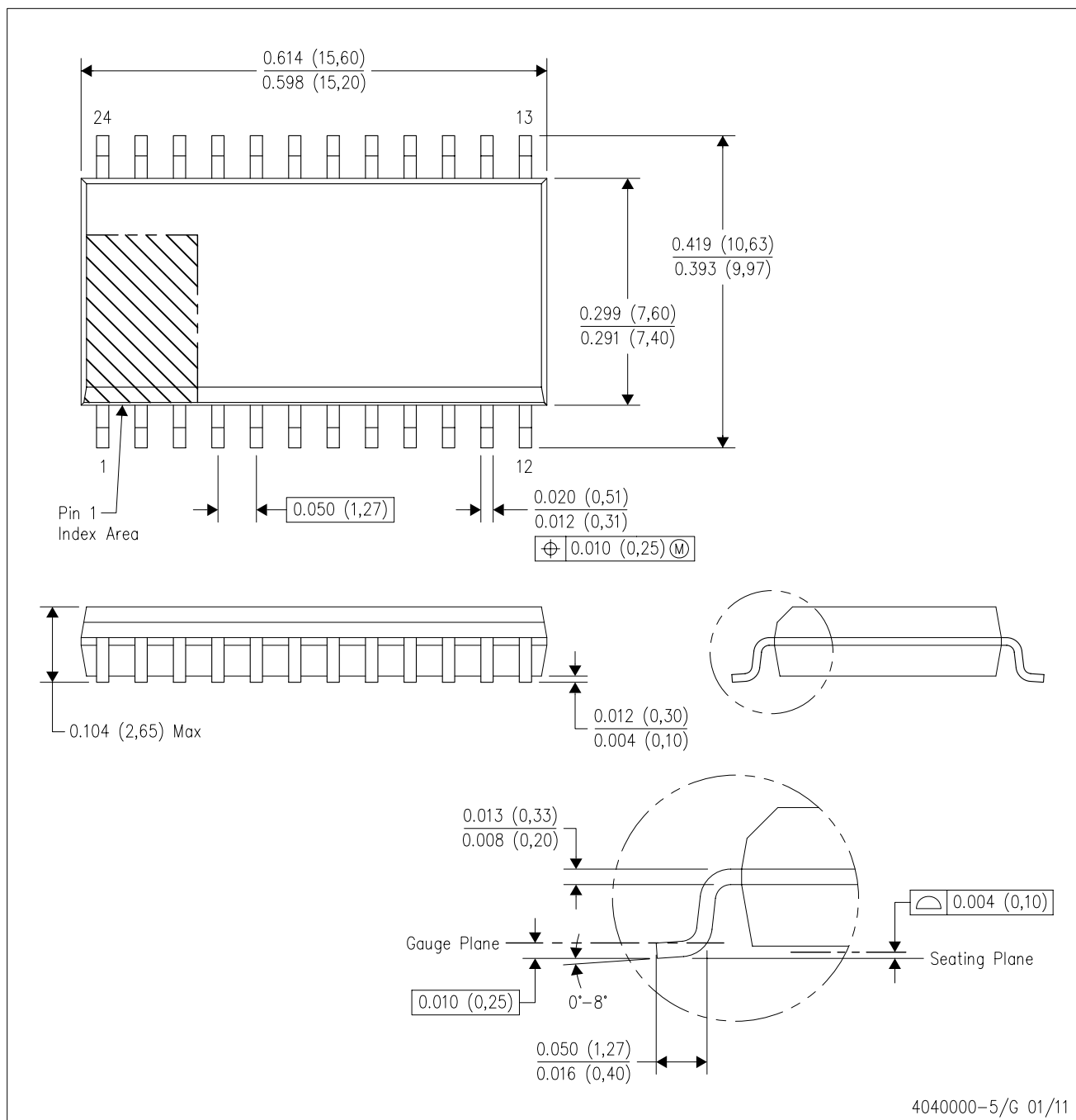


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HCT652M	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD74HCT652M.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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