CD74HC4094-Q1 Automotive High-Speed CMOS Logic 8-Stage Shift and Store Bus Register, Three-State

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Buffered inputs
- Separate serial outputs synchronous to both positive and negative clock edges for cascading
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs

2 Applications

- Increase the number of outputs on a microcontroller
- Store up to 8 bits of data temporarily

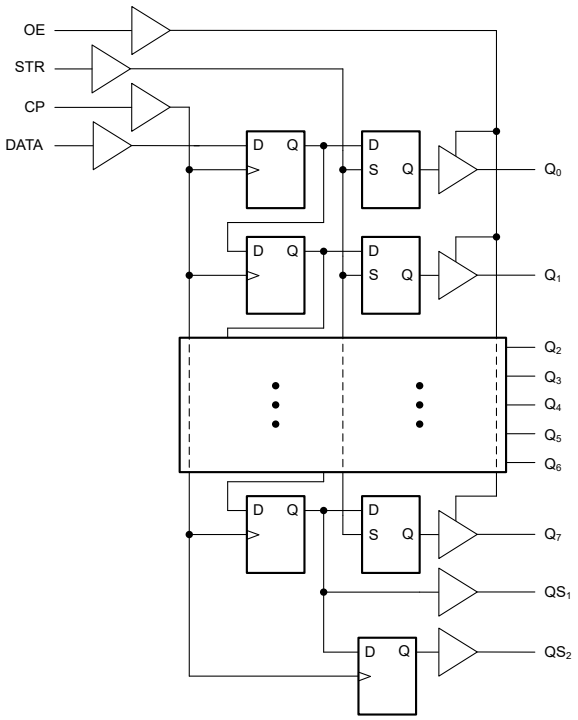
3 Description

The CD74HC4094-Q1 contains 8-stage serial shift registers with a storage latch associated with each stage for strobing data from the serial input to parallel buffered tri-state outputs. The parallel outputs can connect directly to common bus lines. Data shifts on positive clock transitions. When the Strobe input is high, the data in each shift register stage transfers to the storage register. Data in the storage register appears at the outputs when the Output-Enable signal is high.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
CD74HC4094-Q1	PW (TSSOP, 16)	5.00mm × 4.40mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The body size (length × width) is a nominal value and does not include pins.



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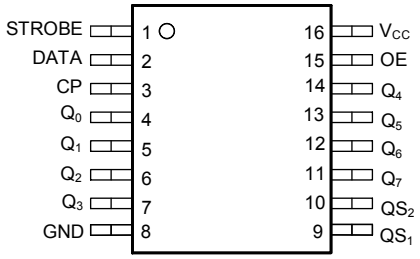


PW package;
16-Pin TSSOP
Top View

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
Strobe	1	I	Strobe input
Data	2	I	Serial data input
CP	3	I	Clock input
Q_0	4	O	Output 0
Q_1	5	O	Output 1
Q_2	6	O	Output 2
Q_3	7	O	Output 3
GND	8	G	Ground
QS_1	9	O	Serial data output 1, rising-edge synchronized
QS_2	10	O	Serial data output 2, falling-edge synchronized
Q_7	11	O	Output 7
Q_6	12	O	Output 6
Q_5	13	O	Output 5
Q_4	14	O	Output 4
OE	15	I	Output enable, active high
V_{CC}	16	P	Positive Supply

(1) I = input, O = output, P = power, G = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp diode current(2)	V_I < -0.5 or V_I > V_{CC} + 0.5V		±20	mA
I_{OK}	Output clamp diode current(2)	V_O < -0.5 or V_O > V_{CC} + 0.5V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
I_{CC}	Continuous output current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C
	Maximum lead temperature (Soldering 10s) (SOIC - lead tips only)			300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings can be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordrance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2		6	V
V_{IH}	High-level input voltage	V_{CC} = 2V	1.5			V
		V_{CC} = 4.5V	3.15			
		V_{CC} = 6V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2V			0.5	V
		V_{CC} = 4.5V			1.35	
		V_{CC} = 6V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Δt/Δv	Input transition rise and fall rate	V_{CC} = 2V			500	ns/V
		V_{CC} = 4.5V			111	
		V_{CC} = 6V			67	
T_A	Ambient temperature		–40		125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
PW (TSSOP)	16	141.2	78.8	85.8	27.7	85.5	—	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range; typical ratings measured at TA = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OH} = -20µA	2V	1.9	1.99		V
				4.5V	4.4	4.49		V
				6V	5.9	5.99		V
			I_{OH} = -6mA, V_{CC} = 4.5V	4.5V	3.84			V
			I_{OH} = -7.8mA, V_{CC} = 6V	6V	5.34			V
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20µA	2V		0.02	0.1	V
				4.5V		0.01	0.1	V
				6V		0.01	0.1	V
			I_{OL} = 6mA	4.5V			0.33	V
			I_{OL} = 7.8mA	6V			0.33	V
I_I	Input leakage current	$V_I = V_{CC}$ or 0		6V			±0.1	µA
I_{OZ}	Off-State (High-Impedance State) Output Current	$V_O = V_{CC}$ or 0, Q_A-Q_H		6V			±1	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0, I_O = 0		6V			5	µA
C_i	Input capacitance			2V to 6V		2		pF
C_O	Output capacitance			2V to 6V		2		pF
C_{pd}	Power dissipation capacitance	No load		2V to 6V		69		pF

5.6 Timing Characteristics

over operating free-air temperature range (unless otherwise noted), C_L = 50pF

PARAMETER			V_{CC}	MIN	MAX	UNIT
t_w	Pulse duration	CP	2V	14		ns
			4.5V	10		
			6V	6		
		STR	2V	14		
			4.5V	10		
			6V	6		
t_{su}	Setup time	DATA before CLK↑	2V	14		ns
			4.5V	10		
			6V	6		
		STROBE before CLK↑	2V	14		
			4.5V	10		
			6V	6		

5.6 Timing Characteristics (continued)

over operating free-air temperature range (unless otherwise noted), C_L = 50pF

PARAMETER			V_{CC}	MIN	MAX	UNIT
t_h	Hold time	DATA after CLK↑	2V	0		ns
			4.5V	0		
			6V	0		
		STROBE after CLK↑	2V	0		
			4.5V	0		
			6V	0		

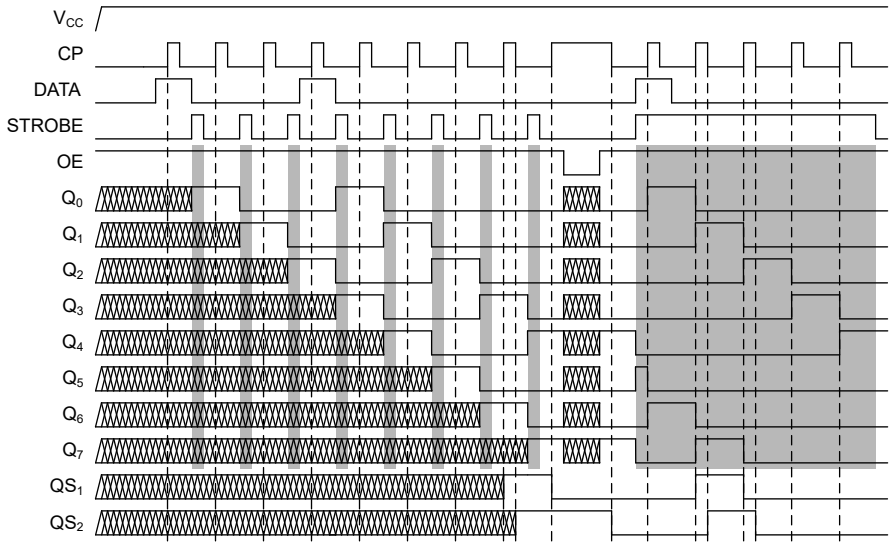


Figure 5-1. Timing Diagram

5.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted), C_L = 50pF

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	Temp	MIN	TYP	MAX	UNIT
f_{max}	Max switching frequency	CP		2V		35	41		MHz
				4.5V		50	69		
				6V		81	83		
t_{pd}	Propagation delay	CP	QS_1	2V				34	ns
				4.5V				19	
				6V				15	
			QS_2	2V				39	
				4.5V				25	
				6V				16	
			Q_N	2V				59	
				4.5V				28	
				6V				22	
		STROBE	Q_N	2V				38	
				4.5V				17	
				6V				14	

5.7 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted), C_L = 50pF

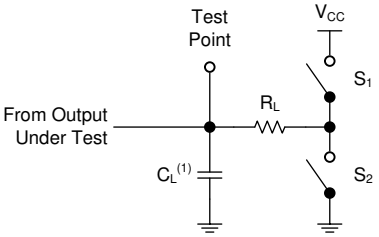
PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	Temp	MIN	TYP	MAX	UNIT
t_{en}	Enable time	OE	Q_N	2V				39	ns
				4.5V				20	
				6V				16	
t_{dis}	Disable time	OE	Q_N	2V				29	ns
				4.5V				21	
				6V				14	
t_t	Transition-time		Any output	2V				75	ns
				4.5V				15	
				6V				13	

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns .

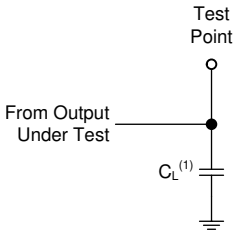
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) C_L includes probe and test-fixture capacitance.

Figure 6-2. Load Circuit for Push-Pull Outputs

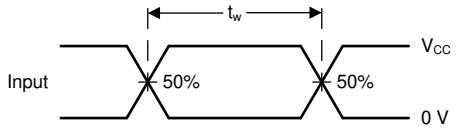


Figure 6-3. Voltage Waveforms, Pulse Duration

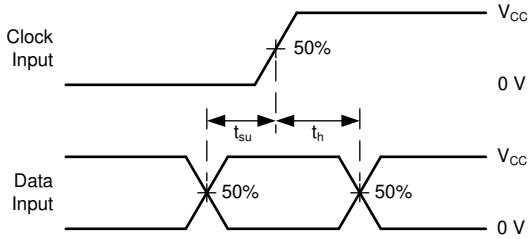
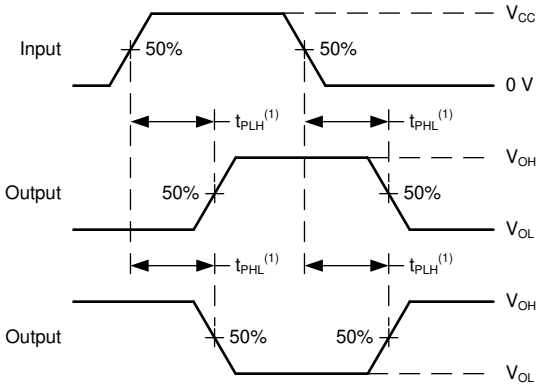


Figure 6-4. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-5. Voltage Waveforms Propagation Delays

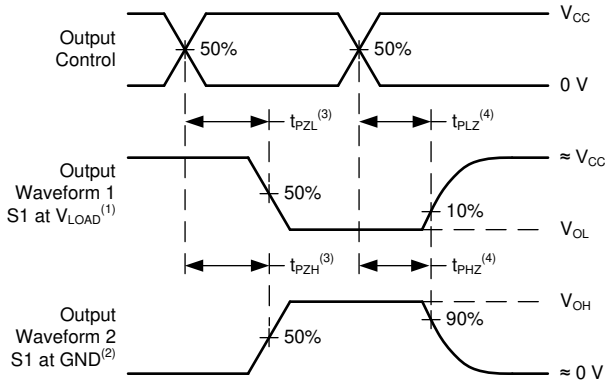
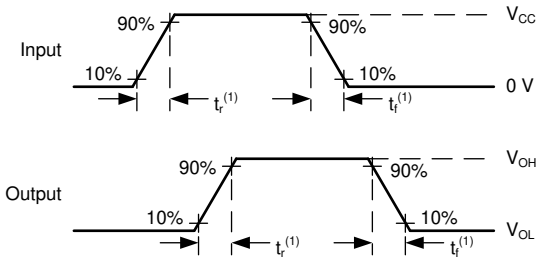


Figure 6-6. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-7. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The CD74HC4094-Q1 contains 8-stage serial shift registers with a storage latch associated with each stage for strobing data from the serial input to parallel buffered tri-state outputs. The parallel outputs can connect directly to common bus lines. Data shifts on positive clock transitions. When the Strobe input is high, the data in each shift register stage transfers to the storage register. Data in the storage register appears at the outputs whenever the Output-Enable signal is high.

Two serial outputs are available for cascading several devices. Data is available at the QS_1 serial output terminal on positive clock edges to allow for high-speed operation in cascaded system in which the clock rise-time is fast. The same serial information, available at the QS_2 terminal on the next negative clock edge, provides a means for cascading these devices when the clock rise-time is slow.

7.2 Feature Description

7.2.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.2.2 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs: driving high, driving low, and high impedance. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without damage. Limit the output power of the device to avoid damage from overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output does not source or sink current except minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the device does not control the output voltage. The output current is dependent on external factors. A floating node is a node that has no other drivers connected, and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while the device is in the high-impedance state. The value of the resistor depends on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor meets these requirements.

Leave unused 3-state CMOS outputs disconnected.

7.2.3 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

7.2.4 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst

case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10kΩ resistor, however, is recommended and typically meets all requirements.

7.2.5 Clamp Diode Structure

As shown in Figure 7-1, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

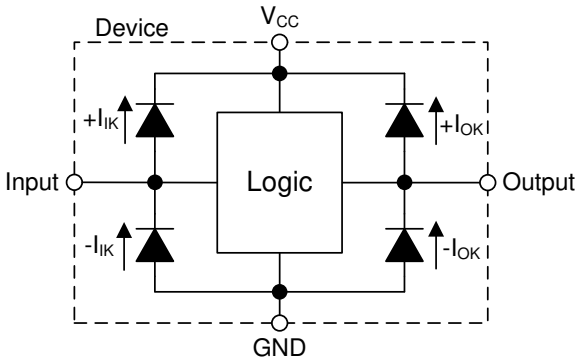


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.2.6 Positive Clamp Diodes

The CD74HC4094-Q1 includes inputs with positive clamp diodes. The positive clamp diodes prevent the input voltage from reaching levels dangerous to the device, holding the input voltage (V_A) to approximately V_{CC} + 0.5V as long as the input clamp current (I_{IK}) does not exceed the maximum limit provided in *Absolute Maximum Ratings*.

The input can draw significant current when the input voltage (V_A) exceeds the supply voltage (V_S) because the diode is forward biased and must be externally limited to avoid damage to the device. Additionally, the input clamp current, I_{IK}, can be several orders of magnitude larger than I_{CC}, resulting in current returning to the supply (the reverse of normal operation) which must be accounted for by the system designer, as shown in Figure 7-2.

A resistor (R) can be used to prevent excessive current on the input as shown in Figure 7-2. The resistor value can be determined with $R \geq (V_{IN} - V_A)/I_{IK(max)}$, with $V_A = V_S + 0.5V$. The system-level input voltage (V_{IN}) may exceed the supply voltage (V_S) because the device input voltage (V_A) is held at approximately V_S + 0.5V by the clamp diode.

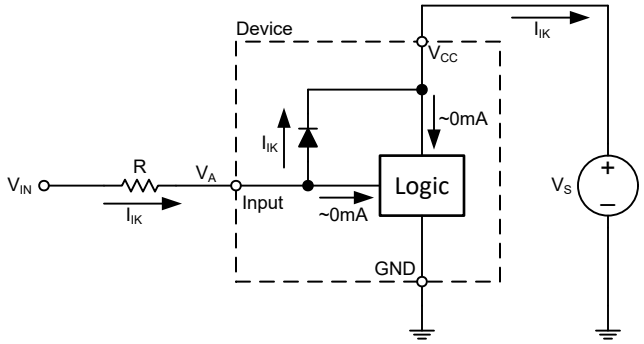
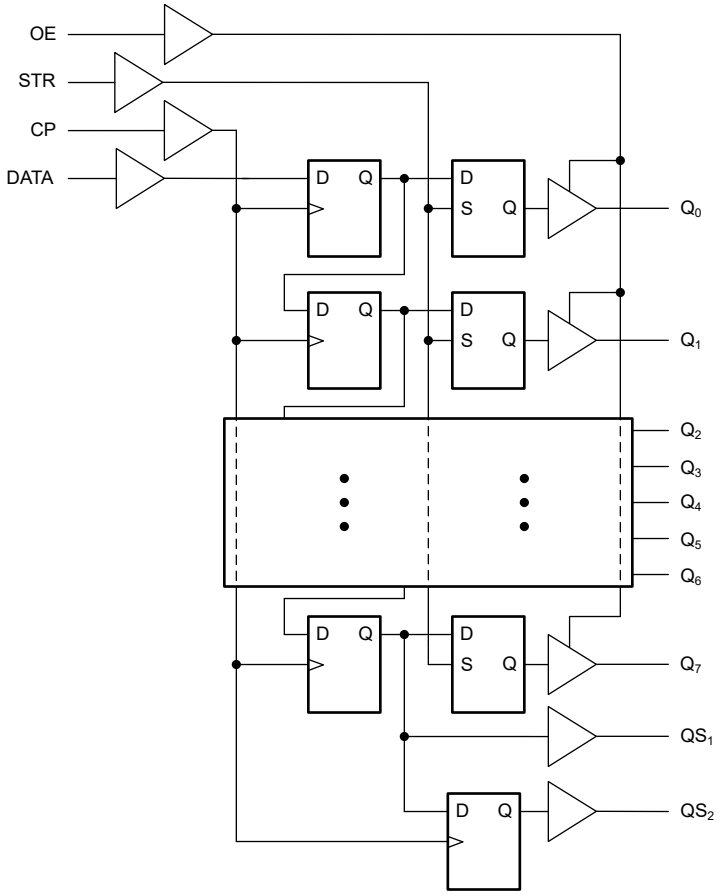


Figure 7-2. Example with resistor to limit input current

7.3 Functional Block Diagram



7.4 Device Functional Modes

Table 7-1. Truth Table

Inputs[1]				Parallel Outputs		Serial Outputs	
CP	OE	STROBE	DATA	Q_0	Q_n	QS_1 [2]	QS_2
↑	L	X	X	Z	Z	Q_6	NC
↓	L	X	X	Z	Z	NC	Q_7
↑	H	L	X	NC	NC	Q_6	NC
↑	H	H	L	L	Q_{n-1}	Q_6	NC
↑	H	H	H	H	Q_{n-1}	Q_6	NC

Table 7-1. Truth Table (continued)

Inputs[1]				Parallel Outputs		Serial Outputs	
CP	OE	STROBE	DATA	Q_0	Q_n	QS_1 [2]	QS_2
↓	H	H	H	NC	NC	NC	Q_7

(1) H = High voltage level, L = Low voltage level, X = Don't care, NC = No change, Z = High-impedance, ↑ = Transition from low-to-high level, ↓ = Transition from high to low.
(2) At the positive clock edge the information in the seventh register stage transfers to the eighth register stage and QS_1 output.

8 Application and Implementation

8.1 Application Information

The CD74HC4094-Q1 can be used to drive signals over relatively long traces or transmission lines. A series damping resistor placed in series with the transmitter's output can be used to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

8.2 Typical Application

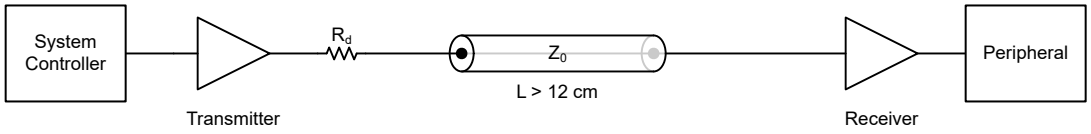


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CD74HC4094-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Verify that the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the CD74HC4094-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The CD74HC4094-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied; however, TI recommends adding a series resistor between the output and capacitor to prevent excessive current.

The CD74HC4094-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the CD74HC4094-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The CD74HC4094-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the Electrical Characteristics table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that can be in opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.1.4 Application Curve

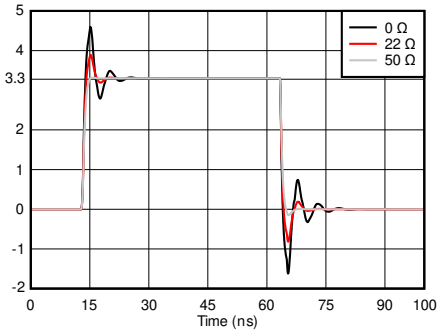


Figure 8-2. Simulated Signal Integrity at the Receiver with Different Damping Resistor (R_d) Values

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance.

A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

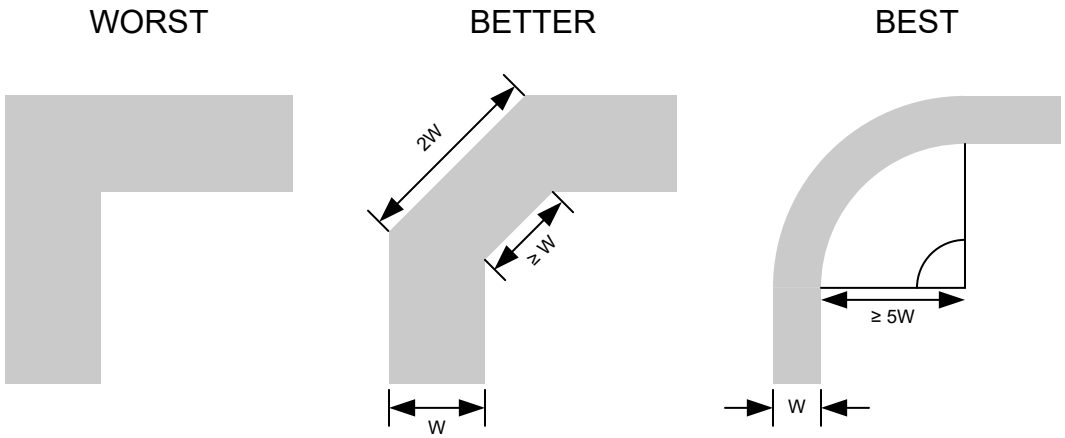


Figure 8-3. Example Trace Corners for Improved Signal Integrity

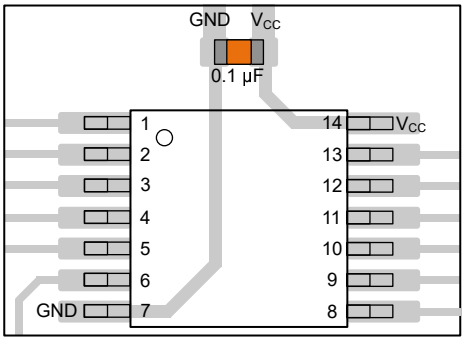


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

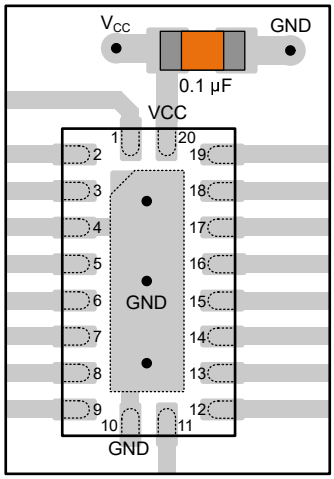


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

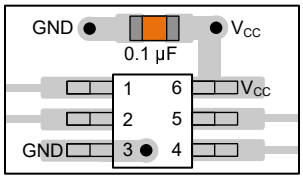


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

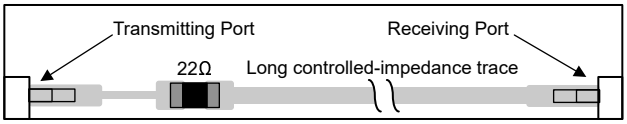


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC4094PWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	HJ4094Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD74HC4094-Q1 :

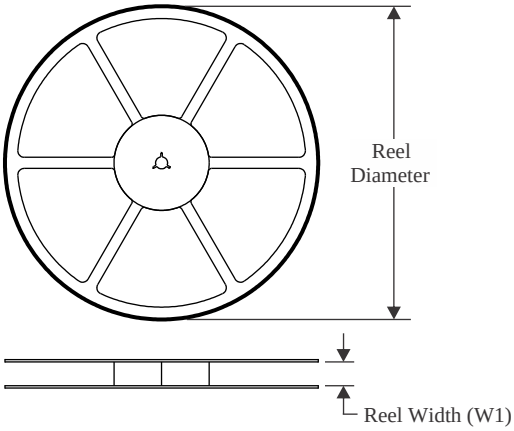
- Catalog : CD74HC4094
- Military : CD54HC4094

NOTE: Qualified Version Definitions:

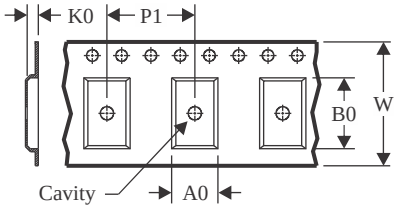
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

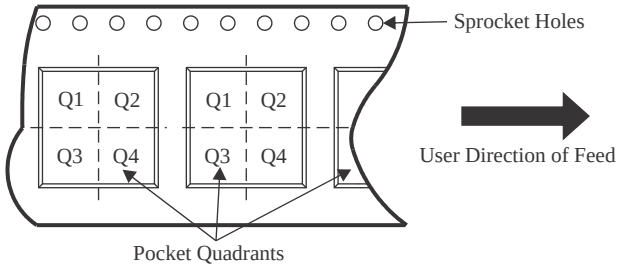


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

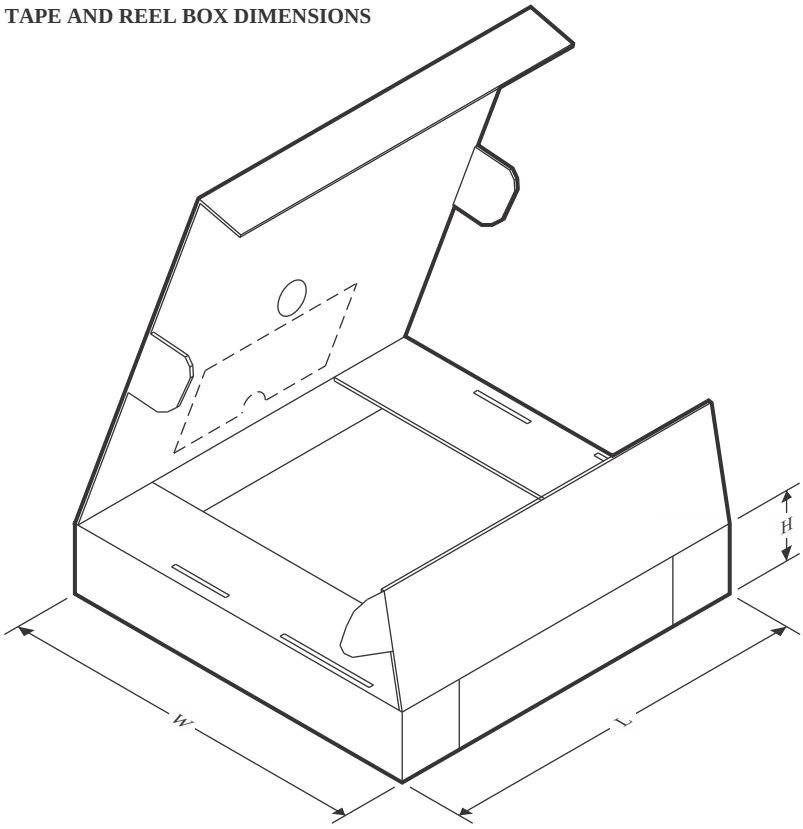
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4094PWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

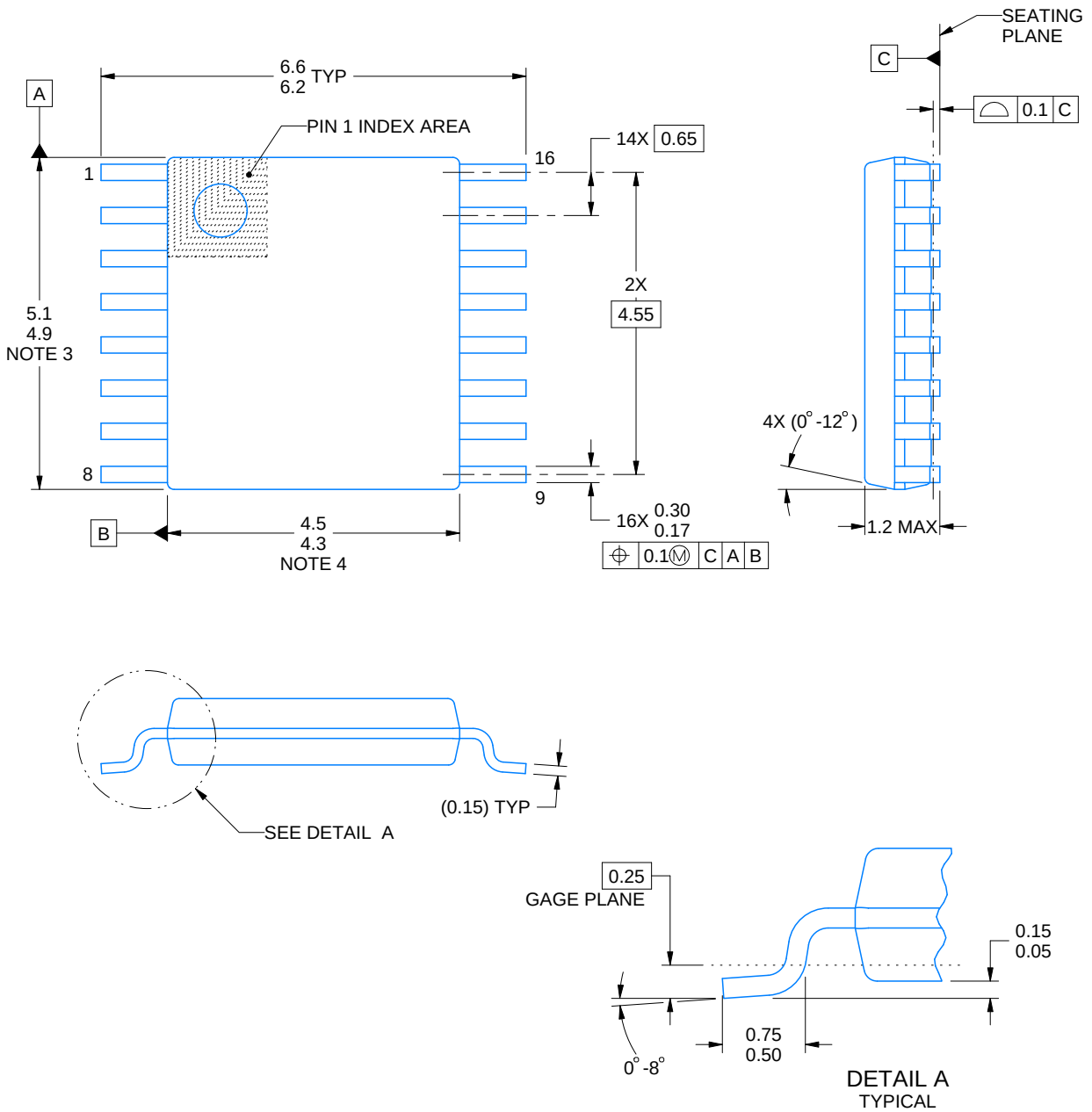
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4094PWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

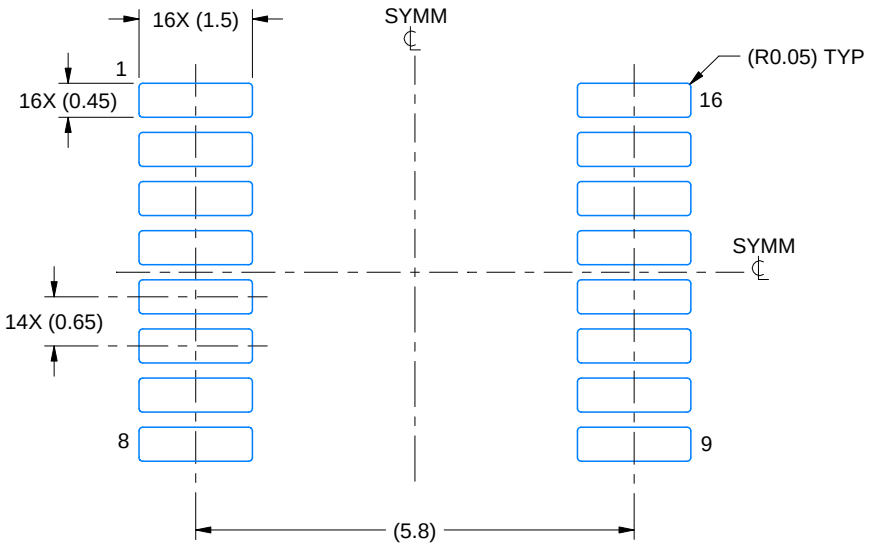
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



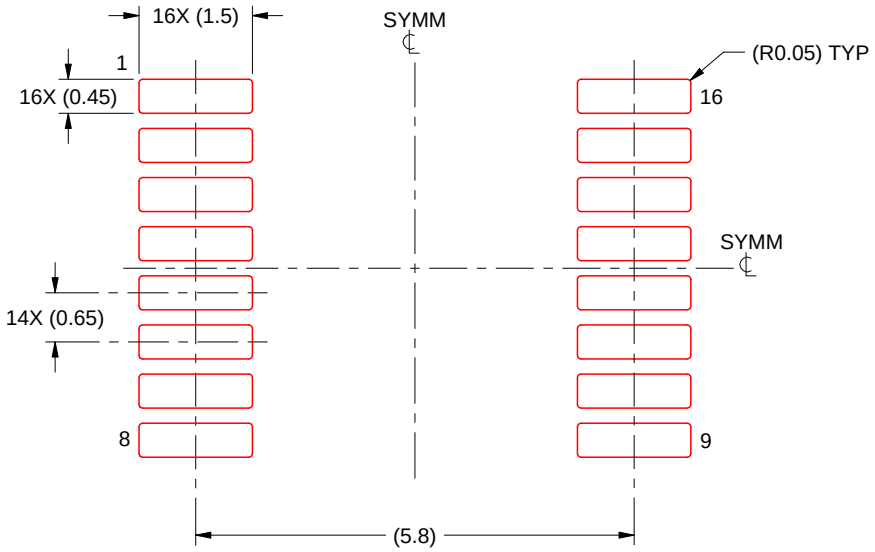
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025