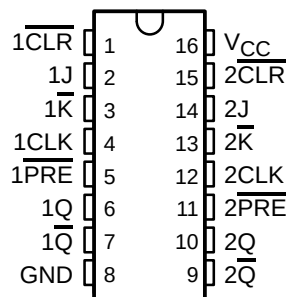


# CD54ACT109, CD74ACT109 DUAL J- $\bar{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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- Inputs Are TTL-Voltage Compatible
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- $\pm 24$ -mA Output Drive Current
  - Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54ACT109 . . . F PACKAGE  
CD74ACT109 . . . E OR M PACKAGE  
(TOP VIEW)



## description/ordering information

The 'ACT109 devices contain two independent J- $\bar{K}$  positive-edge-triggered flip-flops. A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the J and  $\bar{K}$  inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and  $\bar{K}$  inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding  $\bar{K}$  and tying J high. They also can perform as D-type flip-flops if J and  $\bar{K}$  are tied together.

## ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE† |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------|---------------|-----------------------|------------------|
| –55°C to 125°C | PDIP – E | Tube          | CD74ACT109E           | CD74ACT109E      |
|                | SOIC – M | Tube          | CD74ACT109M           | ACT109M          |
|                |          | Tape and reel | CD74ACT109M96         |                  |
|                | CDIP – F | Tube          | CD54ACT109F3A         | CD54ACT109F3A    |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each flip-flop)

| INPUTS           |                  |     |   |           | OUTPUTS |             |
|------------------|------------------|-----|---|-----------|---------|-------------|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | J | $\bar{K}$ | Q       | $\bar{Q}$   |
| L                | H                | X   | X | X         | H       | L           |
| H                | L                | X   | X | X         | L       | H           |
| L                | L                | X   | X | X         | H†      | H†          |
| H                | H                | ↑   | L | L         | L       | H           |
| H                | H                | ↑   | H | L         | Toggle  |             |
| H                | H                | ↑   | L | H         | Q0      | $\bar{Q}$ 0 |
| H                | H                | ↑   | H | H         | H       | L           |
| H                | H                | L   | X | X         | Q0      | $\bar{Q}$ 0 |

† Unpredictable and unstable condition if both  $\overline{PRE}$  and  $\overline{CLR}$  go high simultaneously after both being low at the same time



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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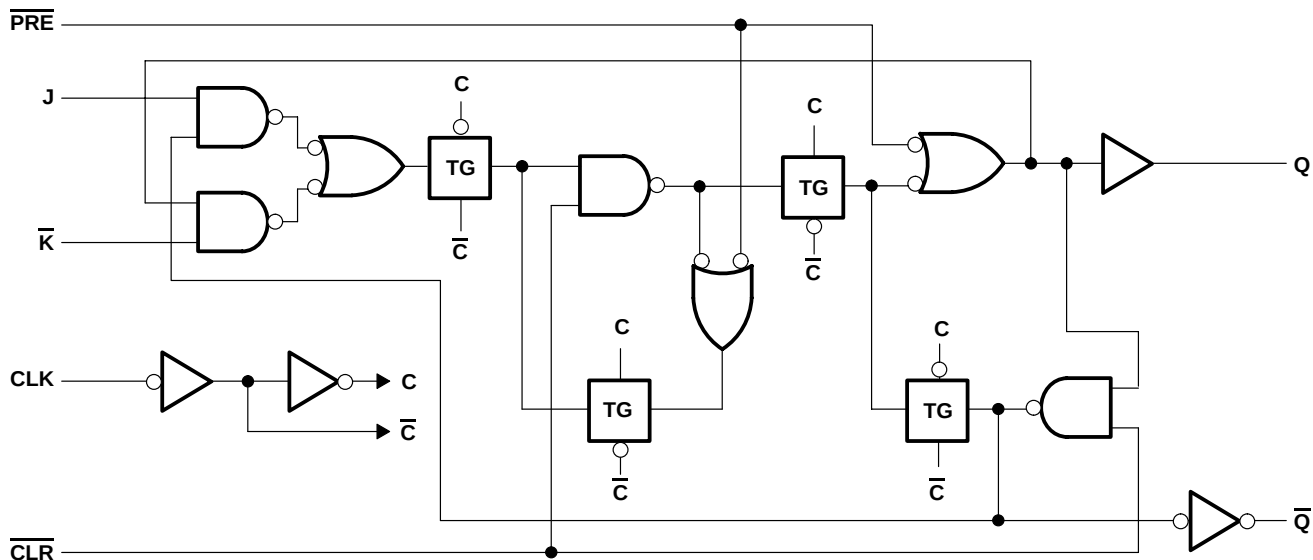
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# CD54ACT109, CD74ACT109

## DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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### logic diagram, each flip-flop (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                               |                |
|-------------------------------------------------------------------------------|----------------|
| Supply voltage range, $V_{CC}$                                                | –0.5 V to 6 V  |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ V or $V_I > V_{CC}$ ) (see Note 1)  | ±20 mA         |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ V or $V_O > V_{CC}$ ) (see Note 1) | ±50 mA         |
| Continuous output current, $I_O$ ( $V_O > 0$ V or $V_O < V_{CC}$ )            | ±50 mA         |
| Continuous current through $V_{CC}$ or GND                                    | ±100 mA        |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): E package              | 67°C/W         |
| M package                                                                     | 73°C/W         |
| Storage temperature range, $T_{stg}$                                          | –65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

|                                                        | $T_A = 25^\circ\text{C}$ |          | –55°C to 125°C |          | –40°C to 85°C |          | UNIT |
|--------------------------------------------------------|--------------------------|----------|----------------|----------|---------------|----------|------|
|                                                        | MIN                      | MAX      | MIN            | MAX      | MIN           | MAX      |      |
| $V_{CC}$ Supply voltage                                | 4.5                      | 5.5      | 4.5            | 5.5      | 4.5           | 5.5      | V    |
| $V_{IH}$ High-level input voltage                      | 2                        |          | 2              |          | 2             |          | V    |
| $V_{IL}$ Low-level input voltage                       |                          | 0.8      |                | 0.8      |               | 0.8      | V    |
| $V_I$ Input voltage                                    | 0                        | $V_{CC}$ | 0              | $V_{CC}$ | 0             | $V_{CC}$ | V    |
| $V_O$ Output voltage                                   | 0                        | $V_{CC}$ | 0              | $V_{CC}$ | 0             | $V_{CC}$ | V    |
| $I_{OH}$ High-level output current                     |                          | –24      |                | –24      |               | –24      | mA   |
| $I_{OL}$ Low-level output current                      |                          | 24       |                | 24       |               | 24       | mA   |
| $\Delta t/\Delta v$ Input transition rise or fall rate |                          | 10       |                | 10       |               | 10       | ns/V |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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# CD54ACT109, CD74ACT109

## DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

### WITH CLEAR AND PRESET

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                     | TEST CONDITIONS                                             |                                       | V <sub>CC</sub> | T <sub>A</sub> = 25°C |      | –55°C to 125°C |      | –40°C to 85°C |      | UNIT |
|-------------------------------|-------------------------------------------------------------|---------------------------------------|-----------------|-----------------------|------|----------------|------|---------------|------|------|
|                               |                                                             |                                       |                 | MIN                   | MAX  | MIN            | MAX  | MIN           | MAX  |      |
| V <sub>OH</sub>               | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>         | I <sub>OH</sub> = –50 µA              | 4.5 V           | 4.4                   |      | 4.4            |      | 4.4           |      | V    |
|                               |                                                             | I <sub>OH</sub> = –24 mA              | 4.5 V           | 3.94                  |      | 3.7            |      | 3.8           |      |      |
|                               |                                                             | I <sub>OH</sub> = –50 mA <sup>†</sup> | 5.5 V           |                       |      | 3.85           |      |               |      |      |
|                               |                                                             | I <sub>OH</sub> = –75 mA <sup>†</sup> | 5.5 V           |                       |      |                |      | 3.85          |      |      |
| V <sub>OL</sub>               | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>         | I <sub>OL</sub> = 50 µA               | 4.5 V           |                       | 0.1  |                | 0.1  |               | 0.1  | V    |
|                               |                                                             | I <sub>OL</sub> = 24 mA               | 4.5 V           |                       | 0.36 |                | 0.5  |               | 0.44 |      |
|                               |                                                             | I <sub>OL</sub> = 50 mA <sup>†</sup>  | 5.5 V           |                       |      |                | 1.65 |               |      |      |
|                               |                                                             | I <sub>OL</sub> = 75 mA <sup>†</sup>  | 5.5 V           |                       |      |                |      |               | 1.65 |      |
| I <sub>I</sub>                | V <sub>I</sub> = V <sub>CC</sub> or GND                     |                                       | 5.5 V           |                       | ±0.1 |                | ±1   |               | ±1   | µA   |
| I <sub>CC</sub>               | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 |                                       | 5.5 V           |                       | 4    |                | 80   |               | 40   | µA   |
| ΔI <sub>CC</sub> <sup>‡</sup> | V <sub>I</sub> = V <sub>CC</sub> – 2.1 V                    |                                       | 4.5 V to 5.5 V  |                       | 2.4  |                | 3    |               | 2.8  | mA   |
| C <sub>i</sub>                |                                                             |                                       |                 |                       | 10   |                | 10   |               | 10   | pF   |

<sup>†</sup> Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

<sup>‡</sup> Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

**ACT INPUT LOAD TABLE**

| INPUT      | UNIT LOAD |
|------------|-----------|
| J or CLK   | 1         |
| K          | 0.53      |
| CLR or PRE | 0.58      |

Unit Load is ΔI<sub>CC</sub> limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

**timing requirements over recommended operating conditions (unless otherwise noted)**

|                    |                            |                 | –55°C to 125°C |     | –40°C to 85°C |     | UNIT |
|--------------------|----------------------------|-----------------|----------------|-----|---------------|-----|------|
|                    |                            |                 | MIN            | MAX | MIN           | MAX |      |
| f <sub>clock</sub> | Clock frequency            |                 |                | 100 |               | 114 | MHz  |
| t <sub>w</sub>     | Pulse duration             | CLK high or low |                | 5   |               | 4.4 | ns   |
|                    |                            | CLR or PRE low  |                | 5.5 |               | 4.8 |      |
| t <sub>su</sub>    | Setup time, before CLK↑    | J or K          |                | 5.5 |               | 4.8 | ns   |
| t <sub>h</sub>     | Hold time, after CLK↑      | J or K          |                | 0   |               | 0   | ns   |
| t <sub>rec</sub>   | Recovery time, before CLK↑ | CLR↑ or PRE↑    |                | 2.5 |               | 2.2 | ns   |



**CD54ACT109, CD74ACT109**  
**DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS**  
**WITH CLEAR AND PRESET**

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

| PARAMETER  | FROM<br>(INPUT)                                    | TO<br>(OUTPUT) | –55°C to<br>125°C |      | –40°C to<br>85°C |      | UNIT |
|------------|----------------------------------------------------|----------------|-------------------|------|------------------|------|------|
|            |                                                    |                | MIN               | MAX  | MIN              | MAX  |      |
| $f_{\max}$ |                                                    |                | 100               |      | 114              |      | MHz  |
| $t_{PLH}$  | CLK                                                | Q or $\bar{Q}$ | 2.6               | 10.3 | 2.7              | 9.4  | ns   |
|            | $\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ |                | 3.1               | 12.2 | 3.2              | 11.1 |      |
| $t_{PHL}$  | CLK                                                | Q or $\bar{Q}$ | 2.6               | 10.3 | 2.7              | 9.4  | ns   |
|            | $\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ |                | 3.1               | 12.2 | 3.2              | 11.1 |      |

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

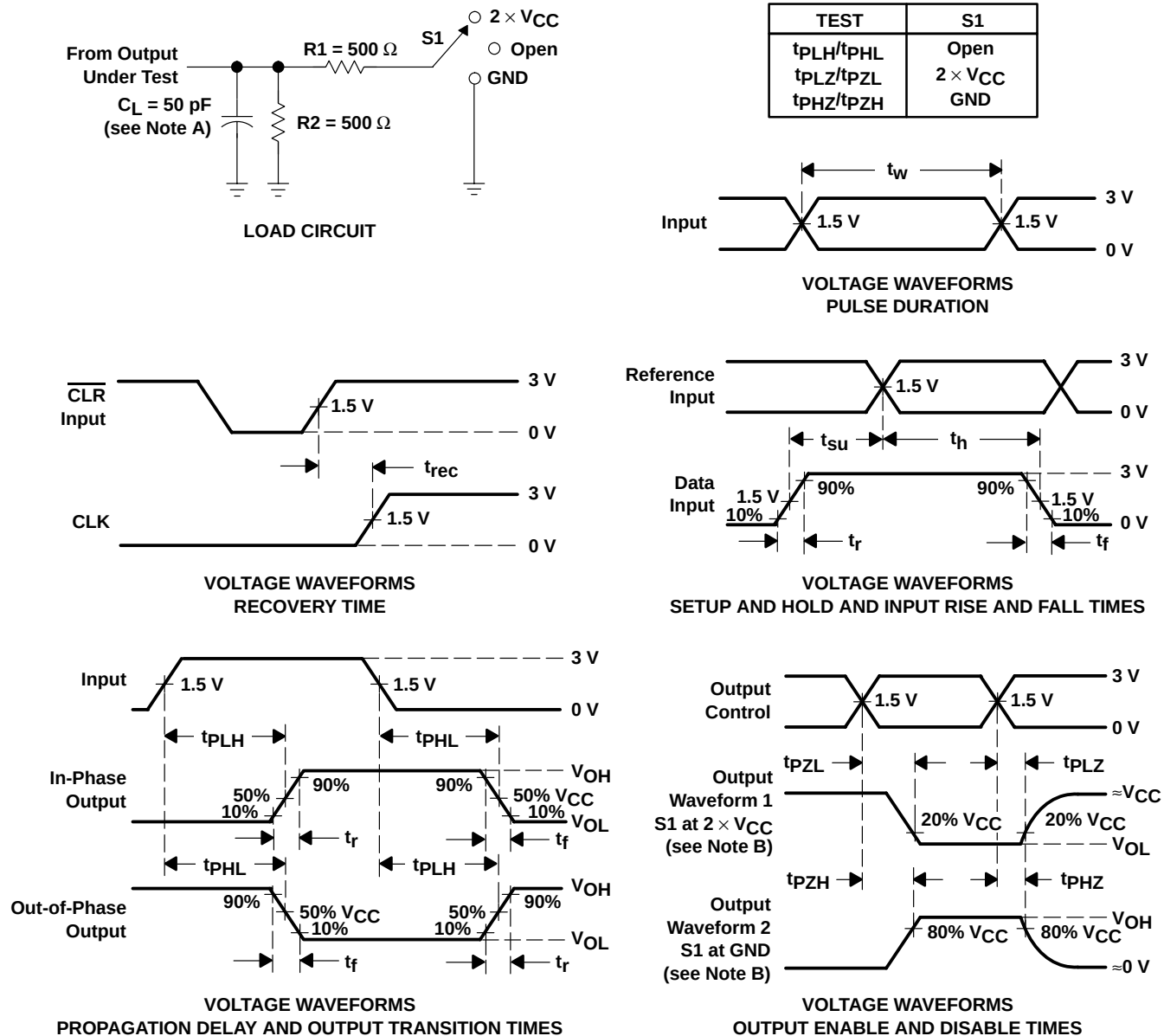
| PARAMETER |                               | TYP | UNIT |
|-----------|-------------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | 56  | pF   |



# CD54ACT109, CD74ACT109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ . Phase relationships between waveforms are arbitrary.
  - For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
  - The outputs are measured one at a time with one input transition per measurement.
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CD54ACT109F3A</a> | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54ACT109F3A       |
| CD54ACT109F3A.A               | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54ACT109F3A       |
| <a href="#">CD74ACT109E</a>   | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74ACT109E         |
| CD74ACT109E.A                 | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74ACT109E         |
| <a href="#">CD74ACT109M</a>   | Obsolete      | Production           | SOIC (D)   16  | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | ACT109M             |
| <a href="#">CD74ACT109M96</a> | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | ACT109M             |
| CD74ACT109M96.A               | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | ACT109M             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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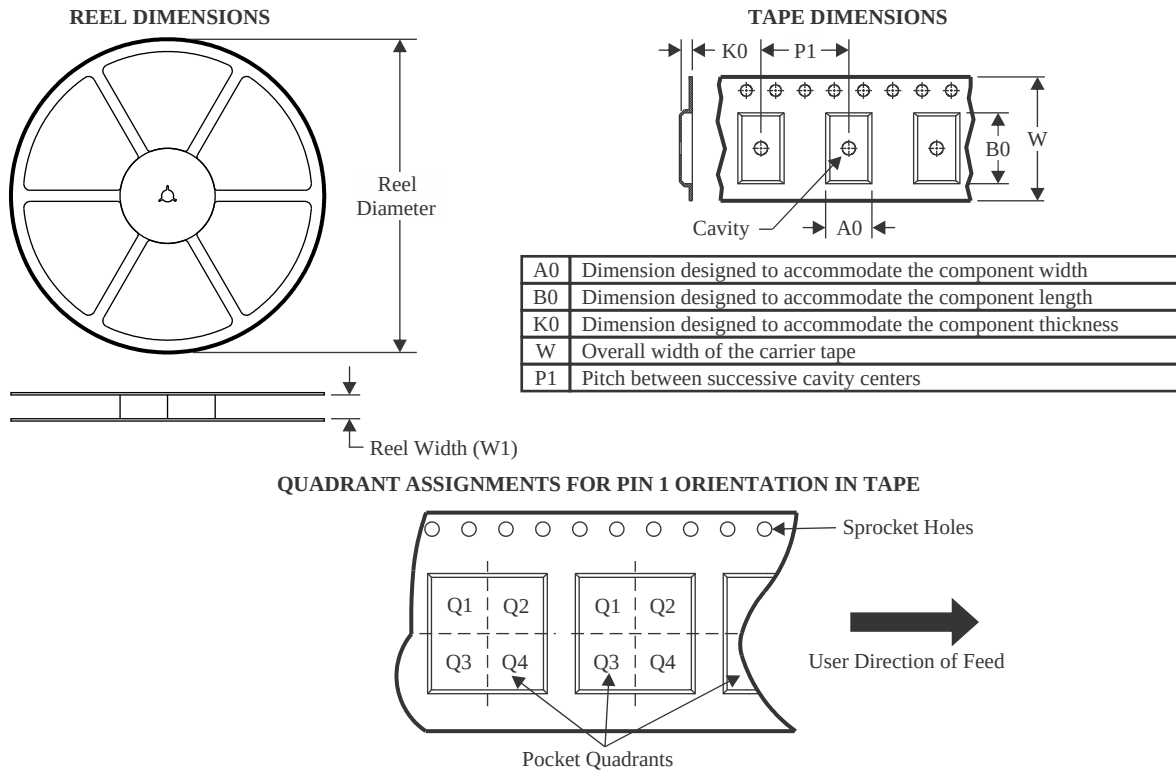
**OTHER QUALIFIED VERSIONS OF CD54ACT109, CD74ACT109 :**

- Catalog : [CD74ACT109](#)
- Military : [CD54ACT109](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

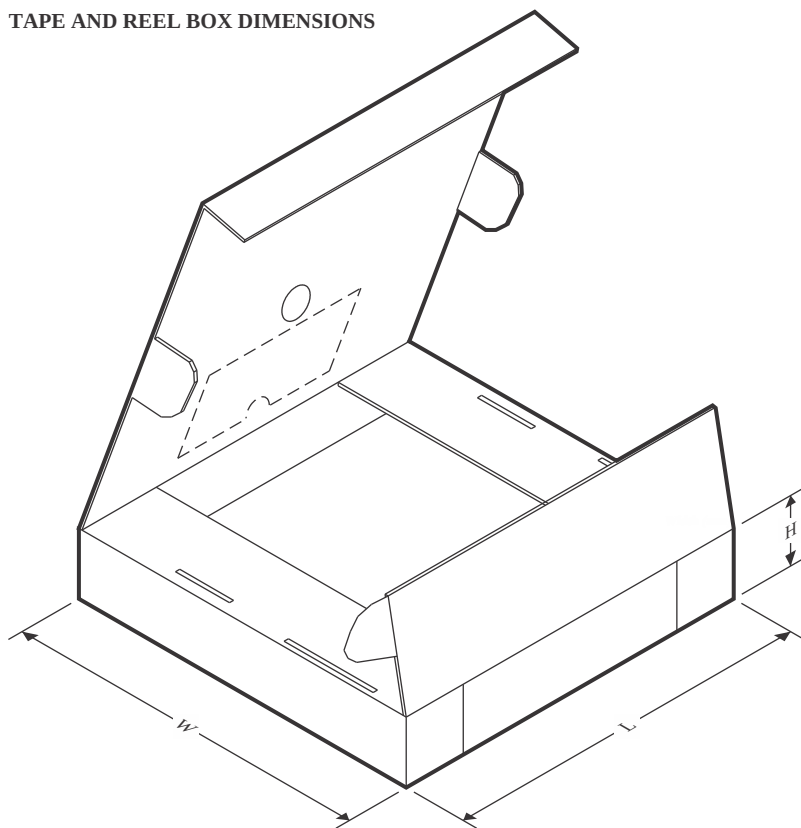


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74ACT109M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |

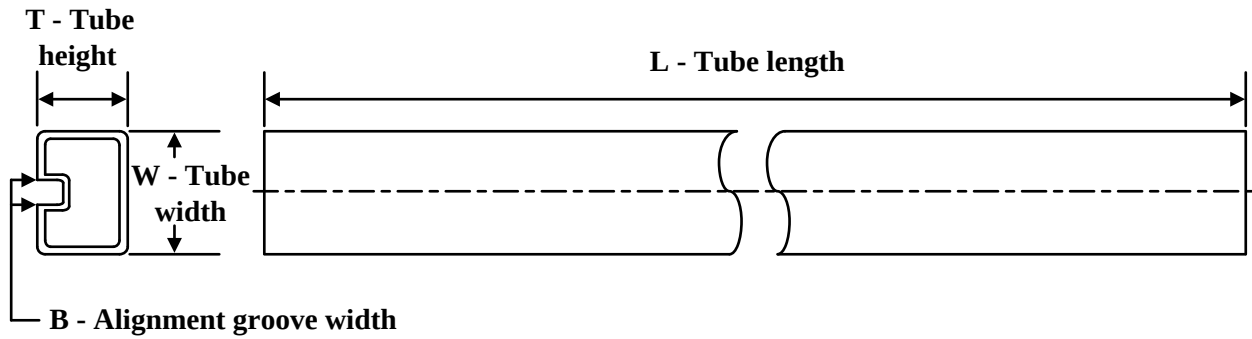


## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74ACT109M96 | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |

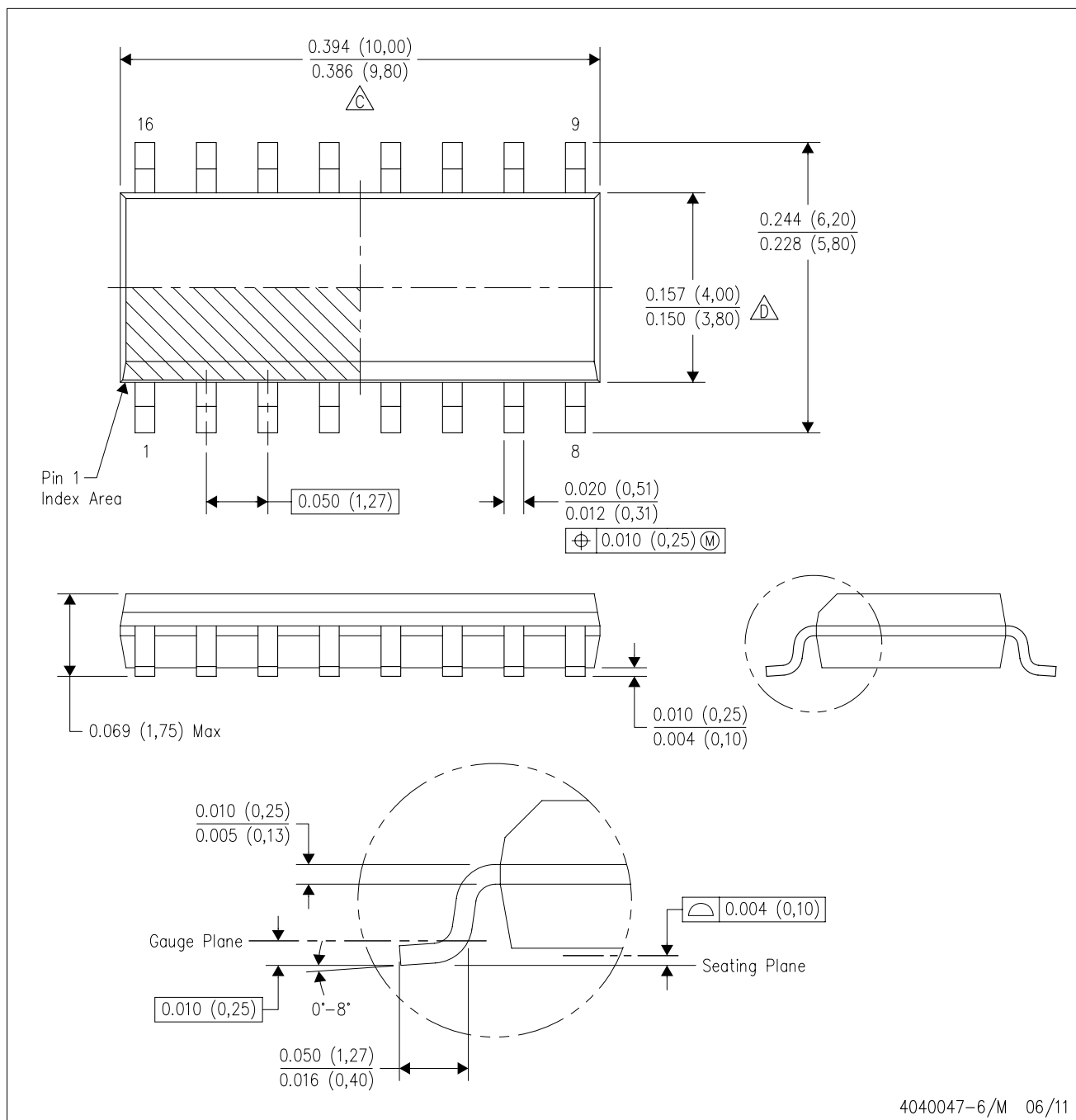
**TUBE**


\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74ACT109E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74ACT109E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74ACT109E.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74ACT109E.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

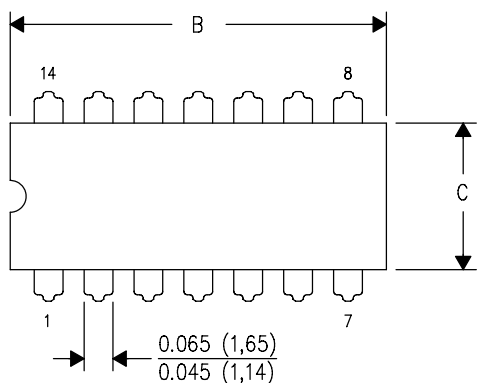
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

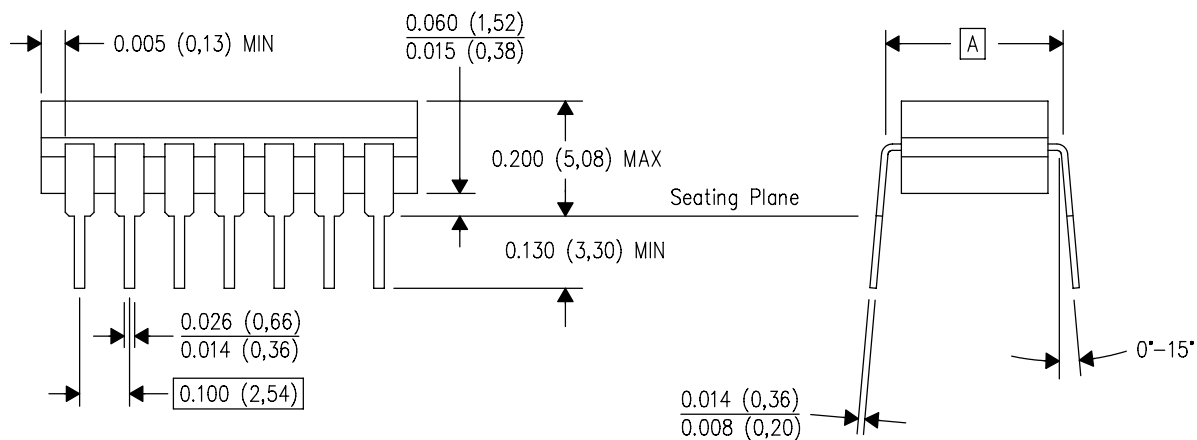
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



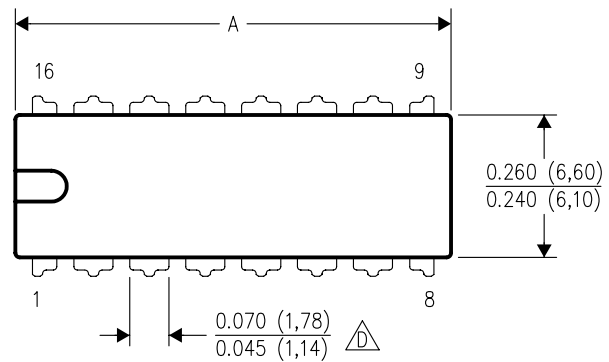
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

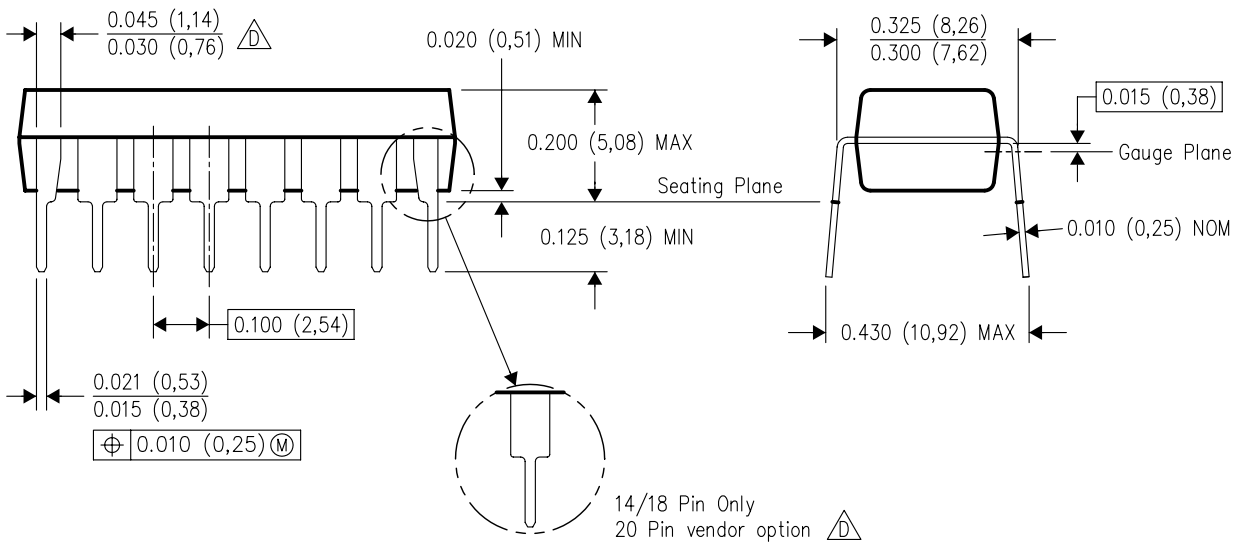
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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