

CMOS Programmable Timer High Voltage Types (20V Rating)

Features

- Low Symmetrical Output Resistance, Typically 100Ω at V_{DD} = 15V
- Built-In Low-Power RC Oscillator
- Oscillator Frequency Range DC to 100kHz
- External Clock (Applied to Pin 3) can be Used Instead of Oscillator
- Operates as 2^N Frequency Divider or as a Single-Transition Timer
- Q/Q̄ Select Provides Output Logic Level Flexibility
- AUTO or MASTER RESET Disables Oscillator During Reset to Reduce Power Dissipation
- Operates With Very Slow Clock Rise and Fall Times
- Capable of Driving Six Low Power TTL Loads, Three Low-Power Schottky Loads, or Six HTL Loads Over the Rated Temperature Range
- Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- 5V, 10V, and 15V Parametric Ratings
- Meets All Requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Description

CD4541B programmable timer consists of a 16-stage binary counter, an oscillator that is controlled by external R-C components (2 resistors and a capacitor), an automatic power-on reset circuit, and output control logic. The counter increments on positive-edge clock transitions and can also be reset via the MASTER RESET input.

The output from this timer is the Q or Q̄ output from the 8th, 10th, 13th, or 16th counter stage. The desired stage is chosen using time-select inputs A and B (see Frequency Select Table).

The output is available in either of two modes selectable via the MODE input, pin 10 (see Truth Table). When this MODE input is a logic "1", the output will be a continuous square wave having a frequency equal to the oscillator frequency divided by 2^N. With the MODE input set to logic "0" and after a MASTER RESET is initiated, the output (assuming Q output has been selected) changes from a low to a high state after 2^{N-1} counts and remains in that state until another MASTER RESET pulse is applied or the MODE input is set to a logic "1".

Timing is initialized by setting the AUTO RESET input (pin 5) to logic "0" and turning power on. If pin 5 is set to logic "1", the AUTO RESET circuit is disabled and counting will not start until after a positive MASTER RESET pulse is applied and returns to a low level. The AUTO RESET consumes an appreciable amount of power and should not be used if low-power operation is desired. For reliable automatic power-on reset, V_{DD} should be greater than 5V.

The RC oscillator, shown in Figure 2, oscillates with a frequency determined by the RC network and is calculated using:

$$f = \frac{1}{2.3 R_{TC} C_{TC}}$$

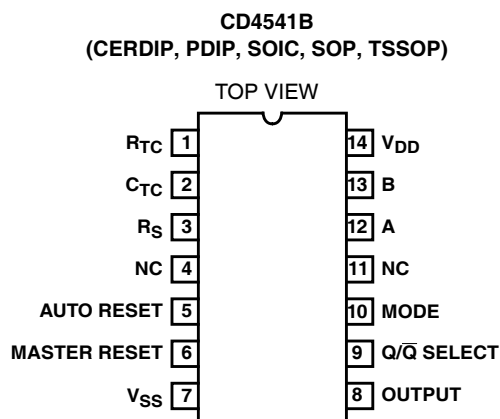
Where f is between 1kHz and 100kHz and R_S ≥ 10kΩ and ≈ 2R_{TC}

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD4541BF3A	-55 to 125	14 Ld Cerdip
CD4541BE	-55 to 125	14 Ld PDIP
CD4541BM	-55 to 125	14 Ld SOIC
CD4541BMT	-55 to 125	14 Ld SOIC
CD4541BM96	-55 to 125	14 Ld SOIC
CD4541BNSR	-55 to 125	14 Ld SOP
CD4541BPW	-55 to 125	14 Ld TSSOP
CD4541BPWR	-55 to 125	14 Ld TSSOP

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout



Functional Diagram

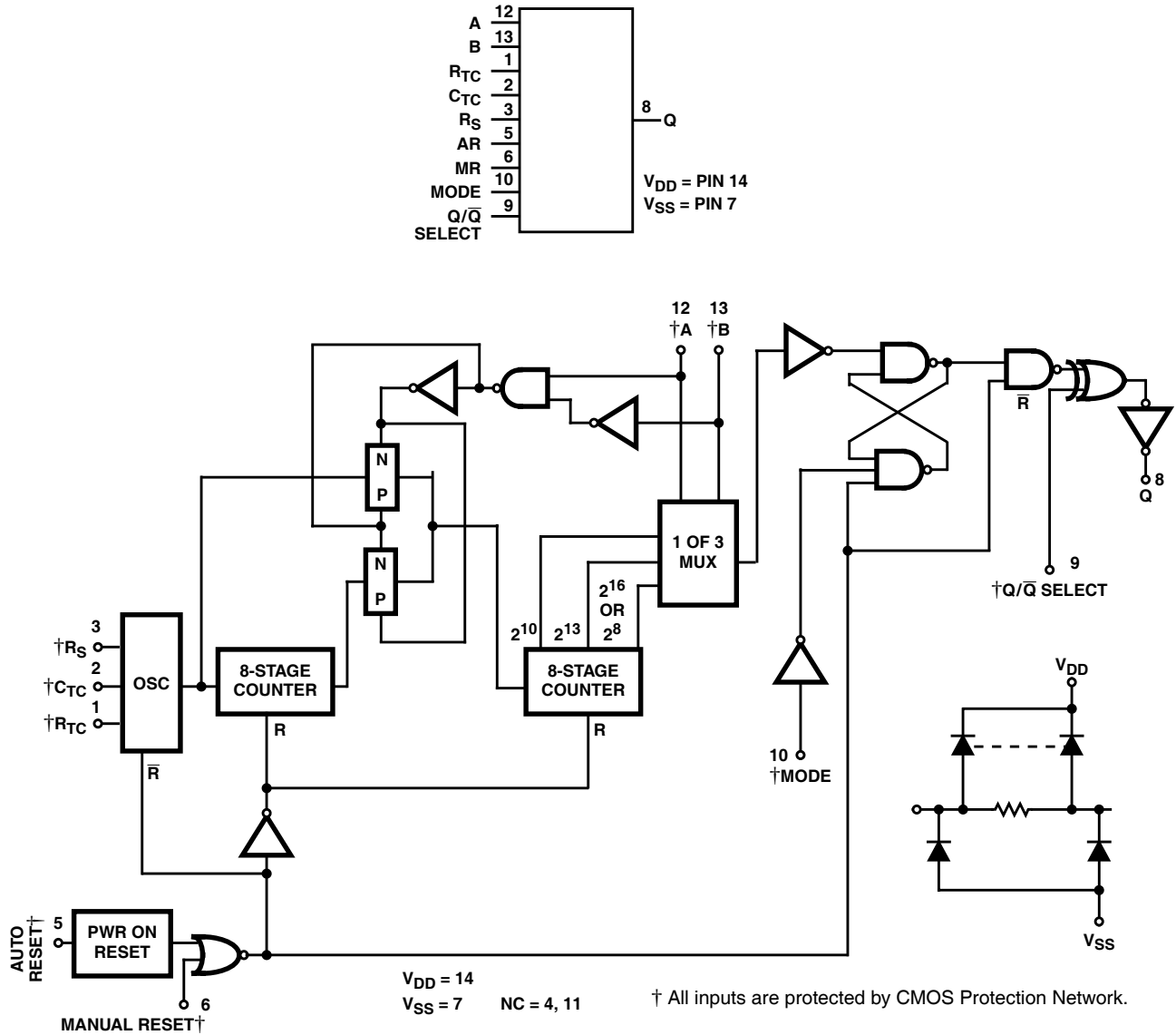


FIGURE 1.

FREQUENCY SELECTION TABLE

A	B	NO. OF STAGES N	COUNT 2 ^N
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

PIN	STATE	
	0	1
5	Auto Reset On	Auto Reset Disable
6	Master Reset Off	Master Reset On
9	Output Initially Low After Reset (Q)	Output Initially High After Reset ($\bar{Q}$)
10	Single Transition Mode	Recycle Mode

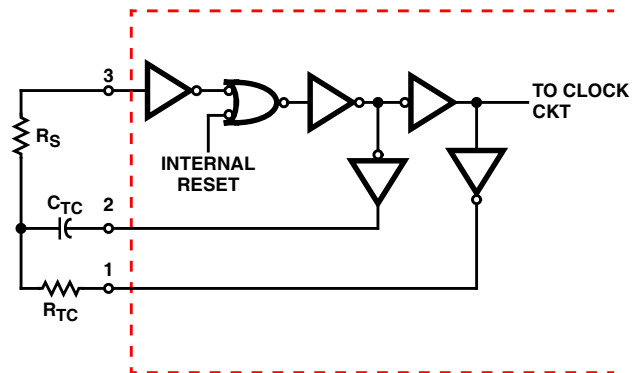


FIGURE 2. RC OSCILLATOR CIRCUIT

Absolute Maximum RatingsDC Supply - Voltage Range, V_{DD} Voltages Referenced to V_{SS} Terminal -0.5V to +20VInput Voltage Range, All Inputs -0.5V to $V_{DD} + 0.5V$ DC Input Current, Any One Input $\pm 10mA$

Device Dissipation Per Output Transistor

For T_A = Full Package Temperature Range

(All Package Types) 100mW

Operating ConditionsTemperature Range T_A -55°C to 125°C

Supply Voltage Range

For T_A = Full Package Temperature Range 3V (Min), 18V (Typ)**Thermal Information**Package Thermal Impedance, θ_{JA} (see Note 1)

PDIP package 80°C/W

SOIC package 86°C/W

SOP package 76°C/W

TSSOP package 113°C/W

Maximum Junction Temperature (Plastic Package) 150°C

Maximum Storage Temperature Range (T_{STG}) . . . -65°C to 150°C

Maximum Lead Temperature (Soldering 10s)

At Distance 1/16in $\pm$ 1/32in (1.59mm $\pm$ 0.79mm)

from case for 10s Maximum 265°C

(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JEDEC 51-7.

Electrical Specifications

PARAMETER	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	85	125	25			
								MIN	TYP	MAX	
Quiescent Device Current, (Note 2) I _{DD} (Max)	-	0, 5	5	5	5	150	150	-	0.04	5	μA
	-	0, 10	10	10	10	300	300	-	0.04	10	μA
	-	0, 15	15	20	20	600	600	-	0.04	20	μA
	-	0, 20	20	100	100	3000	3000	-	0.08	100	μA
Output Low (Sink) Current I _{OL} (Min)	0.4	0, 5	5	1.9	1.85	1.26	1.08	1.55	3.1	-	mA
	0.5	0, 10	10	5	4.8	3.3	2.8	4	8	-	mA
	1.5	0, 15	15	12.6	12	8.4	7.2	10	20	-	mA
Output High (Source) Current, I _{OH} (Min)	4.6	0, 5	5	-1.9	-1.85	-1.26	-1.08	-1.55	-3.1	-	mA
	2.5	0, 5	5	-6.2	-6	-4.1	-3	-5	-10	-	mA
	9.5	0, 10	10	-5	-4.8	-3.3	-2.8	-4	-8	-	mA
	13.5	0, 15	15	-12.6	-12	-8.4	-7.2	-10	-20	-	mA
Output Voltage: Low-Level, V _{OL} (Max)	-	0, 5	5	-	0.05			-	0	0.05	V
	-	0, 10	10	-	0.05			-	0	0.05	V
	-	0, 15	15	-	0.05			-	0	0.05	V
Output Voltage: High-Level, V _{OH} (Min)	-	0, 5	5	-	4.95			4.95	5	-	V
	-	0, 10	10	-	9.95			9.95	10	-	V
	-	0, 15	15	-	14.95			14.95	15	-	V
Input Low Voltage, V _{IL} (Max)	0.5, 4.5	-	5	-	1.5			-	-	1.5	V
	1, 9	-	10	-	3			-	-	3	V
	1.5, 13.5	-	15	-	4			-	-	4	V

CD4541B

Electrical Specifications (Continued)

PARAMETER	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	85	125	25			
								MIN	TYP	MAX	
Input High Voltage, V _{IH} (Min)	0.5, 4.5	-	5	-		3.5		3.5	-	-	V
	1, 9	-	10	-		7		7	-	-	V
	1.5, 13.5	-	15	-		11		11	-	-	V
Input Current, I _{IN} (Max)	-	0, 18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

NOTE:

2. With AUTO RESET enabled, additional current drain at 25°C is:

7μA (Typ), 200μA (Max) at 5V;

30μA (Typ), 350μA (Max) at 10V;

80μA (Typ), 500μA (Max) at 15V

Dynamic Electrical Specifications T_A = 25°C, Input t_r, t_f = 20ns, C_L = 50pF, R_L = 200kΩ

PARAMETER	SYMBOL	V _{DD} (V)	MIN	TYP	MAX	UNITS
Propagation Delay Times Clock to Q	(2 ⁸) t _{PHL} , t _{PLH}	5	-	3.5	10.5	μs
		10	-	1.25	3.8	μs
		15	-	0.9	2.9	μs
	(2 ¹⁶) t _{PHL} , t _{PLH}	5	-	6.0	18	μs
		10	-	3.5	10	μs
		15	-	2.5	7.5	μs
Transition Time	t _{THL}	5	-	100	200	ns
		10	-	50	100	ns
		15	-	40	80	ns
	t _{THL}	5	-	180	360	ns
		10	-	90	180	ns
		15	-	65	130	ns
MASTER RESET, CLOCK Pulse Width		5	900	300	-	ns
		10	300	100	-	ns
		15	225	85	-	ns
Maximum Clock Pulse Input Frequency	f _{CL}	5	-	1.5	-	MHz
		10	-	4	-	MHz
		15	-	6	-	MHz
Maximum Clock Pulse Input Rise or Fall time	t _r , t _f	5, 10, 15	Unlimited			μs

Digital Timer Application

A positive pulse on MASTER RESET resets the counters and latch. The output goes high and remains high until the number of pulses, selected by A and B, are counted. This circuit is retriggerable and is as accurate as the input frequency. If additional accuracy is desired, an external clock can be used on pin 3. A setup time equal to the width of the one-shot output is required immediately following initial power up, during which time the output will be high.

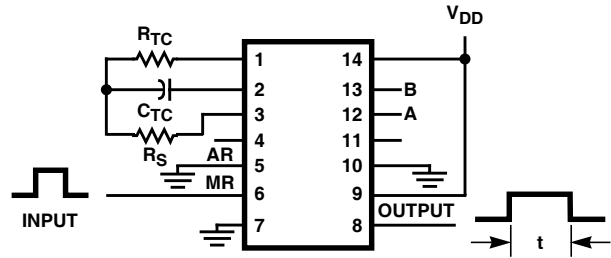


FIGURE 3. DIGITAL TIMER APPLICATION CIRCUIT

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4541BE	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4541BE
CD4541BE.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4541BE
CD4541BEE4	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4541BE
CD4541BEE4.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4541BE
CD4541BF	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4541BF
CD4541BF.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4541BF
CD4541BF3A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4541BF3A
CD4541BF3A.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4541BF3A
CD4541BM	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4541BM
CD4541BM.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4541BM
CD4541BM96	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4541BM
CD4541BM96.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4541BM
CD4541BMT	Active	Production	SOIC (D) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4541BM
CD4541BMT.A	Active	Production	SOIC (D) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4541BM
CD4541BMTG4	Active	Production	SOIC (D) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4541BM
CD4541BNSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4541B
CD4541BNSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4541B
CD4541BPW	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM541B
CD4541BPW.A	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM541B
CD4541BPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	CM541B
CD4541BPWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM541B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD4541B, CD4541B-MIL :

- Catalog : [CD4541B](#)
- Military : [CD4541B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4541BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4541BNSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4541BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

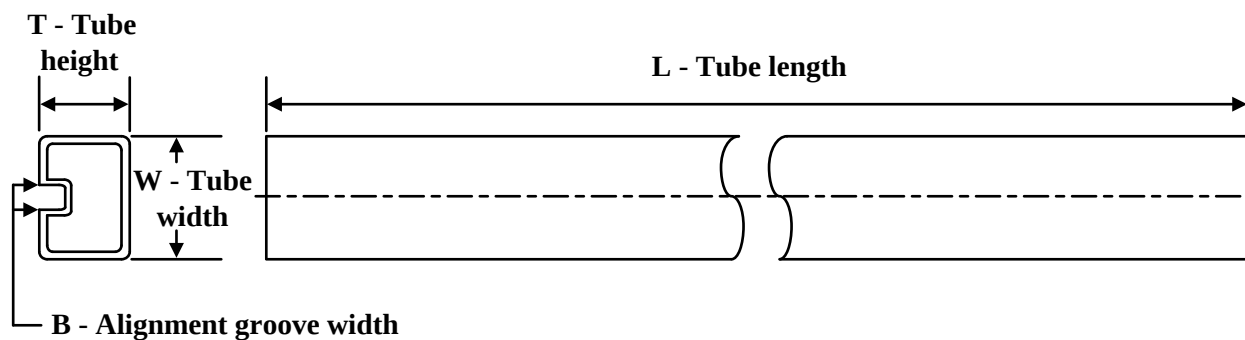
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

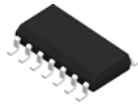
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4541BM96	SOIC	D	14	2500	353.0	353.0	32.0
CD4541BNSR	SOP	NS	14	2000	353.0	353.0	32.0
CD4541BPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE

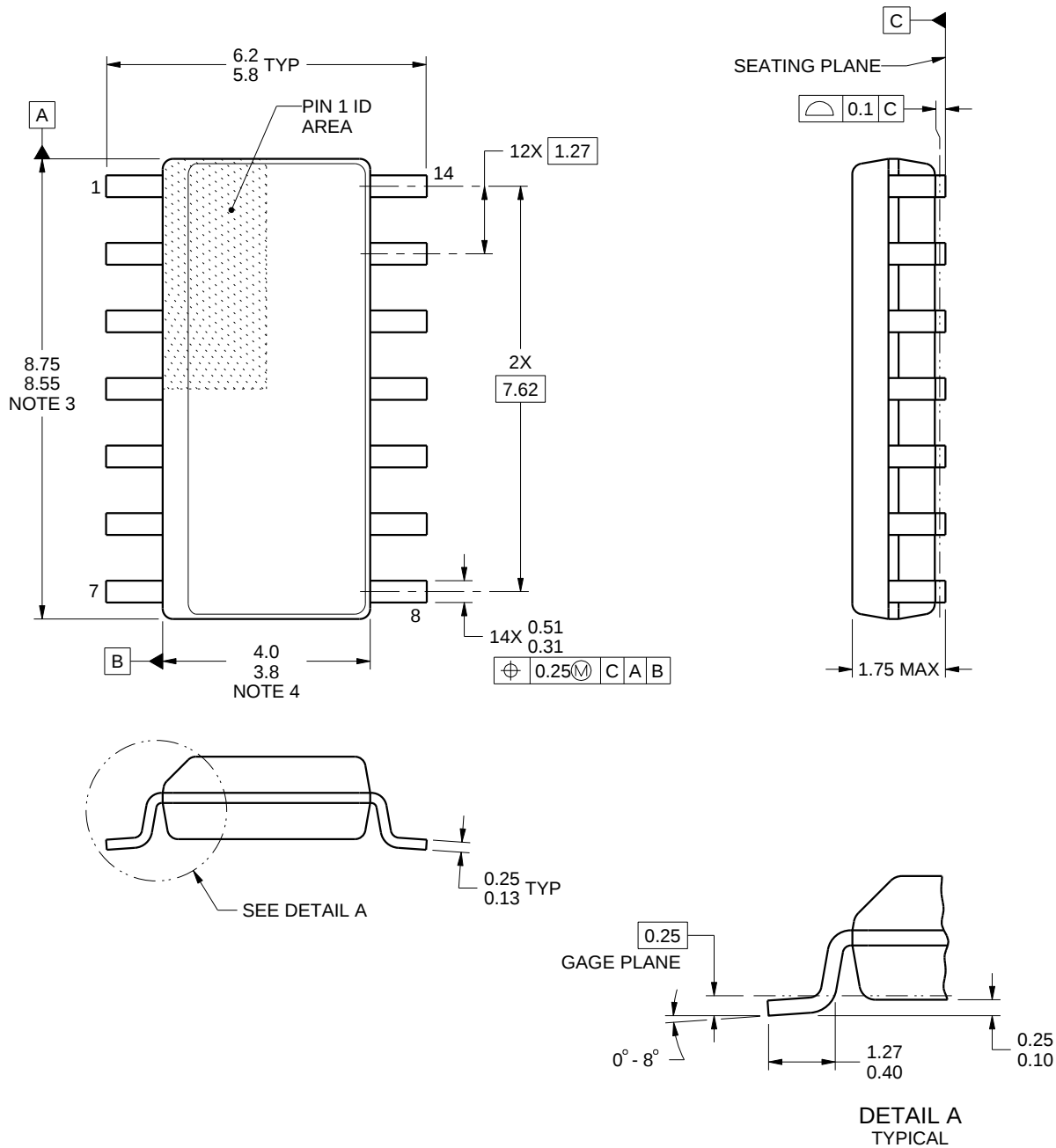


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4541BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4541BE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4541BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4541BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4541BEE4.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4541BEE4.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4541BM	D	SOIC	14	50	506.6	8	3940	4.32
CD4541BM.A	D	SOIC	14	50	506.6	8	3940	4.32
CD4541BPW	PW	TSSOP	14	90	530	10.2	3600	3.5
CD4541BPW.A	PW	TSSOP	14	90	530	10.2	3600	3.5

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

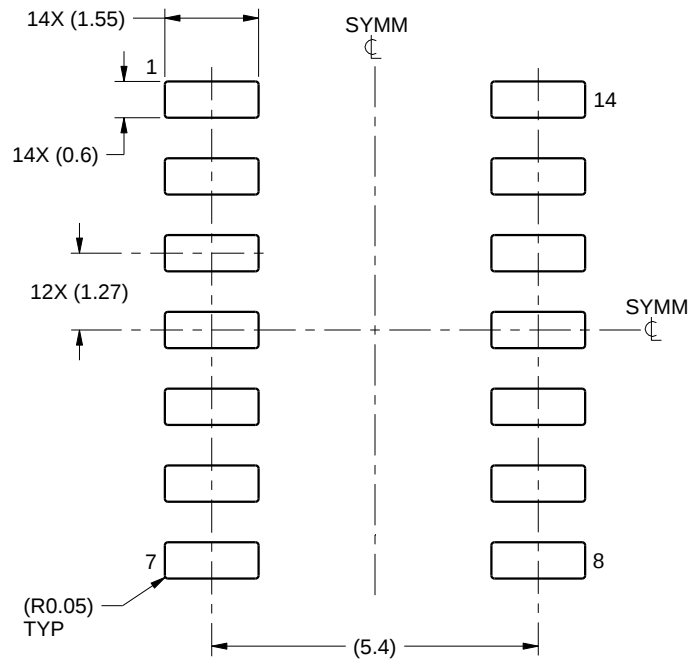
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

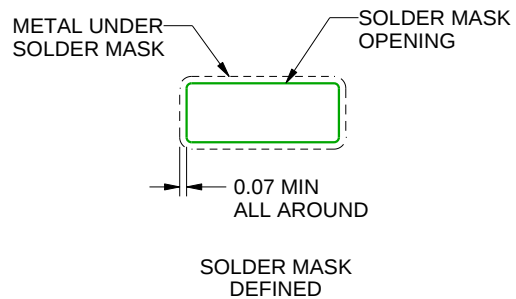
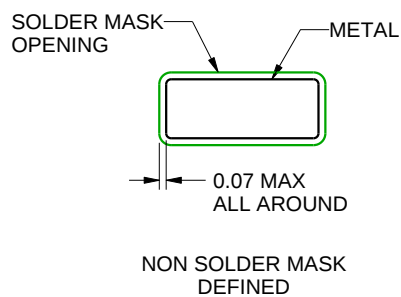
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

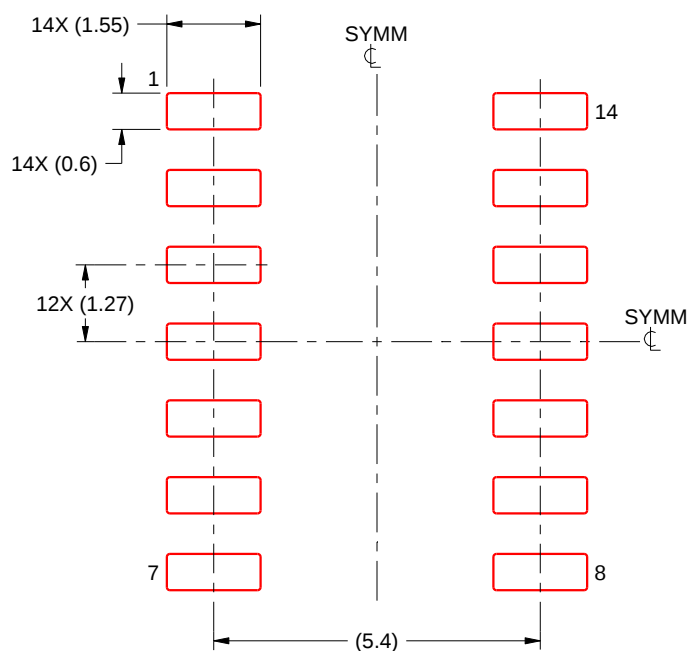
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

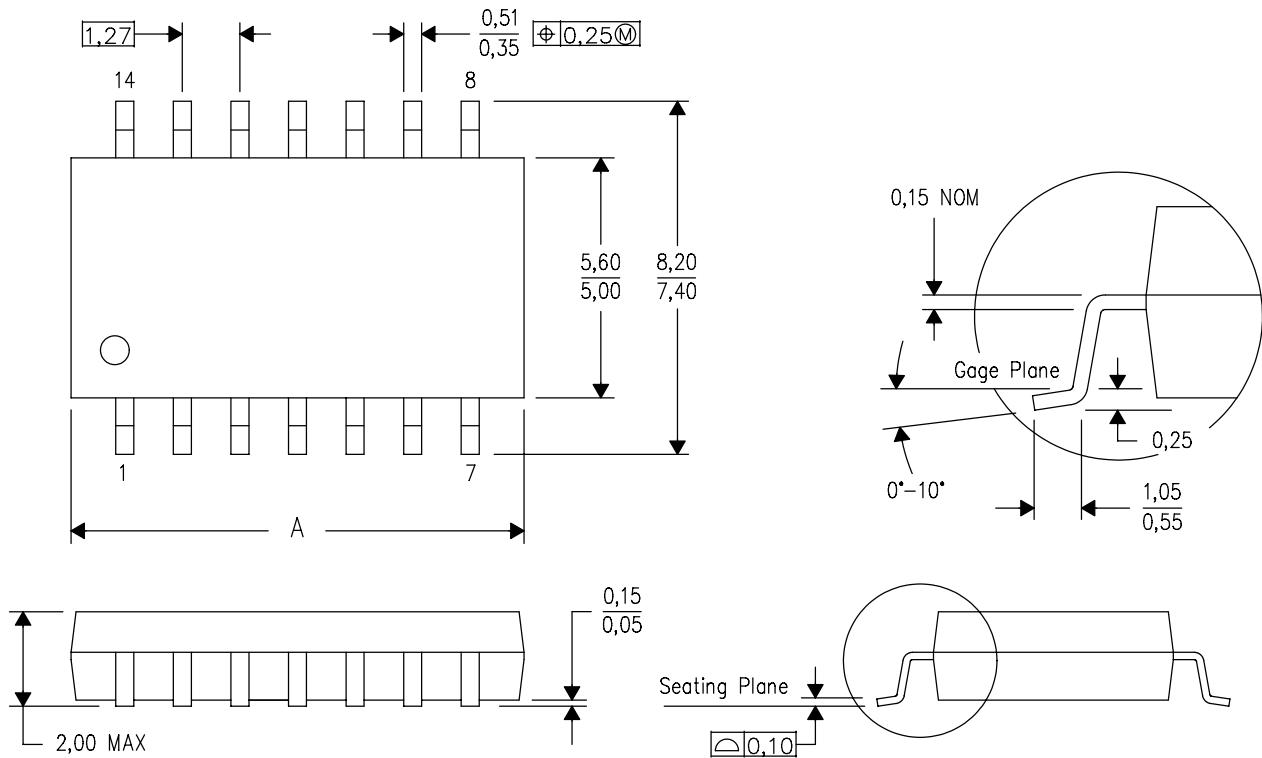
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

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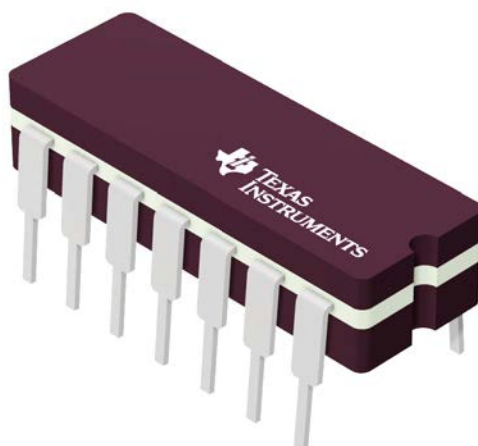
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

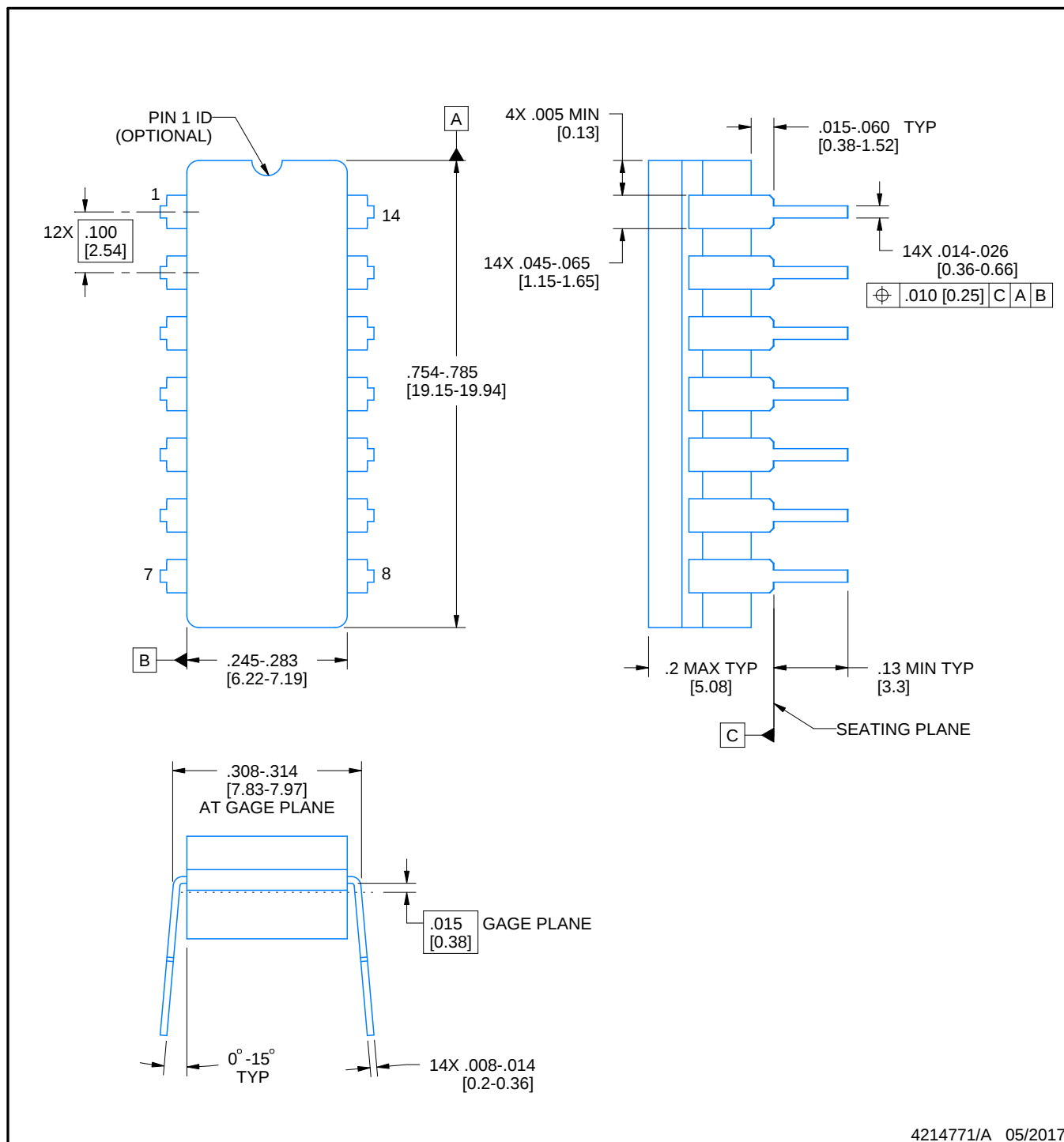


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PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



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NOTES:

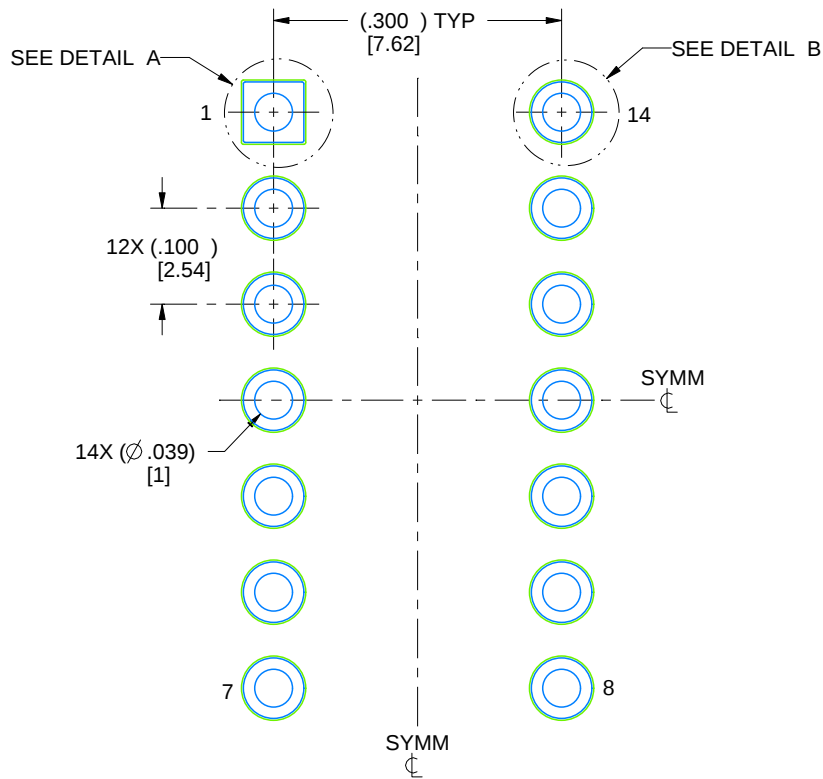
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

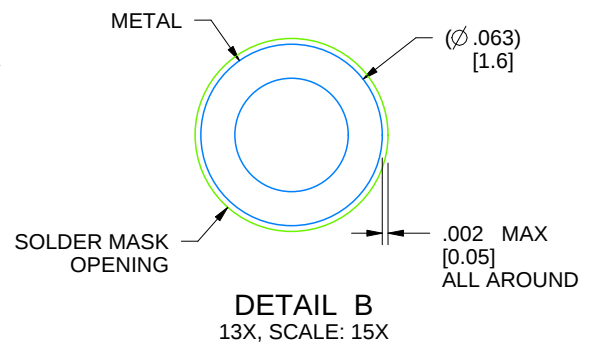
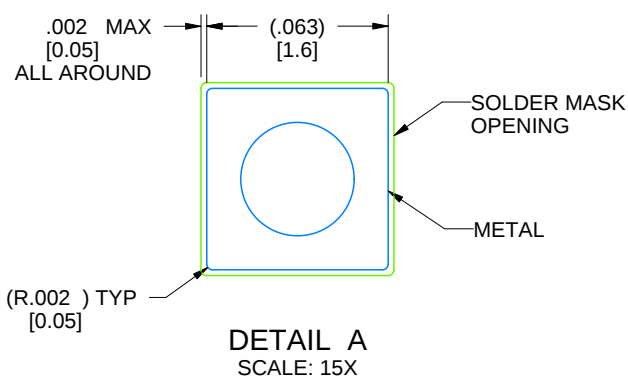
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CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

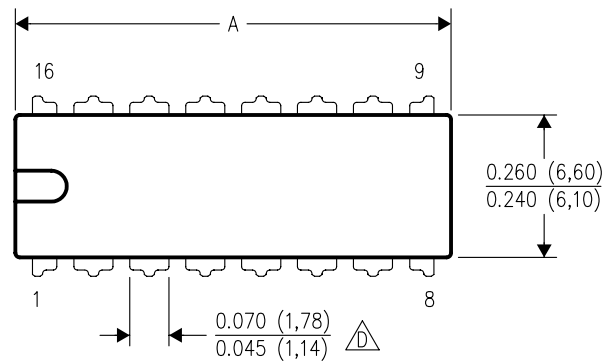


4214771/A 05/2017

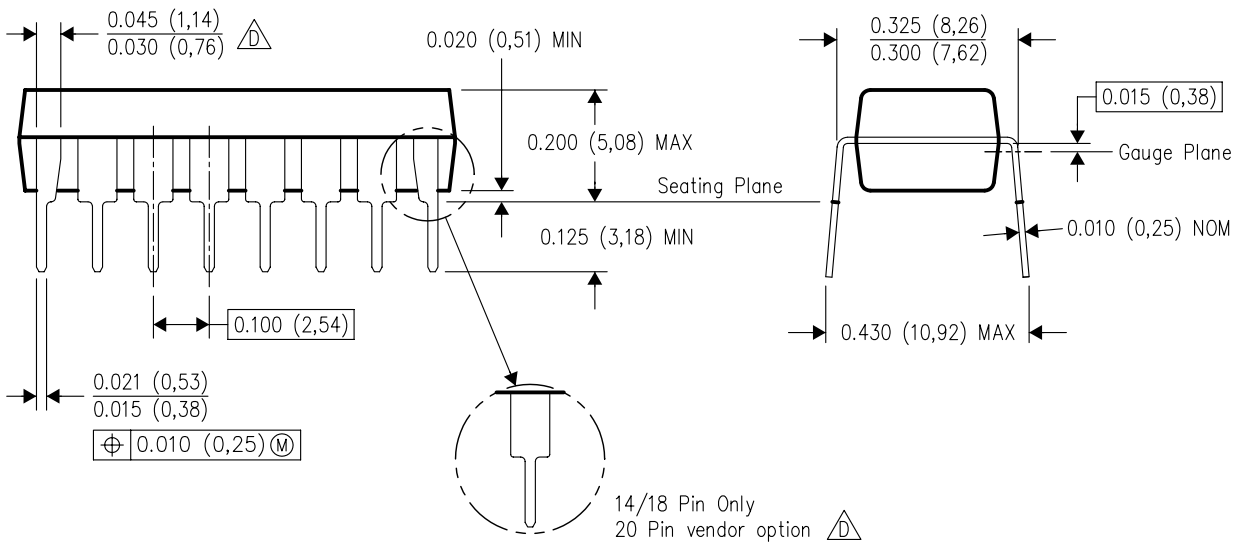
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

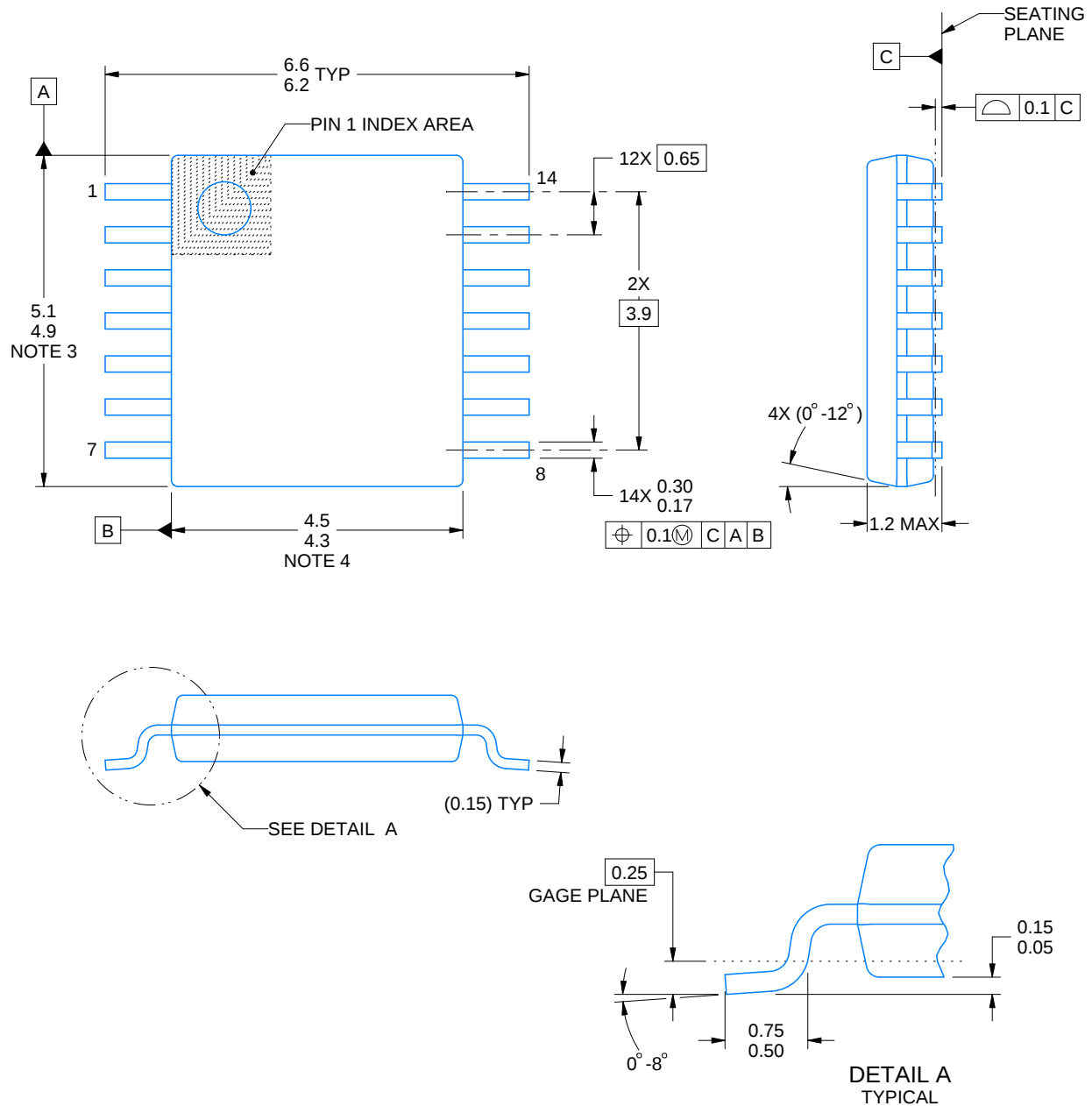
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

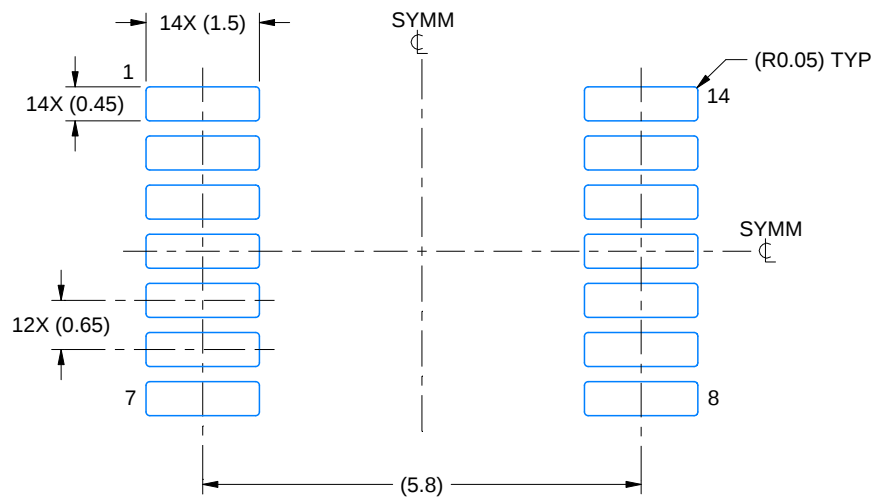
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

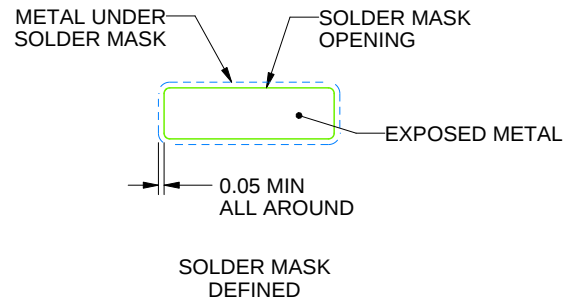
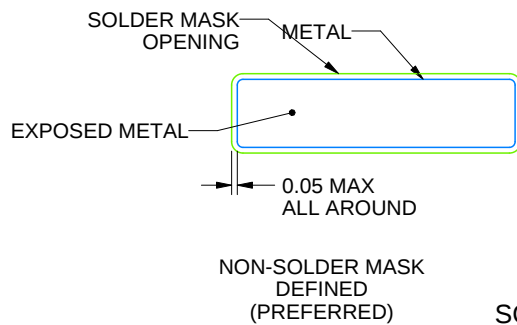
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

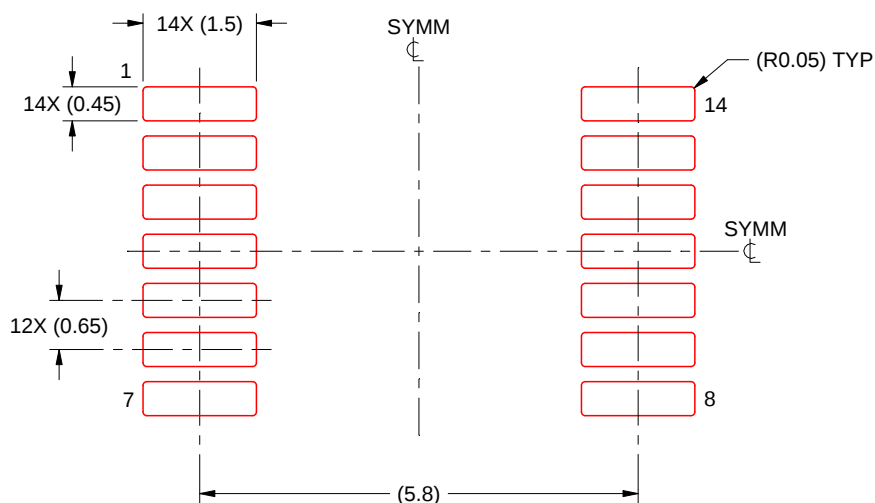
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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