

## CMOS 8-Stage Shift-and-Store Bus Register

High-Voltage Types (20-Volt Rating)

■ CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the  $Q_S$  serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the  $Q'_S$  terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

The CD4094B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

- 3-state parallel outputs for connection to common bus
- Separate serial outputs synchronous to both positive and negative clock edges for cascading
- Medium speed operation – 5 MHz at 10 V (typ.)
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range):  
1 V at  $V_{DD} = 5$  V      2 V at  $V_{DD} = 10$  V  
2.5 V at  $V_{DD} = 15$  V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Serial-to-parallel data conversion
- Remote control holding register
- Dual-rank shift, hold, and bus applications

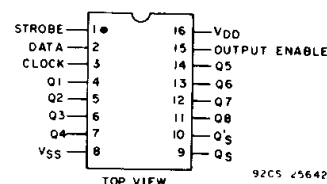
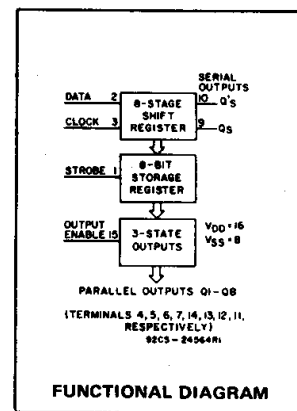


Fig. 1 – Terminal assignment.

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal) ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to  $V_{DD} + 0.5$ V

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm 10$ mA

POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearly at 12mW/ $^\circ\text{C}$  to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$  ..... 100mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79mm) from case for 10s max .....  $+265^\circ\text{C}$

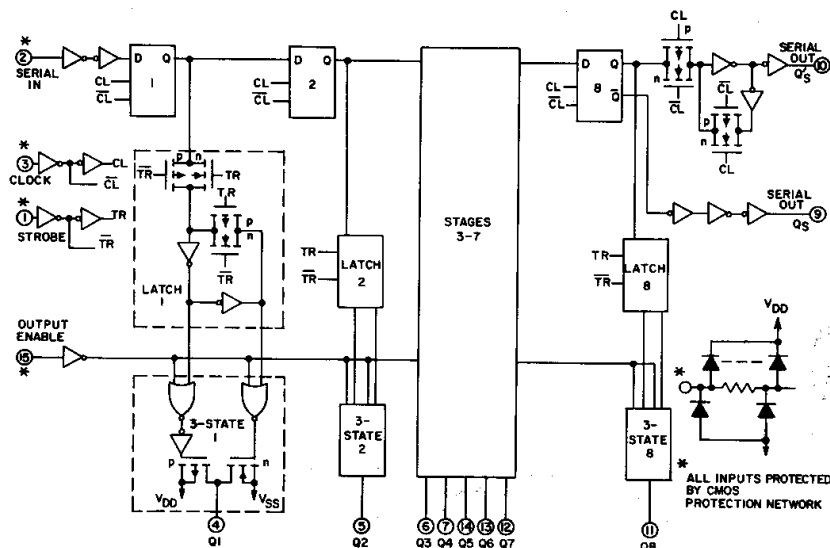


Fig. 2 – CD4094B Logic diagram.

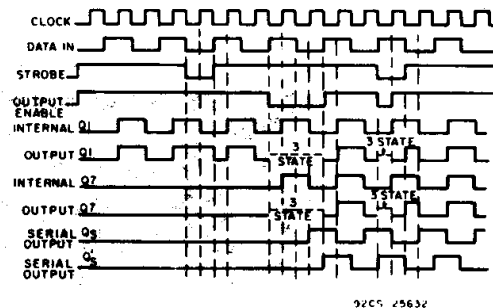


Fig. 3 – Timing diagram.

# CD4094B Types

**RECOMMENDED OPERATING CONDITIONS at  $T_A = 25^\circ\text{C}$ , Except as Noted.**  
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC                                                   | VDD<br>(V)    | LIMITS           |                  | UNITS         |
|------------------------------------------------------------------|---------------|------------------|------------------|---------------|
|                                                                  |               | MIN.             | MAX.             |               |
| Supply-Voltage Range (For $T_A$ =Full Package-Temperature Range) |               | 3                | 18               | V             |
| Data Setup Time, $t_S$                                           | 5<br>10<br>15 | 125<br>55<br>35  | —<br>—<br>—      | ns            |
| Clock Pulse Width, $t_W$                                         | 5<br>10<br>15 | 200<br>100<br>83 | —<br>—<br>—      | ns            |
| Clock Input Frequency, $f_{CL}$                                  | 5<br>10<br>15 | dc               | 1.25<br>2.5<br>3 | MHz           |
| Clock Input Rise or Fall time,<br>$t_{rCL}$ , $t_{fCL}$ *        | 5<br>10<br>15 | —                | 15<br>5<br>5     | $\mu\text{s}$ |
| Strobe Pulse Width, $t_W$                                        | 5<br>10<br>15 | 200<br>80<br>70  | —<br>—<br>—      | ns            |

\*If more than one unit is cascaded  $t_{rCL}$  (for  $Q_S$  only) should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the output driving stage for the estimated capacitive load.

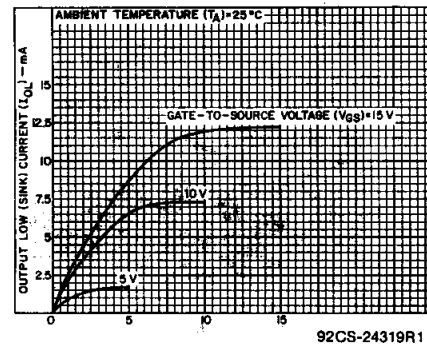


Fig. 5 - Minimum output low (sink) current characteristics.

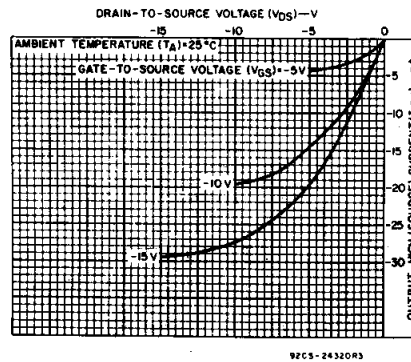


Fig. 6 - Typical output high (source) current characteristics.

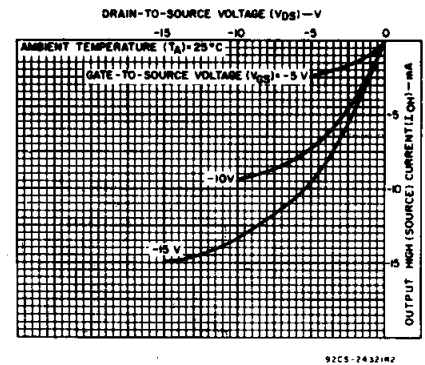


Fig. 7 - Minimum output high (source) current characteristics.

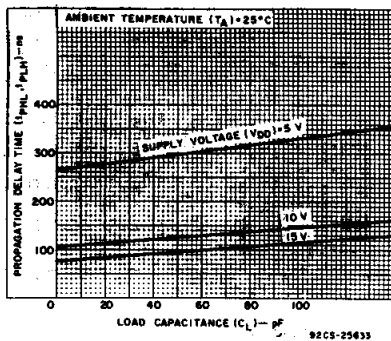


Fig. 8 - Clock-to-serial output  $Q_S$  propagation delay vs  $C_L$ .

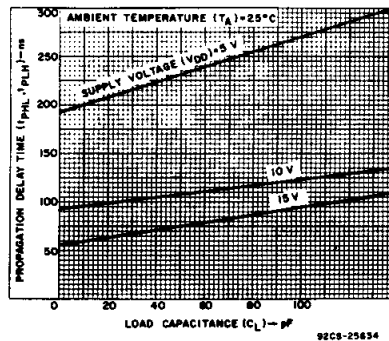


Fig. 9 - Clock-to-serial output  $Q'_S$  propagation delay vs  $C_L$ .

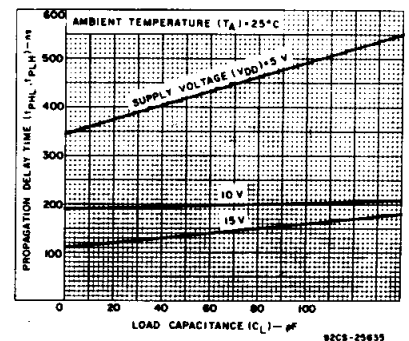


Fig. 10 - Clock-to-parallel output propagation delay vs  $C_L$ .

TRUTH TABLE

| CL <sup>Δ</sup> | Output Enable | Strobe | Data | Parallel Outputs |                   | Serial Outputs   |                 |
|-----------------|---------------|--------|------|------------------|-------------------|------------------|-----------------|
|                 |               |        |      | Q1               | Q <sub>N</sub>    | Q <sub>S</sub> * | Q' <sub>S</sub> |
|                 | 0             | X      | X    | OC               | OC                | Q7               | NC              |
|                 | 0             | X      | X    | OC               | OC                | NC               | Q7              |
|                 | 1             | 0      | X    | NC               | NC                | Q7               | NC              |
|                 | 1             | 1      | 0    | 0                | Q <sub>N</sub> -1 | Q7               | NC              |
|                 | 1             | 1      | 1    | 1                | Q <sub>N</sub> -1 | Q7               | NC              |
|                 | 1             | 1      | 1    | NC               | NC                | NC               | Q7              |

<sup>Δ</sup> = Level Change

X = Don't Care

NC = No Change

OC = Open Circuit

Logic 1  $\equiv$  High

Logic 0  $\equiv$  Low

\* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the  $Q_S$  output.

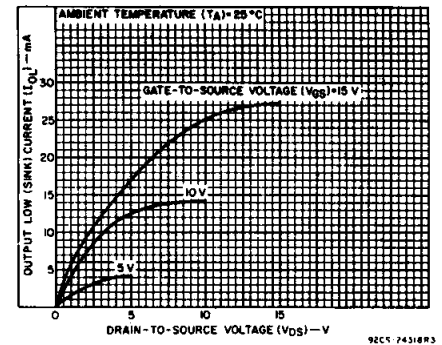


Fig. 4 - Typical output low (sink) current characteristics.

# CD4094B Types

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTER-<br>ISTIC                                         | CONDITIONS            |                        |                        | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|-------------------------------------------------------------|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|                                                             | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>DD</sub><br>(V) |                                       |       |       |       | +25   |                   |      |       |
|                                                             |                       |                        |                        | -55                                   | -40   | +85   | +125  | Min.  | Typ.              | Max. |       |
| Quiescent Device<br>Current,<br>I <sub>DD</sub> Max.        | —                     | 0,5                    | 5                      | 5                                     | 5     | 150   | 150   | —     | 0.04              | 5    | μA    |
|                                                             | —                     | 0,10                   | 10                     | 10                                    | 10    | 300   | 300   | —     | 0.04              | 10   |       |
|                                                             | —                     | 0,15                   | 15                     | 20                                    | 20    | 600   | 600   | —     | 0.04              | 20   |       |
|                                                             | —                     | 0,20                   | 20                     | 100                                   | 100   | 3000  | 3000  | —     | 0.08              | 100  |       |
| Output Low<br>(Sink) Current<br>I <sub>OL</sub> Min.        | 0.4                   | 0,5                    | 5                      | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | —    | mA    |
|                                                             | 0.5                   | 0,10                   | 10                     | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | —    |       |
|                                                             | 1.5                   | 0,15                   | 15                     | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | —    |       |
| Output High<br>(Source)<br>Current,<br>I <sub>OH</sub> Min. | 4.6                   | 0,5                    | 5                      | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | —    | mA    |
|                                                             | 2.5                   | 0,5                    | 5                      | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | —    |       |
|                                                             | 9.5                   | 0,10                   | 10                     | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | —    |       |
|                                                             | 13.5                  | 0,15                   | 15                     | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              | —    |       |
| Output Voltage:<br>Low-Level,<br>V <sub>OL</sub> Max.       | —                     | 0,5                    | 5                      | 0.05                                  |       |       |       | —     | 0                 | 0.05 | V     |
|                                                             | —                     | 0,10                   | 10                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
|                                                             | —                     | 0,15                   | 15                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
| Output Voltage:<br>High-Level,<br>V <sub>OH</sub> Min.      | —                     | 0,5                    | 5                      | 4.95                                  |       |       |       | 4.95  | 5                 | —    | V     |
|                                                             | —                     | 0,10                   | 10                     | 9.95                                  |       |       |       | 9.95  | 10                | —    |       |
|                                                             | —                     | 0,15                   | 15                     | 14.95                                 |       |       |       | 14.95 | 15                | —    |       |
| Input Low<br>Voltage,<br>V <sub>IL</sub> Max.               | 0.5, 4.5              | —                      | 5                      | 1.5                                   |       |       |       | —     | —                 | 1.5  | V     |
|                                                             | 1, 9                  | —                      | 10                     | 3                                     |       |       |       | —     | —                 | 3    |       |
|                                                             | 1.5, 13.5             | —                      | 15                     | 4                                     |       |       |       | —     | —                 | 4    |       |
| Input High<br>Voltage,<br>V <sub>IH</sub> Min.              | 0.5, 4.5              | —                      | 5                      | 3.5                                   |       |       |       | 3.5   | —                 | —    | V     |
|                                                             | 1, 9                  | —                      | 10                     | 7                                     |       |       |       | 7     | —                 | —    |       |
|                                                             | 1.5, 13.5             | —                      | 15                     | 11                                    |       |       |       | 11    | —                 | —    |       |
| Input Current<br>I <sub>IN</sub> Max.                       | —                     | 0,18                   | 18                     | ±0.1                                  | ±0.1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0.1 | μA    |
| 3-State Output<br>Leakage Current<br>I <sub>OUT</sub> Max.  | 0,18                  | 0,18                   | 18                     | ±0.4                                  | ±0.4  | ±12   | ±12   | —     | ±10 <sup>-4</sup> | ±0.4 | μA    |

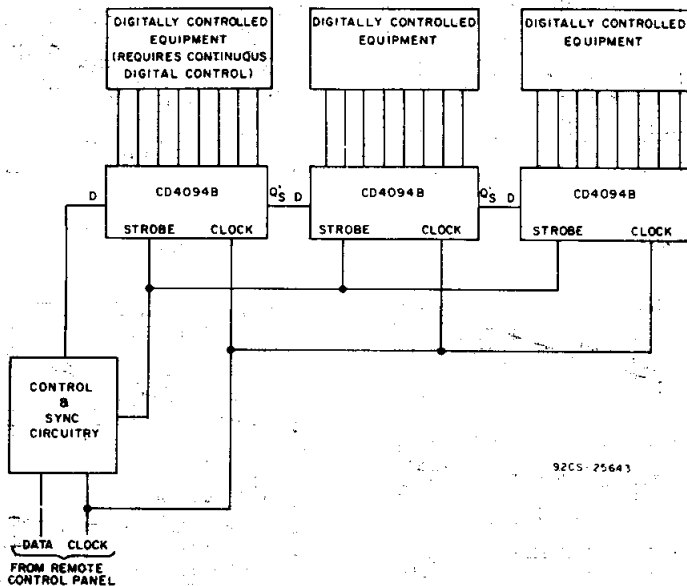


Fig. 14 — Remote control holding register.

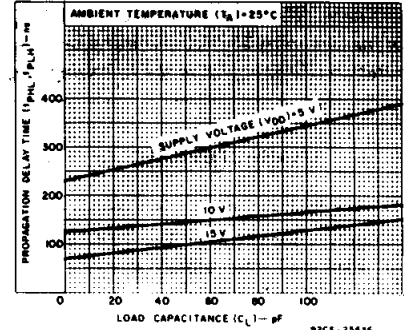


Fig. 11 — Strobe-to-parallel output propagation delay vs. C<sub>L</sub>.

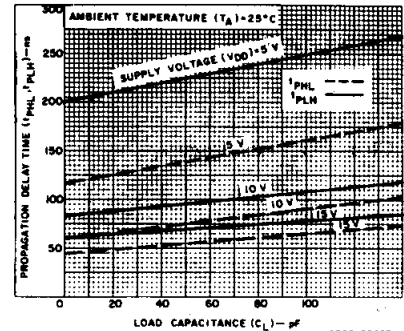


Fig. 12 — Output enable-to-parallel output propagation delay vs. C<sub>L</sub>.

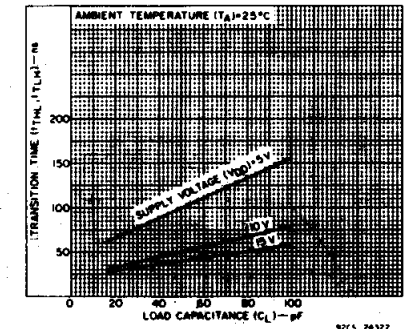


Fig. 13 — Typical transition time vs. load capacitance.

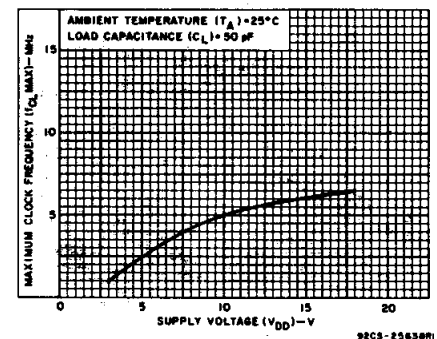


Fig. 15 — Typical maximum-clock-frequency vs. supply voltage.

## CD4094B Types

### DYNAMIC ELECTRICAL CHARACTERISTICS

At  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC                                               | VDD<br>(V) | LIMITS |      |      | UNITS         |
|--------------------------------------------------------------|------------|--------|------|------|---------------|
|                                                              |            | MIN.   | TYP. | MAX. |               |
| Propagation Delay Time,<br>$t_{PHL}, t_{PLH}$                | 5          | —      | 300  | 600  | ns            |
| Clock to Serial Output $Q_S$                                 | 10         | —      | 125  | 250  |               |
|                                                              | 15         | —      | 95   | 190  |               |
| Clock to Serial Output $Q'_S$                                | 5          | —      | 230  | 460  | ns            |
|                                                              | 10         | —      | 110  | 220  |               |
|                                                              | 15         | —      | 75   | 150  |               |
| Clock to Parallel Output                                     | 5          | —      | 420  | 840  | ns            |
|                                                              | 10         | —      | 195  | 390  |               |
|                                                              | 15         | —      | 135  | 270  |               |
| Strobe to Parallel Output                                    | 5          | —      | 290  | 580  | ns            |
|                                                              | 10         | —      | 145  | 290  |               |
|                                                              | 15         | —      | 100  | 200  |               |
| Output Enable to Parallel<br>Output:<br>$t_{PHZ}, t_{PZH}$   | 5          | —      | 140  | 280  | ns            |
|                                                              | 10         | —      | 60   | 120  |               |
|                                                              | 15         | —      | 45   | 90   |               |
| $t_{PLZ}, t_{PZL}$                                           | 5          | —      | 100  | 200  | ns            |
|                                                              | 10         | —      | 50   | 100  |               |
|                                                              | 15         | —      | 40   | 80   |               |
| Minimum Strobe Pulse<br>Width, $t_W$                         | 5          | —      | 100  | 200  | ns            |
|                                                              | 10         | —      | 40   | 80   |               |
|                                                              | 15         | —      | 35   | 70   |               |
| Minimum Clock Pulse<br>Width, $t_W$                          | 5          | —      | 100  | 200  | ns            |
|                                                              | 10         | —      | 50   | 100  |               |
|                                                              | 15         | —      | 40   | 83   |               |
| Minimum Data Setup<br>Time, $t_S$                            | 5          | —      | 60   | 125  | ns            |
|                                                              | 10         | —      | 30   | 55   |               |
|                                                              | 15         | —      | 20   | 35   |               |
| Transition Time;<br>$t_{THL}, t_{TLH}$                       | 5          | —      | 100  | 200  | ns            |
|                                                              | 10         | —      | 50   | 100  |               |
|                                                              | 15         | —      | 40   | 80   |               |
| Maximum Clock Input Rise<br>or Fall Time, $t_{rCL}, t_{fCL}$ | 5          | 15     | —    | —    | $\mu\text{s}$ |
|                                                              | 10         | 5      | —    | —    |               |
|                                                              | 15         | 5      | —    | —    |               |
| Maximum Clock Input<br>Frequency, $f_{CL}$                   | 5          | 1.25   | 2.5  | —    | MHz           |
|                                                              | 10         | 2.5    | 5    | —    |               |
|                                                              | 15         | 3      | 6    | —    |               |
| Input Capacitance $C_{IN}$<br>(Any Input)                    | —          | —      | 5    | 7.5  | pF            |

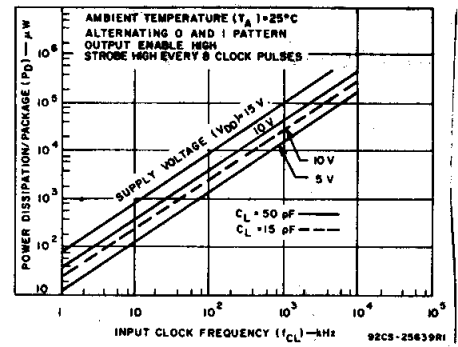


Fig. 16 — Dynamic power dissipation vs input clock frequency.

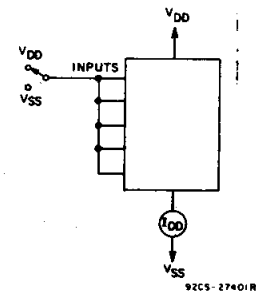


Fig. 17 — Quiescent device current test circuit.

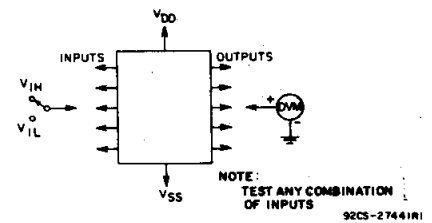


Fig. 18 — Input voltage test circuit.

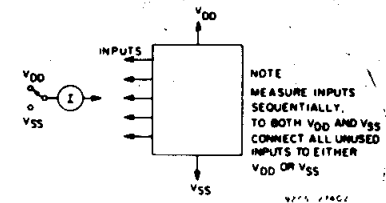
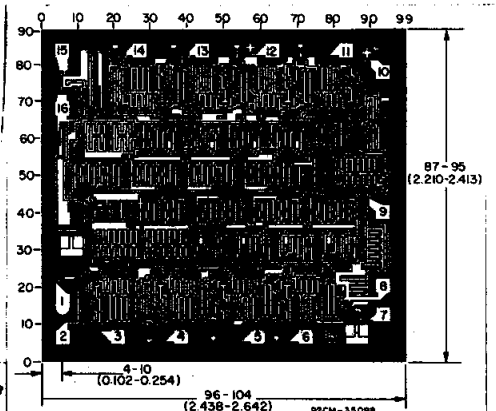


Fig. 19 — Input current test circuit.



Dimensions and Pad Layout for CD4094B Chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)     |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------|
| <a href="#">7702501EA</a>    | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7702501EA<br>CD4094BF3A |
| <a href="#">CD4094BE</a>     | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD4094BE                |
| CD4094BE.A                   | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD4094BE                |
| CD4094BEE4                   | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD4094BE                |
| <a href="#">CD4094BF</a>     | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD4094BF                |
| CD4094BF.A                   | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD4094BF                |
| <a href="#">CD4094BF3A</a>   | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7702501EA<br>CD4094BF3A |
| CD4094BF3A.A                 | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7702501EA<br>CD4094BF3A |
| <a href="#">CD4094BNSR</a>   | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD4094B                 |
| CD4094BNSR.A                 | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD4094B                 |
| <a href="#">CD4094BPW</a>    | Obsolete      | Production           | TSSOP (PW)   16 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | CM094B                  |
| <a href="#">CD4094BPWR</a>   | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -55 to 125   | CM094B                  |
| CD4094BPWR.A                 | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CM094B                  |
| <a href="#">CD4094BPWRG4</a> | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CM094B                  |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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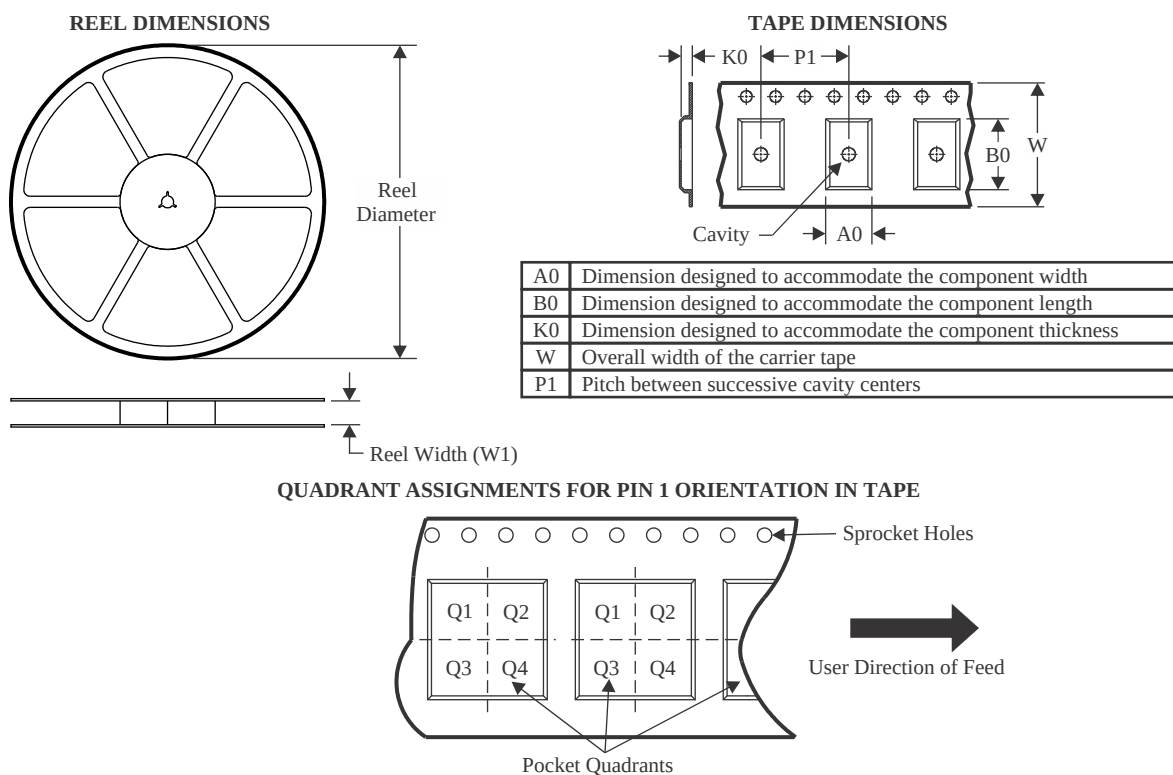
**OTHER QUALIFIED VERSIONS OF CD4094B, CD4094B-MIL :**

- Catalog : [CD4094B](#)
- Military : [CD4094B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

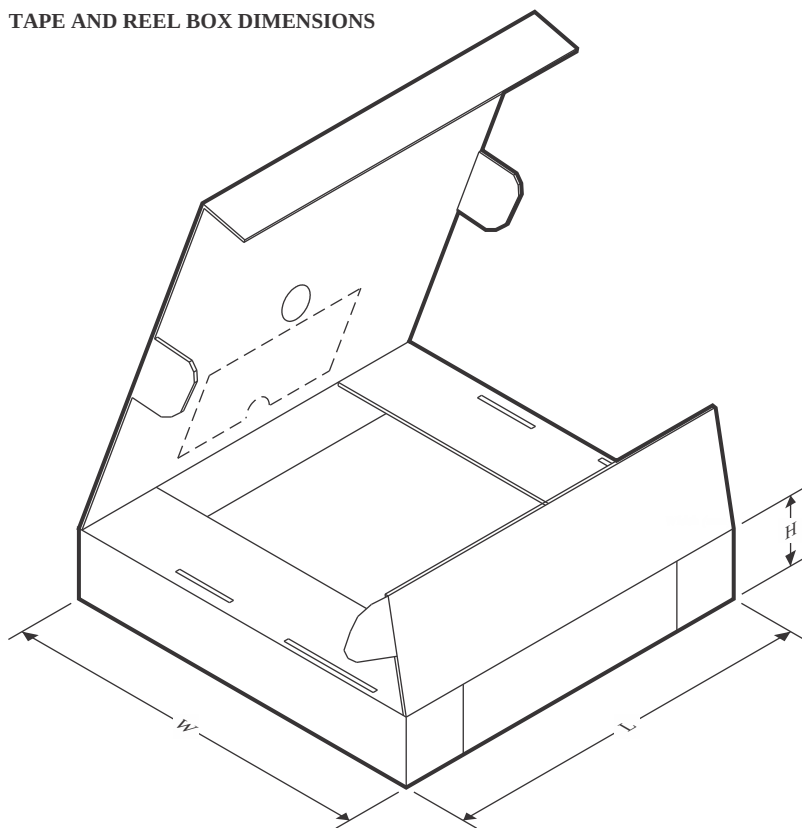
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4094BNSR   | SOP          | NS              | 16   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |
| CD4094BPWR   | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD4094BPWR   | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD4094BPWRG4 | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

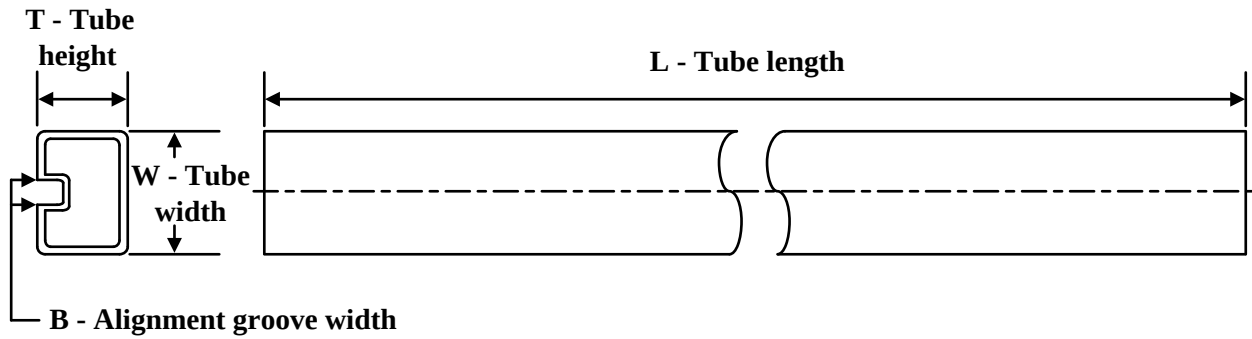
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4094BNSR   | SOP          | NS              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| CD4094BPWR   | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| CD4094BPWR   | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| CD4094BPWRG4 | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |

## TUBE



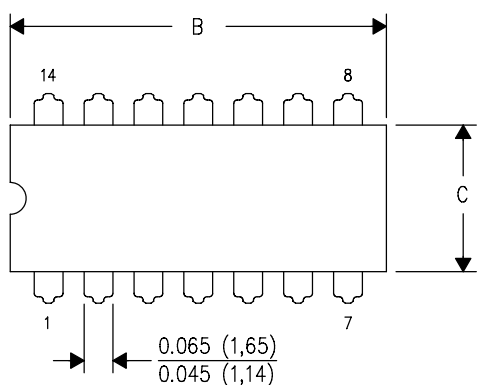
\*All dimensions are nominal

| Device     | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD4094BE   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD4094BE.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD4094BEE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |

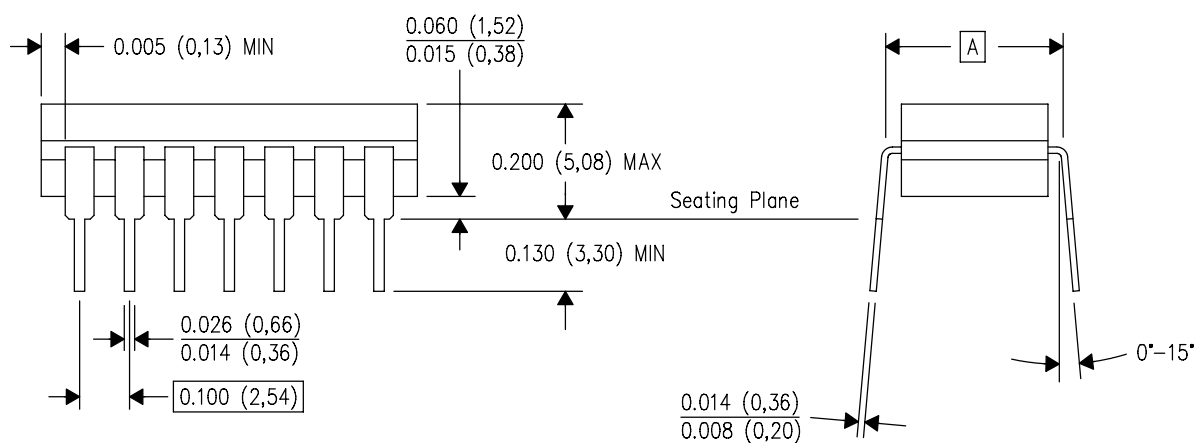
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

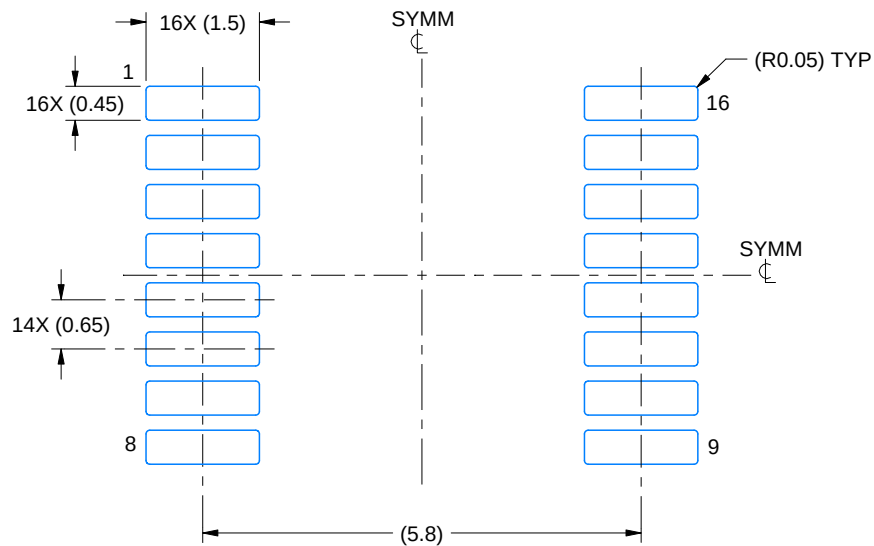


# EXAMPLE BOARD LAYOUT

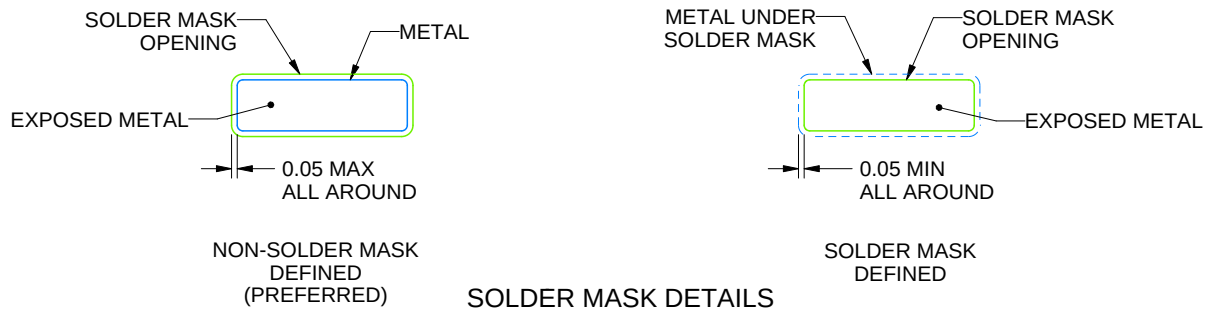
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

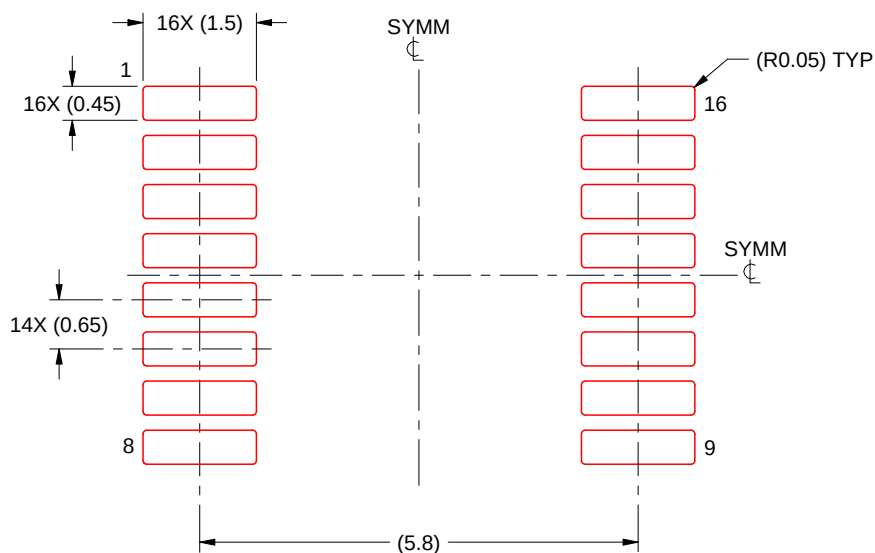
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

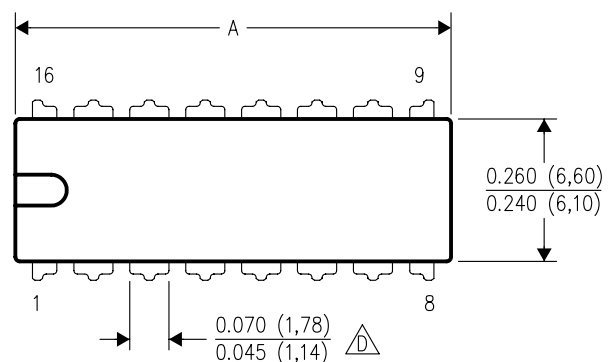
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

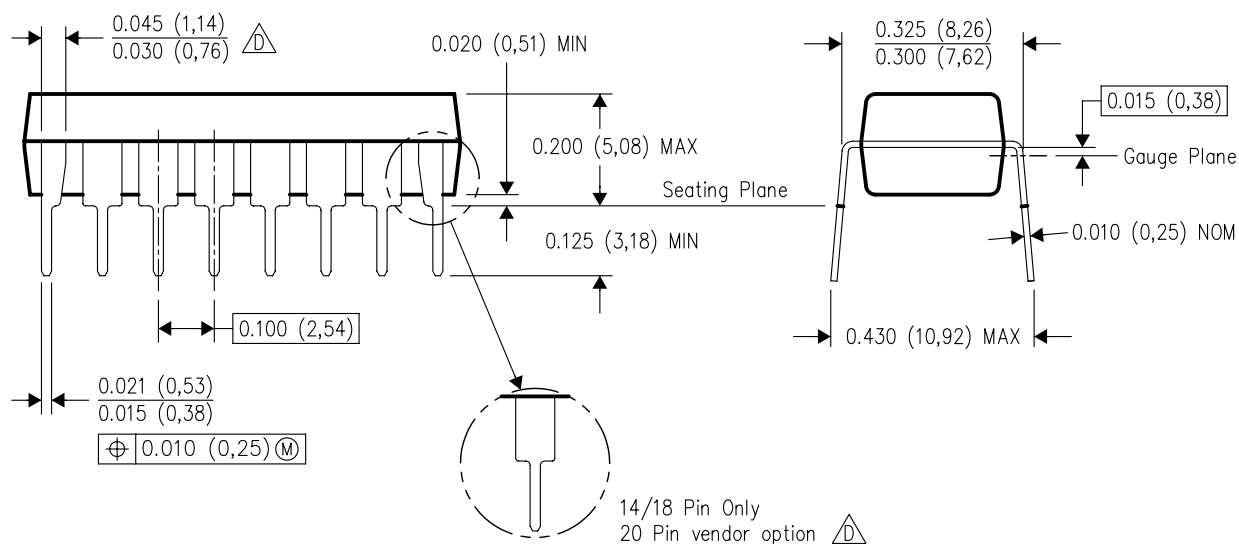
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.



**NS0016A**

**SOP - 2.00 mm max height**

SOP



NOTES:

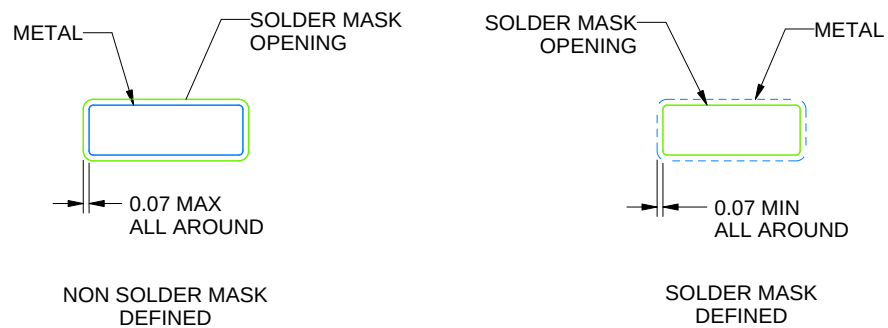
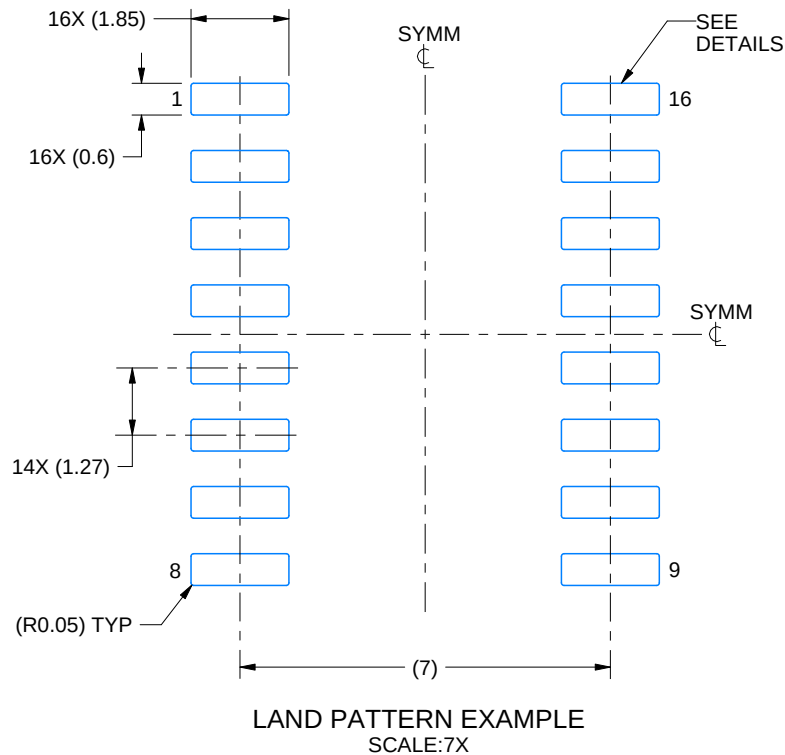
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



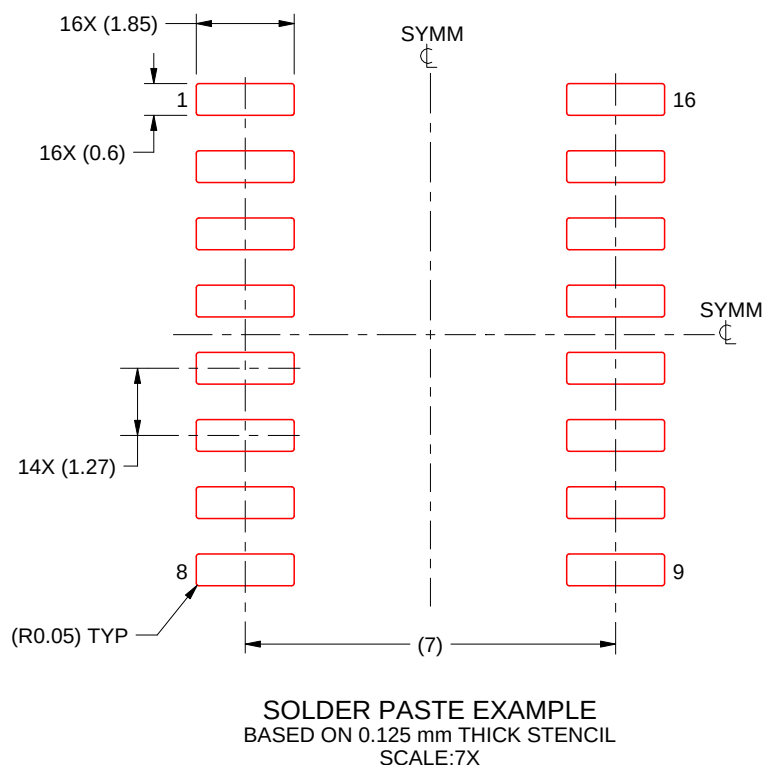
SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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