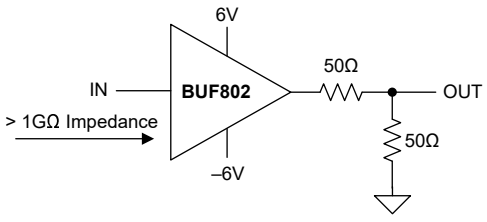
BUF802 Wide-Bandwidth, 2.3nV/√Hz, High-Input Impedance Buffer

1 Features

- Large-signal bandwidth ($1V_{PP}$): 3.1GHz
- Slew rate: 7000V/µs
- Input voltage noise: 2.3nV/√Hz
- 1% settling time: 0.7ns
- Input-impedance: 50GΩ || 2.4pF
- Capable of driving 50Ω load
- Adjustable quiescent current for power and performance trade-off
- Integrated input and output clamp with fast overdrive recovery
- Voltage supply: ±4.5V to ±6.5V
- Low phase noise

2 Applications

- Oscilloscope front-end
- High-frequency data acquisition
- High input-impedance and high slew rate T&M systems
- Oscilloscope encoder and front-end add-on cards
- Active probes
- Nondestructive testing (NDT)
- Clock drivers and clock buffers



Impedance Transformation Circuit Using the BUF802

3 Description

The BUF802 device is an open-loop, unity gain buffer with a JFET input stage that offers low-noise, high-impedance buffering for data acquisition system (DAQ) front ends. The BUF802 supports DC-to-3.1GHz of bandwidth, while offering excellent distortion and noise performance across the frequency range.

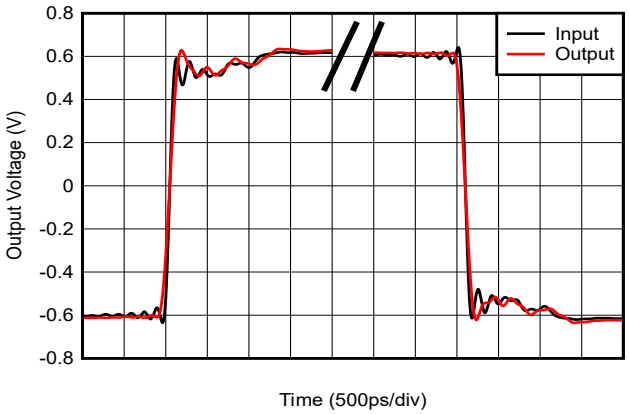
The BUF802 can be used in a composite loop with a precision amplifier in applications where higher precision performance is required. The BUF802 uses a remarkable architecture to simplify the design of high-precision, wide-bandwidth composite loops.

The BUF802 features an adjustable quiescent current pin that enables designers to trade bandwidth and distortion for a lower quiescent current. This feature makes the device an excellent choice across a wide-frequency range. The BUF802 has integrated input and output clamps to protect the device and the subsequent signal-chain from overdrive voltages.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
BUF802	RGT (VQFN, 16)	3mm × 3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Transient Response

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4 Pin Configuration and Functions

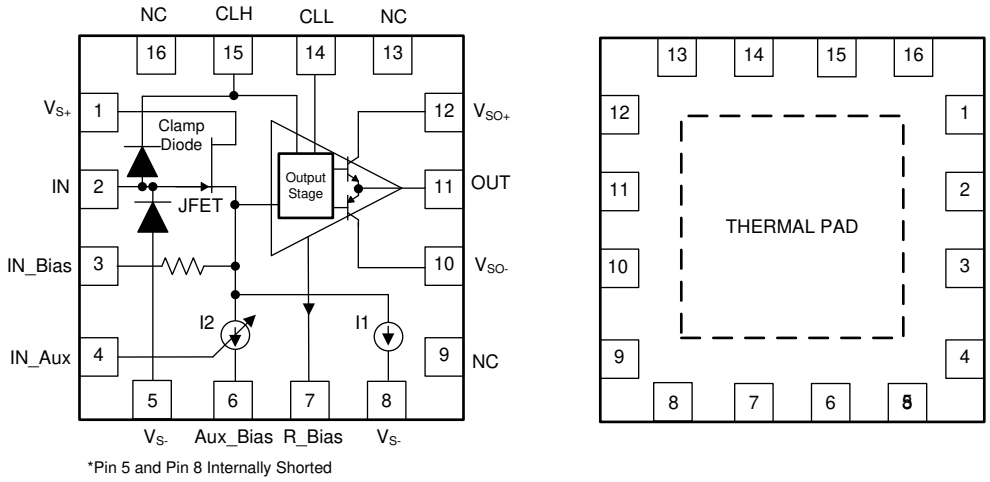


Figure 4-1. RGT Package, 16-Pin VQFN (Top View and Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[1]	OPERATING MODE[2] [3]	DESCRIPTION
NAME	NO.			
Aux_Bias	6	P	CL	Connect to $V_{S–}$ to enable control of OUT through the In_Aux
CLH	15	I	BF, CL	Input pin for setting positive clamp voltage
CLL	14	I	BF, CL	Input pin for setting negative clamp voltage
IN	2	I	BF, CL	Signal input
In_Aux	4	I	CL	Auxiliary input for controlling OUT through an external amplifier
In_Bias	3	I	CL	JFET biasing pin
NC	16, 13, 9	NC	—	Do not connect
OUT	11	O	BF, CL	Signal output
R_Bias	7	I	BF, CL	Output-stage bias-current setting pin
V_{S+}	1	P	BF, CL	Positive power supply connection for the input stage
$V_{S–}$	5, 8	P	BF, CL	Negative power supply connection for the input stage; pin 5 and pin 8 are internally shorted
V_{SO+} [4]	12	P	BF, CL	Positive power supply connection for the output stage
$V_{SO–}$ [4]	10	P	BF, CL	Negative power supply connection for the output stag
Thermal Pad		—	—	The thermal pad is electrically isolated from the die and pins; connect the thermal pad to any potential

(1) I = input, O= output, P= power, NC = no connect.
(2) See Section 7.4 for more information on *Buffer Mode (BF)* and *Composite Loop Mode (CL)* functional modes.
(3) Use pins specified as *CL* only when operating in *Composite Loop Mode*, and float these pins when operating in *Buffer Mode*.
(4) Tie V_{SO} and V_S to the same potential because these pins are internally connected to the other through back-to-back diodes.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Input stage supply voltage, $V_S = (V_{S+}) – (V_{S–})$(2)		14	V
V_{SO}	Output stage supply voltage, $V_{SO} = (V_{SO+}) – (V_{SO–})$ (2)		14	V
IN	Input voltage	$(V_{S–}) – 0.5$	(V_{S+})	V
CLH	Positive clamp voltage	Mid-supply	V_{S+}	V
CLL	Negative clamp voltage	$V_{S–}$	Mid-supply	V
	Input clamp diode		100	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Tie V_{SO} and V_S to the same potential. V_{SO} and V_S are internally connected together through back-to-back diodes.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, $V_S = (V_{S+}) – (V_{S–})$(1)	Dual-supply voltage	±4.5	±5	±6.5	V
		Single-supply voltage	9	10	13	
T_A	Ambient temperature		–40	25	85	°C

(1) The BUF802 can be used with any possible combination of V_{S+} and $V_{S–}$, but do not exceed the *Recommended Operating Conditions*.

5.4 Thermal Information

THERMAL METRIC(1)		BUF802 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	27	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics Wide Bandwidth Mode

at T_A = 25°C, V_S = ±6V, R_L = 100Ω || 400fF, R_S = 25Ω, V_{OCM} = 0V (mid-supply), CLH and CLL tied to V_{S+} and $V_{S–}$ respectively, R_Bias = 17.8kΩ, and wide bandwidth mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_{OUT} = 100m V_{PP}			3.1		GHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}			3.1		GHz
		V_{OUT} = 2 V_{PP}			1.6		
	Bandwidth for 0.1dB flatness	V_{OUT} = 1V_{PP}, R_L = 100Ω			0.6		GHz
	Bandwidth for −1dB flatness	V_{OUT} = 1V_{PP}, R_L = 100Ω			1.8		GHz
	Bandwidth for −2dB flatness	V_{OUT} = 1V_{PP}, R_L = 50Ω			2.4		GHz
SR	Slew rate	V_{OUT} = 1.2V step, V_{IN} slew rate = 13000V/µs			7000		V/µs
	Rise and fall time	V_{OUT} = 1.2V step (10% to 90%)			0.16		ns
		V_{OUT} = 0.25V step (10% to 90%)			0.15		
	Settling time to 0.1%	V_{OUT} = 1.2V step, V_{IN} slew rate = 13000V/µs			1.3		ns
	Settling time to 1%	V_{OUT} = 1.2V step, V_{IN} slew rate = 13000V/µs			0.7		ns
e_n	Voltage noise	1/f corner			18		kHz
		f = 100MHz in BF mode and CL mode			2.3		nV/√Hz
i_n	Current noise	f = 10kHz			1.5		fA/√Hz
HD2/HD3	Harmonic distortion	V_{OUT} = 2 V_{PP}	f = 500MHz		–68/–58		dBc
		V_{OUT} = 1 V_{PP}	f = 1GHz		–55/–59		
			f = 2GHz		–45/–49		
			f = 2GHz, R_L = 50Ω		–43/–41		
DC PERFORMANCE							
V_{OS}	Input offset voltage	V_{OUT} – V_{IN}			600	800	mV
		T_A = –40°C to +85°C				900	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C			±700	±1330	µV/°C
I_B	Input bias current				3	25	pA
		T_A = –40°C to +85°C				220	
I_{AB}	Auxiliary input bias current				44	140	µA
		T_A = –40°C to +85°C				200	
G	DC gain	V_{OUT} = ± 0.5V	R_L = 200Ω	0.97	0.978	0.99	V/V
			R_L = 100Ω	0.96	0.971	0.98	
			R_L = 50Ω	0.95	0.961	0.97	
		V_{OUT} = ± 0.5V, T_A = –40°C to +85°C	R_L = 200Ω	0.97		0.99	
			R_L = 100Ω	0.96		0.98	
			R_L = 50Ω	0.94		0.97	

5.5 Electrical Characteristics Wide Bandwidth Mode (continued)

at T_A = 25°C, V_S = ±6V, R_L = 100Ω || 400fF, R_S = 25Ω, V_{OCM} = 0V (mid-supply), CLH and CLL tied to V_{S+} and $V_{S–}$ respectively, R_Bias = 17.8kΩ, and wide bandwidth mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
Z_{IN}	Input impedance	f = 100MHz			50 || 2.4		GΩ || pF
	Input clamp current rating	Continuous current rating			100		mA
V_{CLH}	High side clamp voltage(1)			0		V_{S+}	V
V_{CLL}	Low side clamp voltage(1)			$V_{S–}$		0	V
	CLH clamping time	Time taken to clamp V_{OUT} to V_{CLH} during overdrive			0.2		ns
	CLL clamping time	Time taken to clamp V_{OUT} to V_{CLL} during overdrive			0.2		ns
	Input voltage	THD = –40dBc	f = 500MHz		4.5		V_{PP}
			f = 1GHz		2.1		V_{PP}
			f = 2GHz		1.2		V_{PP}
OUTPUT							
	Output swing	T_A = 25°C		$V_{S–}$ + 3.4		V_{S+} – 1.9	V
		T_A = –40°C to +85°C		$V_{S–}$ + 3.4		V_{S+} – 2.0	V
Z_O	Output impedance	f = 100MHz			1.2		Ω
AUXILIARY INPUT							
G_{AUX}	V_{OUT} / In_Aux gain	At low frequency (V_{IN} is left floating)		6.15		20	V/V
		At crossover frequency (V_{IN} shorted to GND)		0.18	0.26		V/V
	Default voltage at In_Aux	Driving In_Aux to default voltage results in V_{OUT} = mid-supply		$V_{S–}$ + 2.3	$V_{S–}$ + 3	$V_{S–}$ + 3.8	V
	In_Aux input voltage	At crossover frequency		$V_{S–}$ + 1.0		$V_{S–}$ + 5.0	V
G_{AUX} BW	V_{OUT} / In_Aux bandwidth				800		MHz
	RHF	Resistance between In_Bias to JFET source			100		kΩ
POWER SUPPLY							
I_Q	Quiescent current	I_{OUT} = 0mA (R_bias = 17.8kΩ)			34	37	mA
			T_A = –40°C to +85°C		35.5		mA
			CL Mode enabled		36	40	mA
PSRR	Power-supply rejection ratio	PSRR at 100kHz on V_{S+}			49		dB
		PSRR at 100kHz on $V_{S–}$			38		dB

(1) The 0V limits are for bipolar and balanced power supplies. For other supply configurations mid-supply sets the minimum limit for V_{CLH} and maximum limit for V_{CLL}.

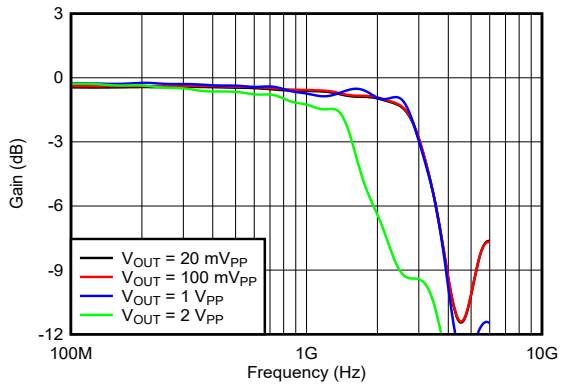
5.6 Electrical Characteristics Low Quiescent Current Mode

at T_A = 25°C, V_S = ±6V, R_L = 100Ω || 400 fF, R_S = 25Ω, V_{OCM} = 0V (mid-supply), CLH and CLL tied to V_{S+} and $V_{S–}$ respectively, R_Bias = 35.7kΩ, and low quiescent current mode (unless otherwise specified)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_{OUT} = 100mV_{PP}			2.6		GHz
LSBW	Large-signal bandwidth	V_{OUT} = 1V_{PP}			2		GHz
		V_{OUT} = 2V_{PP}			0.7		
	Bandwidth for 0.1dB flatness	V_{OUT} = 1V_{PP}			0.45		GHz
	Bandwidth for –1dB flatness	V_{OUT} = 1V_{PP}			1.4		GHz
SR	Slew rate	V_{OUT} = 1.2V step, V_{IN} slew rate = 13000V/µs			5500		V/µs
	Rise and fall time	V_{OUT} = 1.2V step (10% to 90%)			0.3		ns
		V_{OUT} = 0.25V step (10% to 90%)			0.16		
	Settling time to 0.1%	V_{OUT} = 1.2V step, V_{IN} slew rate = 13000V/µs			1.4		ns
	Settling time to 1%	V_{OUT} = 1.2V step, V_{IN} slew rate = 13000V/µs			0.8		
e_n	Voltage noise	1/f corner			10		kHz
		f = 100MHz			2.2		nV/√Hz
i_n	Current noise	f = 10kHz			1.5		fA/√Hz
HD2/HD3	Harmonic distortion	V_{OUT} = 2V_{PP}	f = 500MHz		–35/–32		dBc
		V_{OUT} = 1V_{PP}	f = 100MHz		–80/–77		
			f = 500MHz		–56/–54		
DC PERFORMANCE							
G	DC gain	V_{OUT} = ±0.5V	R_L = 200Ω	0.96	0.975	0.99	V/V
			R_L = 100 Ω	0.95	0.963	0.98	
		V_{OUT} = ±0.5V, T_A = –40°C to +85°C	R_L = 200Ω	0.96		0.99	
			R_L = 100Ω	0.95		0.98	
INPUT							
	CLH clamping time	Time taken to clamp V_{OUT} to V_{CLH} during overdrive			0.3		ns
	CLL clamping time	Time taken to clamp V_{OUT} to V_{CLL} during overdrive			0.7		
OUTPUT							
Z_O	Output impedance	f = 100MHz			1.2		Ω
POWER SUPPLY							
I_Q	Quiescent current	I_{OUT} = 0mA (R_bias = 35.7kΩ)			21	24	mA
			T_A = –40°C to +85°C		22		

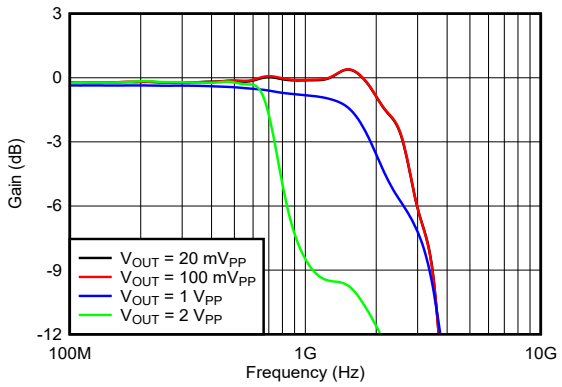
5.7 Typical Characteristics

at T_A = 25°C, V_S = ±6V, R_L = 100Ω || 400fF, R_S = 25 Ω, V_{OCM} = 0V (mid-supply), CLH and CLL tied to V_{S+} and $V_{S–}$, respectively, R_Bias = 17.8kΩ, and wide bandwidth mode (unless otherwise noted)



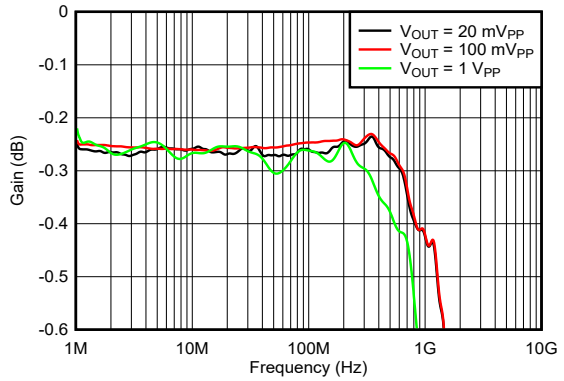
Wide Bandwidth mode

Figure 5-1. Frequency Response vs Output Voltage



Low Quiescent Current mode

Figure 5-2. Frequency Response vs Output Voltage



Wide Bandwidth mode

Figure 5-3. Frequency Response vs Output Voltage, 0.1dB Flatness

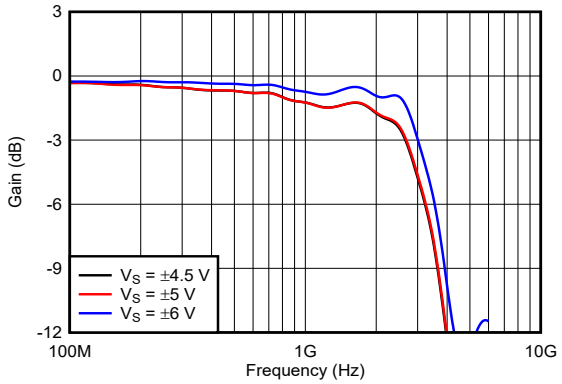


Figure 5-4. Frequency Response vs Supply Voltage

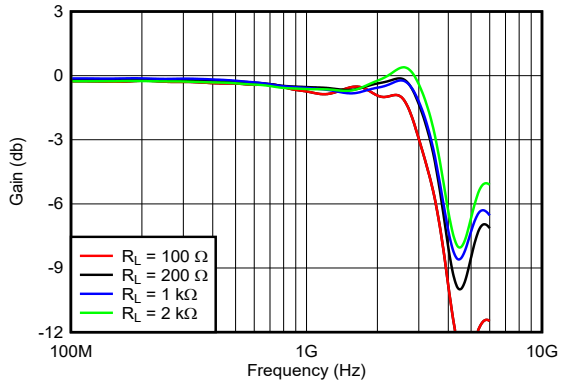


Figure 5-5. Frequency Response vs Output Load

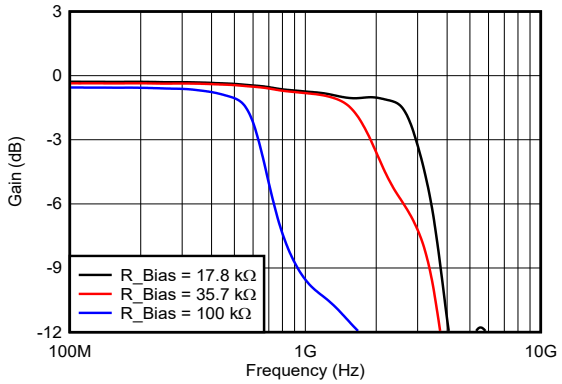


Figure 5-6. Frequency Response vs R_Bias Resistance

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±6V, R_L = 100Ω || 400fF, R_S = 25 Ω, V_{OCM} = 0V (mid-supply), CLH and CLL tied to V_{S+} and $V_{S–}$, respectively, R_Bias = 17.8kΩ, and wide bandwidth mode (unless otherwise noted)

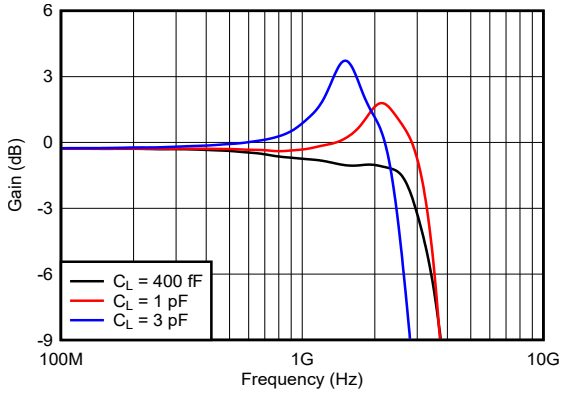


Figure 5-7. Frequency Response vs Capacitive Load

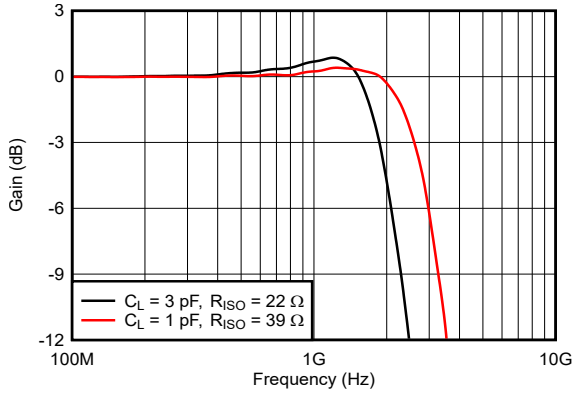
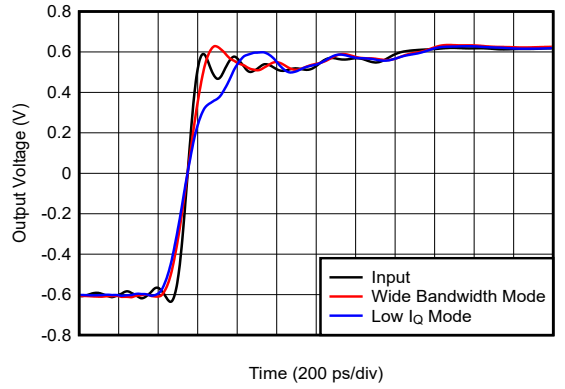
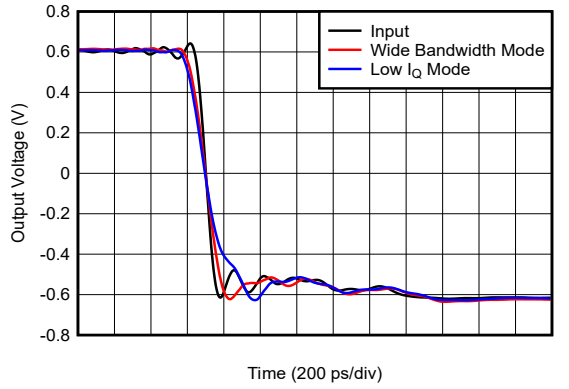


Figure 5-8. Frequency Response vs Capacitive Load With Recommended R_{ISO}



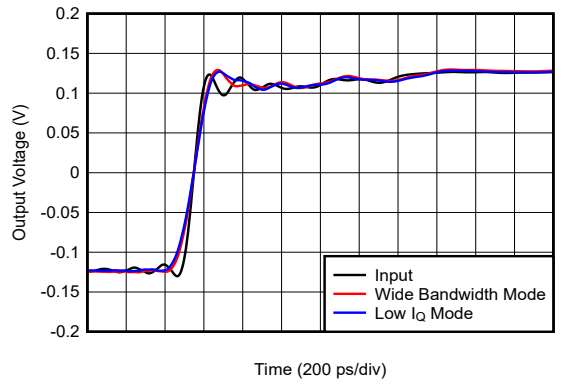
Rising edge, V_{OUT} = 1.2 V_{PP}

Figure 5-9. Large-Signal Transient Response



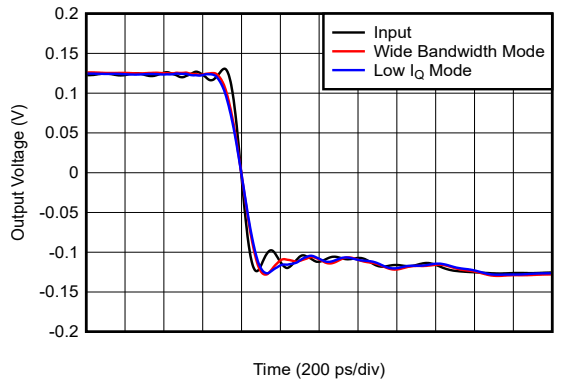
Falling edge, V_{OUT} = 1.2 V_{PP}

Figure 5-10. Large-Signal Transient Response



Rising edge, V_{OUT} = 250 m V_{PP}

Figure 5-11. Small-Signal Transient Response



Falling edge, V_{OUT} = 250 m V_{PP}

Figure 5-12. Small-Signal Transient Response

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±6V, R_L = 100Ω || 400fF, R_S = 25 Ω, V_{OCM} = 0V (mid-supply), CLH and CLL tied to V_{S+} and $V_{S–}$, respectively, R_Bias = 17.8kΩ, and wide bandwidth mode (unless otherwise noted)

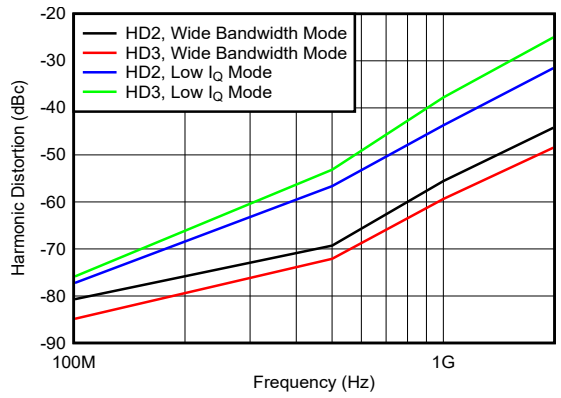


Figure 5-13. Harmonic Distortion vs Frequency

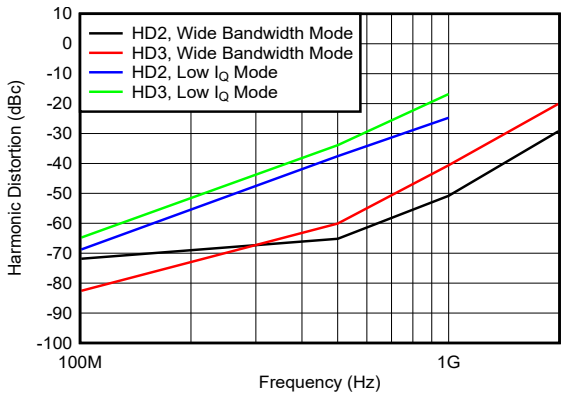


Figure 5-14. Harmonic Distortion vs Frequency

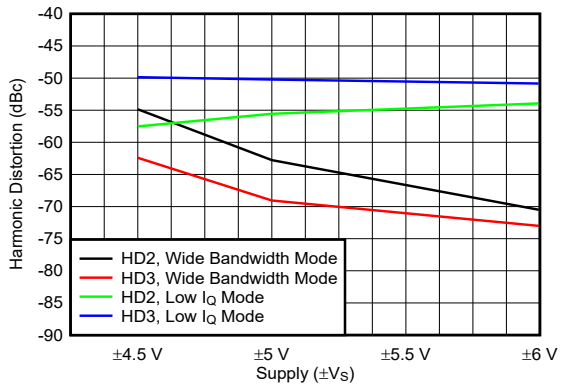


Figure 5-15. Harmonic Distortion vs Supply Voltage

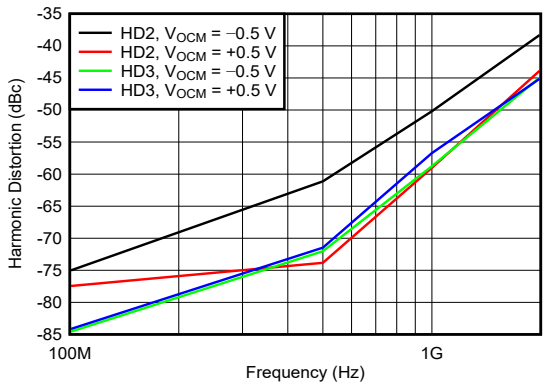


Figure 5-16. Harmonic Distortion vs Output Common-Mode Voltage

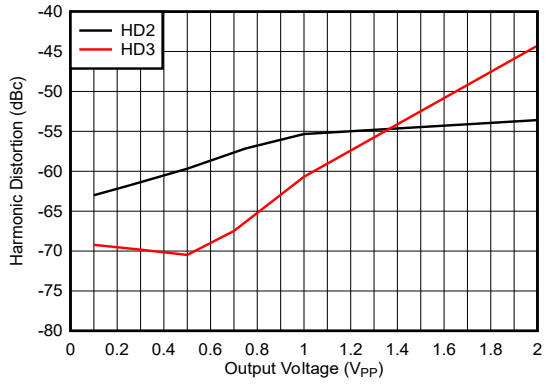


Figure 5-17. Harmonic Distortion vs Output Voltage

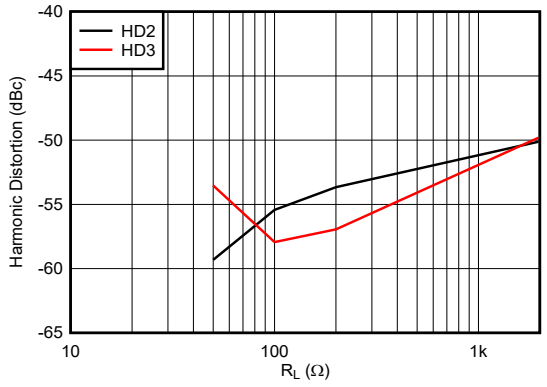


Figure 5-18. Harmonic Distortion vs Output Load

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±6V, R_L = 100Ω || 400fF, R_S = 25 Ω, V_{OCM} = 0V (mid-supply), CLH and CLL tied to V_{S+} and $V_{S–}$, respectively, R_Bias = 17.8kΩ, and wide bandwidth mode (unless otherwise noted)

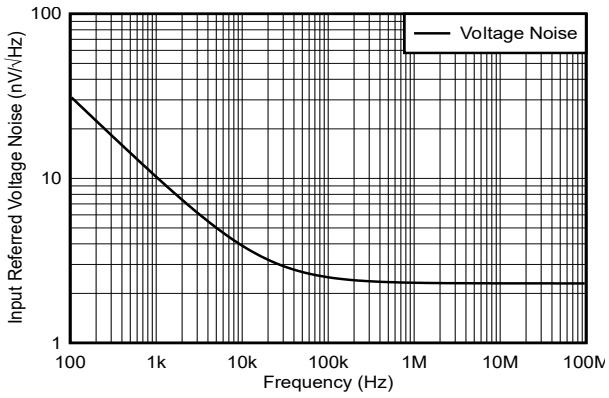


Figure 5-19. Voltage Noise Density vs Frequency

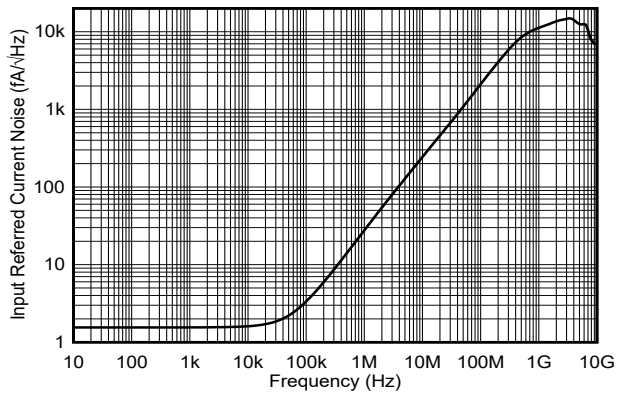
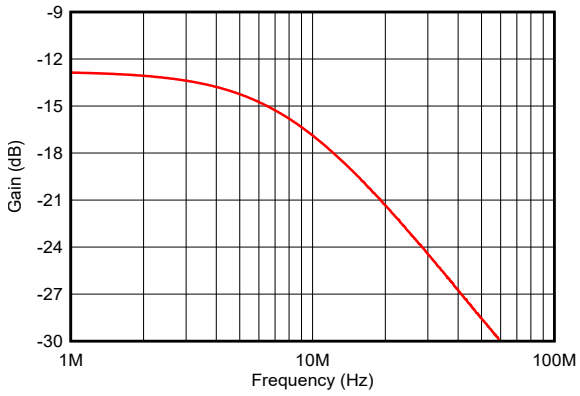


Figure 5-20. Current Noise Density vs Frequency



With RC pole of 2kΩ and 10pF at IN_Aux pin

Figure 5-21. Auxiliary Path Frequency Response

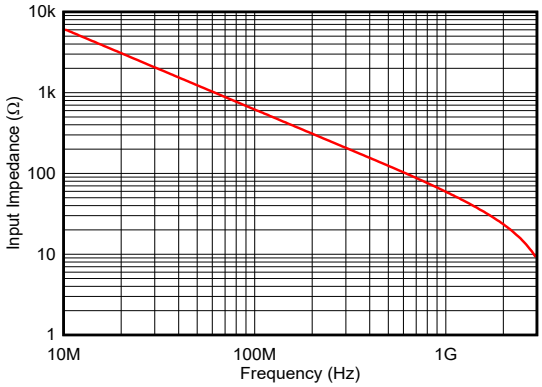


Figure 5-22. Input Impedance vs Frequency

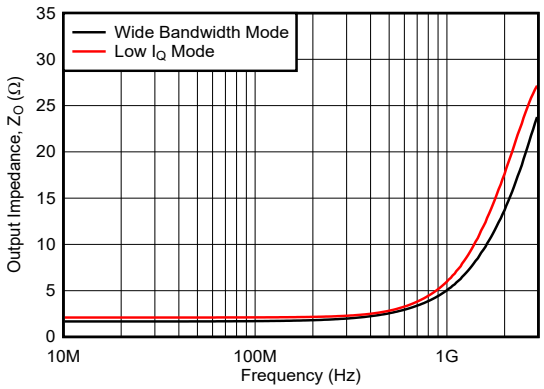
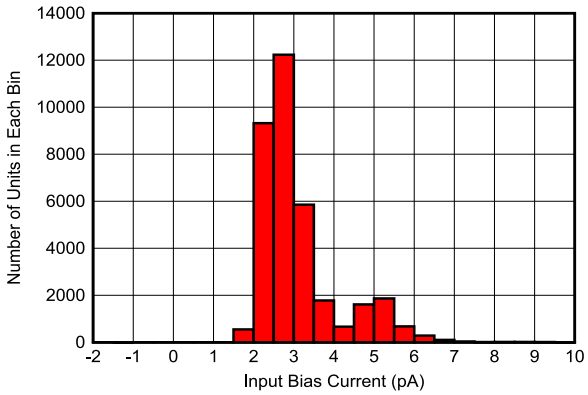


Figure 5-23. Output Impedance vs Frequency



μ = 3.1 pA, σ = 1.03 pA

Figure 5-24. Input Bias Current Distribution

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±6V, R_L = 100Ω || 400fF, R_S = 25 Ω, V_{OCM} = 0V (mid-supply), CLH and CLL tied to V_{S+} and $V_{S–}$, respectively, R_Bias = 17.8kΩ, and wide bandwidth mode (unless otherwise noted)

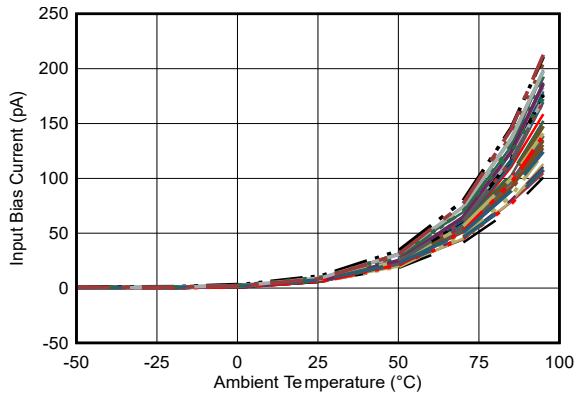


Figure 5-25. Input Bias Current vs Temperature

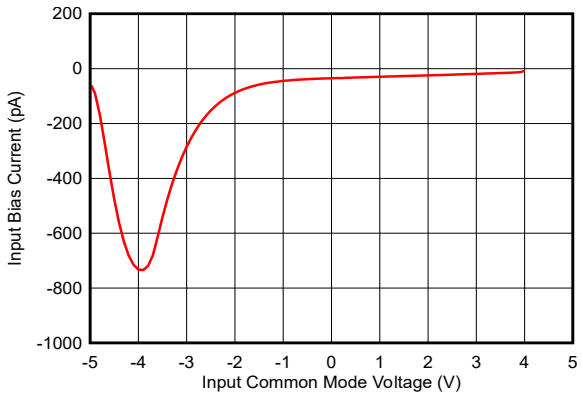


Figure 5-26. Input Bias Current vs Input Common-Mode Voltage

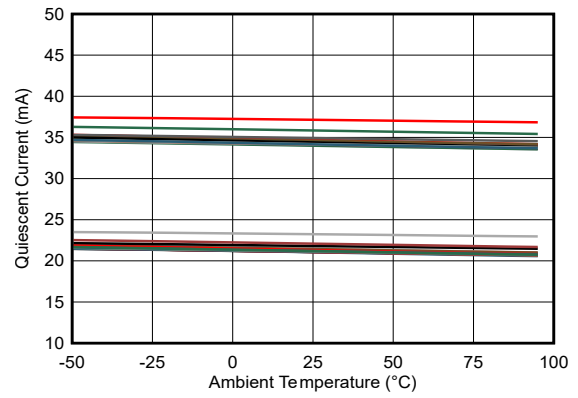


Figure 5-27. Quiescent Current vs Temperature

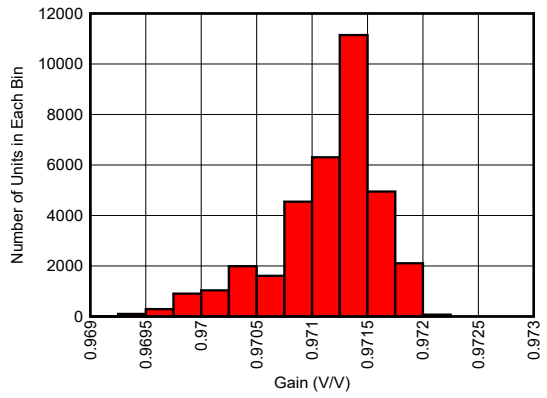


Figure 5-28. DC Gain Histogram

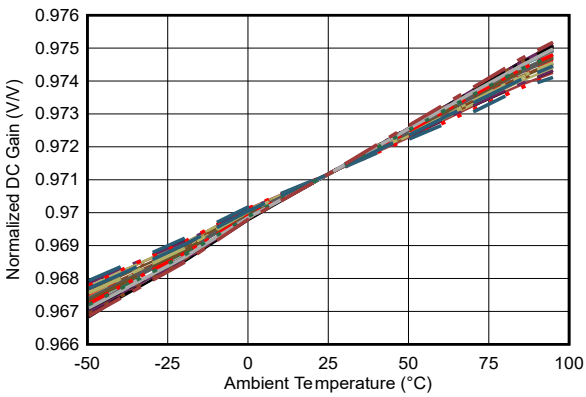


Figure 5-29. DC Gain vs Temperature

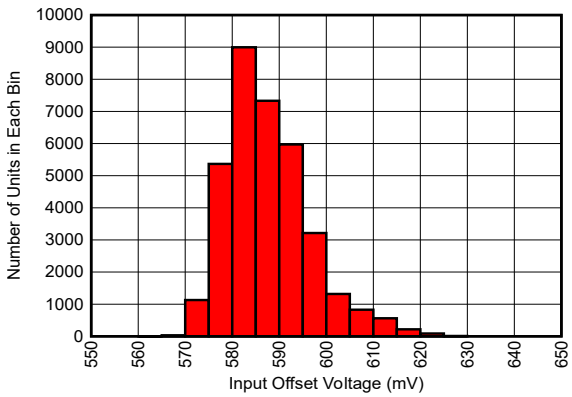


Figure 5-30. Offset Voltage Histogram

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±6V, R_L = 100Ω || 400fF, R_S = 25 Ω, V_{OCM} = 0V (mid-supply), CLH and CLL tied to V_{S+} and $V_{S–}$, respectively, R_Bias = 17.8kΩ, and wide bandwidth mode (unless otherwise noted)

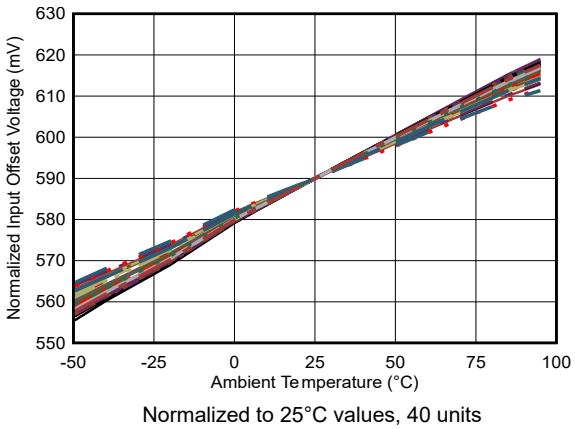


Figure 5-31. Offset Voltage vs Temperature

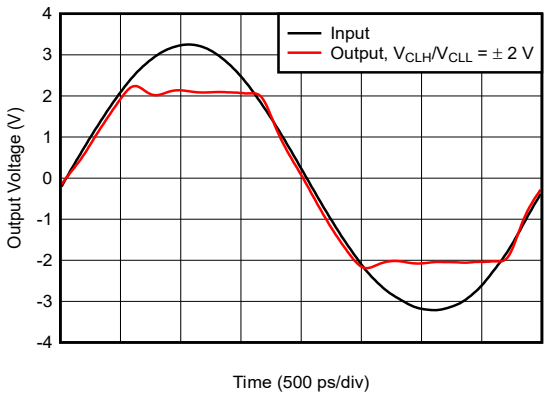


Figure 5-32. Transient Clamp Response

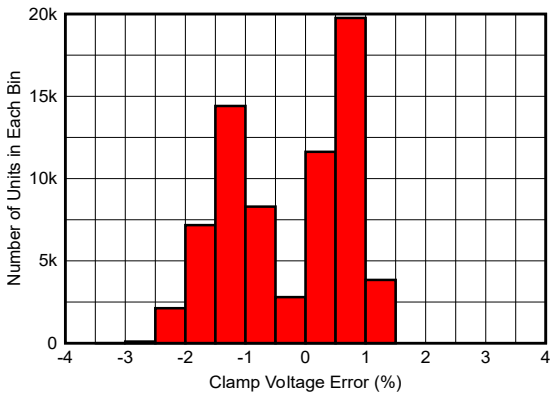


Figure 5-33. Clamp Voltage Error Histogram

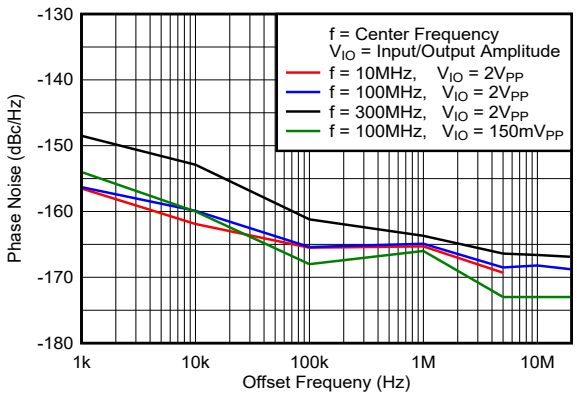


Figure 5-34. Phase Noise

6 Parameter Measurement Information

Figure 6-1 through Figure 6-3 show the various test setup configurations for the BUF802.

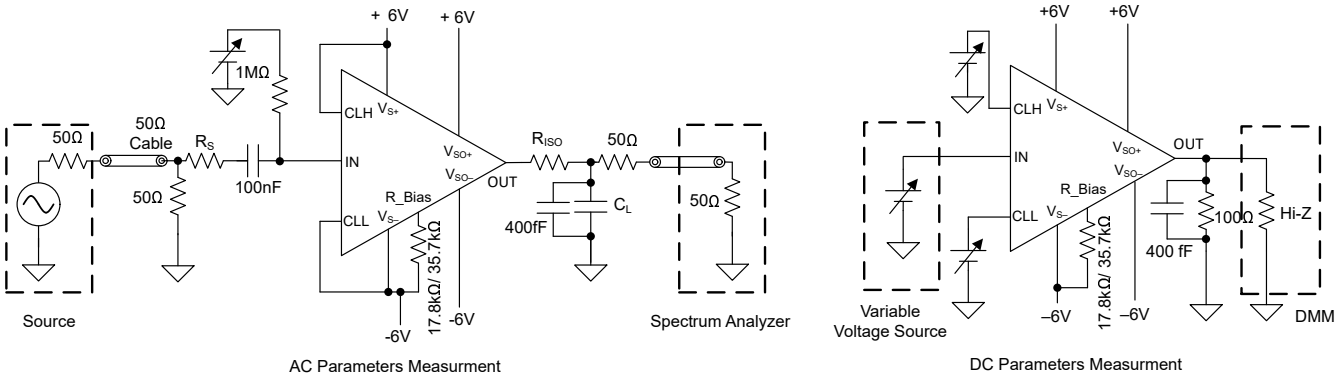


Figure 6-1. Main Path Electrical Characteristics Measurement

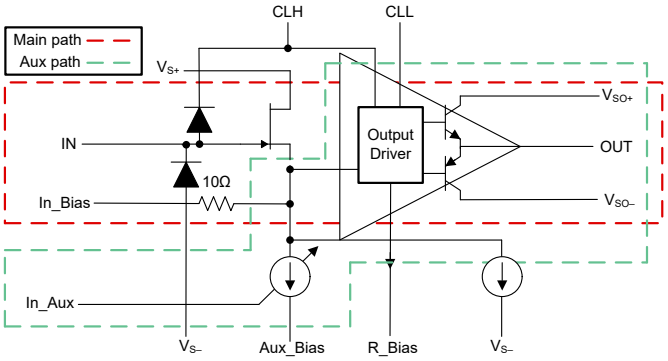


Figure 6-2. Main Path and Auxiliary Path

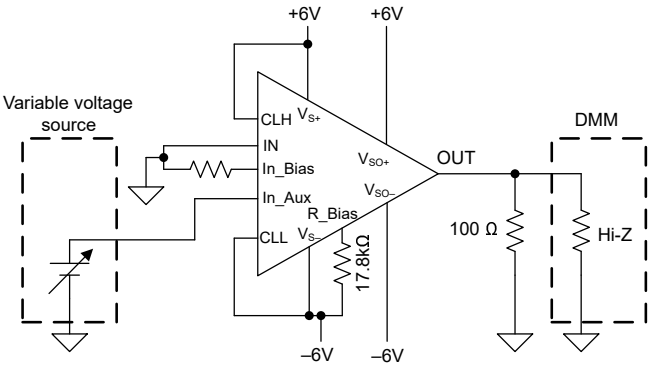


Figure 6-3. Auxiliary Path Electrical Characteristics Measurement

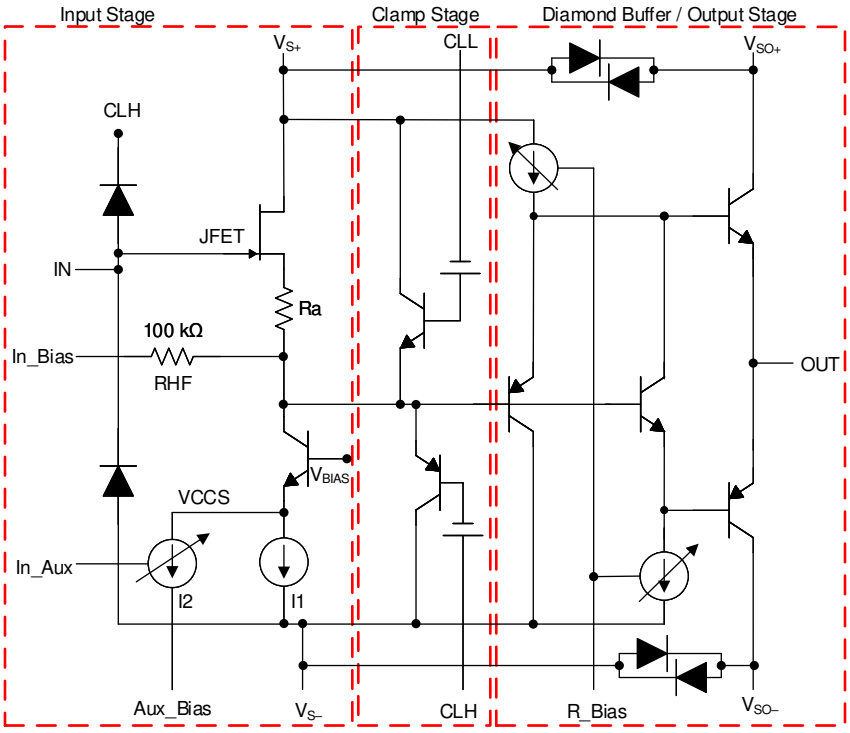
Figure 6-2 shows the two inputs for BUF802 (IN and In_Aux) which control the output. The IN pin controls the output of BUF802 through the Main Path, whereas the In_Aux pin controls the output through the Auxiliary Path. Either the Main Path or the Auxiliary Path, can be used to steer the output. The electrical characteristics of the Main Path and the Auxiliary Path is specified in Section 5.7.

7 Detailed Description

7.1 Overview

The BUF802 device is a high input-impedance, open-loop buffer used in signal acquisition front-end applications. The BUF802 is used as a standalone buffer in *Buffer Mode (BF Mode)*, or in a composite loop with a precision amplifier in *Composite Loop Mode (CL Mode)* to achieve DC precision and a wide, large-signal bandwidth. The low output impedance and high output current drive strength enables the BUF802 to drive loads as large as 50Ω. The BUF802 comes with adjustable quiescent current to customize system level power and performance trade-offs.

7.2 Functional Block Diagram



The functional block diagram shows an overview of the internal structure of the BUF802. The internal schematic of the BUF802 is divided into the following three parts:

- **Input Stage**: consists of a low-noise JFET with biasing circuitry. The input stage is configurable in two modes: *BF Mode* and *CL Mode*. Choosing one of the two modes affects the circuit operation of the input stage. The clamp and output stage operation are unaffected by the mode selection. Section 7.4 describes the two modes in greater detail.
- **Clamp Stage**: provides the following functions:
  1. Protects the input of the BUF802 against large input signal transients through diode clamps to V_{S-} and CLH.
  2. Prevents the output voltage of the BUF802 from exceeding the voltage at the CLH and CLL.
- **Output Stage**: tracks the JFET source voltage and is optimized to drive 50Ω and 100Ω loads while maintaining signal fidelity.

7.3 Feature Description

7.3.1 Input and Output Overvoltage Clamp

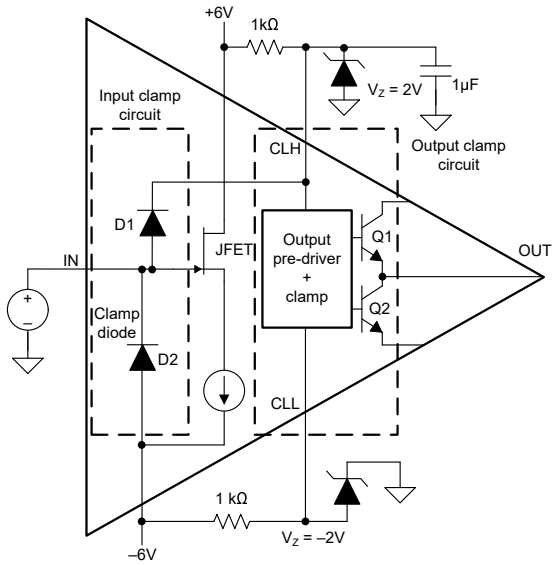


Figure 7-1. Internal Input and Output Overvoltage Clamp

The BUF802 device integrates an input and output clamp circuit. The input clamp protects the BUF802 from large input transients and the output clamp protects the subsequent stages from being overdriven.

- **Input Clamp Circuit**:
  - Figure 7-1 shows the input of the BUF802 tied to pins CLH and V_{S-} through two internal clamp diodes, D1 and D2. The diodes are rated for 100mA of continuous current and withstand much higher transient currents. If the JFET input voltage exceeds the voltage at CLH or $V_{S–}$, the diodes are forward biased, clamping the JFET to CLH and V_{S-}. A 1µF capacitor connected in parallel to the zener diode helps in transient absorption traveling through the D1 diode.
  - Figure 7-2 shows how the external clamping diodes is used in cases where the 100mA current rating of D1 and D2 is insufficient. When using external clamping, disable the internal protection of the BUF802 by connecting CLH and CLL to V_{S+} and $V_{S–}$.

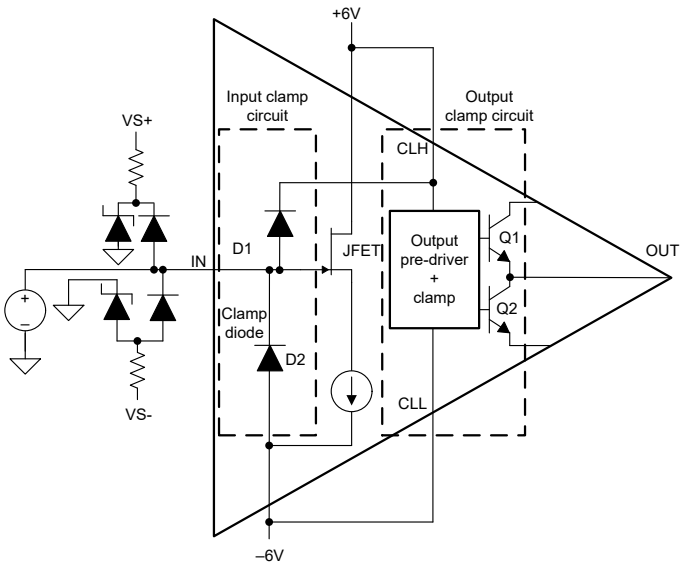


Figure 7-2. External Input Clamp Circuit

- **Output Clamp Circuit**:
  - The output protection circuit prevents the stages following the BUF802 from being overdriven. This circuit also helps the BUF802 recover rapidly from a saturated state resulting from an input- or output-overdrive condition. In a typical data-acquisition system, the BUF802 is followed by a variable gain amplifier (VGA). High-speed VGAs are typically designed on 5V processes, making the device susceptible to potential damage from the 12V BUF802. The voltage applied to the CLH and CLL pins dictate the maximum output swing of the BUF802.
  - Figure 7-2 shows that the internal clamps are disabled by connecting CLH to V_{S+} and CLL to V_{S-}. When the clamps are disabled, the maximum output swing is limited by the output swing specification described in Section 5.5. Section 5.7 shows the response time and accuracy of the output clamp.
  - The output THD of the BUF802 degrades when V_{CLH} and V_{CLL} are set close to the expected V_{OUT} peak value. To prevent signal degradation, maintain at least a 1.5V difference between the expected peak output voltage and the clamp voltage applied at the CLH and CLL pins. Figure 7-3 shows the relation between the absolute clamp voltage value and THD for a 1 V_{PP} output.

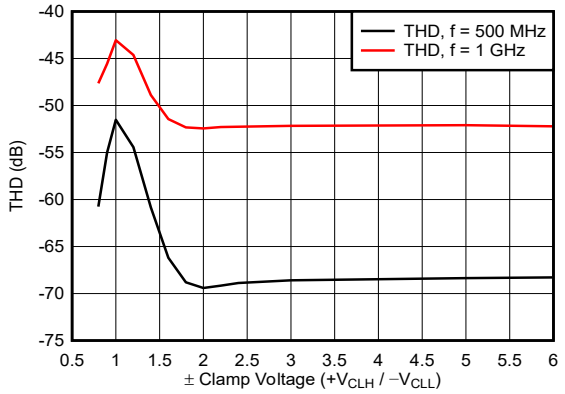


Figure 7-3. THD vs V_{CLH} / V_{CLL} for V_{OUT} = 1 V_{PP}

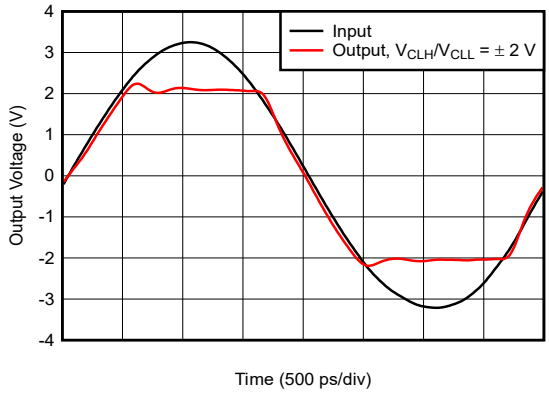


Figure 7-4. Transient Clamp Response

7.3.2 Adjustable Quiescent Current

The BUF802 includes an adjustable quiescent current feature to allow the system designer to trade off the current consumed versus the distortion performance obtained. Section 7.2 shows connecting a resistor between R_Bias and V_{S-} to set the bias point operating current of the output stages. Figure 7-5 shows the quiescent current variation as a function of the R_Bias value.

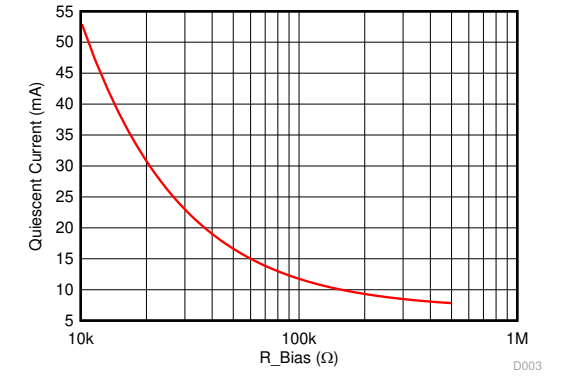


Figure 7-5. Quiescent Current vs R_Bias

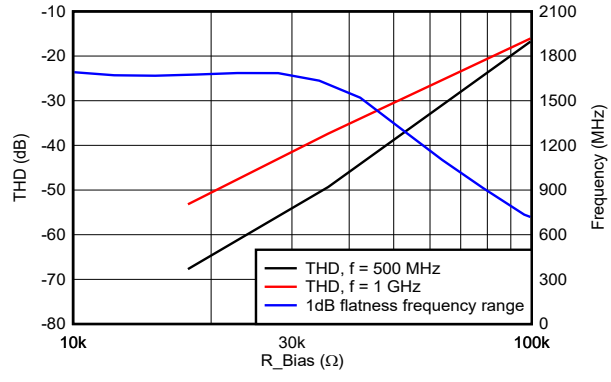


Figure 7-6. THD and Bandwidth vs R_Bias

The Figure 7-6 shows that changing the resistor between the R_Bias and V_{S-} primarily affects the THD of the output signal. Section 5.5 and Section 5.6 specify the AC and DC parameters of the BUF802 at two different R_Bias values. The DC parameters are independent of the quiescent current setting.

7.3.3 ESD Structure

Figure 7-7 shows the internal ESD structure of the BUF802. V_{SO} and V_S supply pins are internally shorted to each other through back-to-back diodes. See also Section 8.3. The input ESD diodes D1 and D2 are specified to carry 100mA of continuous current while the remaining ESD diodes are rated for 10mA.

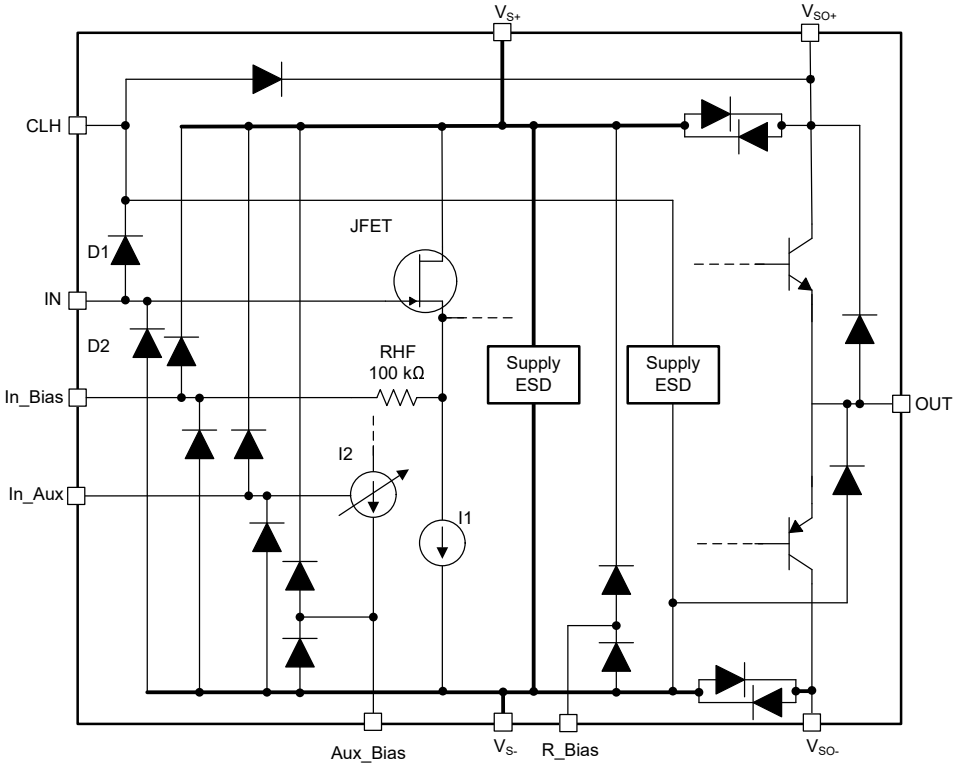


Figure 7-7. Internal ESD Structure

7.4 Device Functional Modes

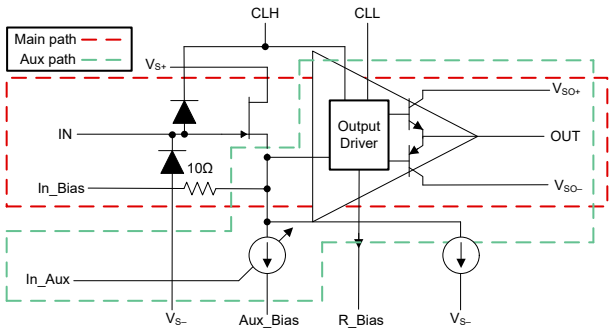


Figure 7-8. Main Path and Auxiliary Path

The BUF802 is designed to operate in two modes: *Buffer Mode (BF Mode)* and *Composite Loop Mode (CL Mode)*.

In *BF Mode*, the BUF802 uses the JFET, output driver and bipolar transistors in the Main Path to reproduce the signal, applied on IN, at the output of the BUF802. Figure 7-8 shows the Main Path and the Auxiliary Path of the BUF802. The BUF802 operates from DC to high-frequency, and is therefore usable as a standalone buffer. When used in *BF Mode*, only the Main Path of the BUF802 is used.

In *CL Mode*, the BUF802 uses the Auxiliary signal path and the Main Path to control the output voltage. As the name suggests in the *Composite Loop Mode*, the BUF802 is used in a composite loop with a precision amplifier to achieve simultaneous DC precision and a wide, large-signal bandwidth. The composite loop splits the applied signal to low-frequency and high-frequency components and passes the signal over to different circuits with an appropriate transfer function. The low-frequency and high-frequency signal components then recombine inside the BUF802 and are reproduced at the OUT pin.

7.4.1 Buffer Mode (BF Mode)

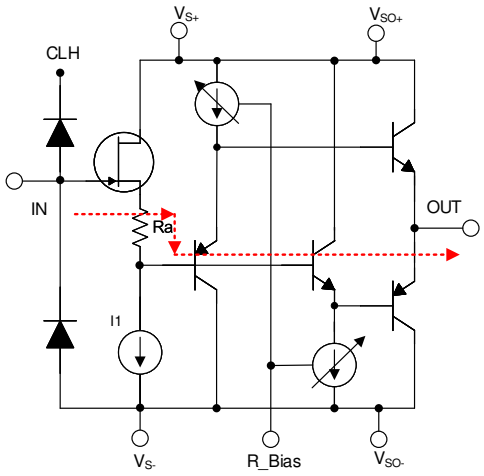


Figure 7-9. Internal Schematic – *BF Mode*

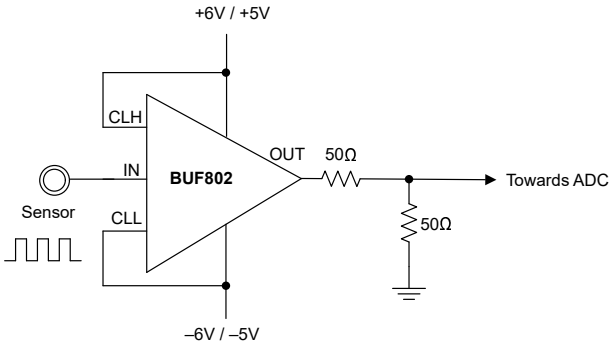


Figure 7-10. BUF802 DC Mode

The BUF802 operates in DC mode to buffer signals in applications such as clock buffers, peak detector, and non precision signal chains.

- The input of the BUF802 is a JFET input, presenting a very high impedance, minimizing loading of sensor or signal sources.

- The output provides a low impedance drive, allowing direct connection to ADCs or multiplexers, including resistive loads up to 50Ω.
- The composite feedback loop is disabled during DC mode operation; therefore, DC correction is not applied, and a small DC error can be observed at the output, refer to Section 5.5.
- This mode is an excellent choice for sensor interfacing, DC signal acquisition, peak detection, and impedance transformation.

7.4.1.1 BUF802 Used in BF Mode for Clock Buffer

BUF802 is used as a single-ended clock buffer for point-to-point clock distribution. The wide bandwidth and high slew rate and the linear class AB architecture of BUF802 allow for sine wave clock support with very low phase noise as shown in Figure 5-34. The device provides strong output drive capability, making a appropriate for the driving capacitive loads or transmission lines.

7.4.2 Composite Loop Mode (CL Mode)

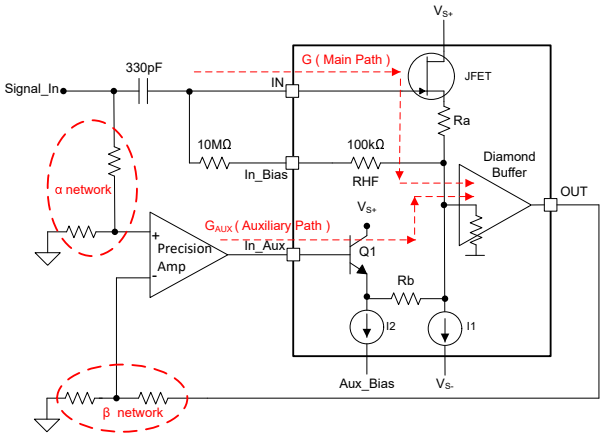


Figure 7-11. Internal Schematic – *CL Mode*

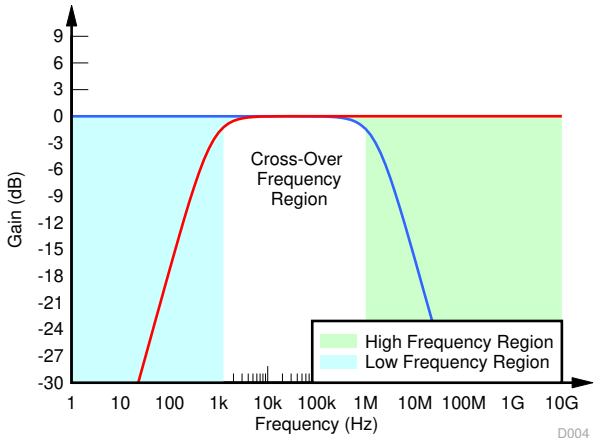


Figure 7-12. *CL Mode* Frequency Response

The 330pF input series capacitor shown in Figure 7-11 splits the input signal into low-frequency and high-frequency components. The low-frequency input signal component is applied to In_Aux and the high-frequency input signal component is applied to IN. The IN pin controls the output of BUF802 through the Main Path, whereas the In_Aux pin controls the output through the Auxiliary Path.

The transfer function of the composite loop in *CL Mode* can be split into the following three frequency regions:

1. **Low Frequency Region**: The gain of the composite loop in the low-frequency region is α/β (determined by α and β network). In the low-frequency region, the 330pF input capacitor presents a high-impedance in the Main Path, causing the signal to flow through the precision amplifier and the In_Aux pin. This region spans from DC to f_{LF}. f_{LF} is the pole resulting from the gain bandwidth of the precision amplifier, the Auxiliary Path bandwidth, and parasitic capacitance of the components along the path.
2. **High Frequency Region**: In the high-frequency region, the precision amplifier and the Auxiliary Path run out of bandwidth. The net gain of the composite loop in this region is determined solely by the Main Path gain of the BUF802, which is denoted by G. This region spans from the pole created at f_{HF} till the LSBW of the BUF802. The f_{HF} is the pole resulting from the 330pF series capacitor and the 10MΩ resistor on the In_Bias pin.
3. **Crossover Frequency Region**: the Main Path and Auxiliary Path work in conjunction to determine the gain in the crossover region. To maintain a flat frequency response in this region, the following conditions must be met:
   a. α/β = G
   b. High frequency response pole f_{HF}<< Low frequency pole f_{LF}

A detailed analysis of discrete component selection to achieve a flat frequency response is discussed further in Section 8.1.

7.4.2.1 Alternative Approach for Realizing Composite Loop

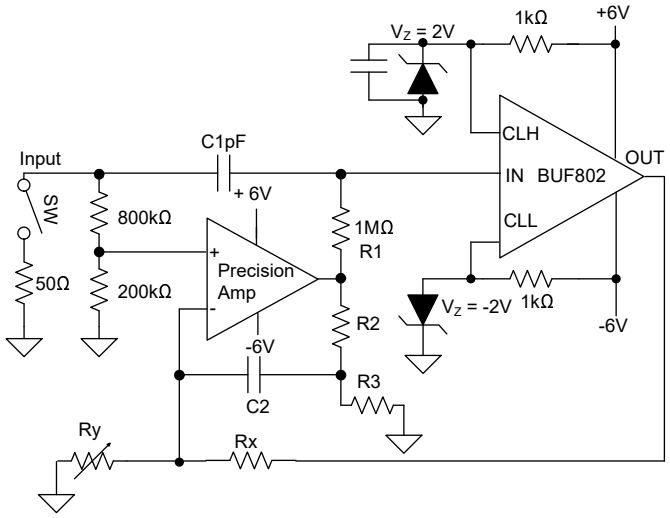


Figure 7-13. Composite Loop Using *BF Mode*

Figure 7-9 shows the BUF802 used in a composite loop without using auxiliary path. This schematic represents an alternative approach of implementing composite loop with BUF802. The low-frequency and high-frequency signals are combined externally through the discrete components R1 and C1 before being applied at the IN pin of BUF802.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The BUF802 offers a wide large-signal bandwidth, high-slew rate along with high-input impedance making this device an excellent choice for data acquisition systems. In applications where DC precision is not needed, or in cases where the input is AC coupled, the BUF802 is usable as a standalone input buffer in *BF Mode*. In case the precision required is greater than that offered by the BUF802, operate the BUF802 in *CL Mode* with a precision amplifier in a composite loop.

8.2 Typical Applications

8.2.1 Oscilloscope Front-End Amplifier Design

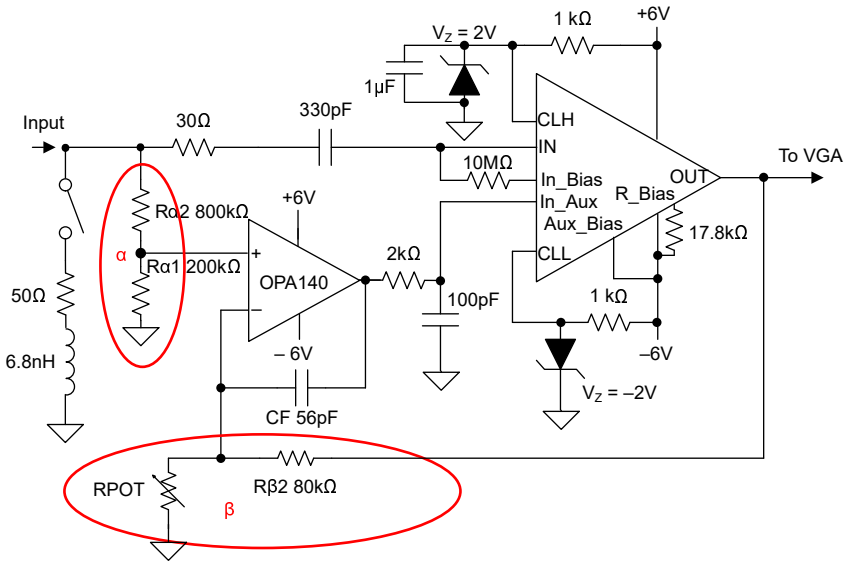


Figure 8-1. Oscilloscope Front-End Amplifier

8.2.1.1 Design Requirements

The following table shows the target specification for a 1GHz oscilloscope front-end and precision amplifier.

SPECIFICATION	VALUE
Input impedance	1MΩ / 50Ω
S parameters (f = 1GHz)	S11 = –15dB, S21 = –1.5dB
Offset drift	1µV/°C, maximum
Noise at highest resolution (50Ω input)	80 μV_{RMS}

8.2.1.2 Detailed Design Procedure

- **Input Impedance**: The JFET-input stage of the BUF802 offers giga-ohms of input impedance, and therefore, enables the front-end to terminate with a 1MΩ resistor without affecting performance. A 50Ω resistance can also be switched in offering matched termination for high-frequency signals. The BUF802 enables the designer to use both 1MΩ and 50Ω termination in the same signal chain.
- **Noise**: The total noise of the front-end amplifier is the function of the voltage and current noise of the BUF802, OPA140, and the resistors thermal noise. The dominant noise source, however, is contributed by the voltage noise of the BUF802 as a result of the noise presence across the complete bandwidth. Thus, the total RMS noise of the front-end amplifier is approximately equal to the voltage noise of BUF802 over 1GHz.

  The specified input-referred voltage noise of the BUF802 (see Section 5.5) is 2.3nV/√Hz. The total input referred RMS noise in a bandwidth of 1GHz is given by the following equation:

$$\mathrm{En_{RMS}} = 2.3\mathrm{nV}/\sqrt{\mathrm{Hz}} \times \sqrt{1\mathrm{GHz} \times 1.22} = 80\mu\mathrm{V_{RMS}} \quad (1)$$

  1.22 = Brick-wall correction factor. See TI Precision Labs – Op Amps: Noise – Spectral Density for detailed calculations.

  Figure 8-3 shows the total input-referred spot noise as a function of frequency. Assuming the oscilloscope has eight divisions on the screen and a highest resolution of 1mV, the full-scale reading is $8\mathrm{mV_{PP}}$ or $2.82\mathrm{mV_{RMS}}$. Thus, the SNR of the front-end amplifier stage at the highest-resolution setting is:

$$20 \times \log\left[\frac{2.82\mathrm{mV_{RMS}}}{80\mu\mathrm{V_{RMS}}}\right] = 31\mathrm{dB} \quad (2)$$

- **S11 Optimization**: The front-end amplifier circuit requires an exact 50Ω termination to achieve the required S11 parameter of –15dB across the frequency. Although mounting an exact 50Ω resistance at the input of the front-end composite loop circuit is possible, the parasitic capacitance of the BUF802 appears in parallel to this 50Ω resistance, resulting in a net-imperfect termination.

  The parasitic input capacitance of BUF802 (IN pin) is 2.4pF. At 1GHz, this parasitic capacitance reduces to an impedance of 66.3Ω. Thus, the net input impedance seen by the signal at the input is:

$$66.3\Omega \parallel 50\Omega = 28.5\Omega \quad (3)$$

  This result is an imperfect termination for the 50Ω source, resulting in a poor S11. The addition of a 30Ω resistance in series with the input trace, and a 6.8nH inductor in series with the on-board 50Ω termination help isolate the input parasitic capacitance. This configuration also helps maintain the net input impedance at 50Ω. Figure 8-4 shows the S11 response of this modified circuit.

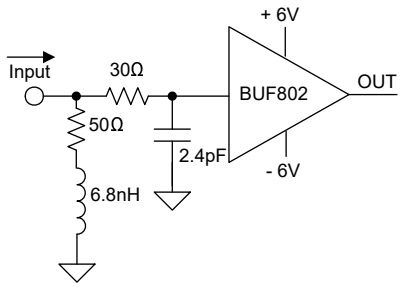


Figure 8-2. Net Input Impedance

- **Uniform Gain Across Frequency**: The front-end amplifier circuit is designed with BUF802 and OPA140 connected in a composite loop. The loop splits the input signal into low- and high-frequency components, taking both components to the output through two different circuits (transfer functions) and recombining them to reproduce a net output signal. The end goal is to achieve a smooth transition between the two circuits and maintain a flat frequency response from AC until the frequency of interest.

  CL Mode of the BUF802 simplifies this design for achieving a flat frequency response from DC until the frequency of interest (1GHz in this case). To achieve a flat response, meet the following two conditions:

  1. High-frequency response pole f_{HF} << low frequency pole f_{LF}
  2. α/β = G

  where

  – α is the input attenuation factor
  – β is the inverse of the non-inverting gain of the precision amplifier
  – G is the dc gain of the main path of the BUF802

  G varies from device-to-device; therefore, trim either α or β to achieve a flat frequency response. In Figure 8-1, trim β using the RPOT.

  G is the typical value, (G = 0.971V/V) from Section 5.5 and

$$\alpha = \frac{1}{5} \times \frac{200\text{k}\Omega}{200\text{k}\Omega + 800\text{k}\Omega} \tag{4}$$

  Therefore, trim RPOT so that β ≅ 1/5.

  For the β network, use resistors that are an order of magnitude of resistance lower than the resistors used in the α network. Therefore, β resistor values of 80 kΩ and ≅ 20kΩ are chosen.

  f_{HF} is the pole resulting from the 330pF series capacitor and the 10MΩ resistor on the In_Bias pin. Reduction in value of 10MΩ helps with the reduction of overdrive recovery time of the composite loop, but increases the f_{HF} pole frequency.

$$f_{HF} = \frac{1}{2 \times \pi \times R \times C} = \frac{1}{2 \times 3.14 \times 10\text{M}\Omega \times 330\text{pF}} = 48\text{Hz} \tag{5}$$

  f_{LF} is the pole resulting from the gain bandwidth of the precision amplifier (OPA140), the auxiliary path bandwidth and other parasitic capacitance of the resistor network.

$$f_{LF1} \text{ of precision amplifier} = \text{GBW} \times G_{AUX} \times \beta = 440\text{kHz} \tag{6}$$

  where

  – GBW is the gain bandwidth product of the precision amplifier (OPA140) = 11MHz
  – G_{AUX} is the gain from In_Aux to OUT = 0.2 V/V
  – 1/β is the external non-inverting gain set for the precision amplifier = 5 V/V

  The common mode input capacitor of the precision amplifier (C_{INPA}) forms a pole with the Rα2 resulting in pole frequency of:

$$f_{LF2} \text{ of } R\alpha 2 \text{ and } C_{INPA} \text{ of amplifier} = \frac{1}{2 \times \pi \times Ra2 \times C_{INPA}} = 28.4\text{kHz} \tag{7}$$

  Since $f_{LF2} < f_{LF1}$, f_{LF2} is considered as the dominant pole for the auxiliary path bandwidth. Based on the above value of f_{HF} and f_{LF2}, the required condition of $f_{HF} << f_{LF2}$ is met.

  CF, connected across the precision amplifier, is required to compensate for the parasitic capacitance and to make the overall poles and zeros cancel each other. Use the following equation to find the value of CF:

$$CF = C_{INPA} \times \left[\frac{G \times R_{\alpha 2}}{R_{\beta 2}} - 1 \right] \quad (8)$$

where

- C_{INPA} is the common-mode input capacitance of the precision amplifier, the OPA140 in this case
- G is the typical value, (G = 0.971V/V) from Section 5.5

Plugging in the value of these components arrives approximately to CF = 61pF, rounding off to nearest standard capacitor CF = 56pF. In the final system, based on the quality of the flat-band response needed, CF is able to be trimmed along with RPOT in the final production flow.

8.2.1.3 Application Curves

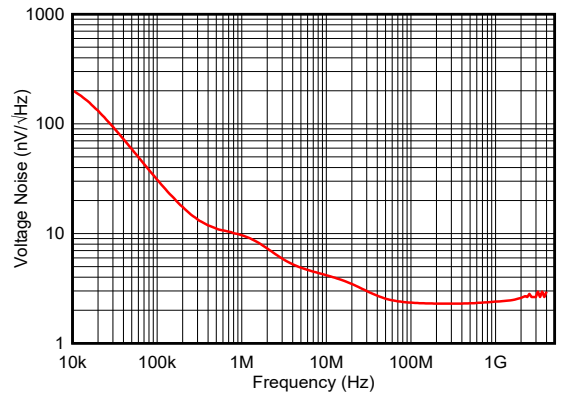


Figure 8-3. Front-End Composite Loop Noise

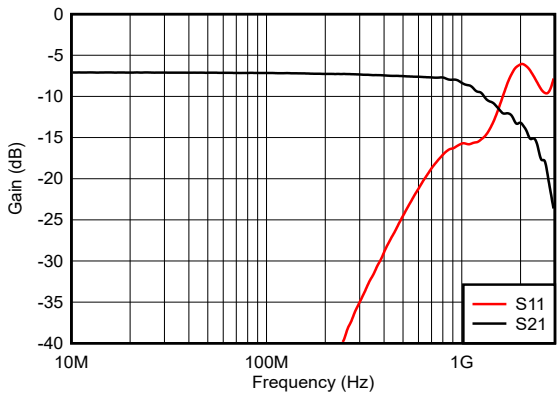


Figure 8-4. S11 and S21 Response

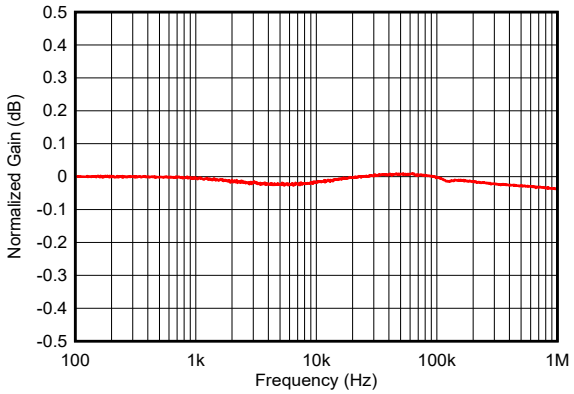


Figure 8-5. Frequency Response Flatness: Crossover Frequency Region

8.2.2 Transforming a Wide-Bandwidth, 50Ω Input Signal Chain to High-Input Impedance

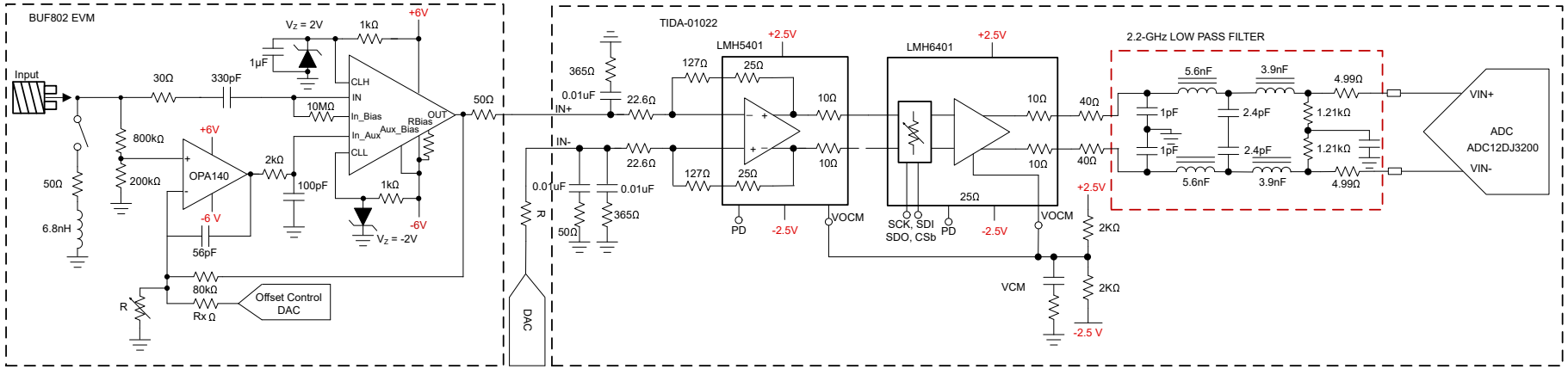


Figure 8-6. BUF802 + TIDA-01022: Signal Chain

8.2.2.1 Detailed Design Procedure

TIDA-01022 reference design primarily focuses on a multichannel high-speed analog front-end, which is typically used in end equipment, such as a digital storage oscilloscope (DSO), wireless communication test equipment (WCTE), and radars. A 50Ω input data-acquisition (DAQ) signal chain, such as the TIDA-01022, is convertible into a high-input impedance DAQ system by inserting the BUF802 at the front.

TIDA-01022 features the following:

- The LMH5401 is a high-performance, differential amplifier with a usable bandwidth from dc to 2GHz. The device is used as single-to-differential conversion amplifier in this signal chain. The device offers excellent linearity performance at a fixed 12dB gain.
- The LMH6401LMH6401 is a wideband digitally controlled variable-gain, differential in and differential out, amplifier. The noise and distortion performance are optimized to drive ultra-wideband analog-to-digital converters (ADCs). The device offers dc to 4.5GHz bandwidth with a gain range from –6dB to 26dB in 1dB steps. The gain is controlled using a standard serial peripheral interface (SPI).
- The ADC12DJ5200RF is a 12-bit, gigasample ADC that directly samples input frequencies from dc to greater than 10GHz. The ADC12DJ5200RF is configurable as a dual-channel, 5.2GSPS ADC or single-channel, 10.4GSPS ADC.

The BUF802 along with offering high-input impedance and low-noise for the front-end amplifier, holds capability of driving matched loads of 50Ω, making this device easy to retrofit with predesigned analog front-end signal chains. Figure 8-7 to Figure 8-9 shows the comparison of native performance of the TI design TIDA-01022 and performance achieved post addition of the BUF802 at the front-end. Adding the BUF802 at the input of TIDA-01022 translates the original 50-Ω input impedance TI design to a high-input impedance DAQ signal chain. Figure 8-6 shows a simplified schematic of the BUF802 + TIDA-01022.

8.2.2.2 Application Curves

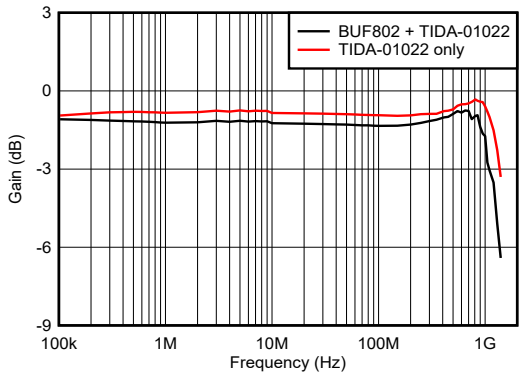


Figure 8-7. Gain vs Frequency

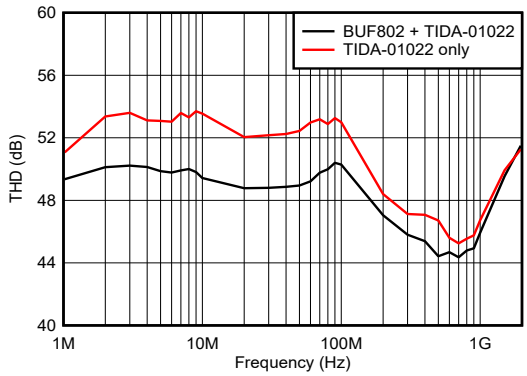


Figure 8-8. Total Harmonic Distortion (THD) vs Frequency

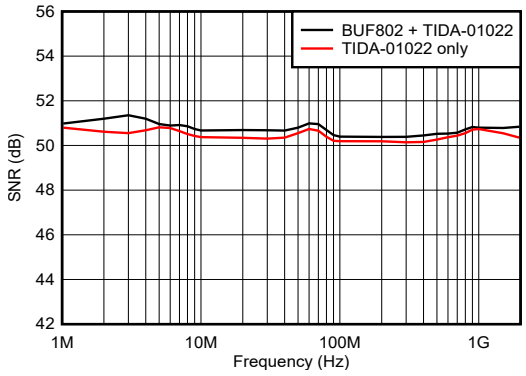


Figure 8-9. Signal-to-Noise Ratio (SNR) vs Frequency

8.3 Power Supply Recommendations

The BUF802 is intended to operate with supplies ranging from ±4.5V to ±6.5V. The BUF802 operates on either single-sided supplies or split supplies. When using split supplies, the supplies are symmetrically balanced around GND or asymmetric. For best ac performance, center the input and output signal around the mid-supply.

Minimize the distance between the power-supply pins and decoupling capacitors. Place the high-frequency capacitors (< 0.1µF) close to the supply-pins, and on the same side of the PCB as the BUF802. Place larger capacitors (> 1µF) further away from the device. Section 8.4 has additional details on decoupling capacitor layout and routing.

The BUF802 has two sets of supply pins:

- V_{S+} and $V_{S–}$
- V_{SO+} and V_{SO}

The separation of the input- and output-stage supply pins minimizes spurious crosstalk and maximizes transient decoupling between the two stages. Section 7.2 shows how both sets of supply pins are internally connected through back-to-back diodes. Therefore, connect the supply pins for the input and output stages to the same potential. Maintain separate and individual decoupling capacitors for all the supply pins; see also Section 8.4.

8.4 Layout

8.4.1 Layout Guidelines

Achieving optimized performance with the BUF802 requires careful attention to board layout, parasitic, and passive component selection. Consider the following:

- **Peaking in the S21 transfer function**: keeping the trace length minimum is of prime importance to prevent peaking in the S21 transfer function of the BUF802. The trace inductance can form a resonant circuit with the input capacitance of the BUF802, causing peaking in the S21 response. Add a small resistor (R5 in Figure 8-10) in series with the dc blocking capacitor to dampen the LC resonance created by the trace inductance and the input capacitance of the BUF802. Select series capacitors (C7 in Figure 8-10) with low equivalent series inductance (ESL) to minimize total inductance.
- **Power-supply bypass capacitors**: mount the power-supply bypass capacitors as close to the supply pins as possible and on the same side of the PCB as the BUF802. As shown in Figure 8-10, select low-inductance LICC capacitors (C5, C6, C13, and C10) to minimize high-frequency impedance between the BUF802 and the bypass capacitors. Use multiple vias between the bypass capacitor and GND to reduce series inductance. As shown in Figure 8-10, also use multiple vias to GND on the 50-Ω input termination resistor (R3). Connect the bypass and termination vias to a solid GND plane.
- **High precision signal path**: consisting of the precision op amp along with discrete components, the signal path can be adjusted and moved around to give precedence to the two previous points. In the Figure 8-12, the precision components are placed on the opposite side of the PCB as the BUF802.
- **Thermal pad**: thermally conductive but electrically insulated to the die. This configuration gives the circuit designer flexibility in connecting the thermal pad to any voltage. Select a power or ground plane with the highest thermal mass for effective heat dissipation.

8.4.2 Layout Example

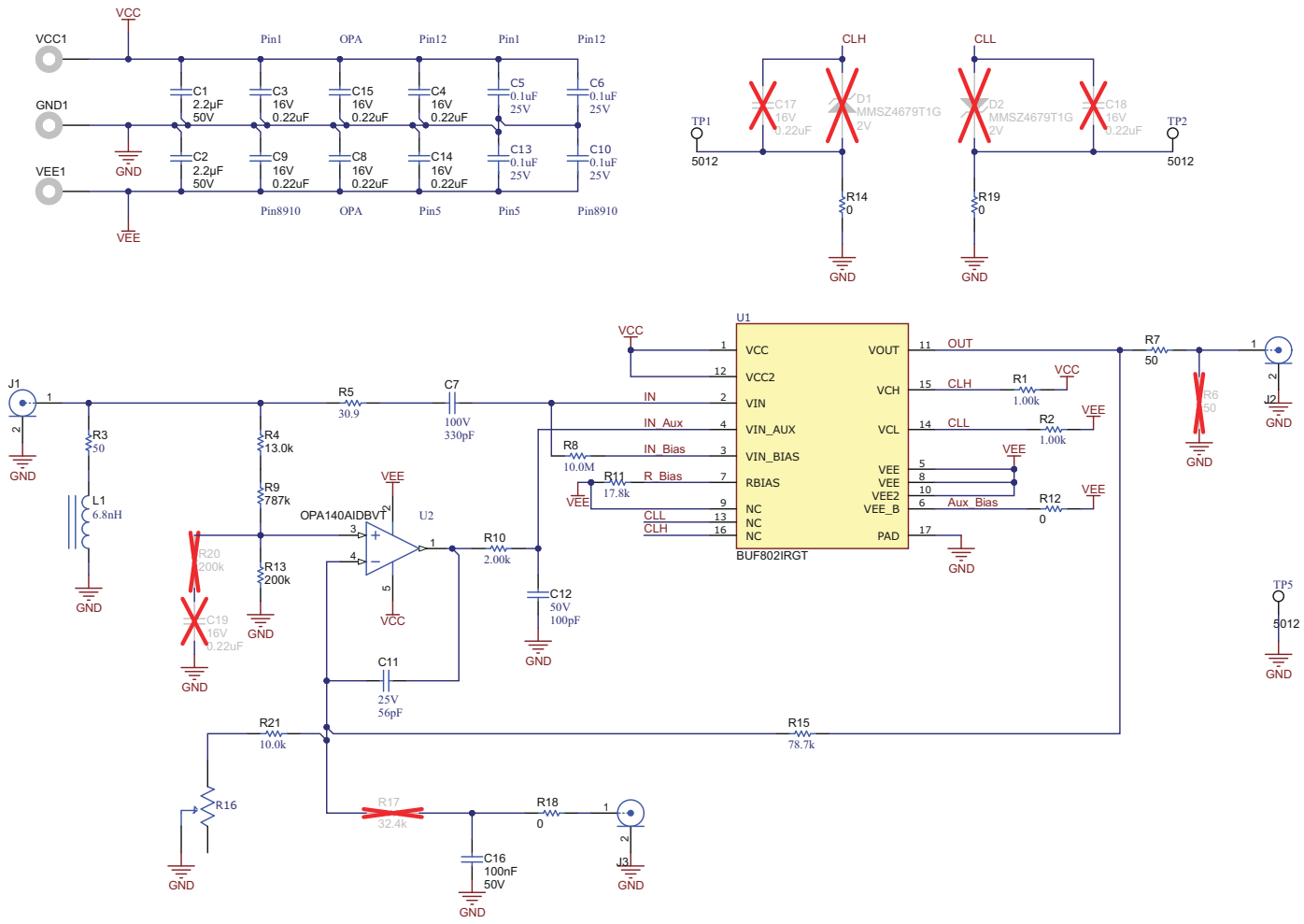


Figure 8-10. Layout Example: Schematic for Layout Reference

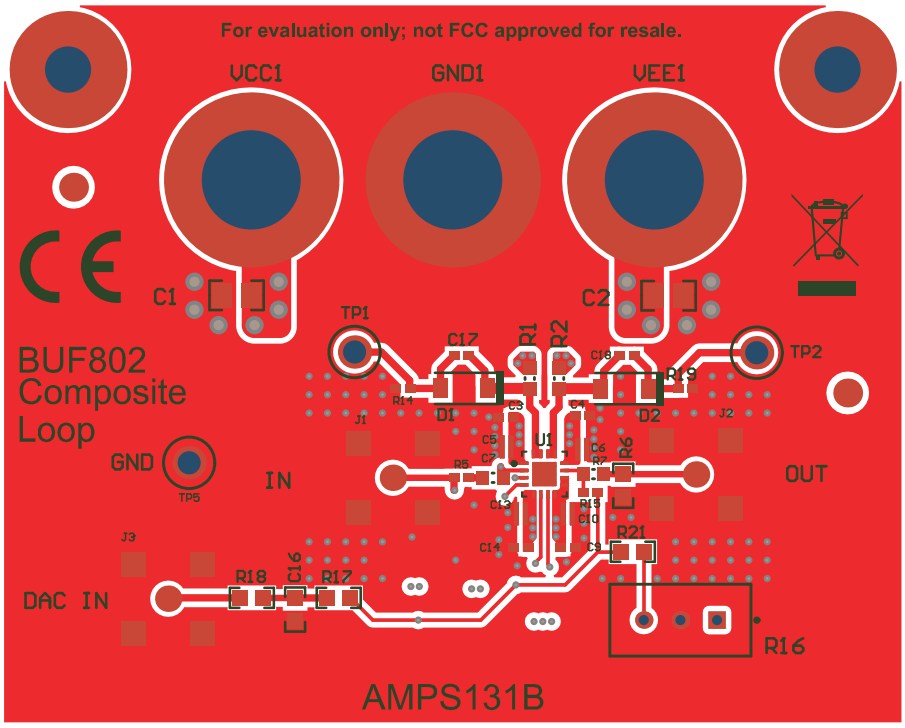


Figure 8-11. Layout Example: Top Layer

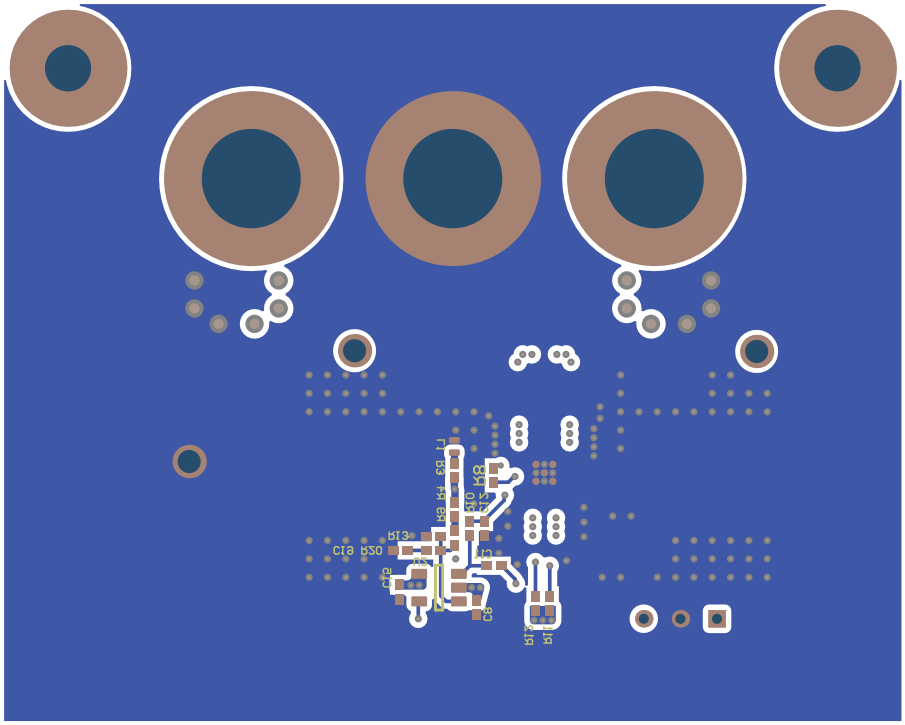


Figure 8-12. Layout Example: Bottom Layer

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Flexible 3.2GSPS multi-channel AFE reference design for DSOs, radar and 5G wireless test systems* reference design

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2025) to Revision E (March 2026)	Page
• Added Low phase noise to *Features*	1
• Added Clock drivers and clock buffers to *Applications*	1
• Updated T_A = 25°C output swing minimum value from: V_{S+} − 1.9V to: V_{S-} + 3.4V	5
• Updated −40°C to +85°C output swing minimum value from: V_{S+} − 2.0V to: V_{S-} + 3.4V	5
• Updated T_A = 25°C output swing maximum value from: V_{S-} + 3.4V to: V_{S+} − 1.9V	5
• Updated −40°C to +85°C output swing maximum value from: V_{S-} + 3.4V to: V_{S+} − 2.0V	5
• Updated V_{OS} input offset voltage typical value from: −600mV to: 600mV	5
• Updated V_{OS} input offset voltage V_{OUT} = V_{IN} maximum value from: −800mV to: 800mV	5
• Updated V_{OS} input offset voltage T_A = −40°C to +85°C maximum value from: −900mV to: 900mV	5
• Added Phase noise plot in *Typical Characteristics*	8
• Added *BUF802 Used in BF Mode for Clock Buffer* section	20
• Added *Alternative Approach for Realizing Composite Loop* section	22

Changes from Revision C (March 2022) to Revision D (July 2025) **Page**

- Deleted maximum dVS/dT for supply turn-on and turn-off from *Absolute Maximum Ratings* 4
- Changed current noise unit from pA/√Hz to fA/√Hz in both *Electrical Characteristics* 5
- Moved V_{CLH} and V_{CLL} to symbol column and expanded text for clarity..... 5
- Deleted across temperature data from G_{AUX} 5
- Changed "to" to "/" in G_{AUX} parameter name for clarity..... 5
- Added new row to G_{AUX} for low frequency region..... 5
- Added crossover text to G_{AUX} 5
- Added test condition to In_Aux input voltage for clarity..... 5
- Added G_{AUX} BW symbol to V_{OUT} / In_Aux bandwidth 5
- Updated G_{AUX} BW to a ratio for clarity..... 5
- Moved Operating voltage to *Recommended Operating Conditions* 5
- Updated voltage noise and current noise density vs frequency plots in *Typical Characteristics* 8
- Changed unit for current noise density vs frequency plot in *Typical Characteristics* 8
- Updated *Detailed Design Procedure* to reflect pole frequencies more accurately, to use G value from *Electrical Characteristics: Wide Bandwidth Mode*, and to clarify CF value..... 24

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BUF802IRGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BUF802
BUF802IRGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BUF802

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

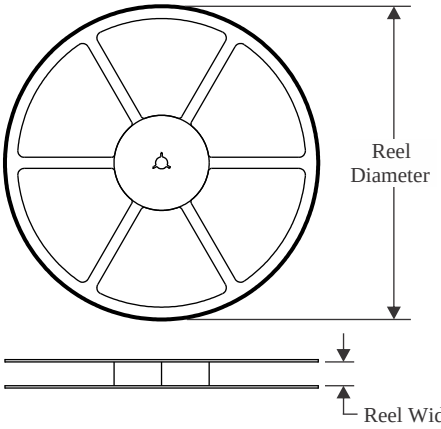
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

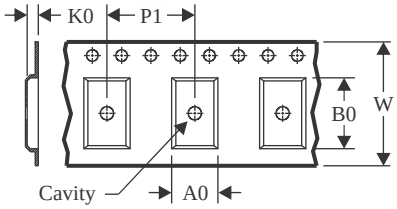
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

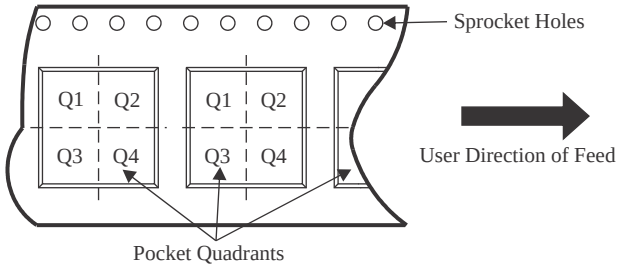


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

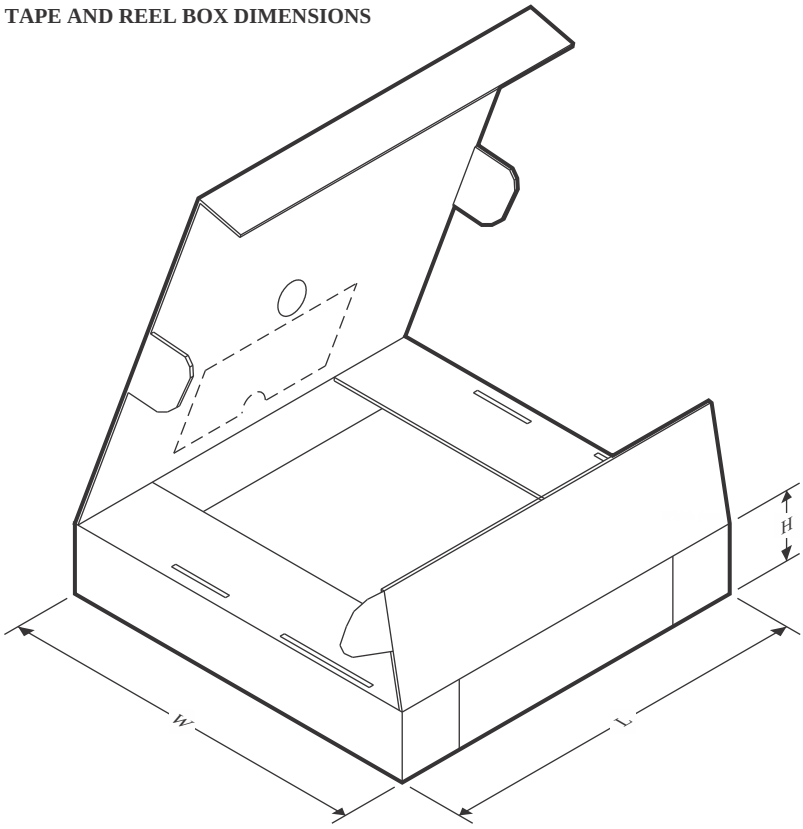
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF802IRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

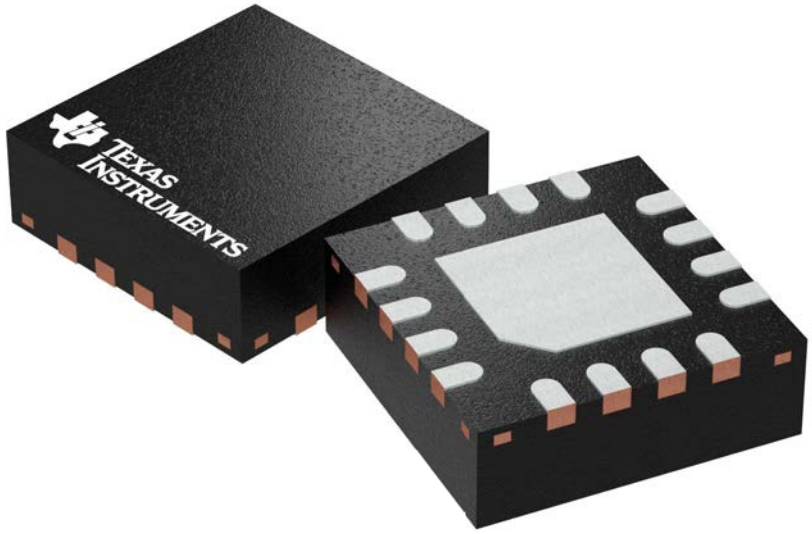


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF802IRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



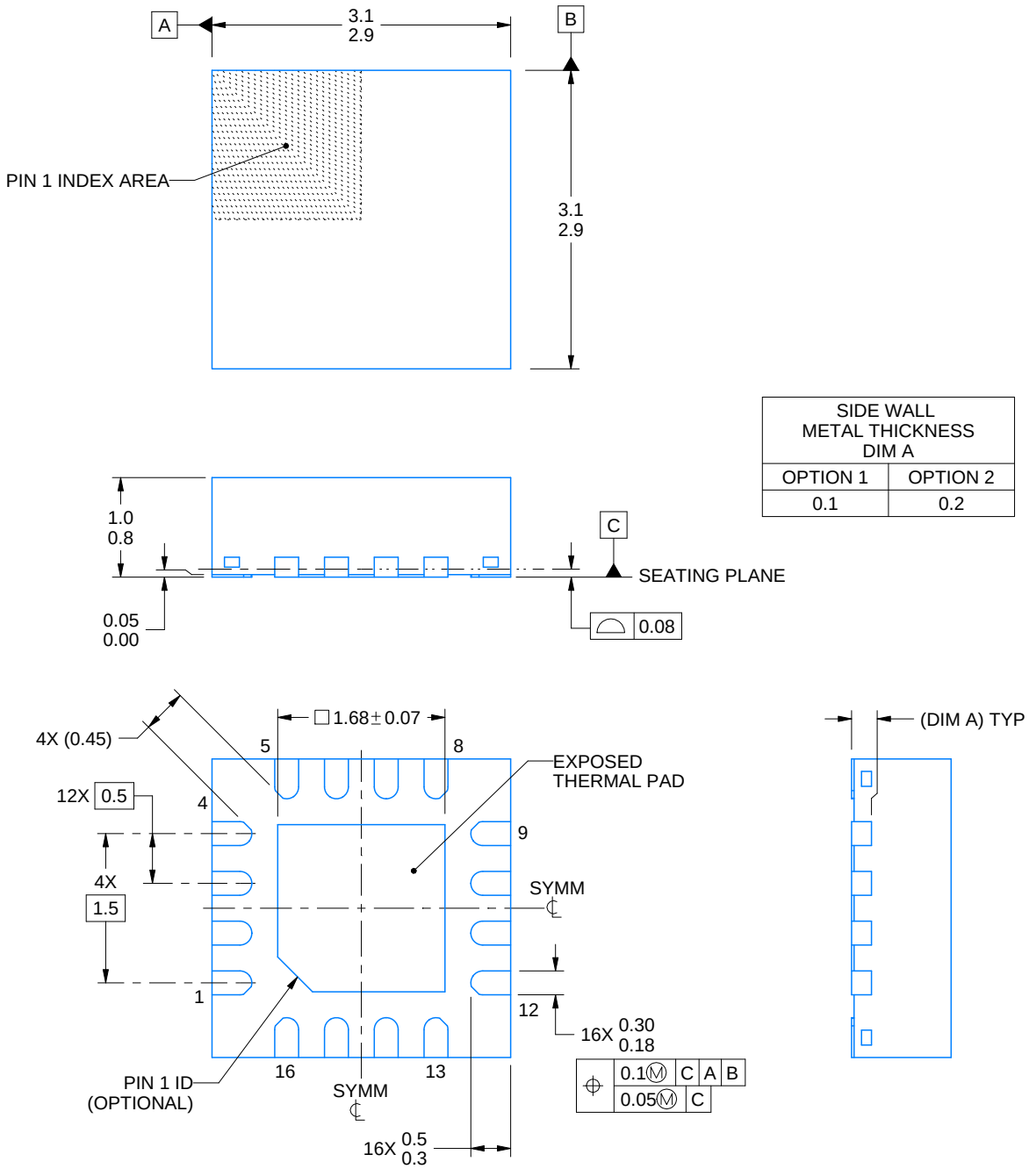
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

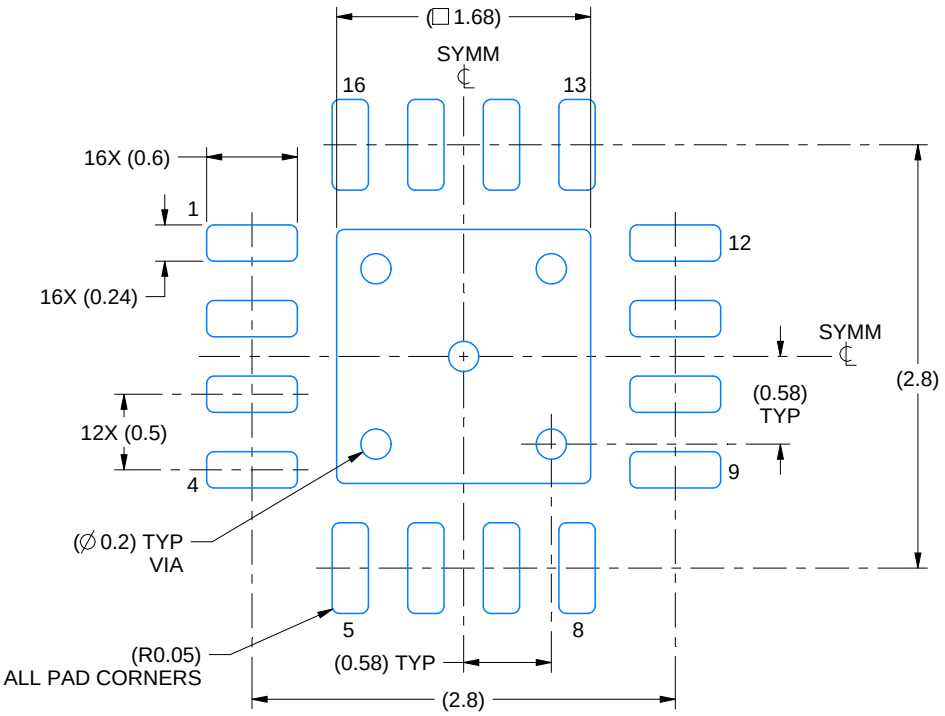
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

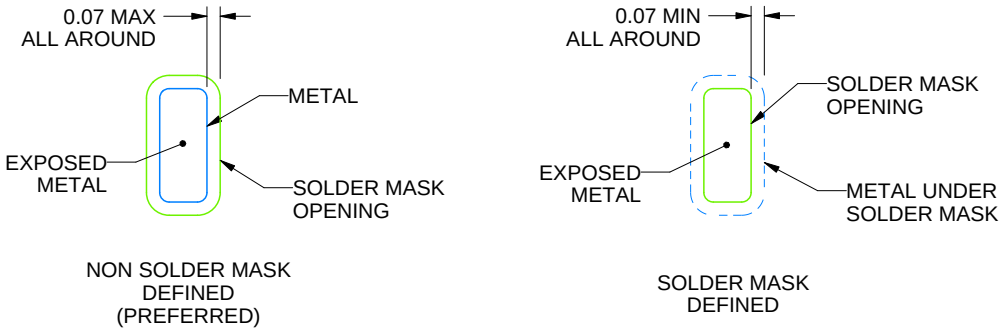


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

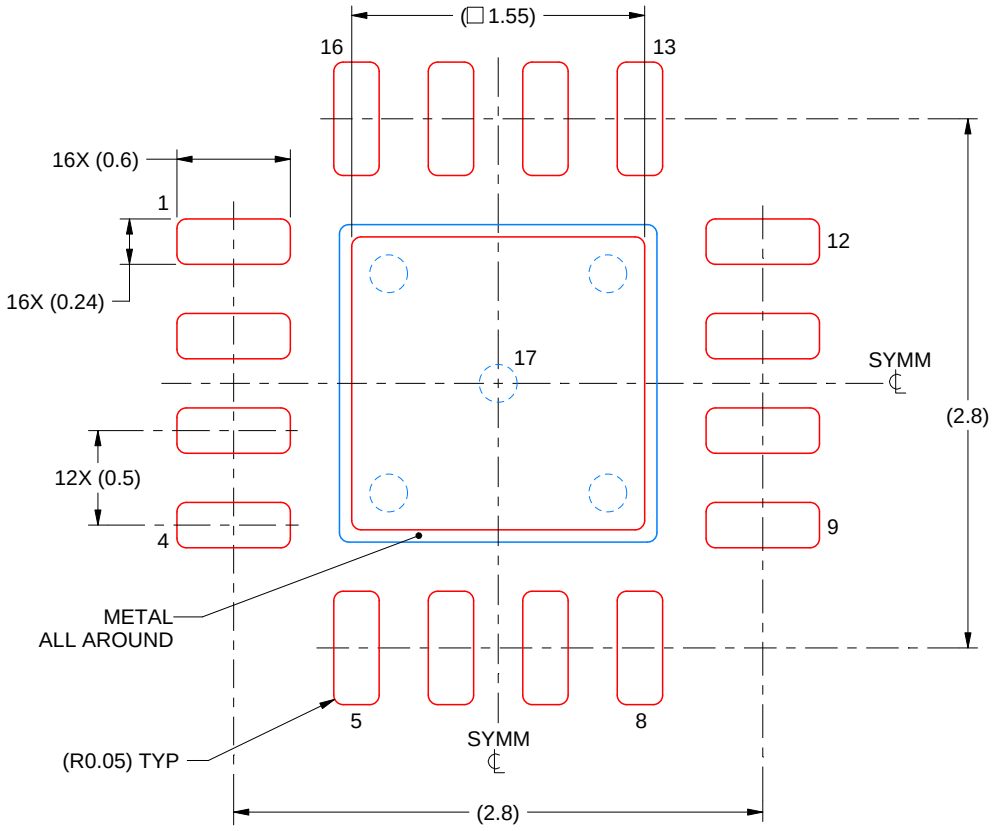


SOLDER MASK DETAILS

4222419/E 07/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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