



22-V Supply, 10+1 Channel Gamma Correction Buffer

FEATURES

- Wide Supply Range: 7 V to 22 V
- Gamma Correction Channels: 10
- Integrated V_{COM} Buffer
- Excellent Output Current Drive:
 - Gamma Channels:
> 30 mA at 0.5 V Swing to Rails⁽¹⁾
 - V_{COM} :
> 100 mA typ at 2 V Swing to Rails⁽¹⁾
- Large Capacitive Load Drive Capability
- Rail-to-Rail Output
- PowerPAD™ Package
- Low-Power/Channel: < 500 μ A
- High ESD Rating: 8 kV HBM, 2 kV CDM, 300 V MM
- Specified for -25°C to $+85^{\circ}\text{C}$

(1) See Typical Characteristic curves for details.

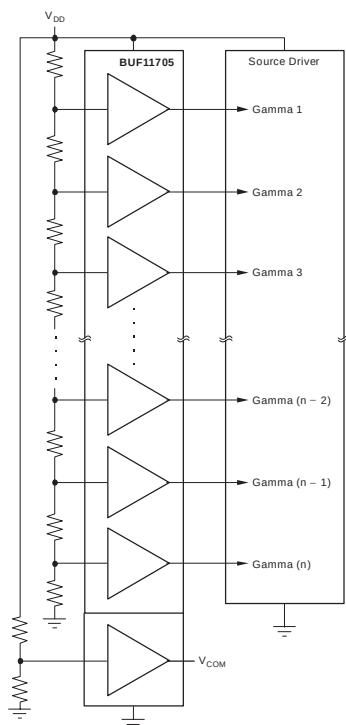
DESCRIPTION

The BUF11705 is a multi-channel buffer targeted towards gamma correction in high-resolution LCD panels. It is pin-compatible with the existing BUF11702 and BUF11704 and operates at higher supply voltages up to 22 V (24 V absolute max). The higher supply voltage enables faster response times and brighter images in large-screen LCD panels. This is especially important in LCD TV applications.

The BUF11705 offers 10 gamma channels. For additional space and cost savings, a V_{COM} channel with > 100 mA drive capability is integrated into the BUF11705.

The BUF11705 is available in the TSSOP-28 PowerPAD package for dramatically increased power dissipation capability. This allows a large number of channels to be handled safely in one package.

A flow-through pinout has been adopted to allow simple PCB routing and maintain cost-effectiveness. All inputs and outputs of the BUF11705 incorporate internal ESD protection circuits that prevent functional failures at voltages up to 8 kV (HBM), 2 kV (CDM), and 300 V (MM).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range unless otherwise noted.

PARAMETERS	BUF11705	UNIT
Supply voltage, V_{DD} ⁽²⁾	24	V
Input voltage range, V_I	$\pm V_{DD}$	
Continuous total power dissipation	See dissipation rating table	
Operating free-air temperature range, T_A	-25 to +85	°C
Maximum junction temperature, T_J	+125	°C
Storage temperature range, T_{STG}	-65 to +150	°C
Lead temperature 1.6mm (1/16 inch) from case for 10s	+260	°C
ESD rating:		
Human body model (HBM)	8	kV
Charged-device model (CDM)	2	kV
Machine model (MM)	300	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND.

ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE MARKING
BUF11705	TSSOP-28	BUF11705

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet or see the TI website at www.ti.com.

DISSIPATION RATING TABLE

PACKAGE TYPE	PACKAGE DESIGNATOR	θ_{JC} ⁽¹⁾ (°C/W)	θ_{JA} ⁽¹⁾ (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING
TSSOP-28	PWP (28)	0.72	27.9	3.58 W

(1) PowerPAD attached to PCB, 0 lfm airflow, and 76mm x 76mm copper area.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	7		22	V
Operating free-air temperature, T_A	-25		+85	°C

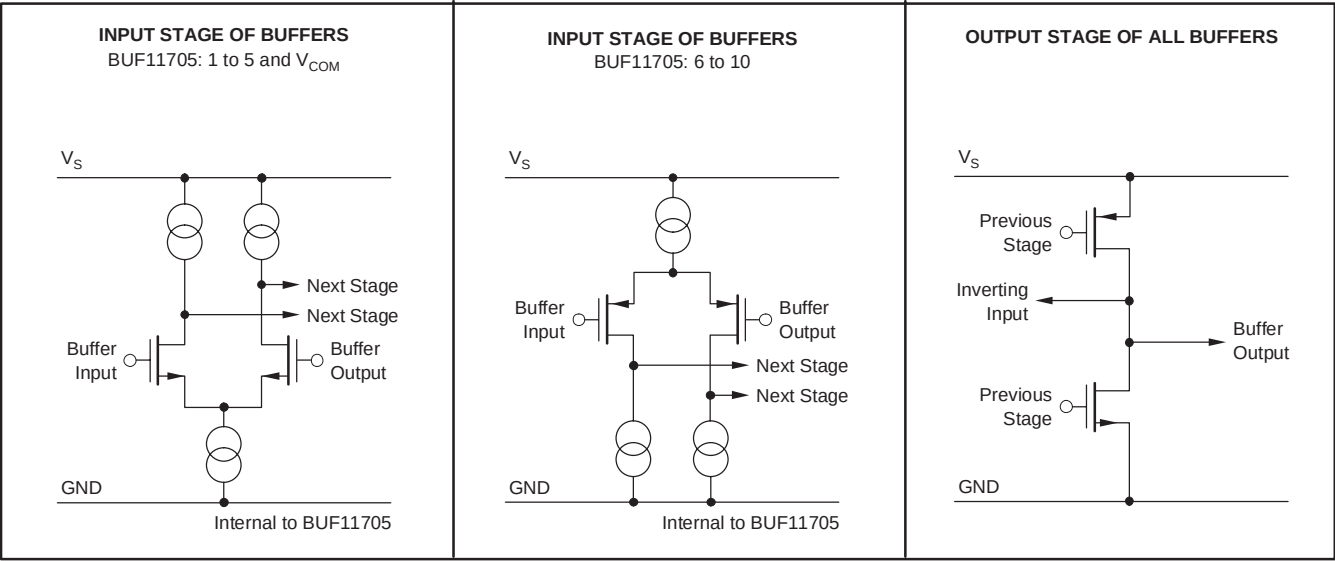
ELECTRICAL CHARACTERISTICS: BUF11705

Over operating free-air temperature range, $V_{DD} = 18\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

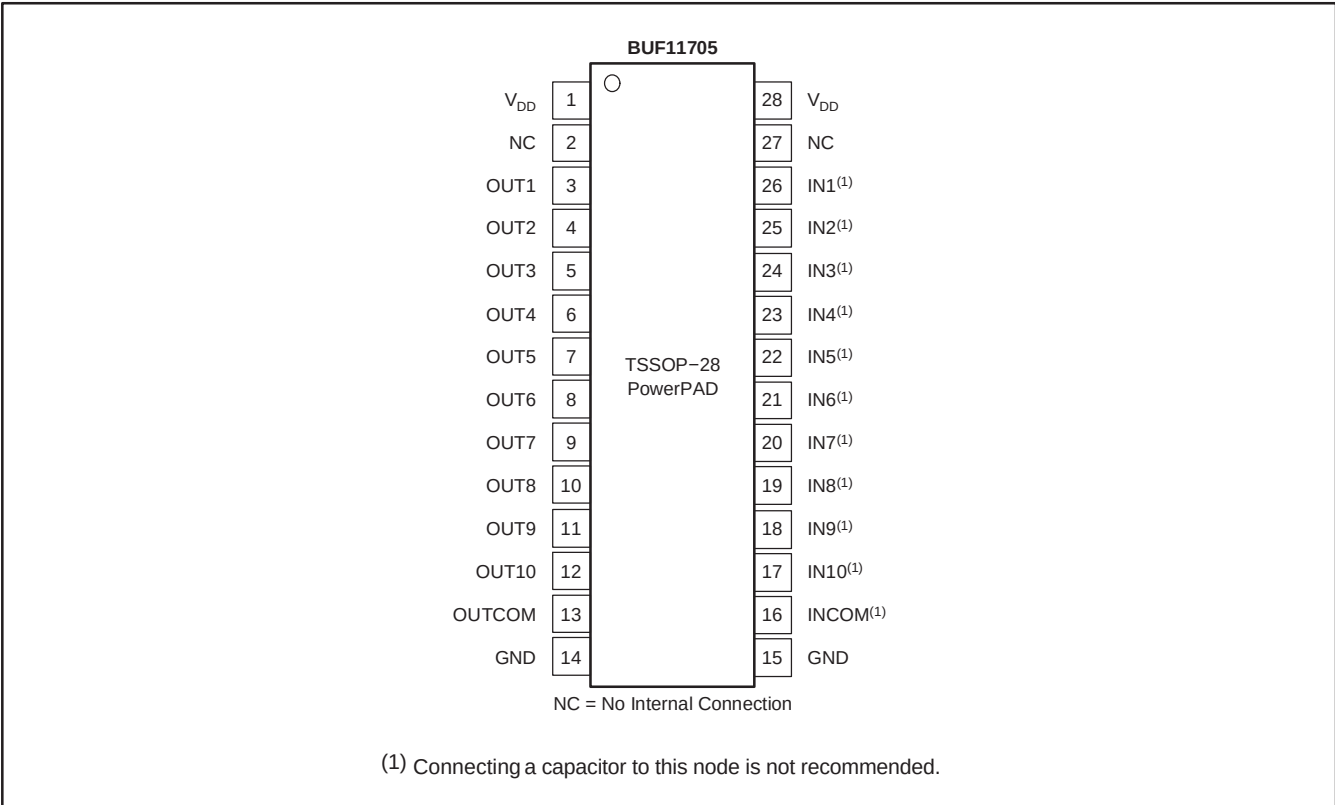
PARAMETER			TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	Gamma buffers	V _I = 9V	+25°C		−1	20	mV
				Full range(1)		20		
		V _{COM}		+25°C		−1	30	
				Full range(1)		30		
I _{IB} Input bias current			V _I = V _{DD} /2	+25°C		1		pA
				Full range(1)		200		
PSRR Power-Supply Rejection Ratio			V _{DD} = 4.5 V to 22 V	+25°C	62	80		dB
				Full range(1)	60			
Buffer gain			V _I = 5 V	+25°C		0.9995		V/V
BW_3dB	3dB bandwidth	Gamma buffers V _{COM} buffer	C _L = 100 pF, R _L = 2 kΩ	+25°C		1 0.6		MHz
SR	Slew rate	Gamma buffers V _{COM} buffer	C _L = 100 pF, R _L = 2 kΩ V _{IN} = 2 V to 16 V	+25°C		1.6 4.6		V/μs
	Crosstalk		V _I PP = 6 V, f = 1 kHz	+25°C		85		dB
I _{DD} Supply current		ALL	V _O = V _{DD} /2 No Load	25°C		5	9.0	mA
				Full range			9.0	
Common-mode input range		Buffers 1-5		+25°C	1	V _{DD}		V
		Buffers 6-10			GND	V _{DD} − 1		
		V _{COM} buffer			1	V _{DD}		
Load regulation		V _{COM} buffer sinking	I _O = 1 mA to 100 mA, V _{IN} = 2 V	+25°C	1	5	mV/mA	
				Full range		5		
		V _{COM} buffer sourcing	I _O = −1 mA to −100 mA V _{IN} = 16 V	+25°C	1	5		
				Full range		5		
		Buffers 1-10 sinking	I _O = 1 mA to 10 mA V _{IN} = 1 V	+25°C	1	5		
				Full range		5		
Buffers 1-10 sourcing	I _O = −1 mA to −10 mA V _{IN} = 17 V	+25°C	1	5				
		Full range		5				
VOH1-5	High-level output voltage	Buffers 1-5	V _{IN} = 18 V I _{SOURCE} = 10 mA	+25°C	17.85	17.9	V	
Buffers 6-10		V _{IN} = 17 V I _{SINK} = 10 mA V _{IN} = 17 V I _{SOURCE} = 10 mA	+25°C	17	17.15	V		
				16.85	17			
VOL1-5	Low-level output voltage	Buffers 1-5	V _{IN} = 1 V I _{SINK} = 10 mA	+25°C	1.0	1.15	V	
V _{IN} = 1 V I _{SOURCE} = 10 mA			0.85		1.0			
VOL6-10		Buffers 6-10	V _{IN} = 0 V I _{SINK} = 10 mA	+25°C	0	0.15	V	
VOHCOM	High-level output voltage	V _{COM} buffer	V _{IN} = 16 V I _{SINK} = 100 mA	+25°C	16	16.15	V	
			V _{IN} = 16 V I _{SOURCE} = 100 mA		15.85	16		
VOLCOM	Low-level output voltage	V _{COM} buffer	V _{IN} = 2 V I _{SINK} = 100 mA	+25°C	2	2.15	V	
			V _{IN} = 2 V I _{SOURCE} = 100 mA		1.85	2		

(1) Full range is -25°C to $+85^\circ\text{C}$.

EQUIVALENT SCHEMATICS OF INPUTS AND OUTPUTS



PIN CONFIGURATION



TYPICAL CHARACTERISTICS

Over operating free-air temperature range, unless otherwise noted.

DC CURVES

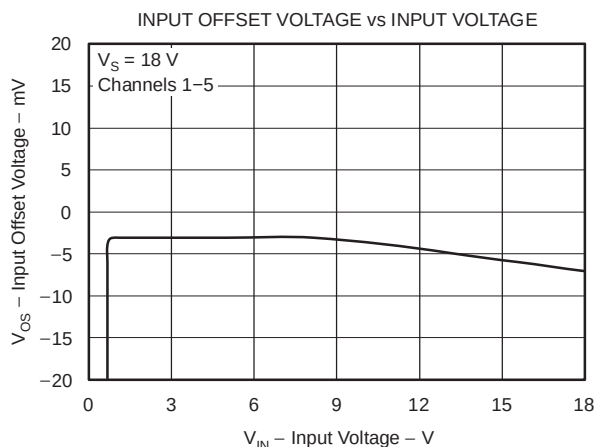


Figure 1

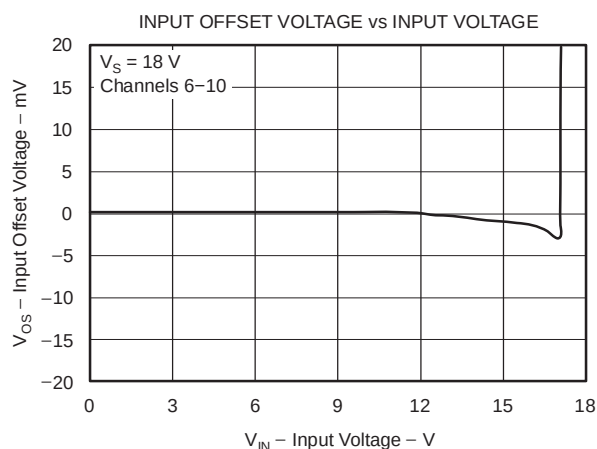


Figure 2

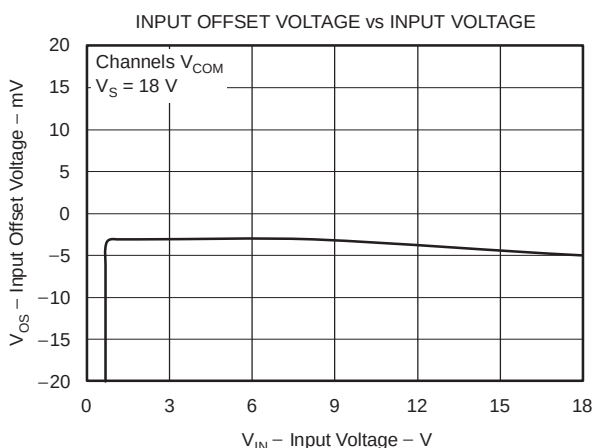


Figure 3

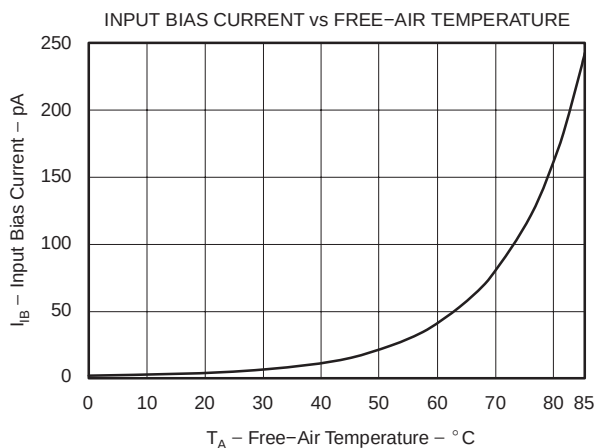


Figure 4

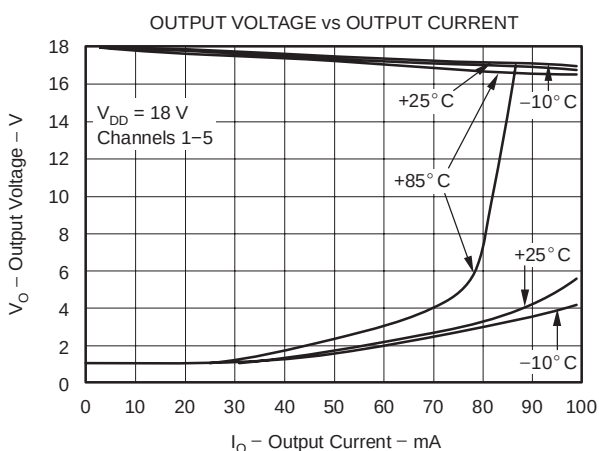


Figure 5

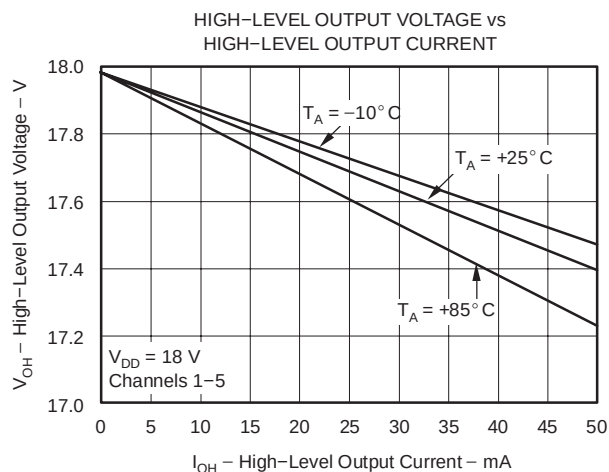


Figure 6

TYPICAL CHARACTERISTICS (continued)

Over operating free-air temperature range, unless otherwise noted.

DC CURVES (continued)

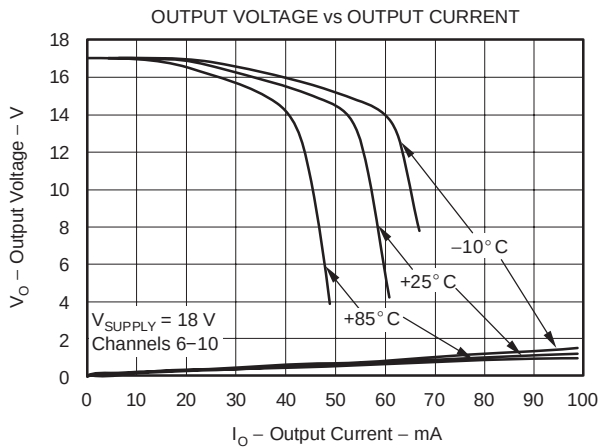


Figure 7

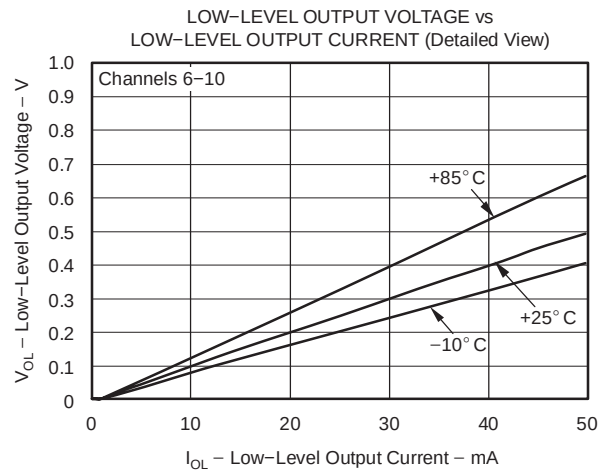


Figure 8

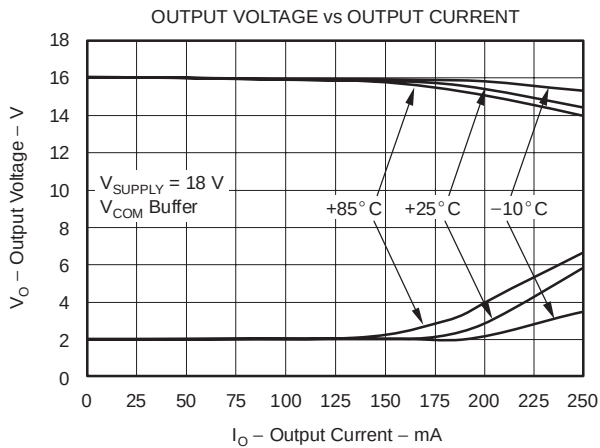


Figure 9

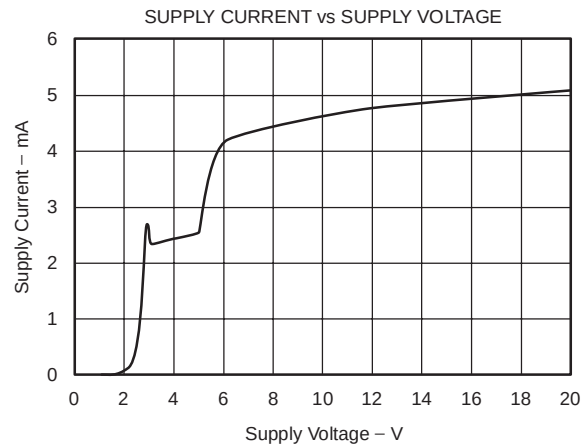


Figure 10

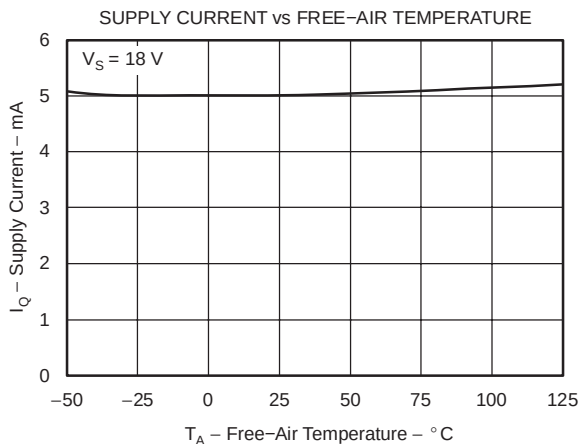


Figure 11

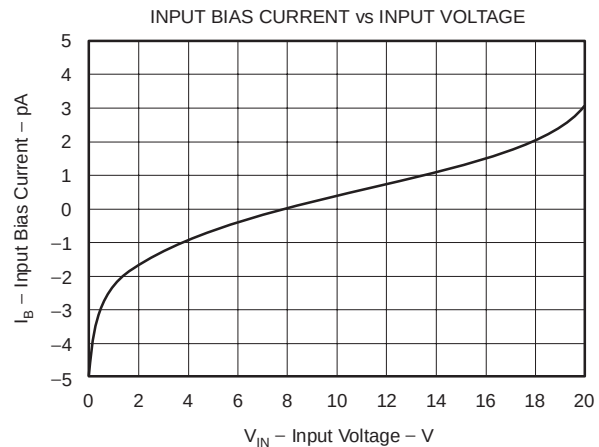


Figure 12

TYPICAL CHARACTERISTICS (continued)

Over operating free-air temperature range, unless otherwise noted.

AC CURVES

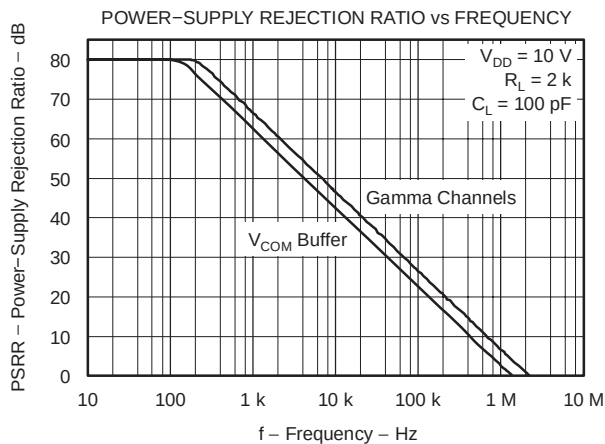


Figure 13

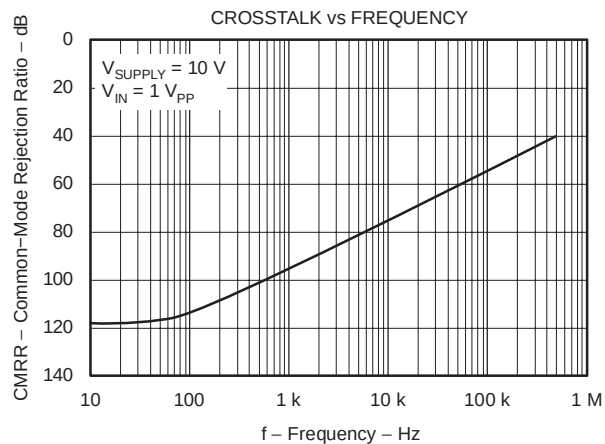


Figure 14

TYPICAL CHARACTERISTICS (continued)

Over operating free-air temperature range, unless otherwise noted.

SMALL- AND LARGE-SIGNAL WAVEFORM CURVES

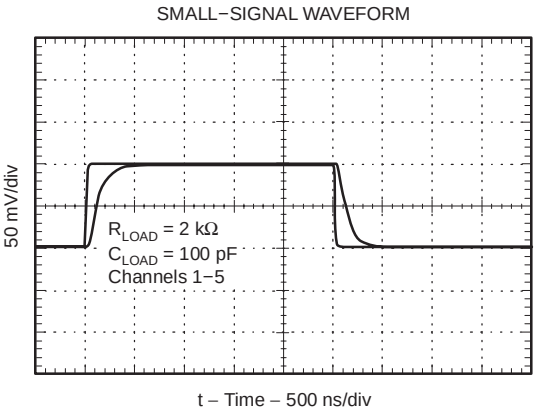


Figure 15

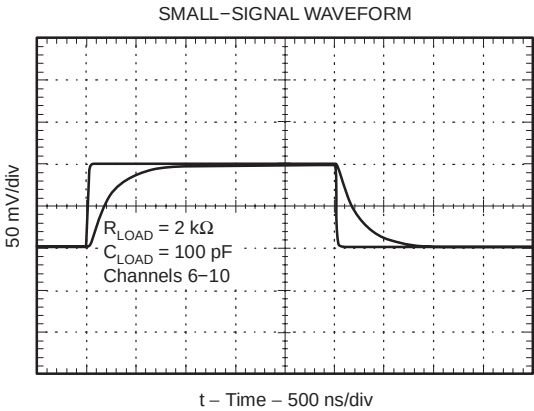


Figure 16

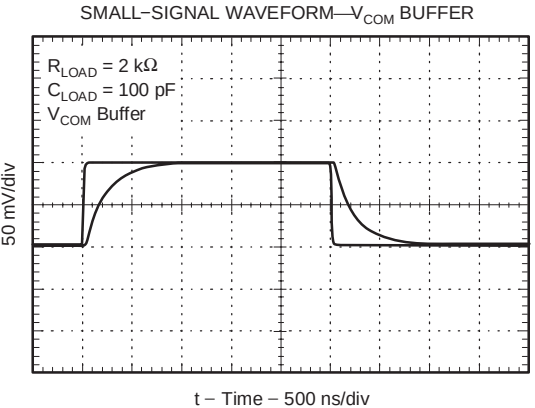


Figure 17

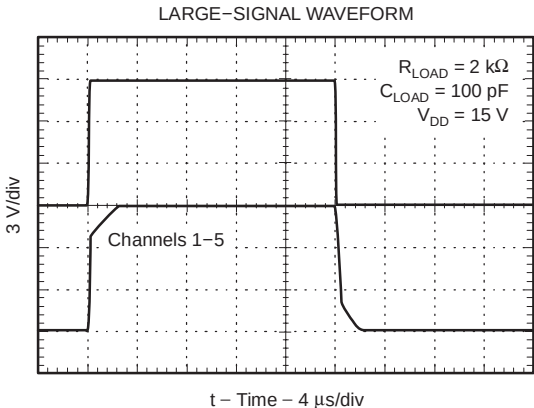


Figure 18

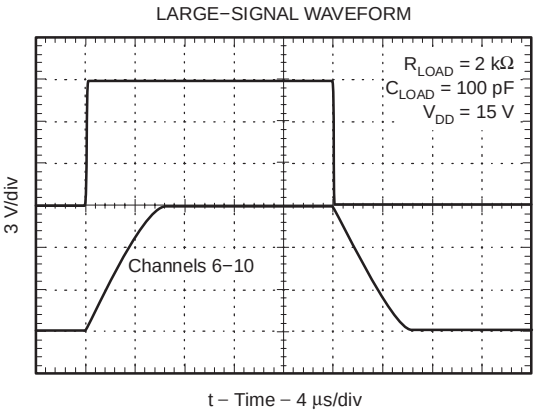


Figure 19

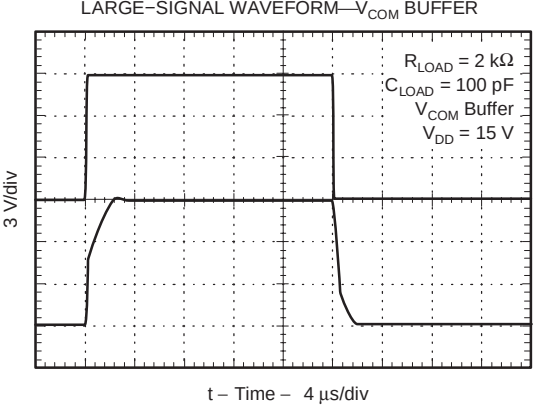


Figure 20

APPLICATION INFORMATION

The requirements on the number of gamma correction channels vary greatly from panel to panel. Therefore, the BUF11705 series of gamma correction buffers offer different channel combinations using 10 gamma channels plus one V_{COM} channel. The V_{COM} channel can be used to drive the V_{COM} node on the LCD panel.

Gamma correction voltages are often generated using a simple resistor ladder, as shown in Figure 21. The BUF11705 buffers the various nodes on the gamma

correction resistor ladder. The low output impedance of the BUF11705 forces the external gamma correction voltage on the respective reference node of the LCD source driver. Figure 21 shows an example of the BUF11705 in a typical block diagram driving an LCD source driver with 10-channel gamma correction reference inputs.

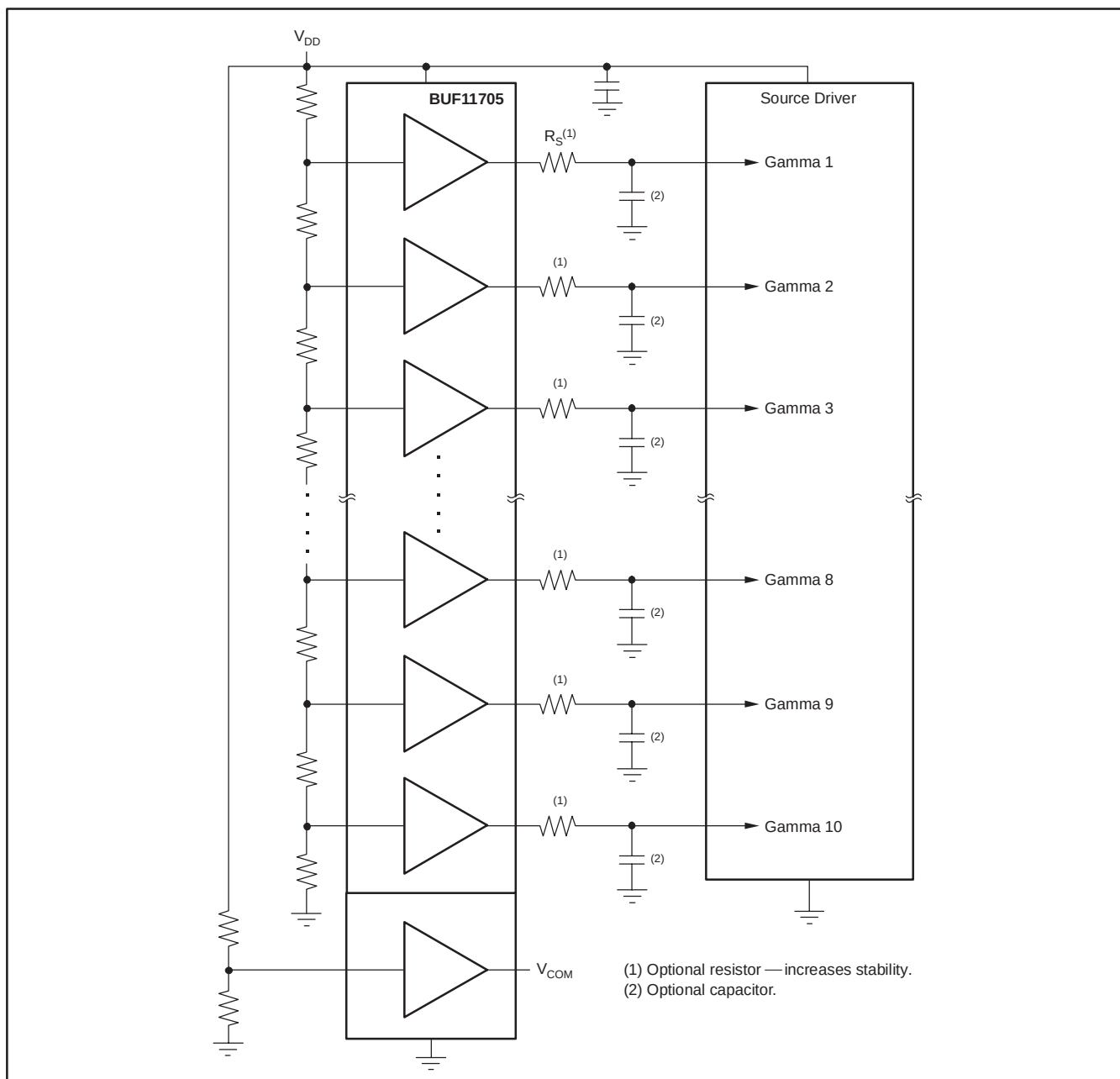


Figure 21. LCD Source Driver Typical Block Diagram

ESD RATINGS

The BUF11705 has excellent ESD performance: 8 kV HBM; 2 kV CDM; and 300 V MM. These ESD ratings allow for increased manufacturability, fewer production failures, and higher reliability.

INPUT VOLTAGE RANGE GAMMA BUFFERS

Figure 22 shows a typical gamma correction curve with 10 gamma correction reference points (GMA1 through GMA10). As can be seen from this curve, the voltage requirements for each buffer vary greatly. The swing capability of the input stages of the various buffers is carefully matched to the application. Buffers 1 through 5 have input stages that include V_{DD} , but will only swing within 1 V to GND. Buffers 1 through 5 have only a single NMOS input stage. Buffers 6 through 10 have only a single PMOS input stage. The input range of the PMOS input stage includes GND.

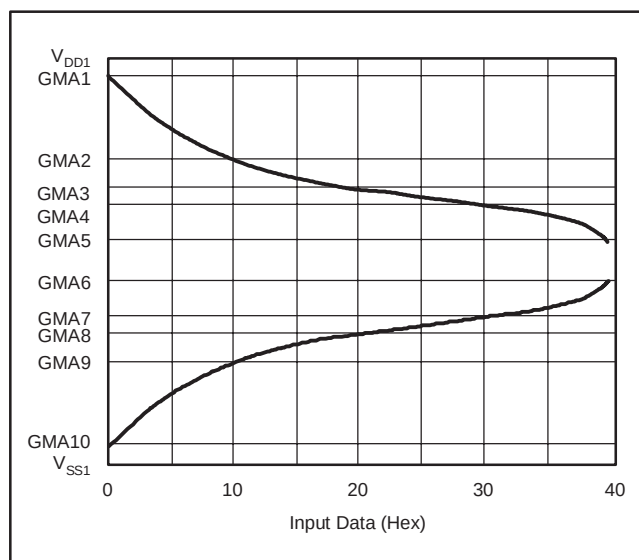


Figure 22. Gamma Correction Curve

OUTPUT VOLTAGE SWING GAMMA BUFFERS

The output stages have been designed to match the characteristic of the input stage. This means that the output stage of buffers 1 through 5 swing very close to

V_{DD} (typically, $V_{CC} - 100$ mV at 10 mA). The ability of buffers 1 through 5 to swing to GND is limited. Buffers 6 through 10 swing closer to GND than V_{DD} . Buffers 6 through 10 are designed to swing very close to GND; typically, GND + 100 mV at a 10 mA load current. See the *Typical Characteristics* for more details. This approach significantly reduces the silicon area and overall cost of the whole solution. However, due to this architecture, the correct buffer must be connected to the correct gamma correction voltage. Connect buffer 1 to the gamma voltage closest to V_{DD} , and buffers 2 through 5 to the sequentially voltages. Buffer 10 should be connected to the gamma correction voltage closest to GND (or the negative rail), and buffers 9 through 6 to the sequentially higher voltages.

COMMON BUFFER (V_{COM})

The common buffer output of the BUF11705 has a greater output drive capability than the gamma buffers in order to meet the heavier current demands of driving the common node of the LCD panel. The common buffer output was also designed to drive heavier capacitive loads. Excellent output swing is possible with high currents (> 100 mA), as shown in Figure 23.

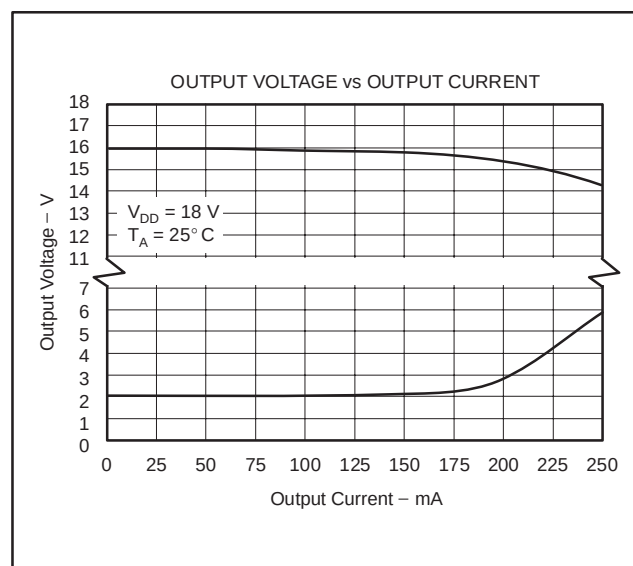


Figure 23. V_{COM} Output Drive Capability

CAPACITIVE LOAD DRIVE

The BUF11705 has been designed to sink/source large dc currents. Its output stage has been designed to deliver output current transients with little disturbance of the output voltage. However, there are times when very fast current pulses are required. Therefore, in LCD source driver buffer applications, it is quite normal for capacitors to be placed at the outputs of the reference buffers. These capacitors improve the transient load regulation and will typically have values of 100pF or more. The BUF11705 gamma buffers were designed to drive capacitances in excess of 100 pF. The output is able to swing within 150 mV of the rails on 10 mA of output current, as shown in Figure 24.

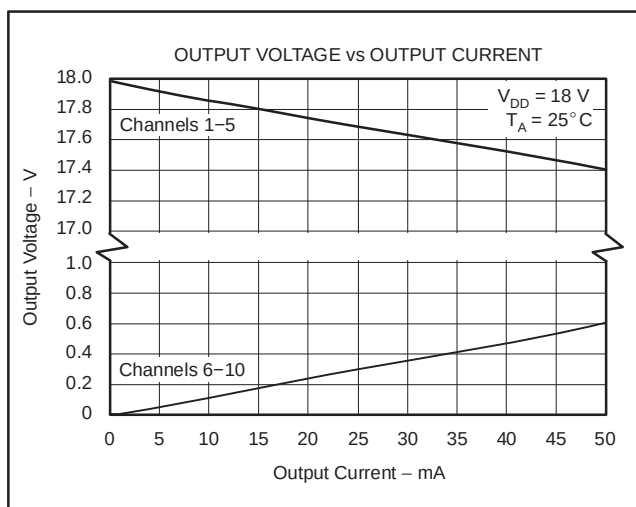


Figure 24. Gamma Buffer Drive Capability

APPLICATIONS WITH >10 GAMMA CHANNELS

When a greater number of gamma correction channels are required, two or more BUF11705 devices can be used in parallel, as shown in Figure 25. This capability provides a cost-effective way of creating more reference voltages over the use of quad-channel op amps or buffers. The suggested configuration in Figure 25 simplifies layout. The various different channel versions provide a high degree of flexibility and also minimize total cost and space.

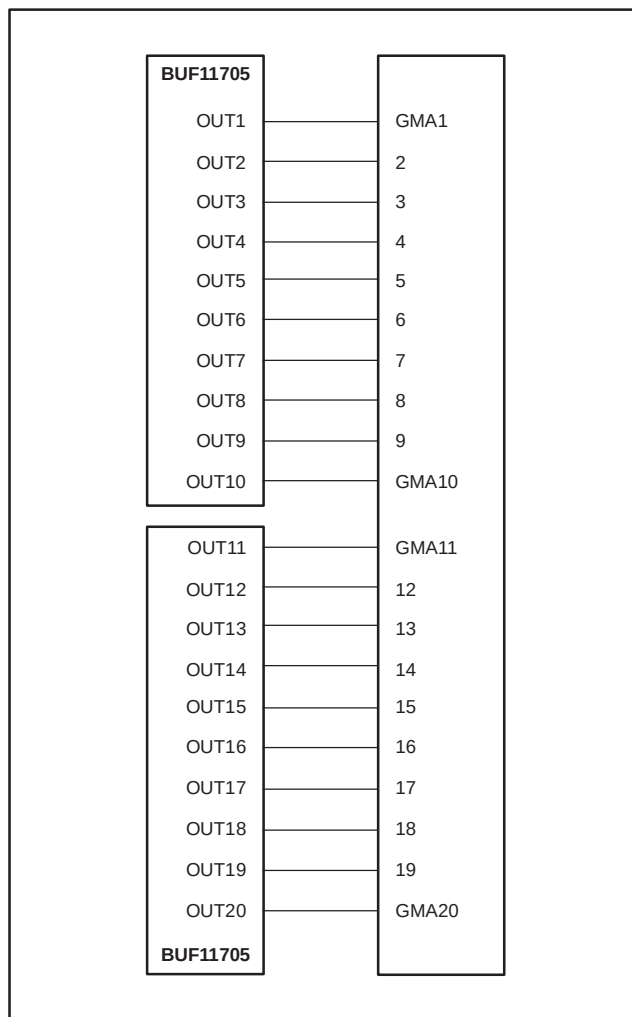


Figure 25. Creating > 10 Gamma Voltage Channels

COMPLETE LCD SOLUTION FROM TI

In addition to the BUF11705 line of gamma correction buffers, TI offers a complete set of ICs for the LCD panel

market, including various power-supply solutions, and audio power solutions. Figure 26 shows the total IC solution from TI.

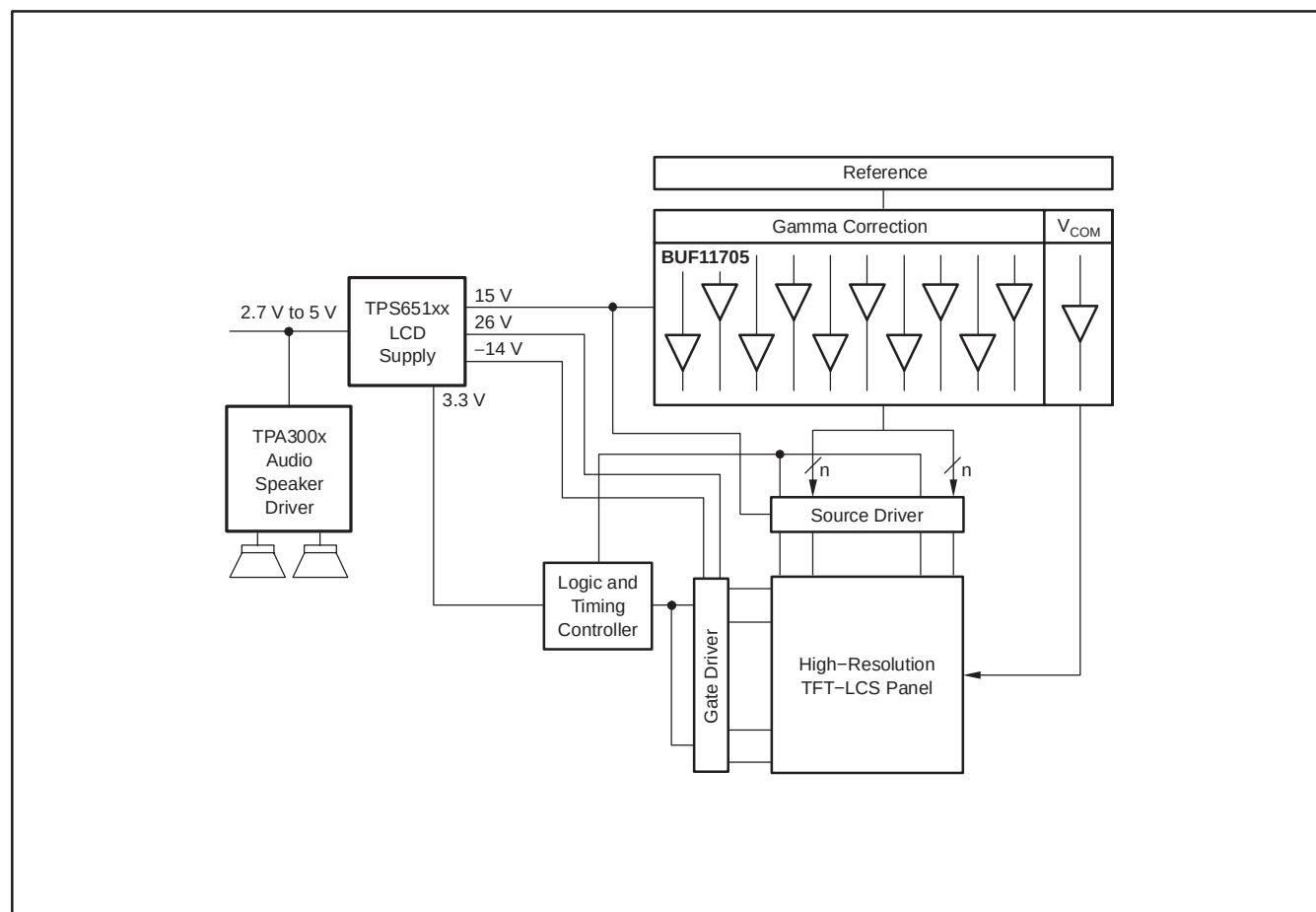


Figure 26. TI LCD Solution

GENERAL PowerPAD DESIGN CONSIDERATIONS

The BUF11705 is available in the thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted, as shown in Figure 27(a) and (b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 27(c). Due to this thermal pad having direct thermal contact with the die, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. **Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation.** This provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the most negative supply voltage of the device.

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns can be seen in technical brief, SLMA002 *PowerPAD Thermally-Enhanced Package*, available for download at www.ti.com. These holes should be 13 mils (0.33 mm) in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow.

3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the BUF11705 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; so that, wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. Web connections make the soldering of vias easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUF11705 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its ten holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the BUF11705 IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.

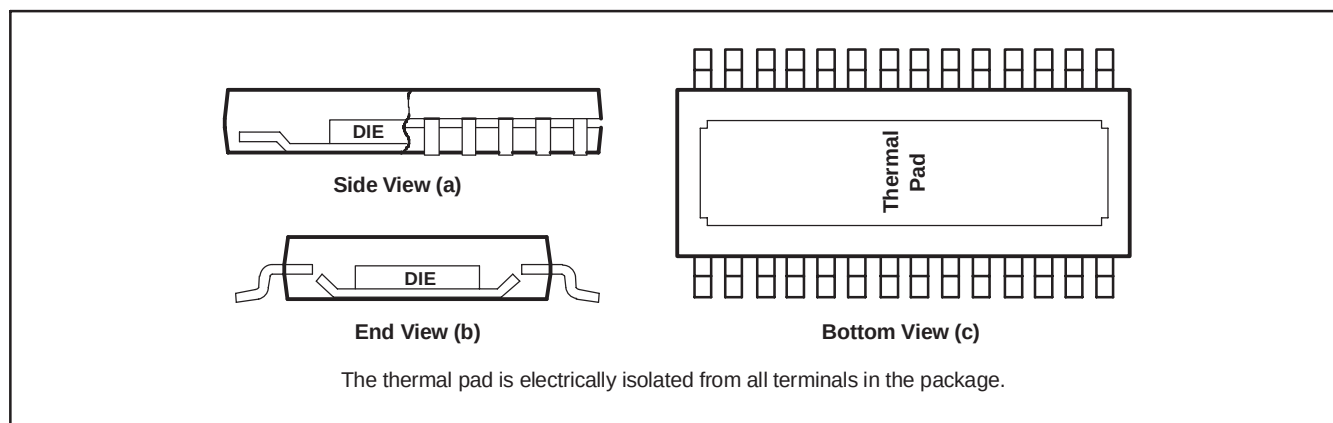


Figure 27. Views of Thermally-Enhanced DGN Package

For a given θ_{JA} , the maximum power dissipation is shown in Figure 28, and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = maximum power dissipation (W)

T_{MAX} = absolute maximum junction temperature (125°C)

T_A = free-ambient air temperature (°C)

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} = thermal coefficient from junction to case (°C/W)

θ_{CA} = thermal coefficient from case-to-ambient air (°C/W)

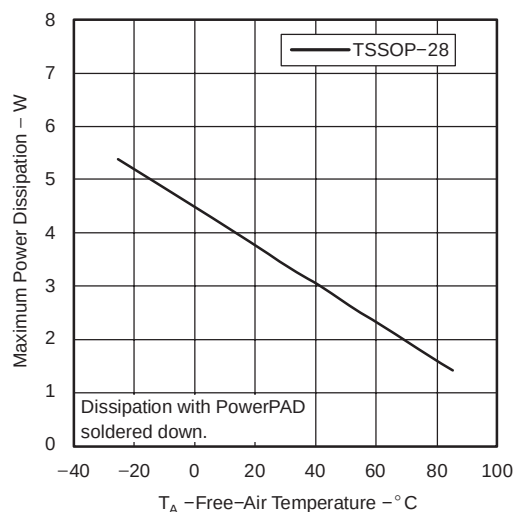


Figure 28. Views of Thermally-Enhanced DGN Package

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BUF11705AIPWPR	NRND	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	BUF11705
BUF11705AIPWPR.A	NRND	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	BUF11705

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

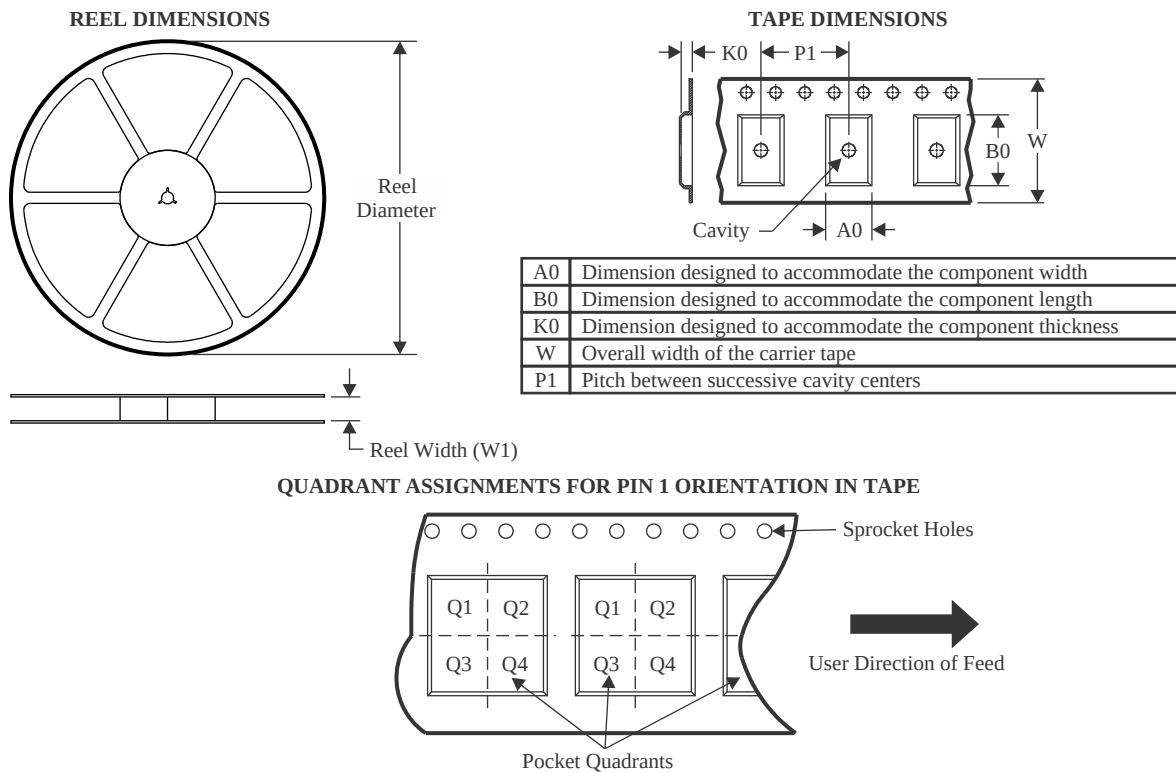
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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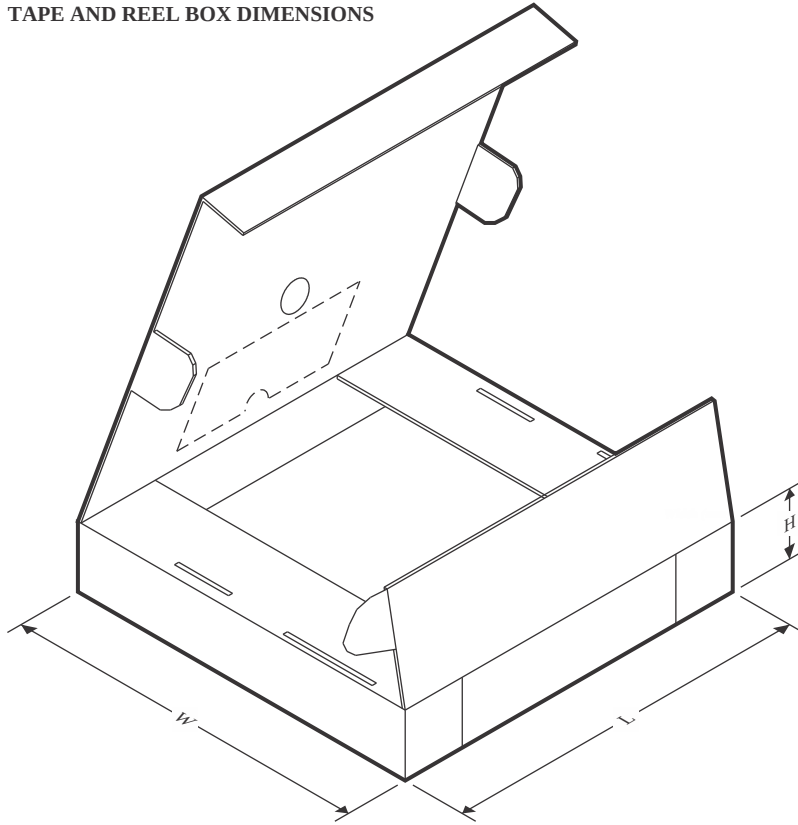
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF11705AIPWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF11705AIPWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

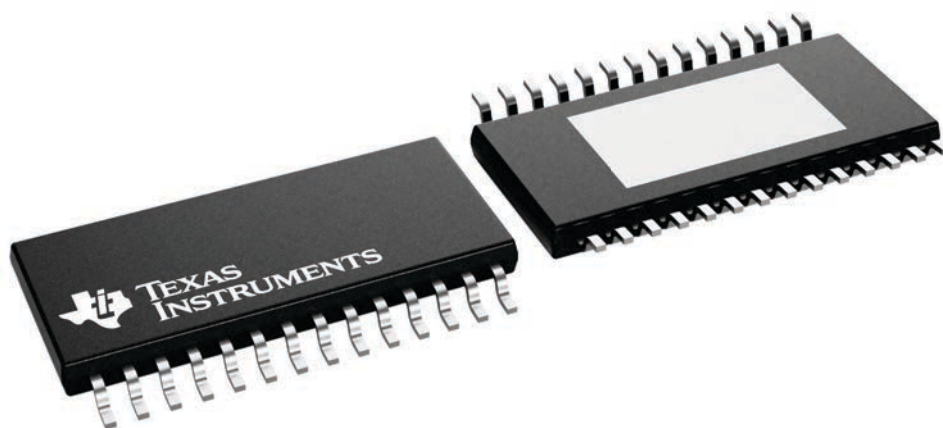
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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