



## Programmable Voltage Source with Memory

### FEATURES

- 10-BIT RESOLUTION
- RAIL-TO-RAIL OUTPUT
- ONBOARD NONVOLATILE MEMORY
- $I_{OUT}$ : 100mA
- LOW SUPPLY CURRENT: 900 $\mu$ A
- SUPPLY VOLTAGE: 7V to 18V
- DIGITAL SUPPLY: 2.0V to 5.5V
- INDUSTRY-STANDARD, TWO-WIRE INTERFACE
- HIGH ESD RATING:  
2kV HBM, 500V CDM

### APPLICATIONS

- LCD PANEL  $V_{COM}$  CALIBRATION
- LCD PANEL BRIGHTNESS AND CONTRAST CONTROL
- POTENTIOMETER REPLACEMENT
- MOTOR DRIVE
- PROGRAMMABLE POWER SUPPLY
- PROGRAMMABLE OFFSET ADJUSTMENT
- ACTUATOR CONTROL

### BUF01900, BUF01901 RELATED PRODUCTS

| FEATURES                                           | PRODUCT  |
|----------------------------------------------------|----------|
| 22V High Supply Voltage Gamma Buffers              | BUF11705 |
| 12--Channel Programmable Buffer, 10-Bit, $V_{COM}$ | BUF12800 |
| 20-Channel Programmable Buffer, 10-Bit, $V_{COM}$  | BUF20800 |
| 16-Channel Programmable Buffer with Memory         | BUF16820 |
| 20-Channel Programmable Buffer with Memory         | BUF20820 |

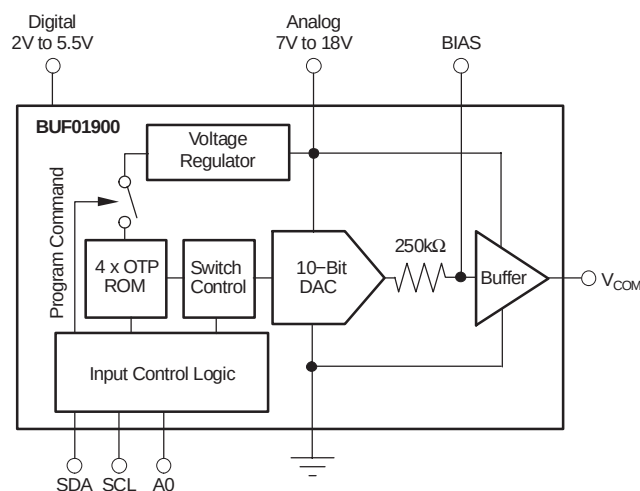
### DESCRIPTION

The BUF01900 and BUF01901 provide a programmable voltage output with 10-bit resolution. Programming of the output occurs through an industry-standard, two-wire serial interface. Once the correct  $V_{COM}$  voltage is established it can easily be stored into the integrated nonvolatile memory.

An initial output voltage and adjustment range can be set by an external resistor-divider. With its large output current capability (up to 100mA), the BUF01900 and BUF01901 are ideally suited as programmable  $V_{COM}$  calibrators in LCD panels.

The BUF01901 has the digital-to-analog converter (DAC) output brought out directly. It has a slightly lower cost than the BUF01900, and works very well with the integrated  $V_{COM}$  in traditional gamma buffers such as the BUFxx702, BUFxx703, BUFxx704 and BUF11705.

The BUF01900 and BUF01901 are both available in TSSOP-8 and 3mm x 3mm DFN-10 packages. The DFN-10 package (only 0.9mm in height) is especially well-suited for notebook computers. Both devices are specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a registered trademark of Texas Instruments. All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|                                     |                       |
|-------------------------------------|-----------------------|
| Supply Voltage, $V_S$               | +20V                  |
| Supply Voltage, $V_{SD}$            | +6V                   |
| Signal Input Terminals,<br>BIAS:    |                       |
| Voltage                             | -0.5V to $V_S + 0.5V$ |
| SCL, SDA, A0, A1:                   |                       |
| Voltage                             | -0.5V to +6V          |
| Current                             | ±10mA                 |
| Output Short Circuit <sup>(2)</sup> | Continuous            |
| Operating Temperature               | -40°C to +95°C        |
| Storage Temperature                 | -65°C to +150°C       |
| Junction Temperature                | +125°C                |
| ESD Rating:                         |                       |
| Human Body Model (HBM)              | 2000V                 |
| Charged-Device Model (CDM)          | 500V                  |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

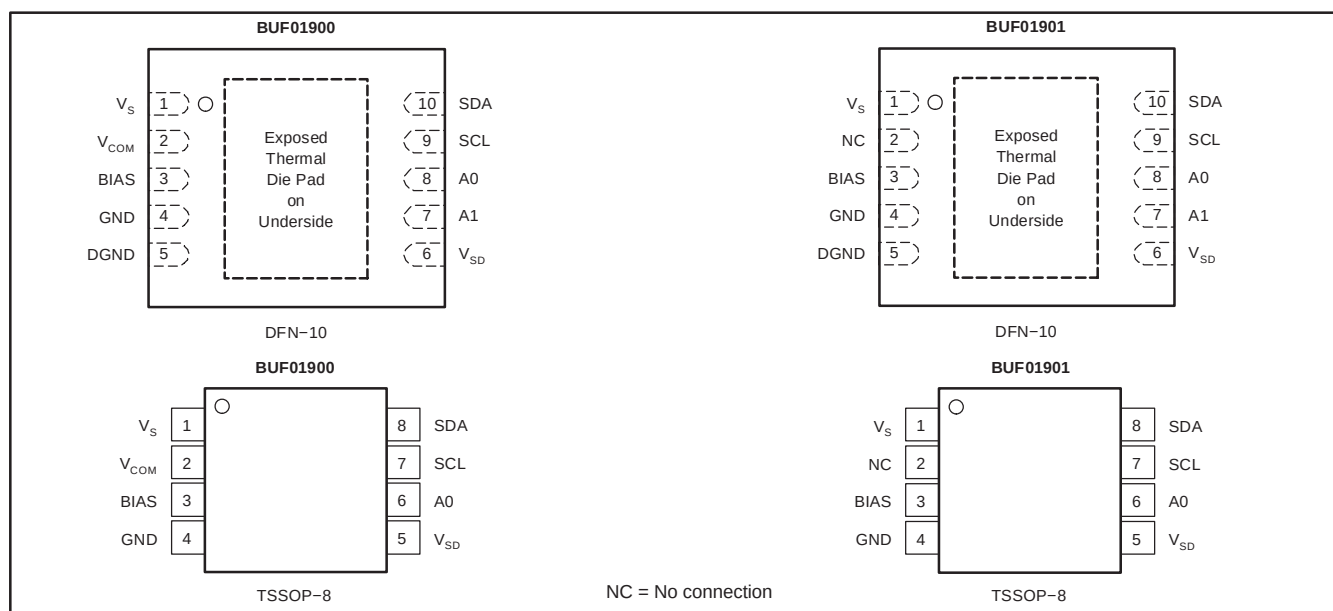
(2) Short-circuit to ground.

## ORDERING INFORMATION<sup>(1)</sup>

| PRODUCT  | PACKAGE-LEAD | PACKAGE DESIGNATOR | PACKAGE MARKING |
|----------|--------------|--------------------|-----------------|
| BUF01900 | DFN-10       | DRC                | BOO             |
| BUF01900 | TSSOP-8      | PW                 | F01900          |
| BUF01901 | DFN-10       | DRC                | BOP             |
| BUF01901 | TSSOP-8      | PW                 | F01901          |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## PIN CONFIGURATIONS



## ELECTRICAL CHARACTERISTICS

**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

At  $T_A = +25^{\circ}\text{C}$ ,  $V_S = 18\text{V}$ ,  $V_{SD} = 5\text{V}$ ,  $R_L = 1.5\text{k}\Omega$  connected to ground, and  $C_L = 200\text{pF}$ , unless otherwise noted.

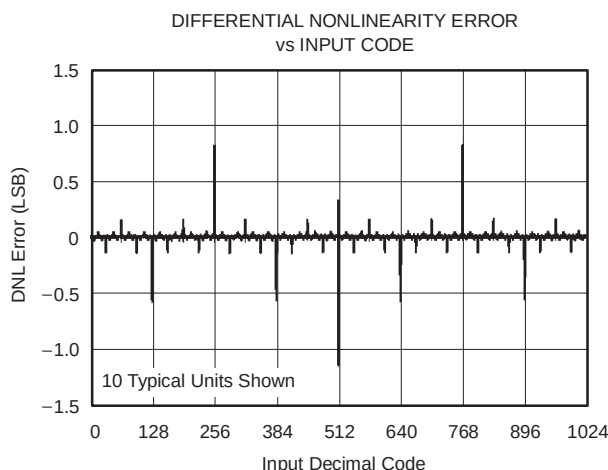
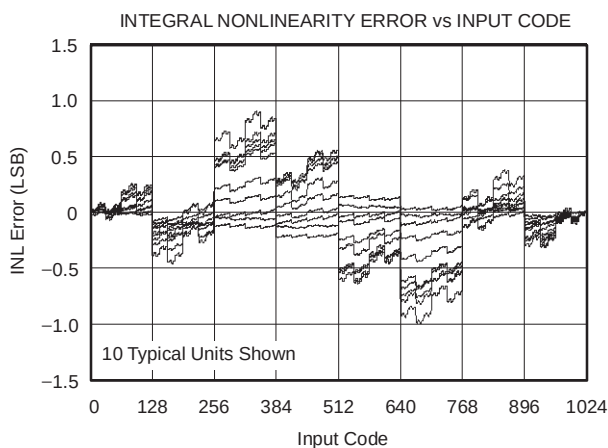
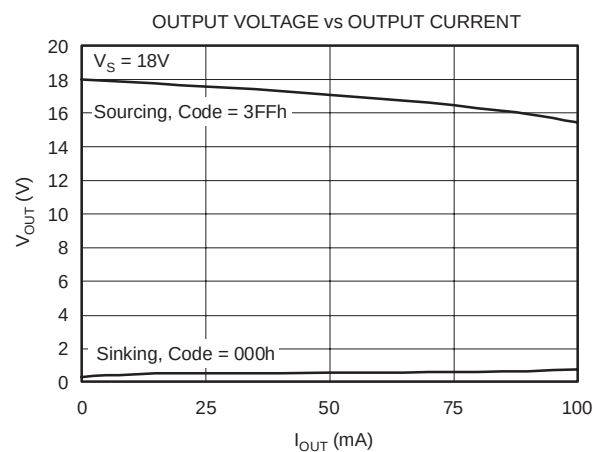
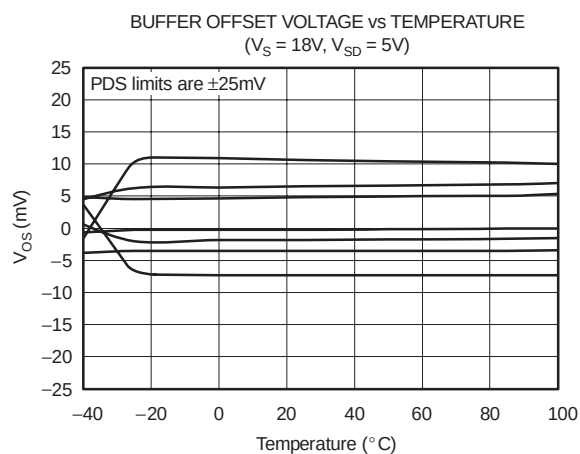
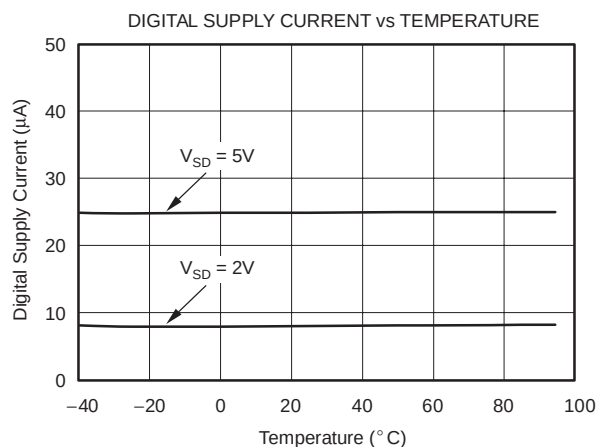
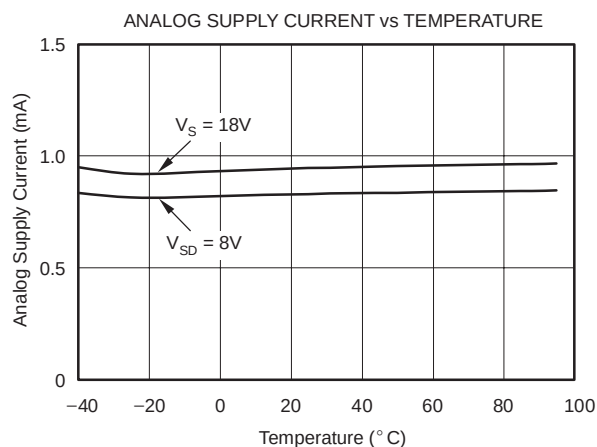
| PARAMETER                                                | CONDITIONS                                                                                                                           | BUF01900, BUF01901  |                           |                          | UNIT                            |
|----------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|---------------------|---------------------------|--------------------------|---------------------------------|
|                                                          |                                                                                                                                      | MIN                 | TYP                       | MAX                      |                                 |
| <b>ANALOG</b>                                            |                                                                                                                                      |                     |                           |                          |                                 |
| $V_{COM}$ Output Swing <sup>(1)</sup>                    | <b>Sourcing 10mA, Code 1023</b><br><b>Sinking 10mA, Code 00</b><br><b>Sourcing 100mA, Code 1023</b><br><b>Sinking 100mA, Code 00</b> | <b>17.7</b>         | <b>17.8</b><br><b>0.6</b> | <b>1</b>                 | <b>V</b><br><b>V</b>            |
| $V_{COM}$ Output Reset and Power-Up Value <sup>(1)</sup> | OTP not programmed, Code 512                                                                                                         | <b>15</b>           | <b>16</b><br><b>0.75</b>  | <b>1</b>                 | <b>V</b><br><b>V</b>            |
| Nominal $V_{BIAS}$ Output Impedance                      | No Load on $V_{BIAS}$ , $V_{COM}$                                                                                                    |                     | $V_S/2$<br>250            |                          | $\text{k}\Omega$                |
| Program to Out Delay                                     |                                                                                                                                      |                     | 5                         |                          | $\mu\text{s}$                   |
| Output Accuracy                                          | $1\text{V} < V_{COM} < 17.7$                                                                                                         |                     | 20                        | 50                       | mV                              |
| Load Regulation                                          | $V_{OUT} = V_S/2$ , $I_{OUT} = +50\text{mA}$ to $-50\text{mA}$ Step                                                                  |                     | 0.5                       | 1.5                      | mV/mA                           |
| $V_{COM}$ <sup>(1)</sup> Offset                          |                                                                                                                                      |                     | $\pm 5$                   | $\pm 25$                 | mV                              |
| Offset Drift                                             | $-25^{\circ}\text{C}$ to $+100^{\circ}\text{C}$                                                                                      |                     | 5                         |                          | $\mu\text{V}/^{\circ}\text{C}$  |
| Common-Mode Range                                        |                                                                                                                                      |                     | 0.8 to 18                 |                          | V                               |
| Common-Mode Rejection                                    | $0.8\text{V} < V_{IN} < 17.9\text{V}$                                                                                                |                     | 85                        |                          | dB                              |
| Slew Rate                                                |                                                                                                                                      |                     | 5                         |                          | V/ $\mu\text{s}$                |
| $V_{BIAS}$                                               | No Load on $V_{BIAS}$                                                                                                                |                     |                           |                          |                                 |
| Integral Nonlinearity                                    |                                                                                                                                      |                     | 0.1                       | 2                        | LSB                             |
| Differential Nonlinearity                                |                                                                                                                                      |                     | 0.1                       | 2                        | LSB                             |
| Gain Error                                               |                                                                                                                                      |                     | 0.1                       | 1                        | %FSC                            |
| Accuracy                                                 |                                                                                                                                      |                     | 20                        | 50                       | mV                              |
| <b>ANALOG POWER SUPPLY</b>                               |                                                                                                                                      |                     |                           |                          |                                 |
| Operating Range <sup>(2)</sup>                           | $V_S$                                                                                                                                | 7                   |                           | 18                       | V                               |
| Total Analog Supply Current                              | $I_S$                                                                                                                                |                     | 0.9                       | 1.5                      | mA                              |
| <b>over Temperature</b>                                  |                                                                                                                                      |                     |                           | <b>1.5</b>               | <b>mA</b>                       |
| <b>DIGITAL</b>                                           |                                                                                                                                      |                     |                           |                          |                                 |
| Logic 1 Input Voltage                                    | $V_{IH}$                                                                                                                             | $0.7 \times V_{SD}$ |                           |                          | V                               |
| Logic 0 Input Voltage                                    | $V_{IL}$                                                                                                                             |                     |                           | $0.3 \times V_{SD}$      | V                               |
| Logic 0 Output Voltage                                   | $V_{OL}$                                                                                                                             |                     | 0.15                      | 0.4                      | V                               |
| Input Leakage                                            |                                                                                                                                      |                     | $\pm 0.01$                | $\pm 10$                 | $\mu\text{A}$                   |
| Clock Frequency                                          | $f_{CLK}$                                                                                                                            |                     |                           | <b>400</b><br><b>3.4</b> | <b>kHz</b><br><b>MHz</b>        |
|                                                          |                                                                                                                                      |                     |                           |                          |                                 |
| <b>DIGITAL POWER SUPPLY</b>                              |                                                                                                                                      |                     |                           |                          |                                 |
| Operating Voltage Range                                  | $V_{SD}$                                                                                                                             | 2.0                 |                           | 5.5                      | V                               |
| Digital Supply Current <sup>(2)</sup>                    | $I_{SD}$                                                                                                                             |                     | 25                        | 50                       | $\mu\text{A}$                   |
| <b>over Temperature</b>                                  |                                                                                                                                      |                     | <b>100</b>                |                          | <b><math>\mu\text{A}</math></b> |
| <b>TEMPERATURE</b>                                       |                                                                                                                                      |                     |                           |                          |                                 |
| Specified Temperature Range                              |                                                                                                                                      | $-40$               |                           | $+85$                    | $^{\circ}\text{C}$              |
| Operating Temperature Range                              |                                                                                                                                      | $-40$               |                           | $+95$                    | $^{\circ}\text{C}$              |
| Storage Temperature Range                                |                                                                                                                                      | $-65$               |                           | $+150$                   | $^{\circ}\text{C}$              |
| Thermal Resistance                                       | $\theta_{JA}$                                                                                                                        |                     |                           |                          |                                 |
| TSSOP-8                                                  |                                                                                                                                      |                     | 150                       |                          | $^{\circ}\text{C}/\text{W}$     |
| DFN-10                                                   |                                                                                                                                      |                     | 47                        |                          | $^{\circ}\text{C}/\text{W}$     |

(1) BUF01900 only.

(2) Minimum analog supply voltage is 8.5V when programming OTP memory.

## TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 18\text{V}$ ,  $V_{SD} = 5\text{V}$ ,  $R_L = 1.5\text{k}\Omega$  connected to ground, and  $C_L = 200\text{pF}$ , unless otherwise noted.



## TYPICAL CHARACTERISTICS (cont)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 18\text{V}$ ,  $V_{SD} = 5\text{V}$ ,  $R_L = 1.5\text{k}\Omega$  connected to ground, and  $C_L = 200\text{pF}$ , unless otherwise noted.

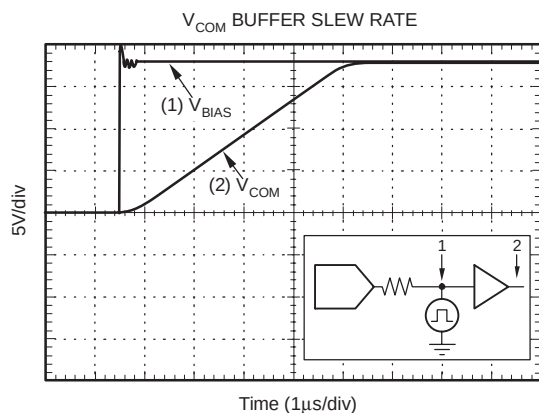


Figure 7

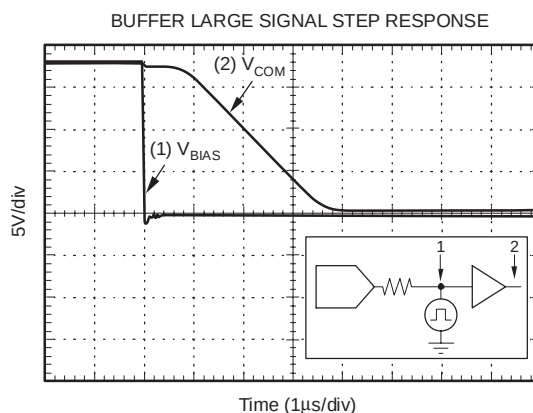


Figure 8

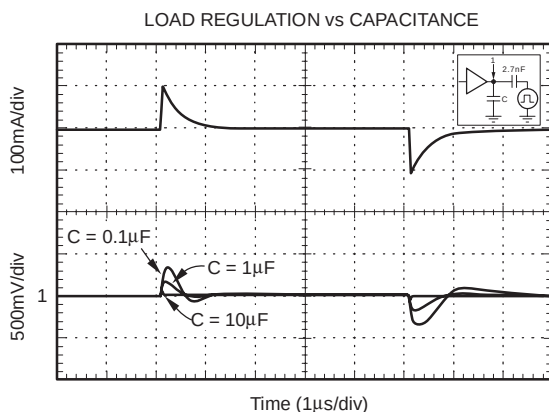


Figure 9

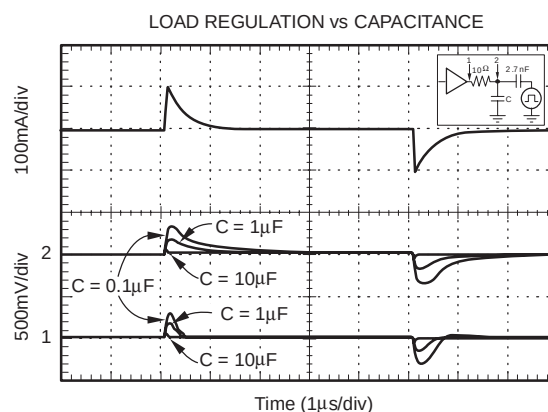


Figure 10

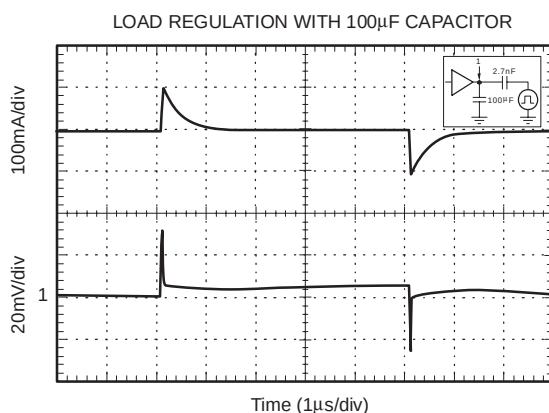


Figure 11

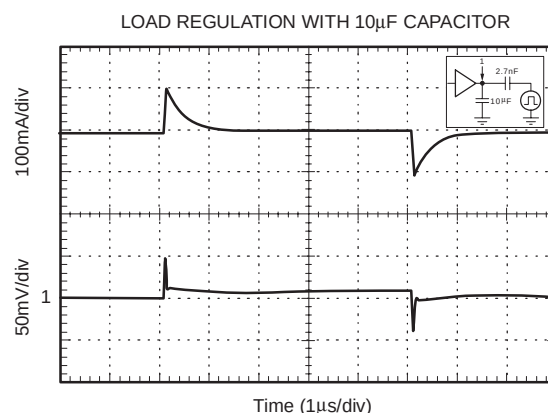
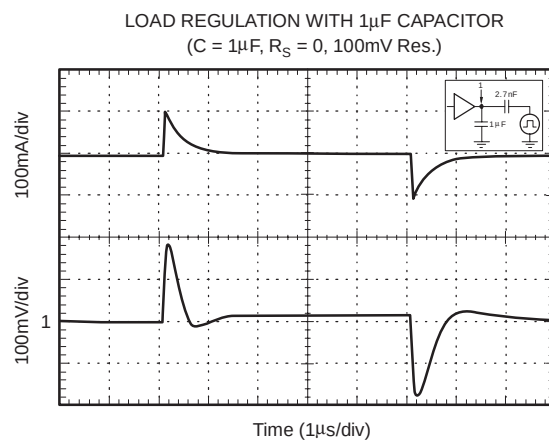


Figure 12

## TYPICAL CHARACTERISTICS (cont)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 18\text{V}$ ,  $V_{SD} = 5\text{V}$ ,  $R_L = 1.5\text{k}\Omega$  connected to ground, and  $C_L = 200\text{pF}$ , unless otherwise noted.



**Figure 13**

## APPLICATIONS INFORMATION

### OVERVIEW

The BUF0190x family of products consists of a 10-bit digital-to-analog converter (DAC) that is programmed through an industry-standard two-wire interface. It contains on-chip nonvolatile memory that stores a specific DAC value that is read at power-up. The BUF0190x family consists of two devices: The BUF01900 contains a voltage buffer that is capable of driving high-current; the BUF01901 is a lower-cost version without the buffer. The BUF0190x is especially well-suited for  $V_{COM}$  calibration in LCD panels; however, it can also be used in many other applications. Figure 14 shows the BUF01900 in a typical configuration.

### BUF01900: ON-CHIP BUFFER

Unlike many programmable  $V_{COM}$  calibrators on the market, the BUF01900 offers an integrated  $V_{COM}$  buffer with high current output drive capability. The output is capable of delivering peak currents over 100mA to within 4V from the positive supply and to within 2V from the negative supply. Using this option is very cost-effective and convenient in systems that do not use multi-channel gamma buffers with integrated  $V_{COM}$  drive. Figure 15 shows the BUF01900 in a typical configuration.

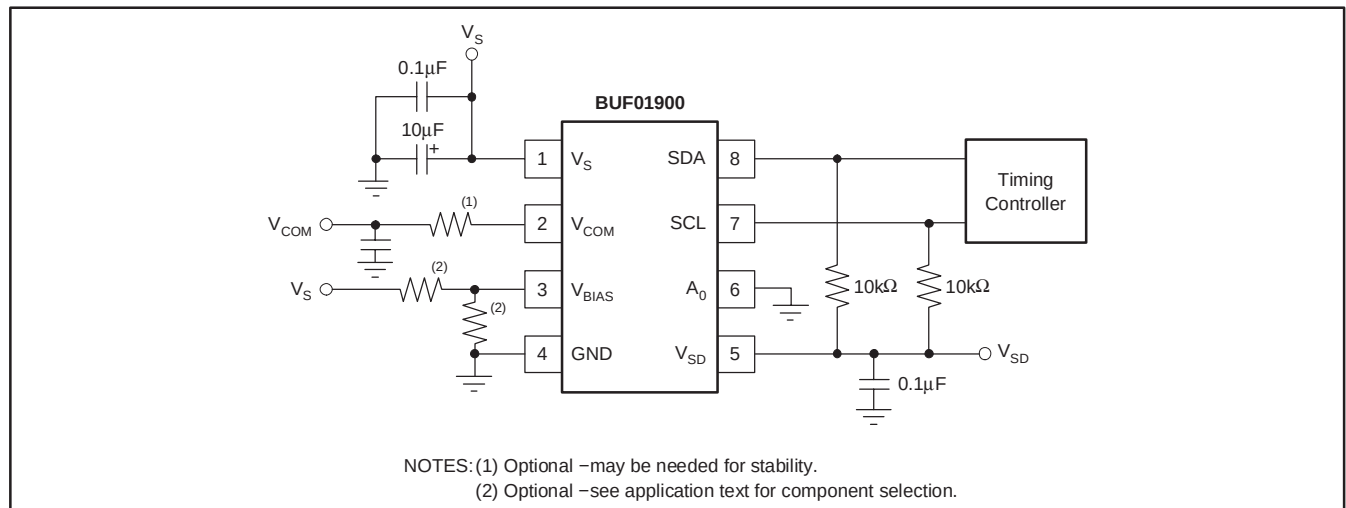


Figure 14. Typical Application Diagram

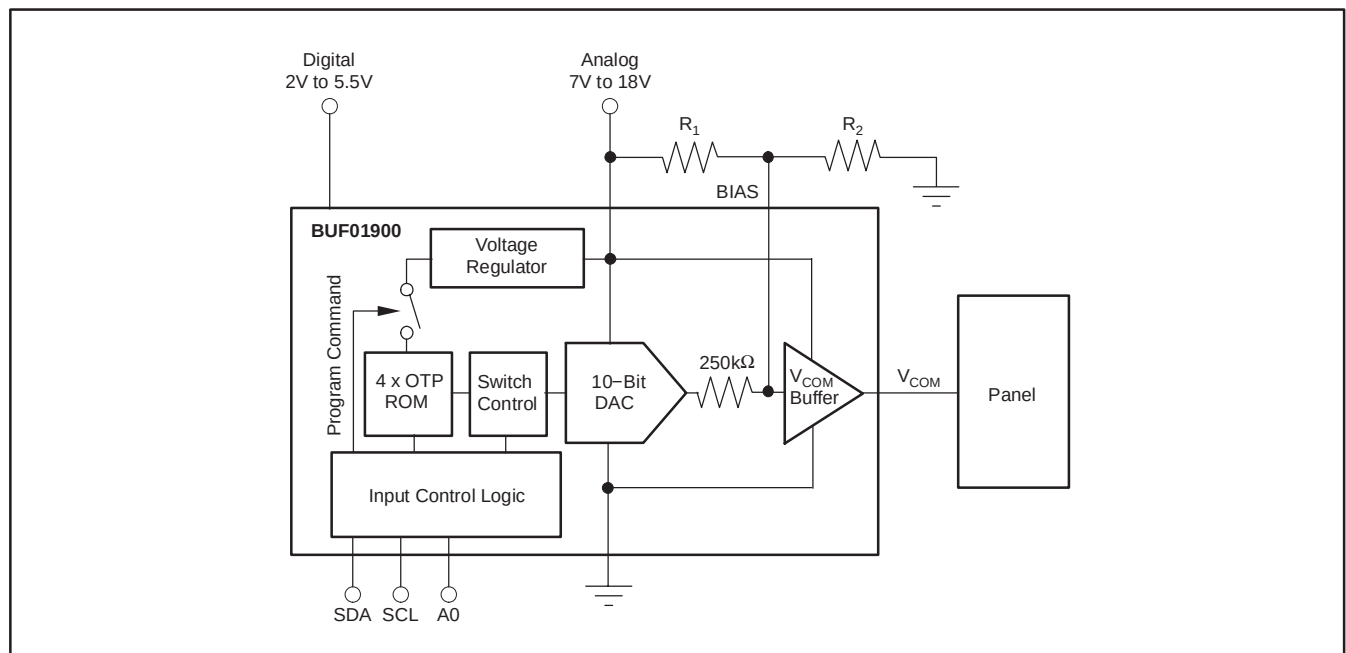


Figure 15. BUF01900 Typical Configuration

## BUF01901: USING EXTERNAL $V_{COM}$ BUFFER

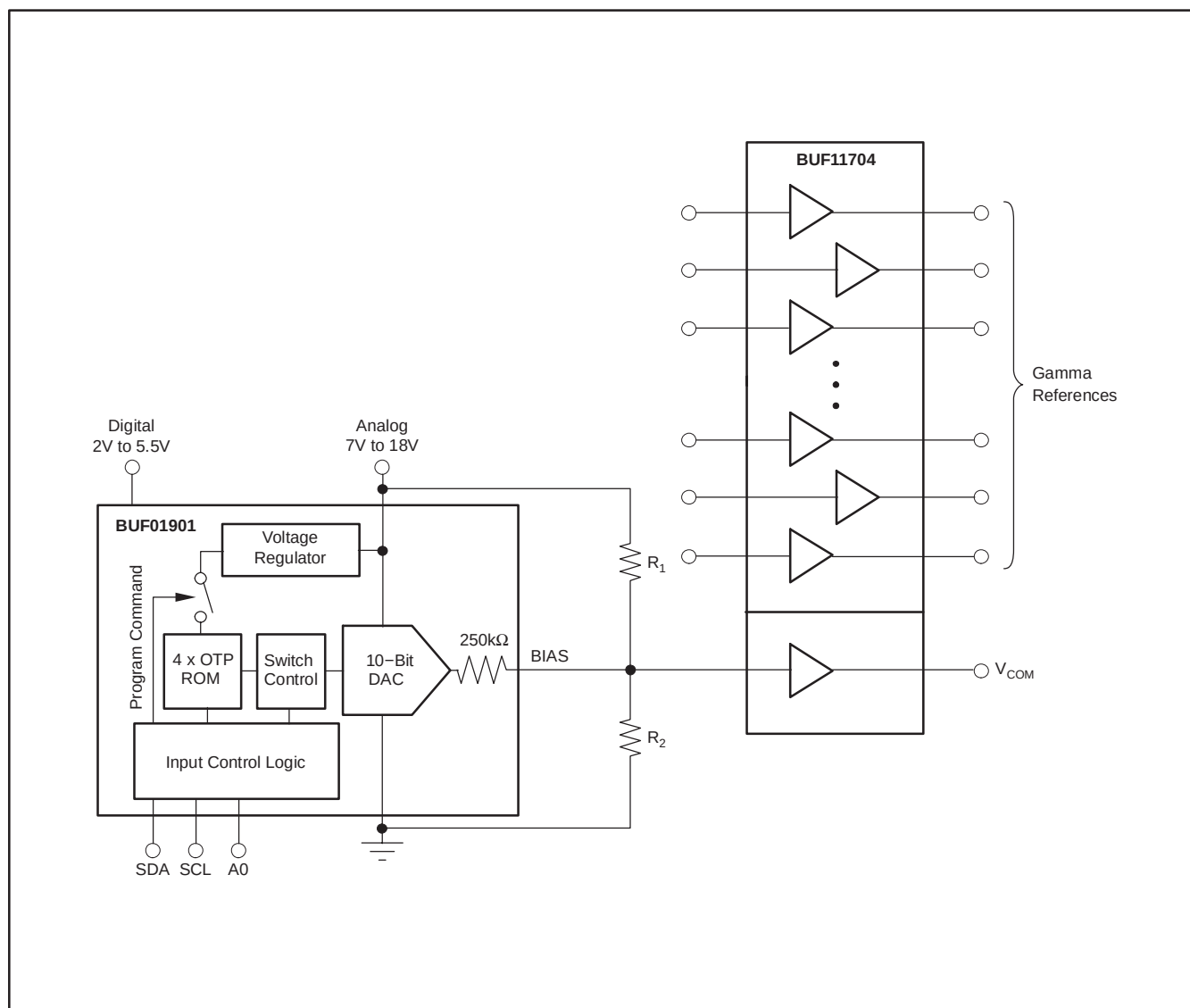
Many LCD panel modules use gamma buffers, such as TI's BUFxx704, BUFxx703, BUF11702 and the new BUF11705, that already include an integrated  $V_{COM}$  driver. Some other LCD modules use more complicated compensation schemes that require an external high-speed  $V_{COM}$  op amp. BUF01901 is optimized for lowest cost and is intended to be used with an external  $V_{COM}$  buffer or op amp. Figure 16 illustrates a typical configuration of the BUF01901 with the BUF11705.

## ON-CHIP NONVOLATILE MEMORY

The BUF0190x is optimized for the smallest die size available and consequently the lowest cost to support high vol-

ume production. The on-chip OTP (one-time-programmable) memory helps to achieve significant die size reduction over EEPROM memory technology. This reduction is partly because of the smaller area of the OTP memory cell, but also a result of the fact that an EEPROM requires a high programming voltage typically generated with an onboard charge pump. OTP memory technology does not require the higher programming voltage; consequently, no charge pump is needed, resulting in a smaller and lower-cost solution.

During production, the  $V_{COM}$  voltage is typically adjusted only once. However, to allow for programming errors and rework, the BUF0190x supports a total of four write cycles to the OTP memory. This capacity means that the previously programmed code in the OTP can be overwritten a total of three times.



**Figure 16. BUF01901 Typical Configuration**



## POWER-SUPPLY VOLTAGE

The BUF0190x can be powered using an analog supply voltage from 7V to 18V, and a digital supply from 2V to 5.5V. The digital supply must be applied prior to the analog supply to avoid excessive current and power consumption. During programming of the OTP, the analog power supply must be at least 8.5V.

## BUFFER INPUT AND OUTPUT RANGE

The integrated buffer has a single p-channel input stage. The input range includes the positive supply and extends down to typically 0.8V above the negative supply (GND). In a typical LCD application, this is normally sufficient because the nominal  $V_{COM}$  level is often close to  $V_2/2$  and, therefore, fairly far away from either supply rail. In addition, the adjustment range is usually not much larger than 1V in either direction of the nominal  $V_{COM}$  voltage. In applications requiring a wider output swing, the output voltage to the buffer should be limited to approximately 0.8V above the negative power supply to keep the buffer input stage in its linear operating region. For lower input voltages, the output results might not be valid; however, they will also not lead to damage of the device.

The Rail-to-Rail output stage is designed to drive large peak currents greater than 100mA.

## TWO-WIRE BUS OVERVIEW

The BUF0190x communicates through an industry-standard, two-wire interface to receive data in slave mode. This standard uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a *master*, and the devices controlled by the master are *slaves*. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH will be interpreted as a START or STOP condition.

Once all data has been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH.

The BUF0190x can act only as a slave device; therefore, it never drives SCL. The SCL is only an input for the BUF0190x.

## ADDRESSING THE BUF01900 AND BUF01901

The address of the BUF0190x in the TSSOP-8 package is 111011x, where x is the state of the A0 pin. When the A0 pin is LOW, the device acknowledges on address 76h. If the A0 pin is HIGH, the device acknowledges on address 77h. Table 1 summarizes device addresses.

**Table 1. Quick-Reference Table of Addresses**

| DEVICE/COMPONENT                                                       | ADDRESS |
|------------------------------------------------------------------------|---------|
| <b>TSSOP Package:</b>                                                  |         |
| A0 pin is LOW<br>(device will acknowledge on address 76h)              | 1110110 |
| A0 pin is HIGH<br>(device will acknowledge on address 77h)             | 1110111 |
| <b>DFN Package:</b>                                                    |         |
| A0 pin is LOW, A1 is LOW<br>(device will acknowledge on address 74h)   | 1110100 |
| A0 pin is HIGH, A1 is LOW<br>(device will acknowledge on address 75h)  | 1110101 |
| A0 pin is LOW, A1 is HIGH<br>(device will acknowledge on address 76h)  | 1110110 |
| A0 pin is HIGH, A1 is HIGH<br>(device will acknowledge on address 77h) | 1110111 |

The address of the BUF0190x in the DFN-10 package is 11101yx, where x is the state of the A0 pin and y is the state of the A1 pin. When the A0 and A1 pins are both LOW, the device acknowledges on address 74h. If the A0 is HIGH and A1 is LOW, the device acknowledges on address 75h. When the A0 is LOW, and A1 is HIGH, the device acknowledges on address 76h. If the A0 and A1 pins are both HIGH, the device address is 77h.

Other addresses are possible through a simple mask change. Contact your TI representative for ordering information and availability.

## DATA RATES

The two-wire bus operates in one of three speed modes:

- Standard: allows a clock frequency of up to 100kHz;
- Fast: allows a clock frequency of up to 400kHz; and
- High-speed mode (or Hs mode): allows a clock frequency of up to 3.4MHz.

The BUF0190x is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001xxx, with  $SCL \leq 400\text{kHz}$ , following the START condition; xxx are bits unique to the Hs-capable master, which can be any value. This byte is called the *Hs master code*. (Note that this is different from normal address bytes—the low bit does not indicate read/write status.) The BUF0190x will respond to the High-speed command regardless of the value of these last three bits. The BUF0190x does not acknowledge this byte; the communication protocol prohibits acknowledgment of the Hs master code. On receiving a master code, the BUF0190x switches on its Hs mode filters, and communicates at up to 3.4MHz.

Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF0190x switches out of Hs mode with the next STOP condition.

## GENERAL CALL RESET AND POWER-UP

The BUF0190x responds to a General Call Reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110). The BUF0190x acknowledges both bytes. Upon receiving a General Call Reset, the BUF0190x performs a full internal reset, as though it had been powered off and then on. It always acknowledges the General Call address byte of 00h (0000 0000), but does not acknowledge any General Call data bytes other than 06h (0000 0110).

The BUF0190x automatically performs a reset upon power-up. As part of the reset, the BUF0190x is configured for the output to change to the programmed OTP memory value, or to mid-scale, '1000000000', if the OTP value has not been programmed. Table 2 provides a summary of command codes.

**Table 2. Quick-Reference Table of Command Codes**

| COMMAND            | CODE                                                                                                                                  |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| General Call Reset | Address byte of 00h followed by a data byte of 06h.                                                                                   |
| High-Speed Mode    | 00001xxx, with $SCL \leq 400\text{kHz}$ ; where xxx are bits unique to the Hs-capable master. This byte is called the Hs master code. |

## READ/WRITE OPERATIONS:

Read commands are performed by setting the read/write bit HIGH. Setting the read/write bit LOW performs a write transaction.

Figure 17 and Figure 18 show the timing diagrams for read and write operations.

### Writing:

*To write to the DAC register:*

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF01900/BUF01901 will acknowledge this byte.
3. Send two bytes of data for the DAC register. Begin by sending the most significant byte (bits D15—D8; only bits D9 and D8 are used, and D15—D13 must *not* be 010 or 001), followed by the least significant byte (bits D7—D0). The register is updated after receiving the second byte.
4. Send a STOP condition on the bus.

The BUF0190x acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the DAC output will not update.

### Reading:

*To read the register of the DAC:*

1. Send a START condition on the bus.
2. Send the device address and read/write bit = HIGH. The BUF0190x will acknowledge this byte.
3. Receive two bytes of data. The first received byte is the most significant byte (bits D15—D8; only bits D9 and D8 have meaning, and bits D15—D12 will show the programming status of the OTP memory). See Table 3. The next byte is the least significant byte (bits D7—D0).
4. Acknowledge after receiving the first byte only.
5. Do not acknowledge the second byte of data or send a STOP condition on the bus.

Communication may be terminated by the master by sending a premature STOP or START condition on the bus, or by not sending the Acknowledge.

**Table 3. OTP Memory Status**

| CODE<br>(Bits D15 – D12) | OTP PROGRAMMING STATUS             |
|--------------------------|------------------------------------|
| 0000                     | OTP has not been programmed.       |
| 0001                     | OPT has been programmed once.      |
| 0011                     | OTP has programmed twice.          |
| 0111                     | OPT has programmed three times.    |
| 1111                     | OTP has programmed all four times. |

## ACQUIRE OF OTP MEMORY

An acquire command updates the DAC output to the value stored in OTP memory. If the OTP memory has not been programmed, the DAC output code is '0000000000'.

Figure 19 shows the timing diagram for the acquire command.

### Acquire Command

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The device will acknowledge this byte.
3. Send the acquire command. Bits D7—D5 must be set to 001. Bits D4—D0 do not have meaning. This byte will be acknowledged.
4. Send a STOP condition on the bus.

### Writing OTP Memory

The BUF0190x is able to write to the OTP memory a maximum of four times. Writing to the OTP memory a fourth time uses all available memory and disables the ability to perform additional writes (see table 3). A reset or acquire command updates the DAC output to the most recently written OTP memory value.

When programming the OTP memory, the analog supply voltage must be between 8.5V and 18V.

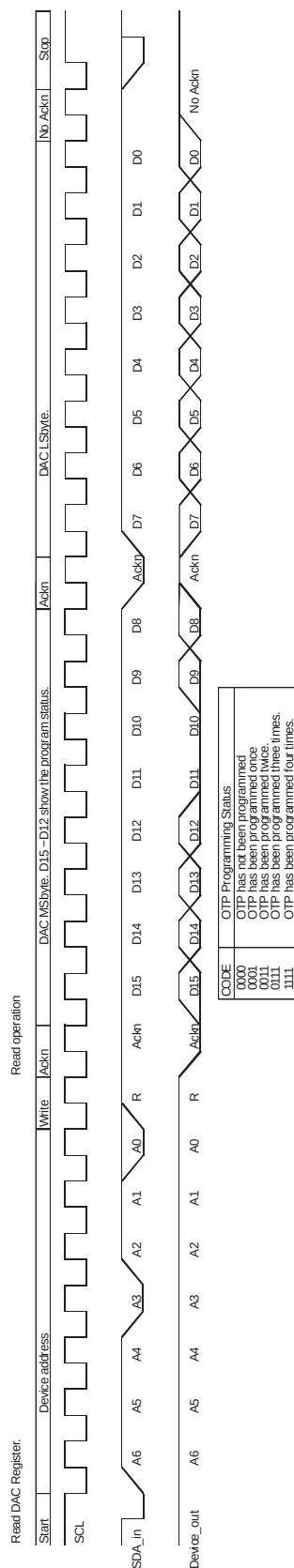
Write commands are performed by setting the read/write bit LOW.

*To write to OTP memory:*

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF0190x acknowledges this byte.
3. Send two bytes of data for the OTP memory. Begin by sending the most significant byte first (bits D15—D8, of which only bits D9 and D8 are data bits, and bits D15—D13 must be 010), followed by the least significant byte (bits D7—D0). The register updates after receiving the second byte.
4. Send a STOP condition on the bus.

The BUF0190x acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified OTP register will not be updated. Writing an OTP register updates the DAC output voltage.

Programming timing is taken from the two-wire bus. Therefore, the master must provide correct timing on the bus to ensure data is successfully written into OTP memory. Figure 20 shows the timing requirements for timing when the OTP write supply and OTP write signal are active.



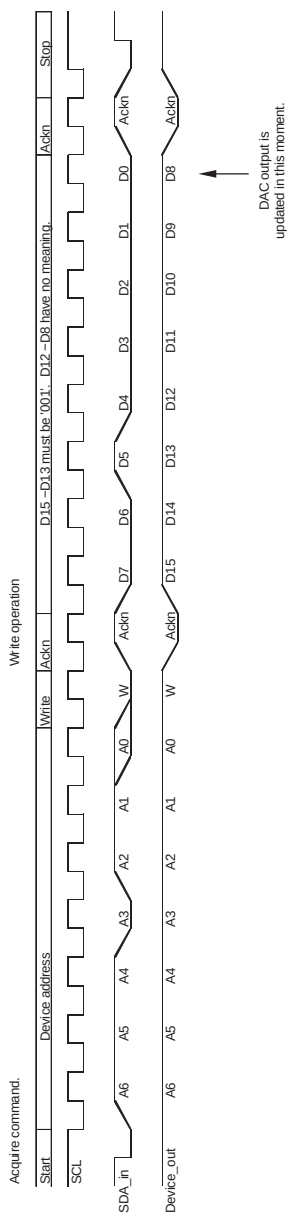


Figure 19. Timing Diagram for Acquire Command

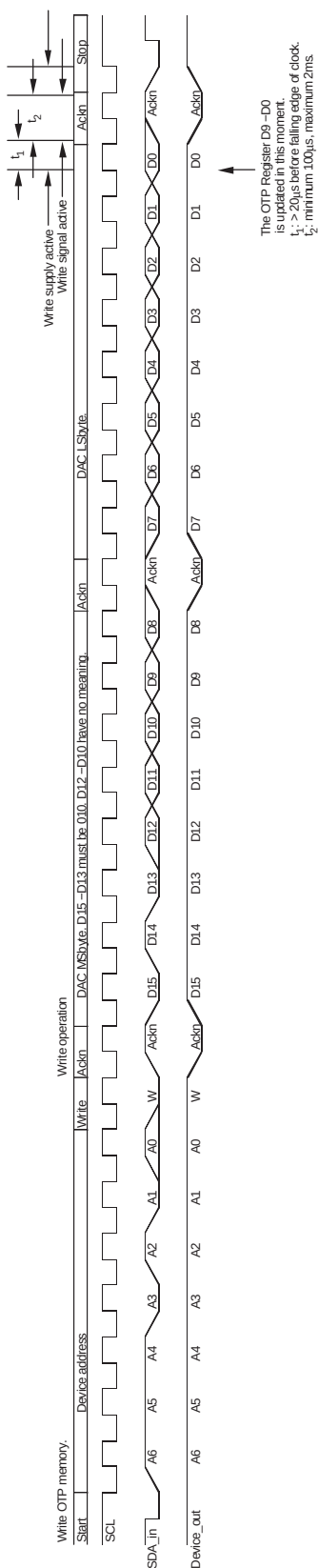


Figure 20. Timing Diagram for Write OTP Register

## V<sub>COM</sub> CALIBRATION

The BUF0190x provides a simple, time- and cost-efficient means to adjust the flicker performance of LCD panels either manually or automatically during the final stages of the LCD panel manufacturing process.

The 10-bit adjustment resolution of the BUF0190x exceeds the typical adjustment resolution of existing V<sub>COM</sub> calibrators significantly. As with a traditional V<sub>COM</sub> adjustment, which uses a mechanical potentiometer and a voltage divider for adjustment (see Figure 21), the BUF0190x uses an external voltage divider that is used to set the initial V<sub>COM</sub> voltage as well as the adjustment range.

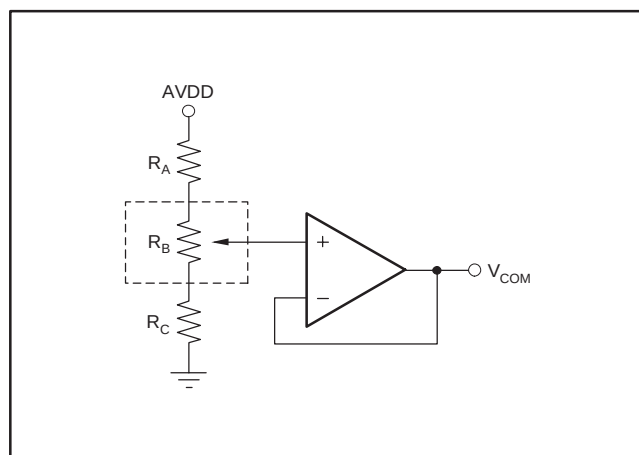


Figure 21. Traditional V<sub>COM</sub> Adjustment

As Figure 22 shows, the 10-bit DAC acts as a Rail-to-Rail output voltage source with a nominal 250kΩ of output impedance. For example, at Code 000h, the lowest V<sub>COM</sub> voltage is achieved since the 250kΩ impedance is now in parallel with R<sub>2</sub>, which lowers the impedance of the lower side of the voltage divider. Consequently, code 3FFh results in the highest adjustable V<sub>COM</sub> voltage.

Once the desired output level is obtained, the part can store the final setting using the non-volatile on-chip memory. See *Programming* section for detailed information.

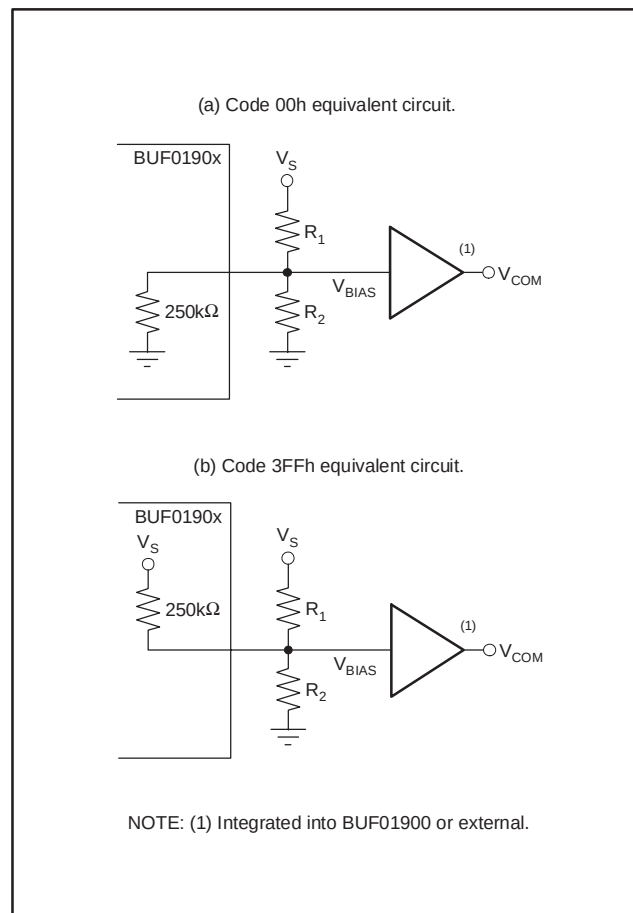


Figure 22. Simplified Block Diagram for V<sub>COM</sub> Adjustment using BUF0190x

## SELECTING THE ADJUSTMENT STEP SIZE

A maximum of 1024 adjustment steps can be realized with the BUF0190x, leading to very high adjustment resolution and very small step sizes. This flexibility can be advantageous during the panel development phase. In a practical production setting, however, this capability might lead to adjustment times that can be too long. A simple solution is to increase the step size between settings to more practical values for mass production. Limiting the number of adjustment steps between code 000h and code 3FFh to between 16 and 128 has been shown to typically yield acceptable adjustment results in the smallest amount of adjustment time.

## EXTERNAL VOLTAGE DIVIDER RESISTOR SELECTION

The external resistive voltage-divider consisting of  $R_1$  and  $R_2$  (see Figure 16, Figure 17, and Figure 18) sets both the maximum value of the  $V_{COM}$  adjustment range and the initial  $V_{COM}$  voltage. Follow the steps below to calculate the correct values for  $R_1$  and  $R_2$ .

**Step 1:** Choose the supply voltage, ( $V_S$ )

**Step 2:** Set the nominal  $V_{COM}$  voltage. This voltage is the  $V_{COM}$  voltage at which the unadjusted panel should be at power-on. The default power-up DAC code is midscale.

**Step 3:** Choose the  $V_{COM}$  adjustment range. The adjustment range is the difference between the lowest and the highest desired  $V_{COM}$  voltage. If the default power-up code is not overwritten by software at the beginning of the adjustment cycle, the adjustment range is symmetrical around the chosen nominal  $V_{COM}$  voltage.

**Step 4:** Calculate the resistors based on the following formulas or simply download the Microsoft Excel™ calculator located in the product folder of BUF0190x available at www.ti.com.

$$R_1 = \frac{250k\Omega \cdot Adj\_range}{V_{COM} - 0.5 \cdot (Adj\_range)} \quad (1)$$

$$R_2 = \frac{1}{\frac{V_S}{V_{COM}} \left( \frac{1}{R_1} + \frac{1}{500k\Omega} \right) - \frac{1}{R_1} - \frac{1}{250k\Omega}} \quad (2)$$

## CALCULATING THE $V_{COM}$ OUTPUT VOLTAGE

With  $R_1$  and  $R_2$  properly set,  $V_{BIAS}$  or  $V_{COM}$  output voltage can be calculated for any digital code with the following formula:

$$V_{COM} = \frac{250k\Omega \cdot R_2 \cdot V_S + R_1 \cdot R_2 \cdot V_S (Code/1023)}{R_1 \cdot R_2 + 250k\Omega \cdot (R_1 + R_2)} \quad (3)$$

## CALCULATING THE ADJUSTMENT RESOLUTION

The resolution of the adjustment is a function of the step size. The resolution can be calculated by simply dividing the chosen adjustment range by the number of steps:

Resolution = Adj\_range/steps (example: 32 steps between code 0h and code 3FFh)

## DESIGN EXAMPLE

**Step 1:** Supply Voltage is 10V.

**Step 2:** Nominal  $V_{COM}$  is determined to be 4V.

**Step 3:** The desired total adjustment range is 1V. In the case of using the default power-up DAC code (midscale), the adjustment range for the  $V_{COM}$  voltage will be from 3.5V to 4.5V.

**Step 4:** Calculation of  $R_1$  and  $R_2$

$R_1 = 71.4k\Omega \Rightarrow$  choose closest 1% resistor (71.5k $\Omega$ )

$R_2 = 45.5k\Omega \Rightarrow$  choose closest 1% resistor (45.3k $\Omega$ )

**Step 5:** Appropriate number of adjustment steps between code 00h and code 3FFh is determined to be 32. This value leads to a step size of 32 codes between adjustment points, which translates into approximately 31mV voltage difference between steps.

## MOTOR DRIVE CIRCUIT

The BUF01900 can be used to drive small motors directly because of the large output drive capability (> 100mA), as illustrated in Figure 23.

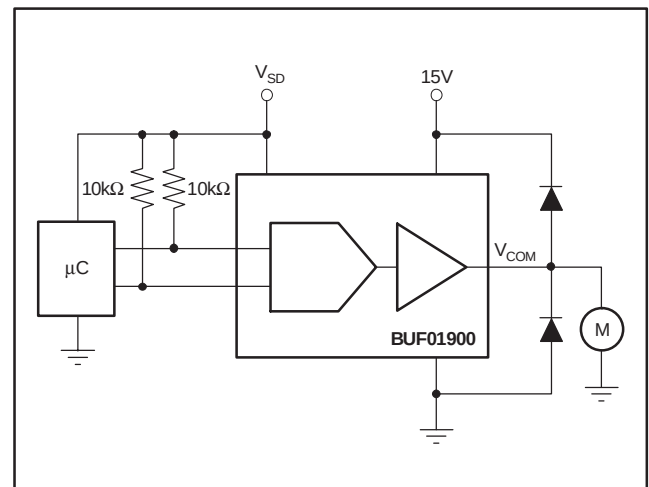


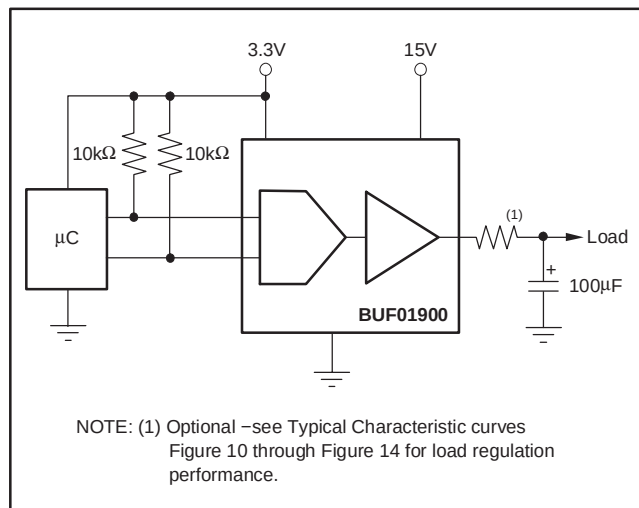
Figure 23. Motor Drive Circuit



## PROGRAMMABLE POWER SUPPLY

The BUF0190x integrated buffer amplifier can drive large capacitive loads (see Typical Characteristics) and greater than 100mA of output current, making it well-suited for programmable power supplies.

Note that the BUF01900 integrated buffer has an input range that only extends to about 0.8V above GND; therefore, the programmable power supply is not able to output voltages less than approximately 0.8V.



**Figure 24. Programmable Power Supply**

## QFN/DFN THERMALLY-ENHANCED PACKAGE

The BUF0190x uses the 10-lead DFN package, a thin, thermally-enhanced package designed to eliminate the use of bulky heat sinks and slugs traditionally used in thermal packages. The DFN package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See QFN/SON PCB Attachment Application Note (SLUA271) available at [www.ti.com](http://www.ti.com).

The thermal resistance junction to ambient ( $R_{\theta JA}$ ) of the DFN package depends on the PCB layout. Using thermal vias and wide PCB traces improves thermal resistance. The thermal pad must be soldered to the PCB. The thermal pad on the bottom of the package should be connected to GND.

Soldering the exposed thermal pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.



## PACKAGING INFORMATION

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C)          | Part marking<br>(6) |
|-----------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|-----------------------|---------------------|
| BUF01900AIDRCR        | NRND          | Production           | VSON (DRC)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -                     | BOO                 |
| BUF01900AIDRCR.A      | NRND          | Production           | VSON (DRC)   10 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | See<br>BUF01900AIDRCR | BOO                 |
| BUF01900AIDRCT        | NRND          | Production           | VSON (DRC)   10 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -                     | BOO                 |
| BUF01900AIDRCT.A      | NRND          | Production           | VSON (DRC)   10 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | See BUF01900AIDRCT    | BOO                 |
| BUF01900AIPW          | NRND          | Production           | TSSOP (PW)   8  | 150   TUBE            | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -                     | F01900              |
| BUF01900AIPW.A        | NRND          | Production           | TSSOP (PW)   8  | 150   TUBE            | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | See BUF01900AIPW      | F01900              |
| BUF01900AIPWR         | NRND          | Production           | TSSOP (PW)   8  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -                     | F01900              |
| BUF01900AIPWR.A       | NRND          | Production           | TSSOP (PW)   8  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | See BUF01900AIPWR     | F01900              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

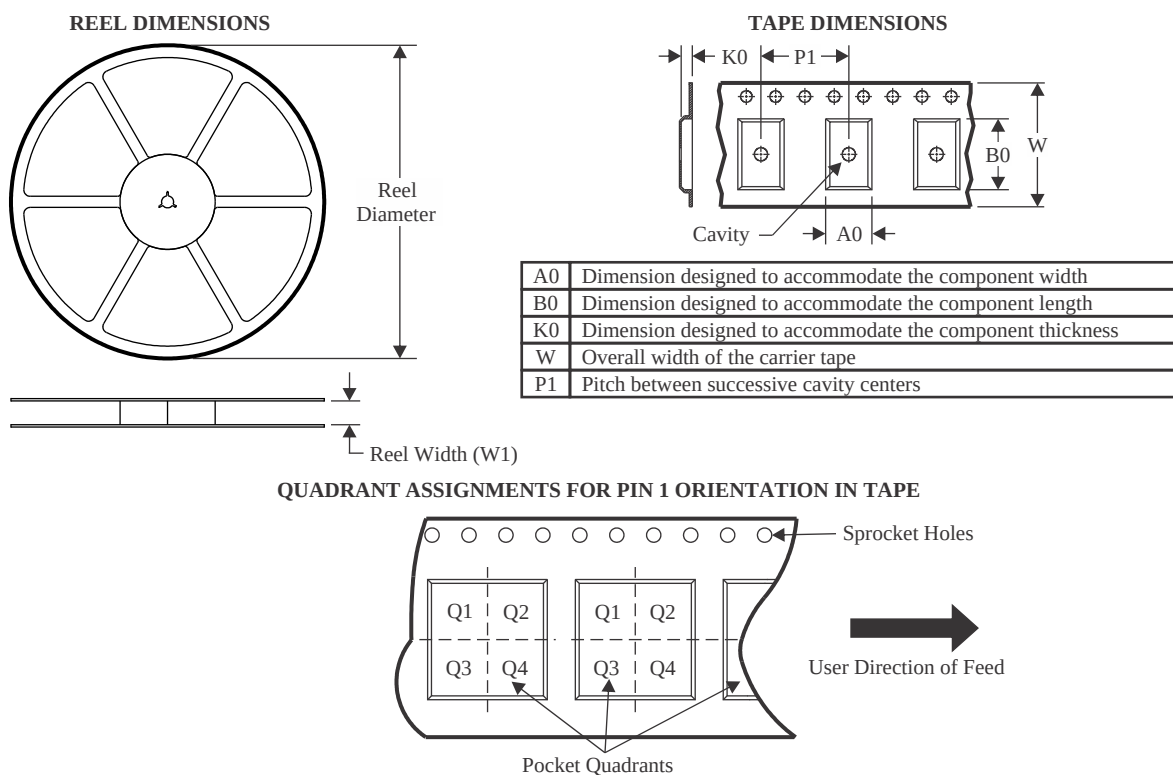
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

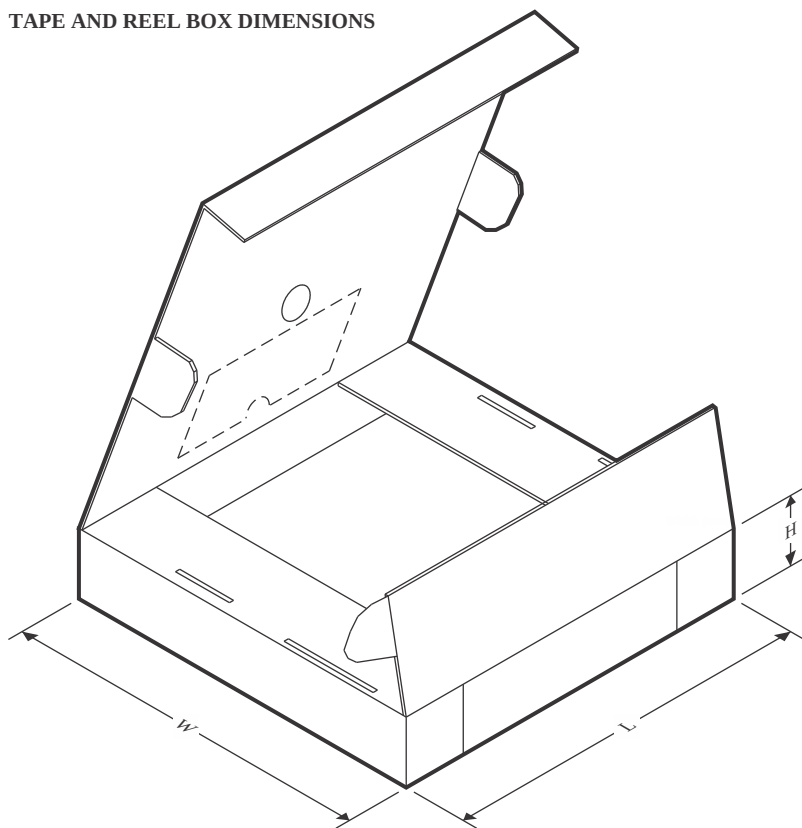
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BUF01900AIDRCR | VSON         | DRC             | 10   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| BUF01900AIDRCT | VSON         | DRC             | 10   | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| BUF01900AIPWR  | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |

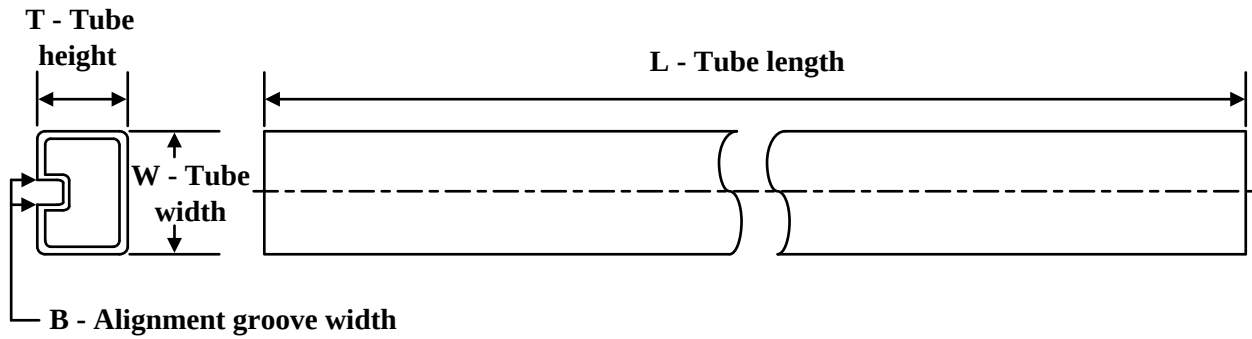
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BUF01900AIDRCR | VSON         | DRC             | 10   | 3000 | 353.0       | 353.0      | 32.0        |
| BUF01900AIDRCT | VSON         | DRC             | 10   | 250  | 213.0       | 191.0      | 35.0        |
| BUF01900AIPWR  | TSSOP        | PW              | 8    | 2000 | 353.0       | 353.0      | 32.0        |

## TUBE



\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| BUF01900AIPW   | PW           | TSSOP        | 8    | 150 | 530    | 10.2   | 3600   | 3.5    |
| BUF01900AIPW.A | PW           | TSSOP        | 8    | 150 | 530    | 10.2   | 3600   | 3.5    |

## GENERIC PACKAGE VIEW

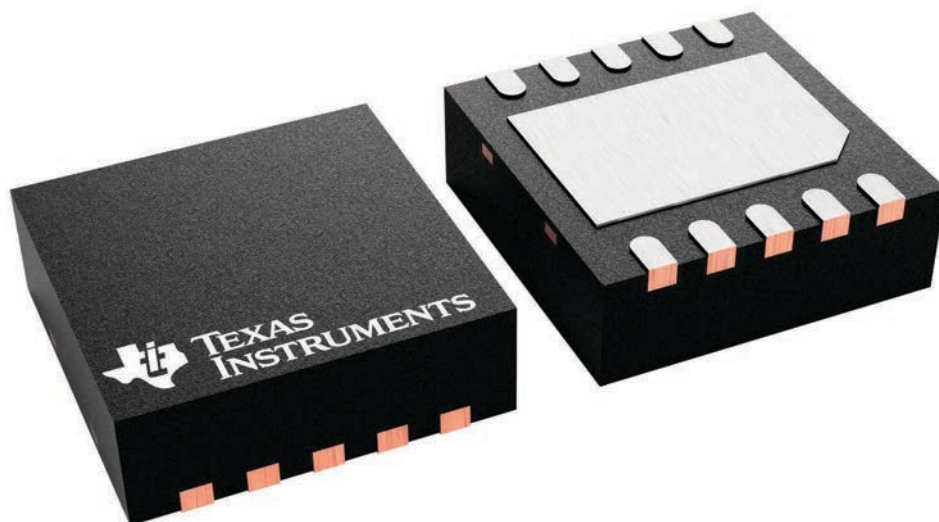
**DRC 10**

**VSON - 1 mm max height**

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



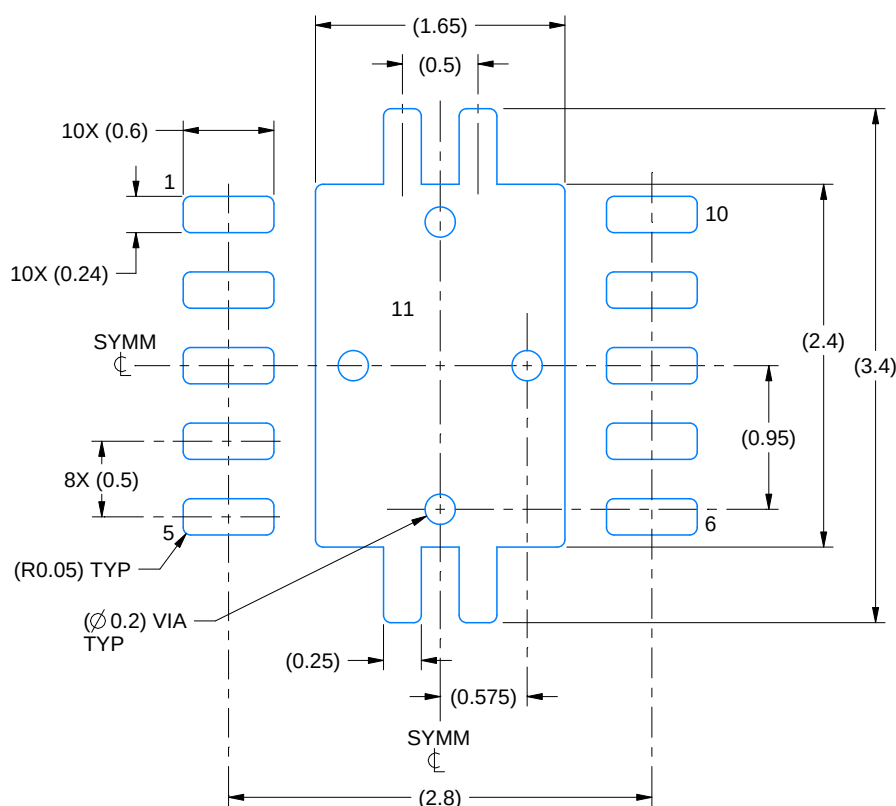


# EXAMPLE BOARD LAYOUT

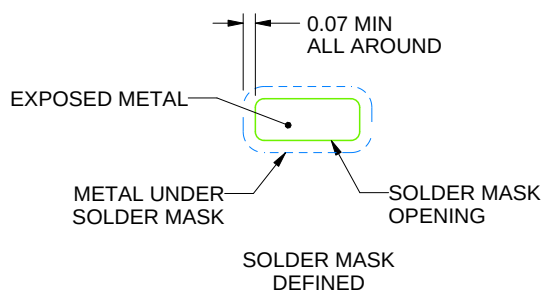
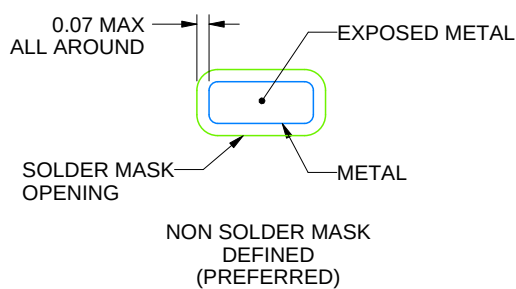
DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:20X



**SOLDER MASK DETAILS**

4218878/B 07/2018

NOTES: (continued)

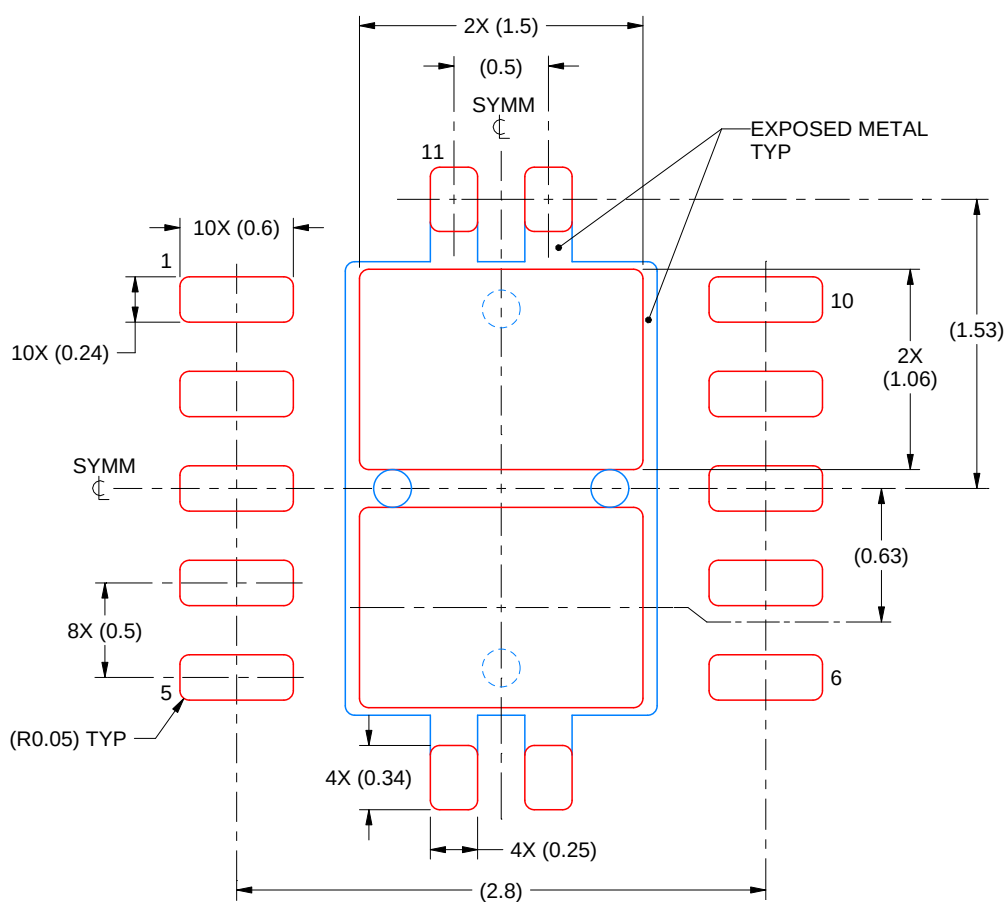
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



**DRC0010J**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

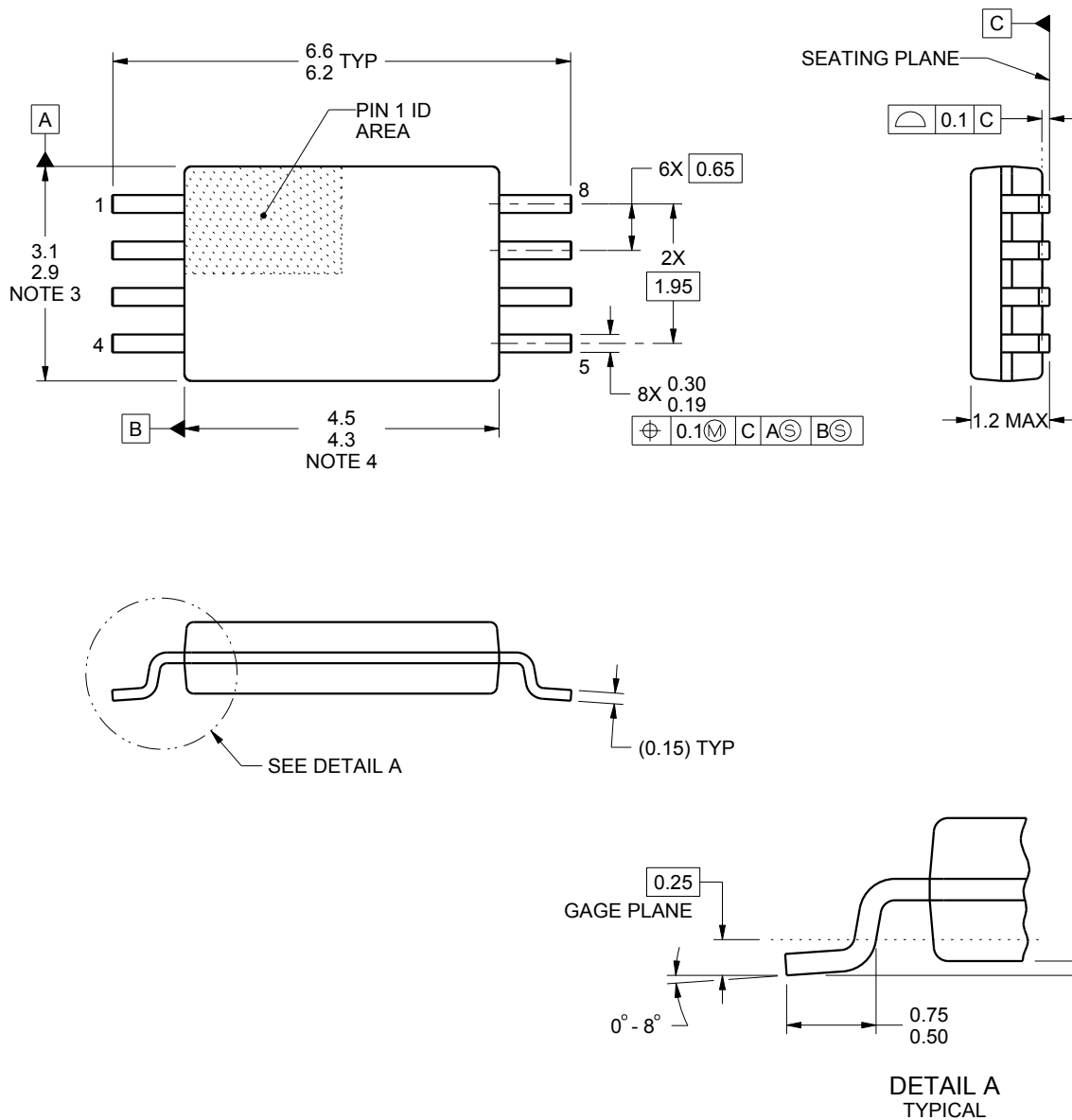
PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

### NOTES:

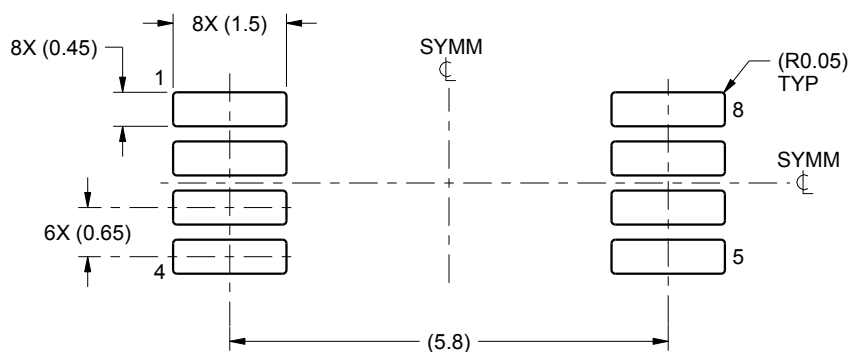
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

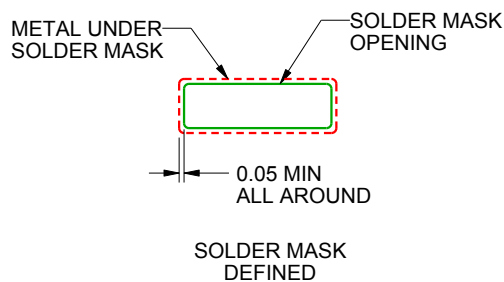
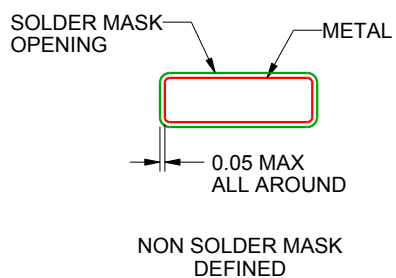
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

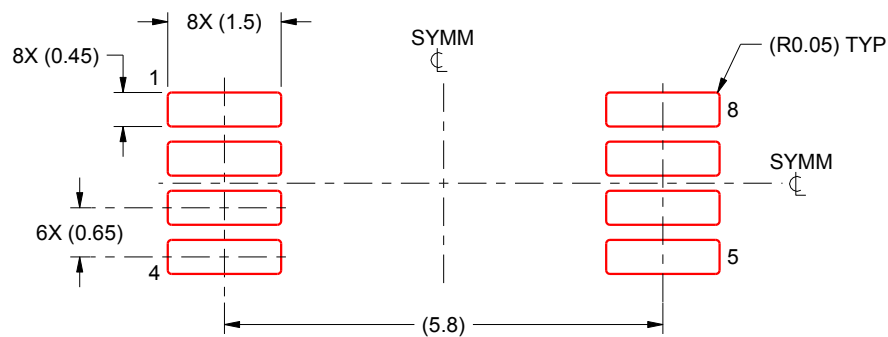
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025