BQ25883 2-Cell, 2-A Boost-Mode Battery Charger With Power Path, USB On-The-Go Boost (OTG) For USB Input

1 Features

- High-efficiency 2-A, 1.5MHz switch mode boost charger
  - 93.4% Charge efficiency at 5V adapter, 7.6-V battery, 1-A charge
  - Optimized for USB input and 2-cell Li-Ion battery
  - Selectable low power PFM mode for light load operation
- Single input to support USB input adapters
  - Supports 3.9 V – 6.2 V input voltage range with 20-V absolute maximum input voltage rating
  - Input current limit (500 mA to 3.3 A with 100-mA resolution) to support USB2.0, USB3.0 standard adapters
  - Maximum power tracking by input voltage limit up-to 5.5 V
  - Integrated USB D+/D- auto-detect USB SDP, CDP, DCP, and non-standard adapters
- Power path management and I^2C control
  - Highest battery discharge efficiency with 17mΩ battery discharge MOSFET
  - Narrow VDC (NVDC) power path management
    - Instant-on system on with no battery or deeply discharged battery
    - Ideal diode operation in battery supplement mode
- USB on-the-go (OTG) with adjustable output from 4.5V to 5.5V
  - Buck converter with up-to 2 A output
  - 94% Efficiency at 5 V, 1 A output
  - Accurate constant current (CC) regulation and output short protection
  - Selectable low power PFM mode for light load operation with out-of-audio option
- Input current optimizer (ICO) to maximize input power without overloading adapters
- Integrated 16-bit ADC for system monitoring (BUS voltage and current, each cell voltage, charge current, SYS voltage, and NTC and die temperature)
- High integration includes all MOSFETs, current sensing and loop compensation
- High accuracy
  - ±0.5% Charge voltage regulation
  - ±5% Charge current regulation
  - ±7.5% Input current regulation
- Safety
  - Battery temperature sensing in charge and OTG buck mode
  - Thermal regulation and thermal shutdown

2 Applications

- Bluetooth speaker
- EPOS Printer
- Portable POS
- Wireless security camera

3 Description

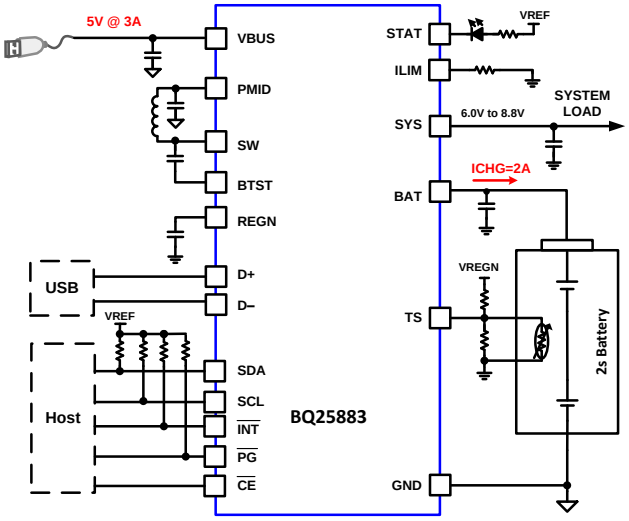
The BQ25883 is a highly-integrated 2-A boost switch-mode battery charge management and system power path management device for 2-cell (2s) Li-Ion and Li-polymer battery. The BQ25883 has I^2C control with OTG and power path.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
BQ25883	VQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (February 2019) to Revision A	Page
• Changed from Advance Information to Production Data	1

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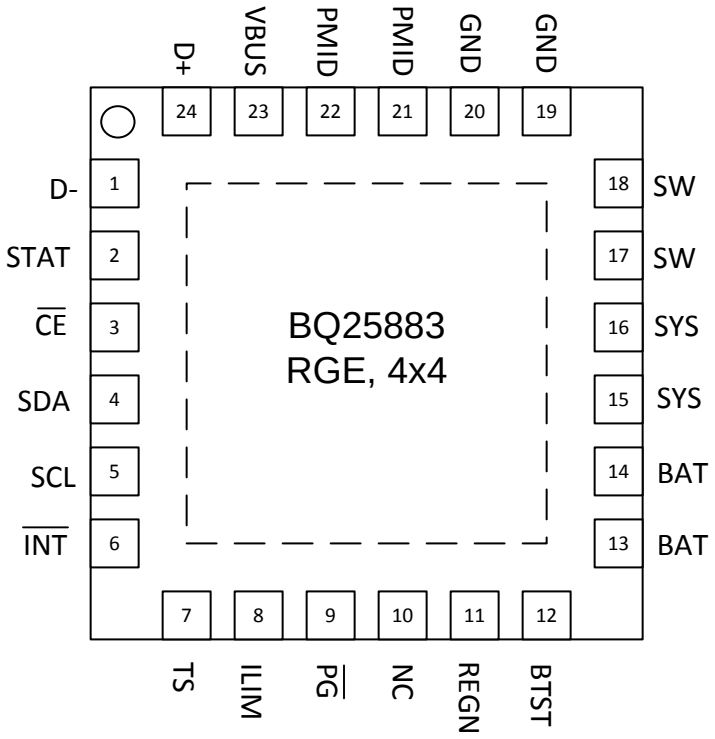
5 Device Comparison Table

Table 1. Device Comparison

PART NUMBER	BQ25882	BQ25883	BQ25886	BQ25887
VBUS Operating Range	3.9 to 6.2 V	3.9 to 6.2 V	4.3 to 6.2 V	3.9 to 6.2 V
USB Detection	D+/D-	D+/D-	D+/D-	PSEL
Power Path	Yes	Yes	Yes	No
Cell Balancing	No	No	No	Yes
OTG	Up to 2 A	Up to 2 A	Up to 2 A	No OTG
16 bit ADC	Yes	Yes	No	Yes
Control Interface	I2C	I2C	Standalone	I2C
Status Pin	/PG	STAT, /PG	STAT, /PG	STAT, /PG
Package	2.1x2.1 WCSP-25	4x4 QFN-24	4x4 QFN-24	4x4 QFN-24

6 Pin Configuration and Functions

RGE Package
24-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
D+	24	AIO	**Positive USB data line –** D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD) and secondary detection in BC1.2.
D–	1	AIO	**Negative USB data line –** D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD) and secondary detection in BC1.2.
STAT	2	DO	**Open drain charge status indicator –** Connect to the pull-up rail via 10-kΩ resistor. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault occurs, the STAT pin blinks at 1Hz. The STAT function can be disabled when the STAT_DIS bit is set.
$\overline{CE}$	3	DI	**Active Low Charge Enable Pin –** Battery charging is enabled when EN_CHG bit is 1 and $\overline{CE}$ pin is LOW. $\overline{CE}$ pin is internally pulled low with 900k-Ω resistor.
SDA	4	DIO	**I2C Interface Data –** Connect SDA to the pull up rail through a 10-kΩ resistor.
SCL	5	DI	**I2C Interface Clock –** Connect SCL to the pull up rail through a 10-kΩ resistor.
$\overline{INT}$	6	DO	**Open drain active Interrupt Output –** Connect $\overline{INT}$ to the pull up rail via a 10-kΩ resistor. The $\overline{INT}$ pin sends active low, 256-µs pulse to the host to report charger device status and fault.
TS	7	AI	**Temperature Qualification Voltage –** Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range. Recommend 103AT-2 thermistor.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
ILIM	8	AI	**Input Current Limit (IINDPM) –** ILIM pin sets the maximum input current and can be used to monitor input current. IINDPM loop regulates ILIM pin voltage at 0.8V. When ILIM pin is less than 0.8V, the input current can be calculated by IIN = KILIM x VILIM / (RILIM x 0.8V). A resistor connected from ILIM pin to ground sets the input current limit as maximum (IINMAX = KILIM / RILIM). When ILIM pin is short to GND, the input current limit is set to maximum by ILIM. The actual input current limit is the lower limit set by ILIM pin (when EN_ILIM bit is HIGH) or IINDPM register bits. Input current limit less than 500mA is not supported on ILIM pin. The ILIM pin function can be disabled when EN_ILIM bit is 0. If ILIM pin is not used, pull this pin to GND.Do not float this pin.
$\overline{PG}$	9	DO	**Open drain active low power good indicator –** Connect to the pull up rail via 10-kΩ resistor. LOW indicates a good input source if the input voltage is within VVBUS_OP (3.9 V), and can provide more than IPOORSRC (30 mA).
REGN	11	P	**Gate Drive Supply –** Bias supply for internal MOSFETs driver and IC. Bypass REGN to GND with a 4.7-µF ceramic capacitor. REGN current limit is 50 mA.
BTST	12	P	**PWM High-side Driver Supply –** Internally, BTST is connected to the cathode of the boot-strap diode. Connect a 47nF bootstrap capacitor from SW to BTST.
BAT	13, 14	P	**Battery Power Connection –** Connect minimum recommended 10-µF capacitance after derating closely to the BAT pin and GND.
SYS	15, 16	P	**System Connection –** The internal BATFET is connected between SYS and BAT. When the battery falls below the minimum system voltage, the switch-mode converter keeps SYS above the minimum system voltage. Connect a 2x22-µF capacitance after derating closely to the SYS pin and PGND.
SW	17, 18	P	**Inductor Connection –** Connect to the switched side of the external inductor.
GND	19, 20,	–	**Ground Return**
PMID	21, 22	P	**Blocking MOSFET Connection –** The minimum recommended total input low-ESR capacitance on VBUS and PMID, after applied derating, is 10 uF. At least 1-uF is recommended at VBUS with the remainder at PMID. Typical value for PMID is 10 uF.
VBUS	23	P	**Input Supply –** VBUS is connected to the external DC supply. Bypass VBUS to GND with at least 1-µF ceramic capacitor, placed as close to the IC as possible.
NC	10	–	**No Connect –** Leave these pins floating or tie to ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage Range (with respect to GND unless otherwise specified)	VBUS (converter not switching)	-0.3	20	V
	PMID (converter not switching)	-0.3	8.5	V
	BAT, SYS (converter not switching)	-0.3	12	V
	SW	-0.3	13	V
	BTST	-0.3	19	V
	REGN, STAT, /PG, TS	-0.3	6	V
	ILIM	-0.3	5	V
	BTST to SW	-0.3	6	V
	D+, D-, /CE, SDA, SCL, /INT	-0.3	6	V
Output Sink Current	/INT, STAT, /PG		6	mA
Junction Temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I_{VBUS}	Average input current (VBUS)			3.3	A
I_{BAT}	Average charge current (IBAT)			2.2	A
I_{BAT_RMS}	RMS discharging current with internal MOSFET			5	A
I_{BAT_PK}	Peak discharging current with internal MOSFET			9 (up to 1us)	A
V_{BAT}	Battery Voltage			9.2 (1)	V
T_A	Operating free-air temperature range	-40		85	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on SW pin. A tight layout minimizes switching noise.

7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC (1)		BQ25883 RGE (VQFN) 24-PIN	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	32.4	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	26.7	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	10.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

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Thermal Information (continued)

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC[1]		BQ25883 RGE (VQFN) 24-PIN	UNIT
$R_{\Theta\ JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	°C/W

7.5 Electrical Characteristics

$V_{VBUS_UVLO_RISING}$< V_{VBUS} < V_{VBUS_OV}, T_J = -40°C to+125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT)	VBAT = 9 V, No VBUS, SCL, SDA = 0 V or 1.8 V, T_J=25C, ADC Disabled		12	14	µA
		VBAT = 9 V, No VBUS, SCL, SDA = 0 V or 1.8 V, T_J < 85C, ADC Disabled		12	20	µA
I_{VBUS_HIZ}	Input supply current (VBUS) in HIZ	VBUS = 5 V, High-Z Mode, no battery, ADC Disabled, 25℃		30	38	µA
		VBUS = 5 V, High-Z Mode, no battery, ADC Disabled, <85℃		30	48	µA
I_{VBUS}	Input supply current (VBUS)	VBUS = 5 V, V_{BAT} = 7.6 V, converter not switching		1.5	3	mA
		VBUS = 5 V, V_{BAT} = 7.6 V, converter switching, I_{SYS} = 0A		3		mA
I_{BAT_OTG}	Battery discharge current in OTG mode	VBAT = 8.4 V, OTG Buck Mode, I_{VBUS} = 0A, converter switching		3		mA
VBUS/VBAT POWER UP						
V_{VBUS_OP}	VBUS operating range		3.9		6.2	V
$V_{VBUS_UVLO_RISING}$	VBUS rising for active I2C, no battery	VBUS rising		3.3	3.68	V
V_{VBUS_OV}	VBUS over-voltage rising threshold	VBUS rising	6.2		6.6	V
	VBUS over-voltage falling threshold	VBUS falling	5.9		6.4	V
$V_{BAT_UVLO_RISING}$	Battery for active I2C	VBAT rising	3.7	4	4.42	V
$V_{POORSRC_FALLING}$	Bad adapter detection threshold	VBUS falling below $V_{POORSRC_FALLING}$		3.7		V
$I_{POORSRC}$	Bad adapter detection current source			15		mA
POWER-PATH						
V_{SYS}	Typical System Regulation Voltage	ISYS = 0A, VBAT = 8.80 V > SYS_MIN[3:0], Charge Disabled (EN_CHG = 0)		V_{BAT}+0.1		V
		ISYS = 0A, VBAT < SYS_MIN[3:0], Charge Disabled (EN_CHG = 0)		VSYS_MIN+0.2		V
V_{SYS_MIN}	System Regulation Voltage	VBAT < SYS_MIN[3:0] = 0010, Charge Disabled (EN_CHG = 0)	6.2	6.4		V
BATTERY CHARGER						
V_{REG_RANGE}	Typical charge voltage regulation range		6.8		9.2	V
V_{REG_STEP}	Typical charge voltage step			10		mV
V_{REG_ACC}	Charge voltage	VREG = 8.40 V, T_J = 0°C to 85°C,	8.35	8.4	8.44	V
I_{CHG_RANGE}	Charge current regulation range		100		2200	mA
I_{CHG_STEP}	Charge current regulation step			50		mA
I_{CHG_ACC}	Fast Charge current regulation accuracy	ICHG = 1000 mA, VBAT = 6.2 V or 7.6 V, T_J = 0°C to 85°C	-7.5		7.5	%
I_{CHG_ACC}	Fast Charge current regulation accuracy	ICHG = 500mA, VBAT = 6.2 V or 7.6 V, T_J = 0°C to 85°C	-15		15	%

Electrical Characteristics (continued)

$V_{VBUS_UVLO_RISING}$< V_{VBUS} < V_{VBUS_OV}, T_J = -40°C to+125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CHG_ACC}	Fast Charge current regulation accuracy	ICHG = 250 mA, VBAT = 6.2 V or 7.6 V, T_J = 0°C to 85°C	-25		25	%
I_{PRECHG_RANGE}	Precharge current range		50		800	mA
I_{PRECHG_STEP}	Typical precharge current step			50		mA
I_{PRECHG_ACC}	Precharge current accuracy	VBAT = 5.2 V, IPRECHG = 200 mA, T_J = 25°C	170		237	mA
		VBAT = 5.2 V, IPRECHG = 200 mA, T_J = 0°C to 85°C	150		245	mA
I_{TERM_RANGE}	Termination current range		50		800	mA
I_{TERM_STEP}	Typical termination current step			50		mA
I_{TERM_ACC}	Termination current accuracy	ICHG = 1.5A, ITERM = 150 mA, T_J = 25°C	143		157	mA
		ICHG = 1.5A, ITERM = 150 mA, T_J = 0°C to 85°C	120		180	mA
		ICHG = 1.5A, ITERM = 50 mA, T_J = 25°C	45		60	mA
		ICHG = 1.5A, ITERM = 50 mA, T_J = 0°C to 85°C	22		75	mA
$V_{BAT_SHORT_RISING}$	Short Battery Voltage rising threshold to start pre-charging	VBAT rising	4.1	4.4	4.7	V
$V_{BAT_SHORT_FALLING}$	Short Battery Voltage falling threshold to stop pre-charging	VBAT falling	3.7	4	4.3	V
I_{BAT_SHORT}	Low Battery Voltage trickle charging current	VBAT < 4.4 V		100		mA
$V_{BAT_LOWV_RISING}$	VBAT LOWV Rising threshold to start fast-charging	VBAT rising, VBATLOWV = 6.0 V	5.7	6	6.3	V
		VBAT rising, VBATLOW = 5.6 V	5.3	5.6	5.9	V
$V_{BAT_LOWV_FALLING}$	VBAT LOWV Falling threshold to stop fast-charging	VBAT falling, VBATLOW = 5.6 V	4.9	5.2	5.5	V
		VBAT falling, VBATLOWV = 6.0 V	5.3	5.6	5.9	V
V_{RECHG}	Recharge threshold below V_{REG}	VBAT falling, VRECHG[1:0] = 01		200		mV
		VBAT falling, VRECHG[1:0] = 10		300		mV
R_{ON_QHS} (Q2)	High-side switching MOSFET on-resistance between SW and SYS (Q2)	T_J = 25°C		32	34.2	mΩ
		T_J = – 40°C to 125°C		32	46.5	mΩ
R_{ON_QLS} (Q3)	Low-side switching MOSFET on-resistance between SW and GND (Q3)	T_J = 25°C		42	45.8	mΩ
		T_J = – 40°C to 125°C		42	62.9	mΩ
R_{ON_QBAT} (Q4)	MOSFET on-resistance between SYS and BAT (Q4)	T_J = 25°C		18	18.8	mΩ
		T_J = – 40°C - 85°C		18	22.5	mΩ
I_{BAT_DISCHG}	BAT Discharge current source	VBAT = 8V, EN_BAT_DISCHG = 1	8	11.5	16	mA
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_RANGE}	Input voltage regulation range		3.9		5.5	V
V_{INDPM_STEP}	Input voltage regulation step			100		mV
V_{INDPM}	Input voltage limit	VINDPM = 3.9 V	3.783	3.9	4.017	V
		VINDPM = 4.4 V	4.268	4.4	4.532	V
I_{INDPM_RANGE}	Input current regulation range		500		3300	mA
I_{INDPM_STEP}	Input current regulation step			100		mA
I_{INDPM_ACC}	Input current regulation limit	IINDPM = 500 mA	438	469	500	mA
		IINDPM = 900 mA	765	832	900	mA
		IINDPM = 2500 mA	2125	2312	2500	mA
		IINDPM = 3000 mA	2550	2775	3000	mA
K_{ILIM}	I_{INMAX} = K_{ILIM}/R_{ILIM}	Input Current regulation by ILIM pin = 1.5A	1012	1098	1185	A x Ω

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Electrical Characteristics (continued)

$V_{VBUS_UVLO_RISING} < V_{VBUS} < V_{VBUS_OV}$, T_J = -40°C to+125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ON_QBLK} (Q1)	Blocking MOSFET on-resistance between VBUS and PMID (QBLK)	T_J = 25°C		33	36.8	mΩ
		T_J = – 40°C to 125°C		33	50.9	mΩ
D + /D- DETECTION						
$V_{D+D-_600MVSRC}$	D+/D- Voltage Source (600 mV)		500	600	700	mV
$I_{D+_10UASRC}$	D+ Current Source (10 µA)	VD + = 200 mV,	7	10	14	µA
$I_{D+D-_100UASNK}$	D+/D- Current Sink (100 µA)	VD + = 500 mV,	50	100	150	µA
V_{D+D-_0P325}	D+/D- Comparator Threshold for Secondary Detection	D + pin Rising	250		400	mV
R_{D-_19K}	D- Resistor to Ground (19 kΩ)	VD- = 500 mV,	14.25		24.8	kΩ
V_{D+_0P8}	D+ Comparator Threshold for Data Contact Detection	D + pin Rising			800	mV
V_{D+D-_1P2}	D+/D- Threshold for Non-standard adapter		1.05		1.35	V
V_{D+D-_2P0}	D+/D- Comparator Threshold for Non-standard adapter		1.85		2.15	V
V_{D+D-_2P8}	D+/D- Threshold for Non-standard adapter		2.55		2.85	V
I_{D+D-_LKG}	D+/D- Leakage Current	HiZ	-1		1	µA
BATTERY OVER-VOLTAGE PROTECTION						
$V_{BAT_OVP_RISING}$	Battery over-voltage rising threshold	VBAT rising, as percentage of VREG	102.5	104	105	%
$V_{BAT_OVP_FALLING}$	Battery over-voltage falling threshold	VBAT falling, as percentage of VREG	101	102	103.3	%
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	TREG = 120°C		120		°C
T_{SHUT_RISING}	Thermal Shutdown Rising threshold	Temperature Increasing		150		°C
	Thermal Shutdown Falling threshold	Temperature Decreasing		120		°C
JEITA THERMISTOR COMPARATOR (BOOST MODE)						
V_{T1}	TS pin voltage rising. T1 (0°C) threshold, Charge suspended below this temperature.	As Percentage to REGN	72.75	73.25	73.75	%
V_{T1_HYS}	TS pin voltage falling. Charge re-enabled to ICHG/2 and VREG above this temperature	As Percentage to REGN		1.3		%
V_{T2}	TS pin voltage rising. T2 (10°C) threshold, charge set to ICHG/2 and VREG below this temperature	As Percentage to REGN	67.75	68.25	68.75	%
V_{T2_HYS}	TS pin voltage falling. Charge set to ICHG and VREG above this temperature	As Percentage to REGN		1.2		%
V_{T3}	TS pin voltage falling. T3 (45°C) threshold, charge set to ICHG and 8.1 V above this temperature.	As Percentage to REGN	44.25	44.75	45.25	%
V_{T3_HYS}	TS pin voltage rising. Charge set to ICHG and VREG below this temperature	As Percentage to REGN		1		%
V_{T5}	TS pin voltage falling. T5 (60°C) threshold, charge suspended above this temperature.	As Percentage to REGN	33.875	34.375	34.875	%
V_{T5_HYS}	TS pin voltage rising. Charge set to ICHG and 8.1 V below this temperature	As Percentage to REGN		1.35		%
COLD/HOT THERMISTOR COMPARATOR (OTG BUCK MODE)						

Electrical Characteristics (continued)

$V_{VBUS_UVLO_RISING}$< V_{VBUS} < V_{VBUS_OV}, T_J = -40°C to+125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BCOLD0}	Cold Temperature Threshold 0, TS pin Voltage Rising Threshold	As Percentage to REGN, BCOLD = 0 (Approx. – 10°C w/ 103AT)	76.5	77	77.5	%
V_{BCOLD0_HYS}	Cold Temperature Threshold 0, TS pin Voltage Falling Threshold	As Percentage to REGN		1		%
V_{BCOLD1}	Cold Temperature Threshold 1, TS pin Voltage Rising Threshold	As Percentage to REGN, BCOLD = 1 (Approx. – 20°C w/ 103AT)	79.5	80	80.5	%
V_{BCOLD1_HYS}	Cold Temperature Threshold 1, TS pin Voltage Falling Threshold	As Percentage to REGN		1		%
V_{BHOT0}	Hot Temperature Threshold 0, TS pin Voltage Falling Threshold	As Percentage to REGN, BHOT[1:0] = 01 (Approx. 55°C w/ 103AT)	37.25	37.75	38.25	%
V_{BHOT0_HYS}	Hot Temperature Threshold 0, TS pin Voltage Rising Threshold	As Percentage to REGN		3		%
V_{BHOT1}	Hot Temperature Threshold 1, TS pin Voltage falling Threshold	As Percentage to REGN, BHOT[1:0] = 00 (Approx. 60°C w/ 103AT)	33.875	34.375	34.875	%
V_{BHOT1_HYS}	Hot Temperature Threshold 1, TS pin Voltage rising Threshold	As Percentage to REGN		3		%
V_{BHOT2}	Hot Temperature Threshold 2, TS pin Voltage falling Threshold	As Percentage to REGN, BHOT[1:0] = 10 (Approx. 65°C w/ 103AT)	30.75	31.25	31.75	%
V_{BHOT2_HY2}	Hot Temperature Threshold 2, TS pin Voltage rising Threshold	As Percentage to REGN		3		%
BOOST MODE CONVERTER						
F_{SW}	PWM switching frequency	Oscillator frequency	1.35	1.5	1.65	MHz
OTG BUCK MODE CONVERTER						
V_{OTG_BAT}	Battery voltage exiting OTG mode	VBAT falling	5.85	6	6.15	V
V_{OTG_RANGE}	Typical OTG Buck mode voltage regulation range		4.5		5.5	V
V_{OTG_STEP}	Typical OTG Buck mode voltage regulation step			100		mV
V_{OTG_ACC}	OTG Buck mode voltage regulation accuracy	IVBUS = 0A, OTG_VLIM = 5.1 V	-3		3	%
I_{OTG_RANGE}	Typical OTG Buck mode current regulation range		0.5		2	A
I_{OTG_STEP}	Typical OTG Buck mode current regulation step			100		mA
I_{OTG_ACC}	OTG Buck mode current regulation accuracy	OTG_ILIM = 1A	-15	-7.5	0	%
V_{OTG_OVP}	OTG Buck mode over-voltage threshold		5.8	6		V
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5 V, I_{REGN} = 20 mA	4.7	4.8	5.15	V
I_{REGN}	REGN LDO current limit	V_{VBUS} = 5 V, V_{REGN} = 3.8 V	50			mA
Analog-to-Digital Converter (ADC)						
t_{ADC_CONV}	Conversion time, each measurement	ADC_SAMPLE[1:0] = 11		24		ms
		ADC_SAMPLE[1:0] = 10		12		ms
		ADC_SAMPLE[1:0] = 01		6		ms
		ADC_SAMPLE[1:0] = 00		3		ms
ADCRES	Effective resolution	ADC_SAMPLE[1:0] = 11	14	15		bits
		ADC_SAMPLE[1:0] = 10	13	14		bits
		ADC_SAMPLE[1:0] = 01	12	13		bits
		ADC_SAMPLE[1:0] = 00	10	12		bits
ADC MEASUREMENT RANGES AND LSB						

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Electrical Characteristics (continued)

$V_{VBUS_UVLO_RISING}$< V_{VBUS} < V_{VBUS_OV}, T_J = -40°C to+125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{BUS_ADC_RANGE}$	ADC BUS current range		0		4	A
$I_{BUS_ADC_LSB}$	ADC BUS current LSB			1		mA
$I_{BAT_ADC_RANGE}$	ADC BAT current range		0		4	A
$I_{BAT_ADC_LSB}$	ADC BAT current LSB			1		mA
$V_{BUS_ADC_RANGE}$	ADC BUS voltage range		0		6.5	V
$V_{BUS_ADC_LSB}$	ADC BUS voltage LSB			1		mV
$V_{SYS_ADC_RANGE}$	ADC SYS voltage range		0		10	V
$V_{SYS_ADC_LSB}$	ADC SYS voltage LSB			1		mV
$V_{BAT_ADC_RANGE}$	ADC BAT voltage range		0		10	V
$V_{BAT_ADC_LSB}$	ADC BAT voltage LSB			1		mV
$V_{TS_ADC_RANGE}$	ADC TS voltage range		20		80	%
$V_{TS_ADC_LSB}$	ADC TS voltage LSB			0.098		%
$V_{TDIE_ADC_RANGE}$	ADC Die temperature range		0		150	°C
$V_{TDIE_ADC_LSB}$	ADC Die temperature LSB			0.5		°C
I2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level, SDA and SCL	Pull-up rail 1.8 V	1.3			V
V_{IL}	Input low threshold level	Pull-up rail 1.8 V			0.4	V
V_{OL}	Output low threshold level	Sink current = 5 mA			0.4	V
I_{BIAS}	High level leakage current	Pull-up rail 1.8 V			1	uA
LOGIC I/O PIN (/CE)						
V_{IH_CEZ}	Input high threshold level, /CE		1.3			V
V_{IL_CEZ}	Input low threshold level, /CE				0.4	V
$I_{IN_BIAS_CEZ}$	High level leakage current, /CE	Pull-up rail 1.8 V			2.5	uA
LOGIC O PIN (/INT, /PG, STAT)						
V_{OL}	Output low threshold level	Sink current = 5 mA			0.4	V
I_{OUT_BIAS}	High level leakage current	Pull-up rail 1.8 V			1	µA

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
VBUS/BAT POWER UP						
t_{VBUS_OV}	VBUS OVP reaction time	VBUS rising above V_{BUS_OV} threshold to converter turn off		200		ns
$t_{POORSRC}$	Bad adapter detection duration			30		ms
BATTERY CHARGER						
t_{TERM_DGL}	Deglitch time for charge termination	Charge current falling below I_{TERM}		250		ms
t_{RECGH_DGL}	Deglitch time for recharge threshold	BAT voltage falling below VRECHG = 100 mV		250		ms
$t_{BAT_OVP_DGL}$	Deglitch time for battery over-voltage to disable charge			1		µs
t_{TOP_OFF}	Typical Top-Off Timer Accuracy	TOP_OFF_TIMER = 30 min	24	30	36	min
t_{SAFETY}	Charge Safety Timer Accuracy	CHG_TIMER = 12 hours	10.8	12	13.2	hr
I2C INTERFACE						
f_{SCL}	SCL clock frequency				1000	kHZ
t_{SU_STA}	Data set-up time		10			ns
t_{HD_DAT}	Data hold time		0		70	ns
t_{rDA}	Rise time of SDA signal		10		80	ns

Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{fDA}	Fall time of SDA signal		10		80	ns
DIGITAL CLOCK AND WATCHDOG TIMER						
f_{LPDIG}	Digital low power clock	REGN LDO disabled	18	30	45	kHZ
f_{DIG}	Digital clock	REGN LDO enabled	1.35	1.5	1.65	MHz

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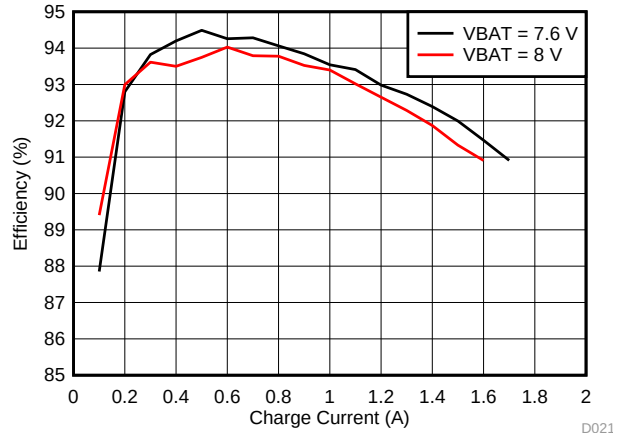
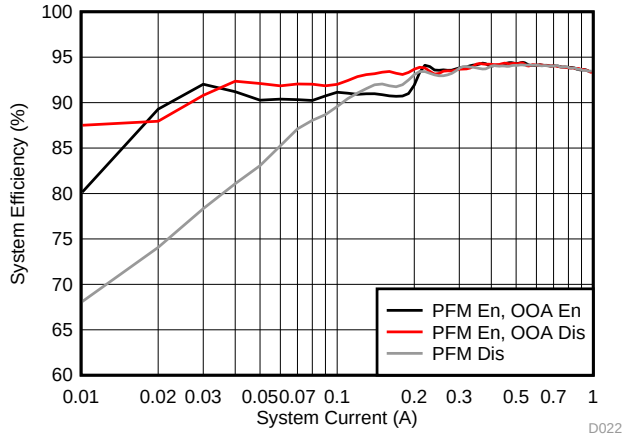
7.7 Typical Characteristics

C_{VBUS} = 1µF, C_{PMID}= 10µF, C_{SYS}= 44µF, C_{BAT} = 10µF, L = 1µH (IHLP2525CZER1R0k01) (unless otherwise specified)



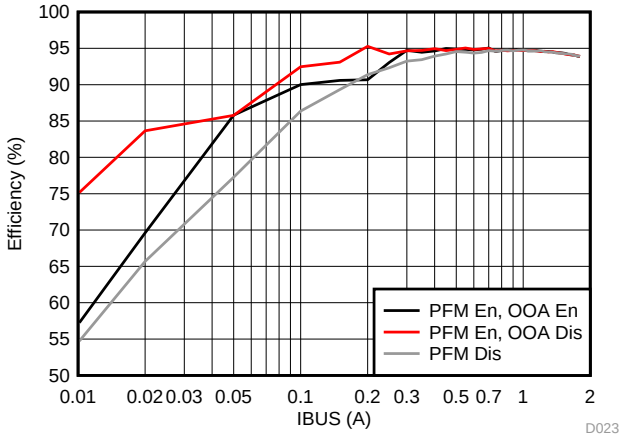
VBUS = 5 V

Figure 1. Charge Efficiency vs Charge Current



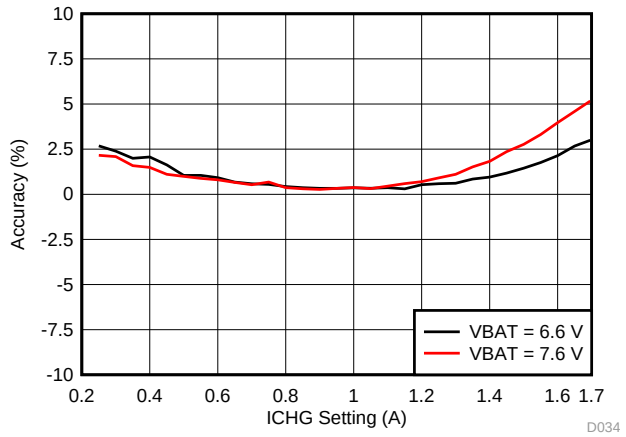
VBUS = 5 V VBAT = 8.4 V

Figure 2. System Efficiency vs System Current



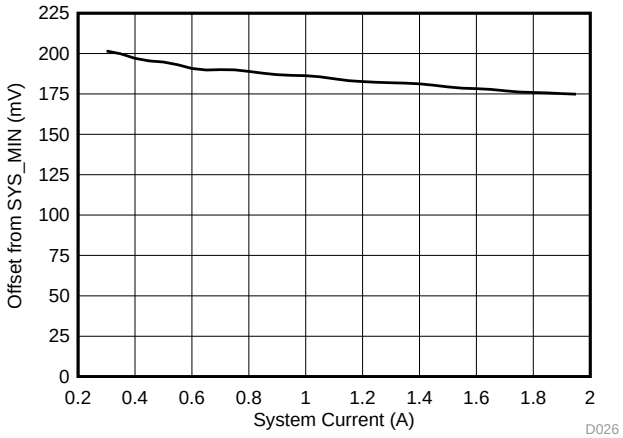
OTG_VLIM = 5 V VBAT = 7.6 V

Figure 3. OTG Efficiency vs VBUS Output Current



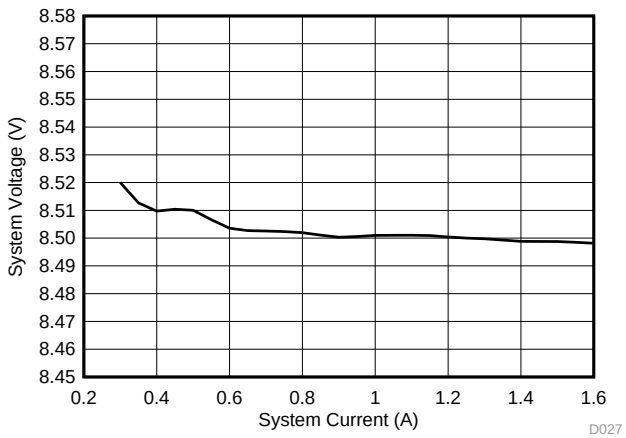
VBUS = 5 V

Figure 4. Charge Current Accuracy vs ICHG Setting



VBUS = 5 V VBAT = 6 V SYS_MIN = 7 V
EN_CHG = 0

Figure 5. SYSMIN Load Regulation

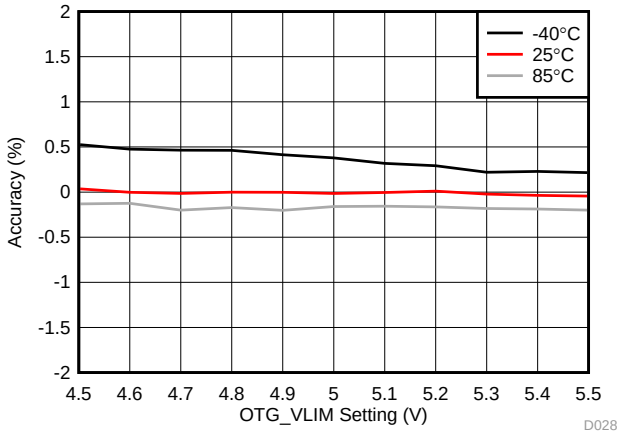


VBUS = 5 V VBAT = 8.4 V EN_CHG = 0

Figure 6. System Load Regulation After Charge Done

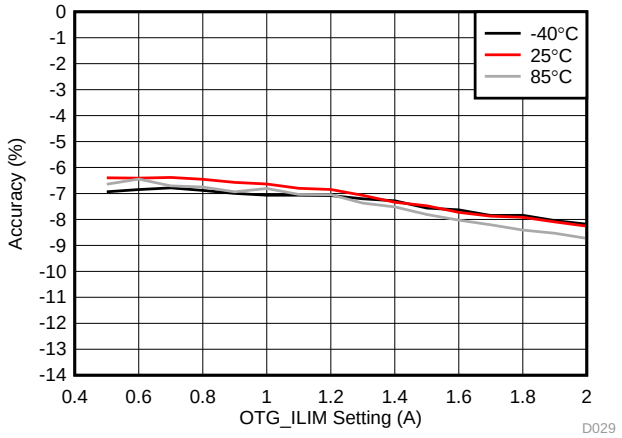
Typical Characteristics (continued)

C_{VBUS} = 1µF, C_{PMID}= 10µF, C_{SYS}= 44µF, C_{BAT} = 10µF, L = 1µH (IHLP2525CZER1R0k01) (unless otherwise specified)



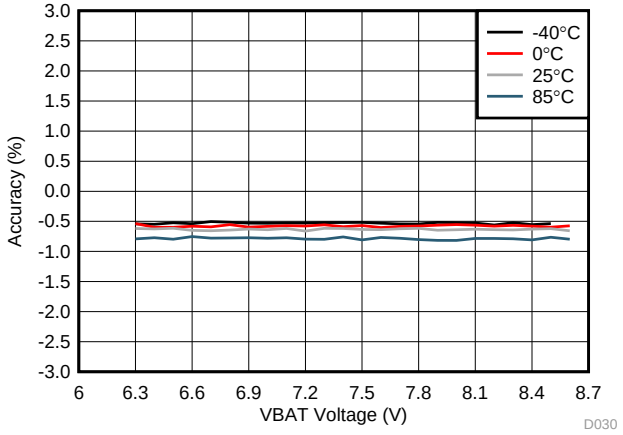
VBAT = 7.6 V

Figure 7. OTG VBUS Regulation vs OTG_VLIM Setting



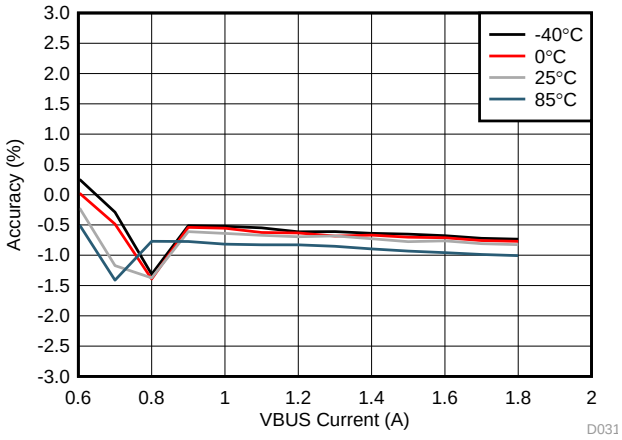
VBAT = 8 V

Figure 8. OTG IBUS Limit vs OTG_ILIM Setting



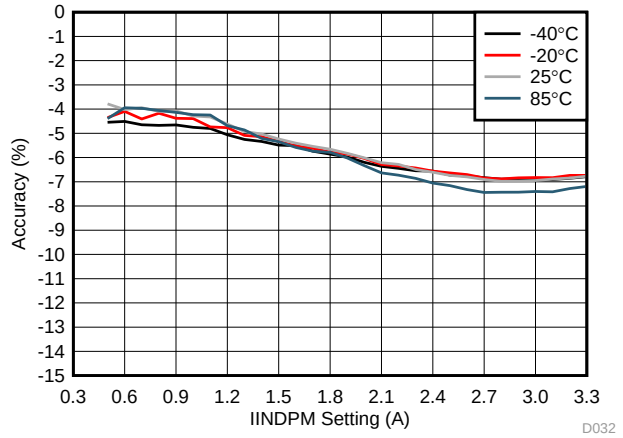
VOTG = 5.1 V

Figure 9. OTG Voltage Regulation vs VBAT Voltage



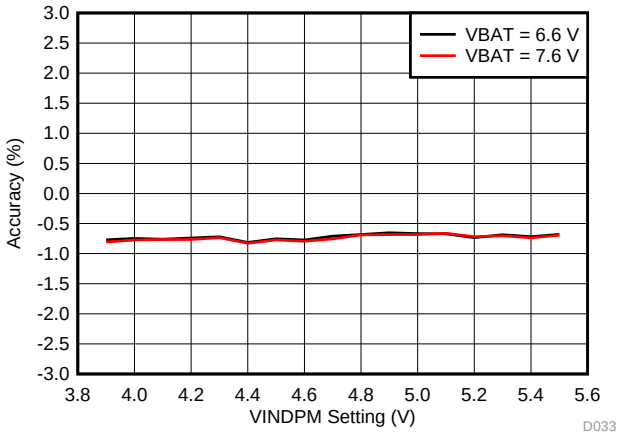
VOTG = 5.1 V VBAT = 8 V

Figure 10. OTG Voltage Regulation vs OTG BUS Current



VBUS = 5 V VBAT = 7.6 V

Figure 11. Input Current Limit Accuracy vs IINDPM Setting



T_A = 25°C

Figure 12. Input Voltage Limit Accuracy vs VINDPM Setting

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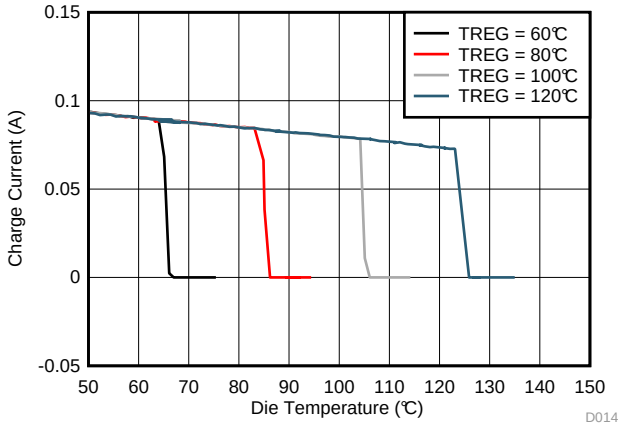
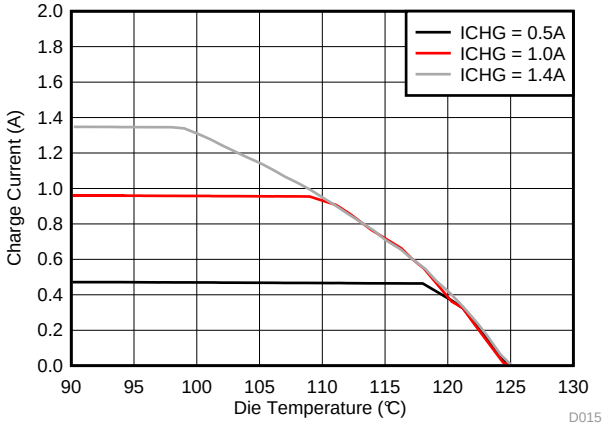
Typical Characteristics (continued)

C_{VBUS} = 1µF, C_{PMID}= 10µF, C_{SYS}= 44µF, C_{BAT} = 10µF, L = 1µH (IHLP2525CZER1R0k01) (unless otherwise specified)



VBUS = 5V VBAT = 7.6V ICHG = 100mA

Figure 13. TREG Profiles



VBUS = 5V VBAT = 7.6V ICHG = 0.5A, 1.0A, 1.4A

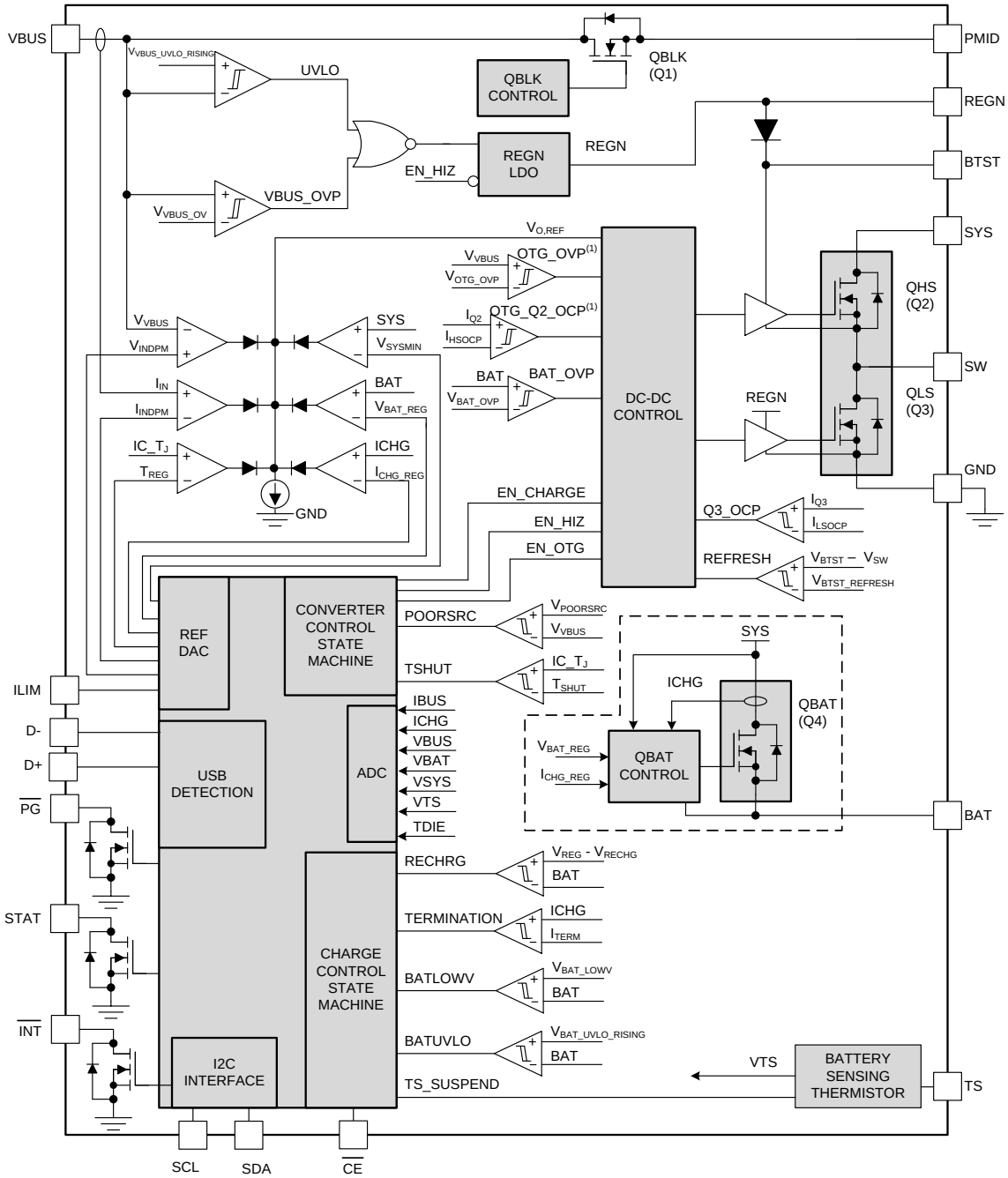
Figure 14. Max Current Temperature Profile

8 Detailed Description

8.1 Overview

The BQ25883 device is a highly integrated 2-A switch-mode battery charger for 2s Li-Ion and Li-Polymer battery. It integrates the input blocking FET (Q1, QBLK), high-side switching FET (Q2, QHS), low-side switching FET (Q3, QLS), and battery FET (Q4, QBAT). The device also integrates the boot-strap diode for high-side gate drive.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Device Power-On-Reset

The internal bias circuits are powered from either VBAT or VBUS when it rises above $V_{VBUS_UVLO_RISING}$ or $V_{BAT_UVLO_RISING}$. When VBUS rises above $V_{VBUS_UVLO_RISING}$ or BAT rises above $V_{BAT_UVLO_RISING}$, the BATFET driver is active. I2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

8.3.2 Device Power Up from Battery without Input Source

If only the battery is present and the voltage is above UVLO threshold ($V_{BAT_UVLO_RISING}$), the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low $R_{DS(ON)}$ of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

8.3.3 Device Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the boost converter is started. The power up sequence from input source is as listed:

1. Poor Source Qualification
2. Input Source Type Detection based on D+/D– to set default Input Current Limit (IINDPM) register and input source type
3. Power Up REGN LDO
4. Converter Power-up

8.3.3.1 Poor Source Qualification

After REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to start the boost converter.

1. VBUS voltage below V_{VBUS_OVP}
2. VBUS voltage above $V_{POORSRC}$ when pulling $I_{POORSRC}$ (typical 30mA)

If V_{BUS_OVP} is detected (condition 1 above), the device automatically retries detection once the over-voltage fault goes away. If a poor source is detected (condition 2 above), the device repeats poor source qualification routine every 2 seconds. After 7 consecutive failures, the device goes to HIZ mode. The battery powers up the system when the device is in HIZ. On BQ25883 adapter re-plugin and/or EN_HIZ bit toggle is required to restart device operation. The EN_HIZ bit is cleared automatically when the adapter is plugged in. If the fault is not removed, the part will enter HIZ mode again after the 7 consecutive failures.

8.3.3.2 Input Source Type Detection

After input source is qualified, the charger device runs input source type detection.

The BQ25883 follows the USB Battery Charging Specification 1.2 (BC1.2) to detect input source (SDP/CDP/DCP) and non-standard adapter through USB D+/D- lines. After input source type detection, the following registers and pins are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit
2. Input Voltage Limit (VINDPM) register is changed to set default limit (if EN_VINDPM_RST = 1, otherwise VINDPM value remains unchanged)
3. VBUS_STAT bits change to reflect the detected source
4. $\overline{\text{INT}}$ pin pulses to notify the host
5. $\overline{\text{PG}}$ pin is pulled LOW, and PG_STAT bit is set to '1'

After detection is completed, the host can over-write IINDPM or VINDPM registers to change the input current, or input voltage limit if needed. The charger input current is always limited by the lower of IINDPM register , ILIM pin, or Input Current Optimizer (ICO) setting when ICO is enabled.

When AUTO_INDET_EN is disabled, the Input Source Type Detection is bypassed, and the Input Current Limit (IINDPM) register remains unchanged from previous value. When EN_VINDPM_RST is disabled, the Input Voltage Limit (VINDPM) register remains unchanged from previous value.

Feature Description (continued)

8.3.3.2.1 D+/D– Detection Sets Input Current Limit

The BQ25883 contains a D+/D- based input source detection to program the input current limit. The D+/D- detection has three major steps: Data Contact Detect (DCD), Primary Detection, and Secondary Detection.

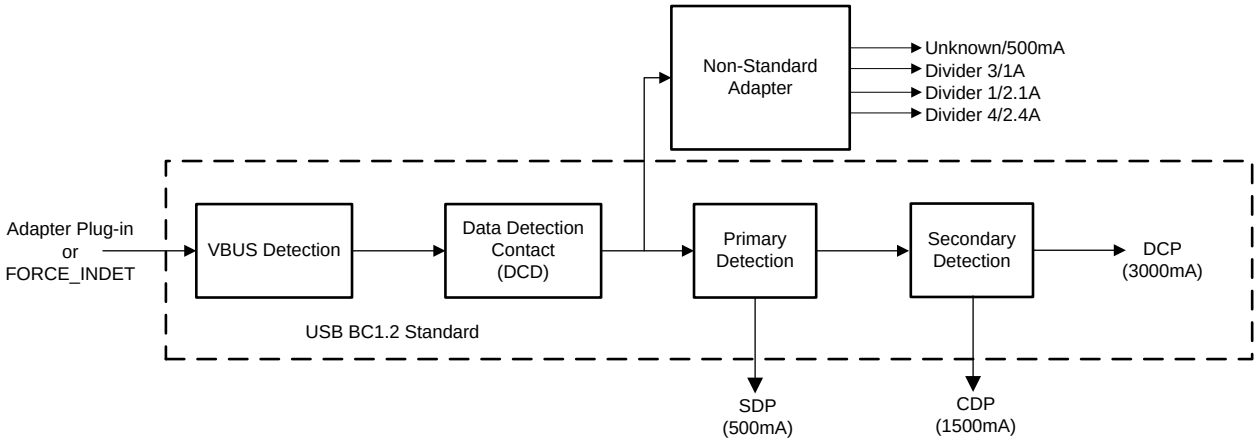

Figure 15. D+/D- Detection Flow

Table 2. Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D+ THRESHOLD	D– THRESHOLD	INPUT CURRENT LIMIT
Divider 1	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P0_VTH}	2.1A
Divider 3	V_{D+} within V_{2P0_VTH}	V_{D-} within V_{2P8_VTH}	1A
Divider 4	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P8_VTH}	2.4A

After the Input Source Type Detection is done, an $\overline{INT}$ pulse is asserted to the host. In addition, the following registers including Input Current Limit register (IINDPM), and VBUS_STAT are updated as below:

Table 3. Input Current Limit Setting from D+/D– Detection

D+/D– DETECTION	INPUT CURRENT LIMIT (IINDPM)	VBUS_STAT
USB SDP (USB500)	500mA	001
USB CDP	1.5A	010
USB DCP	3.0A	011
Divider 3	1A	110
Divider 1	2.1A	110
Divider 4	2.4A	110
Unknown 5V Adapter	500mA	101

8.3.3.2.2 Force Input Current Limit Detection

In host mode, the host can force the device to run Input Current Limit Detection by setting FORCE_INDET bit. After the detection is completed, FORCE_INDET bit returns to 0 by itself and input result is updated.

8.3.3.3 Power Up REGN Regulator (LDO)

The REGN LDO supplies internal bias circuits as well as the QHS and QLS gate drive. The LDO also provides bias rail to TS external resistors. The pull-up rail of STAT and PG can be connected to REGN as well. The REGN is enabled when all the below conditions are valid.

1. VBUS above $V_{VBUS_UVLO_RISING}$ in boost mode or VBUS below $V_{VBUS_UVLO_RISING}$ in buck mode
2. Poor Source Qualification detects a valid input source
3. Input Source Type Detection completes and sets appropriate input current limit

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4. After 220 ms delay is complete

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than I_{VBUS_HIZ} from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

8.3.3.4 Converter Power Up

After the input current limit is set, the $\overline{PG}$ pin is pulled LOW, the PG_STAT and VBUS_STAT bits are changed, and the converter is enabled, allowing the HSFET and LSFET to start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery. The device provides soft-start when is ramped up.

Before charging begins, the battery discharge source (IBAT_DISCHG) is enabled automatically to detect the presence of battery. The host can enable IBAT_DISCHG via the EN_BAT_DISCHG bit at any point during operation, including in Battery Only or HIZ modes.

As a battery charger, the device deploys a highly efficient 1.5 MHz boost switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

In order to improve light-load efficiency, the device switches to PFM (Pulse Frequency Modulation) control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

8.3.4 Input Current Optimizer (ICO)

The device provides innovative Input Current Optimizer (ICO) to identify maximum power point without overloading the input source. The algorithm automatically identifies maximum input current limit of a power source without staying in VINDPM to avoid input source overload.

On BQ25883, this feature is enabled by default (EN_ICO=1) and can be disabled by setting EN_ICO bit to 0. After DCP type input source is detected based on the procedures describe above (Input Source Type Detection). The algorithm runs automatically when EN_ICO bit is set. The algorithm can also be forced to execute by setting FORCE_ICO bit regardless of input source type detected .

Table 4. Input Current Optimizer Automatic Operation

DEVICE	INPUT SOURCE	INPUT CURRENT LIMIT (IINDPM)	AUTOMATIC START ICO ALGORITHM WHEN EN_ICO = 1
BQ25883 (D+/D–)	USB SDP (USB500)	500mA	Disable
	USB CDP	1.5A	Disable
	USB DCP	3.0A	Enable
	Divider 3	1A	Disable
	Divider 1	2.1A	Disable
	Divider 4	2.4A	Disable
	Unknown 5V Adapter	500mA	Disable

The actual input current limit used by the Dynamic Power Management is reported in ICO_ILIM register while Input Current Optimizer is enabled (EN_ICO = 1) or set by IINDPM register when the algorithm is disabled (EN_ICO=0). In addition, the current limit is clamped by ILIM pin unless EN_ILIM bit is 0 to disable ILIM pin function.

When the algorithm is enabled, it runs continuously to adjust input current limit of Dynamic Power Management (IINDPM) using ICO_ILIM register until ICO_STAT[1:0] and ICO_FLAG bits are set (the ICO_FLAG bit indicates any change in ICO_STAT[1:0] bits). The algorithm operates depending on battery voltage:

1. When voltage at BAT pin is below SYS_MIN, the algorithm starts ICO_ILIM register with IINDPM which is the maximum input current limit allowed by system
2. When voltage at BAT is above SYS_MIN, the algorithm starts ICO_ILIM register with 500mA which is the minimum input current limit to minimize adapter overload

When optimal input current is identified, the ICO_STAT[1:0] and ICO_FLAG bits are set to indicate input current limit in ICO_ILIM register would not be changed until the algorithm is forced to run by the following event (these events also reset the ICO_STAT[1:0] bits to '01'):

1. A new input source is plugged-in, or EN_HIZ bit is toggled
2. IINDPM register is changed
3. VINDPM register is changed
4. FORCE_ICO bit is set to 1
5. VBUS_OVP event

8.3.5 Buck Mode Operation from Battery (OTG)

The device supports buck converter operation to deliver power from the battery to other portable devices through USB port. The buck mode output current rating meets the USB On-The-Go 500 mA (OTG_ILIM bits = 000) output requirement. The maximum output current is up to 2.0 A. The buck operation can be enabled if the following conditions are valid:

1. BAT above V_{OTG_BAT}
2. VBUS less than $V_{VBUS_PRESENT}$
3. ADC is enabled
4. Buck mode operation is enabled (EN_OTG = 1 and EN_CHG = 0)
5. Voltage at TS (thermistor) pin is within range configured by Buck Mode Temperature Monitor as configured by BHOT and BCOLD register bits
6. After 30 ms delay from buck mode enable

In buck mode, the device employs 1.5 MHz step-down switching regulator based on system requirements. During buck mode, the status register VBUS_STAT bits are set to 111, the VBUS output is 5.1V by default (selectable via OTG_VLIM register bits) and the output current can reach up to 2.0 A, selected via I2C (OTG_ILIM bits). The buck output is maintained when BAT is above V_{OTG_BAT} threshold, and VBUS is above $V_{VBUS_PRESENT}$ threshold. After OTG startup, the ADC maybe disabled.

8.3.6 Power Path Management

The device accommodates a wide range of input sources from USB, to wall adapter, to power bank. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

8.3.6.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by SYS_MIN bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 6.2V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 200mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of BATFET.

When the battery charging is disabled and VBAT is above minimum system voltage setting or charging is terminated, the system is always regulated at typically 50mV above battery voltage. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

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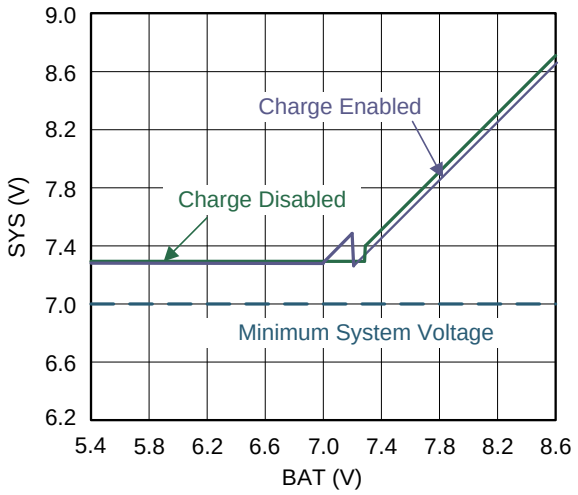

Figure 16. System Voltage vs. Battery Voltage

8.3.6.2 Dynamic Power Management

To meet the maximum current limit in the USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (IINDPM or ICO_ILIM or ILIM pin setting) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the Supplement Mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register bits VINDPM_STAT (VINDPM) and/or IINDPM_STAT (IINDPM) go high. The figure shows the DPM response with 5V/3A adapter, 6.4V battery, 1.5A charge current and 6.8V minimum system voltage setting.

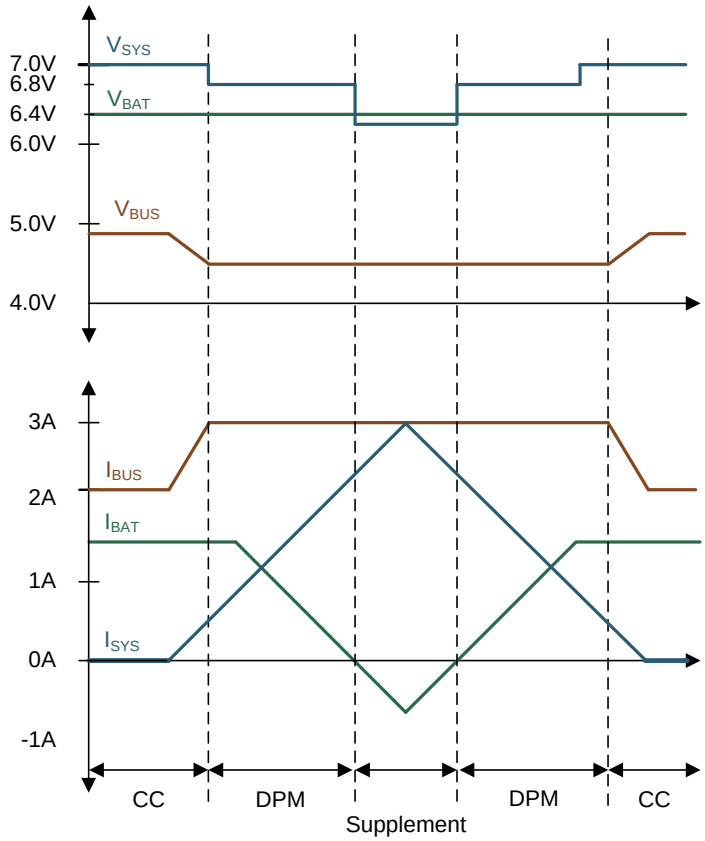

Figure 17. DPM Response

8.3.6.3 Supplement Mode

When the voltage falls below the battery voltage, the BATFET turns on.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce R_{DSON} until the BATFET is in full conduction. At this point onwards, the BATFET V_{DS} linearly increases with discharge current. The figure shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit Supplement Mode when the battery is below battery depletion threshold ($V_{BAT_UVLO_RISING}$).

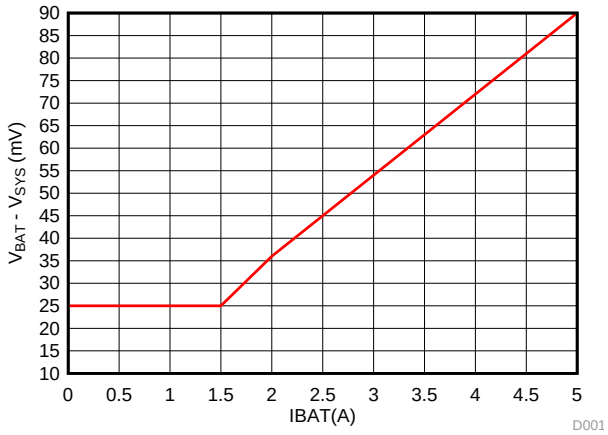

Figure 18. BATFET I-V Curve

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8.3.7 Battery Charging Management

The BQ25883 charges 2-cell Li-Ion battery with up to 2.2-A charge current for high capacity battery. The low $R_{DS(ON)}$ BATFET improves charging efficiency and minimize the voltage drop during discharging.

8.3.7.1 Autonomous Charging Cycle

When battery charging is enabled (EN_CHG bit =1 and $\overline{CE}$ pin is LOW;), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table below. On BQ25883, the host can always control the charging operation and optimize the charging parameters by writing to the corresponding registers through I^2C.

Table 5. Charging Parameter Default Settings

DEFAULT MODE	BQ25883
Charging Voltage	8.40 V
Charging Current	1.50 A
Pre-Charge Current	150 mA
Termination Current	150 mA
Temperature Profile	JEITA
Safety Timer	12 hours
Topoff Timer	Disabled

A new charge cycle starts when the following conditions are valid:

1. Converter starts
2. Battery charging is enabled by I2C register bit (EN_CHG = 1 and $\overline{CE}$ pin is LOW and ICHG register is not 0 mA)
3. No thermistor fault on TS
4. No safety timer fault

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and device is not in DPM mode or thermal regulation. When a full battery voltage is discharged below recharge threshold (threshold selectable via VRECHG[1:0] bits on BQ25883), the device automatically starts a new charging cycle. After the charge is done, either toggle $\overline{CE}$ pin or EN_CHG bit can initiate a new charging cycle.

The STAT output indicates the charging status of: charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). If no battery is connected, the STAT pin blinks as capacitance connected at BAT charges, discharges, then recharges. The STAT output can be disabled by setting STAT_DIS bit. In addition, the status register (CHRG_STAT) indicates the different charging phases as:

- 000 – Not Charging
- 001 – Trickle Charge (VBAT < V_{BAT_SHORT})
- 010 – Pre-charge (V_{BAT_SHORT} < VBAT < V_{BAT_LOWV})
- 011 – Fast-charge (CC mode)
- 100 – Taper Charge (CV mode)
- 101 – Top-off Timer Charging
- 110 – Charge Termination Done

8.3.7.2 Battery Charging Profile

The device charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage, and top-off timer charging. At the beginning of a charging cycle, the device checks the battery voltage and regulates current/voltage accordingly.

Table 6. Default Charging Current Setting

VBAT	CHARGING CURRENT	REGISTER DEFAULT SETTING	CHRG_STAT
< V_{BAT_SHORT}	I_{BAT_SHORT}	100 mA	001
V_{BAT_SHORT} – V_{BAT_LOWV}	I_{PRECHG}	150 mA	010

Table 6. Default Charging Current Setting (continued)

VBAT	CHARGING CURRENT	REGISTER DEFAULT SETTING	CHRG_STAT
> V_{BAT_LOWV}	I_{CHG}	1500 mA	011

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate, as explained in the *Charging Safety Timer* section.

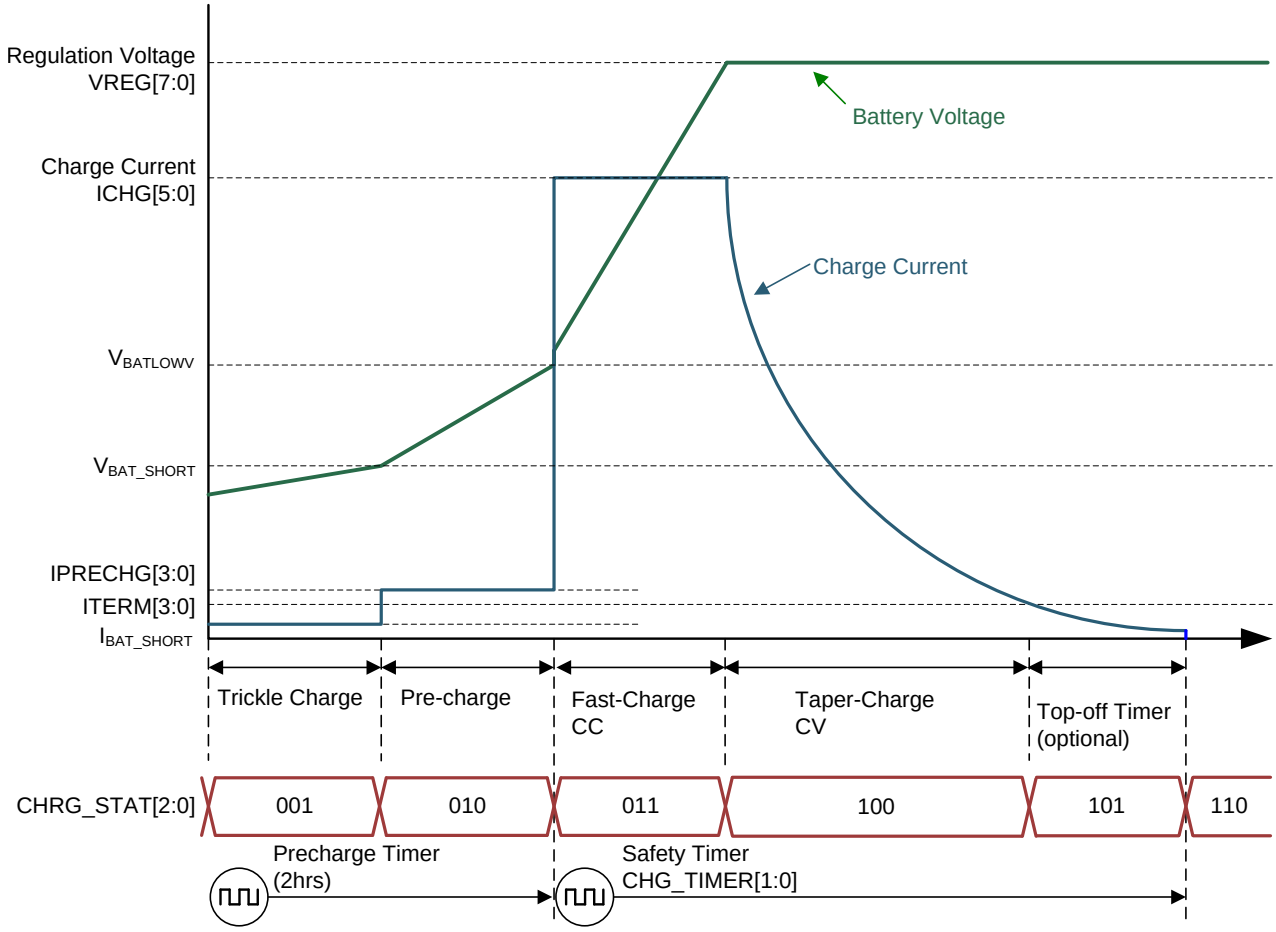

Figure 19. Battery Charging Profile

8.3.7.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage Supplement Mode.

When termination occurs, the STAT pin goes HIGH (charge current will continue to taper if top-off timer is enabled), status register CHRG_STAT is set to 110, and an $\overline{INT}$ pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be permanently disabled by writing 0 to EN_TERM bit prior to charge termination.

At low termination currents (50mA-100mA), due to the comparator offset, the actual termination current may be up to 20% higher than the termination target. In order to compensate for comparator offset, a programmable top-off timer (default disabled) can be applied after termination is detected.The top-off timer will follow safety timer constraints, such that if safety timer is suspended, so will the top-off timer. Similarly, if safety timer is doubled, so will the top-off timer. CHRG_STAT reports whether the top off timer is active via the 101 code. Once the Top-Off timer expires, the CHRG_STAT register is set to 110 and an $\overline{INT}$ pulse is asserted to the host.

Top-off timer gets reset (set to 0 and counting resumes when appropriate) for any of the following conditions:

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1. Charge disable to enable
2. Termination status low to high
3. REG_RST register bit is set (disables top-off timer)

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value after termination will have no effect unless a recharge cycle is initiated. An $\overline{INT}$ is asserted to the host when entering top-off timer segment as well as when top-off timer expires. All charge cycle related $\overline{INT}$ pulses (including top-off timer $\overline{INT}$ pulses) can be masked by CHRG_MASK bit.

8.3.7.4 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitor.

8.3.7.4.1 JEITA Guideline Compliance in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the T1-T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range. At cool temperature (T1-T2), JEITA recommends the charge current to be reduced to half of the charge current or lower. At warm temperature (T3-T5), JEITA recommends charge voltage less than 4.1V / cell.

On BQ25883, the charger provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3-T5) can be VREG, 8.0V, 8.3V, or charge suspend (configured by JEITA_VSET [1:0]). The fast charge current setting at warm temperature (T3-T5) can be 100%, or 40% of fast charge current, ICHG (configured by JEITA_ISETH). The fast charge current setting at cool temperature (T1-T2) can be 100%, 40%, or 20% of fast charge current, ICHG, or charge suspend (configured by JEITA_ISETC[1:0]). Whenever the charger detects "warm" or "cool" temperature, termination is automatically disabled regardless of JEITA_VSET, JEITA_ISETH and JEITA_ISETC register bit settings.

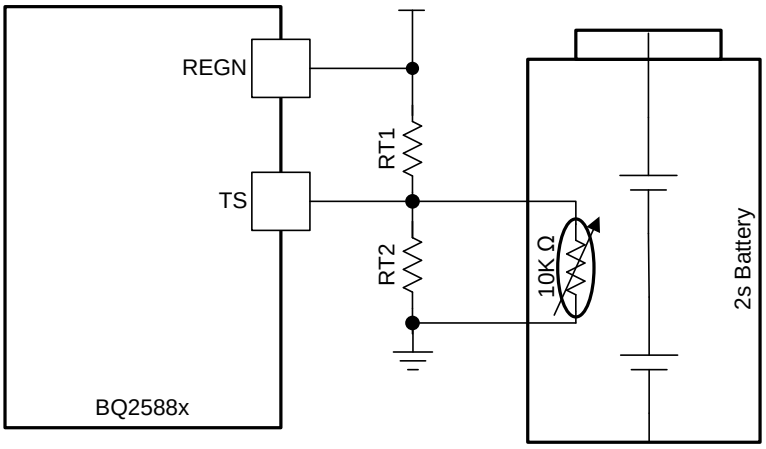

Figure 20. TS Resistor Network

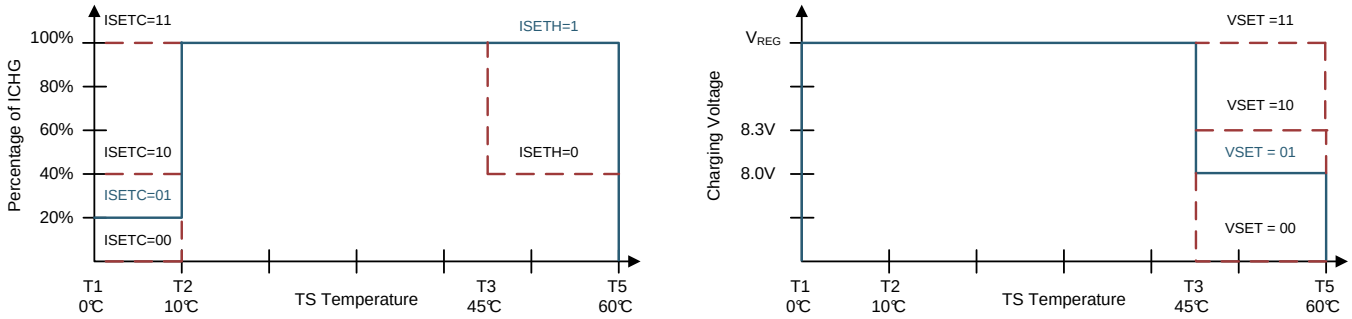

Figure 21. TS Charging Values

Assuming a 103AT NTC (Negative Temperature Coefficient) thermistor on the battery pack as shown above, the value of RT1 and RT2 can be determined by:

$$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T5} \times \left(\frac{1}{V_{T5}} - \frac{1}{V_{T1}}\right)}{R_{NTC,T1} \times \left(\frac{1}{V_{T1}} - 1\right) - R_{NTC,T5} \times \left(\frac{1}{V_{T5}} - 1\right)} \quad (1)$$

$$RT1 = \frac{\frac{1}{V_{T1}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}} \quad (2)$$

Select 0°C to 60°C range for Li-ion or Li-polymer battery:

$R_{NTC,T1}$ = 27.28kΩ

$R_{NTC,T5}$ = 3.02kΩ

RT1 = 5.24kΩ

RT2 = 30.31kΩ

8.3.7.4.2 Cold/Hot Temperature Window in OTG Buck Mode

For battery protection during OTG buck mode, the device monitors the battery temperature to be within the VBCOLD to VBHOT thresholds. When temperature is outside of the temperature thresholds, the OTG mode is suspended. In addition, VBUS_STAT bits are set to 000 and corresponding TS_STAT is reported. Once temperature returns within thresholds, the OTG mode is recovered and TS_STAT is cleared.

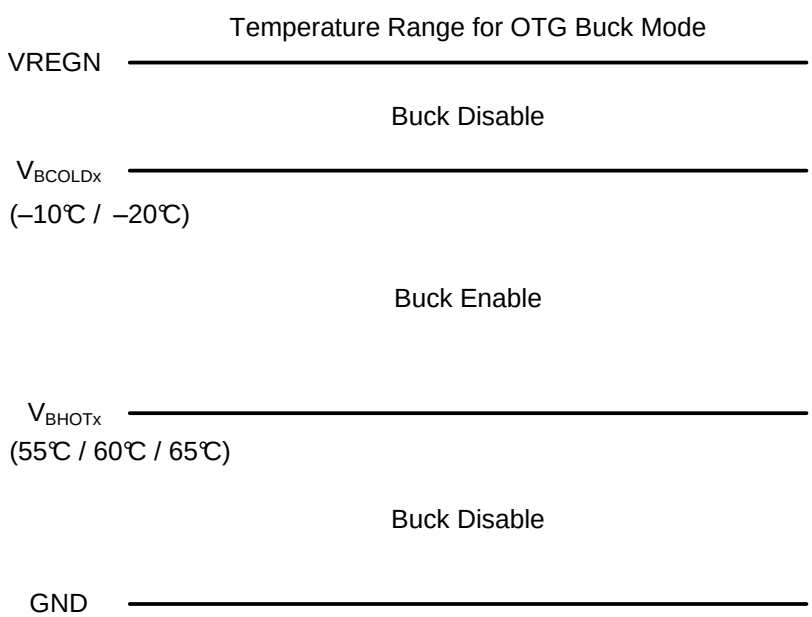

Figure 22. TS Pin Thermistor Sense Threshold in OTG Buck Mode

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8.3.7.5 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The user can program fast charge safety timer through I^2C (CHG_TIMER bits). When safety timer expires, the fault register TMR_STAT bit is set to 1, and an $\overline{INT}$ pulse is asserted to the host. The safety timer feature can be disabled by clearing EN_TIMER bit.

During input voltage, current or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM_STAT=1) throughout the whole charging cycle, and the safety timer is set to 12 hours, then the timer will expire in 24 hours. This half clock rate feature can be disabled by setting TMR2X_EN = 0. Changing the TMR2X_EN bit while the device is running has no effect on the safety timer count, other than forcing the timer to count at half the rate under the conditions dictated above.

During faults which disable charging, or supplement mode, timer is suspended. Since the timer is not counting in this state, the TMR2X_EN bit has no effect. Once the fault goes away, safety timer resumes. If the charging cycle is stopped and started again, the timer gets reset (toggle $\overline{CE}$ pin or EN_CHG bit restarts the timer).

The safety timer is reset for the following events:

1. Charging cycle stop and restart (toggle $\overline{CE}$ pin, EN_CHG bit, or charged battery falls below recharge threshold).
2. BAT voltage changes from pre-charge to fast-charge or vice versa (in host-mode or default mode).

The precharge safety timer (fixed 2hr counter that runs when VBAT < V_{BAT_LOWV}), follows the same rules as the fast-charge safety timer in terms of getting suspended, reset, and counting at half-rate when TMR2X_EN is set.

8.3.8 Integrated 16-Bit ADC for Monitoring

The device includes a 16-bit ADC to monitor critical system information based on the device's modes of operation. The control of the ADC is done through the *ADC Control Register (Address = 15h) [reset = 30h]*. The ADC_EN bit provides the ability to enable and disable the ADC to conserve power. The ADC_RATE bit allows continuous conversion or one-shot behavior. After a one-shot conversion finishes, the ADC_EN bit is cleared, and must be re-asserted to start a new conversion.

To enable the ADC, the ADC_EN bit must be set to '1'. The ADC is allowed to operate if either the $V_{VBUS}>V_{VBUS_UVLO_RISING}$ or $V_{BAT}>V_{BAT_UVLO_RISING}$ is valid. If no adapter is present, and the VBAT is less than $V_{BAT_UVLO_RISING}$, the device will not perform an ADC measurement, nor update the ADC read-back values in REG17 through REG24. Additionally, the device will immediately reset ADC_EN bit without sending any interrupt. The same will happen if the ADC is enabled when all ADC channels are disabled. It is recommended to read back ADC_EN after setting it to '1' to ensure ADC is running a conversion. If the charger changes mode (for example, if adapter is connected, EN_HIZ goes to '1', or EN_OTG goes to '1') while an ADC conversion is running, the conversion is interrupted. Once the mode change is complete, the ADC resumes conversion, starting with the channel where it was interrupted. When device is in HIZ mode, ADC conversion can still be enabled through I2C. In HIZ mode, device power up internally to start ADC convertion and turn back down when ADC conversion is completed.

When TS_ADC conversion performs in battery only mode, the REGN is powered and extra battery current would be drawn. Battery current can be kept low by disabling the TS_ADC conversion in battery only mode.

The integrated ADC has two rate conversion options: a one-shot mode and a continuous conversion mode set by the ADC_RATE bit. By default, all ADC parameters will be converted in one-shot or continuous conversion mode unless disabled in the *ADC Function Disable Register (Address = 16h) [reset = 00h]*. If an ADC parameter is disabled by setting the corresponding bit in REG16, then the read-back value in the corresponding register will be from the last valid ADC conversion or the default POR value (all zeros if no conversions have taken place). If an ADC parameter is disabled in the middle of an ADC measurement cycle, the device will finish the conversion of that parameter, but will not convert the parameter starting the next conversion cycle. Even though no conversion takes place when all ADC measurement parameters are disabled, the ADC circuitry is active and ready to begin conversion as soon as one of the bits in the ADC Function Disable register is set to '0'. If all channels are disabled in one-shot conversion mode, the ADC_EN bit is cleared.

The ADC_DONE_STAT and ADC_DONE_FLAG bits signal when a conversion is completed in one-shot mode only. This event produces an $\overline{INT}$ pulse, which can be masked with ADC_DONE_MASK. During continuous conversion mode, the ADC_DONE_STAT bit has no meaning and will be '0'. The ADC_DONE_FLAG bit will remain unchanged in continuous conversion mode.

ADC conversion operates independently of the faults present in the device. ADC conversion will continue even after a fault has occurred (such as one that causes the power stage to be disabled), and the host must set ADC_EN = '0' to disable the ADC. ADC conversion is interrupted upon adapter plug-in, and will only resume until after Input Source Type Detection is complete. ADC readings are only valid for DC states and not for transients. When host writes ADC_EN=0, the ADC stops immediately, and ADC measurement values correspond to last valid ADC reading.

A recommended method to exit ADC conversion is described below:

1. Write ADC_RATE to one-shot, and the ADC will stop at the end of a complete cycle of conversions, or
2. Disable all ADC conversion channels, and the ADC will stop at the end of the current measurement.

8.3.9 Status Outputs

8.3.9.1 Power Good Indicator ($\overline{PG}$)

The PG_STAT bit goes HIGH and open drain $\overline{PG}$ pin goes low to indicate a good input source when:

1. VBUS above $V_{VBUS_UVLO_RISING}$
2. VBUS below V_{VBUS_OV} threshold
3. VBUS above $V_{POORSRC}$ (typ. 3.7 V) when $I_{POORSRC}$ (typ. 30 mA) current is applied (not a poor source)
4. Input Source Type Detection is completed

8.3.9.2 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED.

Table 7. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including trickle charge, pre-charge, fast-charge, recharge)	LOW
Charging complete (including top-off)	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input over-voltage, TS fault, timer fault or battery over-voltage) OTG Buck Mode suspend (due to TS fault)	Blinking at 1Hz

8.3.9.3 Interrupt to Host

In some applications, the host does not always monitor the charger operation. The $\overline{INT}$ pin notifies the system host on the device operation. By default, the following events will generate an active-low, 256µs $\overline{INT}$ pulse.

1. Good input source detected
   - $V_{VBUS} < V_{VBUS_OV}$ threshold
   - $V_{VBUS} > V_{POORSRC}$ (typ. 3.7 V) when $I_{POORSRC}$ (typ. 30 mA) current is applied (not a poor source)
2. VBUS_STAT changes state (VBUS_STAT any bit change)
3. Good input source removed
4. Entering IINDPM regulation
5. Entering VINDPM regulation
6. Entering IC junction temperature regulation (TREG)
7. I2C Watchdog timer expired
   - At initial power up, this $\overline{INT}$ gets asserted to signal I2C is ready for communication
8. Charger status changes state (CHRG_STAT value change), including Charge Complete
9. TS_STAT changes state (TS_STAT any bit change)
10. VBUS over-voltage detected (VBUS_OVP)
11. Junction temperature shutdown (TSHUT)
12. Battery over-voltage detected (BATOVP)

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13. Charge safety timer expired
14. A rising edge on any of the *_STAT bits

Each one of these $\overline{INT}$ sources can be masked off to prevent $\overline{INT}$ pulses from being sent out when they occur. Three bits exist for each one of these events:

- The STAT bit holds the *current status* of each $\overline{INT}$ source
- The FLAG bit holds information on which source produced an $\overline{INT}$, regardless of the current status
- The MASK bit is used to prevent the device from sending out $\overline{INT}$ for each particular event

When one of the above conditions occurs (a rising edge on any of the *_STAT bits), the device sends out an $\overline{INT}$ pulse and keeps track of which source generated the $\overline{INT}$ via the FLAG registers. The FLAG register bits are automatically reset to zero after the host reads them, and a new edge on STAT bit is required to re-assert the FLAG.

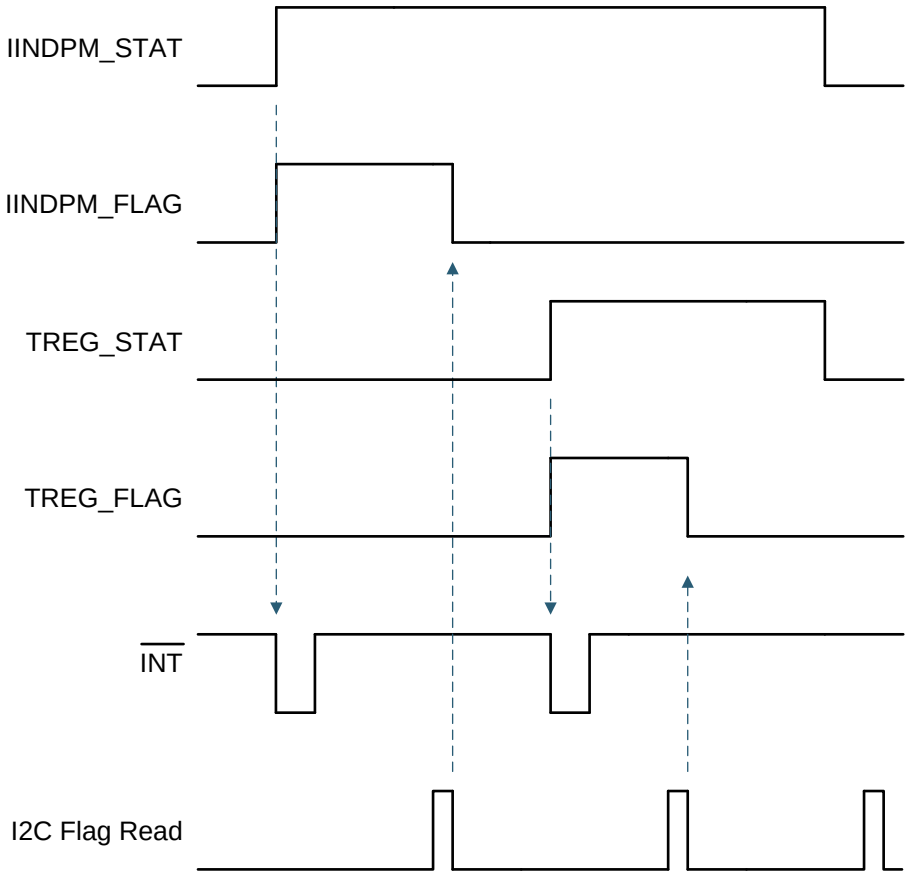

Figure 23. $\overline{INT}$ Generation Behavior Example

8.3.10 Input Current Limit on ILIM Pin

For safe operation, the BQ2588x has an additional hardware pin on ILIM to limit maximum input current. The maximum input current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (3)$$

The actual input current limit is the lower value between ILIM pin setting and register setting (IINDPM). For example, if the register setting is 3.3A (0x1C), and ILIM has a 820-Ω resistor (KILIM = 1276 max) to ground for 1.55A, the input current limit is 1.55A. ILIM pin can be used to set the input current limit rather than the register settings when EN_ILIM bit is set. The device regulates ILIM pin at 0.8V. If ILIM voltage exceeds 0.8V, the device enters input current regulation (Refer to *Dynamic Power Management* section). Entering IINDPM through ILIM pin sets the IINDPM_STAT and FLAG bits, and produces and interrupt to host. The interrupt can be masked via the IINDPM_MASK bit.

The ILIM pin can also be used to monitor input current when EN_ILIM is set. The voltage on ILIM pin is proportional to the input current. ILIM can be used to monitor input current with the following relationship:

$$I_{IN} = \frac{K_{ILIM} \times V_{ILIM}}{R_{ILIM} \times 0.8V} \tag{4}$$

For example, if ILIM pin is set with 820-Ω resistor, and the ILIM voltage 0.5V, the actual input current is 0.795A to 0.973A. If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 0.8V. If ILIM pin is shorted, the input current limit is set by the register.

The ILIM pin function can be disabled by setting the EN_ILIM bit to 0. When the pin is disabled, both input current limit function and monitoring function are not available.

8.3.11 Voltage and Current Monitoring

The device closely monitors the input voltage and system voltage, as well as internal FET currents for safe boost and buck mode operation.

8.3.11.1 Voltage and Current Monitoring in Boost Mode

8.3.11.1.1 Input Over-Voltage Protection

The valid input voltage range for boost mode operation is V_{VBUS_OP}. If VBUS voltage exceeds V_{VBUS_OV}, the device stops switching immediately to protect the power FETs. During input over-voltage, an $\overline{INT}$ pulse is asserted to signal the host, and the VBUS_OVP_STAT and VBUS_OVP_FLAG fault registers get set. The device automatically starts switching again when the over-voltage condition goes away.

8.3.11.1.2 Input Under-Voltage Protection

The valid input voltage range for boost mode operation is V_{VBUS_OP}. If VBUS voltage falls below $V_{POORSRC}$ during operation, the device stops switching. During input under-voltage, an $\overline{INT}$ pulse is asserted to signal the host, and the PG_STAT bit gets cleared. The PG_FLAG bit will get set to signal this event. The device automatically attempts to restart switching when the under-voltage condition goes away.

8.3.11.1.3 System Over-Voltage Protection

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. SYSOVP threshold is 350 mV above system regulation voltage. Upon SYSOVP, converter stops immediately to clamp the overshoot.

8.3.11.1.4 System Over-Current Protection

The charger device continually monitors and compares VBUS to VSYS to protect against a system short-circuit event. In the event that VSYS drops to within 250 mV of VBUS during operation, a short circuit event is flagged and the converter stops switching. The SYS_SHORT_FLAG or SNS_SHORT_FLAG bit is set and an $\overline{INT}$ pulse is asserted to the host. The device attempts to recover from this condition automatically.

8.3.11.2 Voltage and Current Monitoring in OTG Buck Mode

The device closely monitors the VBUS voltage, as well as RBFET (Q1, QBLK) and LSFET (Q3, QLS) current to ensure safe buck mode operation.

8.3.11.2.1 VBUS Over-voltage Protection

When the VBUS voltage rises above regulation target and exceeds V_{OTG_OVP}, the device enters over-voltage protection which stops switching, clears the EN_OTG bit and exits buck mode. During the over-voltage duration, the OTG_FLAG bits are set high to indicate a fault in buck mode operation. An $\overline{INT}$ is also asserted to the host.

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8.3.11.2.2 VBUS Over-Current Protection

The device monitors output current to provide output short protection. The OTG buck mode has built-in constant current regulation to allow OTG to adapt to various types of loads. If short circuit is detected on VBUS, the OTG turns off and retries 7 times. If the retries are not successful, OTG is disabled with EN_OTG bit cleared. In addition OTG_FLAG bits are set high to indicate the fault, and an $\overline{INT}$ is asserted to the host.

8.3.12 Thermal Regulation and Thermal Shutdown

8.3.12.1 Thermal Protection in Boost Mode

The device monitors internal junction temperature, T_J, to avoid overheating and limits the IC surface temperature in boost mode. When the internal junction temperature exceeds the preset thermal regulation limit (TREG bits), the device reduces charge current. A wide thermal regulation range from 60°C to 120°C allows optimization for the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed value in ICHG registers. Therefore, termination is disabled, the safety timer runs at half the clock rate, the status register TREG_STAT bit goes high, and an $\overline{INT}$ is asserted to the host.

Additionally, the device has thermal shutdown to turn off the converter when IC surface temperature exceeds T_{SHUT}. The fault register bits TSHUT_STAT and TSHUT_FLAG are set and an $\overline{INT}$ pulse is asserted to the host. The converter turns back on when IC temperature is below T_{SHUT_HYS}.

8.3.12.2 Thermal Protection in OTG Buck Mode

The BQ2588x monitors the internal junction temperature to provide thermal shutdown during OTG buck mode.

8.3.13 Battery Protection

8.3.13.1 Battery Over-Voltage Protection (BATOVP)

The battery over-voltage limit is clamped at 4% above the battery regulation voltage while charging. When battery over-voltage occurs, the charger device immediately disables charge. The fault register BATOVP_STAT bit goes high and an $\overline{INT}$ pulse is asserted to signal the host. The battery regulation voltage can be changed by JEITA_VSET bits and battery temperature, but BATOVP set point will not change.

8.3.13.2 Battery Over-Discharge Protection

When the battery is discharged below $V_{BAT_SHORT_HYS}$, the BATFET is turned off to protect battery from over-discharge. To recover from over-discharge, an input source is required at VBUS. When an input source is plugged in, the BATFET turns on. The battery is charged with I_{BAT_SHORT} current when the VBAT < V_{BAT_SHORT}, or pre-charge current as set in IPRECHG registers when the battery voltage is between V_{BAT_SHORT} and V_{BAT_LOWV}.

8.3.14 Serial Interface

The device uses I2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I2C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 0x6B, receiving control inputs from the master device like micro-controller or digital signal processor through REG00 – REG25. Register read beyond REG25 (0x25), returns 0xFF. The I2C interface supports both standard mode (up to 100kbits/s), and fast mode (up to 400kbits/s). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

8.3.14.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on SCL line is LOW. One clock pulse is generated for each data bit transferred.

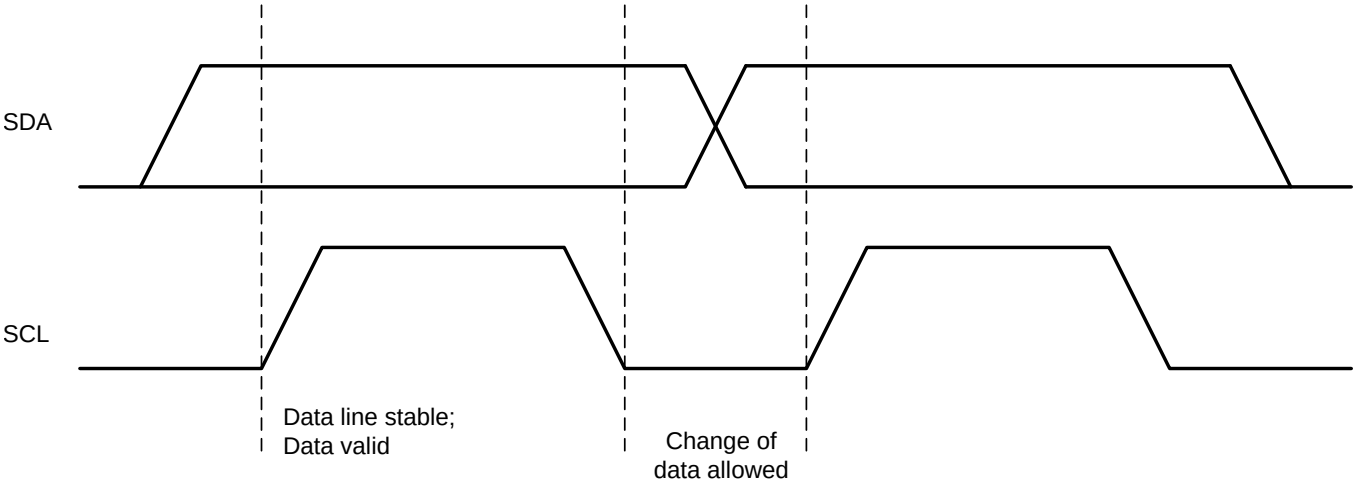

Figure 24. Bit Transfers on the I2C bus

8.3.14.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

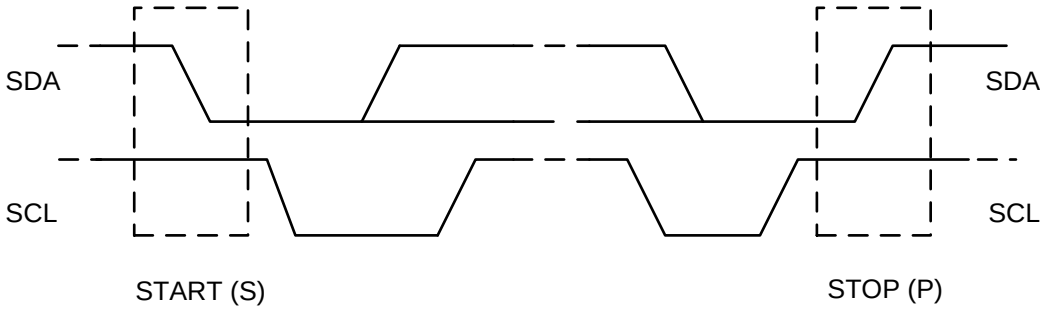

Figure 25. START and STOP conditions on the I2C bus

8.3.14.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and releases the SCL line.

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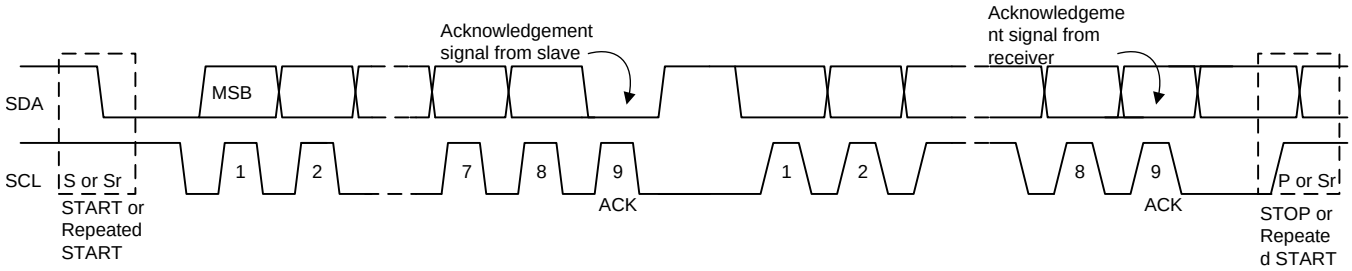

Figure 26. Data Transfer on the I2C Bus

8.3.14.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after byte. The ACK bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

8.3.14.5 Slave Address and Data Direction Bit

After the START signal, a slave address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/$\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as 1101 011' (0x6B) by default. The address bit arrangement is shown below.

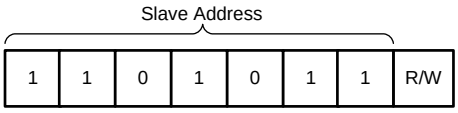

Figure 27. 7-Bit Addressing (0x6B)

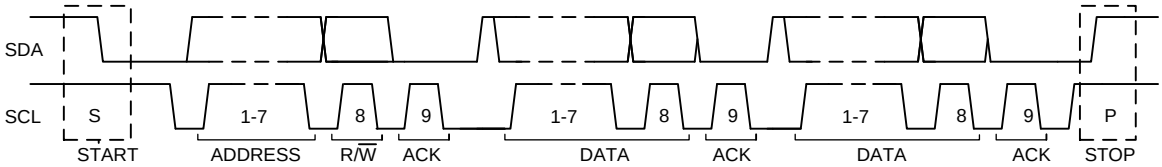

Figure 28. Complete Data Transfer on the I2C Bus

8.3.14.6 Single Write and Read

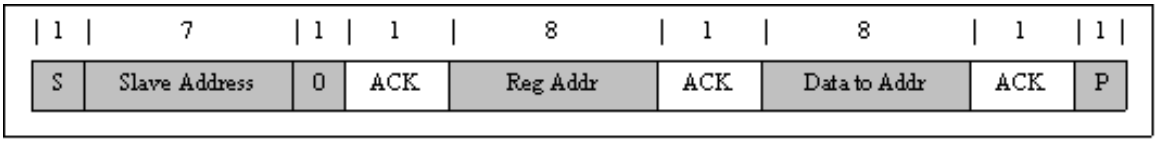

Figure 29. Single Write

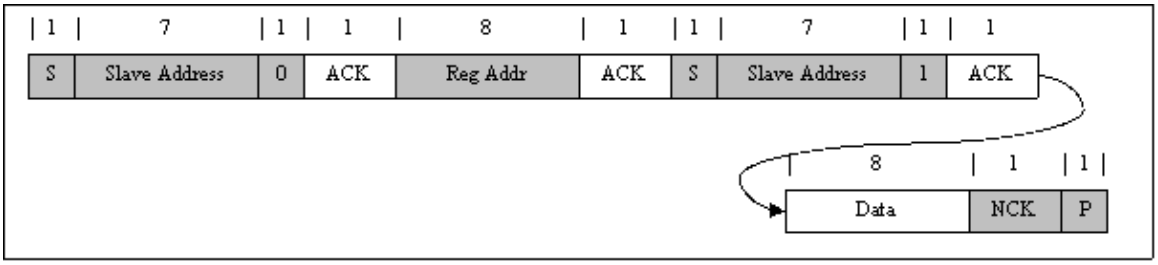

Figure 30. Single Read

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

8.3.14.7 Multi-Write and Multi-Read

The charger device supports multi-read and multi-write of all registers.

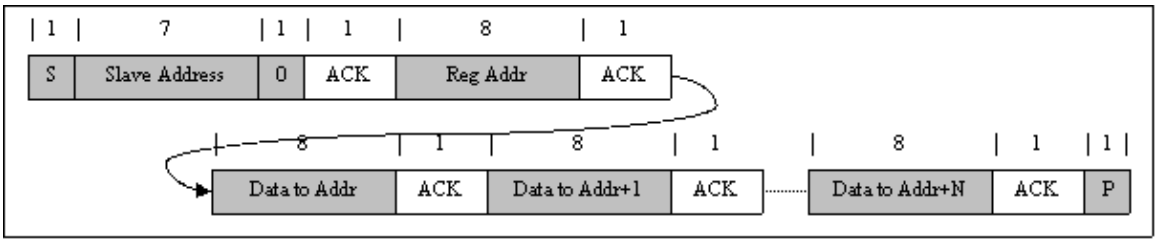

Figure 31. Multi-Write

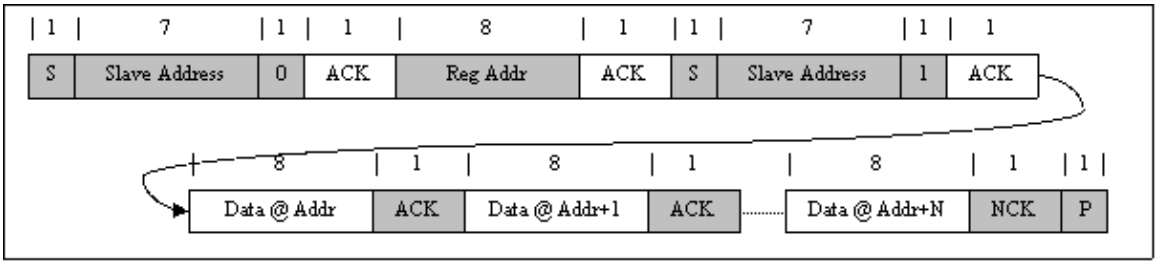

Figure 32. Multi-Read

8.4 Device Functional Modes

8.4.1 Host Mode and Default Mode

The BQ2588x is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD_STAT bit is HIGH. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 12-hour fast charging safety timer. At the end of the 12-hour, the charging is stopped and the boost converter continues to operate to supply system load.

A I2C write to the registers transitions the charger from default mode to host mode and watchdog timer is reset. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits=00.

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Device Functional Modes (continued)

When the watchdog timer (WD_STAT bit = 1) is expired, the device returns to default mode and all registers are reset to default values except as detailed in the *Register Maps* section. The Watchdog timer will be reset on any write if the watchdog timer has expired.

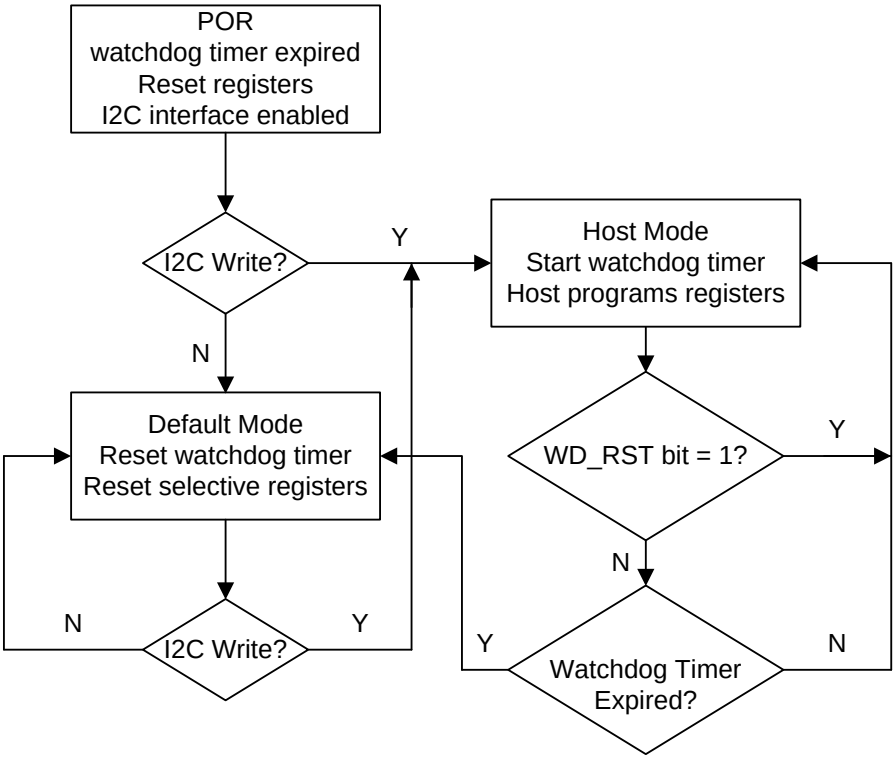

Figure 33. Watchdog Timer Flow Chart

8.5 Register Maps

Default I2C Slave Address: 0x6B (1101 011B + R/$\overline{W}$)

Table 8. I²C Registers

Address	Access Type	Acronym	Register Name	Section
00h	R/W	REG00	Battery Voltage Limit	Go
01h	R/W	REG01	Charge Current Limit	Go
02h	R/W	REG02	Input Voltage Limit	Go
03h	R/W	REG03	Input Current Limit	Go
04h	R/W	REG04	Precharge and Termination Control	Go
05h	R/W	REG05	Charger Control 1	Go
06h	R/W	REG06	Charger Control 2	Go
07h	R/W	REG07	Charger Control 3	Go
08h	R/W	REG08	Charger Control 4	Go
09h	R/W	REG09	OTG Control	Go
0Ah	R	REG0A	ICO Current Limit	Go
0Bh	R	REG0B	Charger Status 1	Go
0Ch	R	REG0C	Charger Status 2	Go
0Dh	R	REG0D	NTC Status	Go
0Eh	R	REG0E	FAULT Status	Go

Table 8. I²C Registers (continued)

Address	Access Type	Acronym	Register Name	Section
0Fh	R	REG0F	Charger Flag 1	Go
10h	R	REG10	Charger Flag 2	Go
11h	R	REG11	Fault Flag	Go
12h	R/W	REG12	Charger Mask 1	Go
13h	R/W	REG13	Charger Mask 2	Go
14h	R/W	REG14	Fault Mask	Go
15h	R/W	REG15	ADC Control	Go
16h	R/W	REG16	ADC Function Disable	Go
17h	R	REG17	IBUS ADC1	Go
18h	R	REG18	IBUS ADC0	Go
19h	R	REG19	ICHG ADC1	Go
1Ah	R	REG1A	ICHG ADC0	Go
1Bh	R	REG1B	VBUS ADC1	Go
1Ch	R	REG1C	VBUS ADC0	Go
1Dh	R	REG1D	VBAT ADC1	Go
1Eh	R	REG1E	VBAT ADC0	Go
1Fh	R	REG1F	VSYS ADC1	Go
20h	R	REG20	VSYS ADC0	Go
21h	R	REG21	TS ADC1	Go
22h	R	REG22	TS ADC0	Go
23h	R	REG23	TDIE ADC1	Go
24h	R	REG24	TDIE ADC0	Go
25h	R/W	REG25	Part Information	Go

Complex bit access types are encoded to fit into small table cells. Table 9 shows the codes that are used for access types in this section.

Table 9. I²C Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset Value		
-n		Value after reset
-X		Undefined value

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8.5.1 Battery Voltage Regulation Limit Register (Address = 00h) [reset = A0h]

REG00 is shown in Figure 34 and described in Table 10.

Return to Summary Table.

Figure 34. REG00 Register

Bit	7	6	5	4	3	2	1	0
Reset	A0h							
Field	VREG[7:0]							

Table 10. REG00 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	VREG[7]	R/W	Yes	Yes	1280 mV	Battery Charge voltage limit Offset: 6.80 V Range: 6.80 V to 9.20 V Default 8.40 V
6	VREG[6]	R/W	Yes	Yes	640 mV	
5	VREG[5]	R/W	Yes	Yes	320 mV	
4	VREG[4]	R/W	Yes	Yes	160 mV	
3	VREG[3]	R/W	Yes	Yes	80 mV	
2	VREG[2]	R/W	Yes	Yes	40 mV	
1	VREG[1]	R/W	Yes	Yes	20 mV	
0	VREG[0]	R/W	Yes	Yes	10 mV	

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8.5.2 Charger Current Limit Register (Address = 01h) [reset = 5Eh]

REG01 is shown in Figure 35 and described in Table 11.

Return to Summary Table.

Figure 35. REG01 Register

Bit	7	6	5	4	3	2	1	0
Reset	0h	1h	1Eh					
Field	EN_HIZ	EN_ILIM	ICHG[5:0]					

Table 11. REG01 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	EN_HIZ	R/W	Yes	Yes	Enable HIZ Mode: 0 – Disable (default) 1 – Enable	
6	EN_ILIM	R/W	Yes	Yes	Enable ILIM Pin Function: 0 – Disable 1 – Enable (default)	
5	ICHG[5]	R/W	Yes	Yes	1600 mA	Fast Charge Current Limit Offset: 100 mA Range: 100mA – 2200mA Default 1500 mA Note: ICHG > 2.2A (2Ch) clamped to 2.2A. ICHG < 100mA (01h) clamped at 100mA
4	ICHG[4]	R/W	Yes	Yes	800 mA	
3	ICHG[3]	R/W	Yes	Yes	400 mA	
2	ICHG[2]	R/W	Yes	Yes	200 mA	
1	ICHG[1]	R/W	Yes	Yes	100 mA	
0	ICHG[0]	R/W	Yes	Yes	50 mA	

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8.5.3 Input Voltage Limit Register (Address = 02h) [reset = 84h]

REG02 is shown in Figure 36 and described in Table 12.

Return to Summary Table.

Figure 36. REG02 Register

Bit	7	6	5	4	3	2	1	0
Reset	1h	0h	0h	04h				
Field	EN_VINDPM_RST	EN_BAT_DISCHG	PFM_OOA_DIS	VINDPM[4:0]				

Table 12. REG02 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	EN_VINDPM_RST	R/W	Yes	Yes	Enable VINDPM automatic reset upon adapter plugin: 0 – Disable VINDPM reset when adapter is plugged in 1 – Enable VINDPM reset when adapter is plugged in (VINDPM resets to default value after Input Source Type Detection) (Default)	
6	EN_BAT_DISCHG	R/W	Yes	Yes	Enable BAT pin discharge load (IBAT_DISCHG): 0 – Disable load (Default) 1 – Enable BAT discharge load	
5	PFM_OOA_DIS	R/W	Yes	No	PFM Out-of-Audio (OOA) Mode Disable: 0 – Out-of-audio mode enabled while converter is in PFM (Default) 1 – Out-of-audio mode disabled while converter is in PFM	
4	VINDPM[4]	R/W	Yes	No	1600 mV	Absolute Input Voltage Limit: Offset: 3.9 V Range: 3.9V – 5.5V Default: 4.3 V Note: VINDPM > 5.5V (10h) clamped to 5.5V. VINDPM register is reset upon adapter plug-in if EN_VINDPM_RST = 1.
3	VINDPM[3]	R/W	Yes	No	800 mV	
2	VINDPM[2]	R/W	Yes	No	400 mV	
1	VINDPM[1]	R/W	Yes	No	200 mV	
0	VINDPM[0]	R/W	Yes	No	100 mV	

8.5.4 Input Current Limit Register (Address = 03h) [reset = 39h]

REG03 is shown in Figure 37 and described in Table 13.

Return to Summary Table.

Figure 37. REG03 Register

Bit	7	6	5	4	3	2	1	0
Reset	0h	0h	1h	19h				
Field	FORCE_ICO	FORCE_INDET	EN_ICO	IINDPM[4:0]				

Table 13. REG03 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	FORCE_ICO	R/W	Yes	Yes	Force Start Input Current Optimizer (ICO): 0 – Do not force ICO (default) 1 – Force ICO start Note: This bit can only be set and always returns 0 after ICO starts. This bit only valid when EN_ICO = 1.	
6	FORCE_INDET	R/W	Yes	Yes	Force D+/D– Detection: 0 – Not in D+/D– detection (default) 1 – Force D+/D– detection	
5	EN_ICO	R/W	Yes	No	Input Current Optimization (ICO) Algorithm Control: 0 – Disable ICO 1 – Enable ICO (default)	
4	IINDPM[4]	R/W	Yes	No	1600 mA	Input Current Limit: Offset: 500 mA Range: 500mA – 3300mA Default: 3000mA Note: IINDPM > 3300 mA (1Ch) clamped to 3300mA. Actual input current limit is lower of I2C, ICO_ILIM,ILIM pin or D+/D-.
3	IINDPM[3]	R/W	Yes	No	800 mA	
2	IINDPM[2]	R/W	Yes	No	400 mA	
1	IINDPM[1]	R/W	Yes	No	200 mA	
0	IINDPM[0]	R/W	Yes	No	100 mA	

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8.5.5 Precharge and Termination Current Limit Register (Address = 04h) [reset = 22h]

REG04 is shown in Figure 38 and described in Table 14.

Return to Summary Table.

Figure 38. REG04 Register

Bit	7	6	5	4	3	2	1	0
Reset	2h				2h			
Field	IPRECHG[3:0]				ITERM[3:0]			

Table 14. REG04 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	IPRECHG[3]	R/W	Yes	Yes	400 mA	Precharge Current Limit: Offset: 50 mA Range: 50mA – 800mA Default: 150mA
6	IPRECHG[2]	R/W	Yes	Yes	200 mA	
5	IPRECHG[1]	R/W	Yes	Yes	100 mA	
4	IPRECHG[0]	R/W	Yes	Yes	50 mA	
3	ITERM[3]	R/W	Yes	Yes	400 mA	Termination Current Limit: Offset: 50 mA Range: 50mA – 800mA Default: 150mA
2	ITERM[2]	R/W	Yes	Yes	200 mA	
1	ITERM[1]	R/W	Yes	Yes	100 mA	
0	ITERM[0]	R/W	Yes	Yes	50 mA	

8.5.6 Charger Control 1 Register (Address = 05h) [reset = 9Dh]

REG05 is shown in Figure 39 and described in Table 15.

Return to Summary Table.

Figure 39. REG05 Register

Bit	7	6	5	4	3	2	1	0
Reset	1h	0h	1h		1h	2h		1h
Field	EN_TERM	STAT_DIS	WATCHDOG[1:0]		EN_TIMER	CHG_TIMER[1:0]		TMR2X_EN

Table 15. REG05 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	EN_TERM	R/W	Yes	Yes	Termination Control: 0 – Disable termination 1 – Enable termination (default)
6	STAT_DIS	R/W	Yes	Yes	STAT Pin Disable: 0 – Enable STAT pin function (default) 1 – Disable STAT pin function
5	WATCHDOG[1]	R/W	Yes	Yes	I2C Watchdog Timer Settings: 00 – Disable WD Timer 01 – 40s (default) 10 – 80s 11 – 160s
4	WATCHDOG[0]	R/W	Yes	Yes	
3	EN_TIMER	R/W	Yes	Yes	Charging Safety Timer Enable 0 – Disable 1 – Enable (Default)
2	CHG_TIMER[1]	R/W	Yes	Yes	Fast Charge Timer Setting 00 – 5 hrs 01 – 8 hrs 10 – 12 hrs (Default) 11 – 20 hrs
1	CHG_TIMER[0]	R/W	Yes	Yes	
0	TMR2X_EN	R/W	Yes	Yes	Safety Timer during DPM or TREG 0 – Safety timer always count normally 1 – Safety timer slowed by 2X during input DPM or TREG (Default)

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8.5.7 Charger Control 2 Register (Address = 06h) [reset = 7Dh]

REG06 is shown in Figure 40 and described in Table 16.

Return to Summary Table.

Figure 40. REG06 Register

Bit	7	6	5	4	3	2	1	0
Reset	0h	1h	3h		1h	1h	0h	
Field	EN_OTG	AUTO_INDET_EN	TREG[1:0]		EN_CHG	BATLOWV	VRECHG[1:0]	

Table 16. REG06 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	EN_OTG	R/W	Yes	Yes	Buck (OTG) Mode control: 0 – Disable OTG (default) 1 – Enable OTG Note: If EN_OTG and EN_CHG are set simultaneously, EN_CHG takes priority	
6	AUTO_INDET_EN	R/W	Yes	Yes	Automatic D+/D– Detection Enable: 0 – Disable D+/D–L detection when VBUS plugs in 1 – Enable D+/D– detection when VBUS plugs in (default)	
5	TREG[1]	R/W	Yes	Yes	Thermal Regulation Threshold 00 – 60°C 01 – 80°C 10 – 100°C 11 – 120°C (Default)	
4	TREG[0]	R/W	Yes	Yes		
3	EN_CHG	R/W	Yes	Yes	Charger Enable Configuration 0 – Charge Disable 1 – Charge Enable (default) Note: If EN_OTG and EN_CHG are set simultaneously, EN_CHG takes priority	
2	BATLOWV	R/W	Yes	Yes	Battery precharge to fast-charge threshold: 0 – 5.6V 1 – 6.0V (default)	
1	VRECHG[1]	R/W	Yes	No	200 mV	Battery Recharge Threshold Offset (below VREG): Offset: 100mV Range: 100mV – 400mV Default: 200mV
0	VRECHG[0]	R/W	Yes	No	100 mV	

8.5.8 Charger Control 3 Register (Address = 07h) [reset = 02h]

REG07 is shown in Figure 41 and described in Table 17.

Return to Summary Table.

Figure 41. REG07 Register

Bit	7	6	5	4	3	2	1	0
Reset	0h	0h	0h		2h			
Field	PFM_DIS	WD_RST	TOPOFF_TIMER[1:0]		SYS_MIN[3:0]			

Table 17. REG07 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	PFM_DIS	R/W	Yes	No	PFM Mode Disable control: 0 – Enable PFM operation (default) 1 – Disable PFM operation	
6	WD_RST	R/W	Yes	Yes	I2C Watchdog Timer Reset: 0 – Normal 1 – Reset (Bit goes back to 0 after timer reset)	
5	TOPOFF_TIMER[1]	R/W	Yes	Yes	Top-off Timer Control : 00 – Disabled (default) 01 – 15 mins 10 – 30 mins 11 – 45 mins	
4	TOPOFF_TIMER[0]	R/W	Yes	Yes		
3	SYS_MIN[3]	R/W	Yes	No	800 mV	Minimum System Voltage Limit Offset: 6.0 V Range: 6.0 V – 7.5V Default: 6.2 V
2	SYS_MIN[2]	R/W	Yes	No	400 mV	
1	SYS_MIN[2]	R/W	Yes	No	200 mV	
0	SYS_MIN[0]	R/W	Yes	No	100 mV	

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8.5.9 Charger Control 4 Register (Address = 08h) [reset = 0Dh]

REG08 is shown in Figure 42 and described in Table 18.

Return to Summary Table.

Figure 42. REG08 Register

Bit	7	6	5	4	3	2	1	0
Reset	0h		0h	1h		1h	1h	
Field	BHOT[1:0]		BCOLD	JEITA_VSET[1:0]		JEITA_ISETH	JEITA_ISETC[1:0]	

Table 18. REG08 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	BHOT[1]	R/W	Yes	Yes	OTG Mode TS HOT Temperature Threshold: 00 – VBHOT1 threshold (34.75%) (default) 01 – VBHOT0 threshold (37.75%) 10 – VBHOT2 threshold (31.25%) 11 – Disable OTG mode thermal protection
6	BHOT[0]	R/W	Yes	Yes	
5	BCOLD	R/W	Yes	Yes	OTG Mode TS COLD Temperature Threshold: 0 – VBCOLD0 threshold (77%) (default) 1 – VBCOLD1 threshold (80%)
4	JEITA_VSET[1]	R/W	Yes	Yes	JEITA High Temp. (45C – 60C) Voltage Setting: 00 – Charge Suspend 01 – Set VREG to 8.0V (default) 10 – Set VREG to 8.3V 11 – VREG unchanged
3	JEITA_VSET[0]	R/W	Yes	Yes	
2	JEITA_ISETH	R/W	Yes	Yes	JEITA High Temp. (45C – 60C) Current Setting (percentage with respect to ICHG REG01[5:0]): 0 – 40% of ICHG 1 – 100% of ICHG (default)
1	JEITA_ISETC[1]	R/W	Yes	Yes	JEITA Low Temp. (0C – 10C) Current Setting (percentage with respect to ICHG REG01[5:0]): 00 – Charge Suspend 01 – 20% of ICHG (default) 10 – 40% of ICHG 11 – 100% of ICHG
0	JEITA_ISETC[0]	R/W	Yes	Yes	

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8.5.10 OTG Control Register (Address = 09h) [reset = F6h]

REG09 is shown in Figure 43 and described in Table 19.

Return to Summary Table.

Figure 43. REG09 Register

Bit	7	6	5	4	3	2	1	0
Reset	Fh				6h			
Field	OTG_ILIM[3:0]				OTG_VLIM[3:0]			

Table 19. REG09 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	OTG_ILIM[3]	R/W	Yes	Yes	800 mA	Buck (OTG) Mode Current Limit: Offset: 0.5A Range: 0.5A – 2.0A Default: 2.0A
6	OTG_ILIM[2]	R/W	Yes	Yes	400 mA	
5	OTG_ILIM[1]	R/W	Yes	Yes	200 mA	
4	OTG_ILIM[0]	R/W	Yes	Yes	100 mA	
3	OTG_VLIM[3]	R/W	Yes	Yes	800 mV	Buck (OTG) Mode Regulation Voltage: Offset: 4.5V Range: 4.5V – 5.5V Default: 5.1V Note: Values above 5.5V (Ah) will be clamped to 5.5V
2	OTG_VLIM[2]	R/W	Yes	Yes	400 mV	
1	OTG_VLIM[1]	R/W	Yes	Yes	200 mV	
0	OTG_VLIM[0]	R/W	Yes	Yes	100 mV	

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8.5.11 ICO Current Limit in Use Register (Address = 0Ah) [reset = XXh]

REG0A is shown in Figure 44 and described in Table 20.

Return to Summary Table.

Figure 44. REG0A Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	X	X	X	X	X
Field	RESERVED	RESERVED	RESERVED	ICO_ILIM[4:0]				

Table 20. REG0A Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	RESERVED	R	No	No	Reserved bit always reads 0	
6	RESERVED	R	No	No	Reserved bit always reads 0	
5	RESERVED	R	No	No	Reserved bit always reads 0	
4	ICO_ILIM[4]	R	No	No	1600 mA	Input Current Limit in use when ICO is enabled: Offset: 500 mA Range: 500mA – 3300mA
3	ICO_ILIM[3]	R	No	No	800 mA	
2	ICO_ILIM[2]	R	No	No	400 mA	
1	ICO_ILIM[1]	R	No	No	200 mA	
0	ICO_ILIM[0]	R	No	No	100 mA	

8.5.12 Charger Status 1 Register (Address = 0Bh) [reset = XXh]

REG0B is shown in Figure 45 and described in Table 21.

Return to Summary Table.

Figure 45. REG0B Register

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
Field	Reserved	IINDPM_STAT	VINDPM_STAT	TREG_STAT	WD_STAT	CHRG_STAT[2:0]		

Table 21. REG0B Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	Reserved	R	No	No	Reserved bit always reads 0
6	IINDPM_STAT	R	No	No	IINDPM Status: 0 – Normal 1 – In IINDPM Regulation (ILIM pin or IINDPM register)
5	VINDPM_STAT	R	No	No	VINDPM Status: 0 – Normal 1 – In VINDPM Regulation
4	TREG_STAT	R	No	No	IC Thermal regulation Status: 0 – Normal 1 – In Thermal Regulation
3	WD_STAT	R	No	No	I2C Watchdog Timer Status bit: 0 – Normal 1 – WD Timer expired
2	CHRG_STAT[2]	R	No	No	Charge Status bits: 000 – Not Charging 001 – Trickle Charge (VBAT < VBAT_SHORT) 010 – Pre-charge (VBAT_UVLO_RISING < VBAT < VBAT_LOWV) 011 – Fast-charge (CC mode) 100 – Taper Charge (CV mode) 101 – Top-off Timer Charging 110 – Charge Termination Done 111 – Reserved
1	CHRG_STAT[1]	R	No	No	
0	CHRG_STAT[0]	R	No	No	

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8.5.13 Charger Status 2 Register (Address = 0Ch) [reset = XXh]

REG0C is shown in Figure 46 and described in Table 22.

Return to Summary Table.

Figure 46. REG0C Register

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	0	X	X	X
Field	PG_STAT	VBUS_STAT[2:0]			RESERVED	ICO_STAT[1]	ICO_STAT[0]	VSYS_STAT

Table 22. REG0C Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	PG_STAT	R	No	No	Power Good Status: 0 – Not Power Good 1 – Power Good
6	VBUS_STAT[2]	R	No	No	VBUS Detection Status 000 – No Input 001 – USB Host SDP 010 - USB CDP (1.5 A) 011 – Adapter (3.0A) 100 – POORSRC detected 7 consecutive times 101 - Unknown Adapter (500 mA) 110 - Non-standard Adapter (1 A/2 A/2.1 A/2.4 A) 111 – OTG
5	VBUS_STAT[1]	R	No	No	
4	VBUS_STAT[0]	R	No	No	
3	RESERVED	R	No	No	Reserved bit always reads 0h
2	ICO_STAT[1]	R	No	No	Input Current Optimizer (ICO) Status: 00 – ICO Disabled 01 – ICO Optimization is in progress 10 – Maximum input current detected 11 – Reserved
1	ICO_STAT[0]	R	No	No	
0	VSYS_STAT	R	No	No	VSYS Regulation Status: 0 – Not in SYS_MIN regulation (BAT > VSYS_MIN) 1 – In SYS_MIN regulation (BAT < VSYS_MIN)

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8.5.14 NTC Status Register (Address = 0Dh) [reset = 0Xh]

REG0D is shown in Figure 47 and described in Table 23.

Return to Summary Table.

Figure 47. REG0D Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	X	X	X
Field	RESERVED		RESERVED	RESERVED	RESERVED	TS_STAT[2:0]		

Table 23. REG0D Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	RESERVED	R	Yes	No	Reserved bit always reads 0h
6	RESERVED	R	Yes	No	Reserved bit always reads 0h
5	RESERVED	R	Yes	No	Reserved bit always reads 0h
4	RESERVED	R	Yes	No	Reserved bit always reads 0h
3	RESERVED	R	Yes	No	Reserved bit always reads 0h
2	TS_STAT[2]	R	No	No	NTC (TS) Status: 000 – Normal 010 – TS Warm 011 – TS Cool 101 – TS Cold 110 – TS Hot
1	TS_STAT[1]	R	No	No	
0	TS_STAT[0]	R	No	No	

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8.5.15 FAULT Status Register (Address = 0Eh) [reset = XXh]

REG0E is shown in Figure 48 and described in Table 24.

Return to Summary Table.

Figure 48. REG0E Register

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	0	0	0	X
Field	VBUS_OVP_STAT	TSHUT_STAT	BATOVP_STAT	TMR_STAT	RESERVED	RESERVED	RESERVED	Reserved

Table 24. REG0E Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	VBUS_OVP_STAT	R	No	No	Input over-voltage Status: 0 – Normal 1 – Device in over-voltage protection
6	TSHUT_STAT	R	No	No	IC Temperature shutdown Status: 0 – Normal 1 – Device in thermal shutdown protection
5	BATOVP_STAT	R	No	No	Battery over-voltage Status: 0 – Normal 1 – BATOVP (VBAT > VBATOVP)
4	TMR_STAT	R	No	No	Charge Safety timer Status: 0 – Normal 1 – Charge Safety timer expired
3	RESERVED	R	No	No	Reserved bit always reads 0h
2	RESERVED	R	No	No	Reserved bit always reads 0h
1	RESERVED	R	No	No	Reserved bit always reads 0h
0	RESERVED	R	No	No	Reserved bit always reads 0h

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8.5.16 Charger Flag 1 Register (Address = 0Fh) [reset = 00h]

REG0F is shown in Figure 49 and described in Table 25.

Return to Summary Table.

Figure 49. REG0F Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	Reserved	IINDPM_FLAG	VINDPM_FLAG	TREG_FLAG	WD_FLAG	RESERVED	RESERVED	CHRG_FLAG

Table 25. REG0F Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	Reserved	R	Yes	No	Reserved bit always reads 0
6	IINDPM_FLAG	R	Yes	No	IINDPM Regulation $\overline{\text{INT}}$ Flag: 0 – Normal 1 – IINDPM signal rising edge detected
5	VINDPM_FLAG	R	Yes	No	VINDPM regulation $\overline{\text{INT}}$ Flag: 0 – Normal 1 – VINDPM signal rising edge detected
4	TREG_FLAG	R	Yes	No	IC Temperature Regulation $\overline{\text{INT}}$ Flag: 0 – Normal 1 – TREG signal rising edge detected
3	WD_FLAG	R	Yes	No	I2C Watchdog $\overline{\text{INT}}$ Flag: 0 – Normal 1 – WD_STAT signal rising edge detected
2	RESERVED	R	Yes	No	Reserved bit always reads 0h
1	RESERVED	R	Yes	No	Reserved bit always reads 0h
0	CHRG_FLAG	R	Yes	No	Charge Status $\overline{\text{INT}}$ Flag: 0 – Normal 1 – CHRG_STAT[2:0] bits changed (transition to any state)

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8.5.17 Charger Flag 2 Register (Address = 10h) [reset = 00h]

REG10 is shown in Figure 50 and described in Table 26.

Return to Summary Table.

Figure 50. REG10 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	PG_FLAG	RESERVED	RESERVED	VBUS_FLAG	RESERVED	TS_FLAG	ICO_FLAG	VSYS_FLAG

Table 26. REG10 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	PG_FLAG	R	Yes	No	Power Good $\overline{\text{INT}}$ Flag: 0 – Normal 1 – PG signal toggle detected
6	RESERVED	R	Yes	No	Reserved bit always reads 0h
5	RESERVED	R	Yes	No	Reserved bit always reads 0h
4	VBUS_FLAG	R	Yes	No	VBUS Status $\overline{\text{INT}}$ Flag: 0 – Normal 1 – VBUS_STAT[2:0] bits changed (transition to any state)
3	RESERVED	R	Yes	No	Reserved bit always reads 0h
2	TS_FLAG	R	Yes	No	TS Status $\overline{\text{INT}}$ Flag: 0 – Normal 1 – TS_STAT[2:0] bits changed (transition to any state)
1	ICO_FLAG	R	Yes	No	Input Current Optimizer (ICO) $\overline{\text{INT}}$ Flag: 0 – Normal 1 – ICO_STAT[1:0] changed (transition to any state)
0	VSYS_FLAG	R	Yes	No	VSYS Regulation $\overline{\text{INT}}$ Flag: 0 – Normal 1 – Entered or exited SYS_MIN regulation

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8.5.18 FAULT Flag Register (Address = 11h) [reset = 00h]

REG11 is shown in Figure 51 and described in Table 27.

Return to Summary Table.

Figure 51. REG11 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	VBUS_OVP_FLAG	TSHUT_FLAG	BATOVP_FLAG	TMR_FLAG	RESERVED	RESERVED	RESERVED	OTG_FLAG

Table 27. REG11 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	VBUS_OVP_FLAG	R	Yes	No	Input over-voltage $\overline{\text{INT}}$ Flag: 0 – Normal 1 – Entered VBUS_OVP Fault
6	TSHUT_FLAG	R	Yes	No	IC Temperature shutdown $\overline{\text{INT}}$ Flag: 0 – Normal 1 – Entered TSHUT Fault
5	BATOVP_FLAG	R	Yes	No	Battery over-voltage $\overline{\text{INT}}$ Flag: 0 – Normal 1 – Entered BATOVP Fault
4	TMR_FLAG	R	Yes	No	Charge Safety timer Fault $\overline{\text{INT}}$ Flag: 0 – Normal 1 – Charge Safety timer expired rising edge detected
3	RESERVED	R	Yes	No	Reserved bit always reads 0
2	RESERVED	R	Yes	No	Reserved bit always reads 0h
1	RESERVED	R	Yes	No	Reserved bit always reads 0h
0	OTG_FLAG	R	Yes	No	OTG Buck Mode Fault $\overline{\text{INT}}$ Flag: 0 – Normal 1 – Entered OTG_STAT (OTG Fault)

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8.5.19 Charger Mask 1 Register (Address = 12h) [reset = 00h]

REG12 is shown in Figure 52 and described in Table 28.

Return to Summary Table.

Figure 52. REG12 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	ADC_DONE_MASK	IINDPM_MASK	VINDPM_MASK	TREG_MASK	WD_MASK	RESERVED	RESERVED	CHRG_MASK

Table 28. REG12 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	ADC_DONE_MASK	R/W	Yes	No	ADC Conversion $\overline{\text{INT}}$ Mask Flag (only one-shot mode) 0 – ADC_DONE does produce $\overline{\text{INT}}$ pulse 1 – ADC_DONE does produce not $\overline{\text{INT}}$ pulseReserved bit always reads 0
6	IINDPM_MASK	R/W	Yes	No	IINDPM Regulation $\overline{\text{INT}}$ Mask 0 – IINDPM entry produces $\overline{\text{INT}}$ pulse 1 – IINDPM entry does not produce $\overline{\text{INT}}$ pulse
5	VINDPM_MASK	R/W	Yes	No	VINDPM Regulation $\overline{\text{INT}}$ Mask 0 – VINDPM entry produces $\overline{\text{INT}}$ pulse 1 – VINDPM entry not produce $\overline{\text{INT}}$ pulse
4	TREG_MASK	R/W	Yes	No	IC Temperature Regulation $\overline{\text{INT}}$ Mask 0 – TREG entry produces $\overline{\text{INT}}$ pulse 1 – TREG entry produce $\overline{\text{INT}}$ pulse
3	WD_MASK	R/W	Yes	No	I2C Watchdog Timer $\overline{\text{INT}}$ Mask 0 – WD_STAT rising edge produces $\overline{\text{INT}}$ pulse 1 – WD_STAT rising edge does not produce $\overline{\text{INT}}$
2	RESERVED	R	Yes	No	Reserved bit always reads 0h
1	RESERVED	R	Yes	No	Reserved bit always reads 0h
0	CHRG_MASK	R/W	Yes	No	Charge Status $\overline{\text{INT}}$ Mask 0 – CHRG_STAT[2:0] bit change produces $\overline{\text{INT}}$ 1 – CHRG_STAT[2:0] bit change does not produce $\overline{\text{INT}}$ pulse

8.5.20 Charger Mask 2 Register (Address = 13h) [reset = 00h]

REG13 is shown in Figure 53 and described in Table 29.

Return to Summary Table.

Figure 53. REG13 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	PG_MASK	RESERVED	RESERVED	VBUS_MASK	RESERVED	TS_MASK	ICO_MASK	VSYS_MASK

Table 29. REG13 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	PG_MASK	R/W	Yes	No	Power Good $\overline{\text{INT}}$ Mask: 0 – PG toggle produces $\overline{\text{INT}}$ pulse 1 – PG toggle does not produce $\overline{\text{INT}}$ pulse
6	RESERVED	R	Yes	No	Reserved bit always reads 0h
5	RESERVED	R	Yes	No	Reserved bit always reads 0h
4	VBUS_MASK	R/W	Yes	No	VBUS Status $\overline{\text{INT}}$ Mask: 0 – VBUS_STAT[2:0] bit change produces $\overline{\text{INT}}$ 1 – VBUS_STAT[2:0] bit change does not produces $\overline{\text{INT}}$
3	RESERVED	R	Yes	No	Reserved bit always reads 0h
2	TS_MASK	R/W	Yes	No	TS Status $\overline{\text{INT}}$ Mask: 0 – TS_STAT[2:0] bit change produces $\overline{\text{INT}}$ 1 – TS_STAT[2:0] bit change does not produces $\overline{\text{INT}}$ pulse
1	ICO_MASK	R/W	Yes	No	Input Current Optimizer (ICO) $\overline{\text{INT}}$ Mask: 0 – ICO_STAT rising edge produces $\overline{\text{INT}}$ 1 – ICO_STAT rising edge does not produce $\overline{\text{INT}}$
0	VSYS_MASK	R/W	Yes	No	VSYS Regulation $\overline{\text{INT}}$ Mask: 0 – Entering or exiting SYS_MIN produces $\overline{\text{INT}}$ 1 – Entering or exiting SYS_MIN does not produce $\overline{\text{INT}}$

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8.5.21 FAULT Mask Register (Address = 14h) [reset = 00h]

REG14 is shown in Figure 54 and described in Table 30.

Return to Summary Table.

Figure 54. REG14 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	VBUS_OVP_MASK	TSHUT_MASK	BATOVP_MASK	TMR_MASK	SYS_SHORT_MASK	RESERVED	RESERVED	OTG_MASK

Table 30. REG14 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	VBUS_OVP_MASK	R/W	Yes	No	Input over-voltage $\overline{INT}$ Mask: 0 – VBUS_OVP rising edge produces $\overline{INT}$ pulse 1 – VBUS_OVP rising edge does not produce $\overline{INT}$ pulse
6	TSHUT_MASK	R/W	Yes	No	Thermal Shutdown $\overline{INT}$ Mask: 0 – TSHUT rising edge produces $\overline{INT}$ pulse 1 – TSHUT rising edge does not produce $\overline{INT}$ pulse
5	BATOVP_MASK	R/W	Yes	No	Battery overvoltage $\overline{INT}$ Mask: 0 – BATOVP rising edge produces $\overline{INT}$ pulse 1 – BATOVP rising edge does not produce $\overline{INT}$ pulse
4	TMR_MASK	R/W	Yes	No	Charge Safety Timer Fault $\overline{INT}$ Mask: 0 – Timer expired rising edge produces $\overline{INT}$ pulse 1 – Timer expired rising edge does not produce $\overline{INT}$ pulse
3	SYS_SHORT_MASK	R/W	Yes	No	System Short Fault $\overline{INT}$ Mask: 0 – System short rising edge produces $\overline{INT}$ pulse 1 – System short rising edge does not produce $\overline{INT}$ pulse
2	RESERVED	R	Yes	No	Reserved bit always reads 0h
1	RESERVED	R	Yes	No	Reserved bit always reads 0h
0	OTG_MASK	R/W	Yes	No	OTG Buck Mode Fault $\overline{INT}$ Mask: 0 – OTG_STAT event produces $\overline{INT}$ 1 – OTG_STAT event does not produce $\overline{INT}$

8.5.22 ADC Control Register (Address = 15h) [reset = 30h]

REG15 is shown in Figure 55 and described in Table 31.

Return to Summary Table.

Figure 55. REG15 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	1	1	0	0	0	0
Field	ADC_EN	ADC_RATE	ADC_SAMPLE[1:0]		RESERVED	RESERVED	RESERVED	RESERVED

Table 31. REG15 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	ADC_EN	R/W	Yes	Yes	ADC Control: 0 – Disable ADC 1 – Enable ADC
6	ADC_RATE	R/W	Yes	No	0 – Continuous conversion 1 – One-shot conversion
5	ADC_SAMPLE[1]	R/W	Yes	No	Sample Speed of ADC: 00 – 15 bit effective resolution 01 – 14 bit effective resolution 10 – 13 bit effective resolution 11 – 12 bit effective resolution
4	ADC_SAMPLE[0]	R/W	Yes	No	
3	RESERVED	R	Yes	No	Reserved bit always reads 0h
2	RESERVED	R	Yes	No	Reserved bit always reads 0h
1	RESERVED	R	Yes	No	Reserved bit always reads 0h
0	RESERVED	R	Yes	No	Reserved bit always reads 0h

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8.5.23 ADC Function Disable Register (Address = 16h) [reset = 00h]

REG16 is shown in Figure 56 and described in Table 32.

Return to Summary Table.

Figure 56. REG16 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	1	0
Field	IBUS_ADC_DIS	ICHG_ADC_DIS	VBUS_ADC_DIS	VBAT_ADC_DIS	VSYS_ADC_DIS	TS_ADC_DIS	Reserved	TDIE_ADC_DIS

Table 32. REG16 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	IBUS_ADC_DIS	R/W	Yes	No	0 – Enable conversion 1 – Disable conversion
6	ICHG_ADC_DIS	R/W	Yes	No	0 – Enable conversion 1 – Disable conversion
5	VBUS_ADC_DIS	R/W	Yes	No	0 – Enable conversion 1 – Disable conversion
4	VBAT_ADC_DIS	R/W	Yes	No	0 – Enable conversion 1 – Disable conversion
3	VSYS_ADC_DIS	R/W	Yes	No	0 – Enable conversion 1 – Disable conversion
2	TS_ADC_DIS	R/W	Yes	No	0 – Enable conversion 1 – Disable conversion
1	RESERVED	R	Yes	No	Reserved bit always reads 1h
0	TDIE_ADC_DIS	R/W	Yes	No	0 – Enable conversion 1 – Disable conversion

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8.5.24 IBUS ADC 1 Register (Address = 17h) [reset = 00h]

REG17 is shown in Figure 57 and described in Table 33.

Return to Summary Table.

Figure 57. REG17 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	IBUS_ADC[15:8]							

Table 33. REG17 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	IBUS_ADC[15]	R	Yes	No	Sign bit: overall results reported in two's complement.	
6	IBUS_ADC[14]	R	Yes	No	16384 mA	
5	IBUS_ADC[13]	R	Yes	No	8192 mA	
4	IBUS_ADC[12]	R	Yes	No	4096 mA	
3	IBUS_ADC[11]	R	Yes	No	2048 mA	VBUS Current Reading (positive current flows into VBUS pin, negative current flows out ot VBUS pin): Range: 0A – 4A
2	IBUS_ADC[10]	R	Yes	No	1024 mA	
1	IBUS_ADC[9]	R	Yes	No	512 mA	
0	IBUS_ADC[8]	R	Yes	No	256 mA	

8.5.25 IBUS ADC 0 Register (Address = 18h) [reset = 00h]

REG18 is shown in Figure 58 and described in Table 34.

Return to Summary Table.

Figure 58. REG18 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	IBUS_ADC[7:0]							

Table 34. REG18 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	IBUS_ADC[7]	R	Yes	No	128 mA	VBUS Current Reading (positive current flows into VBUS pin, negative current flows out ot VBUS pin): Range: 0A – 4A
6	IBUS_ADC[6]	R	Yes	No	64 mA	
5	IBUS_ADC[5]	R	Yes	No	32 mA	
4	IBUS_ADC[4]	R	Yes	No	16 mA	
3	IBUS_ADC[3]	R	Yes	No	8 mA	
2	IBUS_ADC[2]	R	Yes	No	4 mA	
1	IBUS_ADC[1]	R	Yes	No	2 mA	
0	IBUS_ADC[0]	R	Yes	No	1 mA	

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8.5.26 ICHG ADC 1 Register (Address = 19h) [reset = 00h]

REG19 is shown in Figure 59 and described in Table 35.

Return to Summary Table.

Figure 59. REG19 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	RESERVED	ICHG_ADC[14:8]						

Table 35. REG19 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	Reserved	R	Yes	No	Reserved register always reads 0h.	
6	ICHG_ADC[14]	R	Yes	No	16384 mA	
5	ICHG_ADC[13]	R	Yes	No	8192 mA	
4	ICHG_ADC[12]	R	Yes	No	4096 mA	
3	ICHG_ADC[11]	R	Yes	No	2048 mA	Charge Current Reading: Range: 0A – 4A
2	ICHG_ADC[10]	R	Yes	No	1024 mA	
1	ICHG_ADC[9]	R	Yes	No	512 mA	
0	ICHG_ADC[8]	R	Yes	No	256 mA	

8.5.27 ICHG ADC 0 Register (Address = 1Ah) [reset = 00h]

REG1A is shown in Figure 60 and described in Table 36.

Return to Summary Table.

Figure 60. REG1A Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	ICHG_ADC[7:0]							

Table 36. REG1A Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	ICHG_ADC[7]	R	Yes	No	128 mA	Charge Current Reading: Range: 0A – 4A
6	ICHG_ADC[6]	R	Yes	No	64 mA	
5	ICHG_ADC[5]	R	Yes	No	32 mA	
4	ICHG_ADC[4]	R	Yes	No	16 mA	
3	ICHG_ADC[3]	R	Yes	No	8 mA	
2	ICHG_ADC[2]	R	Yes	No	4 mA	
1	ICHG_ADC[1]	R	Yes	No	2 mA	
0	ICHG_ADC[0]	R	Yes	No	1 mA	

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8.5.28 VBUS ADC 1 Register (Address = 1Bh) [reset = 00h]

REG1B is shown in Figure 61 and described in Table 37.

Return to Summary Table.

Figure 61. REG1B Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	VBUS_ADC[15:8]							

Table 37. REG1B Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	VBUS_ADC[15]	R	Yes	No	Sign bit: overall results reported in two's complement.	
6	VBUS_ADC[14]	R	Yes	No	16384 mV	
5	VBUS_ADC[13]	R	Yes	No	8192 mV	VBUS Voltage reading Range: 0V – 10V
4	VBUS_ADC[12]	R	Yes	No	4096 mV	
3	VBUS_ADC[11]	R	Yes	No	2048 mV	
2	VBUS_ADC[10]	R	Yes	No	1024 mV	
1	VBUS_ADC[9]	R	Yes	No	512 mV	
0	VBUS_ADC[8]	R	Yes	No	256 mV	

8.5.29 VBUS ADC 0 Register (Address = 1Ch) [reset = 00h]

REG1C is shown in Figure 62 and described in Table 38.

Return to Summary Table.

Figure 62. REG1C Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	VBUS_ADC[7:0]							

Table 38. REG1C Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	VBUS_ADC[7]	R	Yes	No	128 mV	VBUS Voltage Reading: Range: 0V – 10V
6	VBUS_ADC[6]	R	Yes	No	64 mV	
5	VBUS_ADC[5]	R	Yes	No	32 mV	
4	VBUS_ADC[4]	R	Yes	No	16 mV	
3	VBUS_ADC[3]	R	Yes	No	8 mV	
2	VBUS_ADC[2]	R	Yes	No	4 mV	
1	VBUS_ADC[1]	R	Yes	No	2 mV	
0	VBUS_ADC[0]	R	Yes	No	1 mV	

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8.5.30 VBAT ADC 1 Register (Address = 1Dh) [reset = 00h]

REG1D is shown in Figure 63 and described in Table 39.

Return to Summary Table.

Figure 63. REG1D Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	VBAT_ADC[15:8]							

Table 39. REG1D Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	VBAT_ADC[15]	R	Yes	No	Sign bit: overall results reported in two's complement.	
6	VBAT_ADC[14]	R	Yes	No	16384 mV	
5	VBAT_ADC[13]	R	Yes	No	8192 mV	VBAT Voltage reading: Range: 0V – 10V
4	VBAT_ADC[12]	R	Yes	No	4096 mV	
3	VBAT_ADC[11]	R	Yes	No	2048 mV	
2	VBAT_ADC[10]	R	Yes	No	1024 mV	
1	VBAT_ADC[9]	R	Yes	No	512 mV	
0	VBAT_ADC[8]	R	Yes	No	256 mV	

8.5.31 VBAT ADC 0 Register (Address = 1Eh) [reset = 00h]

REG1E is shown in Figure 64 and described in Table 40.

Return to Summary Table.

Figure 64. REG1E Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	VBAT_ADC[7:0]							

Table 40. REG1E Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	VBAT_ADC[7]	R	Yes	No	128 mV	VBAT Voltage reading: Range: 0V – 10V
6	VBAT_ADC[6]	R	Yes	No	64 mV	
5	VBAT_ADC[5]	R	Yes	No	32 mV	
4	VBAT_ADC[4]	R	Yes	No	16 mV	
3	VBAT_ADC[3]	R	Yes	No	8 mV	
2	VBAT_ADC[2]	R	Yes	No	4 mV	
1	VBAT_ADC[1]	R	Yes	No	2 mV	
0	VBAT_ADC[0]	R	Yes	No	1 mV	

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8.5.32 VSYS ADC 1 Register (Address = 1Fh) [reset = 00h]

REG1F is shown in Figure 65 and described in Table 41.

Return to Summary Table.

Figure 65. REG1F Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	VSYS_ADC[15:8]							

Table 41. REG1F Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	VSYS_ADC[15]	R	Yes	No	Sign bit: overall results reported in two's complement.	
6	VSYS_ADC[14]	R	Yes	No	16384 mV	VSYS Voltage reading: Range: 0V – 10V
5	VSYS_ADC[13]	R	Yes	No	8192 mV	
4	VSYS_ADC[12]	R	Yes	No	4096 mV	
3	VSYS_ADC[11]	R	Yes	No	2048 mV	
2	VSYS_ADC[10]	R	Yes	No	1024 mV	
1	VSYS_ADC[9]	R	Yes	No	512 mV	
0	VSYS_ADC[8]	R	Yes	No	256 mV	

8.5.33 VSYS ADC 0 Register (Address = 20h) [reset = 00h]

REG20 is shown in Figure 66 and described in Table 42.

Return to Summary Table.

Figure 66. REG20 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	VSYS_ADC[7:0]							

Table 42. REG20 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	VSYS_ADC[7]	R	Yes	No	128 mV	VSYS Voltage reading: Range: 0V – 10V
6	VSYS_ADC[6]	R	Yes	No	64 mV	
5	VSYS_ADC[5]	R	Yes	No	32 mV	
4	VSYS_ADC[4]	R	Yes	No	16 mV	
3	VSYS_ADC[3]	R	Yes	No	8 mV	
2	VSYS_ADC[2]	R	Yes	No	4 mV	
1	VSYS_ADC[1]	R	Yes	No	2 mV	
0	VSYS_ADC[0]	R	Yes	No	1 mV	

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8.5.34 TS ADC 1 Register (Address = 21h) [reset = 00h]

REG21 is shown in Figure 67 and described in Table 43.

Return to Summary Table.

Figure 67. REG21 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	TS_ADC[15:8]							

Table 43. REG21 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	TS_ADC[15]	R	Yes	No	Sign bit: overall results reported in two's complement.	
6	TS_ADC[14]	R	Yes	No		
5	TS_ADC[13]	R	Yes	No		
4	TS_ADC[12]	R	Yes	No		
3	TS_ADC[11]	R	Yes	No		
2	TS_ADC[10]	R	Yes	No		
1	TS_ADC[9]	R	Yes	No	50.0 %	TS as percentage of REGN reading: Range: 0% – 94.9%
0	TS_ADC[8]	R	Yes	No	25.0 %	

8.5.35 TS ADC 0 Register (Address = 22h) [reset = 00h]

REG22 is shown in Figure 68 and described in Table 44.

Return to Summary Table.

Figure 68. REG22 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	TS_ADC[7:0]							

Table 44. REG22 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	TS_ADC[7]	R	Yes	No	12.50 %	TS as percentage of REGN reading: Range: 0% – 94.9%
6	TS_ADC[6]	R	Yes	No	6.25 %	
5	TS_ADC[5]	R	Yes	No	3.125 %	
4	TS_ADC[4]	R	Yes	No	1.563 %	
3	TS_ADC[3]	R	Yes	No	0.781 %	
2	TS_ADC[2]	R	Yes	No	0.391 %	
1	TS_ADC[1]	R	Yes	No	0.195 %	
0	TS_ADC[0]	R	Yes	No	0.098 %	

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8.5.36 TDIE ADC 1 Register (Address = 23h) [reset = 00h]

REG23 is shown in Figure 69 and described in Table 45.

Return to Summary Table.

Figure 69. REG23 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	TDIE_ADC[15:8]							

Table 45. REG23 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	TDIE_ADC[15]	R	Yes	No	Sign bit: overall results reported in two's complement.	
6	TDIE_ADC[14]	R	Yes	No		
5	TDIE_ADC[13]	R	Yes	No		
4	TDIE_ADC[12]	R	Yes	No		
3	TDIE_ADC[11]	R	Yes	No		
2	TDIE_ADC[10]	R	Yes	No		
1	TDIE_ADC[9]	R	Yes	No		
0	TDIE_ADC[8]	R	Yes	No	128 °C	TDIE (IC Temperature) reading: Range: 0°C – 128°C

8.5.37 TDIE ADC 0 Register (Address = 24h) [reset = 00h]

REG24 is shown in Figure 70 and described in Table 46.

Return to Summary Table.

Figure 70. REG24 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
Field	TDIE_ADC[7:0]							

Table 46. REG24 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	TDIE_ADC[7]	R	Yes	No	64 °C	TDIE (IC Temperature) reading: Range: 0°C – 128°C
6	TDIE_ADC[6]	R	Yes	No	32 °C	
5	TDIE_ADC[5]	R	Yes	No	16 °C	
4	TDIE_ADC[4]	R	Yes	No	8 °C	
3	TDIE_ADC[3]	R	Yes	No	4°C	
2	TDIE_ADC[2]	R	Yes	No	2 °C	
1	TDIE_ADC[1]	R	Yes	No	1 °C	
0	TDIE_ADC[0]	R	Yes	No	0.5 °C	

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8.5.38 Part Information Register (Address = 25h) [reset = 18h]

REG25 is shown in Figure 71 and described in Table 47.

Return to Summary Table.

Figure 71. REG25 Register

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	1	1	0	0	0
Field	REG_RST	PN[3:0]				DEV_REV[2:0]		

Table 47. REG25 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	REG_RST	R/W	Yes	No	Register Reset: 0 – Keep current register settings 1 – Reset to default register value and reset safety timer (bit resets to 0 after register reset is complete)
6	PN[3]	R	Yes	No	0011: BQ25883
5	PN[2]	R	Yes	No	
4	PN[1]	R	Yes	No	
3	PN[0]	R	Yes	No	
2	DEV_REV[2]	R	Yes	No	Device revision: 001
1	DEV_REV[1]	R	Yes	No	
0	DEV_REV[0]	R	Yes	No	

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A typical application consists of the BQ25883 configured as an I2C controlled power path management device and a 2s battery charger for Li-Ion and Li-polymer batteries used in a wide range of portable devices. It integrates an input blocking FET (QBLK, Q1), high-side switching FET (QHS, Q2), low-side switching FET (QLS, Q3), and battery FET (QBAT, Q4) between system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

9.2 Typical Application

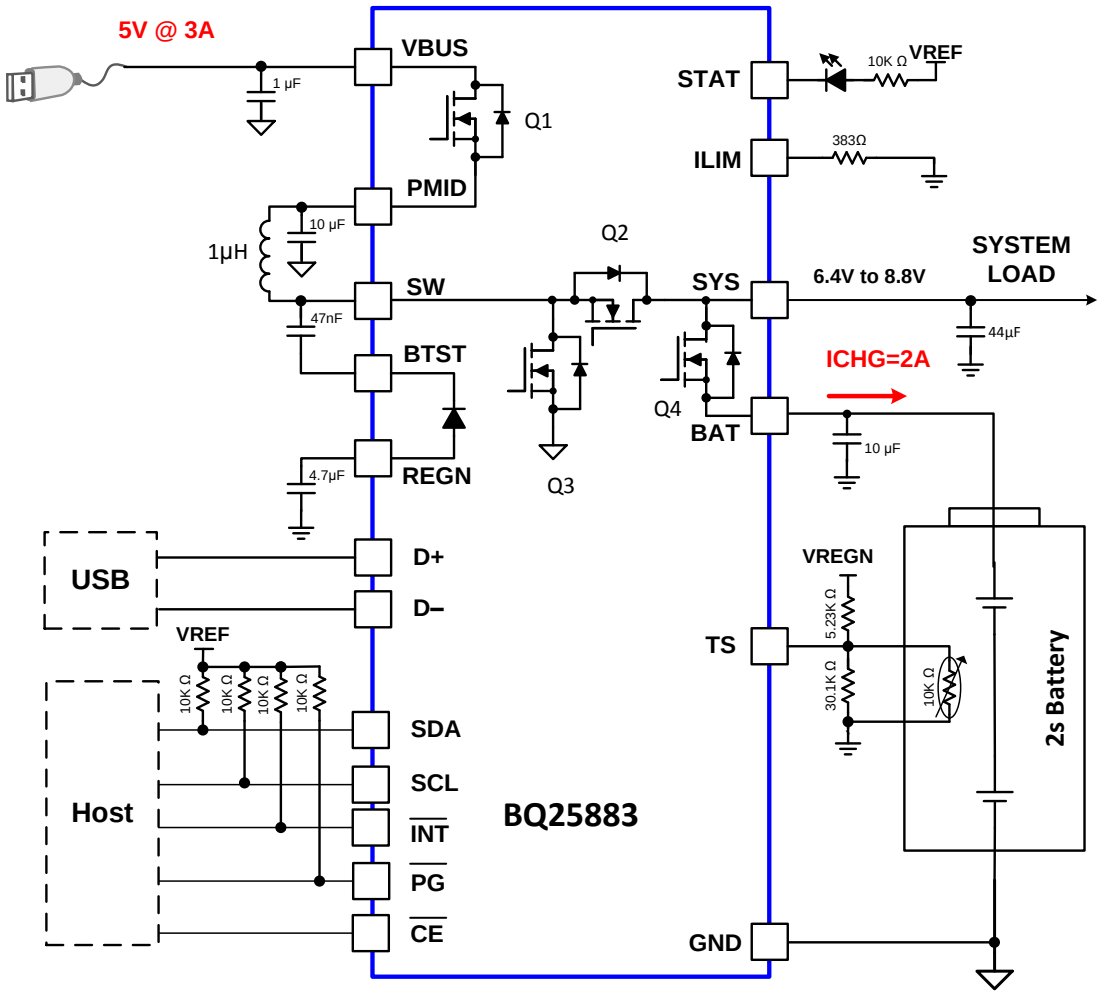

Figure 72. BQ25883 (I2C, OTG, and Power Path) Typical Application Diagram

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Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters shown in the table below.

Table 48. Design Parameters

PARAMETER	VALUE
VBUS voltage range	3.9 V to 6.2 V
Input current limit (IINDPM[4:0])	2.4 A
Fast charge current limit (ICHG[5:0])	1.5 A
Minimum System Voltage (SYS_MIN[3:0])	6.2 V
Battery Regulation Voltage (VREG[7:0])	8.4 V

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The device has 1.5MHz switching frequency to allow the use of small inductor and capacitor values. The inductor saturation current should be higher than the input current (I_{IN}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{IN} + \frac{I_{RIPPLE}}{2} \tag{5}$$

The inductor ripple current (I_{RIPPLE}) depends on input voltage (V_{VBUS}), duty cycle ($D = V_{BAT}/V_{BUS}$), switching frequency (f_{SW}) and inductance (L):

$$I_{RIPPLE} = \frac{V_{BUS} \times (V_{SYS} - V_{BUS})}{V_{SYS} \times f_{SW} \times L} \tag{6}$$

The maximum inductor ripple current happens in the vicinity of D = 0.5. Usually inductor ripple is designed in the range of (20 – 40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

9.2.2.2 Input (VBUS / PMID) Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current occurs when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{PMID} occurs where the duty cycle is closest to 50% and can be estimated by

$$I_{PMID} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{7}$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed close to the PMID and GND pins of the IC. Voltage rating of the capacitor must be higher than normal input voltage level. 25-V rating or higher capacitor is preferred for up to 5-V input voltage. 10-µF capacitor is suggested for up to 3.3-A input current.

9.2.2.3 Output (VSYS) Capacitor

SYS capacitor is the boost converter output capacitor and should also have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{CSYS,\,rms} = I_{OUT} \times \sqrt{\frac{D}{1-D}} \tag{8}$$

The output capacitor voltage ripple is a function of the boost output current (I_{OUT}), and can be calculated as follows:

$$\Delta V_{SYS} = \frac{I_{OUT} \times D}{f_{SW} \times C_{SYS}} \tag{9}$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for SYS decoupling capacitor and should be placed close to theSYS and GND pins of the IC. Voltage rating of the capacitor must be higher than normal output voltage level. 16-V rating or higher capacitor is preferred. 44-μF capacitor is suggested for up to 2.2-A boost converter output current.

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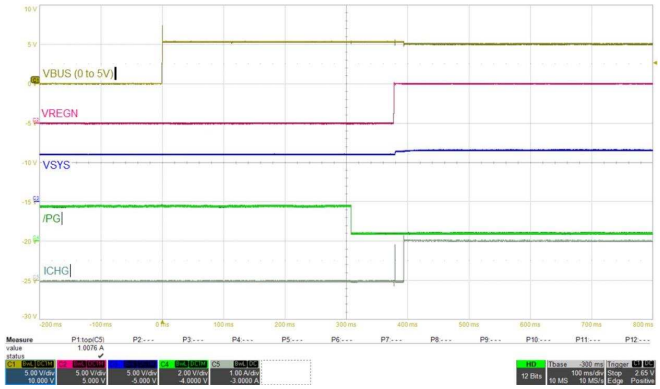
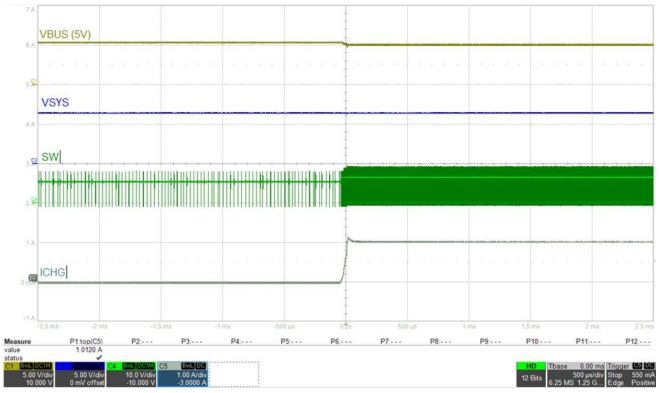
9.2.3 Application Curves

C_{VBUS} = 1µF, C_{PMID}= 10µF, C_{BAT} = 10µF, C_{SYS} = 44µF, L = DFE252012F-1R0 (1µH) (unless otherwise specified)



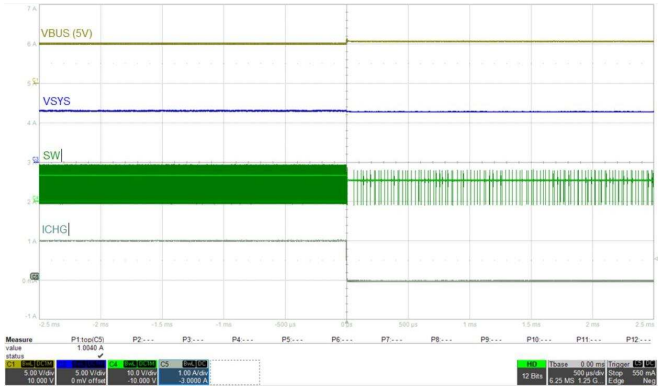
VBUS = 5V VBAT = 6.0V ICHG = 1A

Figure 73. Adapter Power Up with Charge Enabled



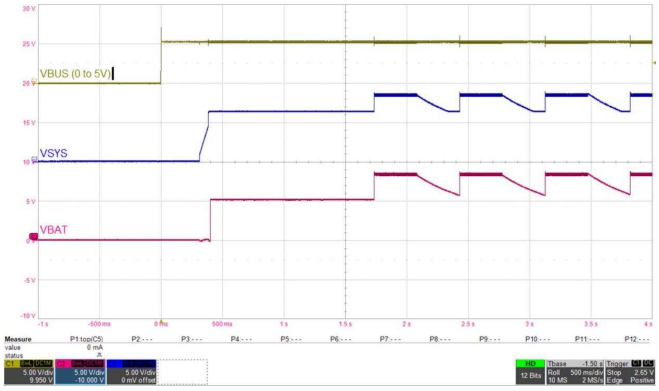
VBUS = 5V VBAT = 7.4V ICHG = 1A

Figure 74. Charge Enable



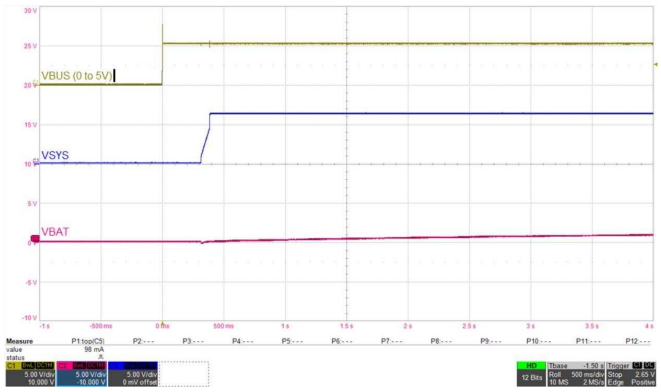
VBUS = 5V VBAT = 7.4V ICHG = 1A

Figure 75. Charge Disabled



VBUS = 5V VBAT = Open Charge enabled

Figure 76. Adapter Plug-in with No Battery



VBUS = 5V VBAT = Open Charge disabled

Figure 77. Adapter Plug-in with No Battery Charge Disabled

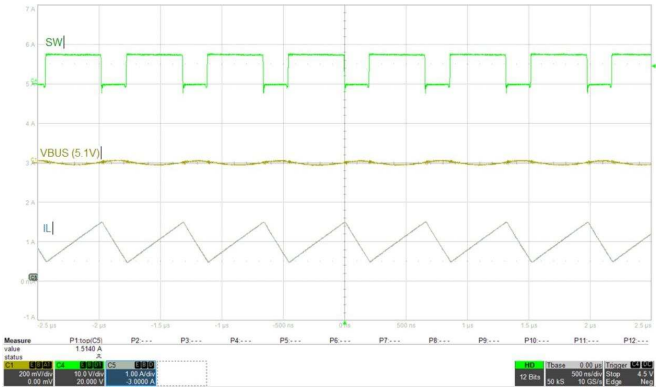
VBAT = 7.6V VBUS = 5.1V No IBUS load

Figure 78. Buck Mode (OTG) Startup

C_{VBUS} = 1µF, C_{PMID}= 10µF, C_{BAT} = 10µF, C_{SYS} = 44µF, L = DFE252012F-1R0 (1µH) (unless otherwise specified)

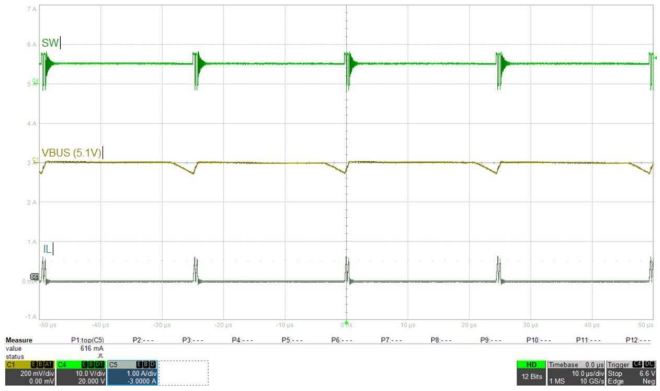
VBAT = 7.6V Adapter removed with EN_OTG = 1 R_{BUS} = 25Ω

Figure 79. Buck Mode Startup After Adapter Removal



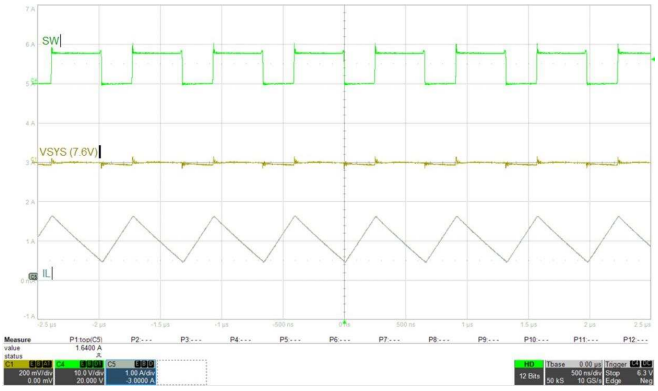
VBAT = 7.6V VBUS = 5.1V IBUS = 1A

Figure 80. Buck Mode (OTG) PWM Switching



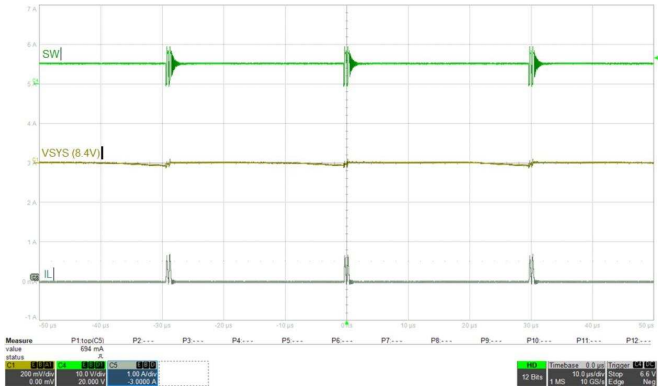
VBAT = 7.6V VBUS = 5.1V IBUS = 0mA

Figure 81. Buck Mode (OTG) PFM Switching



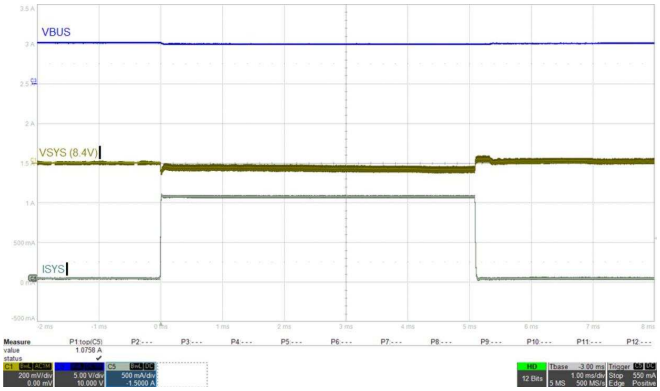
VBUS = 5V VBAT = 7.6V ICHG = 1A

Figure 82. Boost Mode PWM Switching



VBUS = 5V VBAT = 8.4V Charge disabled

Figure 83. Boost Mode PFM Switching



VBUS = 5V VBAT = 8.4V Charge disabled

Figure 84. System Load Transient Response

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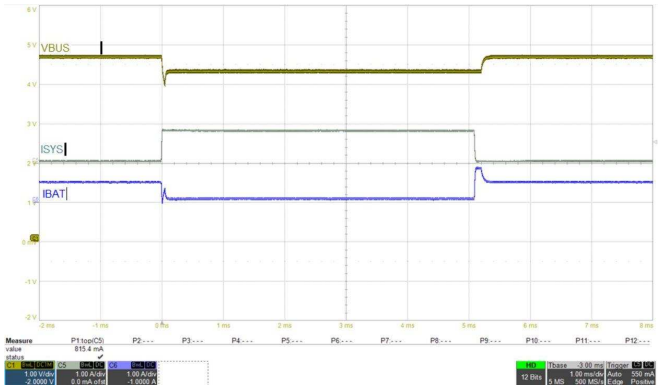
C_{VBUS} = 1µF, C_{PMID}= 10µF, C_{BAT} = 10µF, C_{SYS} = 44µF, L = DFE252012F-1R0 (1µH) (unless otherwise specified)

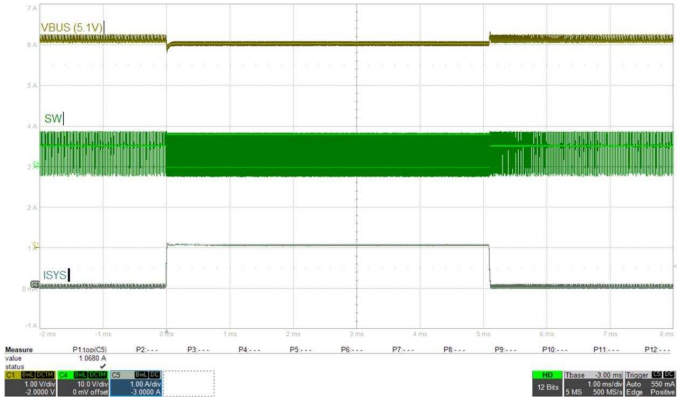


DCP Adapter VBAT = 8.0V Charge enabled

Figure 85. VINDPM Transient Response

DCP Adapter VBAT = 8.0V Charge enabled

Figure 86. IINDPM Transient Response



VBAT = 7.6V VBUS = 5.1V

Figure 87. Buck Mode (OTG) Load Transient Response

10 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.9 V and 6.2 V input with at least 500-mA current rating connected to VBUS or a 2s Li-Ion battery with voltage > VBAT_UVLO connected to BAT The source current rating needs to be at least 3-A in order for the boost converter of the charger to provide maximum output power to SYS.

11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loops is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Put SYS output capacitor as close to SYS and GND pins as possible. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
2. Place PMID input capacitor as close as possible to PMID pins and PGND pins and use shortest copper trace connection or GND plane.
3. Place inductor input terminal to SW pins as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the input current. Minimize parasitic capacitance from this area to any other trace or plane.
4. Decoupling capacitors should be placed on the same side of and next to the IC and make trace connection as short as possible.
5. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0-Ω resistor to tie analog ground to power ground.
6. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
7. Via size and number should be enough for a given current path.

Refer to the EVM design and the Layout Example below for the recommended component placement with trace and via locations.

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11.2 Layout Example

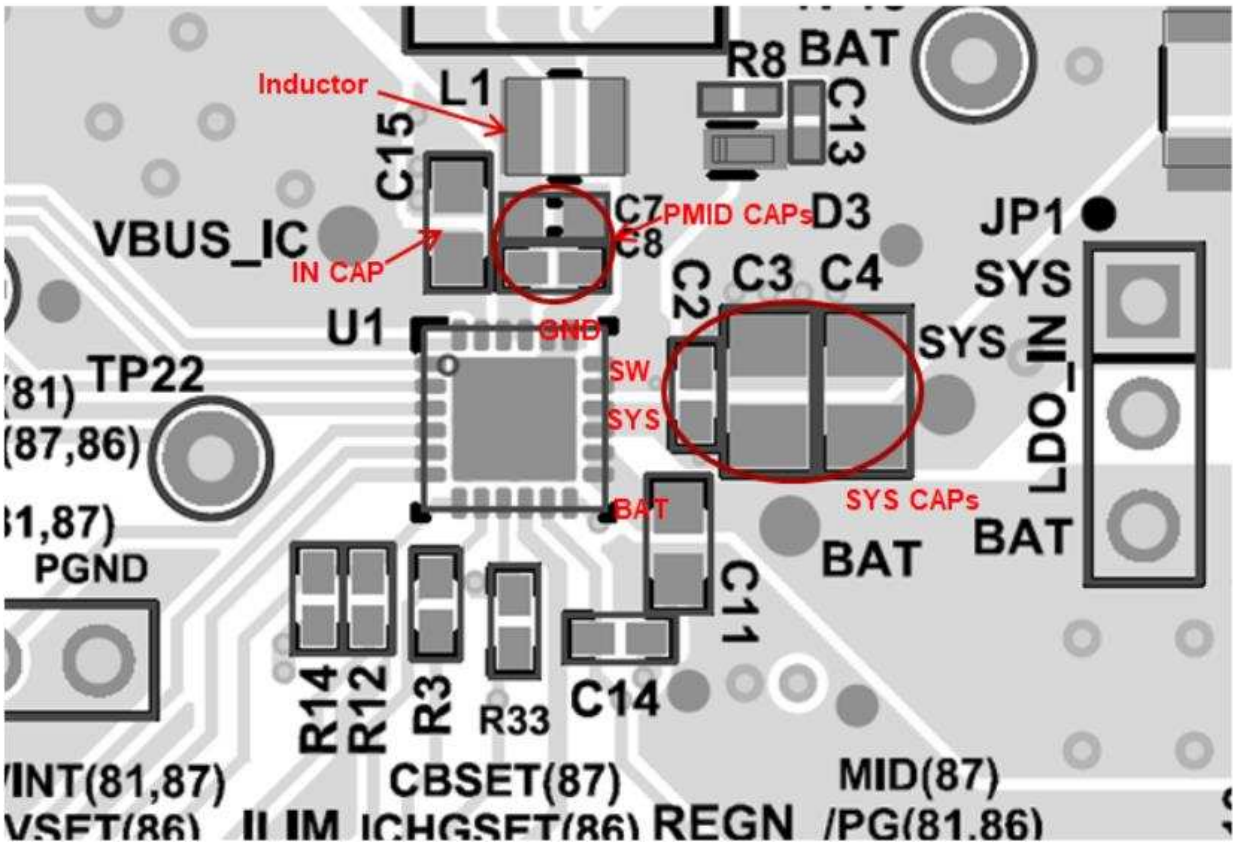

Figure 88. PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *BQ2588x EVM User's Guide* (SLUUBU6)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25883RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25883
BQ25883RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25883
BQ25883RGERG4	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25883
BQ25883RGERG4.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25883
BQ25883RGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25883
BQ25883RGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25883

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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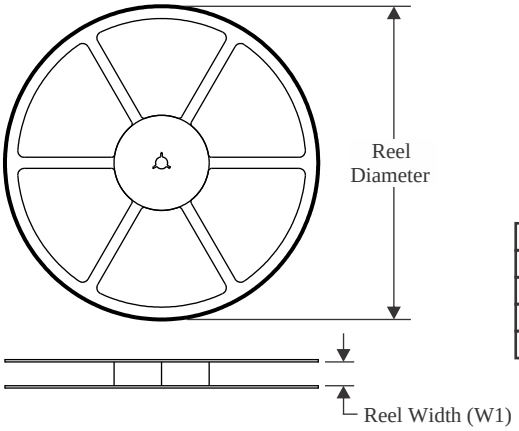
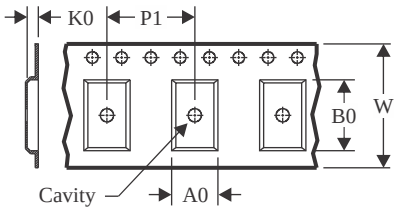
TAPE AND REEL INFORMATION

REEL DIMENSIONS

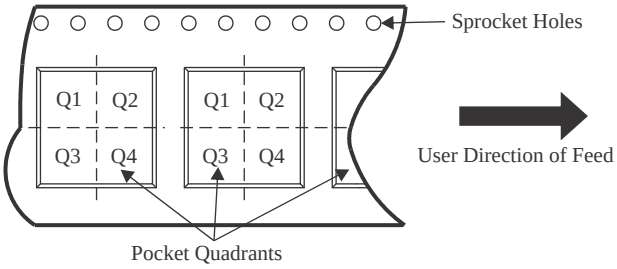


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

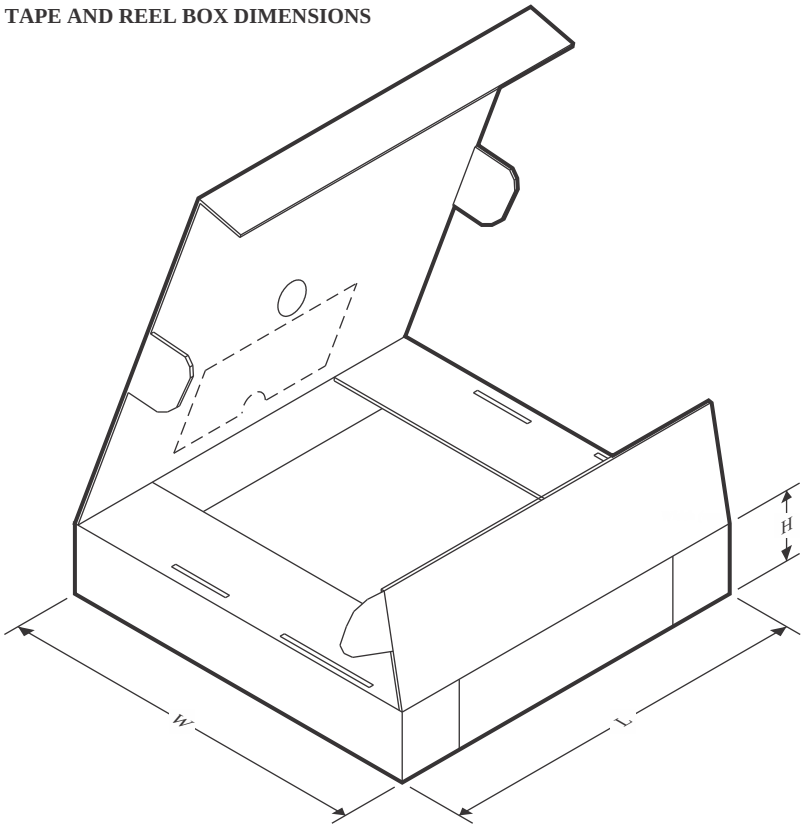
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25883RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q2
BQ25883RGERG4	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25883RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

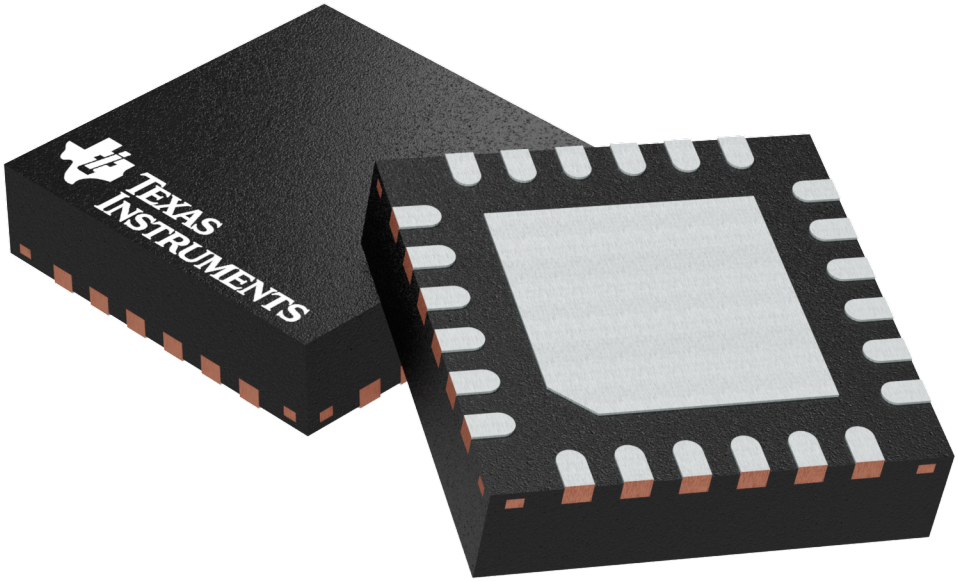


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25883RGER	VQFN	RGE	24	3000	356.0	356.0	36.0
BQ25883RGERG4	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ25883RGET	VQFN	RGE	24	250	210.0	185.0	35.0

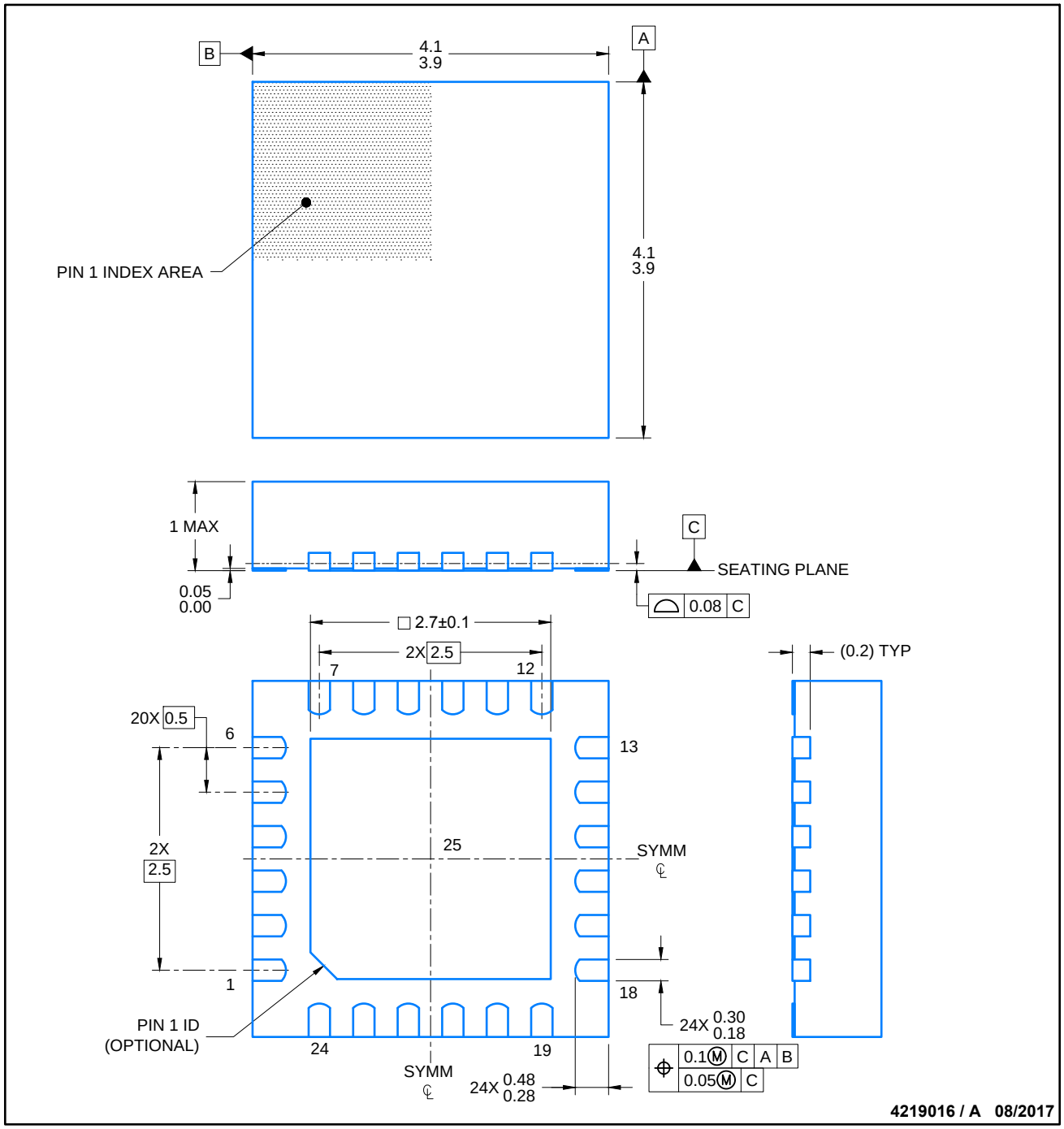
RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



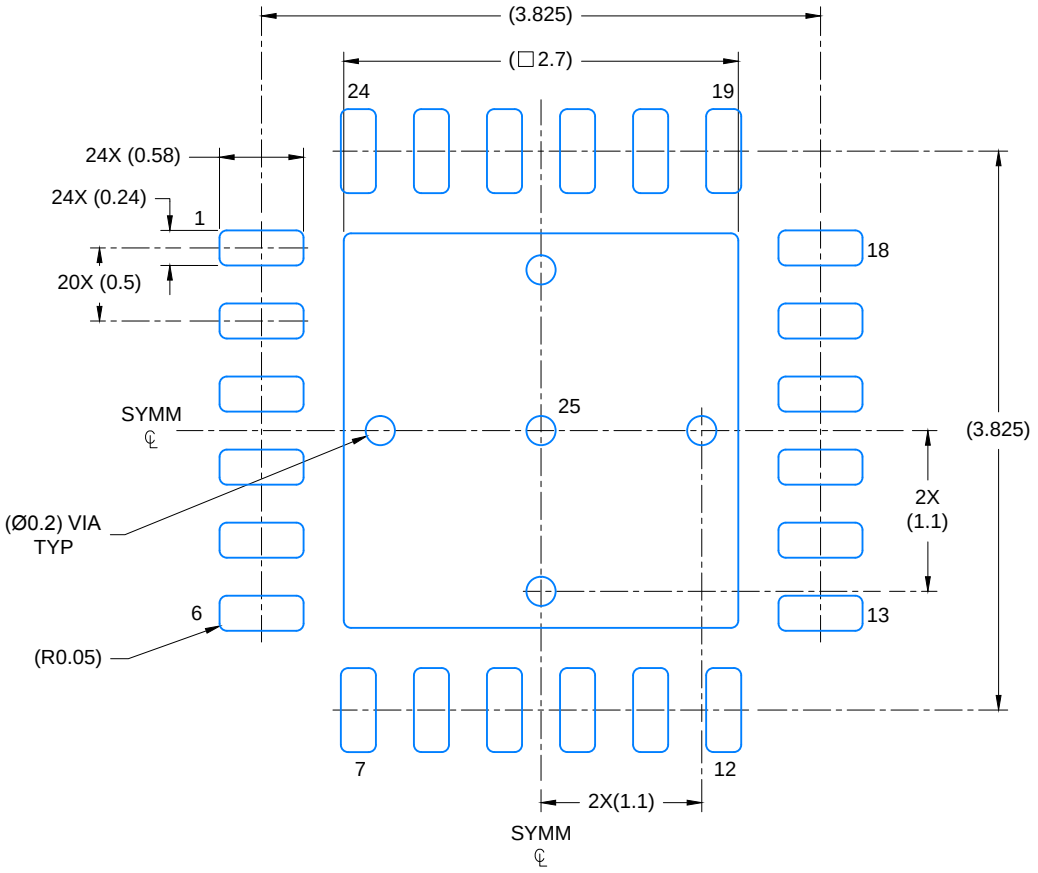
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC QUAD FLATPACK- NO LEAD



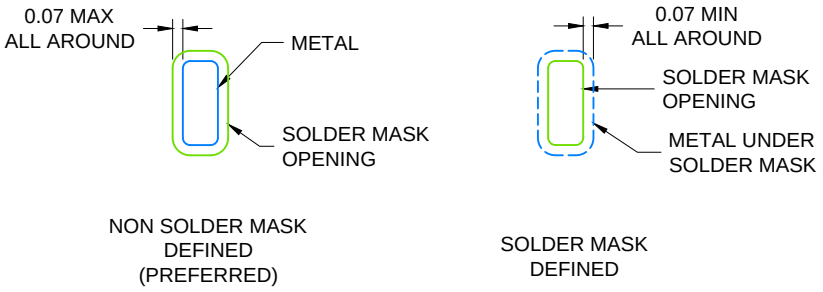
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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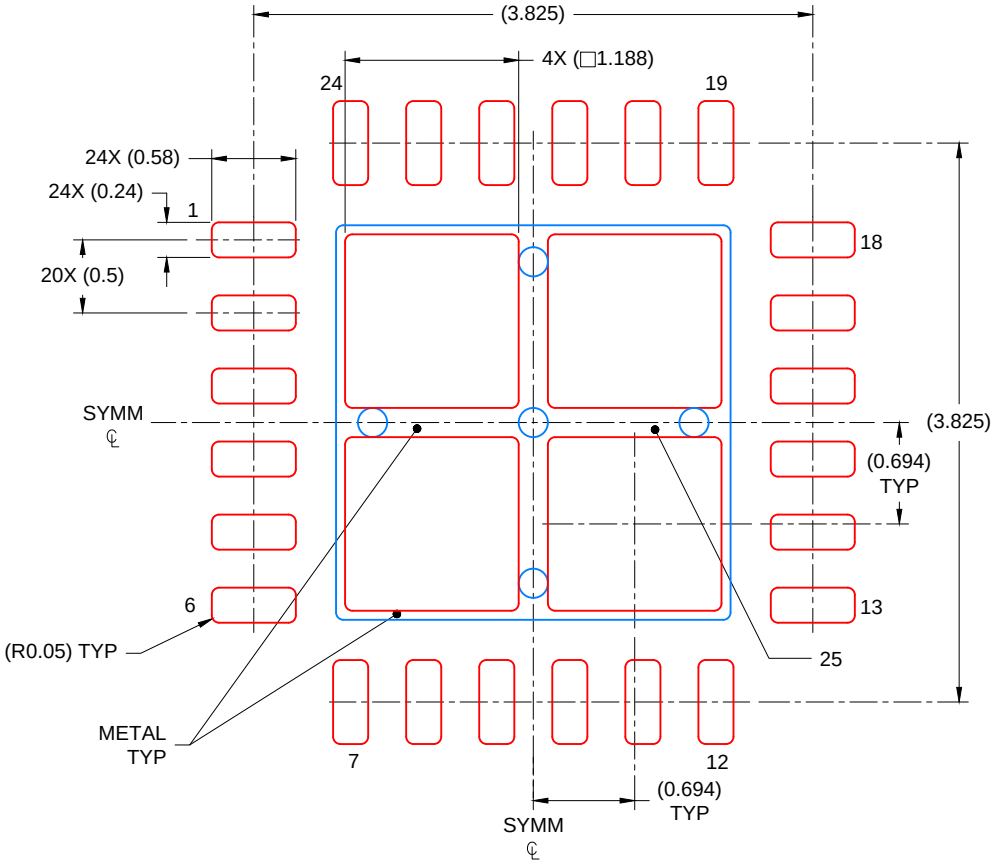
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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