

## **SINGLE-CELL LI-ION CHARGE MANAGEMENT IC FOR PDAs AND INTERNET APPLIANCES**

### **FEATURES**

- **Highly Integrated Solution With FET Pass Transistor and Reverse-Blocking Schottky and Thermal Protection**
- **Integrated Voltage and Current Regulation With Programmable Charge Current**
- **High-Accuracy Voltage Regulation ( $\pm 1\%$ )**
- **Ideal for Low-Dropout Linear Charger Designs for Single-Cell Li-Ion Packs With Coke or Graphite Anodes**
- **Up to 1.2-A Continuous Charge Current**
- **Safety-Charge Timer During Preconditioning and Fast Charge**
- **Integrated Cell Conditioning for Reviving Deeply Discharged Cells and Minimizing Heat Dissipation During Initial Stage of Charge**
- **Optional Temperature or Input-Power Monitoring Before and During Charge**
- **Various Charge-Status Output Options for Driving Single, Double, or Bicolor LEDs or Host-Processor Interface**
- **Charge Termination by Minimum Current and Time**
- **Low-Power Sleep Mode**
- **Packaging: 5 mm  $\times$  5 mm MLP or 20-Lead TSSOP PowerPAD™**

### **APPLICATIONS**

- **PDAs**
- **Internet Appliances**
- **MP3 Players**
- **Digital Cameras**

### **DESCRIPTION**

The bq2400x series ICs are advanced Li-Ion linear charge management devices for highly integrated and space-limited applications. They combine high-accuracy current and voltage regulation; FET pass-transistor and reverse-blocking Schottky; battery conditioning, temperature, or input-power monitoring; charge termination; charge-status indication; and charge timer in a small package.

The bq2400x measures battery temperature using an external thermistor. For safety reasons, the bq2400x inhibits charge until the battery temperature is within the user-defined thresholds. Alternatively, the user can monitor the input voltage to qualify charge. The bq2400x series then charge the battery in three phases: preconditioning, constant current, and constant voltage. If the battery voltage is below the internal low-voltage threshold, the bq2400x uses low-current precharge to condition the battery. A preconditioning timer is provided for additional safety. Following preconditioning, the bq2400x applies a constant-charge current to the battery. An external sense-resistor sets the magnitude of the current. The constant-current phase is maintained until the battery reaches the charge-regulation voltage. The bq2400x then transitions to the constant voltage phase. The user can configure the device for cells with either coke or graphite anodes. The accuracy of the voltage regulation is better than  $\pm 1\%$  over the operating junction temperature and supply voltage range.

Charge is terminated by maximum time or minimum taper current detection

The bq2400x automatically restarts the charge if the battery voltage falls below an internal recharge threshold.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| $T_J$          | PACKAGE                              |                                     | CHARGE STATUS<br>CONFIGURATION |
|----------------|--------------------------------------|-------------------------------------|--------------------------------|
|                | 20-LEAD HTTSOP PowerPAD™<br>(PWP)(1) | 20-LEAD 5 mm × 5 mm MLP<br>(RGW)(2) |                                |
| –40°C to 125°C | bq24001PWP                           | bq24001RGW                          | Single LED                     |
|                | bq24002PWP                           | bq24002RGW                          | 2 LEDs                         |
|                | bq24003PWP                           | bq24003RGW                          | Single bicolor LED             |

(1) The PWP package is available taped and reeled. Add R suffix to device type (e.g. bq24001PWPR) to order. Quantities 2500 devices per reel.

(2) The RGW package is available taped and reeled. Add R suffix to device type (e.g. bq24001RGWR) to order. Quantities 3000 devices per reel.

## PACKAGE DISSIPATION RATINGS

| PACKAGE | $\Theta_{JA}$ | $\Theta_{JC}$ | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_A = 25^\circ\text{C}$ |
|---------|---------------|---------------|---------------------------------------------|---------------------------------------------------|
| PWP(1)  | 30.88°C/W     | 1.19°C/W      | 3.238 W                                     | 0.0324W/°C                                        |
| RGW(2)  | 31.41°C/W     | 1.25°C/W      | 3.183 W                                     | 0.0318W/°C                                        |

(1) This data is based on using the JEDEC high-K board and topside traces, top and bottom thermal pad (6.5 × 3.4 mm), internal 1 oz power and ground planes, 8 thermal via underneath the die connecting to ground plane.

(2) This data is based on using the JEDEC high-K board and topside traces, top and bottom thermal pad (3.25 × 3.25 mm), internal 1 oz power and ground planes, 9 thermal via underneath the die connecting to ground plane.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

|                                                                                                         | bq24001<br>bq24002<br>bq24003 |
|---------------------------------------------------------------------------------------------------------|-------------------------------|
| Supply voltage ( $V_{CC}$ with respect to GND)                                                          | 13.5 V                        |
| Input voltage (IN, ISNS, EN, APG/THERM/CR/STAT1/STAT2, VSENSE, TMR SEL, VSEL) (all with respect to GND) | 13.5 V                        |
| Output current (OUT pins)                                                                               | 2 A                           |
| Output sink/source current (STAT1 and STAT2)                                                            | 10 mA                         |
| Operating free-air temperature range, $T_A$                                                             | –40°C to 70°C                 |
| Storage temperature range, $T_{Stg}$                                                                    | –65°C to 150°C                |
| Junction temperature range, $T_J$                                                                       | –40°C to 125°C                |
| Lead temperature (Soldering, 10 sec)                                                                    | 300°C                         |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

|                                             | MIN | MAX | UNIT |
|---------------------------------------------|-----|-----|------|
| Supply voltage, $V_{CC}$                    | 4.5 | 10  | V    |
| Input voltage, $V_{IN}$                     | 4.5 | 10  | V    |
| Continuous output current                   |     | 1.2 | A    |
| Operating junction temperature range, $T_J$ | –40 | 125 | °C   |

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature supply and input voltages, and  $V_I (V_{CC}) \geq V_I (IN)$  ( unless otherwise noted)

| PARAMETER                                                  | TEST CONDITIONS                                                   | MIN | TYP | MAX | UNIT    |
|------------------------------------------------------------|-------------------------------------------------------------------|-----|-----|-----|---------|
| $V_{CC}$ current                                           | $V_{CC} > V_{CC\_UVLO}$ , $EN \leq V_{IH}(EN)$                    |     |     | 1   | mA      |
| $V_{CC}$ current, standby mode                             | $EN \leq V_{IL}(EN)$                                              |     | 1   |     | $\mu A$ |
| IN current, standby mode                                   | $EN \leq V_{IL}(EN)$                                              |     |     | 10  | $\mu A$ |
| Standby current (sum of currents into OUT and VSENSE pins) | $V_{CC} < V_{CC\_UVLO}$ , $V_{OUT} = 4.3 V$ , $V_{SENSE} = 4.3 V$ |     | 2   | 4   | $\mu A$ |
|                                                            | $EN \leq V_{IL}(EN)$ , $V_{OUT} = 4.3 V$ , $V_{SENSE} = 4.3 V$    |     | 2   | 4   |         |

### VOLTAGE REGULATION, $0^\circ C \leq T_J \leq 125^\circ C$

| PARAMETER                             | TEST CONDITIONS                                                                    | MIN   | TYP  | MAX   | UNIT |
|---------------------------------------|------------------------------------------------------------------------------------|-------|------|-------|------|
| Output voltage                        | $V_{SEL} = V_{SS}$ , $0 < I_O \leq 1.2 A$                                          | 4.059 | 4.10 | 4.141 | V    |
|                                       | $V_{SEL} = V_{CC}$ , $0 < I_O \leq 1.2 A$                                          | 4.158 | 4.20 | 4.242 | V    |
| Load regulation                       | $1 mA \leq I_O \leq 1.2 A$ , $V_I(IN) = 5 V$ , $V_{CC} = 5 V$ , $T_J = 25^\circ C$ |       | 1    |       | mV   |
| Line regulation                       | $V_{OUT} + V_{DO} + V_{ilim}(MAX) < V_I(V_{CC}) < 10 V$ , $T_J = 25^\circ C$       |       | 0.01 |       | %/V  |
| Dropout voltage = $V_I(IN) - V_{out}$ | $I_O = 1.0 A$ , $4.9 V < V_I(V_{CC}) < 10 V$                                       |       |      | 0.7   | V    |
|                                       | $I_O = 1.2 A$ , $V_{OUT} + V_{DO} + V_{ilim}MAX < V_I(V_{CC}) < 10 V$              |       |      | 0.8   | V    |

### CURRENT REGULATION, $0^\circ C \leq T_J \leq 125^\circ C$

| PARAMETER                                  | TEST CONDITIONS                                                                       | MIN   | TYP | MAX   | UNIT |
|--------------------------------------------|---------------------------------------------------------------------------------------|-------|-----|-------|------|
| Current regulation threshold, $V_I(limit)$ | $V_{SENSE} < V_O(V_{SEL-LOW/HIGH})$                                                   | 0.095 | 0.1 | 0.105 | V    |
| Delay time                                 | $V_{SENSE}$ pulsed above $V_{LOWV}$ to $I_O = 10\%$ of regulated value <sup>(1)</sup> |       |     | 1     | ms   |
| Rise time                                  | $I_O$ increasing from 10% to 90% of regulated value. $R_{SNS} \geq 0.2 \Omega$ , (1)  | 0.1   |     | 1     | ms   |

(1) Specified by design, not production tested.

### CURRENT SENSE RESISTOR, $0^\circ C \leq T_J \leq 125^\circ C$

| PARAMETER                                           | TEST CONDITIONS                  | MIN   | TYP | MAX | UNIT     |
|-----------------------------------------------------|----------------------------------|-------|-----|-----|----------|
| External current sense resistor range ( $R_{SNS}$ ) | $100 mA \leq I_{lim} \leq 1.2 A$ | 0.083 |     | 1   | $\Omega$ |

### PRECHARGE CURRENT REGULATION, $0^\circ C \leq T_J \leq 125^\circ C$

| PARAMETER                    | TEST CONDITIONS                                               | MIN | TYP | MAX | UNIT |
|------------------------------|---------------------------------------------------------------|-----|-----|-----|------|
| Precharge current regulation | $V_{SENSE} < V_{LOWV}$ , $0.083 \leq R_{SNS} \leq 1.0 \Omega$ | 40  | 60  | 80  | mA   |

### $V_{CC}$ UVLO COMPARATOR, $0^\circ C \leq T_J \leq 125^\circ C$

| PARAMETER       | TEST CONDITIONS | MIN  | TYP  | MAX  | UNIT |
|-----------------|-----------------|------|------|------|------|
| Start threshold |                 | 4.35 | 4.43 | 4.50 | V    |
| Stop threshold  |                 | 4.25 | 4.33 | 4.40 | V    |
| Hysteresis      |                 | 50   |      |      | mV   |

### APG/THERM COMPARATOR, $0^\circ C \leq T_J \leq 125^\circ C$

| PARAMETER            | TEST CONDITIONS | MIN   | TYP   | MAX   | UNIT    |
|----------------------|-----------------|-------|-------|-------|---------|
| Upper trip threshold |                 | 1.480 | 1.498 | 1.515 | V       |
| Lower trip threshold |                 | 0.545 | 0.558 | 0.570 | V       |
| Input bias current   |                 |       |       | 1     | $\mu A$ |

### LOWV COMPARATOR, $0^\circ C \leq T_J \leq 125^\circ C$

| PARAMETER       | TEST CONDITIONS | MIN  | TYP  | MAX  | UNIT |
|-----------------|-----------------|------|------|------|------|
| Start threshold |                 | 2.80 | 2.90 | 3.00 | V    |
| Stop threshold  |                 | 3.00 | 3.10 | 3.20 | V    |
| Hysteresis      |                 | 100  |      |      | mV   |

**ELECTRICAL CHARACTERISTICS CONTINUED**over recommended operating junction temperature supply and input voltages, and  $V_I (V_{CC}) \geq V_I (IN)$  ( unless otherwise noted)

| <b>HIGHV (RECHARGE) COMPARATOR, <math>0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}</math></b> |                 |      |      |      |      |  |
|--------------------------------------------------------------------------------------------------|-----------------|------|------|------|------|--|
| PARAMETER                                                                                        | TEST CONDITIONS | MIN  | TYP  | MAX  | UNIT |  |
| Start threshold                                                                                  |                 | 3.80 | 3.90 | 4.00 | V    |  |

| <b>OVERV COMPARATOR, <math>0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}</math></b> |                 |      |      |      |      |  |
|---------------------------------------------------------------------------------------|-----------------|------|------|------|------|--|
| PARAMETER                                                                             | TEST CONDITIONS | MIN  | TYP  | MAX  | UNIT |  |
| Start threshold                                                                       |                 | 4.35 | 4.45 | 4.55 | V    |  |
| Stop threshold                                                                        |                 | 4.25 | 4.30 | 4.35 | V    |  |
| Hysteresis                                                                            |                 | 50   |      |      | mV   |  |

| <b>TAPERDET COMPARATOR, <math>0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}</math></b> |                 |     |      |     |      |  |
|------------------------------------------------------------------------------------------|-----------------|-----|------|-----|------|--|
| PARAMETER                                                                                | TEST CONDITIONS | MIN | TYP  | MAX | UNIT |  |
| Trip threshold                                                                           |                 | 12  | 18.5 | 25  | mV   |  |

| <b>EN LOGIC INPUT, <math>0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}</math></b> |                 |      |     |     |            |  |
|-------------------------------------------------------------------------------------|-----------------|------|-----|-----|------------|--|
| PARAMETER                                                                           | TEST CONDITIONS | MIN  | TYP | MAX | UNIT       |  |
| High-level input voltage                                                            |                 | 2.25 |     |     | V          |  |
| Low-level input voltage                                                             |                 |      |     | 0.8 | V          |  |
| Input pulldown resistance                                                           |                 | 100  |     | 200 | k $\Omega$ |  |

| <b>VSEL LOGIC INPUT, <math>0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}</math></b> |                 |      |     |     |            |  |
|---------------------------------------------------------------------------------------|-----------------|------|-----|-----|------------|--|
| PARAMETER                                                                             | TEST CONDITIONS | MIN  | TYP | MAX | UNIT       |  |
| High-level input voltage                                                              |                 | 2.25 |     |     | V          |  |
| Low-level input voltage                                                               |                 |      |     | 0.8 | V          |  |
| Input pulldown resistance                                                             |                 | 100  |     | 200 | k $\Omega$ |  |

| <b>TMR SEL INPUT <math>0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}</math></b> |                                      |     |     |     |               |  |
|-----------------------------------------------------------------------------------|--------------------------------------|-----|-----|-----|---------------|--|
| PARAMETER                                                                         | TEST CONDITIONS                      | MIN | TYP | MAX | UNIT          |  |
| High-level input voltage                                                          |                                      | 2.7 |     |     | V             |  |
| Low-level input voltage                                                           |                                      |     |     | 0.6 | V             |  |
| Input bias current                                                                | $V_I(\text{TMR SEL}) \leq 5\text{V}$ |     |     | 15  | $\mu\text{A}$ |  |

| <b>STAT1, STAT2 (bq24001, bq24003), <math>0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}</math></b> |                                                  |              |     |     |               |  |
|------------------------------------------------------------------------------------------------------|--------------------------------------------------|--------------|-----|-----|---------------|--|
| PARAMETER                                                                                            | TEST CONDITIONS                                  | MIN          | TYP | MAX | UNIT          |  |
| Output (low) saturation voltage                                                                      | $I_O = 10\text{ mA}$                             |              |     | 1.5 | V             |  |
| Output (low) saturation voltage                                                                      | $I_O = 4\text{ mA}$                              |              |     | 0.6 | V             |  |
| Output (high) saturation voltage                                                                     | $I_O = -10\text{ mA}$                            | $V_{CC}-1.5$ |     |     | V             |  |
| Output (high) saturation voltage                                                                     | $I_O = -4\text{ mA}$                             | $V_{CC}-0.5$ |     |     | V             |  |
| Output turn on/off time                                                                              | $I_O = \pm 10\text{ mA}, C = 100\text{ p}^{(1)}$ |              |     | 100 | $\mu\text{s}$ |  |

(1) Assured by design, not production tested.

| <b>POWER-ON RESET (POR), <math>0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}</math></b> |                 |     |     |     |               |  |
|-------------------------------------------------------------------------------------------|-----------------|-----|-----|-----|---------------|--|
| PARAMETER                                                                                 | TEST CONDITIONS | MIN | TYP | MAX | UNIT          |  |
| POR delay                                                                                 | See Note 1      | 1.2 |     | 3   | ms            |  |
| POR falling-edge deglitch                                                                 | See Note 1      | 25  |     | 75  | $\mu\text{s}$ |  |

(1) Assured by design, not production tested.

## ELECTRICAL CHARACTERISTICS CONTINUED

over recommended operating junction temperature supply and input voltages, and  $V_I (V_{CC}) \geq V_I (IN)$  ( unless otherwise noted)

| APG/THERM DELAY, $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ |                 |     |     |     |               |
|--------------------------------------------------------------------|-----------------|-----|-----|-----|---------------|
| PARAMETER                                                          | TEST CONDITIONS | MIN | TYP | MAX | UNIT          |
| APG/THERM falling-edge deglitch                                    | See Note 1      | 25  |     | 75  | $\mu\text{s}$ |

(1) Assured by design, not production tested.

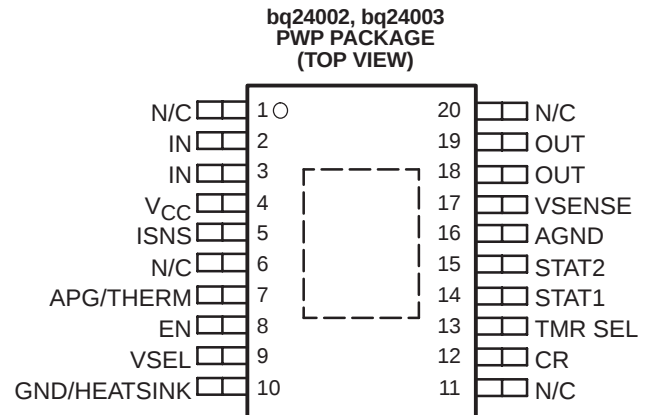
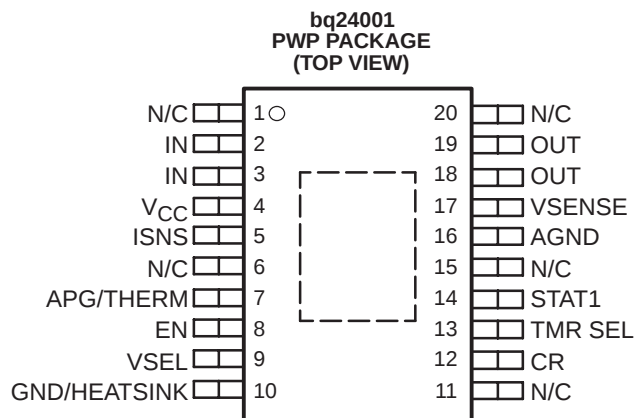
| TIMERS, $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ |                          |      |      |     |        |
|-----------------------------------------------------------|--------------------------|------|------|-----|--------|
| PARAMETER                                                 | TEST CONDITIONS          | MIN  | TYP  | MAX | UNIT   |
| User-selectable timer accuracy                            | $T_A = 25^\circ\text{C}$ | -15% |      | 15% |        |
|                                                           |                          | -20% |      | 20% |        |
| Precharge and taper timer                                 |                          |      | 22.5 |     | minute |

| THERMAL SHUTDOWN, $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ |                 |     |     |     |                  |
|---------------------------------------------------------------------|-----------------|-----|-----|-----|------------------|
| PARAMETER                                                           | TEST CONDITIONS | MIN | TYP | MAX | UNIT             |
| Thermal trip                                                        | See Note 1      |     | 165 |     | $^\circ\text{C}$ |
| Thermal hysteresis                                                  | See Note 1      |     | 10  |     | $^\circ\text{C}$ |

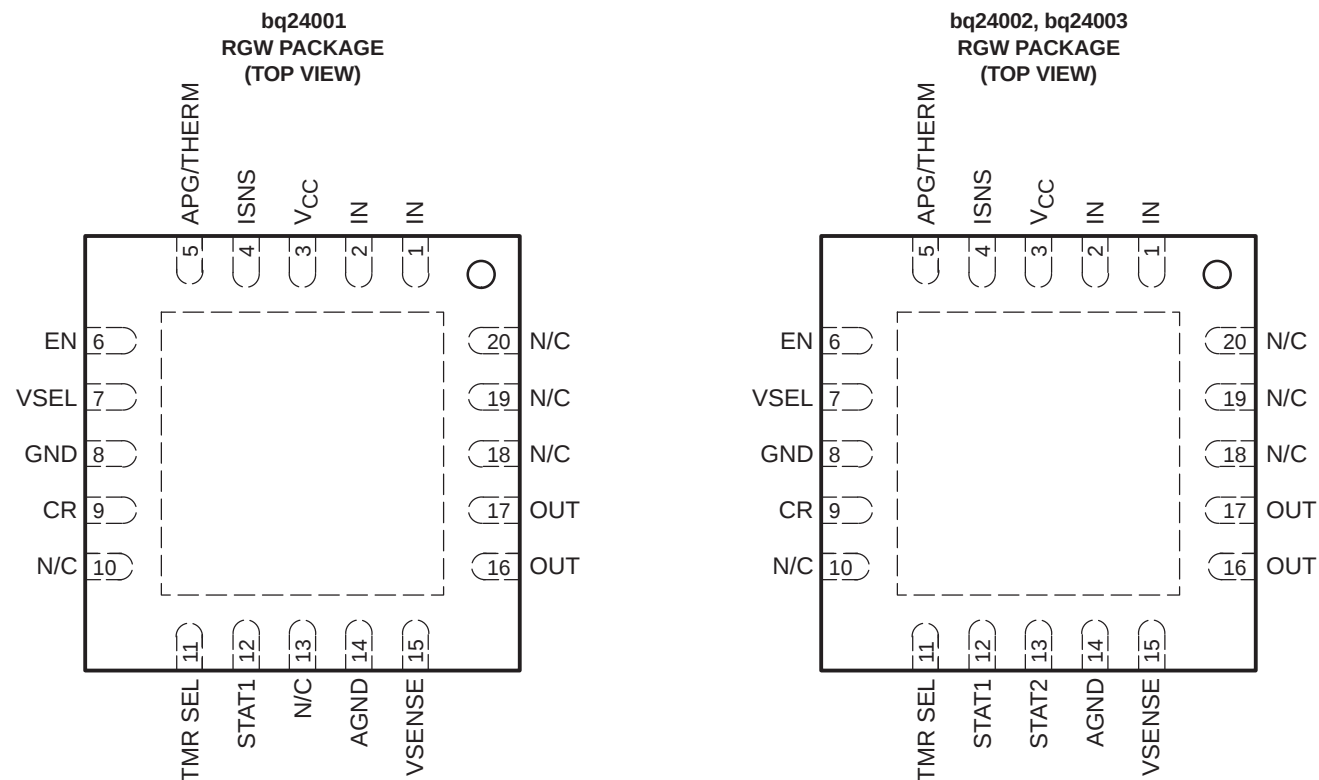
(1) Assured by design, not production tested.

| CR PIN, $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ |                                   |       |      |      |      |
|-----------------------------------------------------------|-----------------------------------|-------|------|------|------|
| PARAMETER                                                 | TEST CONDITIONS                   | MIN   | TYP  | MAX  | UNIT |
| Output voltage                                            | $0 < I_{O(CR)} < 100 \mu\text{A}$ | 2,816 | 2.85 | 2.88 | V    |

## PIN ASSIGNMENTS



N/C – Do not connect



N/C – Do Not Connect

## Terminal Functions

| TERMINAL     |                  |               | I/O | DESCRIPTION                                                                                                             |
|--------------|------------------|---------------|-----|-------------------------------------------------------------------------------------------------------------------------|
| NAME         | NO.              | NO.           |     |                                                                                                                         |
| AGND         | 16               | 14            |     | Ground pin; connect close to the negative battery terminal.                                                             |
| APG/THERM    | 7                | 5             | I   | Adapter power good input/thermistor sense input                                                                         |
| CR           | 12               | 9             | I   | Internal regulator bypass capacitor                                                                                     |
| EN           | 8                | 6             | I   | Charge-enable input. Active-high enable input with internal pull down. Low-current stand-by mode active when EN is low. |
| GND/HEATSINK | 10               | 8             |     | Ground pin; connect to PowerPAD heat-sink layout pattern.                                                               |
| IN           | 2, 3             | 1, 2          | I   | Input voltage. This input provides the charging voltage for the battery.                                                |
| ISNS         | 5                | 4             | I   | Current sense input                                                                                                     |
| N/C          | 1, 6, 11, 15, 20 | 10, 13, 18–20 |     | No connect. These pins must be left floating. Pin 15 is N/C on bq24001PWP only. Pin 13 is N/C on bq24001RGW only.       |
| OUT          | 18, 19           | 16, 17        | O   | Charge current output                                                                                                   |
| STAT1        | 14               | 12            | O   | Status display output 1                                                                                                 |
| STAT2        | 15               | 13            | O   | Status display output 2 (for bq24002 and bq24003 only)                                                                  |
| TMR SEL      | 13               | 11            | I   | Charge timer selection input                                                                                            |
| VCC          | 4                | 3             | I   | Supply voltage                                                                                                          |
| VSEL         | 9                | 7             | I   | 4.1 V or 4.2 V charge regulation selection input                                                                        |
| VSENSE       | 17               | 15            | I   | Battery voltage sense input                                                                                             |



TYPICAL CHARACTERISTICS

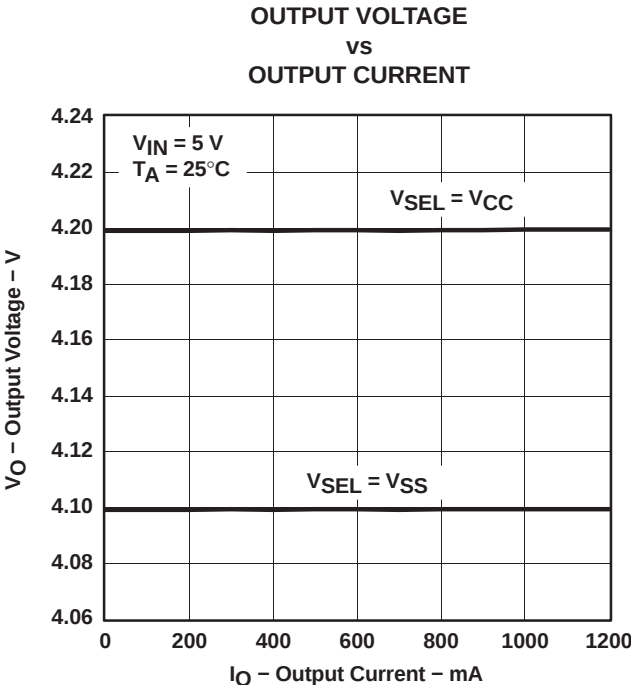


Figure 1

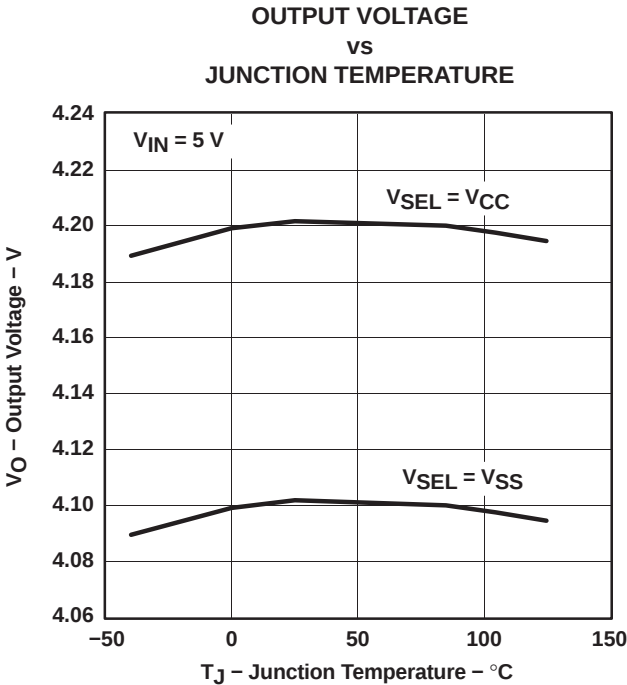


Figure 2

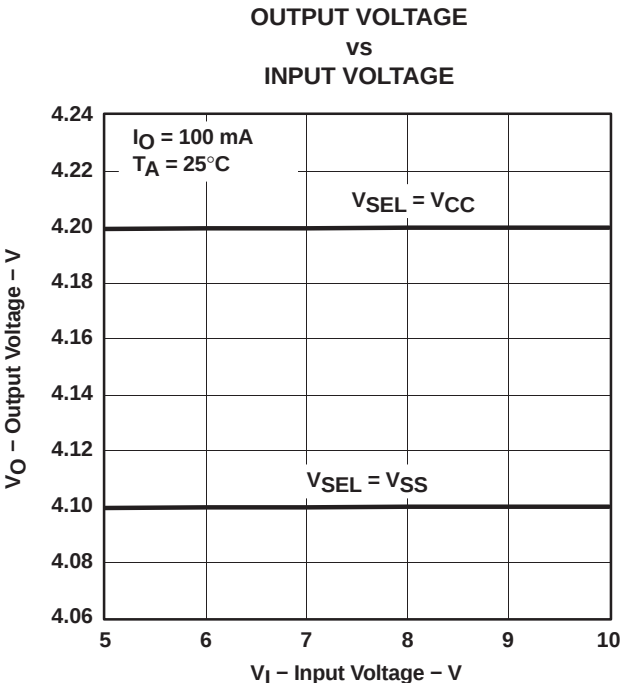


Figure 3

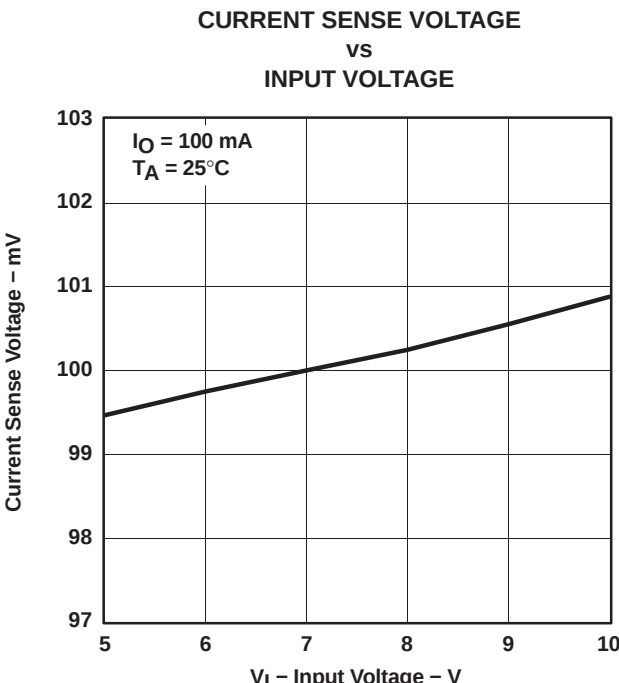


Figure 4

## TYPICAL CHARACTERISTICS

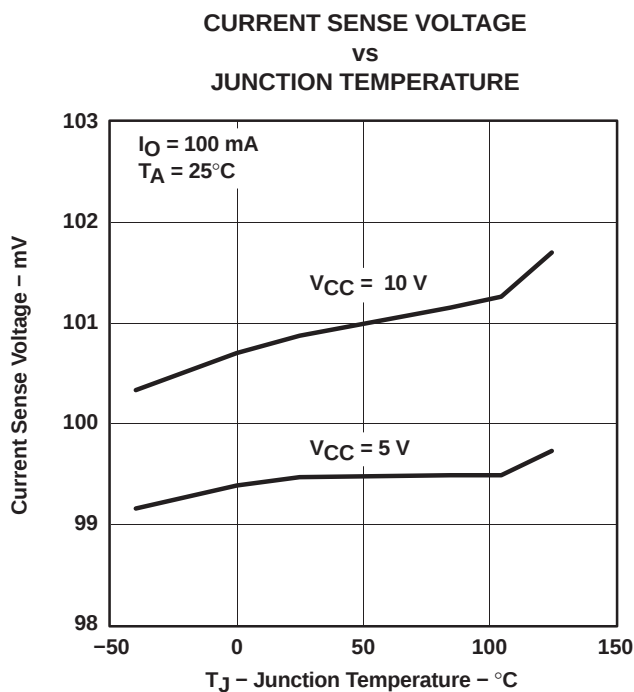


Figure 5

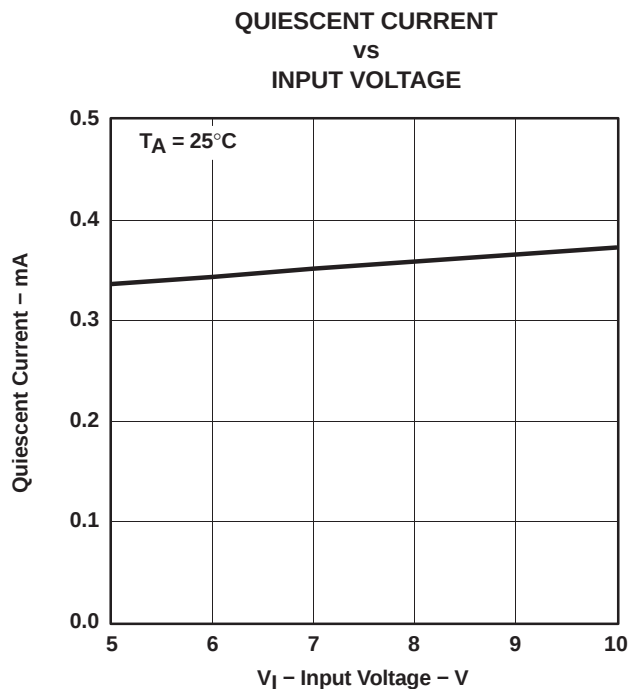


Figure 6

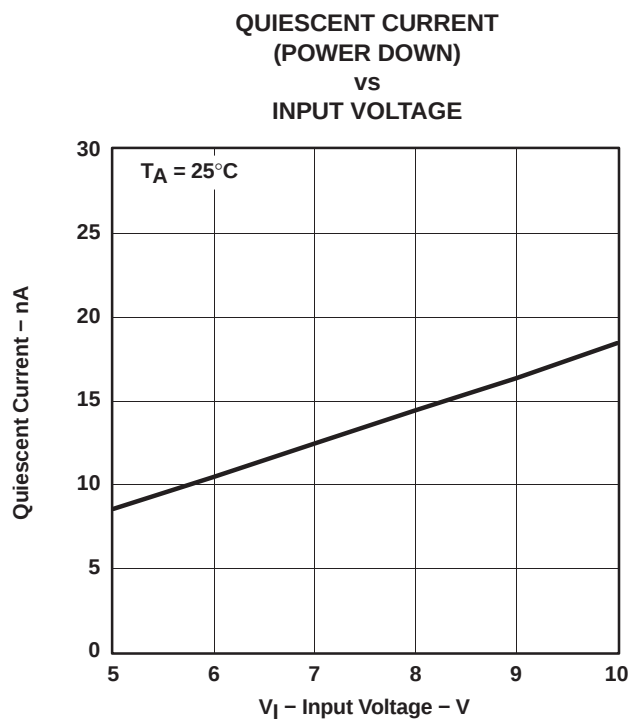


Figure 7

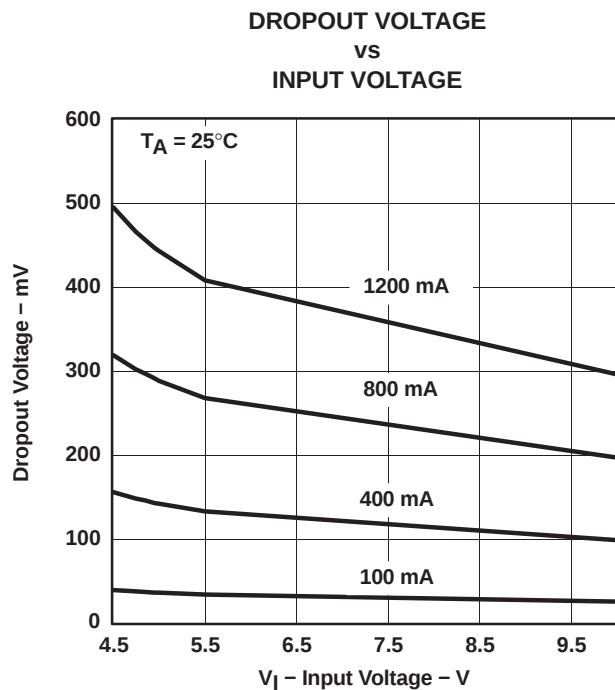


Figure 8

## TYPICAL CHARACTERISTICS

DROPOUT VOLTAGE  
vs  
OUTPUT CURRENT

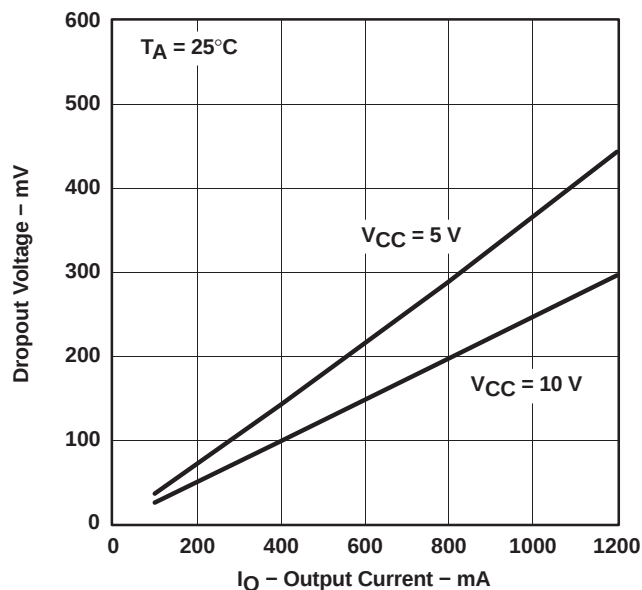


Figure 9

DROPOUT VOLTAGE  
vs  
JUNCTION TEMPERATURE

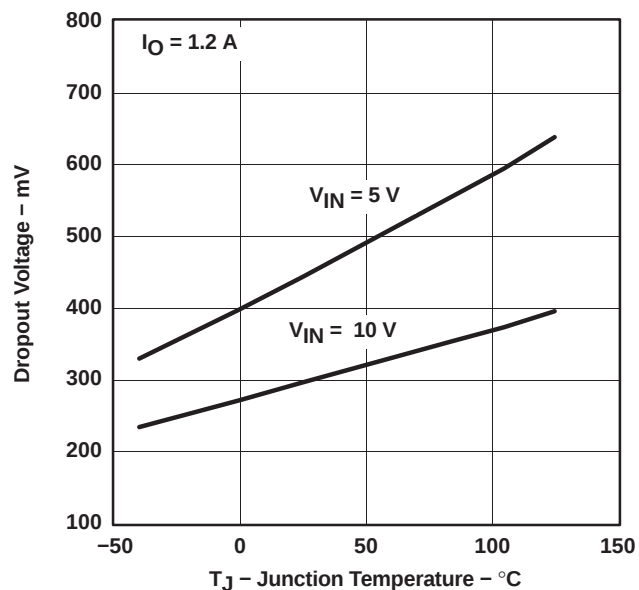


Figure 10

REVERSE CURRENT  
vs  
JUNCTION TEMPERATURE

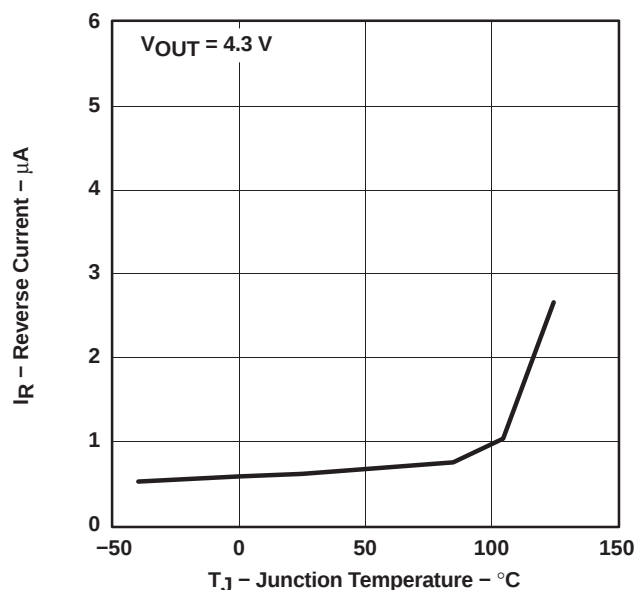


Figure 11

REVERSE CURRENT LEAKAGE  
vs  
VOLTAGE ON OUT PIN

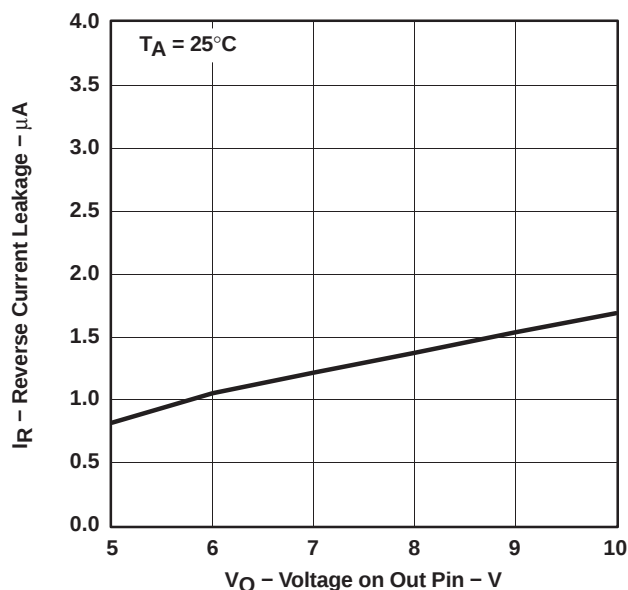


Figure 12

## APPLICATION INFORMATION

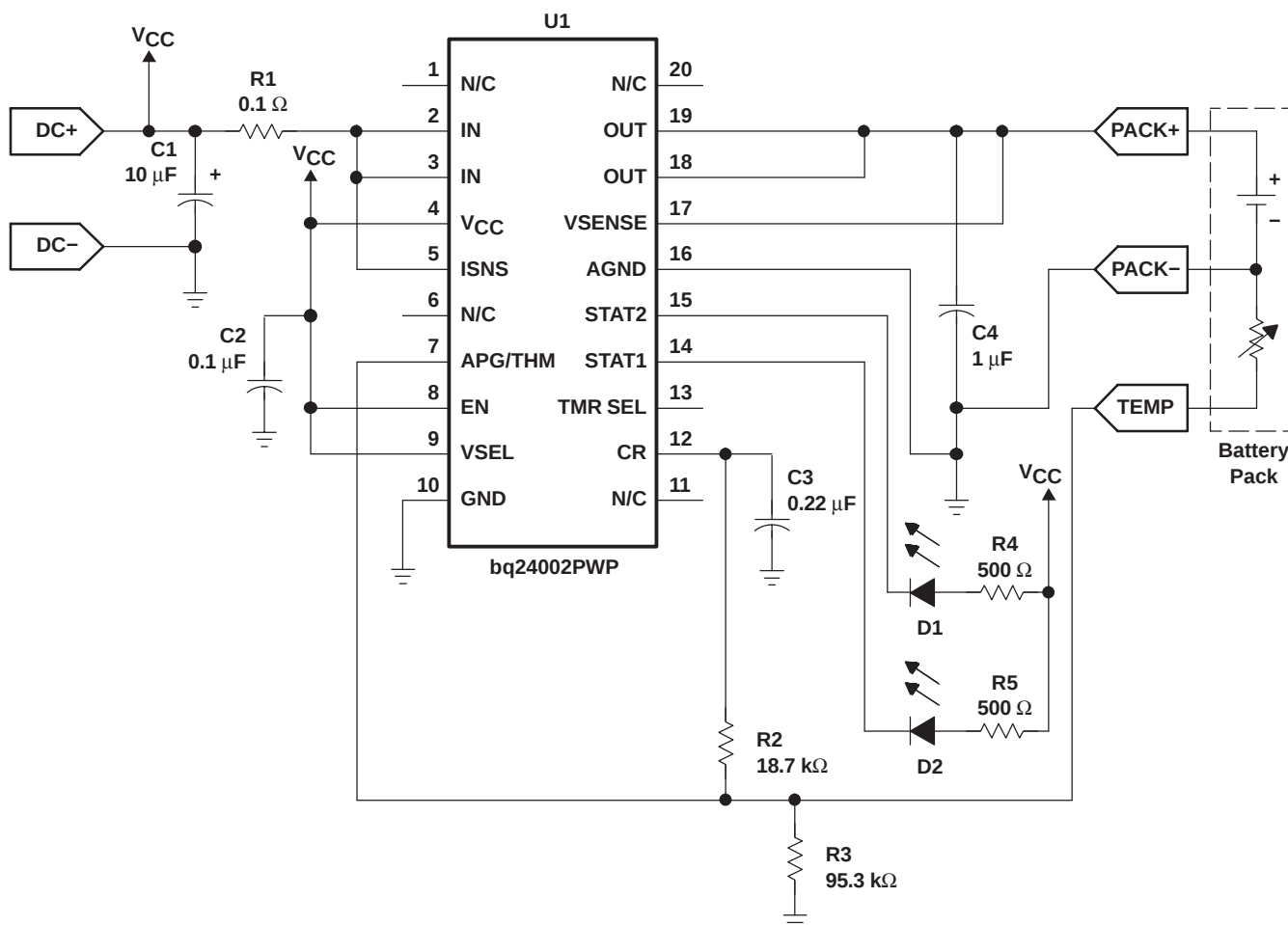


Figure 13. Li-Ion/Li-Pol Charger

- If the TMR SEL pin is left floating (3 HR time), a 10-pF capacitor should be installed between TMR SEL and CR.
- If a micro process is monitoring the STAT pins, it may be necessary to add some hysteresis into the feedback to prevent the STAT pins from cycling while crossing the taper detect threshold (usually less than one half second). See SLUU083 EVM or SLUU113 EVM for additional resistors used for the STAT pins.

## APPLICATION INFORMATION

### FUNCTIONAL DESCRIPTION

The bq2400x supports a precision current- and voltage-regulated Li-Ion charging system suitable for cells with either coke or graphite anodes. See Figure 14 for a typical charge profile and Figure 15 for an operational flowchart.

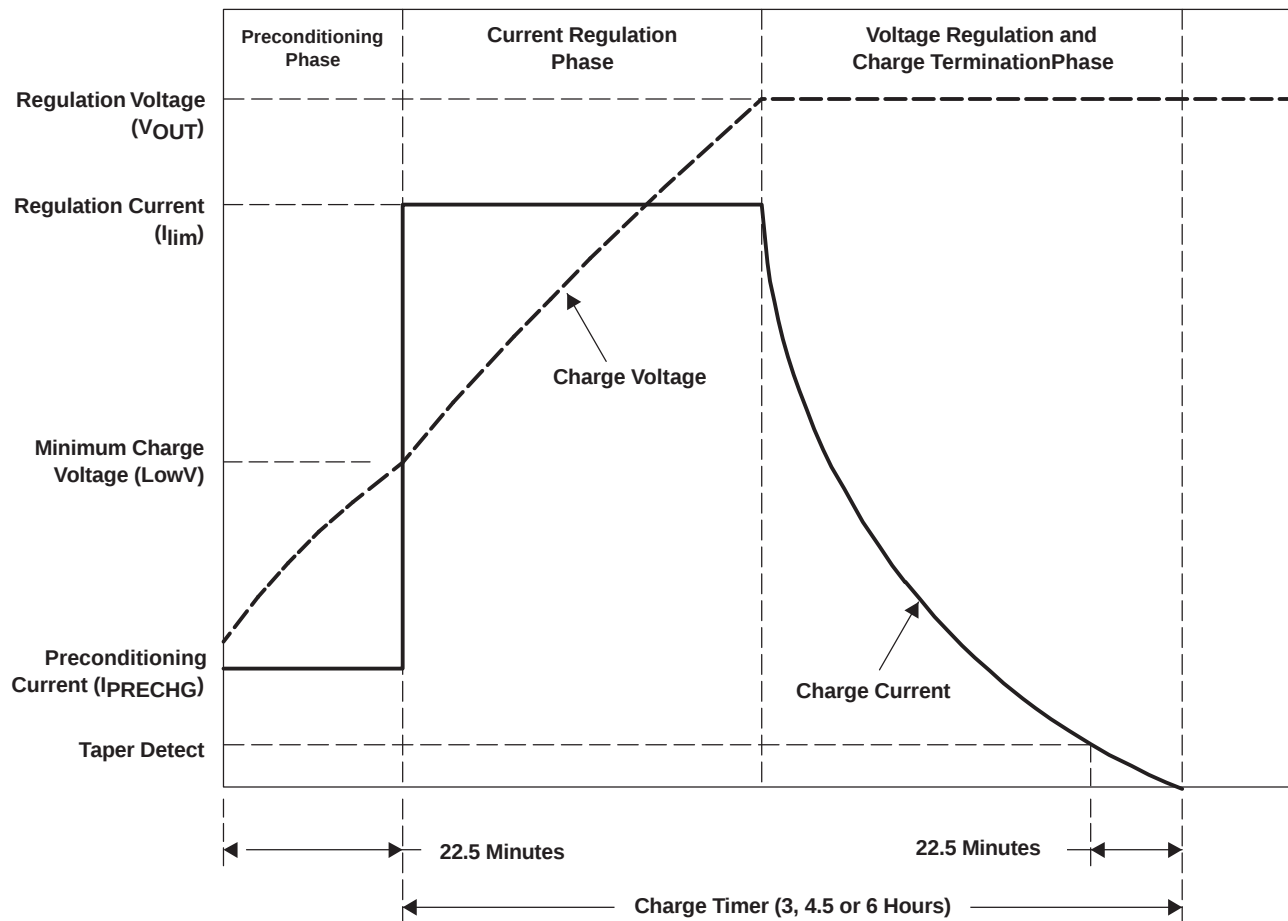


Figure 14. Typical Charge Profile

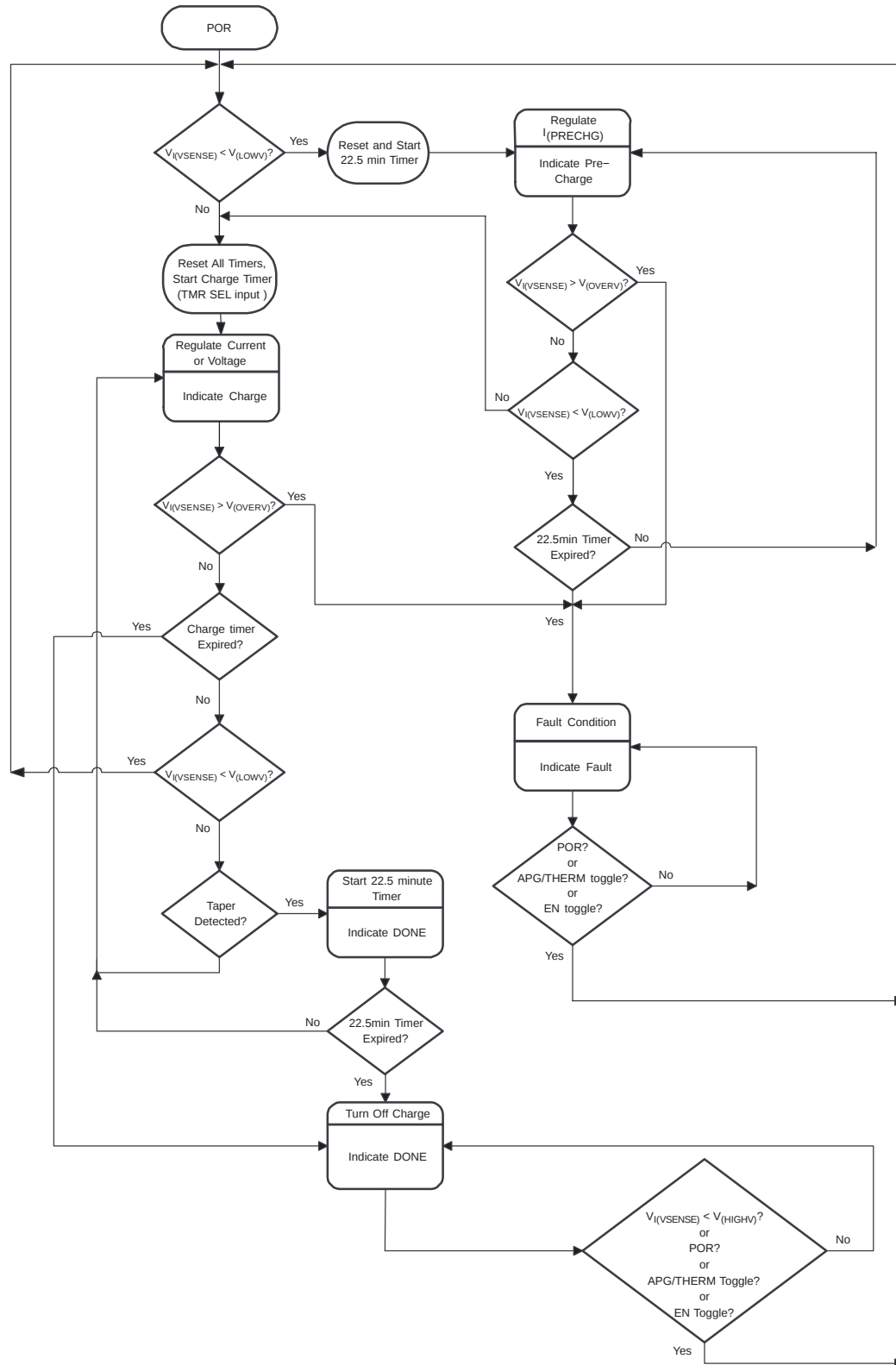


Figure 15. Operational Flow Chart

## Charge Qualification and Preconditioning

The bq2400x starts a charge cycle when power is applied while a battery is present. Charge qualification is based on battery voltage and the APG/THERM input.

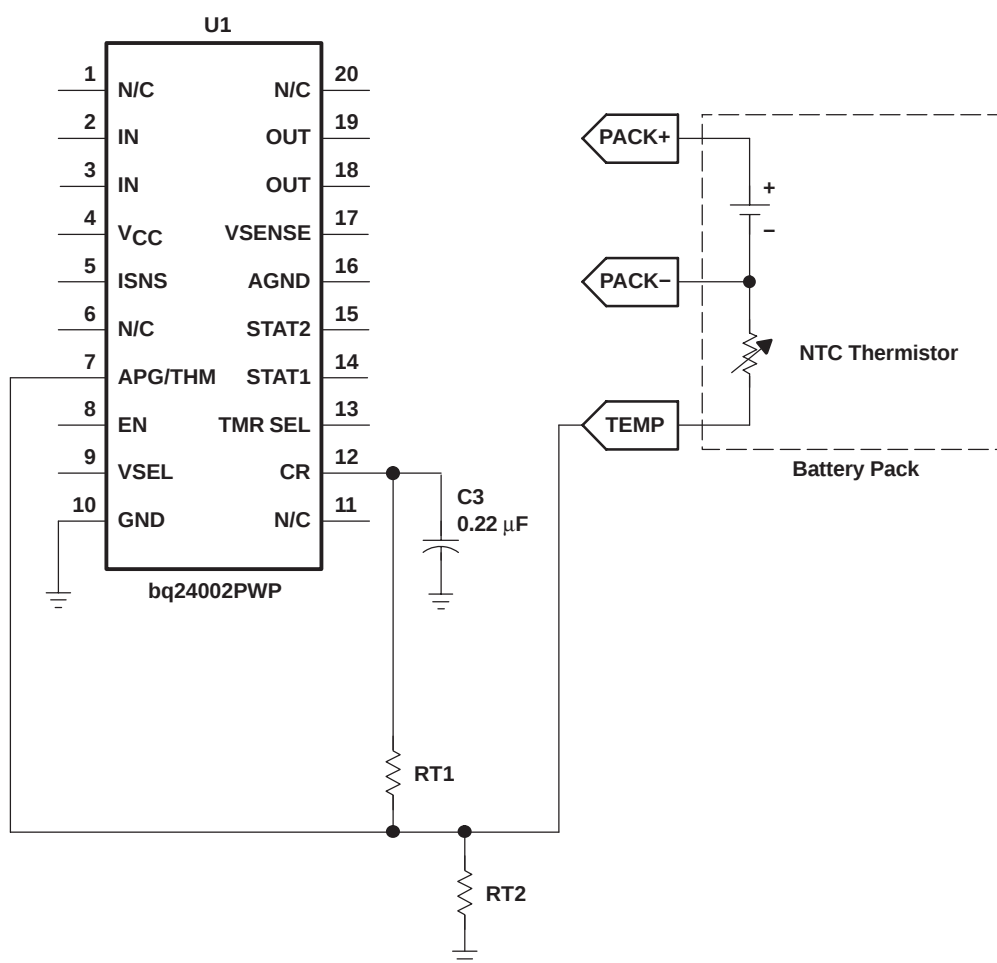
As shown in the block diagram, the internal LowV comparator output prevents fast-charging a deeply depleted battery. When set, charging current is provided by a dedicated precharge current source. The precharge timer limits the precharge duration. The precharge current also minimizes heat dissipation in the pass element during the initial stage of charge.

The APG/THERM input can also be configured to monitor

either the adapter power or the battery temperature using a thermistor. The bq2400x suspends charge if this input is outside the limits set by the user. Please refer to the APG/THERM input section for additional details.

## APG/THERM Input

The bq400x continuously monitors temperature or system input voltage by measuring the voltage between the APG/THERM (adapter power good/thermistor) and GND. For temperature, a negative- or a positive- temperature coefficient thermistor (NTC, PTC) and an external voltage divider typically develop this voltage (see Figure 16). The bq2400x compares this voltage against its internal  $V_{TP1}$  and  $V_{TP2}$  thresholds to determine if charging is allowed. (See Figure 17.)



**Figure 16. Temperature Sensing Circuit**

If the charger designs incorporate a thermistor, the resistor divider RT1 and RT2 is calculated by using the following two equations.

First, calculate RT2.

$$RT2 = \frac{V_B R_H R_C \left[ \frac{1}{V_C} - \frac{1}{V_H} \right]}{R_H \left( \frac{V_B}{V_H} - 1 \right) - R_C \left( \frac{V_B}{V_C} - 1 \right)}$$

then use the resistor value to find RT1.

$$RT1 = \frac{\frac{V_B}{V_C} - 1}{\frac{1}{RT2} + \frac{1}{R_C}}$$

Where:

$V_B = V_{CR}$  (bias voltage)

$R_H$  = Resistance of the thermistor at the desired hot trip threshold

$R_C$  = Resistance of the thermistor at the desired cold trip threshold

$V_H$  = VP2 or the lower APG trip threshold

$V_C$  = VP2 or the upper APG trip threshold

RT1 = Top resistor in the divider string

RT2 = Bottom resistor in the divider string

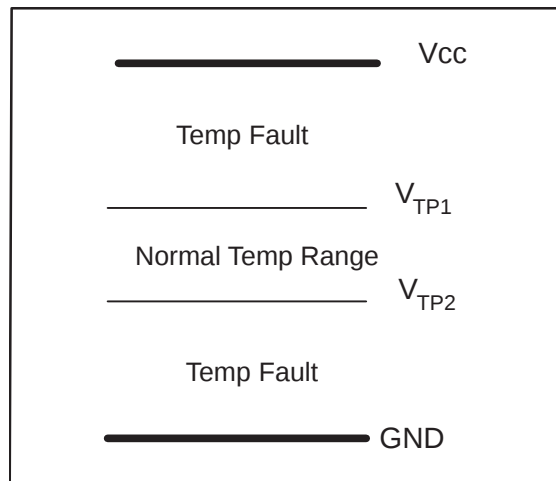


Figure 17. Temperature Threshold

Values of resistors R1 and R2 can be calculated using the following equation:

$$V_{APG} = V_{CC} \frac{R2}{(R1 + R2)}$$

where  $V_{APG}$  is the voltage at the APG/THM pin.

### Current Regulation

The bq2400x provides current regulation while the battery-pack voltage is less than the regulation voltage. The current regulation loop effectively amplifies the error between a reference signal, Vilim, and the drop across the external sense resistor,  $R_{SNS}$ .

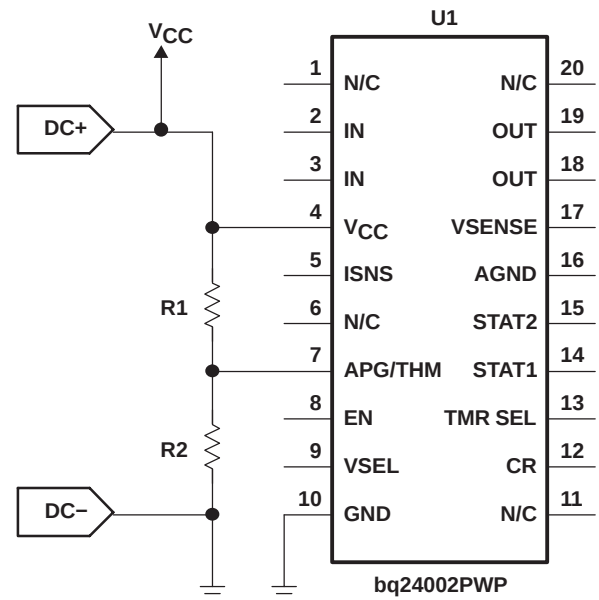


Figure 18. APG Sensing Circuit

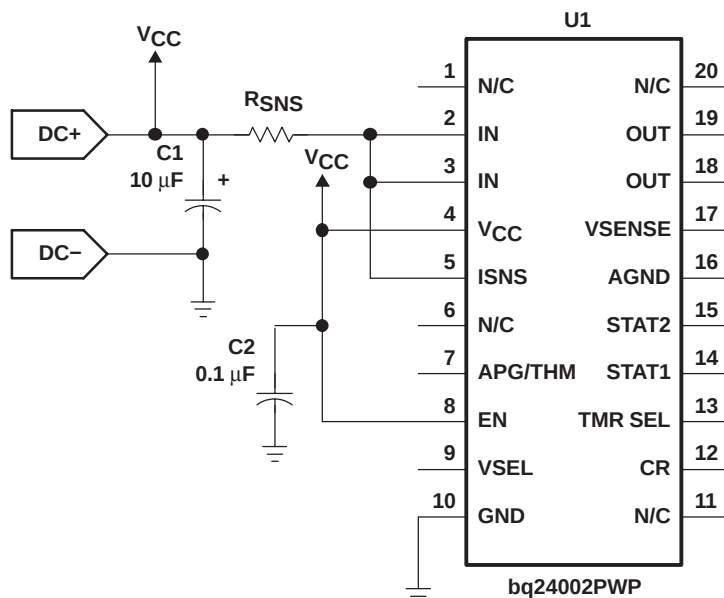


Figure 19. Current Sensing Circuit

Charge current feedback, applied through pin ISNS, maintains regulation around a threshold of Vilim. The following formula calculates the value of the sense resistor:

$$R_{SNS} = \frac{V_{ilim}}{I_{REG}}$$

where I<sub>REG</sub> is the desired charging current.

## Voltage Monitoring and Regulation

Voltage regulation feedback is through pin VSENSE. This input is tied directly to the positive side of the battery pack. The bq2400x supports cells with either coke (4.1 V) or graphite (4.2 V) anode. Pin VSEL selects the charge regulation voltage.

| VSEL State<br>(see Note) | CHARGE REGULATION<br>VOLTAGE |
|--------------------------|------------------------------|
| Low                      | 4.1 V                        |
| High                     | 4.2 V                        |

NOTE: VSEL should not be left floating.

## Charge Termination

The bq2400x continues with the charge cycle until termination by one of the two possible termination conditions:

**Maximum Charge Time:** The bq2400x sets the maximum charge time through pin TMRSEL. The TMR SEL pin allows the user to select between three different total charge-time timers (3, 4, 5, or 6 hours). The charge timer is initiated after the preconditioning phase of the charge and is reset at the beginning of a new charge cycle. Note

that in the case of a fault condition, such as an out-of-range signal on the APG/THERM input or a thermal shutdown, the bq2400x suspends the timer.

| TMRSEL STATE            | CHARGE TIME |
|-------------------------|-------------|
| Floating <sup>(1)</sup> | 3 hours     |
| Low                     | 6 hours     |
| High                    | 4.5 hours   |

<sup>(1)</sup> To improve noise immunity, it is recommended that a minimum of 10 pF capacitor be tied to Vss on a floating pin.

**Minimum Current:** The bq2400x monitors the charging current during the voltage regulation phase. The bq2400x initiates a 22-minute timer once the current falls below the taperdet trip threshold. Fast charge is terminated once the 22-minute timer expires.

## Charge Status Display

The three available options allow the user to configure the charge status display for single LED (bq24001), two individual LEDs (bq24002) or a bicolor LED (bq24003). The output stage is totem pole for the bq24001 and bq24003 and open-drain for the bq24002. The following tables summarize the operation of the three options:

Table 1. bq24001 (Single LED)

| CHARGE STATE      | STAT1                           |
|-------------------|---------------------------------|
| Precharge         | ON (LOW)                        |
| Fast charge       | ON (LOW)                        |
| FAULT             | Flashing (1 Hz, 50% duty cycle) |
| Done (>90%)       | OFF (HIGH)                      |
| Sleep-mode        | OFF (HIGH)                      |
| APG/Therm invalid | OFF (HIGH)                      |
| Thermal shutdown  | OFF (HIGH)                      |
| Battery absent    | OFF (HIGH)                      |

**Table 2. bq24002 (2 Individual LEDs)**

| CHARGE STATE      | STAT1 (RED)                     | STAT2 (GREEN) |
|-------------------|---------------------------------|---------------|
| Precharge         | ON (LOW)                        | OFF           |
| Fast charge       | ON (LOW)                        | OFF           |
| FAULT             | Flashing (1 Hz, 50% duty cycle) | OFF           |
| Done (>90%)       | OFF                             | ON (LOW)      |
| Sleep-mode        | OFF                             | OFF           |
| APG/Therm invalid | OFF                             | OFF           |
| Thermal shutdown  | OFF                             | OFF           |
| Battery absent    | OFF                             | OFF(1)        |

(1) If thermistor is used, then the Green LED is off.

### Thermal Shutdown

The bq2400x monitors the junction temperature  $T_J$  of the DIE and suspends charging if  $T_J$  exceeds 165°C. Charging resumes when  $T_J$  falls below 155°C.

**Table 3. bq24003 (Single Bicolor LED)**

| CHARGE STATE      | LED1 (RED) | LED2 (GREEN)  | APPARENT COLOR |
|-------------------|------------|---------------|----------------|
| Precharge         | ON (LOW)   | OFF (HIGH)    | RED            |
| Fast charge       | ON (LOW)   | OFF (HIGH)    | RED            |
| FAULT             | ON (LOW)   | ON (LOW)      | YELLOW         |
| Done (>90%)       | OFF (HIGH) | ON (LOW)      | GREEN          |
| Sleep-mode        | OFF (HIGH) | OFF (HIGH)    | OFF            |
| APG/Therm invalid | OFF (HIGH) | OFF (HIGH)    | OFF            |
| Thermal shutdown  | OFF (HIGH) | OFF (HIGH)    | OFF            |
| Battery absent    | OFF (HIGH) | OFF (HIGH)(1) | OFF(1)         |

(1) If thermistor is used, then the Green LED is off.

## DETAILED DESCRIPTION

### POWER FET

The integrated transistor is a P-channel MOSFET. The power FET features a reverse-blocking Schottky diode, which prevents current flow from OUT to IN.

An internal thermal-sense circuit shuts off the power FET when the junction temperature rises to approximately 165°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 10°C, the power FET turns back on. The power FET continues to cycle off and on until the fault is removed.

### CURRENT SENSE

The bq2400x regulates current by sensing, on the ISNS pin, the voltage drop developed across an external sense resistor. The sense resistor must be placed between the supply voltage ( $V_{CC}$ ) and the input of the IC (IN pins).

### VOLTAGE SENSE

To achieve maximum voltage regulation accuracy, the bq2400x uses the feedback on the VSENSE pin. Externally, this pin should be connected as close to the battery cell terminals as possible. For additional safety, a 10k $\Omega$  internal pullup resistor is connected between the VSENSE and OUT pins.

### ENABLE (EN)

The logic EN input is used to enable or disable the IC. A high-level signal on this pin enables the bq2400x. A low-level signal disables the IC and places the device in a low-power standby mode.

## THERMAL INFORMATION

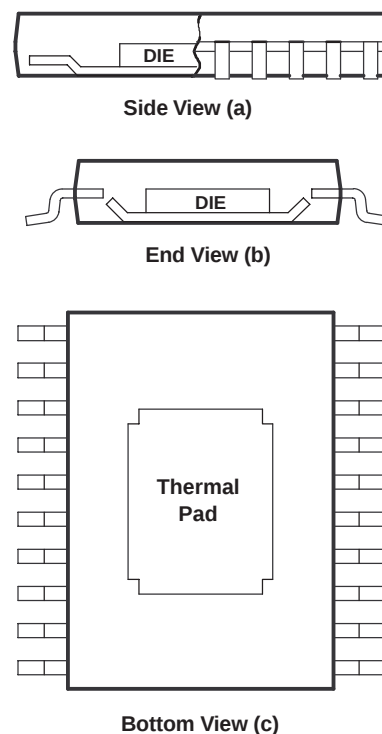
### THERMALLY ENHANCED TSSOP-20

The thermally enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad (see Figure 20) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements ( $<2$  mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.



**Figure 20. Views of Thermally Enhanced PWP Package**

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air. (Reference Figure 22(a), 8 cm<sup>2</sup> of copper heat sink and natural convection.) Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see Figure 22(b) and 22(c)). The line drawn at 0.3 cm<sup>2</sup> in Figures 21 and 22 indicates performance at the minimum recommended heat-sink size.

## THERMAL INFORMATION

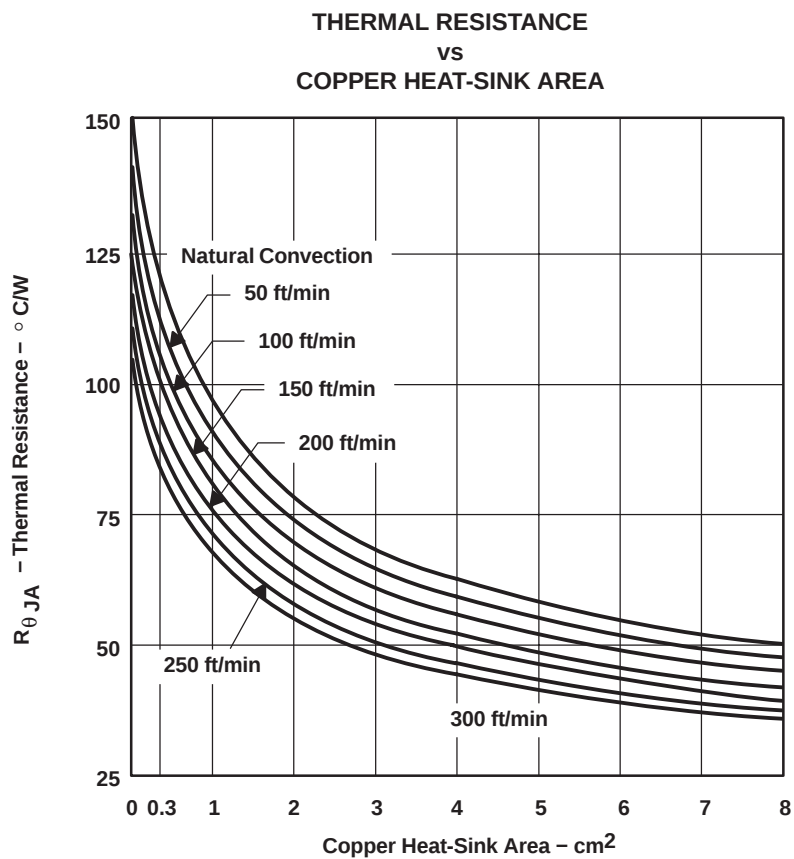
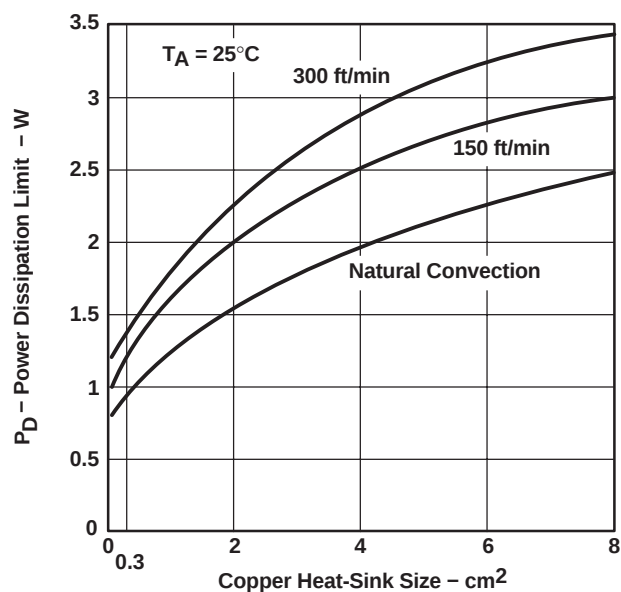
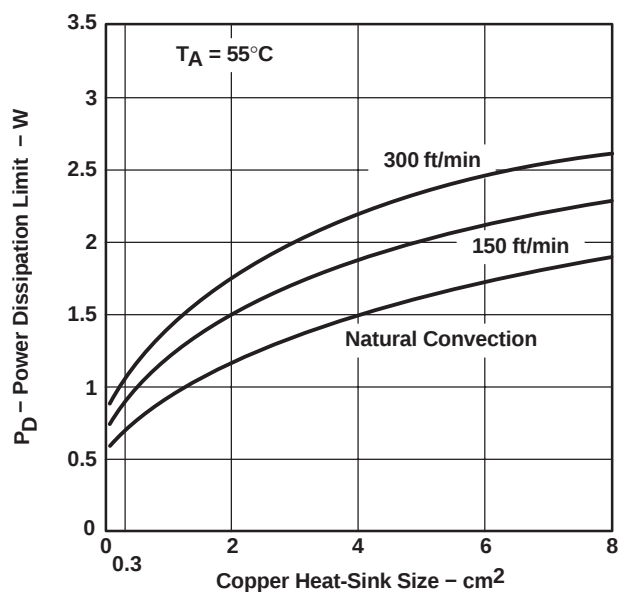


Figure 21

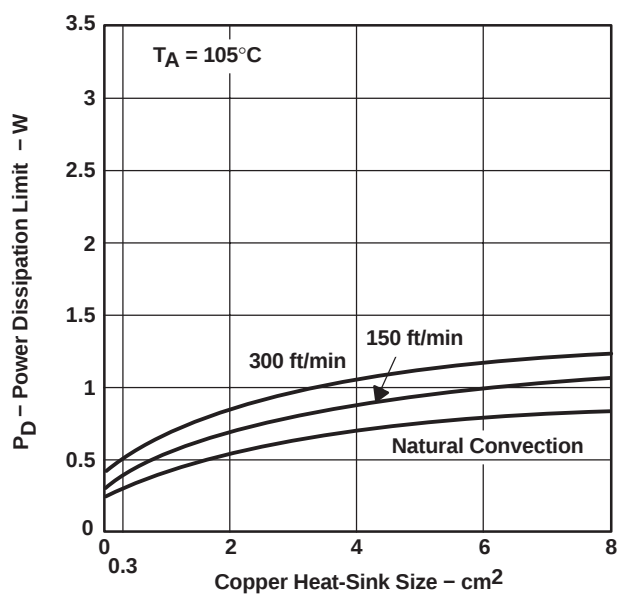
## THERMAL INFORMATION



(a)



(b)



(c)

Figure 22. Power Ratings of the PWP Package at Ambient Temperatures of  $25^\circ\text{C}$ ,  $55^\circ\text{C}$ , and  $105^\circ\text{C}$

## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">BQ24001PWP</a>  | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | BQ24001             |
| BQ24001PWP.A                | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | BQ24001             |
| <a href="#">BQ24002PWP</a>  | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 0       | BQ24002             |
| BQ24002PWP.A                | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 0       | BQ24002             |
| <a href="#">BQ24002PWPR</a> | Active        | Production           | HTSSOP (PWP)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 0       | BQ24002             |
| BQ24002PWPR.A               | Active        | Production           | HTSSOP (PWP)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 0       | BQ24002             |
| <a href="#">BQ24002RGWR</a> | Active        | Production           | VQFN (RGW)   20   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 0       | 24002               |
| BQ24002RGWR.A               | Active        | Production           | VQFN (RGW)   20   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 0       | 24002               |
| <a href="#">BQ24003PWP</a>  | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | BQ24003             |
| BQ24003PWP.A                | Active        | Production           | HTSSOP (PWP)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | BQ24003             |
| <a href="#">BQ24003PWPR</a> | Active        | Production           | HTSSOP (PWP)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | BQ24003             |
| BQ24003PWPR.A               | Active        | Production           | HTSSOP (PWP)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | BQ24003             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ24002PWPR | HTSSOP       | PWP             | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| BQ24002RGWR | VQFN         | RGW             | 20   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |
| BQ24003PWPR | HTSSOP       | PWP             | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ24002PWPR | HTSSOP       | PWP             | 20   | 2000 | 350.0       | 350.0      | 43.0        |
| BQ24002RGWR | VQFN         | RGW             | 20   | 3000 | 353.0       | 353.0      | 32.0        |
| BQ24003PWPR | HTSSOP       | PWP             | 20   | 2000 | 350.0       | 350.0      | 43.0        |

## TUBE



\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| BQ24001PWP   | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| BQ24001PWP.A | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| BQ24002PWP   | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| BQ24002PWP.A | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| BQ24003PWP   | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| BQ24003PWP.A | PWP          | HTSSOP       | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |

## GENERIC PACKAGE VIEW

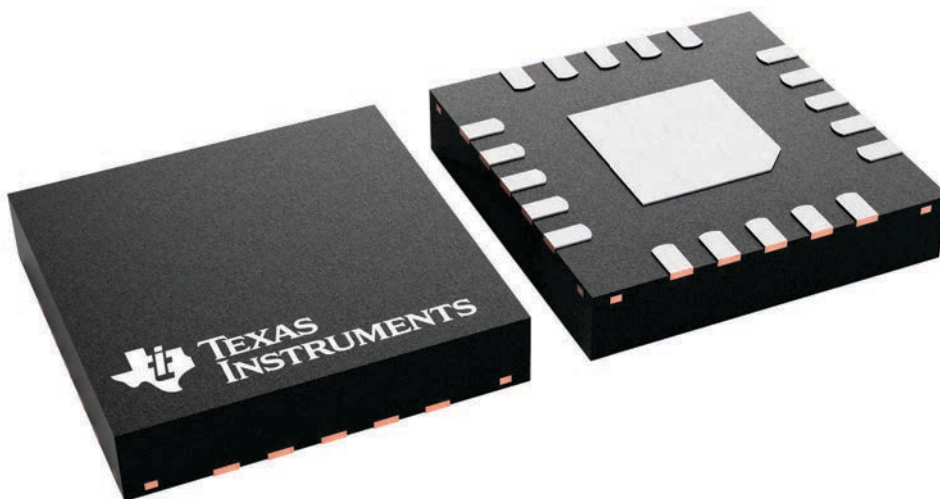
**RGW 20**

**VQFN - 1 mm max height**

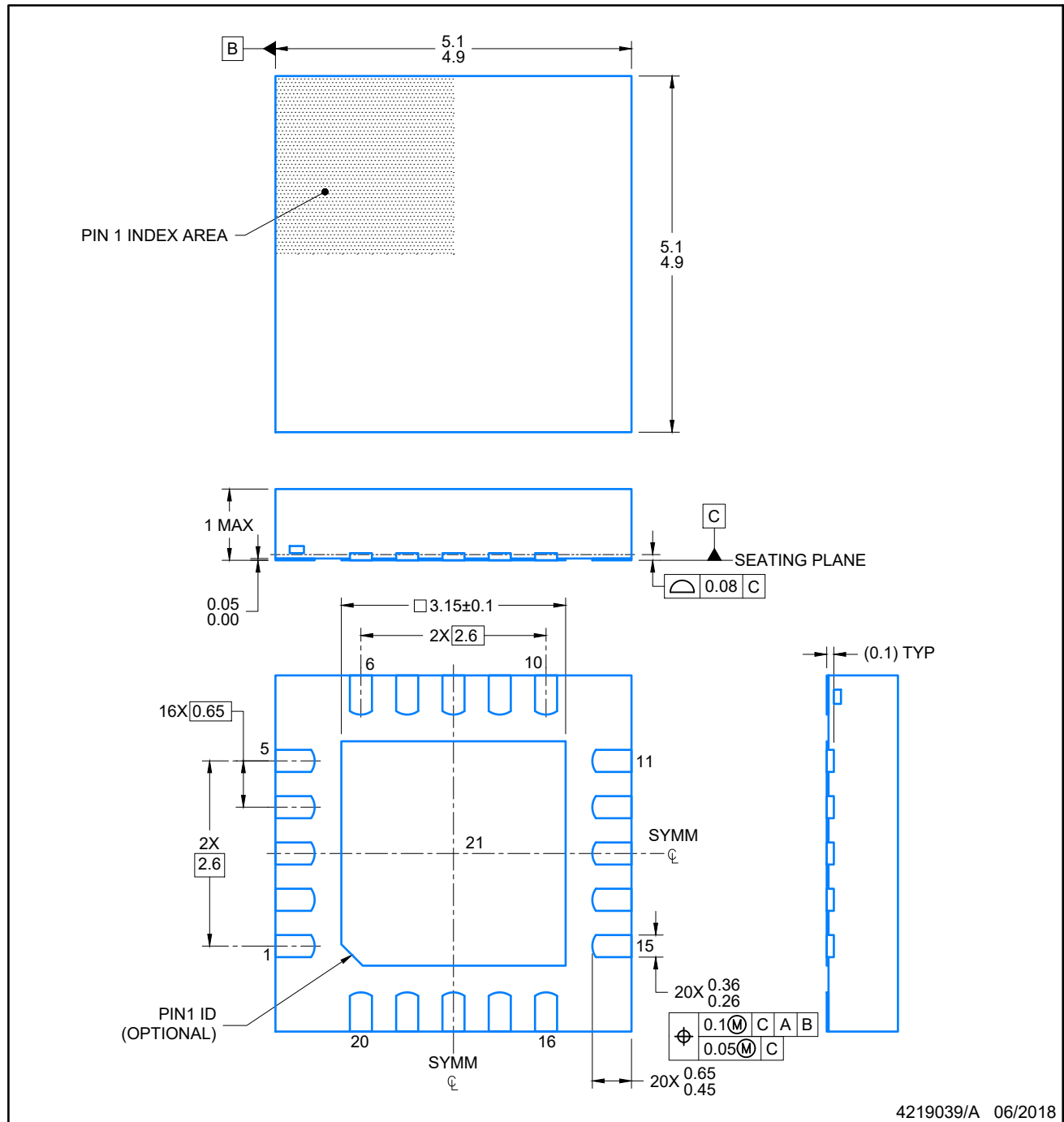
5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

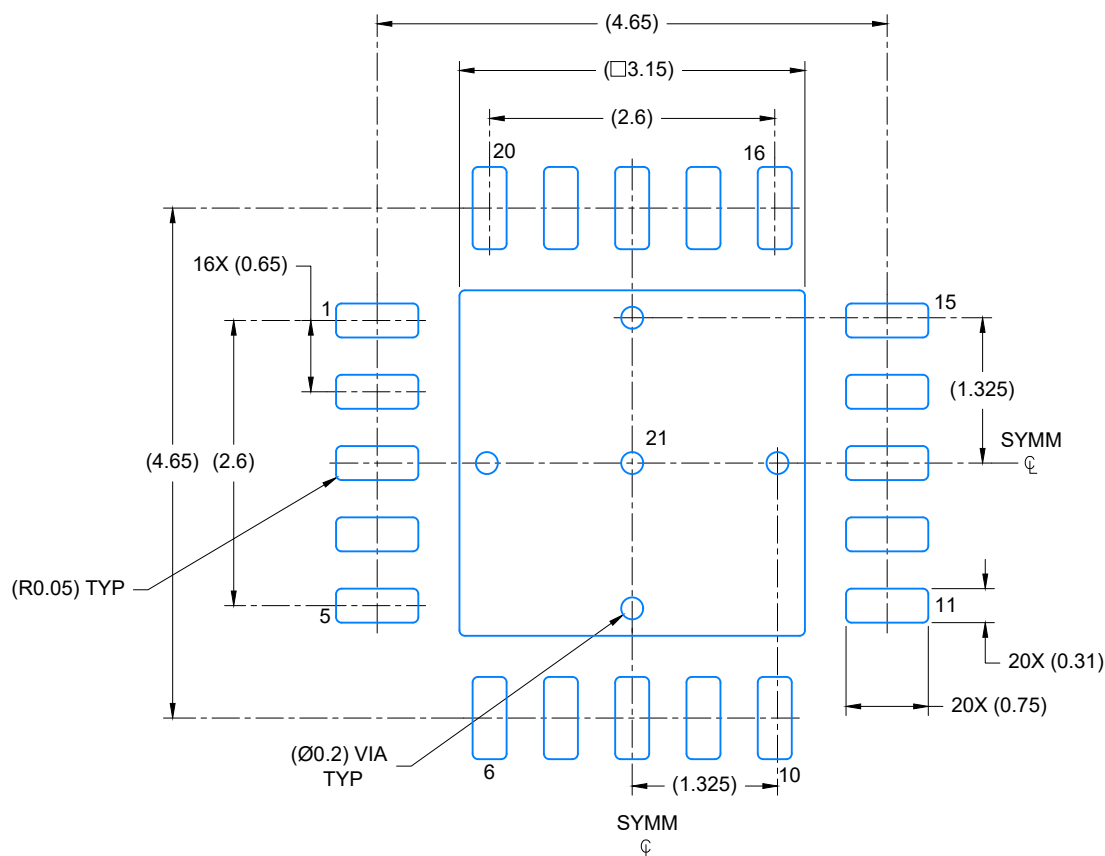


4227157/A



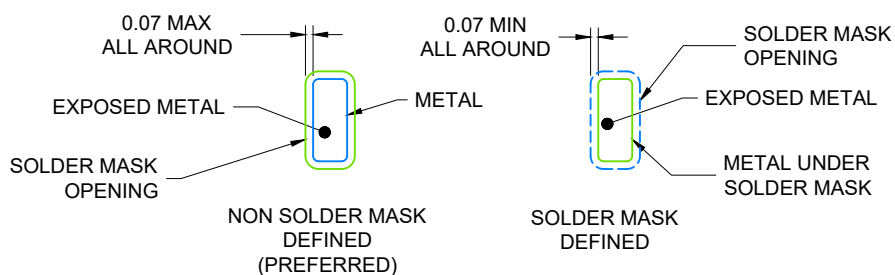
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



## LAND PATTERN EXAMPLE

SCALE: 15X

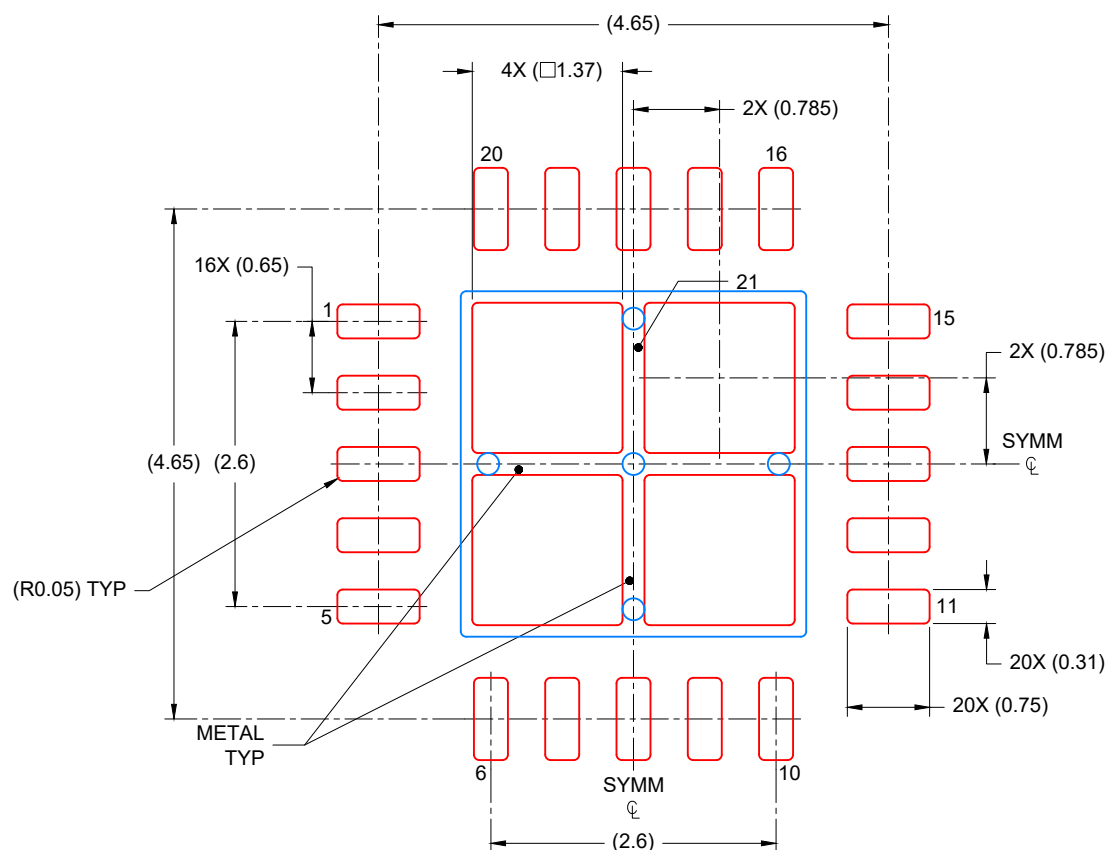


## SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 75% PRINTED COVERAGE BY AREA  
 SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

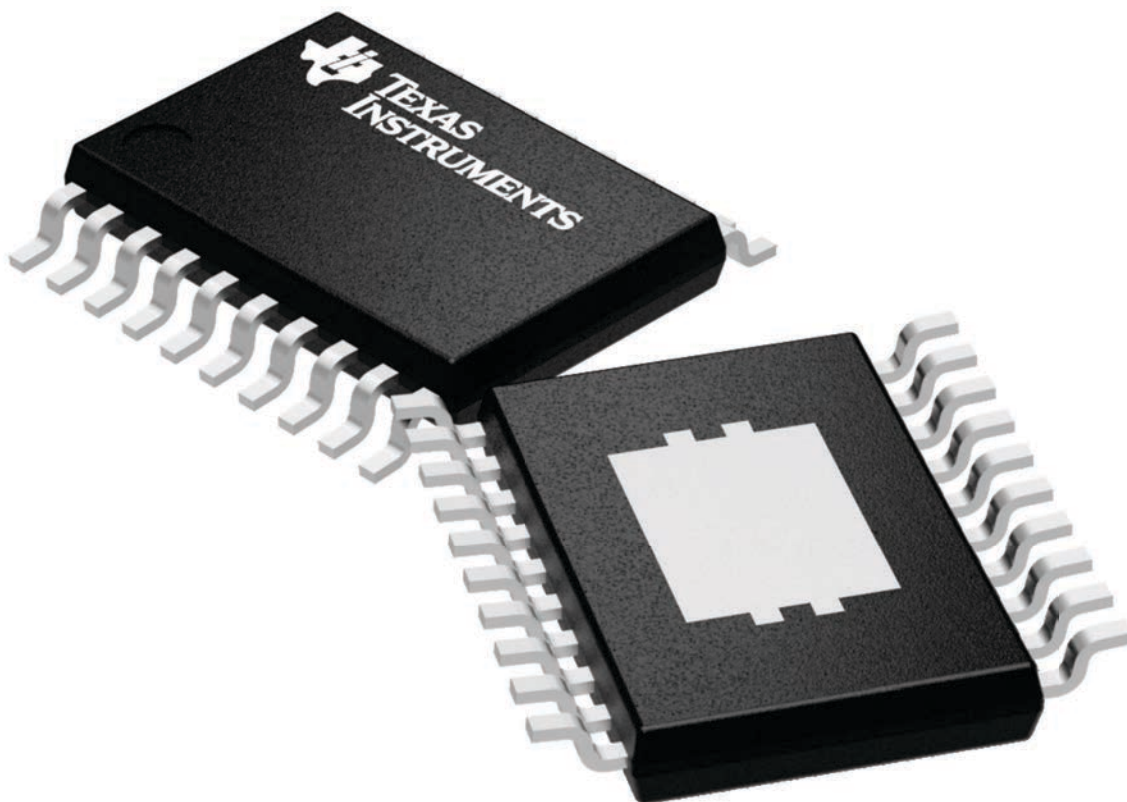
**PWP 20**

**HTSSOP - 1.2 mm max height**

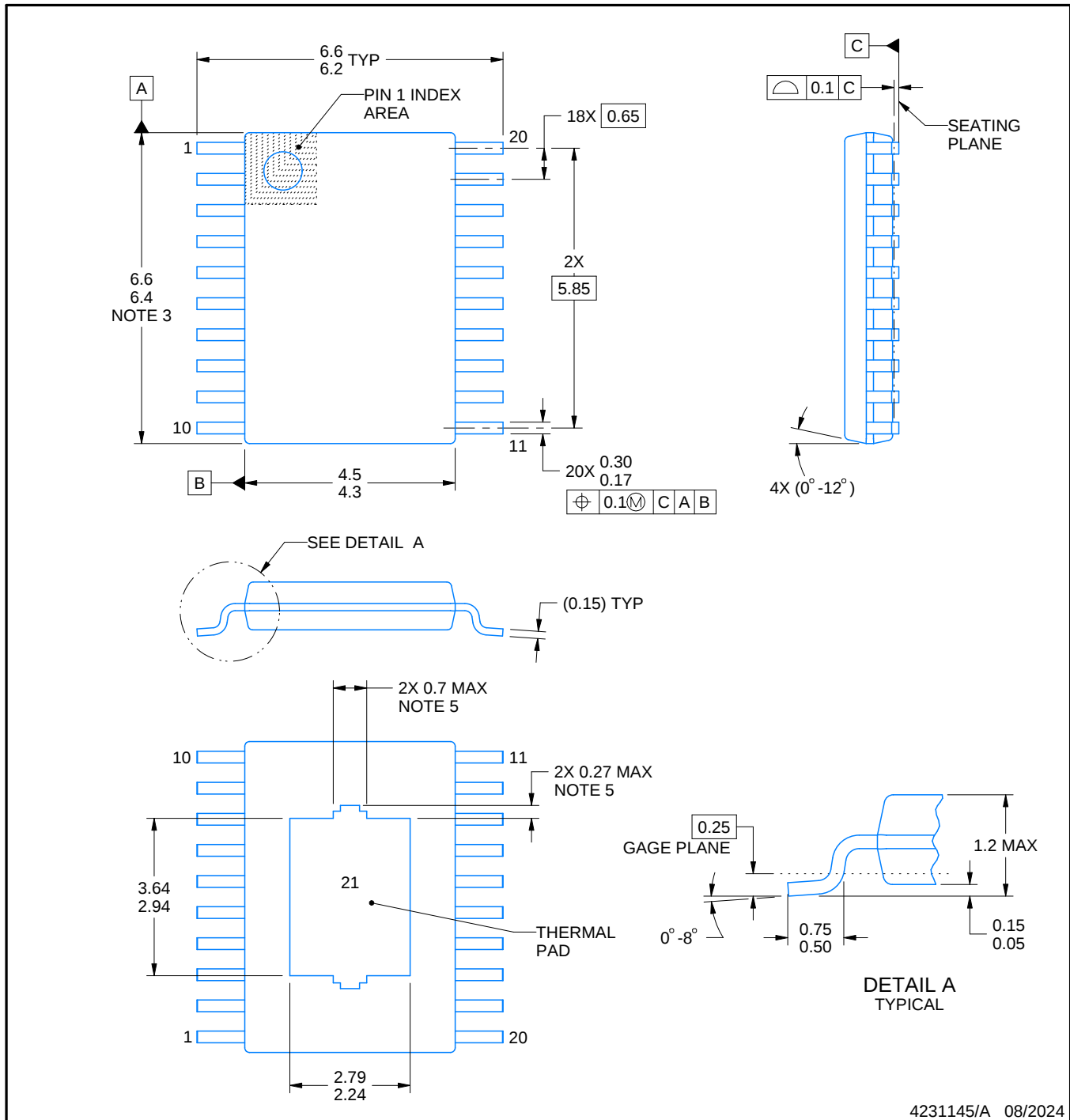
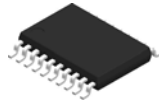
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224669/A



4231145/A 08/2024

PowerPAD is a trademark of Texas Instruments.

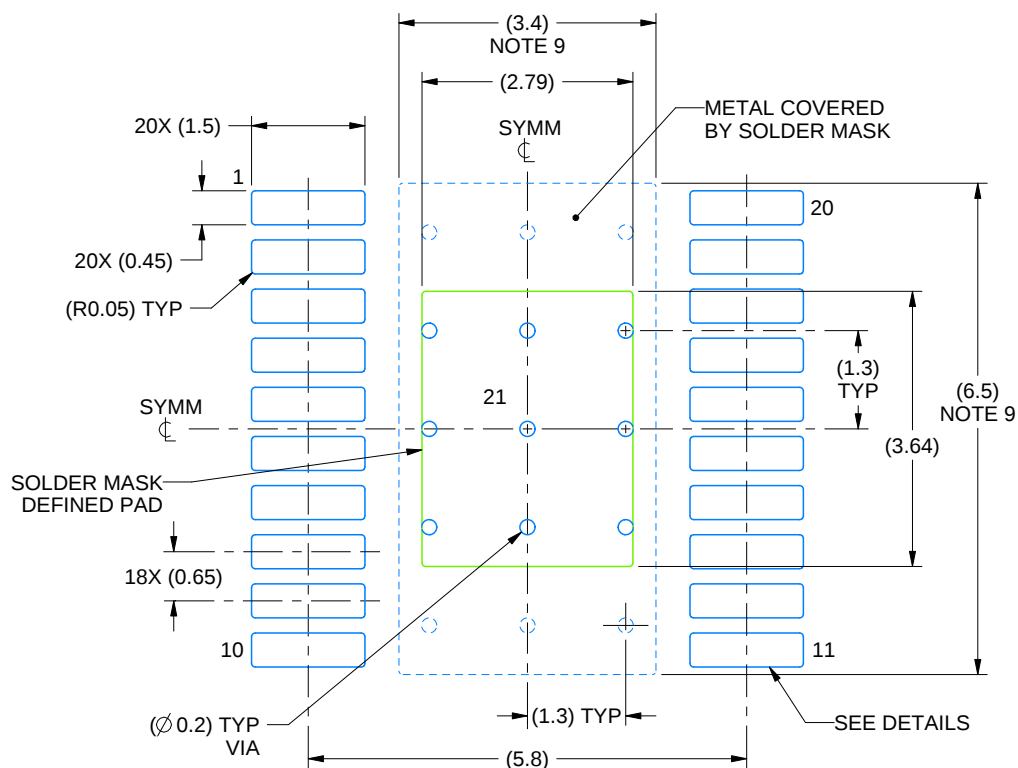
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

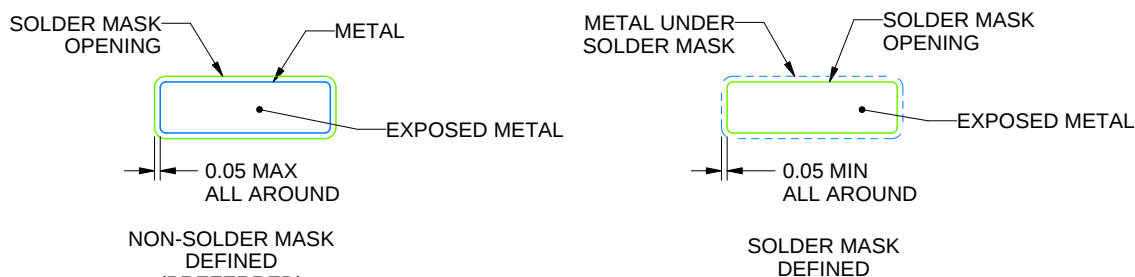
**PWP0020W**

## PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4231145/A 08/2024

NOTES: (continued)

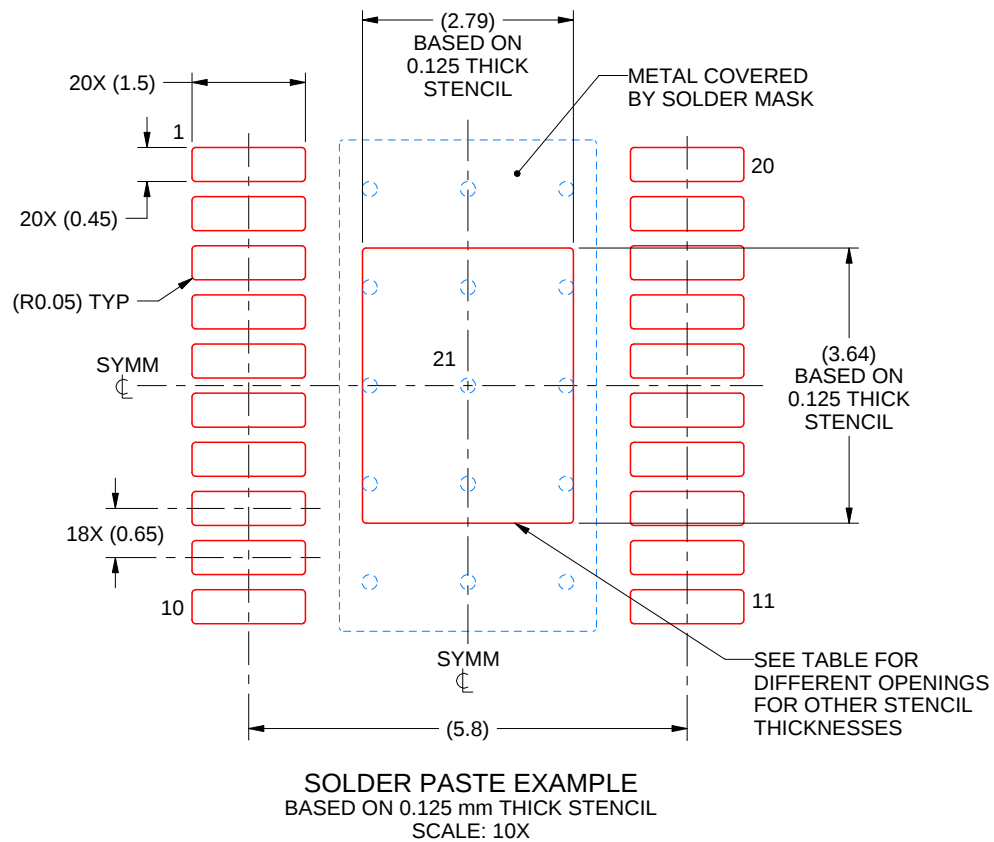
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 3.12 X 4.07            |
| 0.125             | 2.79 X 3.64 (SHOWN)    |
| 0.15              | 2.55 X 3.32            |
| 0.175             | 2.36 X 3.08            |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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