Benchmarq Products from Texas Instruments

bq2003

Fast-Charge IC

Features

- Fast charge and conditioning of nickel cadmium or nickel-metal hydride batteries
- Hysteretic PWM switch-mode current regulation or gated control of an external regulator
- Easily integrated into systems or used as a stand-alone charger
- Pre-charge qualification of temperature and voltage
- Direct LED outputs display battery and charge status
- Fast-charge termination by Δ temperature/Δ time, -ΔV, maximum voltage, maximum temperature, and maximum time
- Optional top-off charge

General Description

The bq2003 Fast Charge IC provides comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device.

Integration of closed-loop current control circuitry allows the bq2003 to be the basis of a cost-effective solution for stand-alone and system-integrated chargers for batteries of one or more cells.

Switch-activated discharge-before-charge allows bq2003-based chargers to support battery conditioning and capacity determination.

High-efficiency power conversion is accomplished using the bq2003 as a hysteretic PWM controller for switch-mode regulation of the charging current. The bq2003 may alternatively be used to gate an externally regulated charging current.

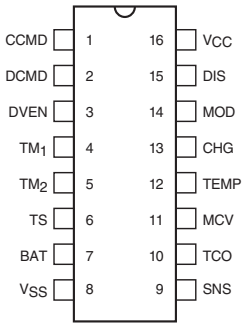
Fast charge may begin on application of the charging supply, replacement of the battery, or switch depression. For safety, fast charge is inhibited unless/until the battery temperature and voltage are within configured limits.

Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Rate of temperature rise ($\Delta T/\Delta t$)
- Negative delta voltage ($-\Delta V$)
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, an optional top-off phase is available. Constant-current maintenence charge is provided by an external trickle resistor.

Pin Connections



16-Pin DIP or SOIC

PN200301.eps

Pin Names

CCMD	Charge command/select
DCMD	Discharge command
DVEN	-ΔV enable/disable
TM_1	Timer mode select 1
TM_2	Timer mode select 2
TS	Temperature sense
BAT	Battery voltage
V_{SS}	System ground
SNS	Sense resistor input
TCO	Temperature cutoff
MCV	Maximum voltage
TEMP	Temperature status output
CHG	Charging status output
MOD	Charge current control
DIS	Discharge control
V_{CC}	5.0V ±10% power

Pin Descriptions

CCMD, DCMD **Charge initiation and discharge-before-charge control inputs**

These two inputs control the conditions that begin a new charge cycle and enable discharge-before-charge. See Table 1.

DVEN **-ΔV enable input**

This input enales/disables -ΔV charge termination. If DVEN is high, the -ΔV test is enabled. If DVEN is low, -ΔV test is disabled. The state of DVEN may be changed at any time.

TM_1–TM_2 **Timer mode inputs**

TM_1 and TM_2 are three-state inputs that configure the fast charge safety timer, -ΔV hold-off time, and that enhance/disable top-off. See Table 2.

TS **Temperature sense input**

Input, referenced to SNS, for an external thermistor monitoring battery temperature.

BAT **Single-cell voltage input**

The battery voltage sense input, referenced to SNS. This is created by a high-impedance resistor divider network connected between the positive and the negative terminals of the battery.

Vss **Ground**

SNS **Charging current sense input**

SNS controls the switching of MOD based on the voltage across an external sense resistor in the current path of the battery. SNS is the reference potential for the TS and BAT pins. If SNS is connected to V_{SS}, MOD switches high at the beginning of charge and low at the end of charge.

TCO **Temperature cutoff threshold input**

Input to set maximum allowable battery temperature. If the potential between TS and SNS is less than the voltage at the TCO input, then fast charge or top-off charge is terminated.

MCV **Maximum-Cell-Voltage threshold input**

Input to set maximum single-cell equivalent voltage. If the voltage between BAT and SNS is greater than or equal to the voltage at the MCV input, then fast charge or top-off charge is inhibited.

Note: For valid device operation, the voltage level on MCV must not exceed $0.6 * V_{CC}$.

TEMP **Temperature status output**

Push-pull output indicating temperature status. TEMP is low if the voltage at the TS pin is not within the allowed range to start fast charge.

CHG **Charging status output**

Push-pull output indicating charging status. See Figure 1.

MOD **Current-switching control output**

MOD is a push/pull output that is used to control the charging current to the battery. MOD switches high to enable charging current flow and low to inhibit charging current flow.

DIS **Discharge FET control output**

Push-pull output used to control an external transistor to discharge the battery before charging.

V_{CC} **V_{CC} supply input**

5.0 V, ±10% power input.

Functional Description

Figure 3 shows a state diagram and Figure 4 shows a block diagram of the bq2003.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of:

$$\frac{RB1}{RB2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1MΩ.

A ground-referenced negative temperature coefficient thermistor placed in proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and battery's negative terminal See Figure 1. Both the BAT and TS inputs are referenced to SNS, so the signals used inside the IC are:

$$V_{BAT} - V_{SNS} = V_{CELL}$$

and

$$V_{TS} - V_{SNS} = V_{TEMP}$$

Table 1. New Charge Cycle and Discharge Stimulus

CCMD Pulled Up/Down to:	DCMD Pulled Up/Down to:	New Charge Cycle Started by:	Discharge-Before-Charge Started by:
V_{SS}	V_{SS}	V_{CC} rising to valid level	A rising edge on DCMD
		Battery replacement (V_{CELL} falling through V_{MCV})	
		A rising edge on CCMD	
V_{CC}	V_{CC}	V_{CC} rising to valid level	A rising edge on DCMD
		Battery replacement (V_{CELL} falling through V_{MCV})	
		A falling edge on CCMD or DCMD	
V_{CC}	V_{SS}	A rising edge on CCMD	A rising edge on DCMD
V_{SS}	V_{CC}	A falling edge on CCMD	A rising edge on DCMD

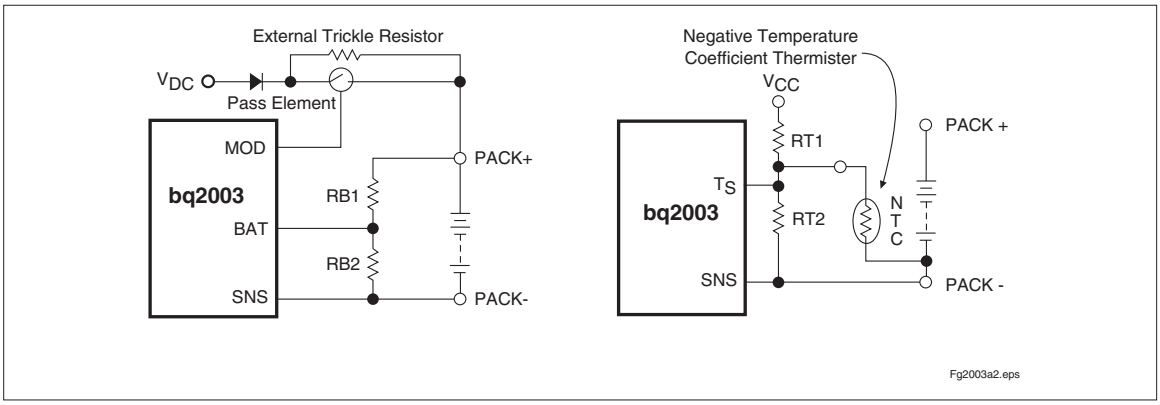


Figure 1. Voltage and Temperature Monitoring and Trickle Resistor

Discharge-Before-Charge

The DCMD input is used to command discharge-before-charge via the DIS output. Once activated, DIS becomes active (high) until V_{CELL} falls below $V_{EDV,}$ at which time DIS goes low and a new fast charge cycle begins. See Table 1 for the conditions that initiate discharge-before-charge. Discharge-before-charge is qualified by the same voltage and temperature conditions that qualify a new charge cycle start (see below). If a discharge is initiated but the pack voltage or temperature is out of range, the chip enters the charge pending mode and trickle charges the battery until the voltage and temperature qualification conditions are met, and then starts to discharge.

Starting A Charge Cycle

The stimulus required to start a new charge cycle is determined by the configuration of the CCMD and DCMD inputs. If CCMD and DCMD are both pulled up or pulled down, then a new charge cycle is started by (see Figure 2):

1. V_{CC} rising above 4.5V
2. V_{CELL} falling through the maximum cell voltage, V_{MCV}. V_{MCV} is the voltage presented at the MCV input pin, and is configured by the user with a resistor divider between V_{CC} and ground. The allowed range is 0.2 to 0.4 * V_{CC}.
3. A rising edge on CCMD if it is pulled down, or a falling edge on CCMD if it is pulled up.

Starting a new charge cycle may be limited to a push-button or logical pulse input only by pulling one member of the DCMD and CCMD pair up while pulling the other input down. In this configuration a new charge cycle will be started only by a falling edge on CCMD if it is pulled up, and by a falling edge on CCMD if it is pulled down. See Table 1.

If the battery is within the configured temperature and voltage limits, the IC begins fast charge. The valid battery voltage range is $V_{EDV} < V_{BAT} < V_{MCV}$ where:

$$V_{EDV} = 0.2 * V_{CC} \pm 30mV$$

The valid temperature range is $V_{HTF} < V_{TEMP} < V_{LTF}$, where:

$$V_{LTF} = 0.4 * V_{CC} \pm 30mV$$

$$V_{HTF} = [(1/8 * V_{LTF}) + (7/8 * V_{TCO})] \pm 30mV$$

V_{TCO} is the voltage presented at the TCO input pin, and is configured by the user with a resistor divider between V_{CC} and ground. The allowed range is 0.2 to 0.4 * V_{CC}.

If the temperature of the battery is out of range, or the voltage is too low, the chip enters the charge pending state and waits for both conditions to fall within their allowed limits. There is no time limit on the charge pending state; the charger remains in this state as long as the voltage or temperature conditons are outside of

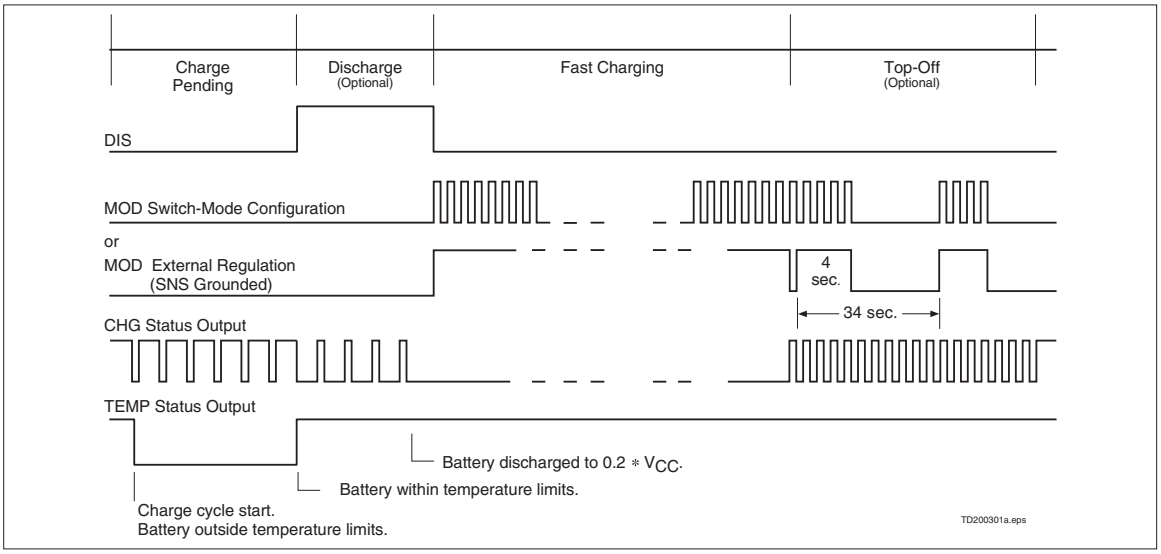


Figure 2. Charge Cycle Phases

Table 2. Fast-Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast-Charge Rate	TM1	TM2	Typical Fast Charge and Top-Off Time Limits	Typical -ΔV/MCV Hold-Off Time (seconds)	Top-Off Rate
C/4	Low	Low	360	137	Disabled
C/2	Float	Low	180	820	Disabled
1C	High	Low	90	410	Disabled
2C	Low	Float	45	200	Disabled
4C	Float	Float	23	100	Disabled
C/2	High	Float	180	820	C/16
1C	Low	High	90	410	C/8
2C	Float	High	45	200	C/4
4C	High	High	23	100	C/2

Note: Typical conditions = 25°C, V_{CC} = 5.0V.

the allowed limits. If the voltage is too high, the chip goes to the battery absent state and waits until a new charge cycle is started.

Fast charge continues until termination by one or more of the five possible termination conditions:

- Delta temperature/delta time (ΔT/Δt)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

-ΔV Termination

If the DVEN input is high, the bq2003 samples the voltage at the BAT pin once every 34s. If V_{CELL} is lower than any previously measured value by 12mV ±4mV, fast charge is terminated. The -ΔV test is valid in the range $V_{MCV} - (0.2 * V_{CC}) < V_{CELL} < V_{MCV}$.

Voltage Sampling

Each sample is an average of 16 voltage measurements taken 57µs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off period, -ΔV termination is disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. ΔT/Δt, maximum voltage and maximum temperature terminations are not affected by the hold-off period.

ΔT/Δt Termination

The bq2003 samples at the voltage at the TS pin every 34s, and compares it to the value measured two samples earlier. If V_{TEMP} has fallen 16mV ±4mV or more, fast charge is terminated. The ΔT/Δt termination test is valid only when $V_{TCO} < V_{TEMP} < V_{LTF}$.

Temperature Sampling

Each sample is an average of 16 voltage measurements taken 57µs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Maximum Voltage, Temperature, and Time

Anytime V_{CELL} rises above $V_{MCV,}$ CHG goes high (the LED goes off) immediately. If the bq2003 is not in the voltage hold-off period, fast charging ceases if V_{CELL} remains above MCV for a minimum of t_{MCV}. If V_{CELL} then falls back below V_{MCV} before $1.5t_{MCV}$ ±50ms, the chip transitions to the Charge Complete state (maximum voltage termination). If V_{CELL} remains above V_{MCV} beyond $1.5t_{MCV}$, the bq2003 transitions to the Battery Absent state (battery removal). See Figure 3.

If the bq2003 is in the voltage hold-off period when V_{CELL} rises above $V_{MCV,}$ the LED goes out but fast charging continues until the expiration of the hold-off period. Temperature sampling continues during the hold-off period as well. If a new battery is inserted before the hold-off period expires, it continues in the fast charge cycle started by its predecessor. No precharge qualification is performed, and a temperature sample

taken on the new battery is compared to ones taken before the original battery was removed and any that may have been taken while no battery was present. If the IC is configured for $\Delta T/\Delta t$ termination, this may result in a premature fast-charge termination on the newly inserted battery.

Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold V_{TCO}. Charge is also terminated if V_{TEMP} rises above the minimum temperature fault threshold, V_{LTF}, after fast charge begins.

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/4, C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for the C/2 through 4C rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time selected by the TM_1 and TM_2 input pins. (See Table 2.) During top-off, the MOD pin is enabled at a duty cycle of 4s active for every 30s inactive. This modulation results in an average rate 1/8th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

External Trickle Resistor

Maintenance charging is provided by the use of an external trickle resistor between the high side of the battery pack and V_{DC}, the input charging supply voltage. (See Figure 1.) This resistor is sized to meet two criteria.

- With the battery removed, the resistor must pull the voltage at the BAT input above MCV for battery insertion and removal detection.
- With the battery at its fully charged voltage, the trickle current should be approximately equal to the self-discharge rate of the battery.

Charge Status Indication

Charge status is indicated by the CHG output. The state of the CHG output in the various charge cycle phases is shown in Figure 3 and illustrated in Figure 1.

Temperature status is indicated by the TEMP output. TEMP is in the high state whenever V_{TEMP} is within the temperature window defined by the V_{LTF} and V_{HTF} temperature limits, and is low when the battery temperature is outside these limits.

In all cases, if V_{CELL} exceeds the voltage at the MCV pin, both CHG and TEMP outputs are held high regardless of other conditions. CHG and TEMP may both be used to directly drive an LED.

Charge Current Control

The bq2003 controls charge current through the MOD output pin. The current control circuitry is designed to support implementation of a constant-current switching regulator or to gate an externally regulated current source.

When used in switch-mode configuration, the nominal regulated current is:

$$I_{REG} = 0.235V/R_{SNS}$$

Charge current is monitored at the SNS input by the voltage drop across a sense resistor, R_{SNS}, between the low side of the battery pack and ground. R_{SNS} is sized to provide the desired fast-charge current.

If the voltage at the SNS pin is less than V_{SNSLO}, the MOD output is switched high to pass charge current to the battery.

When the SNS voltage is greater than V_{SNSHI}, the MOD output is switched low—shutting off charging current to the battery.

$$V_{SNSLO} = 0.044 * V_{CC} \pm 25mV$$

$$V_{SNSHI} = 0.05 * V_{CC} \pm 25mV$$

When used to gate an externally regulated current source, the SNS pin is connected to V_{SS}, and no sense resisitor is required.

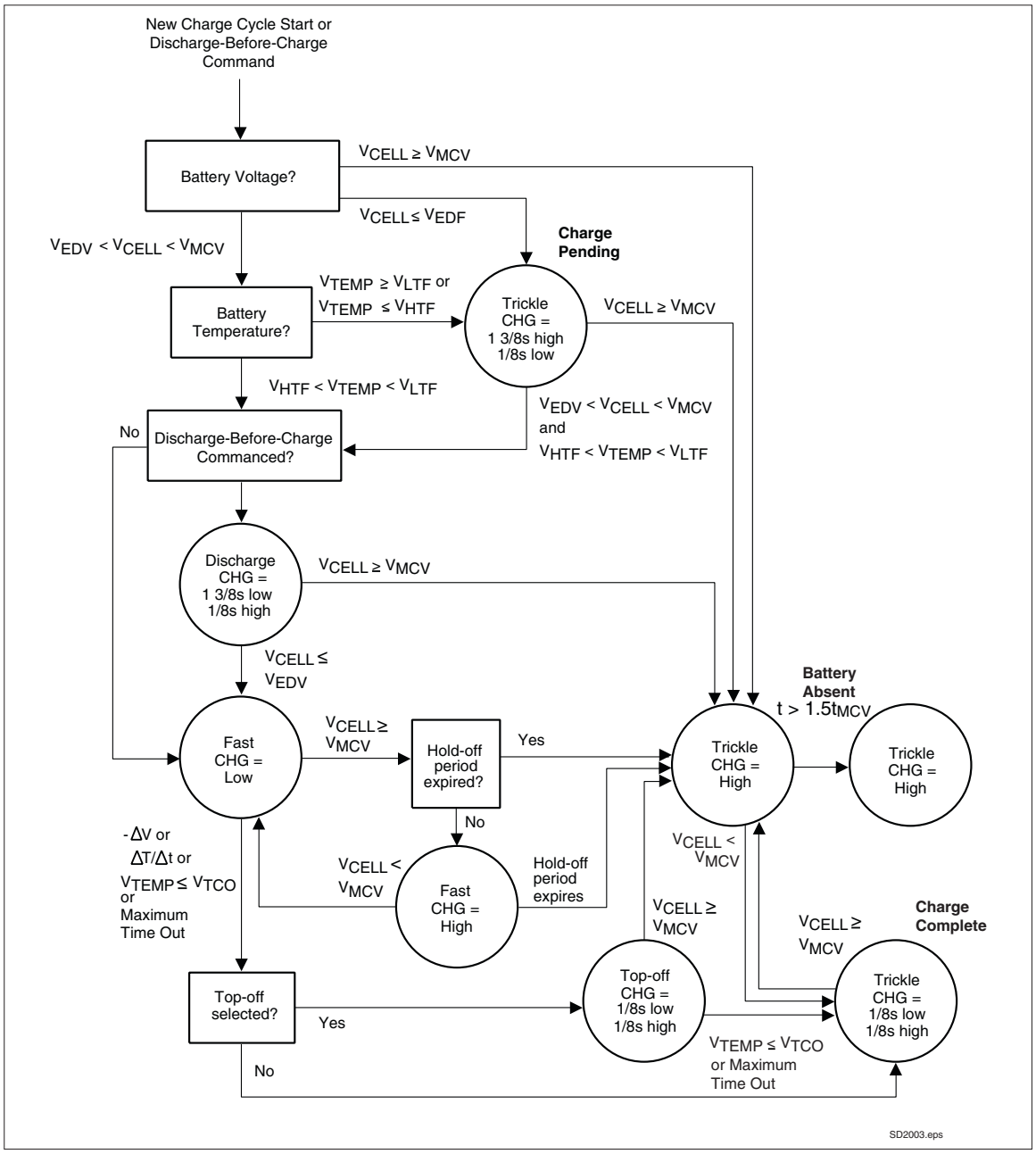


Figure 3. State Diagram

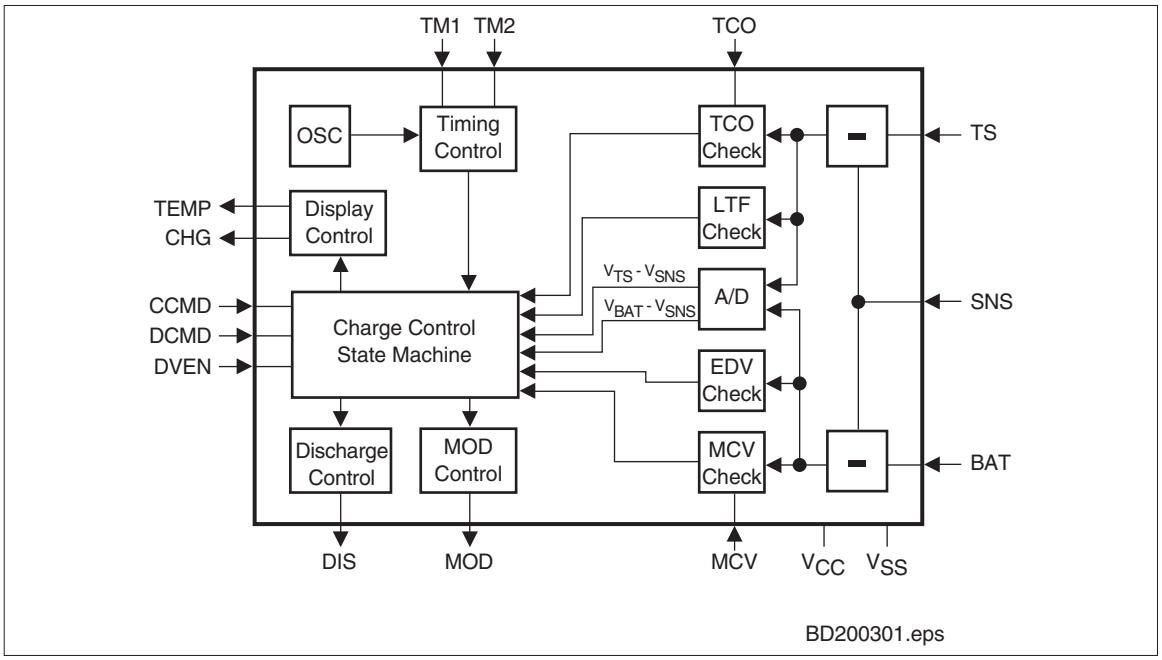


Figure 4. Block Diagram

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at SNS resulting in MOD = Low	$0.05 * V_{CC}$	±0.025	V	Tolerance is common mode deviation.
V_{SNSLO}	Low threshold at SNS resulting in MOD = High	$0.044 * V_{CC}$	±0.025	V	Tolerance is common mode deviation.
V_{LTF}	Low-temperature fault	$0.4 * V_{CC}$	±0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits/ terminates charge
V_{HTF}	High-temperature fault	$(1/8 * V_{LTF}) + (7/8 * V_{TCO})$	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits fast charge
V_{EDV}	End-of-discharge voltage	$0.2 * V_{CC}$	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits fast charge
V_{THERM}	TS input change for $\Delta T/\Delta t$ detection	-16	±4	mV	V_{CC} = 5V, T_A = 25°C
$-\Delta V$	BAT input change for $-\Delta V$ detection	-12	±4	mV	V_{CC} = 5V, T_A = 25°C

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{MCV}	Maximum cell voltage	0.2 * V_{CC}	-	0.4 * V_{CC}	V	
V_{TCO}	Temperature cutoff	0.2 * V_{CC}	-	0.4 * V_{CC}	V	
V_{IH}	Logic input high	V_{CC} - 1.0	-	-	V	CCMD, DCMD, DVEN
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2
V_{IL}	Logic input low	-	-	1.0	V	CCMD, DCMD, DVEN
	Logic input low	-	-	0.3	V	TM_1, TM_2
V_{OH}	Logic output high	V_{CC} - 0.5	-	-	V	DIS, TEMP, CHG, MOD, $I_{OH} \leq$ -5mA
V_{OL}	Logic output low	-	-	0.5	V	DIS, TEMP, CHG, MOD, $I_{OL} \leq$ 5mA
I_{CC}	Supply current	-	0.75	2.2	mA	Outputs unloaded
I_{OH}	DIS, TEMP, MOD, CHG source	-5.0	-	-	mA	@V_{OH} = V_{CC} - 0.5V
I_{OL}	DIS, TEMP, MOD, CHG sink	5.0	-	-	mA	@V_{OL} = V_{SS} + 0.5V
I_{IL}	Input leakage	-	-	±1	µA	CCMD, DCMD, DVEN, V = V_{SS} to V_{CC}
	Logic input low source	-	-	70	µA	TM_1, TM_2, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70	-	-	µA	TM_1, TM_2, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	TM_1, TM_2 tri-state open detection	-2.0	-	2.0	µA	TM_1, TM_2 may be left disconnected (floating) for Z logic input state

Note: All voltages relative to V_{SS} except as noted.

Impedance

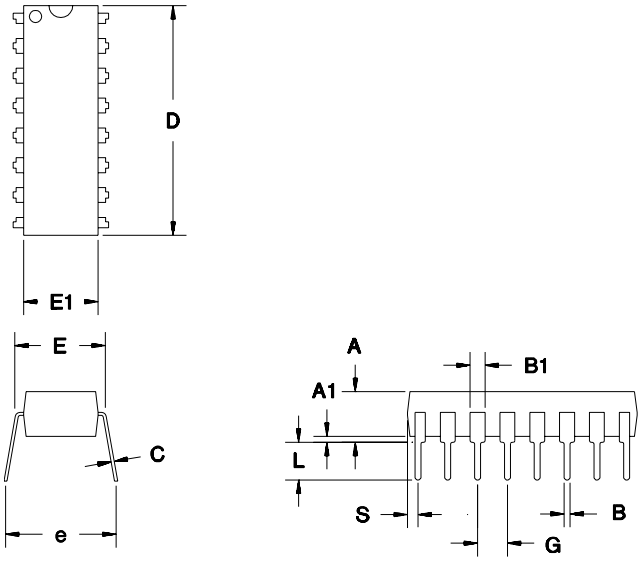
Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{MCV}	MCV input impedance	50	-	-	MΩ
R_{TCO}	TCO input impedance	50	-	-	MΩ
R_{SNS}	SNS input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ

Timing (TA = 0 to +70°C; VCC ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for CCMD, DCMD pulse commands	1	-	-	µs	Pulse start for charge or discharge-before-charge
d_{FCV}	Time base variation	-16	-	16	%	V_{CC} = 4.5V to 5.5V
f_{REG}	MOD output regulation frequency	-	-	300	kHz	
t_{MCV}	Maximum voltage termination time limit	200	250	300	ms	Time limit to distinguish battery removed from charge complete

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

PN: 16-Pin DIP Narrow

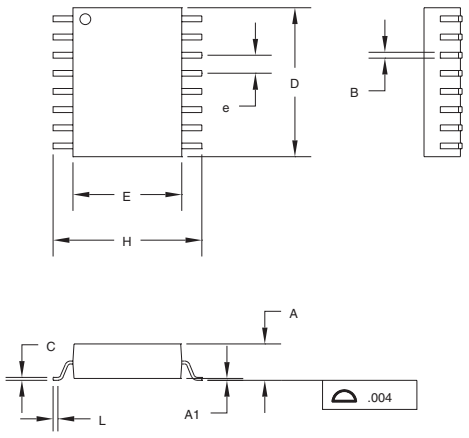


16-Pin PN (DIP Narrow)

Dimension	Minimum	Maximum
A	0.160	0.180
A1	0.015	0.040
B	0.015	0.022
B1	0.055	0.065
C	0.008	0.013
D	0.740	0.770
E	0.300	0.325
E1	0.230	0.280
e	0.300	0.370
G	0.090	0.110
L	0.115	0.150
S	0.020	0.040

All dimensions are in inches.

S: 16-Pin SOIC



16-Pin S (SOIC)

Dimension	Minimum	Maximum
A	0.095	0.105
A1	0.004	0.012
B	0.013	0.020
C	0.008	0.013
D	0.400	0.415
E	0.290	0.305
e	0.045	0.055
H	0.395	0.415
L	0.020	0.040

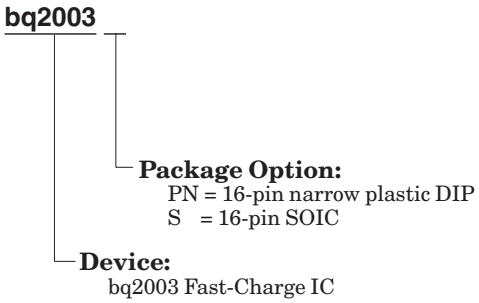
All dimensions are in inches.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
5	2	Changed block diagram	Changed diagram.
5	8	Added top-off values to Table 2.	Added values.
6	All	Revised and expanded format of this data sheet	Clarification
7	9	T_{OPR}	Deleted industrial temperature range.
8	3	Corrected Table 1	Correction
8	5, 7	Corrected and expanded the explanation for maximum voltage conditions	Clarification

Notes: Changes 1–4: Please refer to the *1997 Data Book*.
Change 5 = Sept. 1996 F changes from Oct. 1993 E.
Change 6 = Oct. 1997 G changes from Sept. 1996 F.
Change 7 = June 1999 H changes from Oct. 1997 G.
Change 8 = Oct. 1999 I changes from June 1999 H.

Ordering Information



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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ2003PN	Last Time Buy	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	2003PN
BQ2003PN-N	Last Time Buy	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	2003PN-N
BQ2003PN-N.B	Last Time Buy	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	2003PN-N
BQ2003PN-NG4	Last Time Buy	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	2003PN-N
BQ2003PN-NG4.B	Last Time Buy	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	2003PN-N
BQ2003PN.B	Last Time Buy	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	2003PN
BQ2003S	Last Time Buy	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2003S
BQ2003S-N	Last Time Buy	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2003S-N
BQ2003S-N.B	Last Time Buy	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2003S-N
BQ2003S-NTR	Last Time Buy	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2003S-N
BQ2003S-NTR.B	Last Time Buy	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2003S-N
BQ2003S-NTRG4	Last Time Buy	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2003S-N
BQ2003S-NTRG4.B	Last Time Buy	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2003S-N
BQ2003S.B	Last Time Buy	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2003S
BQ2003SG4	Last Time Buy	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2003S
BQ2003STR	Last Time Buy	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2003S

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ2003STR.B	Last Time Buy	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2003S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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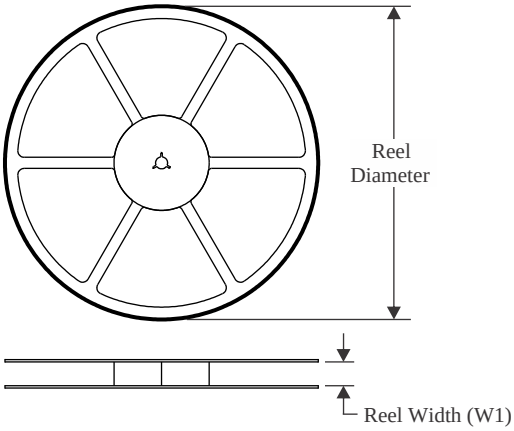
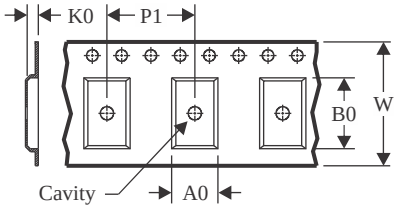
TAPE AND REEL INFORMATION

REEL DIMENSIONS

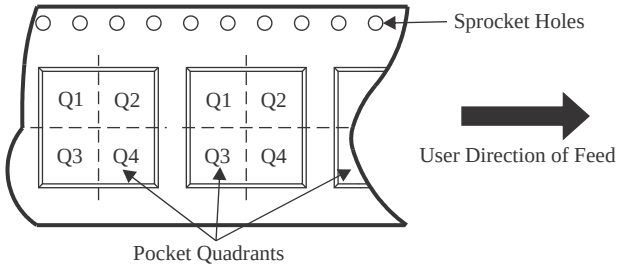


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

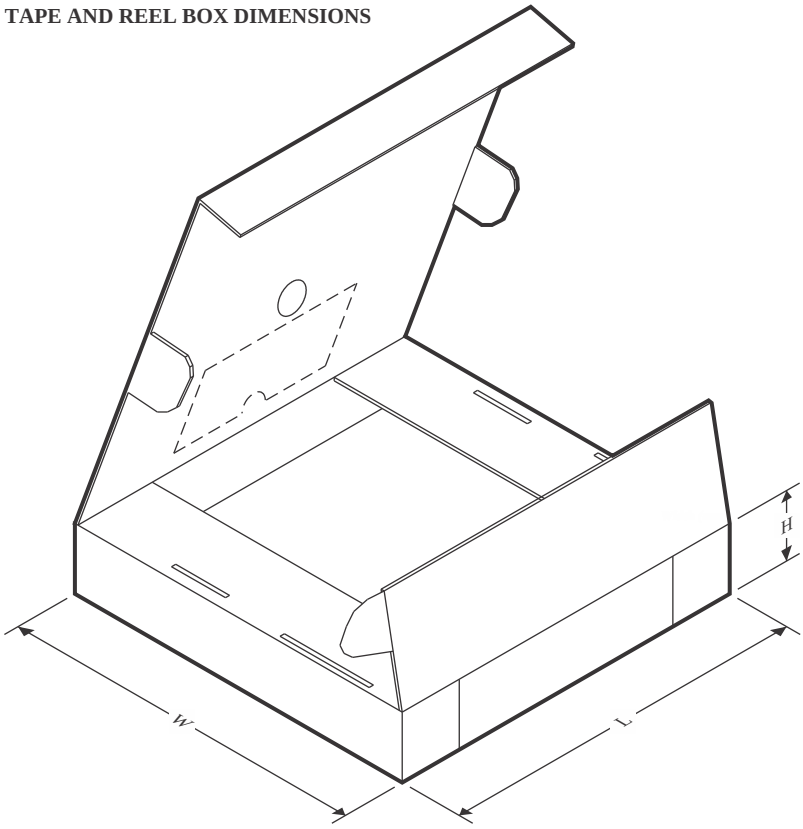
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2003S-NTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
BQ2003S-NTRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
BQ2003STR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

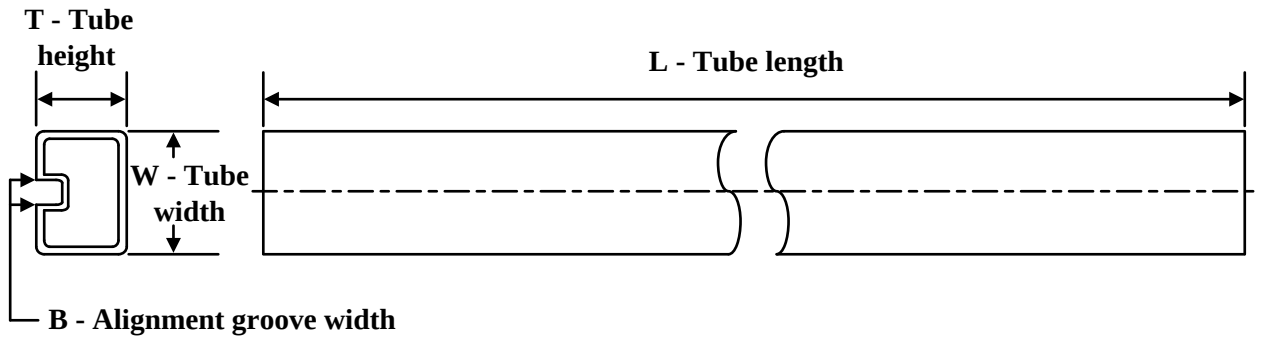
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2003S-NTR	SOIC	DW	16	2000	350.0	350.0	43.0
BQ2003S-NTRG4	SOIC	DW	16	2000	350.0	350.0	43.0
BQ2003STR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ2003PN	N	PDIP	16	25	506	13.97	11230	4.32
BQ2003PN-N	N	PDIP	16	25	506	13.97	11230	4.32
BQ2003PN-N.B	N	PDIP	16	25	506	13.97	11230	4.32
BQ2003PN-NG4	N	PDIP	16	25	506	13.97	11230	4.32
BQ2003PN-NG4.B	N	PDIP	16	25	506	13.97	11230	4.32
BQ2003PN.B	N	PDIP	16	25	506	13.97	11230	4.32
BQ2003S	DW	SOIC	16	40	506.98	12.7	4826	6.6
BQ2003S-N	DW	SOIC	16	40	506.98	12.7	4826	6.6
BQ2003S-N.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
BQ2003S.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
BQ2003SG4	DW	SOIC	16	40	506.98	12.7	4826	6.6

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