AWR2943/AWR2944 Single-Chip 76 to 81GHz FMCW Radar Sensor

1 Features

- FMCW transceiver
  - Integrated PLL, transmitter, receiver, baseband and ADC
  - 76 to 81GHz coverage with over 4GHz continuous bandwidth
  - 4 receive and 3 – 4 transmit channels (AWR2943 with 3 channels and AWR2944 with 4 channels) for PCB interface to antennas
  - Per transmit phase shifter
  - Ultra-accurate chirp engine based on fractional-N PLL
  - TX power
    - 13.5dBm
  - RX noise figure
    - 12dBm
  - Phase noise at 1MHz
    - -96dBc/Hz (76 to 77GHz)
    - -95dBc/Hz (76 to 81GHz)
- Built-in calibration and self-test
  - Built in firmware (ROM)
  - Self-calibrating system across process and temperature
- Processing elements
  - Arm® Cortex-R5F® core (supports lock step operation) @300MHz
  - TI digital signal processor C66x @360MHz (AWR2944/AWR2943)
  - TI radar hardware accelerator (HWA2.1) for operations like FFT, log magnitude, and memory compression.
  - Multiple EDMA instances for data movement
- Host interface
  - 2x CAN-FD
  - 10/100Mbps RGMII/RMII/MII Ethernet (AWR2944/AWR2943)
- Supports a serial flash memory interface (loading user application from QSPI flash memory)
- Other interfaces available to user application
  - Up to 9 ADC channels
  - 2 SPIs
  - 4 UARTs
  - I^2C
  - GPIOs
  - 3 EPWMs
  - 4-lane Aurora LVDS interface for raw ADC data and debug instrumentation (AWR2944/AWR2943)
  - CSI2 Rx interface to enable playback of the captured data (AWR2944/AWR2943)
- On-Chip RAM
  - 3 to 4MBytes (AWR2944LC with 3MB, AWR2943 with 3.5MB, and AWR2944 with 4MB)
  - Memory space split between DSP, MCU, and shared L3
- Device security (*on select part numbers*)
  - Programmable embedded hardware security module (HSM)
  - Secure authenticated and encrypted boot support
  - Customer programmable root keys, symmetric keys (256 bit), asymmetric keys (up to RSA-4K or ECC-512) with key revocation capability
  - Cryptographic hardware accelerators: PKA with ECC, AES (up to 256 bit), SHA (up to 512 bit), TRNG/DRBG
- Functional safety compliant targeted
  - Developed for functional safety applications
  - Documentation will be available to aid ISO 26262 functional safety system design
  - Hardware integrity up to ASIL B targeted
- AEC-Q100 qualified
- Advanced features
  - Embedded self-monitoring with no external processor involvement
  - Embedded interference detection capability
- Power management
  - On-die LDO network for enhanced PSRR
  - LVCMOS IO supports dual voltage 3.3V and 1.8V
- Clock source
  - 40MHz crystal with internal oscillator
  - Supports external oscillator at 40MHz
  - Supports externally driven clock (square or sine wave) at 40MHz
- Effective Power Management
  - Recommended LP87745-Q1 Power Management ICs (PMIC)
    - Companion PMIC specially designed to meet device power supply requirements
    - Flexible mapping and factory programmed configurations to support different use cases
- Cost-reduced hardware design
  - 0.65mm pitch, 12mm × 12mm flip chip BGA package for easy assembly and low-cost PCB design
  - Small solution size
- Supports automotive temperature operating range
  - Operating junction temperature range: –40°C to 140°C

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

2 Applications

- Lane change assist
- Blind spot detection
- Automatic emergency braking
- Adaptive cruise control
- Cross traffic alert

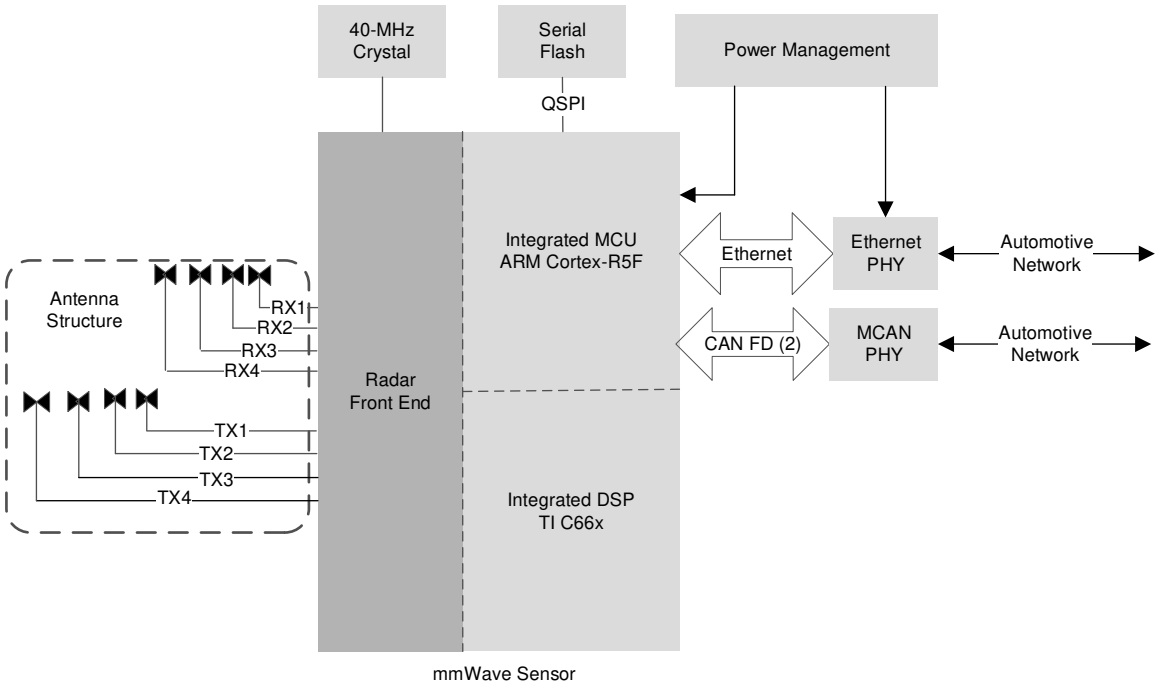

Figure 2-1. Autonomous Radar Sensor For Automotive Applications

3 Description

The AWR294x is a single-chip mmWave sensor composed of a FMCW transceiver, capable of operation in the 76 to 81GHz band, radar data processing elements, and peripherals for in-vehicle networking. The AWR294x is built with TI's low-power 45nm RFCMOS process and enables unprecedented levels of integration in a small form factor and minimal BOM. The AWR294x is a device for low-power, self-monitored, ultra-accurate radar systems in the automotive space.

TI's low-power 45nm RFCMOS process enables a monolithic implementation of a 3-4 TX, 4 RX system with integrated PLL, VCO, mixer, and baseband ADC. Integrated in the DSP subsystem (DSS), is TI's high-performance C66x DSP for radar signal processing. The device includes a Radio Processor Subsystem (RSS), which is responsible for radar front-end configuration, control, and calibration. Within the Main Subsystem (MSS), the device implements a user-programmable Arm Cortex-R5F processor allowing for custom control and automotive interface applications. The hardware accelerator block (HWA 2.1) supplements the DSS and MSS by offloading common radar processing such as FFT, constant false alarm rate (CFAR), scaling, and compression. This saves MIPS on the DSS and MSS, opening up resources for custom applications and higher-level algorithms.

A Hardware Security Module (HSM) is also provisioned in the device (available for only secure part variants). The HSM consists of a programmable Arm Cortex-M4 core and the necessary infrastructure to provide a secure zone of operation within the device.

Simple programming model changes can enable a wide variety of sensor implementation (Short, Mid, Long) with the possibility of dynamic reconfiguration for implementing a multimode sensor.

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Additionally, the AWR294x is provided as a complete platform solution including TI hardware and software reference designs, software drivers, sample configurations, API guides, and user documentation.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)	Device Variant
AWR2943ABGALTQ1	ALT (FCBGA, 266)	12mm × 12 mm	AWR2943
AWR2943ABGALTRQ1	ALT (FCBGA, 266)	12mm × 12 mm	AWR2943
AWR2943ABSALTRQ1	ALT (FCBGA, 266)	12mm × 12 mm	AWR2943
AWR2944ABGALTQ1	ALT (FCBGA, 266)	12mm × 12 mm	AWR2944
AWR2944ABGALTRQ1	ALT (FCBGA, 266)	12mm × 12 mm	AWR2944
AWR2944ABSALTQ1	ALT (FCBGA, 266)	12mm × 12 mm	AWR2944
AWR2944ABSALTRQ1	ALT (FCBGA, 266)	12mm × 12 mm	AWR2944
AWR2944ALBGALTRQ1	ALT (FCBGA, 266)	12mm × 12 mm	AWR2944LC
AWR2944ALBSALTRQ1	ALT (FCBGA, 266)	12mm × 12 mm	AWR2944LC
AWR2944ALBGALTQ1	ALT (FCBGA, 266)	12mm × 12 mm	AWR2944LC

(1) For more information, see Section 12, *Mechanical, Packaging, and Orderable Information*.

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3.1 Functional Block Diagram

Figure 3-1 represents the functional block diagram for the device.

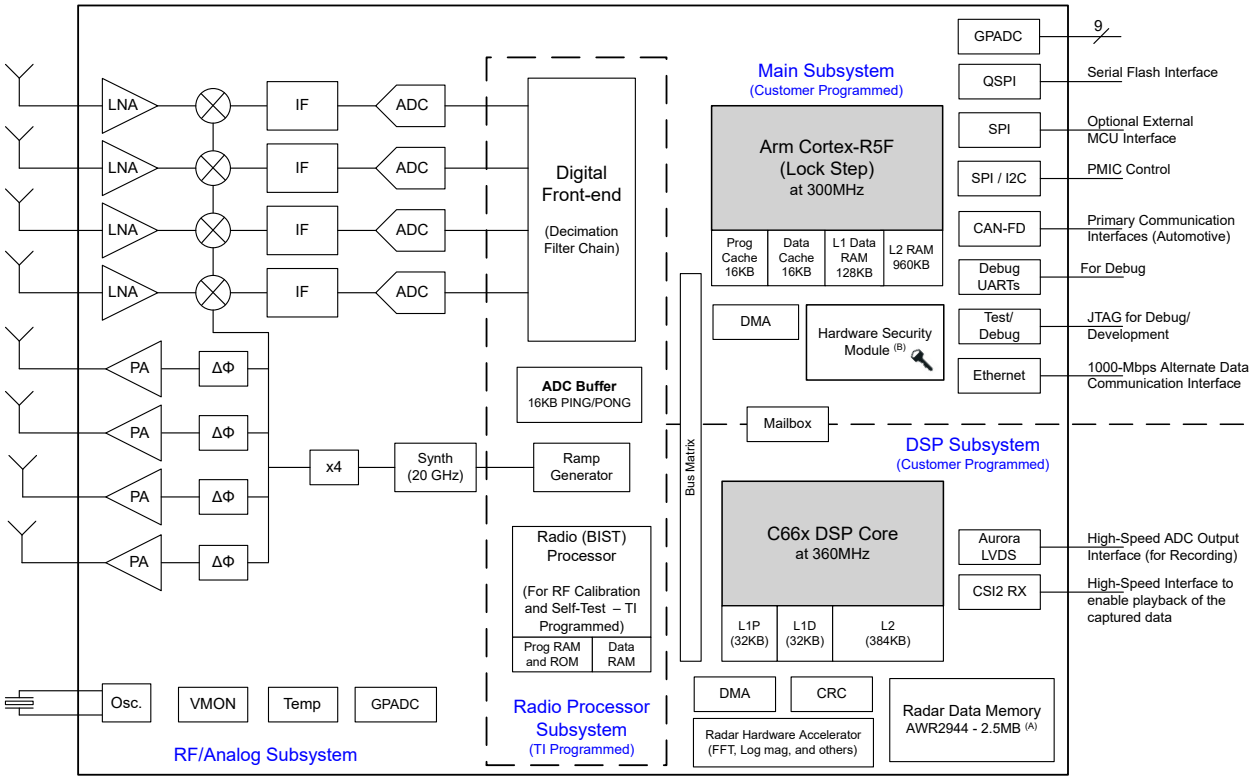

Figure 3-1. Functional Block Diagram

A. Configurable memory can be switched from Radar Data Memory to the main Cortex-R5F program and data RAM per application use case.

B. This feature is only available in select part variants as indicated by the Device Type identifier in the Section 3, Device Information table.

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4 Device Comparison

Table 4-1. Device Features Comparison

FUNCTION		AWR2943	AWR2944	AWR2944LC	AWR2243	AWR1843
Number of receivers		4	4	4	4	4
Number of transmitters		3	4	4	3(1)	3(1)
On-chip memory		3.5MB	4MB	3MB	—	2MB
Max I/F (Intermediate Frequency) (MHz)		15	15	15	20	10
Max real/complex 2x sampling rate (Msps)		37.5 (2)	37.5 (2)	37.5 (2)	45	25
Max complex 1x sampling rate (Msps)		—(2)	—(2)	—(2)	22.5	12.5
Safety and Security (3)						
Device Security(4)		Yes	Yes	Yes	—	Yes
AEC-Q100 Qualified		Yes	Yes	Yes	Yes	Yes
Processor						
MCU (RxF)		Yes(5)	Yes(5)	Yes(5)	—	Yes
DSP (C6xx)		Yes(6)	Yes(6)	—	—	Yes
Hardware accelerator		Yes(7)	Yes(7)	Yes(7)	—	Yes
Hardware Security Module (HSM) (8)		Yes	Yes	Yes	—	—
Security Accelerators (8)		Yes	Yes	Yes	—	Yes
Peripherals						
Serial Peripheral Interface (SPI) ports		2	2	2	1	2
Quad Serial Peripheral Interface (QSPI)		Yes	Yes	Yes	—	Yes
LVDS/Debug		Yes	Yes	Yes	Yes	Yes
Aurora LVDS		Yes	Yes	—	—	—
Ethernet Interface		Yes	Yes	—	—	—
Inter-Integrated Circuit (I^2C) interface		1	1	1	1	1
Controller Area Network (DCAN) interface		—	—	—	—	Yes
CAN FD		2	2	2	—	1
Trace		Yes	Yes	Yes	—	Yes
ePWM		Yes	Yes	Yes	—	Yes
DMM Interface		Yes	Yes	Yes	—	Yes
GPADC		Yes(9)	Yes(9)	Yes(9)	Yes	Yes
CSI2 TX		—	—	—	Yes	—
CSI2 RX (10)		Yes	Yes	—	—	—
Cascade (20-GHz sync)		—	—	—	Yes	—
JTAG		Yes	Yes	Yes	—	Yes
Per chirp configurable Tx phase shifter		Yes	Yes	Yes	Yes	Yes
Product status(11)	PRODUCT PREVIEW (PP), ADVANCE INFORMATION (AI), or PRODUCTION DATA (PD)	PD	PD	PD	PD	PD

(1) 3 Tx Simultaneous operation in AWR1843 and AWR2243 is supported only with 1V LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin. Please refer to the respective datasheets for more information.
(2) AWR294x supports a real only receiver.
(3) Developed for Functional Safety applications, the AWR294x device is targeted to support hardware integrity up to ASIL-B. For other devices, refer to the respective Datasheets.
(4) Device security features including Secure Boot and Customer Programmable Keys are applicable to select part number variants as indicated by the Device Type identifier in the Section 3, Device Information table.
(5) In AWR294x, Main-Subsystem Processing core is changed from Arm CR4F in AWR1843 to Arm CR5F.
(6) The DSP processing core in AWR294x is upgraded from C67x in AWR1843 to C66x.
(7) The hardware accelerator in AWR294x is upgraded to HWA2.1 with additional features as compared to AWR1843. AWR2944LC has M4 core in HWA

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(8) Only applicable for AWR294x Secure Part Variant
(9) AWR294x has a dedicated GPADC for external voltage monitoring.
(10) AWR294x support CSI2 Rx based playback functionality .
(11) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.
ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

4.1 Related Products

For information about other devices in this family of products or related products, see the following links.

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5 Pin Configurations and Functions

5.1 Pin Diagram

Figure 5-1 shows the pin locations for the 12 x12 mm FCBGA package. Figure 5-2, Figure 5-3, Figure 5-4 and Figure 5-5 show the same pins, but split into four quadrants.

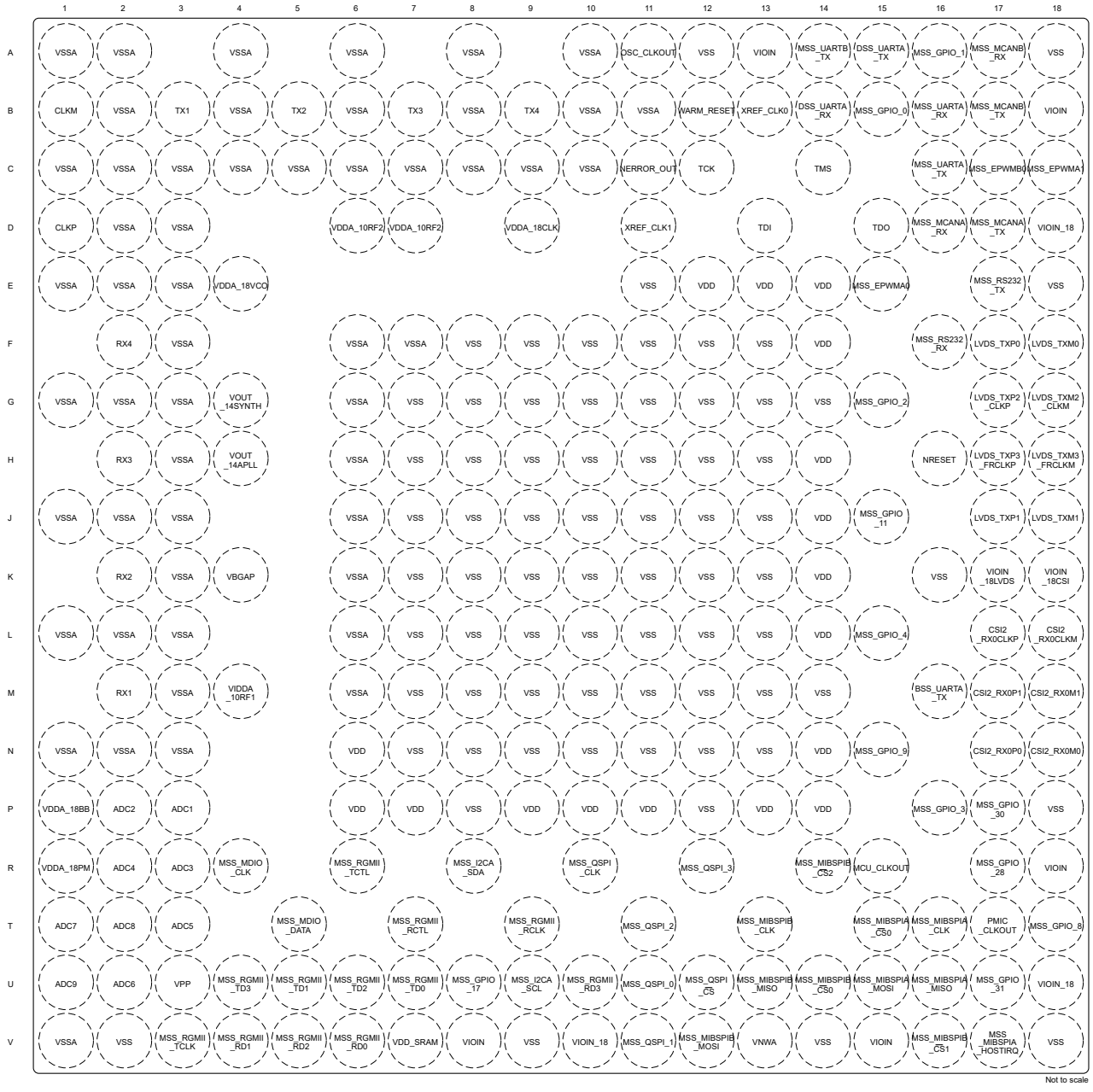

Figure 5-1. Pin Diagram

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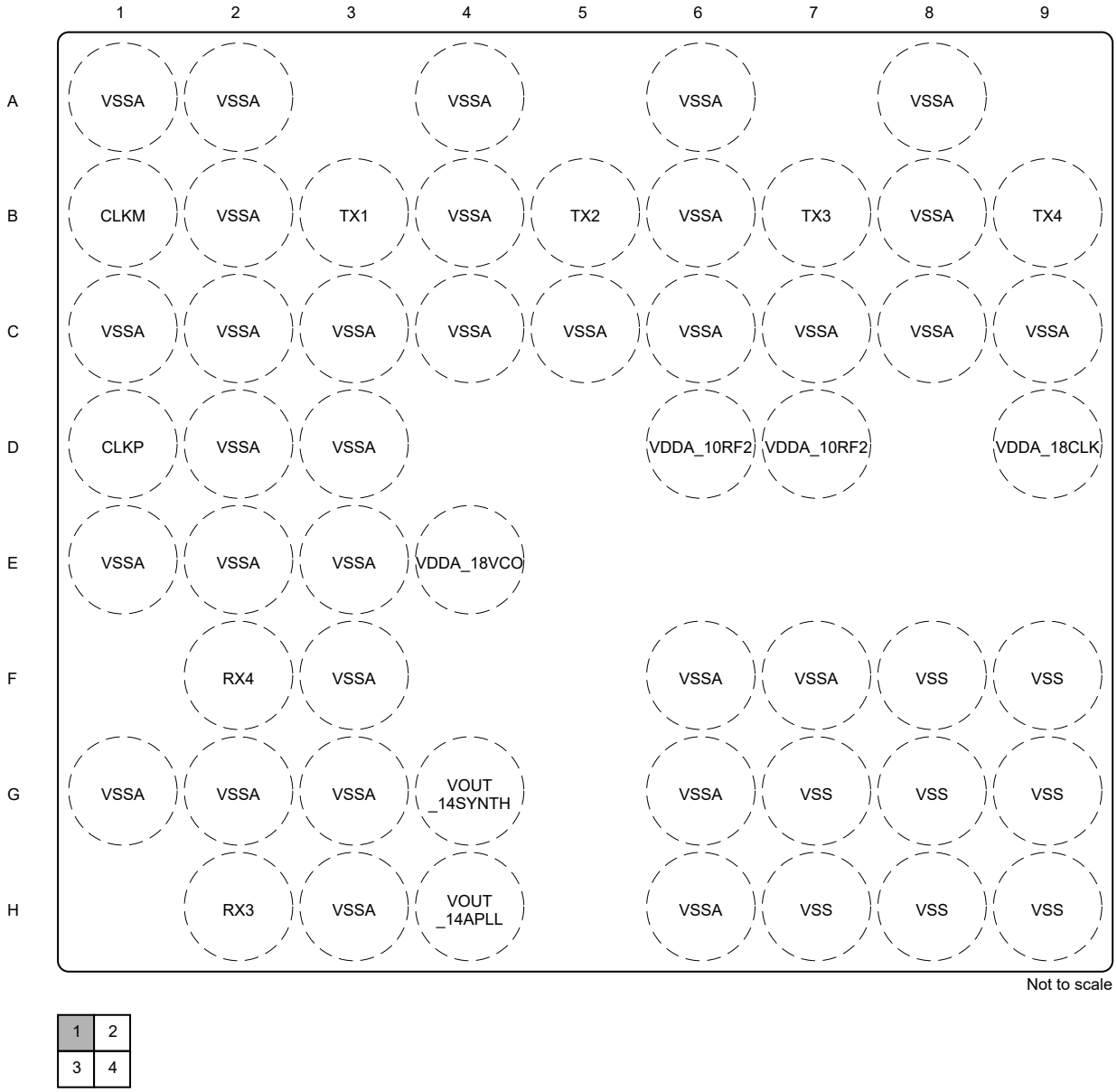

Figure 5-2. Top Left Quadrant

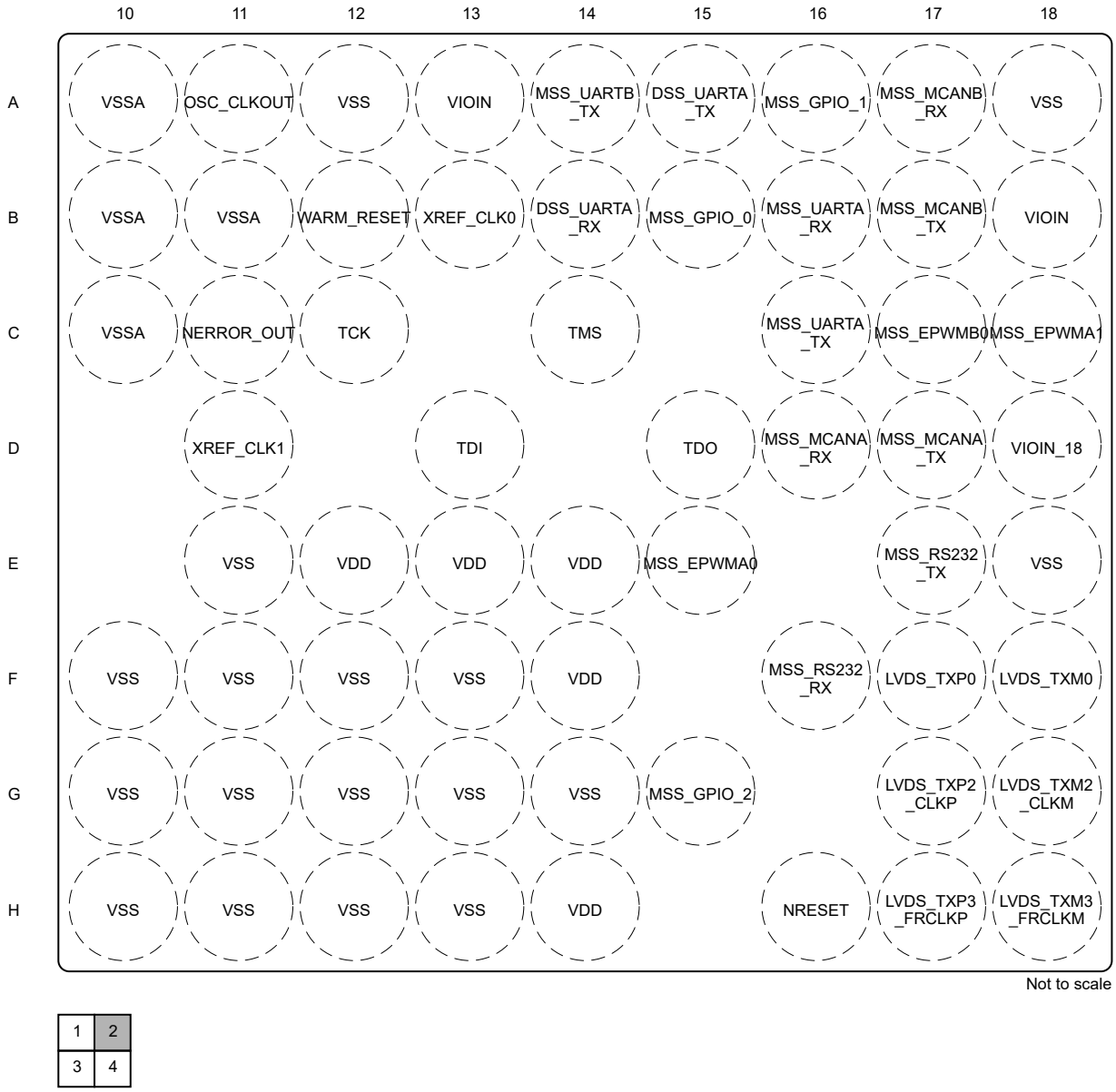

Figure 5-3. Top Right Quadrant

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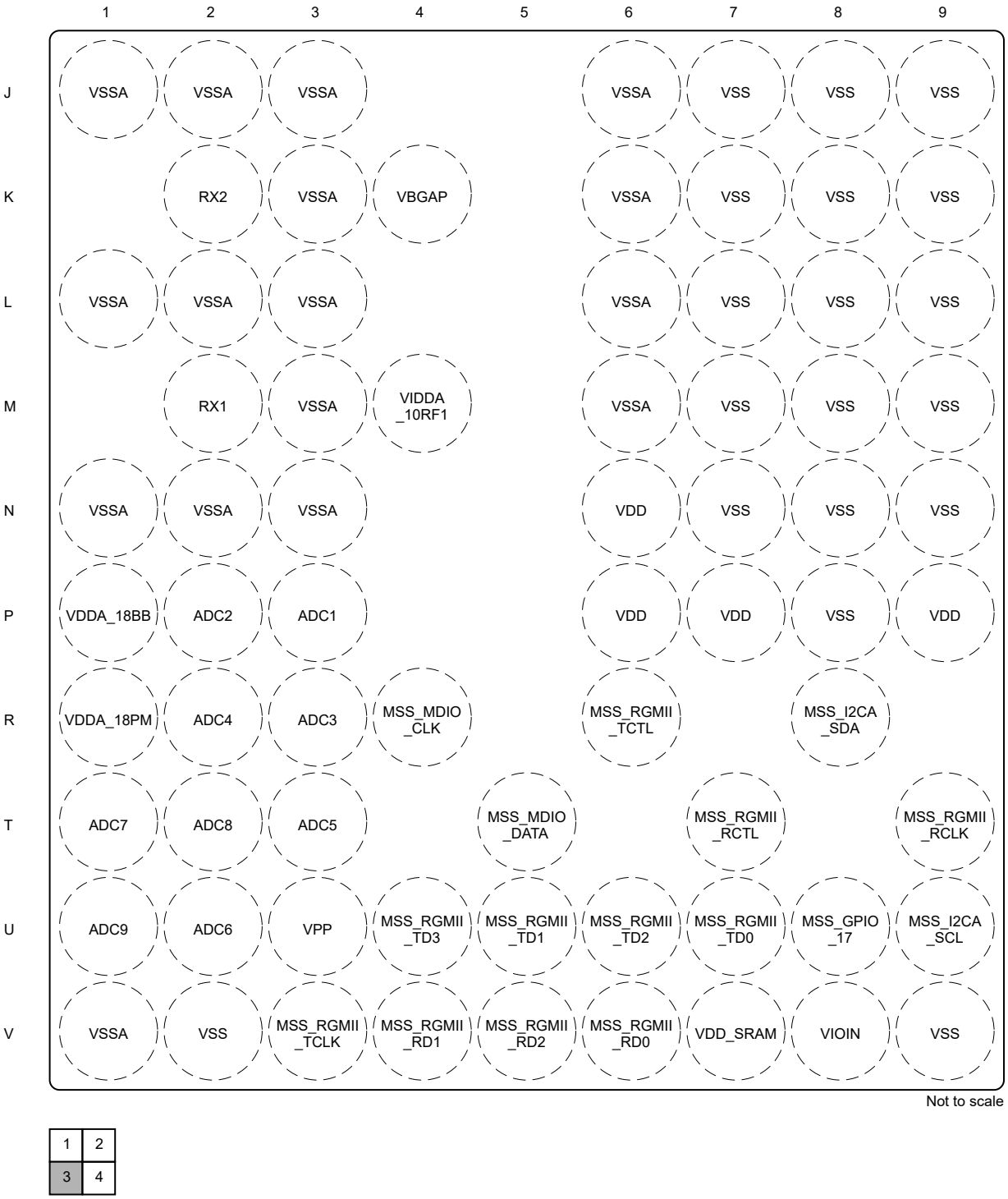

Figure 5-4. Bottom Left Quadrant



Figure 5-5. Bottom Right Quadrant

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5.2 Pin Attributes

BALL NUMBER [1]	PAD NAME [9]	BALL NAME [2]	SIGNAL NAME [3]	MODE [4],[8]	TYPE [5]	BALL RESET STATE [6]	PULL UP/DOWN TYPE [7]
V16	PAD_AA	MSS_MIBSPIB_CS1	MSS_GPIO_12	0	IO	Output Disabled	Pull Down
			MSS_MIBSPIA_HOSTIRQ	1	O		
			ADC_VALID	2	O		
			MSS_MIBSPIB_CS1	6	IO		
B15	PAD_AB	MSS_GPIO_0	MSS_GPIO_13	0	IO	Output Disabled	Pull Down
			MSS_GPIO_0	1	IO		
			PMIC_CLKOUT	2	O		
			MSS_EPWM_TZ2	3	I		
			MSS_EPWMA1	10	O		
			MSS_EPWMB0	11	O		
A16	PAD_AC	MSS_GPIO_1	MSS_GPIO_16	0	IO	Output Disabled	Pull Down
			MSS_GPIO_1	1	IO		
			SYNC_OUT	2	O		
			MSS_EPWM_TZ1	3	I		
			BSS_UARTA_TX	7	O		
			READY_INT	8	O		
			LVDS_VALID	9	O		
			DMM_MUX_IN	12	I		
			MSS_MIBSPIB_CS1	13	IO		
			MSS_MIBSPIB_CS2	14	IO		
			MSS_EPWMA_SYNCI	15	I		
V12	PAD_AH	MSS_MIBSPIB_MOSI	MSS_GPIO_21	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIB_MOSI	1	IO		
			MSS_I2CA_SDA	2	IO		
			MSS_EPWMA0	3	O		
			MSS_MCANB_RX	7	I		
U13	PAD_AI	MSS_MIBSPIB_MISO	MSS_GPIO_22	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIB_MISO	1	IO		
			MSS_I2CA_SCL	2	IO		
			MSS_EPWMB0	3	O		
			DSS_UARTA_TX	6	IO		
			MSS_MCANB_TX	7	O		

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BALL NUMBER (1)	PAD NAME (9)	BALL NAME (2)	SIGNAL NAME (3)	MODE (4),(8)	TYPE (5)	BALL RESET STATE (6)	PULL UP/DOWN TYPE (7)
T13	PAD_AJ	MSS_MIBSPIB_CLK	MSS_GPIO_5	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIB_CLK	1	IO		
			MSS_UARTA_RX	2	IO		
			MSS_EPWMC0	3	O		
			MSS_UARTB_TX	6	IO		
			BSS_UARTA_TX	7	O		
			MSS_MCANA_RX	8	I		
U14	PAD_AK	MSS_MIBSPIB_$\overline{CS}$0	MSS_GPIO_4	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIB_$\overline{CS}$0	1	IO		
			MSS_UARTA_TX	2	IO		
			MSS_UARTB_TX	6	IO		
			BSS_UARTA_TX	7	O		
			MSS_MCANA_TX	9	O		
U11	PAD_AL	MSS_QSPI_0	MSS_GPIO_8	0	IO	Output Disabled	Pull Down
			MSS_QSPI_0	1	IO		
			MSS_MIBSPIB_MISO	2	IO		
V11	PAD_AM	MSS_QSPI_1	MSS_GPIO_9	0	IO	Output Disabled	Pull Down
			MSS_QSPI_1	1	I		
			MSS_MIBSPIB_MOSI	2	IO		
			MSS_MIBSPIB_$\overline{CS}$2	8	IO		
T11	PAD_AN	MSS_QSPI_2	MSS_GPIO_10	0	IO	Output Disabled	Pull Up
			MSS_QSPI_2	1	I		
			ADC_VALID	2	O		
			MSS_MCANA_TX	8	O		
R12	PAD_AO	MSS_QSPI_3	MSS_GPIO_11	0	IO	Output Disabled	Pull Up
			MSS_QSPI_3	1	I		
			ADC_VALID	2	O		
			MSS_MCANA_RX	8	I		
R10	PAD_AP	MSS_QSPI_CLK	MSS_GPIO_7	0	IO	Output Disabled	Pull Down
			MSS_QSPI_CLK	1	IO		
			MSS_MIBSPIB_CLK	2	IO		
			DSS_UARTA_TX	6	IO		
U12	PAD_AQ	MSS_QSPI_$\overline{CS}$	MSS_GPIO_6	0	IO	Output Disabled	Pull Up
			MSS_QSPI_$\overline{CS}$	1	O		
			MSS_MIBSPIB_$\overline{CS}$0	2	IO		
B12	PAD_AS	WARM_RESET	WARM_RESET	0	IO	HiZ Input (Open drain)	
C11	PAD_AT	NERROR_OUT	NERROR_OUT	0	O	HiZ (Open drain)	

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BALL NUMBER [1]	PAD NAME [9]	BALL NAME [2]	SIGNAL NAME [3]	MODE [4],[8]	TYPE [5]	BALL RESET STATE [6]	PULL UP/DOWN TYPE [7]
C12	PAD_AU	TCK	MSS_GPIO_17	0	IO	Output Disabled	Pull Down
			TCK	1	I		
			MSS_UARTB_TX	2	IO		
			BSS_UARTA_RX	6	I		
			MSS_MCANA_TX	8	O		
C14	PAD_AV	TMS	MSS_GPIO_18	0	IO	Output Disabled	Pull Up
			TMS	1	IO		
			BSS_UARTA_TX	2	O		
			MSS_MCANA_RX	6	I		
D13	PAD_AW	TDI	MSS_GPIO_23	0	IO	Output Disabled	Pull Up
			TDI	1	I		
			MSS_UARTA_RX	2	IO		
			DSS_UARTA_RX	7	IO		
D15	PAD_AX	TDO	SOP[0]	During Power-up	I	Output Enabled	
			MSS_GPIO_24	0	IO		
			TDO	1	O		
			MSS_UARTA_TX	2	IO		
			MSS_UARTB_TX	6	IO		
			BSS_UARTA_TX	7	O		
			NDMM_EN	9	O		
R15	PAD_AY	MCU_CLKOUT	MSS_GPIO_25	0	IO	Output Disabled	Pull Down
			MCU_CLKOUT	1	O		
			TRACE_CLK	2	O		
			FRAME_START	7	O		
			READY_INT	8	O		
			LVDS_VALID	9	O		
			BSS_UARTA_RX	10	I		
			MSS_EPWMA0	12	O		
			DMM_CLK	14	I		
			OBS_CLKOUT	15	O		

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BALL NUMBER (1)	PAD NAME (9)	BALL NAME (2)	SIGNAL NAME (3)	MODE (4),(8)	TYPE (5)	BALL RESET STATE (6)	PULL UP/DOWN TYPE (7)
G15	PAD_AZ	MSS_GPIO_2	MSS_GPIO_26	0	IO	Output Disabled	Pull Down
			MSS_GPIO_2	1	IO		
			MSS_UARTB_TX	7	IO		
			MSS_GPIO_2	1	IO		
			SYNC_OUT	9	O		
			PMIC_CLKOUT	10	O		
			CHIRP_START	11	O		
			CHIRP_END	12	O		
			FRAME_START	13	O		
			MSS_EPWM_TZ0	14	I		
			LVDS_VALID	15	O		
T17	PAD_BA	PMIC_CLKOUT	SOP[2]	During Power-up	I	Output Disabled	No Pull
			MSS_GPIO_27	0	IO		
			PMIC_CLKOUT	1	O		
			OBS_CLKOUT	2	O		
			TRACE_CTL	3	O		
			CHIRP_START	6	O		
			CHIRP_END	7	O		
			FRAME_START	8	O		
			READY_INT	9	O		
			LVDS_VALID	10	O		
			MSS_EPWMA1	11	O		
			MSS_EPWMB0	12	O		
			DMM_SYNC	13	I		
R17	PAD_BB	MSS_GPIO_28	MSS_GPIO_28	0	IO	Output Disabled	Pull Down
			SYNC_IN	1	I		
			ADC_VALID	2	O		
			MSS_UARTB_RX	6	IO		
			DMM_MUX_IN	7	I		
			DSS_UARTA_RX	8	IO		
			SYNC_OUT	9	O		

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BALL NUMBER (1)	PAD NAME (9)	BALL NAME (2)	SIGNAL NAME (3)	MODE (4),(8)	TYPE (5)	BALL RESET STATE (6)	PULL UP/DOWN TYPE (7)
R14	PAD_BC	MSS_MIBSPIB_CS2	SOP[1]	During Power-up	I	Output Disabled	
			MSS_GPIO_29	0	IO		
			SYNC_OUT	1	O		
			RCOSC_CLK	2	O		
			READY_INT	6	O		
			LVDS_VALID	7	O		
			DMM_MUX_IN	9	I		
			MSS_MIBSPIB_CS1	10	IO		
			MSS_MIBSPIB_CS2	11	IO		
			MSS_EPWMB0	12	O		
			MSS_EPWMB1	13	O		
F16	PAD_BD	MSS_RS232_RX	MSS_GPIO_15	0	IO	Output Disabled	Pull Up
			MSS_RS232_RX	1	IO		
			MSS_UARTA_RX	2	IO		
			TRACE_CLK	3	O		
			BSS_UARTA_TX	6	O		
			MSS_UARTB_RX	7	IO		
			MSS_MCANA_RX	8	I		
			MSS_I2CA_SCL	9	IO		
			MSS_EPWMB0	10	O		
			MSS_EPWMB1	11	O		
			MSS_EPWMC0	12	O		
E17	PAD_BE	MSS_RS232_TX	MSS_GPIO_14	0	IO	Output Enabled	Pull Up
			MSS_RS232_TX	1	IO		
			TRACE_CTL	2	O		
			MSS_UARTA_TX	5	IO		
			MSS_UARTB_TX	6	IO		
			BSS_UARTA_TX	7	O		
			READY_INT	8	O		
			LVDS_VALID	9	O		
			MSS_MCANA_TX	10	O		
			MSS_I2CA_SDA	11	IO		
			MSS_EPWMA0	12	O		
			MSS_EPWMA1	13	O		
			NDMM_EN	14	O		
			MSS_EPWMB0	15	O		

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BALL NUMBER (1)	PAD NAME (9)	BALL NAME (2)	SIGNAL NAME (3)	MODE (4),(8)	TYPE (5)	BALL RESET STATE (6)	PULL UP/DOWN TYPE (7)
U17	PAD_BF	MSS_GPIO_31	TRACE_DATA_0	0	O	Output Disabled	Pull Down
			MSS_GPIO_31	1	IO		
			DMM0	2	I		
			MSS_UARTA_TX	4	IO		
			MSS_I2CA_SDA	10	IO		
P17	PAD_BG	MSS_GPIO_30	TRACE_DATA_1	0	O	Output Disabled	Pull Down
			MSS_GPIO_30	1	IO		
			DMM1	2	I		
			MSS_EPWMC_SYNCI	3	I		
			MSS_UARTA_RX	4	IO		
			MSS_GPIO_0	6	IO		
			MSS_I2CA_SCL	10	IO		
T18	PAD_BH	MSS_GPIO_8	TRACE_DATA_2	0	O	Output Disabled	Pull Down
			MSS_GPIO_29	1	IO		
			DMM2	2	I		
			MSS_EPWMB_SYNCI	3	I		
			MSS_GPIO_1	6	IO		
			MSS_GPIO_8	7	IO		
N15	PAD_BI	MSS_GPIO_9	TRACE_DATA_3	0	O	Output Disabled	Pull Down
			MSS_GPIO_28	1	IO		
			DMM3	2	I		
			MSS_EPWMC_SYNCO	4	O		
			MSS_GPIO_2	6	IO		
			MSS_GPIO_9	7	IO		
P16	PAD_BJ	MSS_GPIO_3	TRACE_DATA_4	0	O	Output Disabled	Pull Down
			MSS_GPIO_3	1	IO		
			DMM4	2	I		
			MSS_EPWMB_SYNCO	4	O		
			MSS_GPIO_27	6	IO		
L15	PAD_BK	MSS_GPIO_4	TRACE_DATA_5	0	O	Output Disabled	Pull Down
			MSS_GPIO_4	1	IO		
			DMM5	2	I		
			MSS_EPWM_TZ2	4	I		
			MSS_UARTB_TX	5	IO		
			MSS_GPIO_26	6	IO		

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BALL NUMBER (1)	PAD NAME (9)	BALL NAME (2)	SIGNAL NAME (3)	MODE (4),(8)	TYPE (5)	BALL RESET STATE (6)	PULL UP/DOWN TYPE (7)
M16	PAD_BL	BSS_UARTA_TX	TRACE_DATA_6	0	O	Output Disabled	Pull Down
			MSS_GPIO_5	1	IO		
			DMM6	2	I		
			MSS_EPWM_TZ1	4	I		
			BSS_UARTA_TX	5	O		
			MSS_GPIO_25	6	IO		
			MSS_GPIO_10	7	IO		
J15	PAD_BM	MSS_GPIO_11	TRACE_DATA_7	0	O	Output Disabled	Pull Down
			MSS_GPIO_6	1	IO		
			DMM7	2	I		
			MSS_EPWM_TZ0	4	I		
			DSS_UARTA_TX	5	IO		
			MSS_GPIO_24	6	IO		
			MSS_GPIO_11	7	IO		
D17	PAD_BN	MSS_MCANA_TX	TRACE_DATA_8	0	O	Output Disabled	Pull Down
			MSS_GPIO_7	1	IO		
			DMM8	2	I		
			MSS_MCANA_TX	4	O		
			MSS_EPWMA_SYNCI	5	I		
			MSS_GPIO_23	6	IO		
D16	PAD_BO	MSS_MCANA_RX	TRACE_DATA_9	0	O	Output Disabled	Pull Down
			MSS_GPIO_8	1	IO		
			DMM9	2	I		
			MSS_MCANA_RX	4	I		
			MSS_EPWMA_SYNCO	5	O		
			MSS_GPIO_22	6	IO		
E15	PAD_BP	MSS_EPWMA0	TRACE_DATA_10	0	O	Output Disabled	Pull Down
			MSS_GPIO_9	1	IO		
			DMM10	2	I		
			MSS_EPWMA0	3	O		
			MSS_EPWMC0	4	O		
			MSS_GPIO_21	6	IO		
C18	PAD_BQ	MSS_EPWMA1	TRACE_DATA_11	0	O	Output Disabled	Pull Down
			MSS_GPIO_10	1	IO		
			DMM11	2	I		
			MSS_EPWMA1	3	O		
			MSS_EPWMC1	4	O		
			MSS_GPIO_20	6	IO		

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BALL NUMBER (1)	PAD NAME (9)	BALL NAME (2)	SIGNAL NAME (3)	MODE (4),(8)	TYPE (5)	BALL RESET STATE (6)	PULL UP/DOWN TYPE (7)
B17	PAD_BR	MSS_MCANB_TX	TRACE_DATA_12	0	O	Output Disabled	Pull Down
			MSS_GPIO_11	1	IO		
			DMM12	2	I		
			MSS_EPWMB0	3	O		
			MSS_EPWMA0	4	O		
			MSS_MCANB_TX	5	O		
			MSS_GPIO_19	6	IO		
A17	PAD_BS	MSS_MCANB_RX	TRACE_DATA_13	0	O	Output Disabled	Pull Down
			MSS_GPIO_12	1	IO		
			DMM13	2	I		
			MSS_EPWMB1	3	O		
			MSS_EPWMA1	4	O		
			MSS_MCANB_RX	5	I		
			MSS_GPIO_18	6	IO		
C17	PAD_BT	MSS_EPWMB0	TRACE_DATA_14	0	O	Output Disabled	Pull Down
			MSS_GPIO_13	1	IO		
			DMM14	2	I		
			MSS_EPWMC0	3	O		
			MSS_EPWMB0	4	O		
			MSS_GPIO_17	6	IO		
U8	PAD_BX	MSS_GPIO_17	MSS_GPIO_17	0	IO	Output Disabled	Pull Down
			MSS_MII_COL	1	I		
			MSS_RMII_REFCLK	2	IO		
			MSS_EPWMA1	6	O		
R8	PAD_BY	MSS_I2CA_SDA	MSS_GPIO_18	0	IO	Output Disabled	HiZ (Open drain)
			MSS_MII_CRS	1	I		
			MSS_RMII_CRS_DV	2	I		
			MSS_I2CA_SDA	3	IO		
			MSS_EPWMB1	6	O		
U9	PAD_BZ	MSS_I2CA_SCL	MSS_GPIO_19	0	IO	Output Disabled	HiZ (Open drain)
			MSS_MII_RXER	1	I		
			MSS_RMII_RXER	2	I		
			MSS_I2CA_SCL	3	IO		
			MSS_EPWMC1	6	O		
R6	PAD_CA	MSS_RGMII_TCTL	MSS_GPIO_20	0	IO	Output Disabled	Pull Down
			MSS_MII_TXEN	1	O		
			MSS_RMII_TXEN	2	O		
			MSS_RGMII_TCTL	3	O		
			MSS_EPWMA0	6	O		

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BALL NUMBER (1)	PAD NAME (9)	BALL NAME (2)	SIGNAL NAME (3)	MODE (4),(8)	TYPE (5)	BALL RESET STATE (6)	PULL UP/DOWN TYPE (7)
T7	PAD_CB	MSS_RGMII_RCTL	MSS_GPIO_21	0	IO	Output Disabled	
			MSS_MII_RXDV	1	I		
			MSS_RGMII_RCTL	3	I		
			MSS_RMII_CRS_DV	4	I		
			MSS_UARTB_RX	5	IO		
			MSS_EPWMB0	6	O		
U4	PAD_CC	MSS_RGMII_TD3	MSS_GPIO_22	0	IO	Output Disabled	Pull Down
			MSS_MII_TXD3	1	O		
			MSS_RGMII_TD3	3	O		
			MSS_UARTB_TX	5	IO		
			MSS_EPWMC0	6	O		
U6	PAD_CD	MSS_RGMII_TD2	MSS_GPIO_23	0	IO	Output Disabled	Pull Down
			MSS_MII_TXD2	1	O		
			MSS_RGMII_TD2	3	O		
U5	PAD_CE	MSS_RGMII_TD1	MSS_GPIO_24	0	IO	Output Disabled	Pull Down
			MSS_MII_TXD1	1	O		
			MSS_RMII_TXD1	2	O		
			MSS_RGMII_TD1	3	O		
U7	PAD_CF	MSS_RGMII_TD0	MSS_GPIO_25	0	IO	Output Disabled	Pull Down
			MSS_MII_TXD0	1	O		
			MSS_RMII_TXD0	2	O		
			MSS_RGMII_TD0	3	O		
V3	PAD_CG	MSS_RGMII_TCLK	MSS_GPIO_26	0	IO	Output Disabled	Pull Down
			MSS_MII_TXCLK	1	I		
			MSS_RGMII_TCLK	3	O		
T9	PAD_CH	MSS_RGMII_RCLK	MSS_GPIO_27	0	IO	Output Disabled	Pull Down
			MSS_MII_RXCLK	1	I		
			MSS_RGMII_RCLK	3	I		
			MSS_RMII_REFCLK	4	IO		
U10	PAD_CI	MSS_RGMII_RD3	MSS_GPIO_28	0	IO	Output Disabled	
			MSS_MII_RXD3	1	I		
			MSS_RGMII_RD3	3	I		
V5	PAD_CJ	MSS_RGMII_RD2	MSS_GPIO_29	0	IO	Output Disabled	
			MSS_MII_RXD2	1	I		
			MSS_RGMII_RD2	3	I		
V4	PAD_CK	MSS_RGMII_RD1	MSS_GPIO_30	0	IO	Output Disabled	
			MSS_MII_RXD1	1	I		
			MSS_RMII_RXD1	2	I		
			MSS_RGMII_RD1	3	I		

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BALL NUMBER (1)	PAD NAME (9)	BALL NAME (2)	SIGNAL NAME (3)	MODE (4),(8)	TYPE (5)	BALL RESET STATE (6)	PULL UP/DOWN TYPE (7)
V6	PAD_CL	MSS_RGMII_RD0	MSS_GPIO_31	0	IO	Output Disabled	
			MSS_MII_RXD0	1	I		
			MSS_RMII_RXD0	2	I		
			MSS_RGMII_RD0	3	I		
T5	PAD_CM	MSS_MDIO_DATA	MSS_GPIO_30	0	IO	Output Disabled	Pull Up
			MSS_MDIO_DATA	1	IO		
R4	PAD_CN	MSS_MDIO_CLK	MSS_GPIO_31	0	IO	Output Disabled	Pull Up
			MSS_MDIO_CLK	1	O		
U15	PAD_CO	MSS_MIBSPIA_MOSI	MSS_GPIO_0	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIA_MOSI	5	IO		
U16	PAD_CP	MSS_MIBSPIA_MISO	MSS_GPIO_1	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIA_MISO	5	IO		
T16	PAD_CQ	MSS_MIBSPIA_CLK	MSS_GPIO_2	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIA_CLK	5	IO		
T15	PAD_CR	MSS_MIBSPIA_$\overline{CS}$0	MSS_GPIO_3	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIA_$\overline{CS}$0	5	IO		
V17	PAD_$\overline{CS}$	MSS_MIBSPIA_HOSTIRQ	MSS_GPIO_4	0	IO	Output Disabled	Pull Down
			MSS_GPIO_2	2	IO		
			MSS_GPIO_8	3	IO		
			MSS_MIBSPIA_HOSTIRQ	5	O		
			MSS_MIBSPIB_$\overline{CS}$2	6	IO		
			MSS_GPIO_2	7	IO		
			MSS_GPIO_8	10	IO		
B16	PAD_DA	MSS_UARTA_RX	MSS_GPIO_12	0	IO	Output Disabled	Pull Up
			MSS_CPTS0_TS_SYNC	1	O		
			MSS_GPIO_8	3	IO		
			MSS_UARTB_TX	4	IO		
			MSS_UARTA_RX	5	IO		
			DSS_UARTA_TX	6	IO		
C16	PAD_DB	MSS_UARTA_TX	SOP[4]	During Power-up	I	Output Disabled	
			MSS_GPIO_13	0	IO		
			MSS_CPTS0_HW2TSPUSH	1	I		
			MSS_GPIO_9	3	IO		
			MSS_UARTB_RX	4	IO		
			MSS_UARTA_TX	5	IO		
			DSS_UARTA_RX	6	IO		

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BALL NUMBER (1)	PAD NAME (9)	BALL NAME (2)	SIGNAL NAME (3)	MODE (4),(8)	TYPE (5)	BALL RESET STATE (6)	PULL UP/DOWN TYPE (7)
A15	PAD_DC	DSS_UARTA_TX	MSS_GPIO_14	0	IO	Output Disabled	Pull Up
			MSS_CPTS0_HW1TSPUSH	1	I		
			MSS_GPIO_10	3	IO		
			DSS_UARTA_TX	4	IO		
			MSS_UARTA_RX	6	IO		
B14	PAD_DD	DSS_UARTA_RX	MSS_GPIO_15	0	IO	Output Disabled	Pull Up
			DSS_UARTA_RX	1	IO		
			MSS_GPIO_11	3	IO		
			MSS_UARTA_TX	6	IO		
A14	PAD_DE	MSS_UARTB_TX	SOP[3]	During Power-up	I	Output Disabled	
			MSS_GPIO_0	0	IO		
			DSS_UARTA_TX	1	IO		
			MSS_EPWMB_SYNCI	3	I		
			MSS_UARTA_TX	5	IO		
			MSS_UARTB_TX	6	IO		
			LVDS_VALID	8	O		
			MSS_GPIO_31	12	IO		
B13	PAD_DF	XREF_CLK0	MSS_GPIO_1	0	IO	Output Disabled	Pull Down
			XREF_CLK0	1	I		
			MSS_GPIO_8	3	IO		
			MCU_CLKOUT	6	O		
			MSS_GPIO_30	12	IO		
D11	PAD_DG	XREF_CLK1	MSS_GPIO_2	0	IO	Output Disabled	Pull Down
			XREF_CLK1	1	I		
			MSS_GPIO_9	3	IO		
			PMIC_CLKOUT	7	O		
			MSS_GPIO_29	12	IO		

(1) **BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.
(2) **BALL NAME:** Mechanical name from package device (name is taken based on an example implementation).
(3) **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).
(4) **MODE:** Multiplexing mode number: value written to PinMux Cntl register to select specific Signal name for this Ball number. Mode column has bit range value.
(5) **TYPE:** Signal type and direction:
- I = Input
- O = Output
- IO = Input or Output

(6) **BALL RESET STATE:** The state of the terminal at power-on reset
(7) **PULL UP/DOWN TYPE:** indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
- Pull Up: Internal pullup
- Pull Down: Internal pulldown
- HiZ

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(8) Pin Mux Control Value maps to lower 4 bits of register.
(9) There are some PADs that are not mapped to dedicated BGA PINs. These unused PADs need to be disabled in application.

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5.3 Signal Descriptions - Digital

Note

All digital IO pins of the device (except NERROR_OUT and WARM_RESET) are non-failsafe; hence, care needs to be taken that they are not driven externally without the VIO supply being present to the device.

Note

The GPIO state during the power supply ramp is not ensured. In case the GPIO is used in the application where the state of the GPIO is critical, even when NRESET is low , a tri-state buffer should be used to isolate the GPIO output from the radar device and a pull resister used to define the required state in the application. The NRESET signal to the radar device could be used to control the output enable (OE) of the tri-state buffer.

Note

ROM bootloader uses only B16 (MSS_UARTA_RX) and C16 (MSS_UARTA_TX) pins for flash programming. It is recommended to use these pins while building the module.

Note

LVDS and Aurora interfaces are intended for debugging and development purposes, not for production use.

Table 5-1. Signal Descriptions - Digital

FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	PIN NUMBER
SPI Interface	MSS_MIBSPIA_CLK	IO	SPI Channel A - Clock	T16
	MSS_MIBSPIA_MOSI	IO	SPI Channel A - Controller Out Peripheral In	U15
	MSS_MIBSPIA_MISO	IO	SPI Channel A - Controller In Peripheral Out	U16
	MSS_MIBSPIA_$\overline{CS}$0	IO	SPI Channel A Chip Select	T15
	MSS_MIBSPIA_HOSTIRQ	O	Out of Band Interrupt to an external host communicating over SPI	V16,V17
	MSS_MIBSPIB_CLK(1)	IO	SPI Channel B - Clock	T13,R10
	MSS_MIBSPIB_MOSI(1)	IO	SPI Channel B - Controller Out Peripheral In	V12,V11
	MSS_MIBSPIB_MISO(1)	IO	SPI Channel B - Controller In Peripheral Out	U13,U11
	MSS_MIBSPIB_$\overline{CS}$0	IO	SPI Channel B Chip Select (Instance ID 0)	U14,U12
	MSS_MIBSPIB_$\overline{CS}$1	IO	SPI Channel B Chip Select (Instance ID 1)	V16,A16,R14
	MSS_MIBSPIB_$\overline{CS}$2	IO	SPI Channel B Chip Select (Instance ID 2)	A16,V11,R14,V17
CAN-FD	MSS_MCANA_RX	I	CAN-FD A (MCAN) Receive Signal	T13,R12,C14,F16,D16
	MSS_MCANA_TX	O	CAN-FD A (MCAN) Transmit Signal	U14,T11,C12,E17,D17
	MSS_MCANB_RX	I	CAN-FD B (MCAN) Receive Signal	V12,A17
	MSS_MCANB_TX	O	CAN-FD B (MCAN) Transmit Signal	U13,B17
UART (MSS)	MSS_UARTA_RX	IO	Main Subsystem - UART A Receive (For Flash programming)	T13,D13,F16,P17,B16,A15
	MSS_UARTA_TX	IO	Main Subsystem - UART A Transmit (For Flash programming)	U14,D15,E17,U17,C16,B14, A14
	MSS_UARTB_TX	IO	Main Subsystem - UART B Receive	T13,U14,C12,D15,G15,E17, L15,U4,B16,A14
	MSS_UARTB_RX	IO	Main Subsystem - UART B Transmit	R17,F16,T7,C16

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Table 5-1. Signal Descriptions - Digital (continued)

FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	PIN NUMBER
QSPI for Serial Flash	MSS_QSPI_0	IO	QSPI Data Line #0 (Used with Serial Data Flash)	U11
	MSS_QSPI_1	I	QSPI Data Line #1 (Used with Serial Data Flash)	V11
	MSS_QSPI_2	I	QSPI Data Line #2 (Used with Serial Data Flash)	T11
	MSS_QSPI_3	I	QSPI Data Line #3 (Used with Serial Data Flash)	R12
	MSS_QSPI_CLK	IO	QSPI clock (Used with Serial Data Flash)	R10
	MSS_QSPI_$\overline{CS}$	O	QSPI chip select (Used with Serial Data Flash)	U12
I2C interface	MSS_I2CA_SDA	IO	I2C Clock	V12,E17,U17,R8
	MSS_I2CA_SCL	IO	I2C Data	U13,F16,P17,U9
RS232 UART	MSS_RS232_RX	IO	Debug UART (Operates as Bus controller) - Receive Signal	F16
	MSS_RS232_TX	IO	Debug UART (Operates as Bus controller) - Transmit Signal	E17
PWM Module	MSS_EPWMA0	O	PWM Module 1 - Output A0	V12,R15,E17,E15,B17,R6
	MSS_EPWMA1	O	PWM Module 1 - Output A1	B15,T17,E17,C18,A17,U8
	MSS_EPWMA_SYNCI	I	PWM Module 1 - Sync Input	A16,D17
	MSS_EPWMA_SYNCO	O	PWM Module 1 - Sync Output	D16
	MSS_EPWMB0	O	PWM Module 2 - Output B0	B15,U13,T17,R14,F16,E17, B17,C17,T7
	MSS_EPWMB1	O	PWM Module 2 - Output B1	R14,F16,A17,R8
	MSS_EPWMB_SYNCI	I	PWM Module 2 - Sync Input	T18,A14
	MSS_EPWMB_SYNCO	O	PWM Module 2 - Sync Output	P16
	MSS_EPWMC0	O	PWM Module 3 - Output C0	T13,F16,E15,C17,U4
	MSS_EPWMC1	O	PWM Module 3 - Output C1	C18,U9
	MSS_EPWMC_SYNCI	I	PWM Module 3 - Sync Input	P17
	MSS_EPWMC_SYNCO	O	PWM Module 3 - Sync Output	N15
	MSS_EPWM_TZ0	I	PWM module Trip Signal 0	G15,J15
	MSS_EPWM_TZ1	I	PWM module Trip Signal 1	A16,M16
	MSS_EPWM_TZ2	I	PWM module Trip Signal 2	B15,L15

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Table 5-1. Signal Descriptions - Digital (continued)

FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	PIN NUMBER
RGMII/RMII/MII Ethernet	MSS_MII_COL	I	MSS Ethernet MII Collision Detect	U8
	MSS_MII_CRS	I	MSS Ethernet MII Carrier Sense	R8
	MSS_MII_RXER	I	MSS Ethernet MII Receive Error	U9
	MSS_MII_TXEN	O	MSS Ethernet MII Transmit Enable	R6
	MSS_MII_RXDV	I	MSS Ethernet MII Receive Data Valid	T7
	MSS_MII_TXD3	O	MSS Ethernet MII Transmit Data 3	U4
	MSS_MII_TXD2	O	MSS Ethernet MII Transmit Data 2	U6
	MSS_MII_TXD1	O	MSS Ethernet MII Transmit Data 1	U5
	MSS_MII_TXD0	O	MSS Ethernet MII Transmit Data 0	U7
	MSS_MII_TXCLK	I	MSS Ethernet MII Transmit Clock	V3
	MSS_MII_RXCLK	I	MSS Ethernet MII Receive Clock	T9
	MSS_MII_RXD3	I	MSS Ethernet MII Receive Data 3	U10
	MSS_MII_RXD2	I	MSS Ethernet MII Receive Data 2	V5
	MSS_MII_RXD1	I	MSS Ethernet MII Receive Data 1	V4
	MSS_MII_RXD0	I	MSS Ethernet MII Receive Data 0	V6
	MSS_RMII_REFCLK	IO	MSS Ethernet RMII Clock Input	U8,T9
	MSS_RMII_CRS_DV	I	MSS Ethernet RMII Carrier Sense/Receive Data Valid	R8,T7
	MSS_RMII_RXER	I	MSS Ethernet RMII Receive Error	U9
	MSS_RMII_TXEN	O	MSS Ethernet RMII Transmit Enable	R6
	MSS_RMII_TXD1	O	MSS Ethernet RMII Transmit Data 1	U5
	MSS_RMII_TXD0	O	MSS Ethernet RMII Transmit Data 0	U7
	MSS_RMII_RXD1	I	MSS Ethernet MII Receive Data 1	V4
	MSS_RMII_RXD0	I	MSS Ethernet MII Receive Data 0	V6
	MSS_RGMII_TCTL	O	MSS Ethernet RGMII Transmit Control	R6
	MSS_RGMII_RCTL	I	MSS Ethernet RGMII Receive Control	T7
	MSS_RGMII_TD3	O	MSS Ethernet RGMII Transmit Data 3	U4
	MSS_RGMII_TD2	O	MSS Ethernet RGMII Transmit Data 2	U6
	MSS_RGMII_TD1	O	MSS Ethernet RGMII Transmit Data 1	U5
	MSS_RGMII_TD0	O	MSS Ethernet RGMII Transmit Data 0	U7
	MSS_RGMII_TCLK	O	MSS Ethernet RGMII Transmit Clock	V3
	MSS_RGMII_RCLK	I	MSS Ethernet RGMII Receive Clock	T9
	MSS_RGMII_RD3	I	MSS Ethernet RGMII Receive Data 3	U10
	MSS_RGMII_RD2	I	MSS Ethernet RGMII Receive Data 2	V5
	MSS_RGMII_RD1	I	MSS Ethernet RGMII Receive Data 1	V4
	MSS_RGMII_RD0	I	MSS Ethernet RGMII Receive Data 0	V6
	MSS_MDIO_DATA	IO	MSS Ethernet Manage Data Input/Output data	T5
	MSS_MDIO_CLK	O	MSS Ethernet Manage Data Input/Output Clock	R4
	MSS_CPTS0_TS_SYNC	O	Ethernet Timestamp SYNC output	B16
	MSS_CPTS0_HW2TSPUSH	I	Ethernet hardware Timestamp Inputs Pins	C16
	MSS_CPTS0_HW1TSPUSH	I		A15

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Table 5-1. Signal Descriptions - Digital (continued)

FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	PIN NUMBER
Trace Signal	TRACE_DATA_0	O	Debug Trace Output - Data Line	U17
	TRACE_DATA_1	O	Debug Trace Output - Data Line	P17
	TRACE_DATA_2	O	Debug Trace Output - Data Line	T18
	TRACE_DATA_3	O	Debug Trace Output - Data Line	N15
	TRACE_DATA_4	O	Debug Trace Output - Data Line	P16
	TRACE_DATA_5	O	Debug Trace Output - Data Line	L15
	TRACE_DATA_6	O	Debug Trace Output - Data Line	M16
	TRACE_DATA_7	O	Debug Trace Output - Data Line	J15
	TRACE_DATA_8	O	Debug Trace Output - Data Line	D17
	TRACE_DATA_9	O	Debug Trace Output - Data Line	D16
	TRACE_DATA_10	O	Debug Trace Output - Data Line	E15
	TRACE_DATA_11	O	Debug Trace Output - Data Line	C18
	TRACE_DATA_12	O	Debug Trace Output - Data Line	B17
	TRACE_DATA_13	O	Debug Trace Output - Data Line	A17
	TRACE_DATA_14	O	Debug Trace Output - Data Line	C17
	TRACE_CLK	O	Debug Trace Output - Clock	R15
	TRACE_CTL	O	Debug Trace Output - Control	T17

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Table 5-1. Signal Descriptions - Digital (continued)

FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	PIN NUMBER
DMM Interface	DMM0	I	Debug Interface (Hardware In Loop) - Data Line	U17
	DMM1	I	Debug Interface (Hardware In Loop) - Data Line	P17
	DMM2	I	Debug Interface (Hardware In Loop) - Data Line	T18
	DMM3	I	Debug Interface (Hardware In Loop) - Data Line	N15
	DMM4	I	Debug Interface (Hardware In Loop) - Data Line	P16
	DMM5	I	Debug Interface (Hardware In Loop) - Data Line	L15
	DMM6	I	Debug Interface (Hardware In Loop) - Data Line	M16
	DMM7	I	Debug Interface (Hardware In Loop) - Data Line	J15
	DMM8	I	Debug Interface (Hardware In Loop) - Data Line	D17
	DMM9	I	Debug Interface (Hardware In Loop) - Data Line	D16
	DMM10	I	Debug Interface (Hardware In Loop) - Data Line	E15
	DMM11	I	Debug Interface (Hardware In Loop) - Data Line	C18
	DMM12	I	Debug Interface (Hardware In Loop) - Data Line	B17
	DMM13	I	Debug Interface (Hardware In Loop) - Data Line	A17
	DMM14	I	Debug Interface (Hardware In Loop) - Data Line	C17
	DMM_CLK	I	Debug Interface (Hardware In Loop) - Clock	R15
	DMM_SYNC	I	Debug Interface (Hardware In Loop) - Sync	T17
	DMM_MUX_IN	I	Debug Interface (Hardware In Loop) Mux Select between DMM1 and DMM2 (Two Instances)	A16,R17,R14
	NDMM_EN	O	Debug Interface (Hardware In Loop) Enable - Active Low Signal	D15,E17

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Table 5-1. Signal Descriptions - Digital (continued)

FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	PIN NUMBER
General-purpose I/Os	MSS_GPIO_0	IO	General-purpose I/O	B15,P17,U15,A14
	MSS_GPIO_1	IO	General-purpose I/O	A16,T18,U16,B13
	MSS_GPIO_2	IO	General-purpose I/O	G15,N15,T16,V17,D11
	MSS_GPIO_3	IO	General-purpose I/O	P16,T15
	MSS_GPIO_4	IO	General-purpose I/O	U14,L15,V17
	MSS_GPIO_5	IO	General-purpose I/O	T13,M16
	MSS_GPIO_6	IO	General-purpose I/O	U12,J15
	MSS_GPIO_7	IO	General-purpose I/O	R10,D17
	MSS_GPIO_8	IO	General-purpose I/O	U11,T18,D16,V17,B16,B13
	MSS_GPIO_9	IO	General-purpose I/O	V11,N15,E15,C16,D11
	MSS_GPIO_10	IO	General-purpose I/O	T11,M16,C18,A15
	MSS_GPIO_11	IO	General-purpose I/O	R12,J15,B17,B14
	MSS_GPIO_12	IO	General-purpose I/O	V16,A17,B16
	MSS_GPIO_13	IO	General-purpose I/O	B15,C17,C16
	MSS_GPIO_14	IO	General-purpose I/O	E17,A15
	MSS_GPIO_15	IO	General-purpose I/O	F16,B14
	MSS_GPIO_16	IO	General-purpose I/O	A16
	MSS_GPIO_17	IO	General-purpose I/O	C12,C17,U8
	MSS_GPIO_18	IO	General-purpose I/O	C14,A17,R8
	MSS_GPIO_19	IO	General-purpose I/O	B17,U9
	MSS_GPIO_20	IO	General-purpose I/O	C18,R6
	MSS_GPIO_21	IO	General-purpose I/O	V12,E15,T7
	MSS_GPIO_22	IO	General-purpose I/O	U13,D16,U4
	MSS_GPIO_23	IO	General-purpose I/O	D13,D17,U6
	MSS_GPIO_24	IO	General-purpose I/O	D15,J15,U5
	MSS_GPIO_25	IO	General-purpose I/O	R15,M16,U7
	MSS_GPIO_26	IO	General-purpose I/O	G15,L15,V3
	MSS_GPIO_27	IO	General-purpose I/O	T17,P16,T9
	MSS_GPIO_28	IO	General-purpose I/O	R17,N15,U10
	MSS_GPIO_29	IO	General-purpose I/O	R14,T18,V5,D11
	MSS_GPIO_30	IO	General-purpose I/O	P17,V4,T5,B13
	MSS_GPIO_31	IO	General-purpose I/O	U17,V6,R4,A14
UART (DSS)	DSS_UARTA_TX	IO	Debug UART Transmit [DSP]	U13,R10,J15,B16,A15,A14
	DSS_UARTA_RX	IO	Debug UART Receive [DSP]	D13,R17,C16,B14
Chirp/Frame signals	ADC_VALID	O	When high, indicating valid ADC samples	V16,T11,R12,R17
	CHIRP_START	O	Pulse signal indicating the start of each chirp	G15,T17
	CHIRP_END	O	Pulse signal indicating the end of each chirp	G15,T17
	FRAME_START	O	Pulse signal indicating the start of each frame	R15,G15,T17
LVDS_VALID	LVDS_VALID	O	When high, indicating valid LVDS data	A16,R15,G15,T17,R14,E17, A14
External clock out	MCU_CLKOUT	O	Programmable clock given out to external MCU or the processor	R15,B13
	PMIC_CLKOUT	O	Output Clock from the device for PMIC	B15,G15,T17,D11

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Table 5-1. Signal Descriptions - Digital (continued)

FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	PIN NUMBER
System Synchronization	SYNC_IN	I	Low frequency Synchronization signal input	R17
	SYNC_OUT	O	Low Frequency Synchronization Signal output	A16,G15,R17,R14
Clock Output	OBS_CLKOUT	O	Observation Clock Output	R15,T17
	RCOSC_CLK	O	Internal RCOSC Clock Output	R14
Reference Clock	XREF_CLK0	I	External reference input clock 0	B13
	XREF_CLK1	I	External reference input clock 1	D11
JTAG	TCK	I	JTAG Test Clock	C12
	TMS	IO	JTAG Test Mode Signal	C14
	TDI	I	JTAG Test Data Input	D13
	TDO	O	JTAG Test Data Output	D15
UART (BSS)	BSS_UARTA_TX	O	Debug UART Transmit [Radar Block]	A16,T13,U14,C14,D15,F16, E17,M16
	BSS_UARTA_RX	I	Debug UART Receive [Radar Block]	C12,R15
Reset	WARM_RESET	IO	Open drain fail safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset.	B12
Safety	NERROR_OUT	O	Open drain fail safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.	C11
Sense On power	SOP[0]	I	The SOP pins are driven externally (weak drive) and the mmWave device senses the state of these pins during bootup to decide the bootup mode. After boot the same pins have other functionality. • [SOP2 SOP1 SOP0] = [0 0 1] -> Functional QSPI load mode • [SOP2 SOP1 SOP0] = [1 0 1] -> UART load mode • [SOP2 SOP1 SOP0] = [0 1 1] -> debug and development mode The following configuration of SOP pins help decide the reference crystal frequency • [SOP4 SOP3] = [0 0] -> 40 MHz	D15
	SOP[1]	I		R14
	SOP[2]	I		T17
	SOP[3]	I		A14
	SOP[4]	I		C16
CSI2 RX	CSI2_RX0M0	I	CSI2.0 Receiver #1, Negative Polarity, Lane 0	N18
	CSI2_RX0P0	I	CSI2.0 Receiver #1, Positive Polarity, Lane 0	N17
	CSI2_RX0CLKM	I	CSI2.0 Receiver #1, Clock Input, Negative Polarity	L18
	CSI2_RX0CLKP	I	CSI2.0 Receiver #1, Clock Input, Positive Polarity	L17
	CSI2_RX0M1	I	CSI2.0 Receiver #1, Negative Polarity Lane 1	M18
	CSI2_RX0P1	I	CSI2.0 Receiver #1, Positive Polarity Lane 1	M17

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Table 5-1. Signal Descriptions - Digital (continued)

FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	PIN NUMBER
Aurora LVDS	LVDS_TXM0	O	LVDS/Aurora Transmitter, Data Output, Lane 0	F18
	LVDS_TXP0	O		F17
	LVDS_TXM2_CLKM	O	LVDS Clock, Aurora Data output - Lane 2	G18
	LVDS_TXP2_CLKP	O		G17
	LVDS_TXM3_FRCLKM	O	LVDS Frame Clock, Aurora Data Output - Lane 3	H18
	LVDS_TXP3_FRCLKP	O		H17
	LVDS_TXM1	O	LVDS/Aurora Transmitter, Data Output, Lane 1	J18
	LVDS_TXP1	O		J17

(1) In order to meet SPI timings, it is recommended to use MSS_MIBSPIB_CLK = T13 with MSS_MIBSPIB_MOSI = V12 and MSS_MIBSPIB_MISO = U13. The same applies for the other MSS_MIBSPIB_CLK = R10 as well i.e. with MSS_MIBSPIB_MOSI = V11 and MSS_MIBSPIB_MISO = U11

5.4 Signal Descriptions - Analog

INTERFACE	SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NO.
Transmitters	TX1	O	Single ended transmitter 1 O/P	B3
	TX2	O	Single ended transmitter 2 O/P	B5
	TX3	O	Single ended transmitter 3 O/P	B7
	TX4(1)	O	Single ended transmitter 4 O/P	B9
Receivers	RX1	I	Single ended receiver 1 I/P	M2
	RX2	I	Single ended receiver 2 I/P	K2
	RX3	I	Single ended receiver 3 I/P	H2
	RX4	I	Single ended receiver 4 I/P	F2
Reset	NRESET	I	Power on reset for chip. Active low	H16
Reference Oscillator	CLKP	I	In XTAL mode: Input for the reference crystal In External clock mode: Single ended input reference clock port	D1
	CLKM	I	In XTAL mode: Feedback drive for the reference crystal In External clock mode: Connect this port to ground	B1
Reference clock	OSC_CLKOUT	O	Reference clock output from clocking subsystem after cleanup PLL	A11
Bandgap voltage	VBGAP	O	Device's Band Gap Reference Output	K4
Power supply	VDD	Power	1.2V digital power supply	E12,E13,E14,F14,H14,J14,K14,L14,N6,N14,P6,P7,P9,P10,P11,P13,P14
	VDD_SRAM	Power	1.2V power rail for internal SRAM	V7
	VNWA	Power	1.2V power rail for SRAM array back bias	V13
	VIOIN	Power	I/O Supply (3.3V or 1.8V): All CMOS I/Os would operate on this supply	A13,B18,R18,V8,V15
	VIOIN_18	Power	1.8V supply for CMOS IO	D18,U18,V10
	VDDA_18CLK	Power	1.8V supply for clock module	D9
	VDDA_18PM	Power	1.8V supply for PM module	R1
	VIOIN_18LVDS	Power	1.8V supply for LVDS port	K17
	VIOIN_18CSI	Power	1.8V supply for CSI port	K18
	VPP	Power	Voltage supply for fuse chain	U3

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INTERFACE	SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NO.
Power supply	VIDDA_10RF1	Power	1V Analog and RF supply,VDDA_10RF1 and VDDA_10RF2 could be shorted on the board	M4
	VDDA_10RF2	Power	1V Analog and RF supply	D6, D7
	VDDA_18BB	Power	1.8V Analog base band power supply	P1
	VDDA_18VCO	Power	1.8V RF VCO supply	E4
	VSS(3)	Ground	Digital ground	A12,A18,E11,E18,F8,F9,F10,F11,F12,F13,G7,G8,G9,G10,G11,G12,G13,G14,H7,H8,H9,H10,H11,H12,H13,J7,J8,J9,J10,J11,J12,J13,K7,K8,K9,K10,K11,K12,K13,K16,L7,L8,L9,L10,L11,L12,L13,M7,M8,M9,M10,M11,M12,M13,M14,N7,N8,N9,N10,N11,N12,N13,P8,P12,P18,V2,V9,V14,V18
	VSSA(4)	Ground	Analog ground	A1,A2,A4,A6,A8,A10,B2,B4,B6,B8,B10,B11,C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,D2,D3,E1,E2,E3,F3,F6,F7,G1,G2,G3,G6,H3,H6,J1,J2,J3,J6,K3,K6,L1,L2,L3,L6,M3,M6,N1,N2,N3,V1
Internal LDO output/ inputs	VOUT_14APLL	O	Internal LDO output	H4
	VOUT_14SYNTH	O	Internal LDO output	G4
General purpose ADC inputs for external voltage monitoring(2)	ADC1	IO	ADC Channel 1	P3
	ADC2	IO	ADC Channel 2	P2
	ADC3	IO	ADC Channel 3	R3
	ADC4	IO	ADC Channel 4	R2
	ADC5	IO	ADC Channel 5	T3
	ADC6	IO	ADC Channel 6	U2
	ADC7	IO	ADC Channel 7	T1
	ADC8	IO	ADC Channel 8	T2
	ADC9	IO	ADC Channel 9	U1

(1) TX4 is only applicable in the AWR294x variant with 4 transmitters i.e. AWR2944.
(2) For details, see Section 7.4.3
(3) Corner BGAs are VSS and redundant, meaning if they fail the device will still function.
(4) The VSSA BGAs around the launches are not redundant and are required for functionality.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETERS		MIN	MAX	UNIT
VDD	1.2V digital power supply	–0.5	1.4	V
VDD_SRAM	1.2V power rail for internal SRAM	–0.5	1.4	V
VNWA	1.2V power rail for SRAM array back bias	–0.5	1.4	V
VIOIN	I/O supply (3.3V or 1.8 V): All CMOS I/Os would operate on this supply.	–0.5	3.8	V
VIOIN_18	1.8V supply for CMOS IO	–0.5	2	V
VDDA_18CLK	1.8V supply for clock module	–0.5	2	V
VDDA_18PM	1.8V supply for the PM Module	-0.5	2	V
VIOIN_18CSI	1.8V supply for CSI2 port	–0.5	2	V
VIOIN_18LVDS	1.8V supply for LVDS port	–0.5	2	V
VDDA_10RF1	1V Analog and RF supply, VDDA_10RF1 and VDDA_10RF2 could be shorted on the board.	–0.5	1.4	V
VDDA_10RF2				
VDDA_18BB	1.8-V Analog baseband power supply	–0.5	2	V
VDDA_18VCO supply	1.8-V RF VCO supply	–0.5	2	V
RX1-4	Externally applied power on RF inputs		10	dBm
TX1-4	Externally applied power on RF outputs(3)		10	dBm
TX1-4	Temperature Sensor Accuracy	±5		℃
Input and output voltage range	Dual-voltage LVCMOS inputs, 3.3V or 1.8V (Steady State)	–0.3V	VIOIN + 0.3	V
	Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input		VIOIN + 20% up to 20% of signal period	
CLKP, CLKM	Input ports for reference crystal	–0.5	2	V
Clamp current	Input or Output Voltages 0.3V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	–20	20	mA
T_J	Operating junction temperature range	–40	140	°C
T_{STG}	Storage temperature range after soldered onto PC board	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) This value is for an externally applied signal level on the TX. Additionally, a reflection coefficient up to Gamma= 1 can be applied on the TX output.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged-device model (CDM), per AEC Q100-011	GPADC5, GPADC6	±350	
			All other non-corner pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.3 Power-On Hours (POH)

JUNCTION TEMPERATURE (T_j) (1) (2)	OPERATING CONDITION	NOMINAL CVDD VOLTAGE (V)	POWER-ON HOURS [POH] (HOURS)
–40°C	50% duty cycle	1.2	1440 (6%)
75°C			4800 (20%)
95°C			15600 (65%)
130°C			1920 (8%)
140°C			240 (1%)

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) The specified POH are applicable with max Tx output power settings using the default firmware gain tables. The specified POH would not be applicable, if the Tx gain table is overwritten using an API.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	1.2V digital power supply	1.14	1.2	1.26	V
VDD_SRAM	1.2V power rail for internal SRAM	1.14	1.2	1.26	V
VNWA	1.2V power rail for SRAM array back bias	1.14	1.2	1.26	V
VIOIN	I/O supply (3.3V or 1.8 V): All CMOS I/Os would operate on this supply.	3.135	3.3	3.465	V
		1.71	1.8	1.89	
VIOIN_18	1.8V supply for CMOS IO	1.71	1.8	1.89	V
VDDA_18CLK	1.8V supply for clock module	1.71	1.8	1.89	V
VDDA_18PM	1.8V supply for the PM module	1.71	1.8	1.89	V
VIOIN_18CSI	1.8V supply for CSI2 port	1.71	1.8	1.89	V
VIOIN_18LVDS	1.8V supply for LVDS port	1.71	1.8	1.89	V
VDDA_10RF1	1V Analog and RF supply. VDDA_10RF1 and VDDA_10RF2 could be shorted on the board	0.95	1	1.05	V
VDDA_10RF2					
VDDA_18BB	1.8-V Analog baseband power supply	1.71	1.8	1.89	V
VDDA_18VCO	1.8V RF VCO supply	1.71	1.8	1.89	V
V_{IH}	Voltage Input High (1.8V mode)	1.17		0.3 + VIOIN	V
	Voltage Input High (3.3V mode)	2.25		0.3 + VIOIN	
V_{IL}	Voltage Input Low (1.8V mode)	-0.3		0.3*VIOIN	V
	Voltage Input Low (3.3V mode)	-0.3		0.62	
V_{OH}	High-level output threshold (I_{OH} = 6 mA)	VIOIN – 450			mV
V_{OL}	Low-level output threshold (I_{OL} = 6 mA)			450	mV
NRESET SOP[4:0]	V_{IL} (1.8V Mode)			0.45	V
	V_{IH} (1.8V Mode)	0.96			
	V_{IL} (3.3V Mode)			0.65	
	V_{IH} (3.3V Mode)	1.57			
T_J	Operating junction temperature range	-40		140	℃

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6.5 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for authenticated boot devices. During the process of writing the customer specific keys or other fields like software version etc. in the efuse, the user needs to provide the VPP supply.

6.5.1 Recommended Operating Conditions for OTP eFuse Programming

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VPP	Supply voltage range for the eFuse ROM domain during normal operation		NC(2)		
	Supply voltage range for the eFuse ROM domain during OTP programming(1)	1.65	1.7	1.75	V
Duration of VPP Supply	If VPP voltage is supplied for more than recommended Hours, it can cause reliability issue			24	Hours
I(VPP)				50	mA

(1) During normal operation, no voltage should be applied to VPP. This can be typically achieved by disabling the external regulator attached to the VPP terminal.
(2) NC: No Connect

6.5.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.

6.5.3 Impact to Your Hardware Warranty

You recognize and accept at your own risk that your use of eFuse permanently alters the TI device. You acknowledge that eFuse can fail due to incorrect operating conditions or programming sequence. Such a failure may render the TI device inoperable and TI will be unable to confirm the TI device conformed to TI device specifications prior to the attempted eFuse. CONSEQUENTLY, in these cases of faulty EFUSE programmability, TI WILL HAVE NO LIABILITY.

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6.6 Power Supply Specifications

Table 6-1 describes the four required power rails which must be provided to the AWR2944 from an external power supply. In the case when 1.8V LVCMOS IO is utilized, VIOIN is powered from a 1.8V rail and the 3.3V rail can be ommited, so only three rails must be provided. Also, depending on the power topology utilized, additional power supply filtering can be required for the RF 1.0V and baseband, clock and VCO 1.8V supplies to meet the required ripple specifications. This additional filtering results in separate supply power nets being generated from these four basic rails.

Table 6-1. Power Supply Rails Characteristics

SUPPLY VOLTAGE	DEVICE BLOCKS POWERED FROM THE SUPPLY	DEVICE POWER NETS
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, CSI2, LVDS, LVCMOS IO	Input: VDDA_18VCO, VDDA_18CLK, VIN_18PM, VDDA_18BB, VIOIN_18CSI, VIOIN_18LVDS, VIOIN_18 LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.0V	Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution	Input: VDDA_10RF2, VDDA_10RF1
3.3V (or 1.8V for 1.8V I/O mode)	LVCMOS IO	VIOIN
1.2V	Core Digital and SRAM	VDD, VDD_SRAM, VNWA
1.7V	Programming OTP eFuse (For secure devices)	VPP

The 1.0V and 1.8V power supply ripple specifications are mentioned in Table 6-2 The spur and ripple levels have a dB to dB relationship, for example, a 1dB increase in supply ripple leads to an approximately 1dB increase in spur level. Values quoted are rms levels for a sinusoidal input applied at the specified frequency.

Table 6-2. Ripple Specifications

FREQUENCY (kHz)	Spur Level (dBc)	RF RAIL	VCO/IF RAIL
		1V (μV_{RMS})	1.8V (uV_{RMS})
10	-85	22	10990
100	-95	8	1420
200	-98	6	730
500	-102	4	450
1000	-105	3	300
2000	-105	3	80
5000	-105	3	60
10000	-105	3	60
15000	-105	2	40
20000	-105	2	40

Power Supply Guidelines

The LP87745-Q1 Power Management IC (PMIC) is recommended for an integrated AWR2944 power solution. This cost and space optimized solution is designed to power the AWR2944 radar sensor and its principal peripherals.

List of benefits when using LP87745-Q1 PMIC to power AWR2944:

1. Full device performance entitlement as validated on TI Evaluation boards
2. Noise/Ripple performance that meets AWR noise/ripple performance specification
   a. LP87745-Q1 has high switching frequency at 17.6MHz switching outside IF band & avoiding the LDOs helps with thermal performance at the system level and bypasses the need for 2nd stage LC filters to suppress the ripple and filter out the spurs.

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b. Thermal dissipation does not affect RF performance

6.7 Power Consumption Summary

Table 6-3 and Table 6-4 summarize the power consumption at the power terminals.

Table 6-3. Maximum Current Ratings at Power Terminals

PARAMETER[1]	SUPPLY NAME	DESCRIPTION	MIN	TYP	MAX[1]	UNIT
Current consumption	VDD, VDD_SRAM, VNWA	Total current drawn by all nodes driven by 1.2V rail			2000	mA
	VDDA_10RF1, VDDA_10RF2	Total current drawn by all nodes driven by 1V rail when all 4 transmitters are used			2300	
	VIOIN_18, VDDA_18CLK, VDDA_18PM, VIOIN_18CSI, VIOIN_18LVDS, VDDA_18BB, VDDA_18VCO	Total current drawn by all nodes driven by 1.8V rail			550	
	VIOIN	Total current drawn by all nodes driven by 3.3V rail			50[2]	

(1) The specified current values are at Max supply voltage level (Recommended operating conditions).
(2) The exact value will depend on the system use case and design.

Table 6-4. Average Power Consumption at Power Terminals

PARAMETER	CONDITION[2]		DESCRIPTION	MIN	TYP[1]	MAX	UNIT
Average power consumption in single chip mode.	3TX, 4RX	25% duty cycle	Use Case: 76-77GHz chirps (for 50% duty cycle) and 80-81GHz chirps (for 25% duty cycle); Regular mode, 37.5Msps sampling rate, 25.6 ms frame periodicity, 256 chirps/frame, 2-µs idle time, 50-µs ramp end time, 7us ADC start time and excess ramp time Activity of cores : • 70% MSS R5F • 70% C66x DSP and HWA • 50% Arm M4F All the above cores under-clocked/ clock-gated during idle times); Ethernet is enabled for data transfer		1.37		W
		50% duty cycle			1.98		
	4TX, 4RX	25% duty cycle			1.44		
		50% duty cycle			2.11		

(1) The Power consumption numbers are for a typical usecase i.e. for a Nominal device at 25C ambient temperature and nominal voltage conditions.
(2) Frame duty cycle represents the ratio of Frame Active and Total Framing time (including Interchirp and Interframe time).

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6.8 RF Specifications

over recommended operating conditions and with run time calibrations enabled (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Receiver	Noise figure			12		dB
	1-dB compression point (Out Of Band)(1)			-7		dBm
	Maximum gain			44		dB
	Gain range			20		dB
	Gain step size			2		dB
	IF bandwidth(2)				15	MHz
	ADC sampling rate				37.5	Msps
	ADC resolution			16		Bits
	Return loss (S11)			-10		dB
	Gain mismatch variation (over temperature)			±0.5		dB
	Phase mismatch variation (over temperature)			±3		°
	Idle Channel Spurs			-90		dBFS
Transmitter	Output power			13.5		dBm
	Phase shifter accuracy			±5		°
	Amplitude noise			-145		dBc/Hz
Clock subsystem	Frequency range		76		81	GHz
	Ramp rate				250(3)	MHz/µs
	Phase noise at 1-MHz offset	76 to 77 GHz (VCO1)		-96		dBc/Hz
		76 to 81 GHz (VCO2)(4)		-95		

(1) 1-dB Compression Point (Out Of Band) is measured by feeding a continuous wave tone at 5% of the programmed HPF cut-off frequency (i.e. blocker tone). The compression point is determined by the blocker power that results in a 1dB compression of the blocker tone at the RX ADC.

(2) The analog IF stages include a second order high pass filter that can be configured to the following -6dB corner frequencies:

Available HPF Corner Frequencies (kHz)
HPF
300, 350, 700, 1400,

The filtering performed by the digital baseband chain is targeted to provide:

- Less than ±0.5 dB pass-band ripple/droop, and
- Better than 60 dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

(3) The max ramp rate depends on the PLL bandwidth configuration set using the"AWR_APLL_SYNTH_BW_CONTROL_SB" API. For more details, refer to the mmWave Radar Interface Control document.

(4) VCO2 supports a maximum continuous range of 4.5GHz. The supported range can span 76-80.5GHz or 76.5-81GHz through VCO2_RANGE_CONFIG in AWR_ CAL_MON_FREQUENCY_* API.

Figure 6-1 shows variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed

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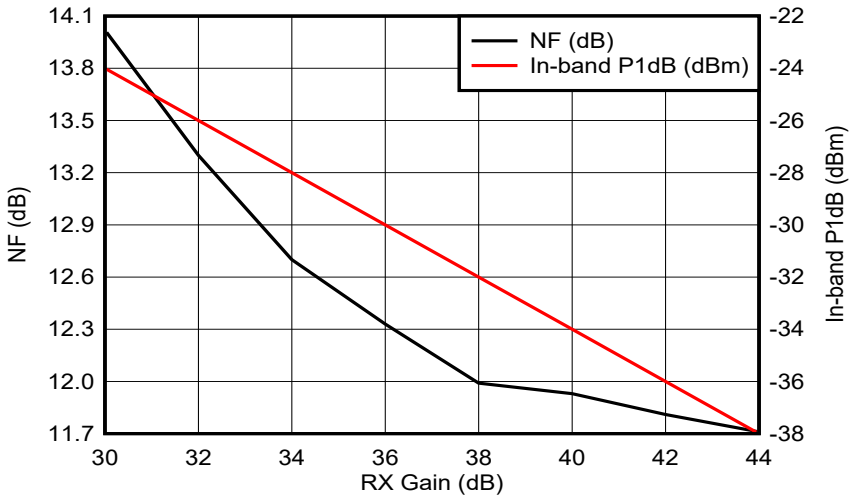

Figure 6-1. Noise Figure, In-band P1dB vs Receiver Gain

6.9 Thermal Resistance Characteristics

THERMAL METRICS(1) (4)		°C/W(2) (3)
$R\Theta_{JC}$	Junction-to-case	3.3
$R\Theta_{JB}$	Junction-to-board	2.9
$R\Theta_{JA}$	Junction-to-free air	14.9
Psi_{JC}	Junction-to-case	0.1
Psi_{JB}	Junction-to-board	2.8

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

A junction temperature of 140°C is assumed.
(4) Air flow = 1 m/s

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6.10 Power Supply Sequencing and Reset Timing

The AWR294x device expects all external 1.2V, 1.8V and 3.3V voltage rails as well as all SOP[4:0] lines to be stable before NRESET is deasserted for a successful device bootup. IO state is not guaranteed until the VIOIN and VIOIN_18 supplies are available. Figure 6-2 describes the device wake-up sequence.

Note

Hardware platform must support supplying 1.7V on the VPP pin only during OTP eFuse programming.

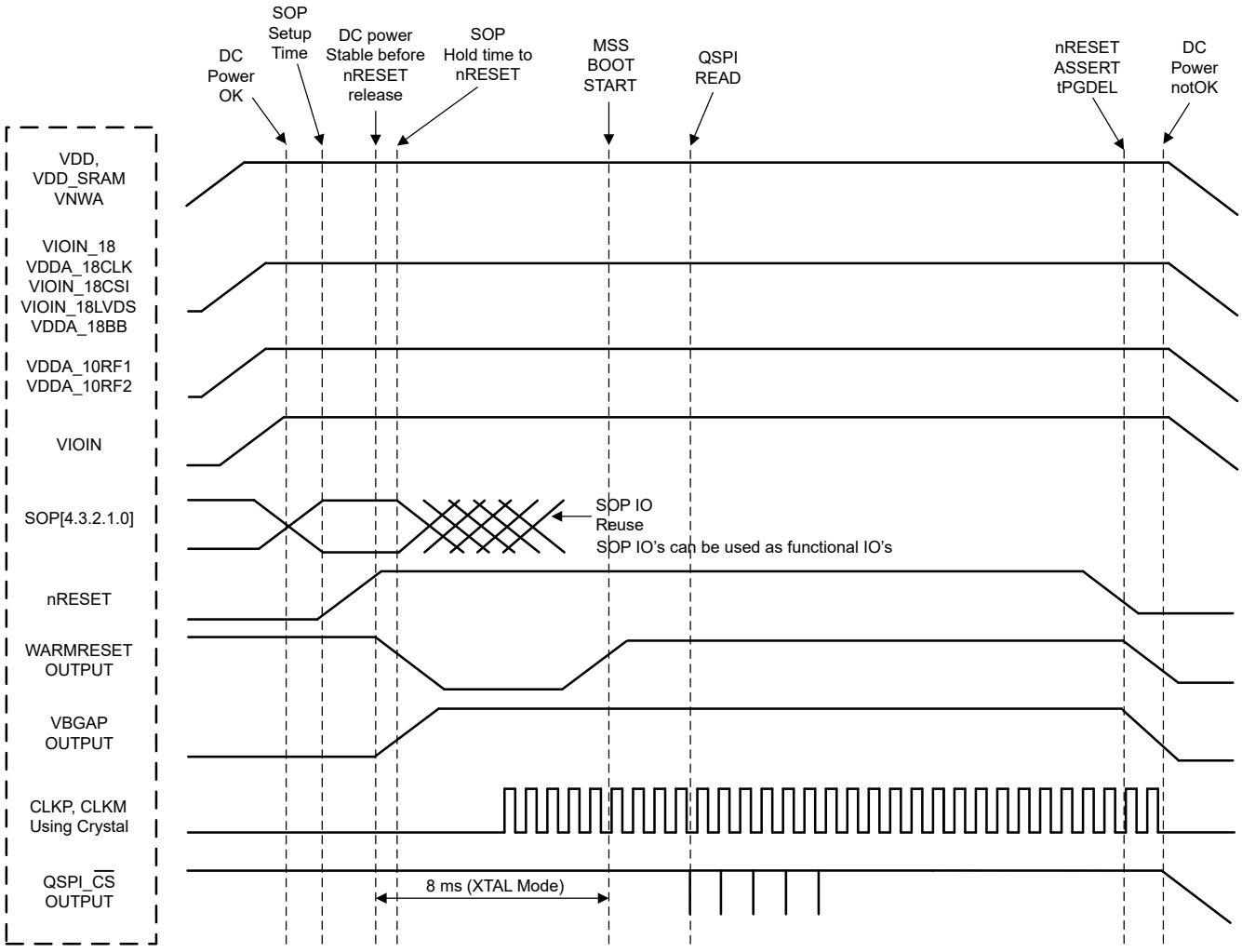

Figure 6-2. Device Wake-up Sequence

6.11 Input Clocks and Oscillators

6.11.1 Clock Specifications

An external crystal is connected to the device pins. Figure 6-3 shows the crystal implementation.

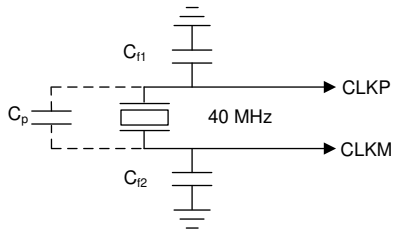

Figure 6-3. Crystal Implementation

Note

The load capacitors, C_{f1} and C_{f2} in Figure 6-3, can be chosen such that Equation 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit can be placed as close as possible to the associated oscillator CLKP and CLKM pins. Note that Cf1 and Cf2 include the parasitic capacitances due to PCB routing.

Note

The board routing parasitics between CLKP/CLKM pins also need to be included in the estimates of C_P

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

Table 6-5 lists the electrical characteristics of the clock crystal.

Table 6-5. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency		40		MHz
C_L	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	-40		140	℃
Frequency tolerance	Crystal frequency tolerance(1) (2)	-100		100(3)	ppm
Drive level			50	200	µW

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
(3) For Ethernet operation, tighter specifications of less than 100 PPM frequency error is required. If the Ethernet interface is not used , a PPM error up to 200 PPM can be tolerated.

In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 40MHz clock is fed externally. Table 6-6 lists the electrical characteristics of the external clock signal.

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Table 6-6. External Clock Mode Specifications

PARAMETER		SPECIFICATION			UNIT
		MIN	TYP	MAX	
Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referred to 40MHz	Frequency		40		MHz
	AC-Amplitude	700		1200	mV (pp)
	DC-trise/fall			10	ns
	Phase Noise at 1 kHz			-132	dBc/Hz
	Phase Noise at 10kHz			–143	dBc/Hz
	Phase Noise at 100kHz			–152	dBc/Hz
	Phase Noise at 1MHz			–153	dBc/Hz
	Duty Cycle	35		65	%
	Freq Tolerance	-100		100	ppm

6.12 Peripheral Information

Initial peripheral descriptions and features are provided in the following sections. Additional peripheral details and interface timing information shall be provided in a later product preview or data sheet release.

6.12.1 QSPI Flash Memory Peripheral

The device includes a Quad-Serial Peripheral Interface for external flash memory access. Flash memory can be utilized for many purposes including: Secondary boot-loader memory, application program memory, security keys storage, and long-term data logs for security and error conditions.

Following features are supported by the QSPI Interface on the device:

- Loopback skew cancellation for clock signal to supported faster flash interface clock rates
- Two chip-select signals to connect two external flash devices
- Memory mapped 'direct' mode and software triggered 'indirect' mode of operation for performing flash data transfers

6.12.1.1 QSPI Timing Conditions

PARAMETER		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	5		15	pF

6.12.1.2 QSPI Timing Requirements (1) (2)

SPECIFICATION NUMBER	PARAMETER		MIN	TYP	MAX	UNIT
Q12	$t_{su(D-SCLK)}$	Setup time, D[3:0] valid before falling SCLK edge (Q12)	5			ns
Q13	$t_{h(SCLK-D)}$	Hold time, D[3:0] valid after falling SCLK edge (Q13)	1			ns
Q14	$t_{su(D-SCLK)}$	Setup time, final D[3:0] bit valid before final falling SCLK edge	5-P(3)			ns
Q15	$t_{h(SCLK-D)}$	Hold time, final D[3:0] bit valid after final falling SCLK edge	1+P(3)			ns

(1) Clock Mode 0 (clock polarity = 0 ; clock phase = 0) is the mode of operation.
(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although nonstandard, The falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.
(3) P = SCLK period in ns.

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6.12.1.3 QSPI Switching Characteristics (1) (2)

SPECIFICATION NUMBER	PARAMETER		MIN	TYP	MAX	UNIT
Q1	$t_{c(SCLK)}$	Cycle time, sclk	12.5			ns
Q2	$t_{w(SCLKL)}$	Pulse duration, sclk low	0.5*P – 0.625			ns
Q3	$t_{w(SCLKH)}$	Pulse duration, sclk high	0.5*P – 0.625			ns
Q4	$t_{d(CS-SCLK)}$	Delay time, sclk falling edge to cs active edge	–M*P – 1		–M*P + 2.5	ns
Q5	$t_{d(SCLK-CS)}$	Delay time, sclk falling edge to cs inactive edge	N*P – 1		N*P + 2.5	ns
Q6	$t_{d(SCLK-D1)}$	Delay time, sclk falling edge to d[0] transition	–4.5		2	ns
Q7	$t_{ena(CS-D1LZ)}$	Enable time, cs active edge to d[0] driven (lo-z)	–P – 4		–P +1	ns
Q8	$t_{dis(CS-D1Z)}$	Disable time, cs active edge to d[0] tri-stated (hi-z)	–P – 4		–P +1	ns
Q9	$t_{d(SCLK-D1)}$	Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only)	–4.5– P		2 – P	ns

(1) P = SCLK period in ns.
(2) M = QSPI_SPI_DC_REG.DDx + 1, N = 2

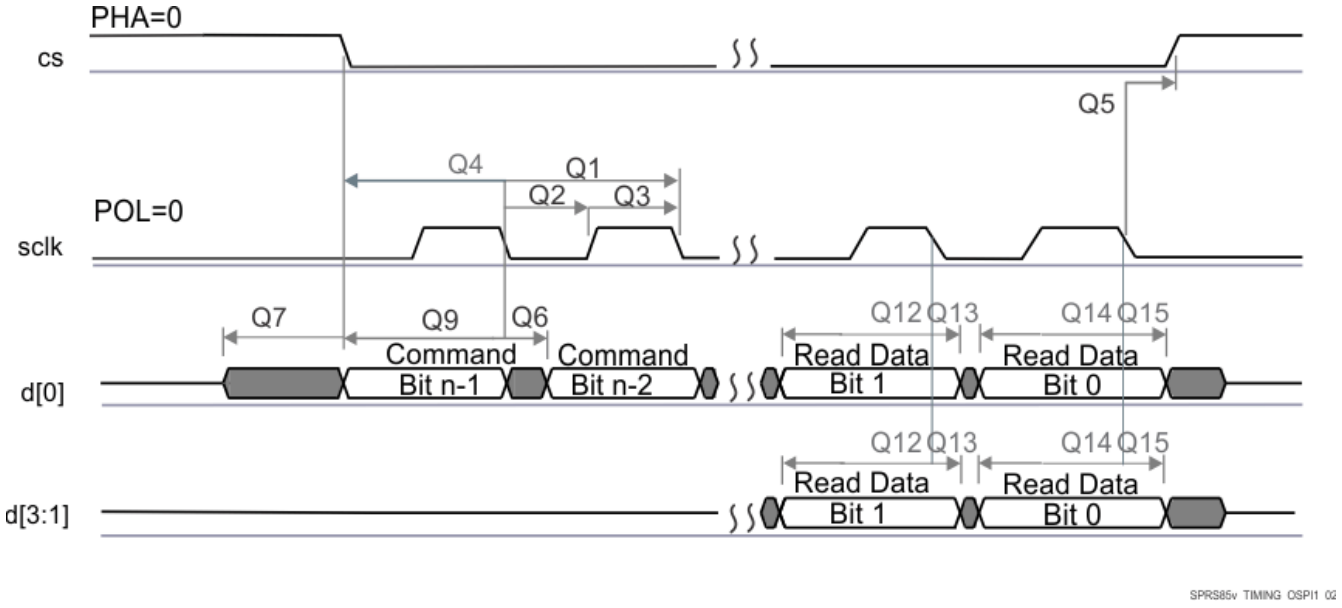

Figure 6-4. QSPI Read (Clock Mode 0)

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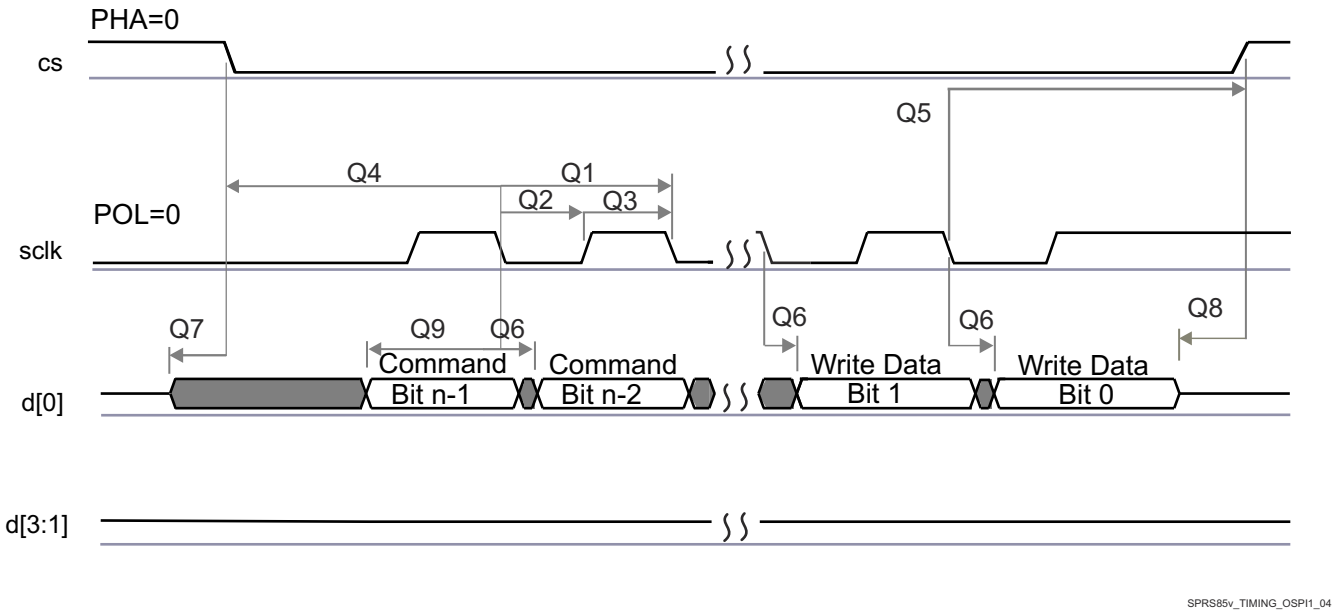

Figure 6-5. QSPI Write (Clock Mode 0)

6.12.2 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

6.12.2.1 MibSPI Peripheral Description

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The device includes two, Multi-Buffered Serial Peripheral Interface (MIBSPI) in the Main Sub-System (MSS). These are intended for external MCU, PMIC, EEPROM and Watchdog communication.

Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit baud clock generator
- SPICLK can be internally-generated (Controller mode) or received from an external clock source (Peripheral mode)
- Maximum clock rate supported over each MIBSPI module shall be 40MHz.
- Each word transferred can have a unique format.
- SPI I/Os not used in the communication can be used as digital input/output signals

6.12.2.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 256 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

Section 6.12.2.2.2 and Section 6.12.2.2.3 assume the operating conditions stated in Section 6.12.2.2.1.

6.12.2.2.1 SPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		20	pF

6.12.2.2.2 SPI Controller Mode Switching Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input) (1) (2) (3)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)	20		$256t_{c(VCLK)}$	ns
2(4)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	
3(4)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	
4(4)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)	$0.5t_{c(SPC)M} - 7$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)	$0.5t_{c(SPC)M} - 7$			
5(4)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)	$0.5t_{c(SPC)M} - 8$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)	$0.5t_{c(SPC)M} - 8$			

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NO.	PARAMETER			MIN	TYP	MAX	UNIT
6[5]	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	(C2TDELAY+2)*$t_{c(VCLK)}$ – 7.5		(C2TDELAY+2) * $t_{c(VCLK)}$ + 7	ns
			CSHOLD = 1	(C2TDELAY +3) * $t_{c(VCLK)}$ – 7.5		(C2TDELAY+3) * $t_{c(VCLK)}$ + 7	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	(C2TDELAY+2)*$t_{c(VCLK)}$ – 7.5		(C2TDELAY+2) * $t_{c(VCLK)}$ + 7	
			CSHOLD = 1	(C2TDELAY +3) * $t_{c(VCLK)}$ – 7.5		(C2TDELAY+3) * $t_{c(VCLK)}$ + 7	
7[5]	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) *$t_{c(VCLK)}$ – 7		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)}$ + 7.5	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) *$t_{c(VCLK)}$ – 7		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)}$ + 7.5	
8[4]	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		5			
9[4]	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		2			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		2			

(1) The Controller bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared (where x= 0 or 1).
(2) $t_{c(MSS_VCLK)}$ = main subsystem clock time = 1 / $f_{(MSS_VCLK)}$. For more details, refer to the device Technical Reference Manual.
(3) When the SPI is in controller mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS+1)t_{c(MSS_VCLK)} \geq 25ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS_VCLK)} \geq 25ns$.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

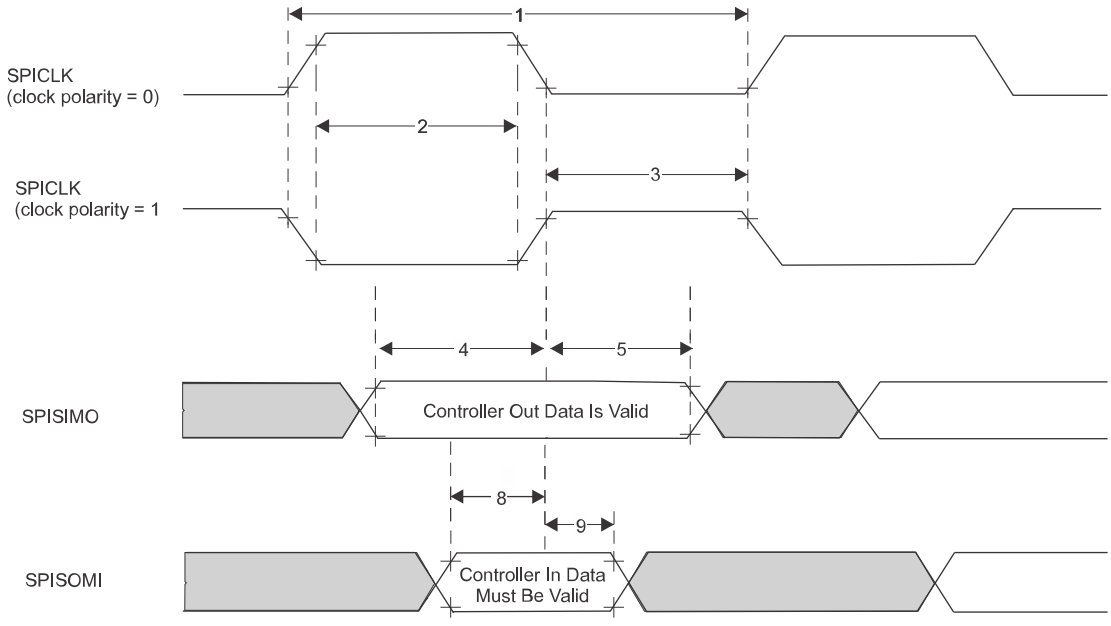

Figure 6-6. SPI Controller Mode External Timing (CLOCK PHASE = 0)

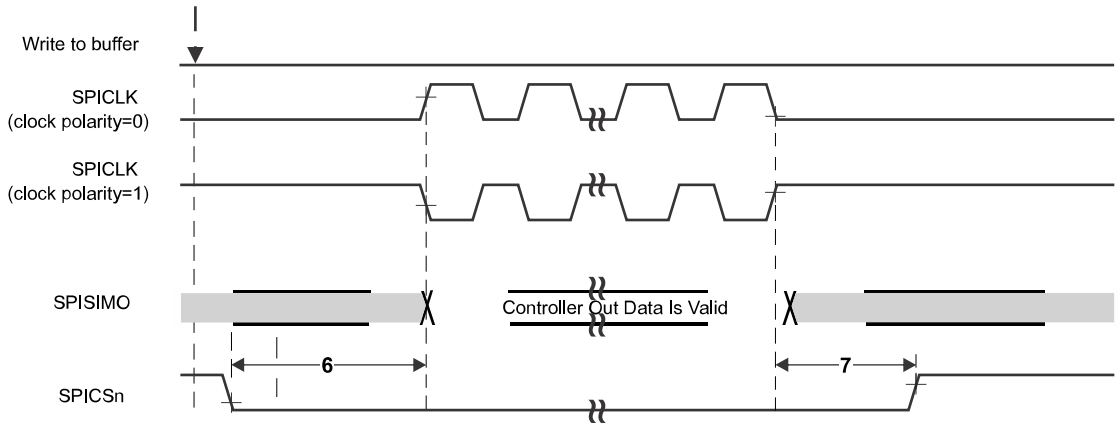

Figure 6-7. SPI Controller Mode Chip Select Timing (CLOCK PHASE = 0)

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6.12.2.2.3 SPI Controller Mode Switching Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input) (1) (2) (3)

NO.	PARAMETER			MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)		20		$256t_{c(VCLK)}$	ns
2(4)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	
3(4)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	
4(4)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 7$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 7$			
5(4)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 8$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 8$			
6(5)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} + 7.5$	
7(5)	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)		$(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)		$(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	
8(4)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		5			
9(4)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		2			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		2			

(1) The Controller bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set (where x = 0 or 1).
(2) $t_{c(MSS_VCLK)}$ = main subsystem clock time = 1 / $f_{(MSS_VCLK)}$. For more details, refer to the device Technical Reference Manual.
(3) When the SPI is in Controller mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(MSS_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS_VCLK)} \geq 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

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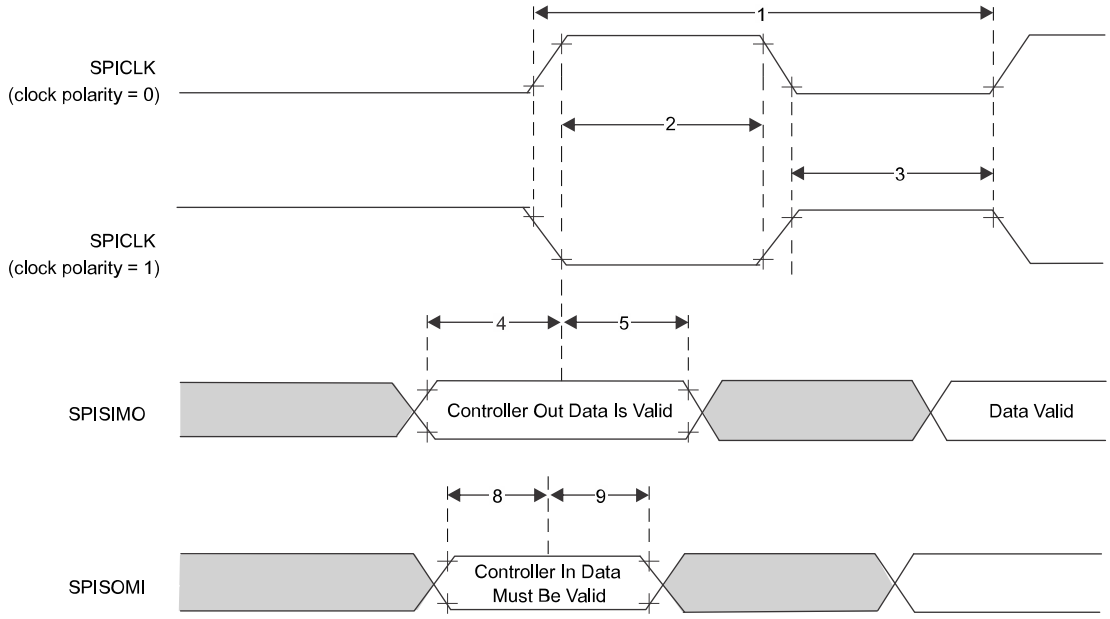

Figure 6-8. SPI Controller Mode External Timing (CLOCK PHASE = 1)

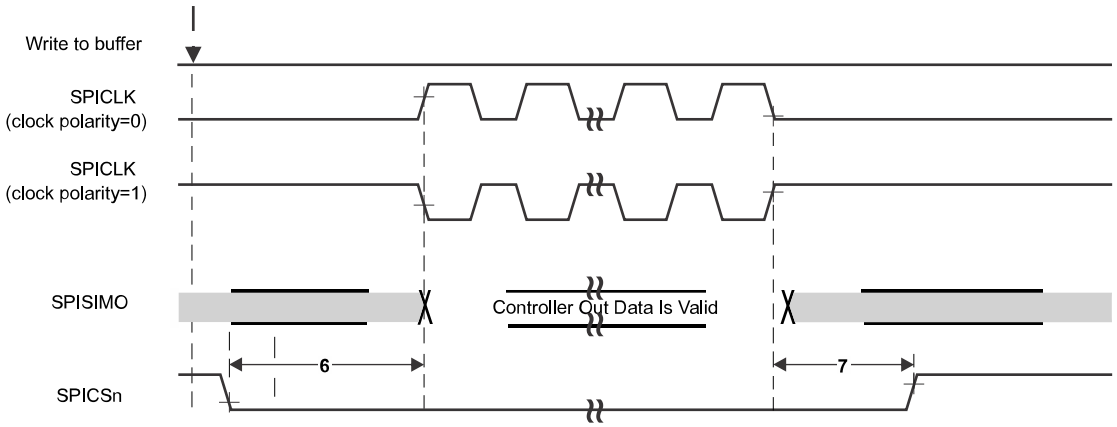

Figure 6-9. SPI Controller Mode Chip Select Timing (CLOCK PHASE = 1)

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6.12.2.3 SPI Peripheral Mode I/O Timings

6.12.2.3.1 SPI Peripheral Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output) (1) (2) (3)

SPECIFICATION NUMBER	PARAMETER(5)		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK (4)	20			ns
2	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	8			ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	8			
3	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	8			ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	8			
4	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)			10	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1)			10	
5	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	2			ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	2			
4	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)			14	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)			14	
5	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	2			ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	2			
6	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	2.1			ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	2.1			
7	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	1			ns
	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	1			

(1) The Controller bit (SPIGCRx.0) is cleared (where x = 0 or 1).
(2) The CLOCK PHASE bit (SPIFMTx.16) is either cleared or set for CLOCK PHASE = 0 or CLOCK PHASE = 1 respectively.
(3) $t_{c(MSS_VCLK)}$ = main subsystem clock time = 1 / $f_{(MSS_VCLK)}$. For more details, refer to the device Technical Reference Manual.
(4) When the SPI is in Peripheral mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS+1)t_{c(MSS_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.For PS values of 0: $t_{c(SPC)S} = 2t_{c(MSS_VCLK)} \geq 25$ ns.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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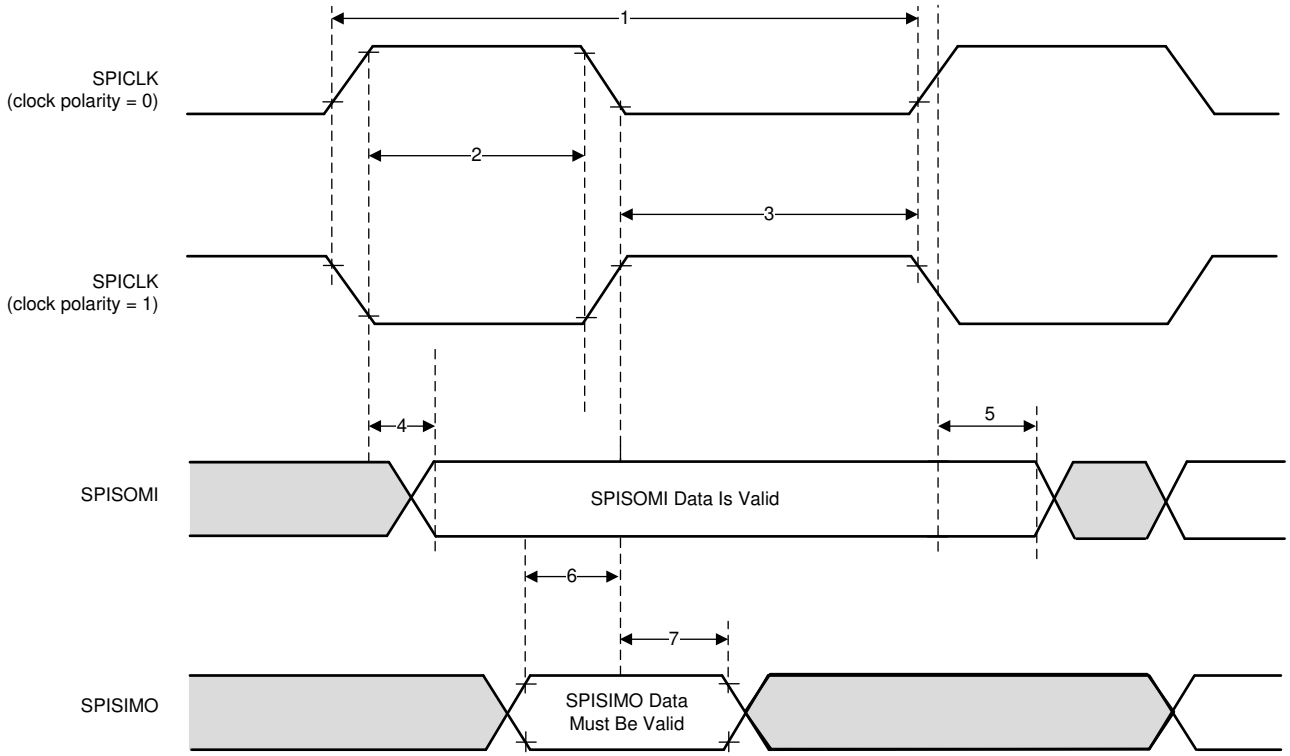

Figure 6-10. SPI Peripheral Mode External Timing (CLOCK PHASE = 0)

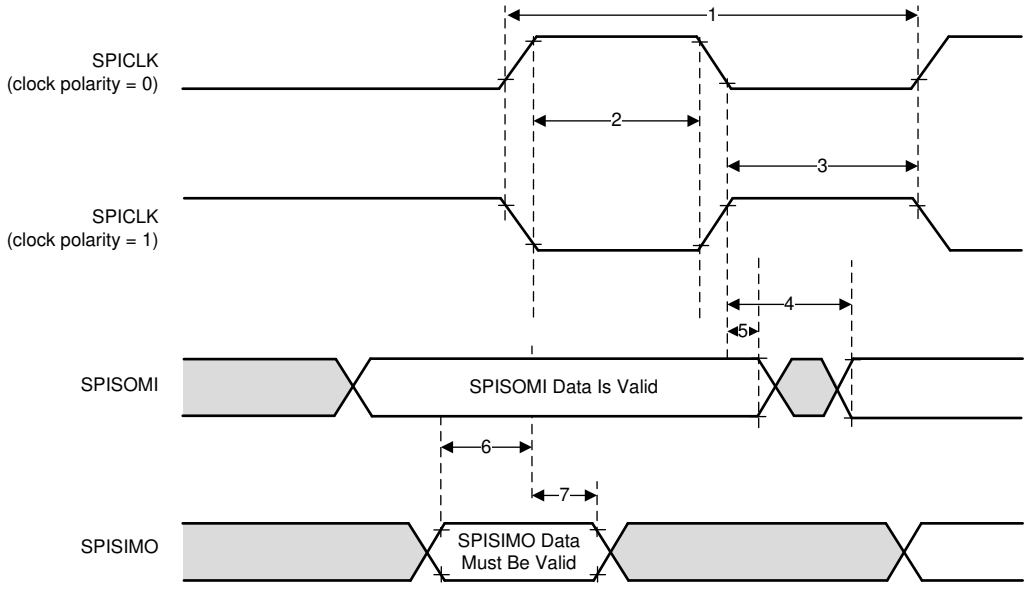

Figure 6-11. SPI Peripheral Mode External Timing (CLOCK PHASE = 1)

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6.12.3 Ethernet Switch (RGMII/RMII/MII) Peripheral

The device integrates a two port Ethernet with one external RGMII/RMII/MII port and another port servicing the Main Sub-System (MSS). This interface is intended to operate primarily as a 100Mbps ECU interface. It can also be used as an instrumentation interface.

- Full Duplex 10/100Mbps wire rate interface to Ethernet PHY over RGMII, RMII, or MII parallel interface
- MDIO Clause 22 and 45 PHY management interface
- IEEE 1588 Synchronous Ethernet support
- AWR synchronous trigger output allowing Ethernet to trigger radar frames

6.12.3.1 RGMII Timing Conditions

SPECIFICATION NUMBER	PARAMETER	MIN	TYP	MAX	UNIT
	Input Conditions				
1	SR_I Input Slew Rate	2.64		5	V/ns
	Output Conditions				
3	C_{LOAD} Output load capacitance	2		20	pF

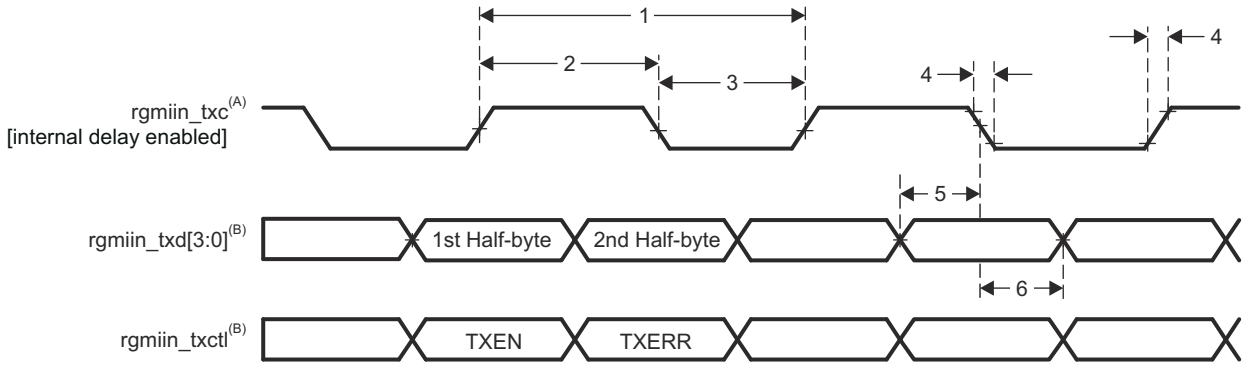
6.12.3.2 RGMII Transmit Clock Switching Characteristics

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(TXC)}$	Cycle time, rgmiin_txc	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
2	$t_{w(TXCH)}$	Pulse duration, rgmiin_txc high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
3	$t_{w(TXCL)}$	Pulse duration, rgmiin_txc low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
4	$t_{t(TXC)}$	Transition time, rgmiin_txc	10 Mbps		0.75	ns
			100 Mbps		0.75	ns

6.12.3.3 RGMII Transmit Data and Control Switching Characteristics

NO.(1)	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
5	$t_{osu(TXD-TXC)}$	Output Setup time, transmit selected signals valid to MSS_RGMII_TCLK high/low	RGMII, Internal Delay Enabled, 10/100 Mbps	1.2		ns
6	$t_{oh(TXC-TXD)}$	Output Hold time, transmit selected signals valid after MSS_RGMII_TCLK high/low	RGMII, Internal Delay Enabled, 10/100 Mbps	1.2		ns

(1) For RGMII, transmit selected signals include: MSS_RGMII_TXD[3:0] and MSS_RGMII_TCTL.



A. TXC is delayed internally before being driven to the rgmiin_txc pin. This internal delay is always enabled.

B. Data and control information is transmitted using both edges of the clocks. rgmiin_txd[3:0] carries data bits 3-0 on the rising edge of rgmiin_txc and data bits 7-4 on the falling edge of rgmiin_txc. Similarly, rgmiin_txctl carries TXEN on rising edge of rgmiin_txc and TXERR of falling edge of rgmiin_txc.

Figure 6-12. RGMII Transmit Interface Switching Characteristics

6.12.3.4 RGMII Receive Clock Timing Requirements

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(RXC)}$	Cycle time, rgmiin_rxc	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
2	$t_{w(RXCH)}$	Pulse duration, rgmiin_rxc high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
3	$t_{w(RXCL)}$	Pulse duration, rgmiin_rxc low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
4	$t_{t(RXC)}$	Transition time, rgmiin_rxc	10 Mbps		0.75	ns
			100 Mbps		0.75	ns

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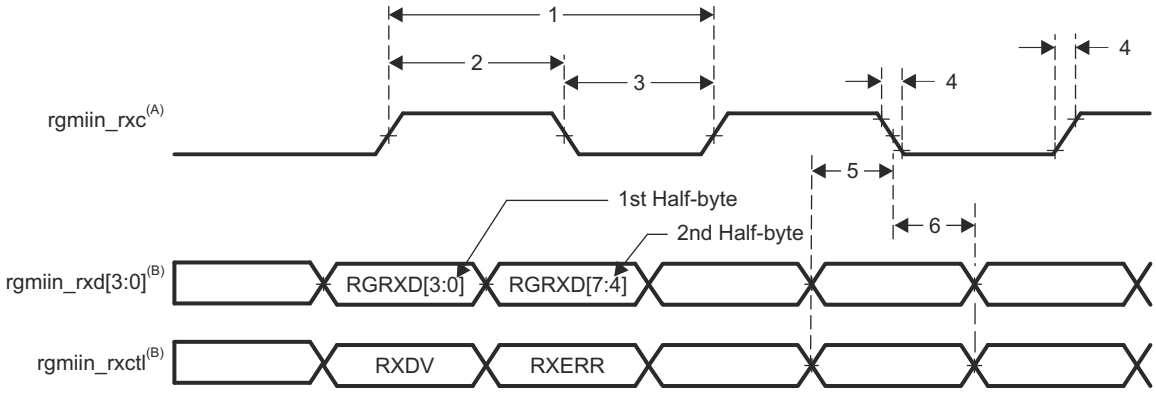
6.12.3.5 RGMII Receive Data and Control Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
5	$t_{su(RXD-RXCH)}$	Setup time, receive selected signals valid before MSS_RGMII_RCLK high/low	1		ns
6	$t_{h(RXCH-RXD)}$	Hold time, receive selected signals valid after MSS_RGMII_RCLK high/low	1		ns



A. rgmiin_rxc must be externally delayed relative to the data and control pins.

B. Data and control information is received using both edges of the clocks. MSS_RGMII_RXD[3:0] carries data bits 3-0 on the rising edge of rgmiin_rxc and data bits 7-4 on the falling edge ofrgmiin_rxc. Similarly, rgmiin_rxctl carries RXDV on rising edge of rgmiin_rxc and RXERR on falling edge of rgmiin_rxc.

Figure 6-13. MAC Receive Interface Timing, RGMIIn operation

6.12.3.6 RMII Transmit Clock Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII7	$t_{c(REF_CLK)}$	Cycle time, REF_CLK	20		ns
RMII8	$t_{w(REF_CLKH)}$	Pulse duration, REF_CLK high	7	13	ns
RMII9	$t_{w(REF_CLKL)}$	Pulse duration, REF_CLK low	7	13	ns
RMII10	$t_{t(REF_CLK)}$	Transition time, REF_CLK		3	ns

6.12.3.7 RMII Transmit Data and Control Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII11	$t_{d(REF_CLK-TXD)}$	Delay time, REF_CLK high to selected transmit signals valid	2	14.2	ns
	$t_{dd(REF_CLK-TXEN)}$				

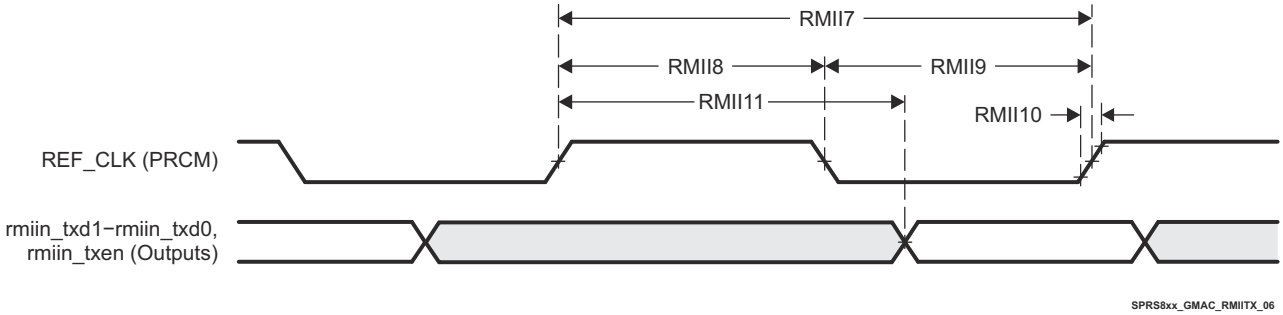


Figure 6-14. MAC Transmit Interface Timing, RMIIn Operation

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6.12.3.8 RMII Receive Clock Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII1	$t_{c(REF_CLK)}$	Cycle time, REF_CLK	20		ns
RMII2	$t_{w(REF_CLKH)}$	Pulse duration, REF_CLK high	7	13	ns
RMII3	$t_{w(REF_CLKL)}$	Pulse duration, REF_CLK low	7	13	ns
RMII4	$t_{tt(REF_CLK)}$	Transition time, REF_CLK		3	ns

6.12.3.9 RMII Receive Data and Control Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII5	$t_{su(RXD-REF_CLK)}$	Setup time, receive selected signals valid before REF_CLK	4		ns
	$t_{su(CRS_DV-REF_CLK)}$				
	$t_{su(RX_ER-REF_CLK)}$				
RMII6	$t_{h(REF_CLK-RXD)}$	Hold time, receive selected signals valid after REF_CLK	2		ns
	$t_{h(REF_CLK-CRS_DV)}$				
	$t_{h(REF_CLK-RX_ER)}$				

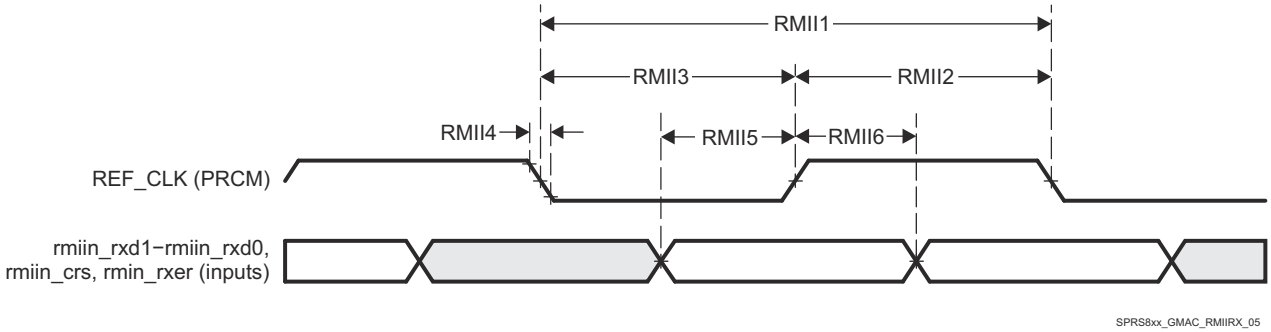

Figure 6-15. MAC Receive Interface Timing, RMIIn operation

6.12.3.10 MII Transmit Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{d(TX_CLK-TXD)}$	Delay time, miin_txclk to transmit selected signals valid	0	25	ns
	$t_{d(TX_CLK-TX_EN)}$				
	$t_{d(TX_CLK-TX_ER)}$				

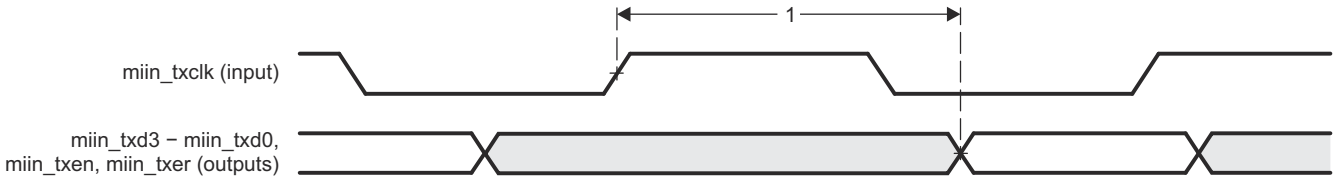

Figure 6-16. MAC Transmit Interface Timing, MIIn operation

6.12.3.11 MII Receive Clock Timing Requirements

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(RX_CLK)}$	Cycle time, miin_rxclk	10 Mbps	400		ns
			100 Mbps	40		ns
2	$t_{w(RX_CLKH)}$	Pulse duration, miin_rxclk high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns

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NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
3	$t_{w(RX_CLKL)}$	Pulse duration, miin_rxclk low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
4	$t_{t(RX_CLK)}$	Transition time, miin_rxclk	10 Mbps		3	ns
			100 Mbps		3	ns

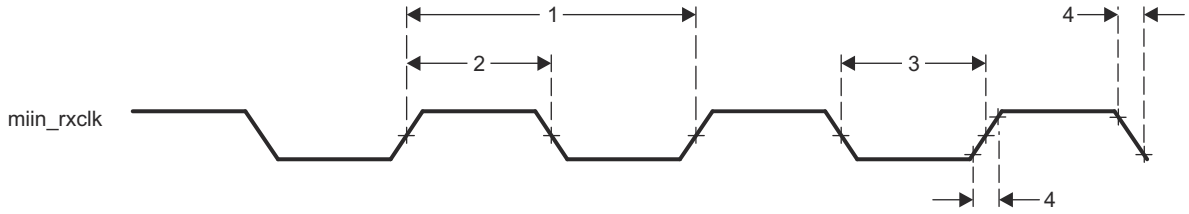

Figure 6-17. Clock Timing (MAC Receive) - MIIn operation

6.12.3.12 MII Receive Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{su(RXD-RX_CLK)}$	Setup time, receive selected signals valid before miin_rxclk	8		ns
	$t_{su(RX_DV-RX_CLK)}$				
	$t_{su(RX_ER-RX_CLK)}$				
2	$t_{h(RX_CLK-RXD)}$	Hold time, receive selected signals valid after miin_rxclk	8		ns
	$t_{h(RX_CLK-RX_DV)}$				
	$t_{h(RX_CLK-RX_ER)}$				

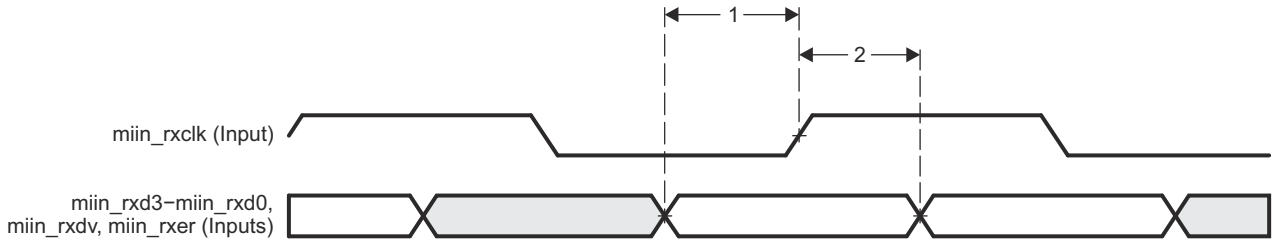

Figure 6-18. MAC Receive Interface Timing, MIIn operation

6.12.3.13 MII Transmit Clock Timing Requirements

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(TX_CLK)}$	Cycle time, miin_txclk	10 Mbps	400		ns
			100 Mbps	40		ns
2	$t_{w(TX_CLKH)}$	Pulse duration, miin_txclk high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
3	$t_{w(TX_CLKL)}$	Pulse duration, miin_txclk low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
4	$t_{t(TX_CLK)}$	Transition time, miin_txclk	10 Mbps		3	ns
			100 Mbps		3	ns

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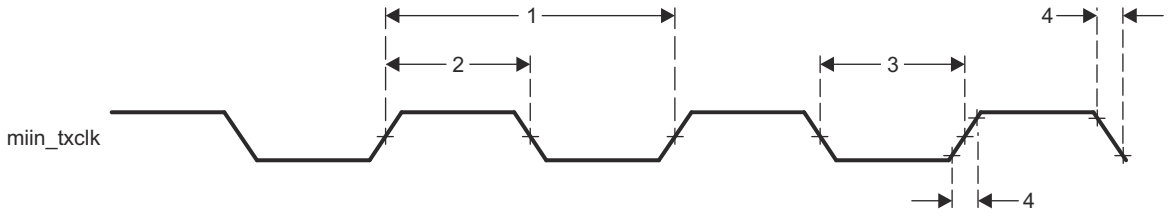

Figure 6-19. Clock Timing (MAC Transmit) - MIIn operation

6.12.3.14 MDIO Interface Timings

> **CAUTION**
>
> The IO Timings provided in this section are only valid for some MAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 6-7, Table 6-8 and Figure 6-20 present switching characteristics and timing requirements for the MDIO interface.

Table 6-7. Timing Requirements for MDIO Input

No	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO1	$t_{c(MDC)}$	Cycle time, MDC	400		ns
MDIO2	$t_{w(MDCH)}$	Pulse Duration, MDC High	160		ns
MDIO3	$t_{w(MDCL)}$	Pulse Duration, MDC Low	160		ns
MDIO4	$t_{su(MDIO-MDC)}$	Setup time, MDIO valid before MDC High	90		ns
MDIO5	$t_{h(MDIO_MDC)}$	Hold time, MDIO valid from MDC High	0		ns

Table 6-8. Switching Characteristics Over Recommended Operating Conditions for MDIO Output

NO	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO6	$t_{t(MDC)}$	Transition time, MDC		5	ns
MDIO7	$t_{d(MDC-MDIO)}$	Delay time, MDC low to MDIO valid	10	(P * 0.5) - 10	ns

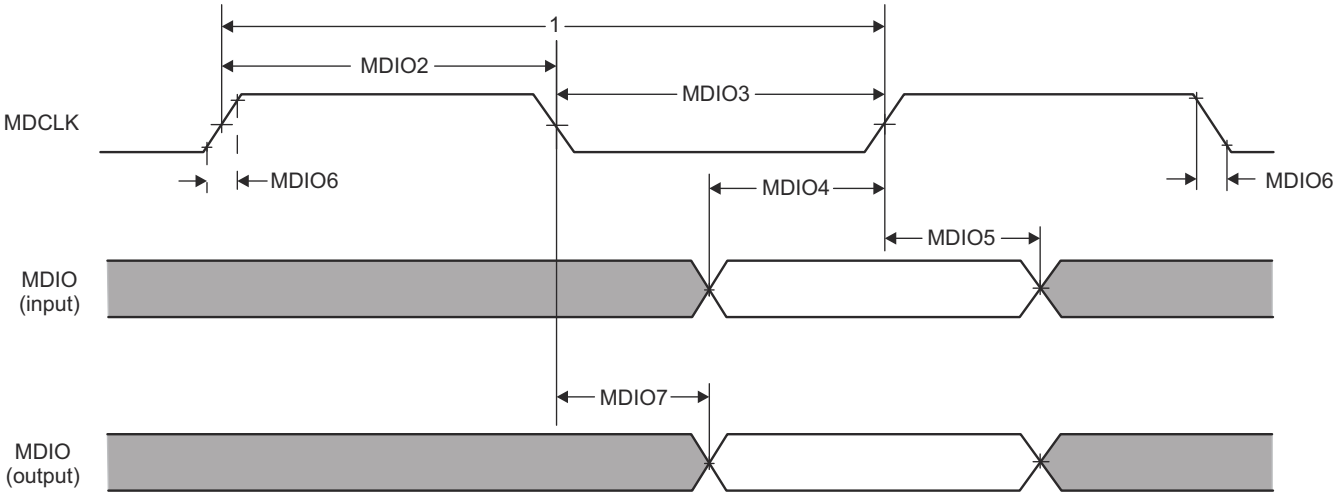

Figure 6-20. MAC MDIO diagrams

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6.12.4 LVDS/Aurora Instrumentation and Measurement Peripheral

The device supports a set of LVDS interfaces in two different modes.

- Legacy LVDS mode
- STM-TWP Aurora interface

The LVDS IO are shared between the above two measurement interface options.

Following features are supported :

- 2-data lane LVDS interface (two additional lanes for Data Clock and Frame Clock)
- 4-Lane STM-TWP-Aurora-LVDS interface mode. It has the following features:
  - Configurable 4/2/1 lane of operation.
  - Transmit data compliant to Aurora 8B/10B Serial Simplex Operation
  - Transmit data compliant to Aurora 64B/66B Serial Simplex Operation

Please see the device TRM for information regarding programming options for both LVDS interfaces.

6.12.4.1 LVDS Interface Configuration

The supported LVDS lane configuration is 2-data lane (LVDS_TXP/M), one Bit Clock lane (LVDS__TXxx_CLKP/M) and one Frame clock lane (LVDS_TXxx_FRCLKP/M). The LVDS interface supports programmable data rates with the maximum being 900 Mbps (450 MHz DDR Clock).

Note that the bit clock is in DDR format and hence the number of toggles in the clock is equivalent to data.

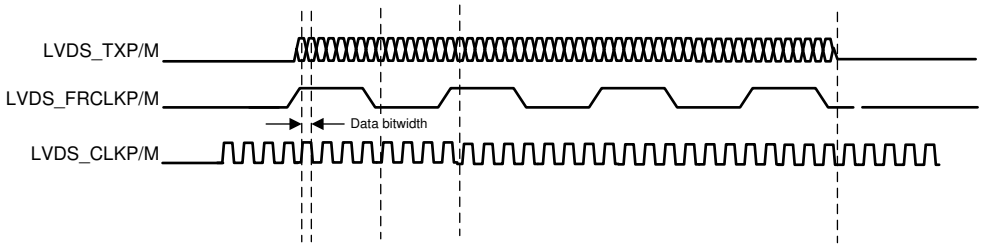

Figure 6-21. LVDS Interface Lane Configuration And Relative Timings

6.12.4.2 LVDS Interface Timings

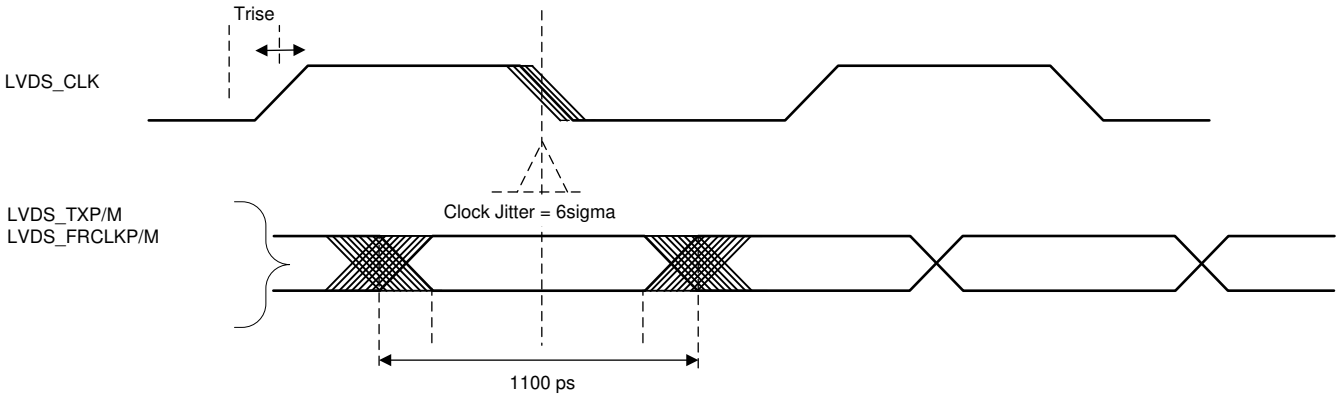

Figure 6-22. Timing Parameters

Table 6-9. LVDS Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty Cycle Requirements	max 1 pF lumped capacitive load on LVDS lanes	48%		52%	
Output Differential Voltage	peak-to-peak single-ended with 100 Ω resistive load between differential pairs	250		450	mV

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Table 6-9. LVDS Electrical Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Offset Voltage		1125		1275	mV
Trise and Tfall	20%-80%, 900 Mbps		330		ps
Jitter (pk-pk)	900 Mbps		80		ps

6.12.5 UART Peripheral

The device includes four UART interfaces. One UART is intended as a secondary boot loader source, one is intended for use as a register debug interface (with XDS110 emulator) and the remaining two are meant for general UART communication support.

- Maximum baud-rate supported shall be at least 1536K baud in all the different clock frequency modes
- UART interfaces multiplexed with other I/O to allow for widest peripheral use flexibility

6.12.5.1 SCI Timing Requirements

		MIN	TYP	MAX	UNIT
f(baud)	Supported baud rate at 20 pF		921.6		kHz

6.12.6 Inter-Integrated Circuit Interface (I2C)

The device supports one Controller/Target Inter-integrated Circuit interface and is intended to be connected to an external PMIC or EEPROM device (alternative control SPI).

The I2C has the following features:

- Standard/fast mode I2C interface compliant with Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - General call
  - START byte
  - Multi-controller transmitter/ target receiver mode
  - Multi-controller receiver/ target transmitter mode
  - Combined controller transmit/receive and receive/transmit mode
  - Transfer rates of 100 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

Note

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the target address second byte every time it sends the target address first byte)

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6.12.6.1 I2C Timing Requirements (1)

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high	250		100		µs
$t_{h(SCLL-SDA)}$(1)	Hold time, SDA valid after SCL low	0	3.45	0	0.9	µs
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
C_b (2) (3)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum th(SDA-SCLL) for I2C bus devices has only to be met if the device does not stretch the low period (tw(SCLL)) of the SCL signal.
(3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

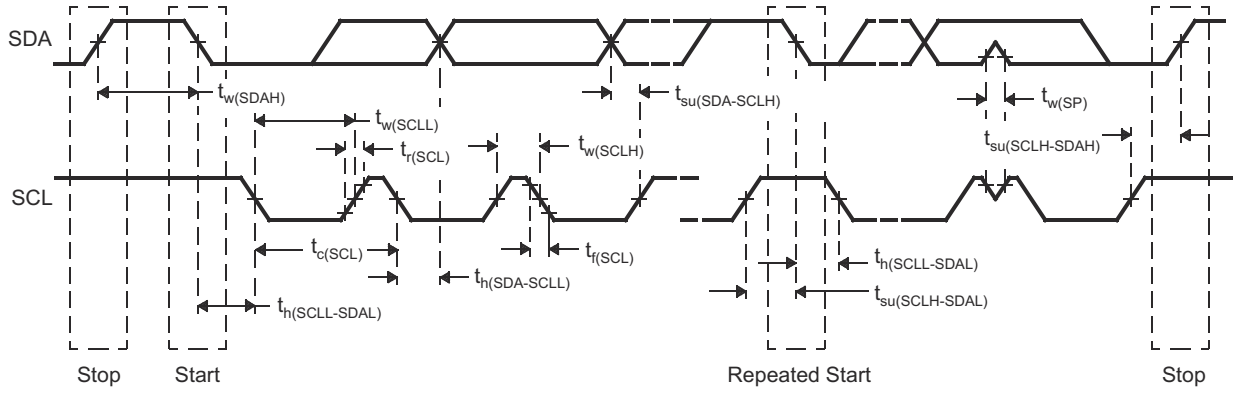

Figure 6-23. I2C Timing Diagram

Note

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum th(SDA-SCLL) has only to be met if the device does not stretch the LOW period (tw(SCLL)) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.

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6.12.7 Controller Area Network - Flexible Data-rate (CAN-FD)

The device integrates two CAN-FD interfaces, MSS_MCANA and MSS_MCANB. This enables support of a typical use case where one CAN-FD interface is used as ECU network interface while the other interface is used as a local network interface, providing communication with the neighboring sensors.

- Support CAN-FD according to ISO 11898-7 protocol with data rate up to 8Mbps
- Multiplexed GPIO can be used for CAN-FD external driver control
- AWRx synchronous trigger output allows CAN-FD to trigger radar frames

6.12.7.1 Dynamic Characteristics for the CAN-FD TX and RX Pins

PARAMETER[1]		MIN	TYP	MAX	UNIT
$t_{d(MSS_CANA_TX)}$	Delay time, transmit shift register to MSS_CANA_TX pin			15	ns
$t_{d(MSS_CANB_TX)}$	Delay time, transmit shift register to MSS_CANB_TX pin			15	ns
$t_{d(MSS_MCANA_RX)}$	Delay time, MSS_MCANA_RX pin to receive shift register			10	ns
$t_{d(MSS_MCANB_RX)}$	Delay time, MSS_MCANB_RX pin to receive shift register			10	ns

(1) These values do not include rise/fall times of the output buffer.

6.12.8 CSI2 Receiver Peripheral

The device integrates one 3-lane MIPI CSI2, D-PHY receiver peripheral in the Radio processing subsystem. The CSI2 interface is primarily functional of operating as a hardware-in-the-loop (HIL) interface, allowing for the playback of recorded radar data for development purposes.

- Interface is compliant with the MIPI CSI-2 D-PHY standard revision 1.2
- 1 x 3-lane (2 data lanes, 1 clock lane) CSI2 receiver interface, working simultaneously at 600 Mbps/lane
- 2-lane, or 1-lane CSI2 configurations
- Support for 4 simultaneous virtual channels and data types
- Support for 8/10/12/14/16-bit RAW data mode with capability of sign extension or zero padding to align with 16-bit memory addressing for RAW 10/12/14 modes
- Support for user defined data types

Please refer to the device Technical Reference Manual for a complete description of all the programmable options.

6.12.8.1 CSI2 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Low Power Receiver (LP-RX)					
V_{IL} [1]	Logic 0 input threshold			550	mV
V_{IH} [2]	Logic 1 input threshold	880			mV
V_{HYST}	Input Hysteresis	25			mV
High Speed Receiver (HS-RX)					
V_{IDTH}	Differential input high threshold	70			mV
V_{IDTL}	Differential input low threshold			-70	mV
V_{IDMAX}	Maximum differential input voltage			270	mV
V_{ILHS}	Single-ended input low voltage	-40			mV
V_{IHHS}	Single-ended input high voltage			460	mV
V_{CMRXDC}	Common-mode voltage	70		330	mV
$\Delta_{VCMRX(HF)}$	Common-mode interference beyond 450 MHz			200	mVPP
$\Delta_{VCMRX(LF)}$	Common mode interference 50MHz – 450MHz	-50		50	mVPP

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
HS DATA-CLOCK Timing Specification (3) (5)					
UI_{INST}	Data/Clock Unit Interval	1.11			ns
T_{SETUP}	Data to Clock setup time	166			ps
T_{HOLD}	Clock to Data hold time	166			ps
$T_{R,}$, T_F (4)	Rise/Fall Times	166		0.4*UI_{INST}	ps

(1) The input low-level voltage, VIL, is the voltage at which the receiver is required to detect a low state in the input signal. VIL is larger than the maximum single-ended line voltage during HS transmission. Therefore, both LP receivers will detect low during HS signaling
(2) The input high-level voltage, VIH, is the voltage at which the receiver is required to detect a high state in the input signal.
(3) TSKEW in the figure is the skew between the clock and data HS signals that can be tolerated at the receiver input. It is only a descriptive parameter. Rx timing is specified by TSETUP/THOLD only.
(4) Rise/Fall from V_{IDTL} to V_{IDTH}.
(5) Setup/hold specification is assuming identical common mode and rise/fall time for both data and clock lane at receiver input. i.e. V_{CMRXDC} and T_R, T_F must be same for clock lane and data lane while measuring T_{SETUP} and T_{HOLD}

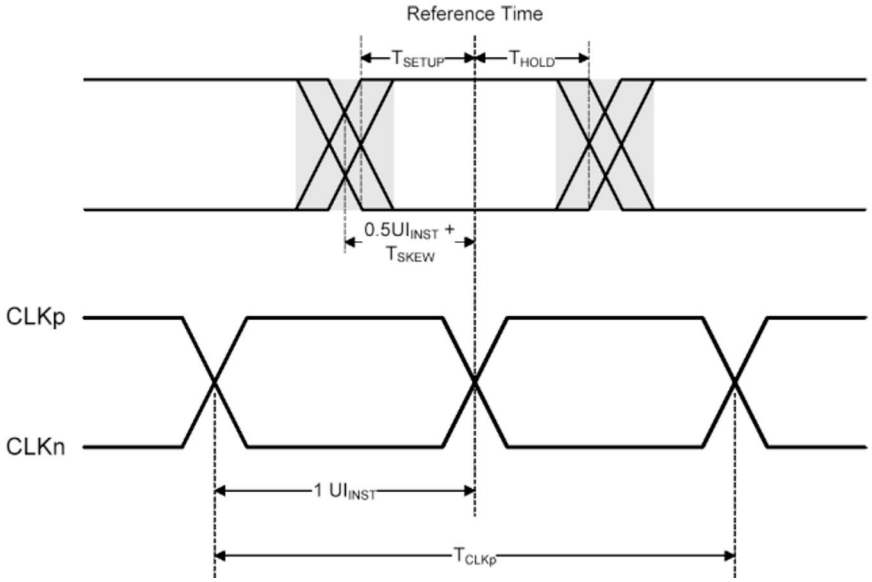

Figure 6-24. Clock and Data Timing in HS Transmission

6.12.9 Enhanced Pulse-Width Modulator (ePWM)

The device includes three Enhanced Pulse-Width Modulation (ePWM) modules. These modules can be used to generate duty-cycled controlled waveforms for a power regulator, or a power management systems, or more complex waveforms for motor control applications.

The module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control for each PWM module
- Each module contains two PWM outputs (EPWMxA and EPWMxB) that shall be usable in the following configurations:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation

6.12.10 General-Purpose Input/Output

Section 6.12.10.1 lists the switching characteristics of output timing relative to load capacitance.

6.12.10.1 Switching Characteristics for Output Timing versus Load Capacitance (C_L) (1) (2)

PARAMETER		TEST CONDITIONS		VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t_r	Max rise time	Slew control = 0	C_L = 20 pF	2.8	3.0	ns
			C_L = 50 pF	6.4	6.9	
			C_L = 75 pF	9.4	10.2	
t_f	Max fall time		C_L = 20 pF	2.8	2.8	ns
			C_L = 50 pF	6.4	6.6	
			C_L = 75 pF	9.4	9.8	
t_r	Max rise time	Slew control = 1	C_L = 20 pF	3.3	3.3	ns
			C_L = 50 pF	6.7	7.2	
			C_L = 75 pF	9.6	10.5	
t_f	Max fall time		C_L = 20 pF	3.1	3.1	ns
			C_L = 50 pF	6.6	6.6	
			C_L = 75 pF	9.6	9.6	

(1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

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6.13 Emulation and Debug

6.13.1 Emulation and Debug Description

6.13.2 JTAG Interface

The JTAG interface implements the IEEE1149.1 standard interface for processor debug and boundary scan testing.

Section 6.13.2.1 and Section 6.13.2.2 assume the operating conditions stated in Figure 6-25.

6.13.2.1 Timing Requirements for IEEE 1149.1 JTAG

Table 6-10. JTAG Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

Table 6-11. JTAG Timing Requirements

NO.			MIN	TYP	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time TCK	33.33			ns
1a	$t_{w(TCKH)}$	Pulse duration TCK high (40% of tc)	13.33			ns
1b	$t_{w(TCKL)}$	Pulse duration TCK low (40% of tc)	13.33			ns
3	$t_{su(TDI-TCK)}$	Input setup time TDI valid to TCK high	2.5			ns
3	$t_{su(TMS-TCK)}$	Input setup time TMS valid to TCK high	2.5			ns
4	$t_{h(TCK-TDI)}$	Input hold time TDI valid from TCK high	18			ns
4	$t_{h(TCK-TMS)}$	Input hold time TMS valid from TCK high	18			ns

6.13.2.2 Switching Characteristics for IEEE 1149.1 JTAG

NO.	PARAMETER		MIN	TYP	MAX	UNIT
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0		21	ns

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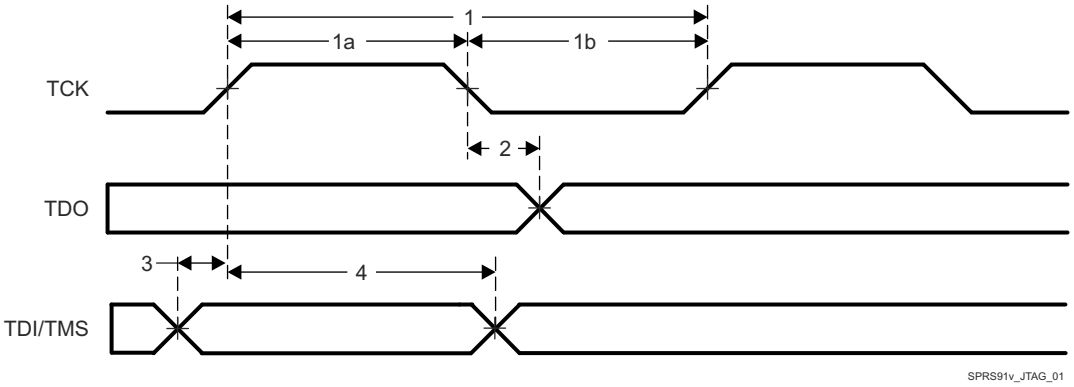

Figure 6-25. JTAG Timing

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6.13.3 ETM Trace Interface

The ETM Trace interface provides a means of exporting real time processor debug information to a host PC through a compatible emulator toolset.

Section 6.13.3.1 and Section 6.13.3.2 describe the operating conditions shown in Figure 6-26 and Figure 6-27.

6.13.3.1 ETM TRACE Timing Requirements

		MIN	TYP	MAX	UNIT
Output Conditions					
C_{LOAD}	Output load capacitance	2		20	pF

6.13.3.2 ETM TRACE Switching Characteristics

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{cyc(ETM)}$	Cycle time, TRACECLK period	16			ns
2	$t_{h(ETM)}$	Pulse Duration, TRACECLK High	7			ns
3	$t_{l(ETM)}$	Pulse Duration, TRACECLK Low	7			ns
4	$t_{r(ETM)}$	Clock and data rise time			3.3	ns
5	$t_{f(ETM)}$	Clock and data fall time			3.3	ns
6	$t_{d(ETMTRACECLKH-ETMDATAV)}$	Delay time, ETM trace clock high to ETM data valid	1		14.5	ns
7	$t_{d(ETMTRACECLKl-ETMDATAV)}$	Delay time, ETM trace clock low to ETM data valid	1		14.5	ns

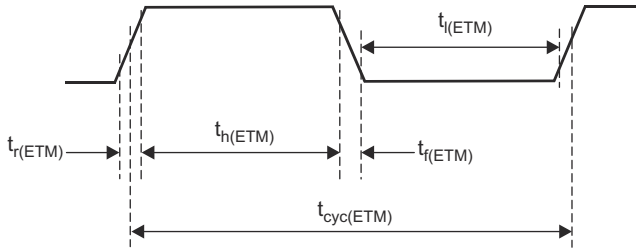


Figure 6-26. ETMTRACECLKOUT Timing

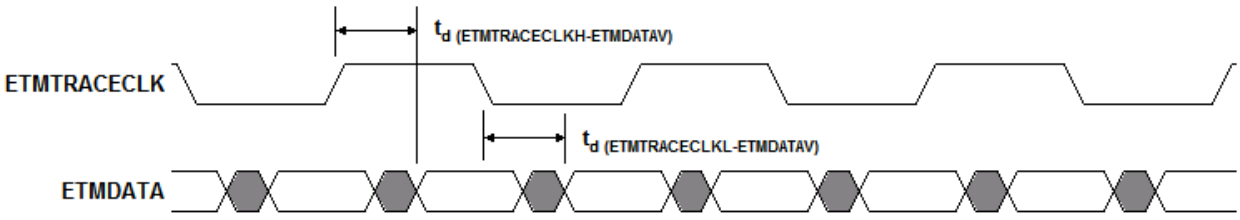


Figure 6-27. ETMDATA Timing

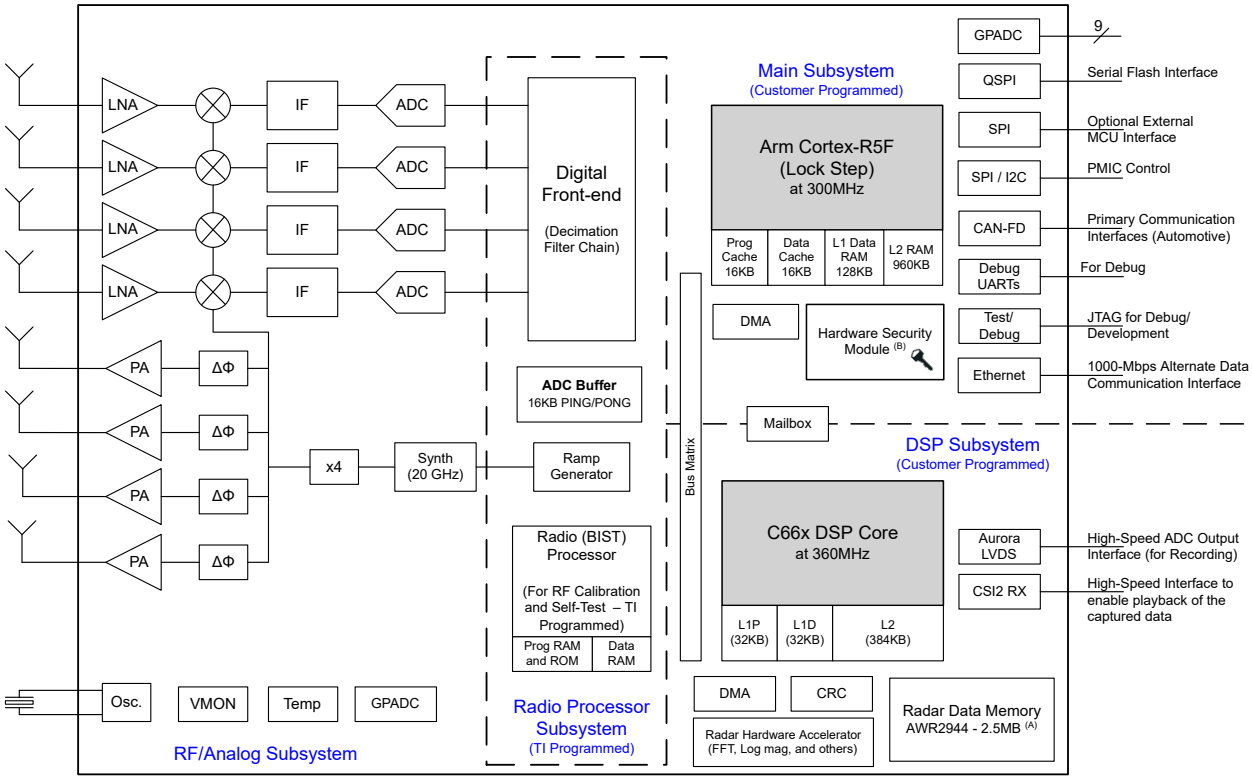
7 Detailed Description

7.1 Overview

The AWR294x device includes the entire Millimeter Wave blocks, and analog baseband signal chain, for three or four transmitters and four receivers, as well as a customer-programmable MCU and DSP. This device is applicable as a radar-on-a-chip in use-cases with modest requirements for memory, processing capacity, and application code size. These can be cost-sensitive automotive applications that are evolving from 24 GHz narrowband implementation and some emerging, ultra-short-range radar applications.

7.2 Functional Block Diagram

Figure 7-1 represents the functional block diagram for the device.



A. Configurable memory can be switched from Radar Data memory to the Main Cortex-R5F program and Data RAMs per application usecase needs.

B. This feature is only available in select part variants as indicated by the Device Type identifier in the Section 3, Device Information table.

Figure 7-1. Functional Block Diagram

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7.3 Subsystems

7.3.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The four transmit and the receive channels can all be operated simultaneously for transmit beamforming purpose and receiving data as required.

7.3.1.1 RF Clock Subsystem

The device clock subsystem generates 76 to 81 GHz from an input reference of 40 MHz crystal. It has a built-in oscillator circuit followed by an Analog PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an x4 multiplier to create the required frequency in the 76 to 81 GHz spectrum. The RF synthesizer output can be modulated by the timing engine block to create the required waveforms for effective sensor operation or it can input a fixed signal of 1GHz directly from APLL.

The Analog PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

Figure 7-2 describes the clock subsystem.

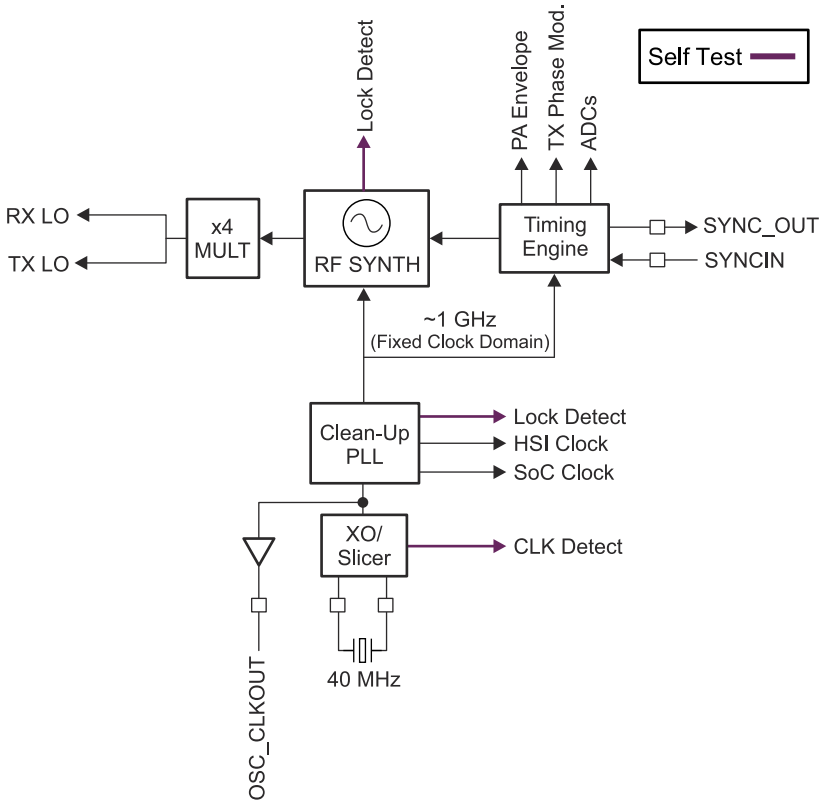

Figure 7-2. RF Clock Subsystem

7.3.1.2 Transmit Subsystem

The device transmit subsystem consists of four parallel transmit chains, each with independent phase and amplitude control. All four transmitters can be used simultaneously or in time-multiplexed fashion. The device supports binary phase modulation and a 6 bit programmable phase shifter for beamforming control on a per chirp basis for each channel as indicated in the figure below.

Each transmit chain can deliver a typical value of 13.5dBm at BGA ball of the package. The transmit chains also support programmable backoff for system optimization.

Figure 7-3 describes the transmit subsystem.

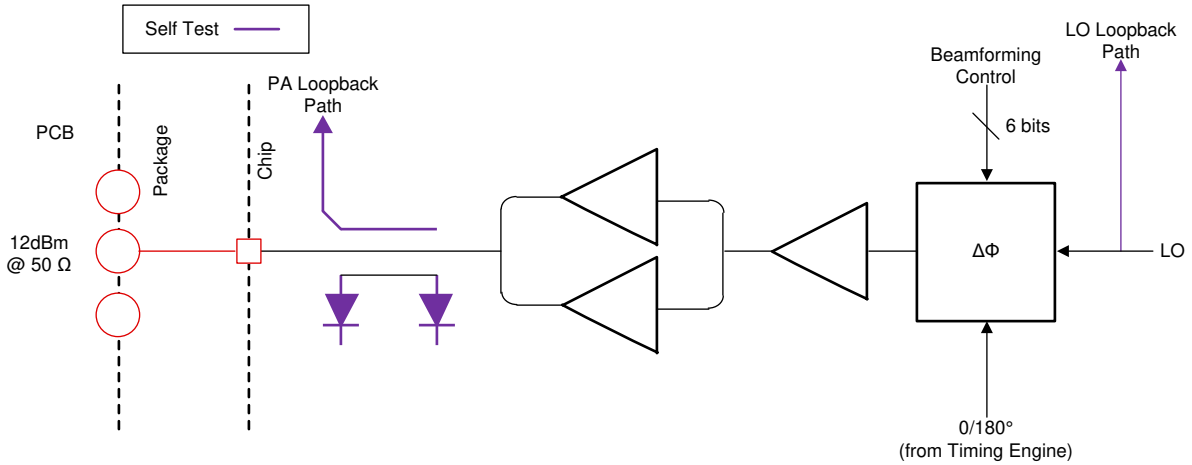

Figure 7-3. Transmit Subsystem (Per Channel)

7.3.1.3 Receive Subsystem

The device Receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, ADC conversion, and decimation. All four receive channels can be operational at the same time. An individual power-down option is also available for system optimization.

The device supports a real-only receiver. The band-pass IF chain has configurable cutoff frequencies above 300 kHz and can support bandwidths up to 15 MHz.

Figure 7-4 describes the receive subsystem.

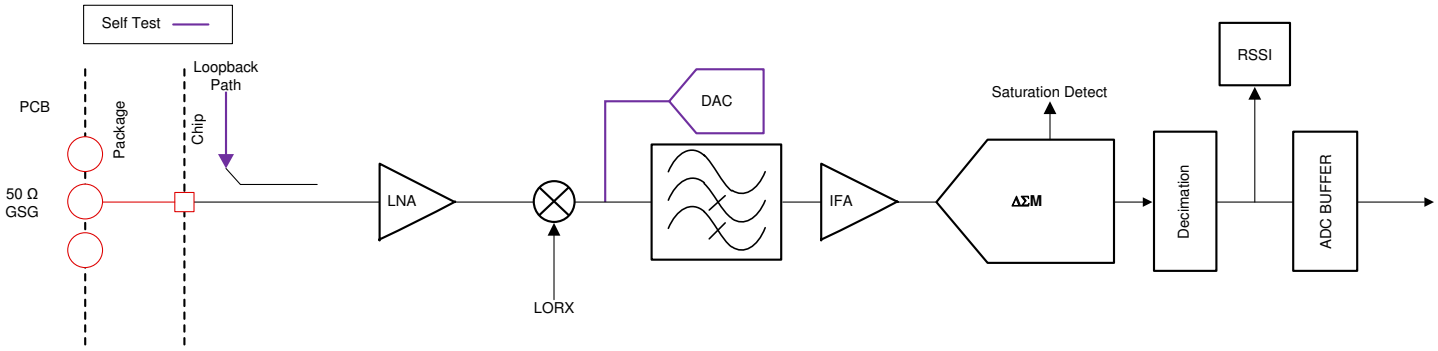

Figure 7-4. Receive Subsystem (Per Channel)

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7.3.2 Processor Subsystem

Figure 7-5 shows the block diagram for customer programmable processor subsystems in the device. At a high level there are two customer programmable subsystems. Left hand side shows the DSP Subsystem which contains TI's high performance C66x DSP, HWA 2.1, a high-bandwidth interconnect for high performance (128-bit, 150MHz), and associated peripherals – six EDMAs for data transfer,Aurora and LVDS interface for Measurement data output, L3 Radar data cube memory, ADC buffers, CRC engine, and data handshake memory (additional memory provided on interconnect).

For more information, see the TMS320C66x DSP CorePac User Guide

The right side of the diagram shows the Main subsystem (MSS). The Main subsystem, as the name suggests, is the primary controller of the device and controls all the device peripherals and house-keeping activities of the device. The Main subsystem contains a Cortex-R5F (MSS R5F) processor and associated peripherals and housekeeping components such as EDMAs, CRC, and peripherals (I^2C, UART, SPIs, CAN-FD, EPWM, and others) connected to the primary interconnect through the Peripheral Central Resource (PCR interconnect).

The Radio Processing Subsystem or the BIST Subsystem (RSS) is responsible for initializing and calibrating the Analog/RF modules. RSS periodically monitors the Analog/RF functionality such that all the Analog/RF modules work in their defined limits.

General-Purpose ADC (GPADC), Fast Fourier Transformation engine (FFT engine) and other modules are provided to monitor the signal from different points in the transmitter and receiver chains. Digital front-end filters (DFE), Ramp Generation module and Analog/DFE registers, which are mainly under the control of BSS, can be indirectly controlled through the API calls from the Main Subsystem.

The device also integrates one two-lane CSI2 receiver interfaces in the radio processing subsystem. The prime functionality of this interface is the Hardware in loop (HIL) functionality, that can be used to perform the radar operations feeding the captured data from outside into the device without involving the RF subsystem.

Refer to the Device TRM (Technical Reference Manual) for MSS Cortex-R5F and DSP C66x memory map.

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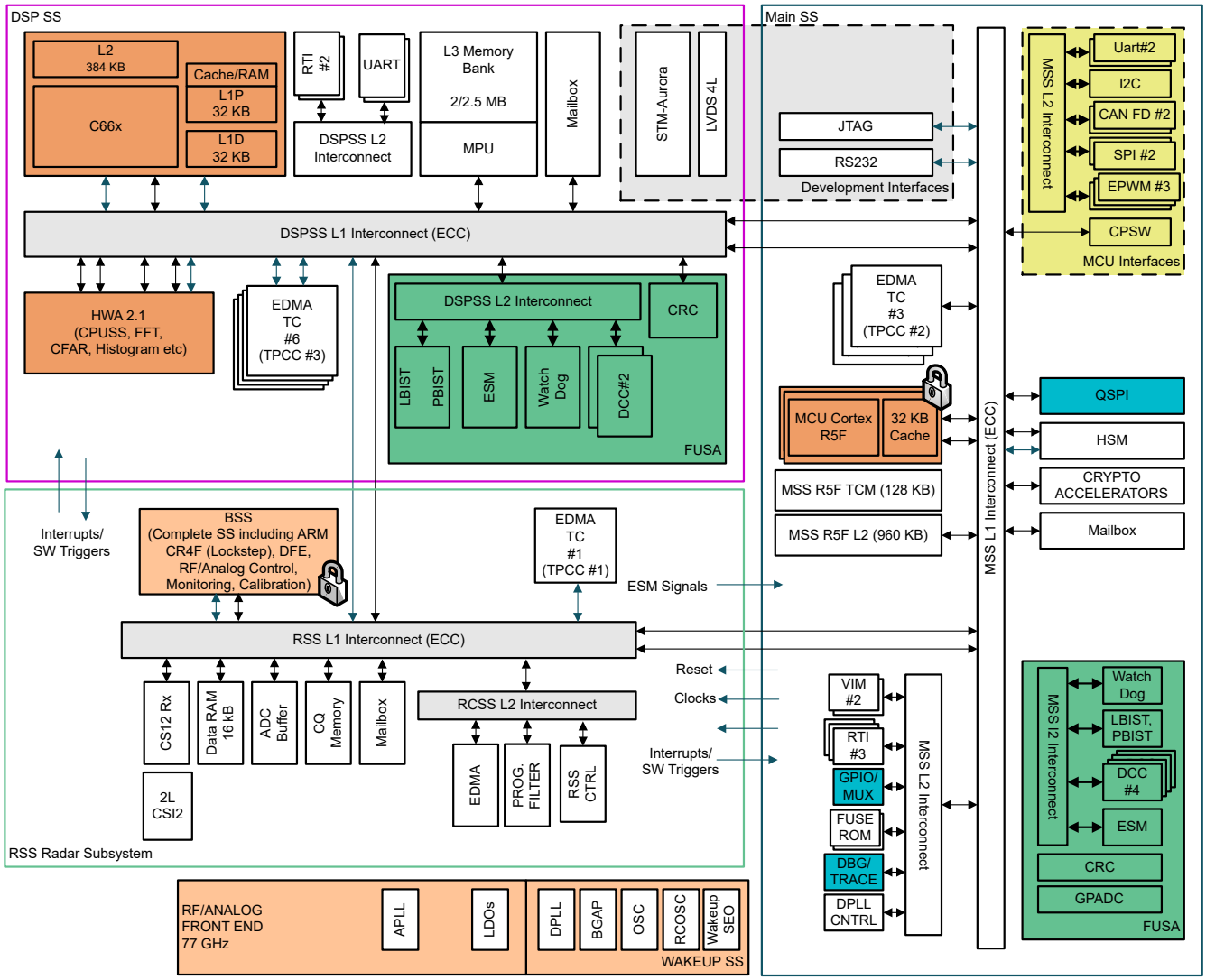

Figure 7-5. Processor subsystem

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7.3.3 Automotive Interfaces

The device communicates with the automotive network over the following main interfaces:

- CAN-FD
- Ethernet

7.4 Other Subsystems

7.4.1 Hardware Accelerator Subsystem

In addition to the DSP core, the device incorporates Radar Hardware Accelerators (HWA2.1) to offload the DSP from pre-processing computations.

To understand the capabilities offered by the Radar Hardware Accelerator 2.1 so as to achieve the desired functionality, please refer to the Hardware Accelerator 2.1 section in the Device Technical reference Manual.

7.4.2 Security – Hardware Security Module

A Hardware Security Module (HSM), which performs a secure zone operation, is provisioned in the device (*operational only in select part variants*). A programmable Arm Cortex-M4 core is available to implement the crypto-agility requirements.

The cryptographic algorithms can be accelerated using the hardware modules in the HSM. Functions include acceleration of AES, SHA, and public key accelerator (PKA) to perform math operations for asymmetric key cryptographic requirements and true random number generation.

The Main subsystem (MSS) Cortex-R5F processor interfaces with the HSM subsystem to perform the cryptographic operations required for the secure boot and secure runtime communications.

Further details on Security can be found in the concerned collaterals. Please reach out to your local TI sales representative for more information.

7.4.3 ADC Channels (Service) for User Application

The device includes provision for an ADC service for user application, where the GPADC engine present inside the device can be used to measure up to nine external and internal voltages. The ADC1, ADC2, ADC3, ADC4, ADC5, ADC6, ADC7, ADC8 and ADC9 pins are used for this purpose.

Note

GPADC structures are also used for measuring the output of internal temperature sensors.

GPADC Specifications:

- 625 Ksps SAR ADC
- 0 to 1.8V input range
- 10-bit resolution

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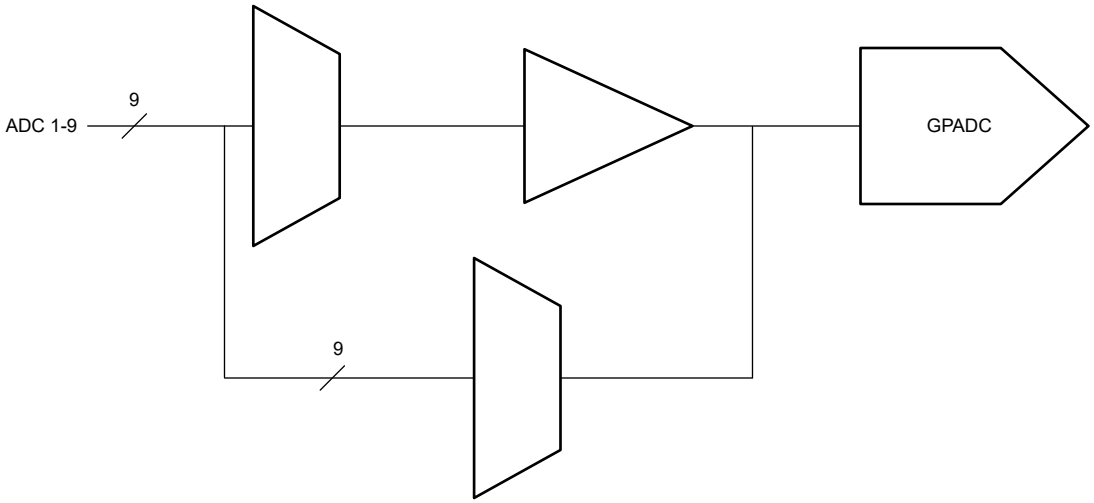

Table 7-1. GP-ADC Parameter

PARAMETER	TYP	UNIT
ADC supply	1.8	V
ADC unbuffered input voltage range	0 – 1.8	V
ADC buffered input voltage range(1)	0.4 – 1.3	V
ADC resolution	10	bits
ADC offset error	±5	LSB
ADC gain error	±5	LSB
ADC DNL	–1/+2.5	LSB
ADC INL	±2.5	LSB
ADC sample rate	625	Ksps
ADC sampling time	400	ns
ADC internal cap	10	pF
ADC buffer input capacitance	2	pF
ADC input leakage current	3	uA

(1) Outside of given range, the buffer output will become nonlinear.

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8 Monitoring and Diagnostics

8.1 Monitoring and Diagnostic Mechanisms

Table 8-1 is a list of the main monitoring and diagnostic mechanisms available in the device.

Table 8-1. Monitoring and Diagnostic Mechanisms for AWR294x

NO	FEATURE	DESCRIPTION
		MAIN SUBSYSTEM
1	Lockstep operation of MSS R5F Core	Device architecture supports lockstep operation of the MSS R5F core that is the operating core in the Main subsystem that is provisioned as the safety island in the device.
2	Boot time LBIST For MSS R5F Core and associated VIM	Device architecture supports hardware logic BIST (LBIST) engine self-test Controller (STC). This logic is used to provide a very high diagnostic coverage (>90%) on the MSS R5F CPU core and Vectored Interrupt Module (VIM) at a transistor level. LBIST for the CPU and VIM need to be triggered by application code before starting the functional safety application. A reset of the CPU is initiated at the end of the STC operation and the reset cause register captures the status of reset. The STC registers can then be read out to identify the status of the STC execution to determine if there were any errors. CPU stays there in while loop and does not proceed further if a fault is identified. There can be a fault injection test also performed which leads to a reset of the CPU with the error status signaled in the STC registers.
3	Boot time PBIST for MSS R5F Memories	MSS R5F has tightly coupled memories (TCM) Level 1 (L1) memories TCMA, TCMB0 and TCMB1 as well as the level 2 (L2) memories. Device architecture supports a hardware programmable memory BIST (PBIST) engine. This logic is used to provide a very high diagnostic coverage (March-13n) on the implemented MSS R5F TCMs at a transistor level. PBIST for L1 and L2 memories is triggered by the bootloader at the boot time before starting download of application from flash or a peripheral interface. The CPU is in a while loop and does not proceed further if a fault is identified.
4	End to End ECC for MSS R5F Memories	The TCMs and L2 memory diagnostic support a single error correction, double error detection (SECDED) ECC diagnostic. For L2 memory, an 8-bit code word is used to store the ECC data as calculated over the 64-bit data bus. For TCMs, a 7-bit code word is used to store the ECC data for a 32-bit data bus. ECC evaluation for TCMs is done by the ECC control logic inside the CPU. This scheme provides end-to-end diagnostics on the transmissions between CPU and TCM. CPU can be configured to have predetermined response (ignore or abort generation) to single and double bit error conditions.
5	MSS R5F bit multiplexing	Logical TCM and L2 memory word and the associated ECC code is split and stored in two physical SRAM banks. This scheme provides an inherent diagnostic mechanism for address decode failures in the physical SRAM banks. Faults in the bank addressing are detected by the CPU as an ECC fault. Further, bit multiplexing scheme is implemented such that the bits accessed to generate a logical (CPU) word are not physically adjacent. This scheme helps to reduce the probability of physical multi-bit faults resulting in logical multi-bit faults; rather the faults manifest as multiple single bit faults. As the SECDED TCM ECC can correct a single bit fault in a logical word, this scheme improves the usefulness of the TCM ECC diagnostic. Both these features are hardware features and cannot be enabled or disabled by application software.
6	Clock Monitor	Device architecture supports four digital clock comparators (EDCCs) and an internal RCOSC. Dual functionality is provided by these modules – clock detection and clock monitoring. EDCCA is dedicated for ADPLL/APLL lock detection monitoring, comparing the ADPLL/APLL output divided version with the Reference input clock of the device. Failure detection for EDCCA can be programmed to cause the device to go into limp mode. Additionally, there is a provision to feed an external reference clock to monitor the internal clock using the EDCCA. EDCCB, EDCCC, EDCCD module is one which is available for user software. Any two clocks can be compared. One example is to compare the CPU clock with the reference or internal RCOSC clock source. Failure detection is indicated to the MSS R5F CPU through the Error Signaling Module (ESM).

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Table 8-1. Monitoring and Diagnostic Mechanisms for AWR294x (continued)

NO	FEATURE	DESCRIPTION
7	RTI/WDT for MSS R5F	Device architecture supports the use of an internal watchdog that is implemented in the real-time interrupt (RTI) module. The internal watchdog has two modes of operation: digital watchdog (DWD) and digital windowed watchdog (DWWD). The modes of operation are mutually exclusive; the designer can elect to use one mode or the other but not both at the same time. Watchdog can issue either an internal (warm) system reset or a CPU non-mask able interrupt upon detection of a failure. The Watchdog is enabled by the bootloader in DWD mode at boot time to track the boot process. When the application code takes control, the watchdog can be configured again for the mode and timings based on the application requirements.
8	MPU for MSS R5F	The Cortex-R5F CPU includes an MPU. The MPU logic can be used to provide spatial separation of software tasks in the device memory. The Cortex-R5F MPU supports 16 regions. The operating system controls the MPU and changes the MPU settings based on the needs of each task. A violation of a configured memory protection policy results in a CPU abort.
9	PBIST for Peripheral interface SRAMs - SPIs,CANs, Ethernet, EDMA, Mailbox	Device architecture supports a hardware programmable memory BIST (PBIST) engine for Peripheral SRAMs as well. PBIST for peripheral SRAM memories can be triggered by the application. User can elect to run the PBIST on one SRAM or on groups of SRAMs based on the execution time, which can be allocated to the PBIST diagnostic. The PBIST tests are destructive to memory contents, and as such are typically run only at boot time. However, the user has the freedom to initiate the tests at any time if peripheral communication can be hindered. Any fault detected by the PBIST results in an error indicated in PBIST status registers.
10	ECC for Peripheral interface SRAMs – SPIs, CANs, Ethernet, EDMA, Mailbox	Peripheral interface SRAMs diagnostic is supported by Single error correction double error detection (SECDED) ECC diagnostic. When a single or double bit error is detected, the MSS R5F is notified via ESM (Error Signaling Module). This feature is disabled after reset. Software must configure and enable this feature in the peripheral and ESM module. ECC failure (both single bit corrected and double bit uncorrectable error conditions) is reported to the MSS R5F as an interrupt via ESM module.
11	Configuration registers protection for Main SS peripherals	All the Main SS peripherals (SPIs, CANs, Ethernet, I2C, DMAs, RTI/WD, DCCs, EDMA, IOMUX etc.) are connected to interconnect via Peripheral Central resource (PCR). This provides two diagnostic mechanisms that can limit access to peripherals. Peripherals can be clock gated per peripheral chip select in the PCR. This can be utilized to disable unused features such that the features cannot interfere. In addition, each peripheral chip select can be programmed to limit access based on privilege level of transaction. This feature can be used to limit access to entire peripherals to privileged operating system code only. These diagnostic mechanisms are disabled after reset. Software must configure and enable these mechanisms. Protection violation also generates an error that result in abort to MSS R5F or error response to other hosts such as DMAs.
12	Cyclic Redundancy Check–Main SS	Device architecture supports hardware CRC engine on Main SS implementing the below polynomials. • CRC16 CCITT – 0x10 • CRC32 Ethernet – 0x04C11DB7 • CRC64 • CRC 32C – CASTAGNOLI – 0x1EDC6F4 • CRC32P4 – E2E Profile4 – 0xF4ACFB1 The read operation of the SRAM contents to the CRC can be done by CPU or by DMA. The comparison of results, indication of fault, and fault response are the responsibility of the software managing the test.
13	MPU	Device architecture supports MPUs on certain peripheral ports in the Main SS that include L2 Memory, PCR peripheral access, QSPI access, R5F AXI-peripheral access. This allows configuring access permissions to these key regions in the Main SS. By default, this control resides with the HSM.
14	MPU for DMAs	Device architecture supports MPUs on Main SS EDMAs. EDMAs also includes MPUs on both read and writes host ports. EDMA MPUs supports 8 regions. Failure detection by MPU is reported to the core as an interrupt via local ESM.

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Table 8-1. Monitoring and Diagnostic Mechanisms for AWR294x (continued)

NO	FEATURE	DESCRIPTION
15	Interconnect ECC	Device architecture supports hardware based ECC protection mechanisms for transfers over the system interconnect. Since code execution includes instruction fetches from memories hosted on the interconnect, the transfers over the interconnect are designed to be safe by a combination of ECC and redundancy based mechanisms. Any failures detected in the transfers are reported over the ESM interface. This mechanism is enabled by default in HW.
16	Error Signaling Module	When a diagnostic detects a fault, the error must be indicated. The Device architecture provides aggregation of fault indication from internal monitoring/diagnostic mechanisms using a peripheral logic known as the Error Signaling Module (ESM). The ESM provides mechanisms to classify errors by severity and to provide programmable error response. ESM module is configured by customer application code and specific error signals can be enabled or masked to generate an interrupt (Low/High priority) for the MSS R5F CPU. Device supports Nerror output signal (IO) which can be monitored externally to identify any kind of high severity faults in the design which are not be handled by the R5F.
17	Temperature Sensor	Device architecture supports various temperature sensors at temperature hotspots in digital across the device that can be monitored by the application using an internal GPADC channel.
18	Voltage Monitors	Device architecture supports monitoring the supply rails connected to the chip, in conjunction with external voltage monitors.
DSP SUB-SYSTEM		
1	Boot time LBIST for DSP core	Device supports boot time LBIST for the DSP Core. LBIST can be triggered by the MSS R5F secondary bootloader/application code before starting the functional safety application.
2	Boot time PBIST for L1P, L1D, L2 and L3 Memories, HWA memories, RSS Memories (ADCBUF, CQ Memory), Mailbox	Device architecture supports a hardware programmable memory BIST (PBIST) engine for DSPSS and RSS memories which provide a very high diagnostic coverage (March-13n). PBIST is triggered by MSS R5F secondary bootloader/application code before starting the functional safety application.
3	Parity on L1P, ECC on L1D	Device architecture supports Parity diagnostic on DSP's L1P memory. Parity error is reported to the CPU as an interrupt. L1D memory is covered by SECDED ECC.
4	ECC on DSP's L2 Memory	Device architecture supports both Parity Single error correction double error detection (SECDED) ECC diagnostic on DSP's L1D and L2 memory. L2 Memory is a unified 384KB of memory used to store program and Data sections for the DSP. A 12-bit code word is used to store the ECC data as calculated over the 256-bit data bus (logical instruction fetch size). The ECC logic for the L2 access is located in the DSP and evaluation is done by the ECC control logic inside the DSP. This scheme provides end-to-end diagnostics on the transmissions between DSP and L2. Byte aligned Parity mechanism is also available on L2 to take care of data section.
5	ECC on Radar Data Cube (L3) Memory, HWA Memories, RSS Memory (ADCBUF), Mailbox	L3 memory is used as Radar data section in the device. The architecture supports Single error correction double error detection (SECDED) ECC diagnostic on L3 memory. A 12-bit code word is used to store the ECC data as calculated over the 256-bit data bus. The RSS memory (ADCBUF) too supports the SECDED ECC diagnostics. Failure detection by ECC logic is reported to the DSP core as an interrupt via ESM.
6	RTI/WDT for DSP Core	Device architecture supports the use of an internal watchdog for DSP C66x that is implemented in the real-time interrupt (RTI) module – replication of same module as used in Main SS. This module supports same features as that of RTI/WD for MSS. This watchdog is enabled by customer application code and Timeout condition is reported via an interrupt to DSP and/or MSS R5F and rest is left to application code in MSS R5F to take the device to a safe state.

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Table 8-1. Monitoring and Diagnostic Mechanisms for AWR294x (continued)

NO	FEATURE	DESCRIPTION
7	CRC for DSP Sub-System	Device architecture supports hardware CRC engine on DSPSS implementing the below polynomials. • CRC16 CCITT – 0x10 • CRC32 Ethernet – 0x04C11DB7 • CRC64 • CRC 32C – CASTAGNOLI – 0x1EDC6F4 • CRC32P4 – E2E Profile4 – 0xF4ACFB1 The read operation of the SRAM contents to the CRC can be done by CPU or by DMA. The comparison of results, indication of fault, and fault response are the responsibility of the software managing the test.
8	MPU for DSP	Device architecture supports MPUs for DSP memory accesses (L1D, L1P, and L2). L2 memory supports 64 regions and 16 regions for L1P and L1D each. Failure detection by MPU is reported to the DSP core as an abort.
9	MPU	Device architecture supports MPUs on certain peripheral ports in the DSP SS that include L3 Memory banks. This allows configuring access permissions to these key regions in the DSP SS. By default, this control resides with the HSM.
BIST (Within RADAR SUB-SYSTEM)		
NOTE: BIST is handled by the TI firmware. Refer to the mmWave Interface Control Document (as a part of mmWave-MCUPLUS-SDK package) and safety manual for information on safety mechanisms.		

Note

Refer to the Device Safety Manual or other relevant collaterals for more details on applicability of all diagnostics mechanisms.

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9 Applications, Implementation, and Layout

Note

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Key device features driving the following applications are:

- Integration of Radar Front End and Programmable MCU
- Flexible boot modes: Autonomous application boot using a serial flash or external boot over SPI
- Hardware Security Module
- High speed 100Mbps Fast Ethernet Support

9.2 Short and Medium Range Radar

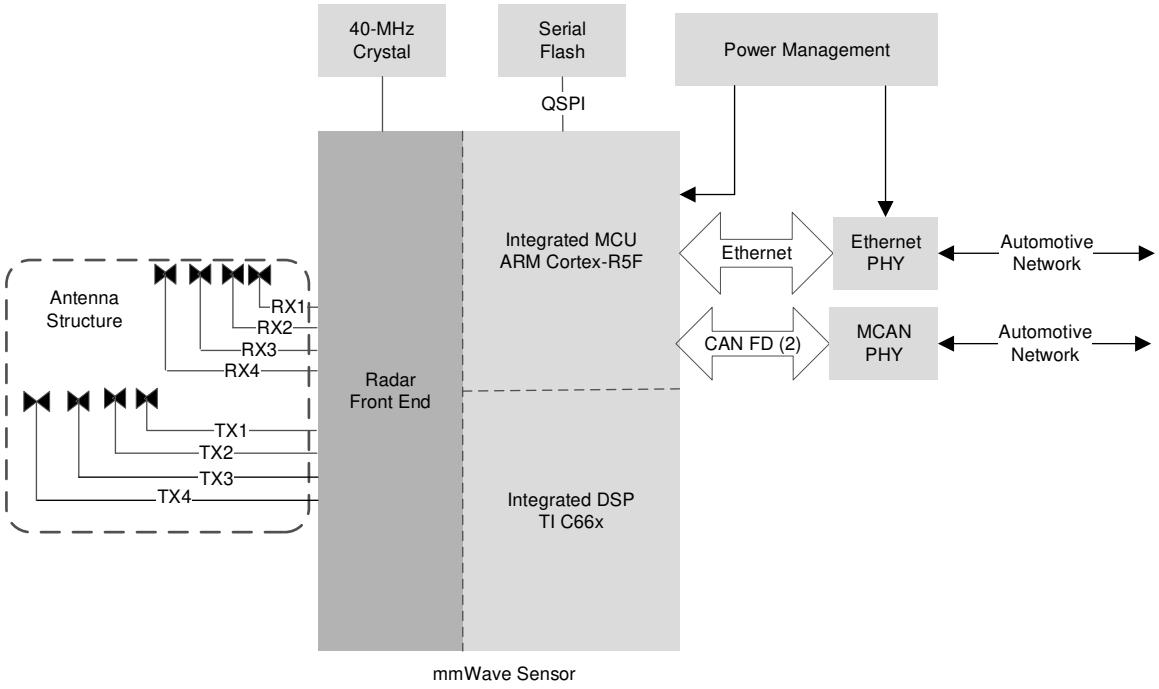

Figure 9-1. Short- and Medium-Range Radar

9.3 Reference Schematic

The reference schematic and power supply information can be found in the AWR2944 EVM Documentation.

Listed for convenience are: Design Files, Schematics, Layouts, and Stack up details for PCB at the AWR2944 EVM Product page.

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Device Support

10.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *XA2943BGALT*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *your package*), the temperature range (for example, blank is the default commercial temperature range), and the device speed range, in megahertz (for example, *your device speed range*). Figure x provides a legend for reading the complete device name for any *your device* device.

For orderable part numbers of *your device* devices in the *your package* package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the AWR2944 Errata

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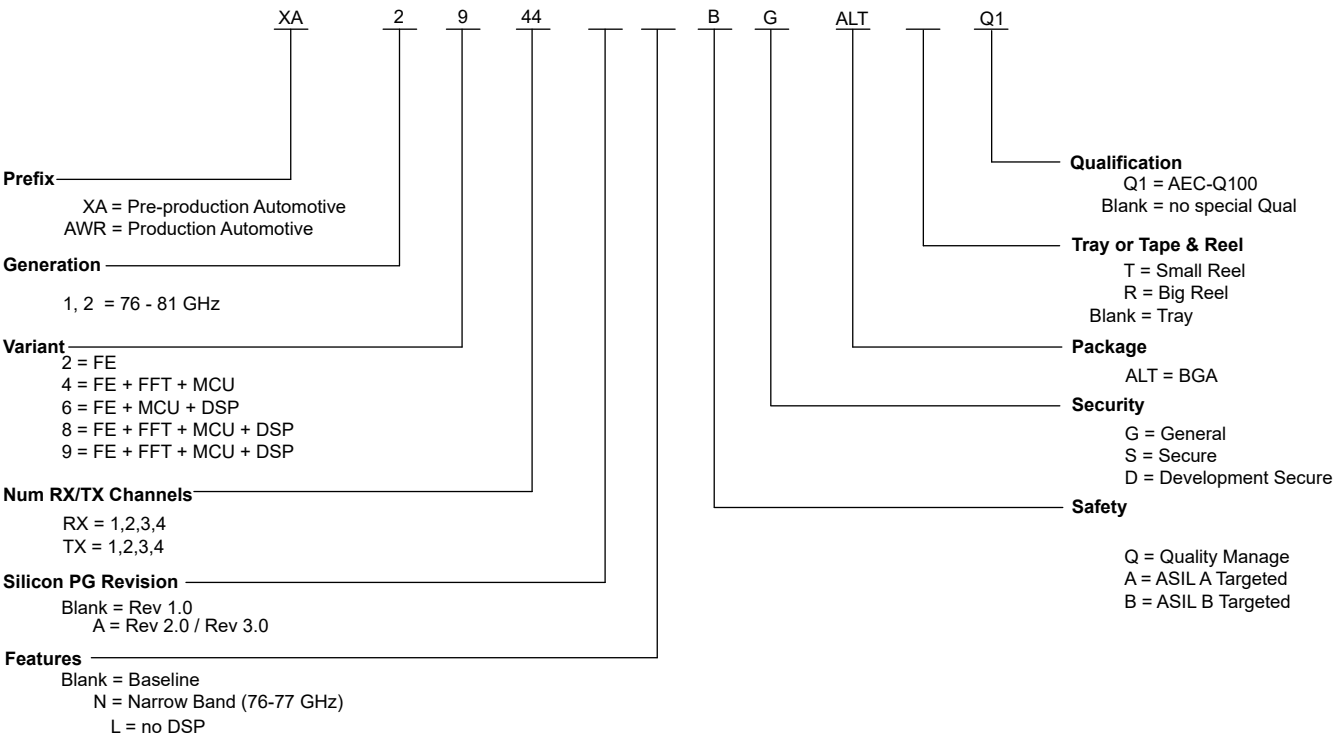

Figure 10-1. Device Nomenclature

10.3 Tools and Software

The contents in this section will be updated in subsequent versions.

10.4 Documentation support

The contents in this section will be updated in subsequent versions.

10.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.7 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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10.9 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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11 Revision History

Changes from September 30, 2024 to February 1, 2026 (from Revision D (September 2024) to Revision E (February 2026)) **Page**

- Updated ESD ratings for GPADC5 and GPADC6.....34

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AWR2943ABGALTQ1	Active	Production	FCCSP (ALT) | 266	168 | JEDEC TRAY (5+1)	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2943 BG 987B
AWR2943ABGALTQ1.B	Active	Production	FCCSP (ALT) | 266	168 | JEDEC TRAY (5+1)	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2943 BG 987B
AWR2943ABGALTRQ1	Active	Production	FCCSP (ALT) | 266	1000 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2943 BG 987B
AWR2943ABGALTRQ1.B	Active	Production	FCCSP (ALT) | 266	1000 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2943 BG 987B
AWR2944ABGALTQ1	Active	Production	FCCSP (ALT) | 266	168 | JEDEC TRAY (5+1)	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2944 BG 987B
AWR2944ABGALTQ1.B	Active	Production	FCCSP (ALT) | 266	168 | JEDEC TRAY (5+1)	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2944 BG 987B
AWR2944ABGALTRQ1	Active	Production	FCCSP (ALT) | 266	1000 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2944 BG 987B
AWR2944ABGALTRQ1.B	Active	Production	FCCSP (ALT) | 266	1000 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2944 BG 987B
AWR2944ALBGALTQ1	Active	Production	FCCSP (ALT) | 266	168 | JEDEC TRAY (5+1)	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2944L BG 987B
AWR2944ALBGALTQ1.B	Active	Production	FCCSP (ALT) | 266	168 | JEDEC TRAY (5+1)	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2944L BG 987B
AWR2944ALBGALTRQ1	Active	Production	FCCSP (ALT) | 266	1000 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2944L BG 987B

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AWR2944ALBGALTRQ1.B	Active	Production	FCCSP (ALT) | 266	1000 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2944L BG 987B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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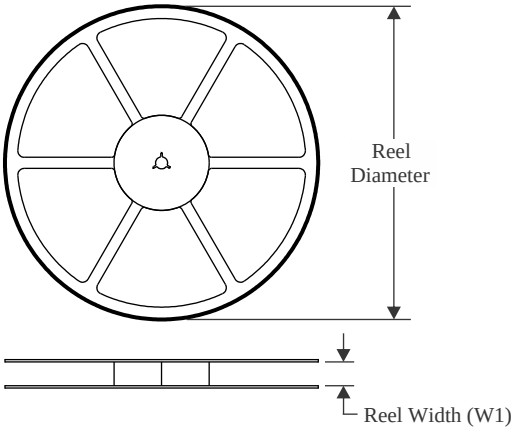
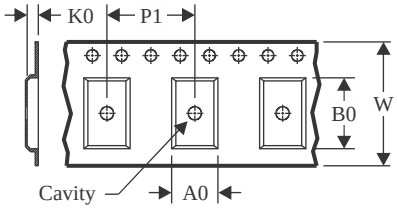
TAPE AND REEL INFORMATION

REEL DIMENSIONS

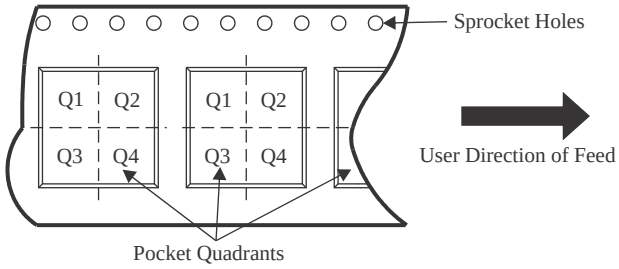


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

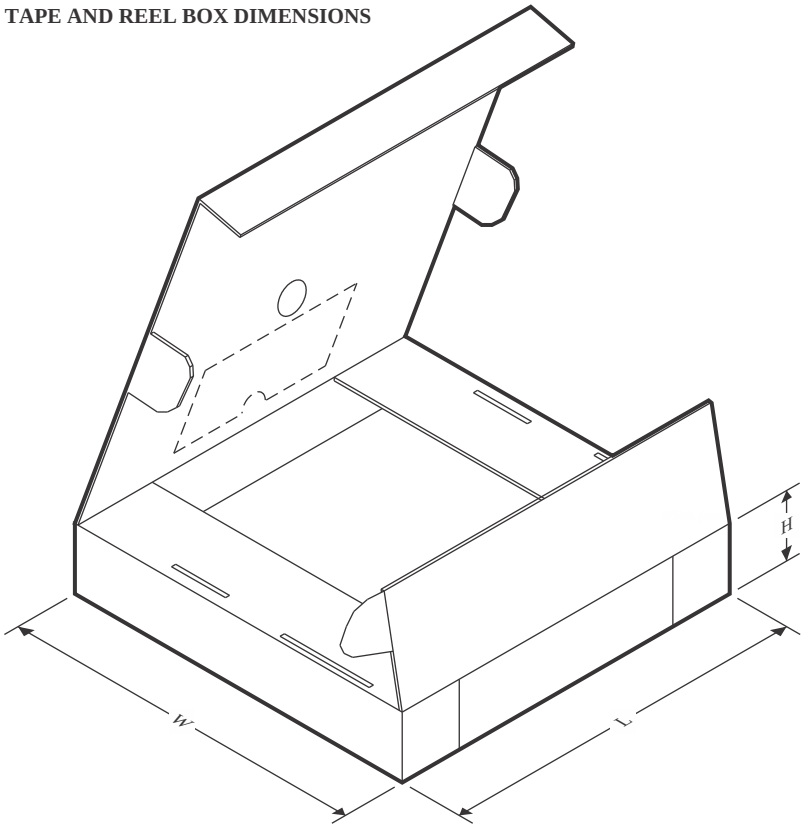
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AWR2943ABGALTRQ1	FCCSP	ALT	266	1000	330.0	24.4	12.3	12.3	1.6	20.0	24.0	Q1
AWR2944ABGALTRQ1	FCCSP	ALT	266	1000	330.0	24.4	12.3	12.3	1.6	20.0	24.0	Q1
AWR2944ALBGALTRQ1	FCCSP	ALT	266	1000	330.0	24.4	12.3	12.3	1.6	20.0	24.0	Q1

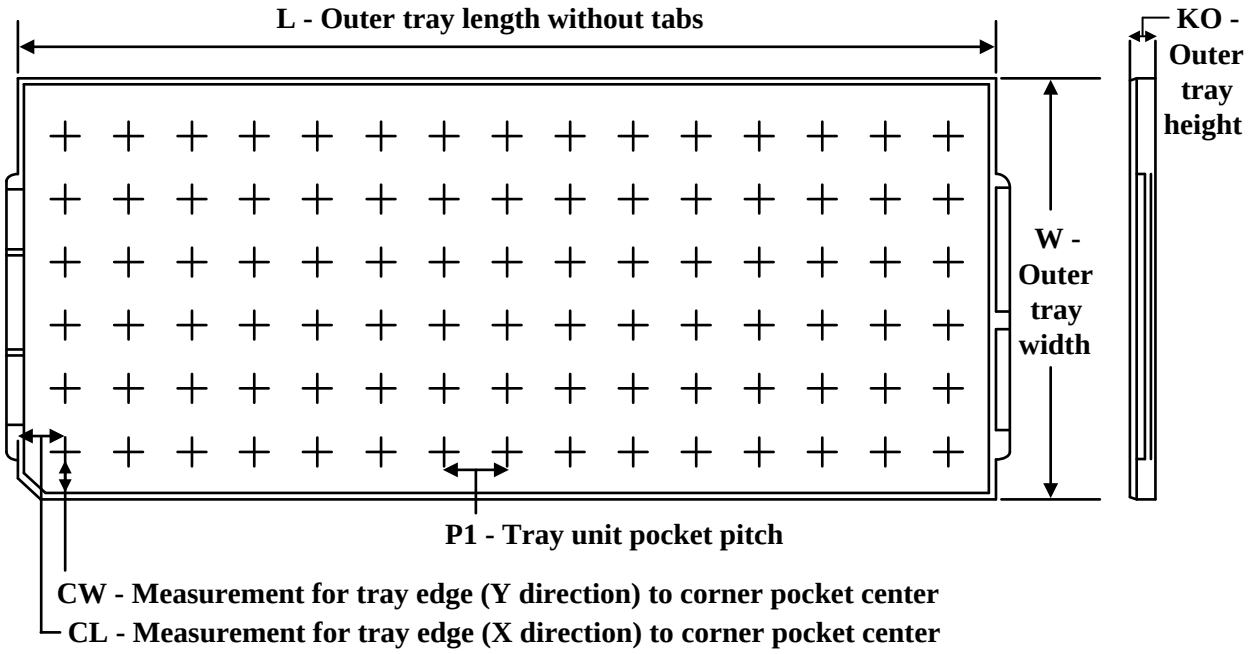
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AWR2943ABGALTRQ1	FCCSP	ALT	266	1000	336.6	336.6	41.3
AWR2944ABGALTRQ1	FCCSP	ALT	266	1000	336.6	336.6	41.3
AWR2944ALBGALTRQ1	FCCSP	ALT	266	1000	336.6	336.6	41.3

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

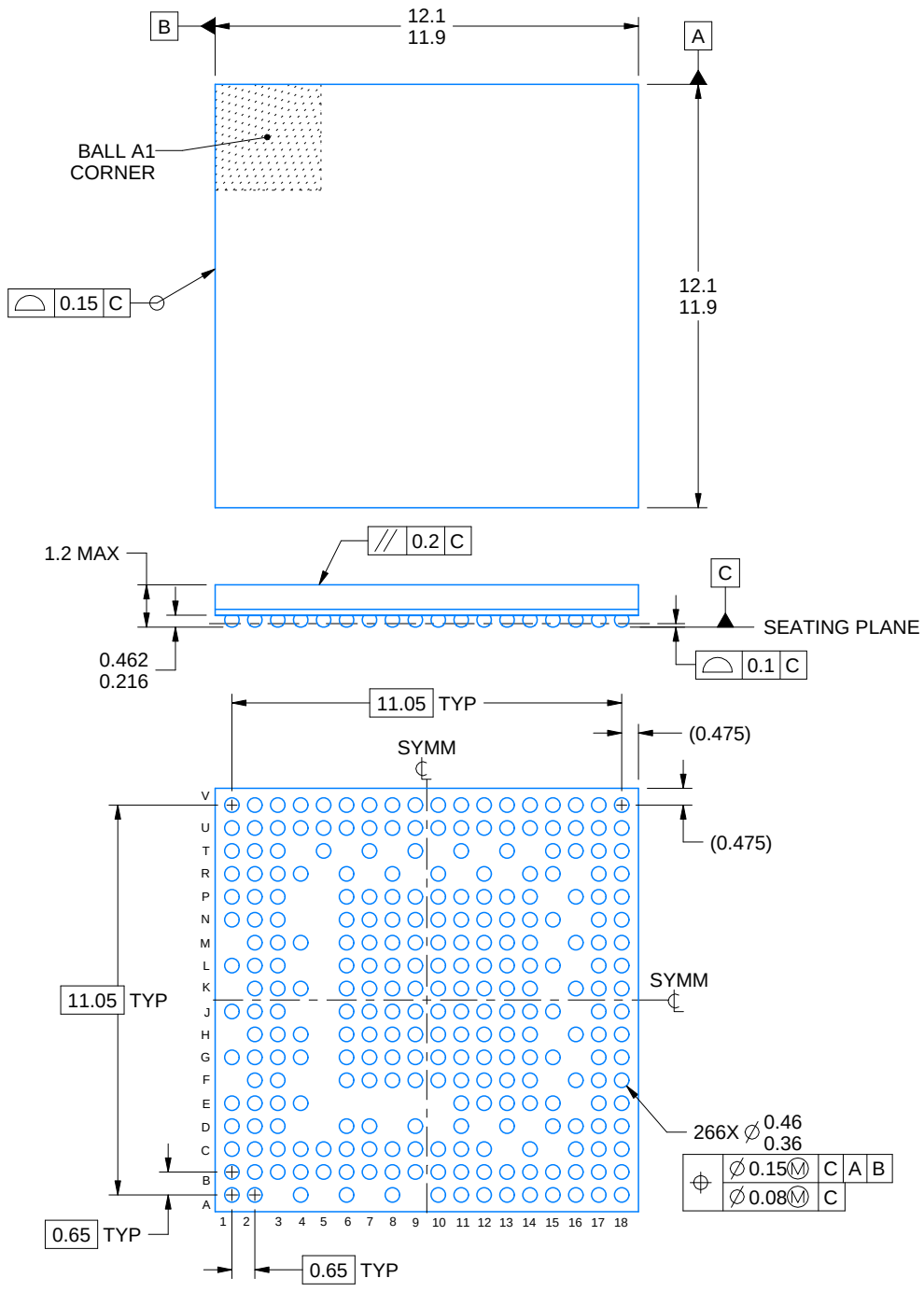
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AWR2943ABGALTQ1	ALT	FCCSP	266	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
AWR2943ABGALTQ1.B	ALT	FCCSP	266	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
AWR2944ABGALTQ1	ALT	FCCSP	266	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
AWR2944ABGALTQ1.B	ALT	FCCSP	266	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
AWR2944ALBGALTQ1	ALT	FCCSP	266	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
AWR2944ALBGALTQ1.B	ALT	FCCSP	266	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
AWR2944ALBGALTRQ1	ALT	FCCSP	266	1000	8 X 21	150	315	135.9	7620	14.65	11	11.95
AWR2944ALBGALTRQ1.B	ALT	FCCSP	266	1000	8 X 21	150	315	135.9	7620	14.65	11	11.95

PACKAGE OUTLINE

ALT0266A

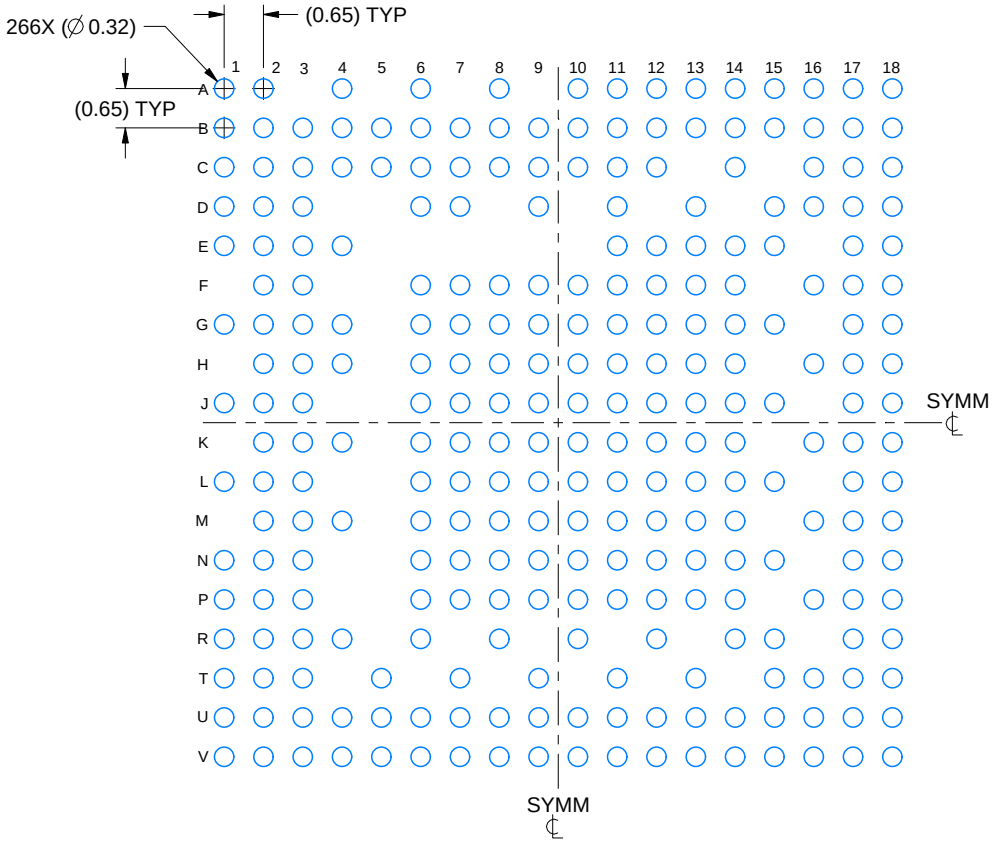
FCBGA - 1.2 mm max height

BALL GRID ARRAY

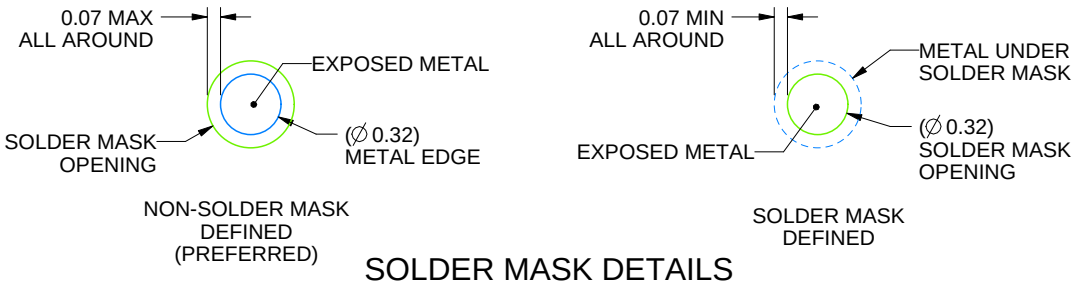


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS
NOT TO SCALE

4226546/B 05/2023

NOTES: (continued)

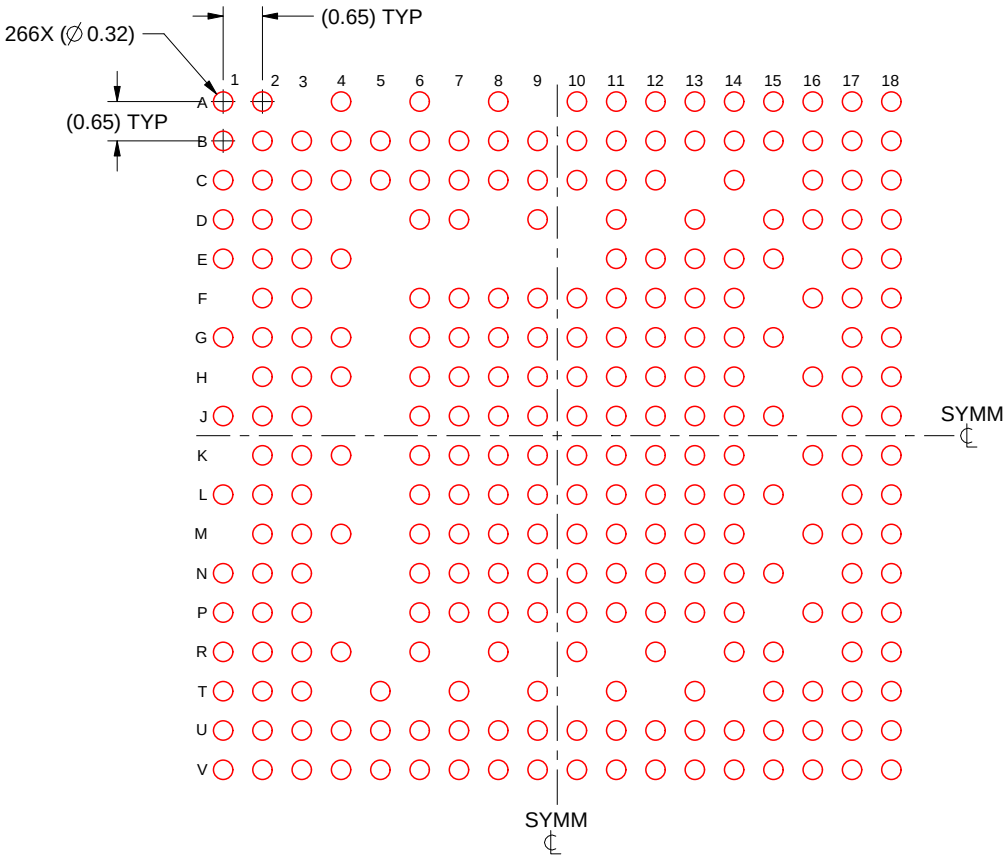
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ALT0266A

FCBGA - 1.2 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4226546/B 05/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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