

## AM654x, AM652x Sitara™ Processors

### Silicon Revision 2.1

## 1 Features

### Processor cores:

- Dual- or quad-core Arm® Cortex®-A53 microprocessor subsystem at up to 1.1 GHz
  - Up to two dual-core or two single-core Arm® Cortex®-A53 clusters with 512KB L2 cache including SECEDED
  - Each A53 core has 32KB L1 ICache and 32K L1 DCache
- Dual-core Arm® Cortex®-R5F at up to 400 MHz
  - Supports lockstep mode
  - 16KB ICache, 16KB DCache, and 64KB RAM per R5F core

### Industrial subsystem:

- Three gigabit Industrial Communication Subsystems (PRU\_ICSSG)
  - Up to two 10/100/1000 Ethernet ports per PRU\_ICSSG
  - Supports two SGMII ports<sup>(2)</sup>
  - Compatibility with 10/100Mb PRU-ICSS
  - 24× PWMs per PRU\_ICSSG
    - Cycle-by-cycle control
    - Enhanced trip control
  - 18× Sigma-delta filters per PRU\_ICSSG
    - Short circuit logic
    - Over-current logic
  - 6× Multi-protocol position encoder interfaces per PRU\_ICSSG

### Memory subsystem:

- Up to 2MB of on-chip L3 RAM with SECEDED
- Multi-core Shared Memory Controller (MSMC)
  - Up to 2MB (2 banks × 1MB) SRAM with SECEDED
    - Shared coherent Level 2 or Level 3 memory-mapped SRAM
    - Shared coherent Level 3 Cache
  - 256-bit processor port bus and 40-bit physical address bus
  - Coherent unified bi-directional interfaces to connect to processors or device masters
  - L2, L3 Cache pre-warming and post flushing
  - Bandwidth management with starvation bound
  - One infrastructure master interface
  - Single external memory master interface
  - Supports distributed virtual system
  - Supports internal DMA engine – Data Routing Unit (DRU)

- ECC error protection
- DDR Subsystem (DDRSS)
  - Supports DDR4 memory types up to DDR-1600
  - 32-bit data bus and 7-bit SECEDED bus
  - 8 GB of total addressable space
- General-Purpose Memory Controller (GPMC)

### Functional Safety:

- [Functional Safety-Compliant](#) [Industrial]
  - Developed for functional safety applications
  - Documentation available to aid IEC 61508 functional safety system design
  - Systematic capability up to SIL 3
  - Hardware Integrity up to SIL 2
  - Safety-related certification
    - [IEC 61508 certified by TÜV SÜD](#)
- Functional safety features:
  - ECC or parity on calculation-critical memories and internal bus interconnect
  - Firewalls to help provide Freedom From Interference (FFI)
    - Built-In Self-Test (BIST) for CPU, high-end timers, and on-chip RAM
  - Hardware error injection support for test-for-diagnostics
  - Error Signaling Modules (ESM) for capture of functional safety related errors
  - Voltage, temperature, and clock monitoring
  - Windowed and non-windowed watchdog timers in multiple clock domains
- MCU island
  - Isolation of the dual-core Arm® Cortex®-R5F microprocessor subsystem
  - Separate voltage, clocks, resets, and dedicated peripherals
  - Internal MCSPI connection to the rest of SoC

### Security:

- Secure boot supported
  - Hardware-enforced root-of-trust
  - Support to switch root-of-trust via backup key
  - Support for takeover protection, IP protection, and anti-roll back protection
- Cryptographic acceleration supported
  - Session-aware cryptographic engine with ability to auto-switch key-material based on incoming data stream
  - Supports cryptographic cores
    - AES – 128/192/256 bits key sizes
    - 3DES – 56/112/168 bits key sizes
    - MD5, SHA1



- SHA2 – 224/256/384/512
- DRBG with true random number generator
- PKA (public key accelerator) to assist in RSA/ECC processing
  - DMA support
- Debugging security
  - Secure software-controlled debug access
  - Security aware debugging
- Trusted Execution Environment (TEE) supported
  - Arm® TrustZone® based TEE
  - Extensive firewall support for isolation
  - Secure DMA path and interconnect
  - Secure watchdog/timer/IPC
- Secure storage support
- On-the-fly encryption and authentication support for OSPI interface
- Networking security support for data (payload) encryption/authentication via packet based hardware cryptographic engine
- Security coprocessor (DMSC) for key and security management, with dedicated device level interconnect for security software

#### SoC services:

- Device Management Security Controller (DMSC)
  - Centralized SoC system controller
  - Manages system services including initial boot, security, functional safety and clock/reset/power management
  - Power management controller for active and low power modes
  - Communication with various processing units over message manager
  - Simplified interface for optimizing unused peripherals
  - Tracing and debugging capability
- Sixteen 32-bit general-purpose timers
- Two data movement and control Navigator Subsystems (NAVSS)
  - Ring Accelerator (RA)
  - Unified DMA (UDMA)
  - Up to 2 Timer Managers (TM) (1024 timers each)

#### Multimedia:

- Display subsystem
  - Two fully input-mapped overlay managers associated with two display outputs
  - One port MIPI® DPI parallel interface
  - One port OLDI
- PowerVR® SGX544-MP1 3D Graphics Processing Unit (GPU)
- One Camera Serial Interface-2 (MIPI CSI-2)
- One port video capture: BT.656/1120 (no embedded sync)

#### High-speed interfaces:

- One Gigabit Ethernet (CPSW) interface supporting
  - RMII (10/100) or RGMII (10/100/1000)
  - IEEE1588 (2008 Annex D, Annex E, Annex F) with 802.1AS PTP
  - Audio/video bridging (P802.1Qav/D6.0)
  - Energy-efficient Ethernet (802.3az)
  - Jumbo frames (2024 bytes)
  - Clause 45 MDIO PHY management
- Two PCI-Express® (PCIe®) revision 3.1 subsystems<sup>(2)</sup>
  - Supports Gen2 (5.0GT/s) operation
  - Two independent 1-lane, or a single 2-lane port
  - Support for concurrent root-complex and end-point operation
- USB 3.1 Dual-Role Device (DRD) subsystem<sup>(2)</sup>
  - One enhanced SuperSpeed Gen1 port
  - One USB 2.0 port
  - Each port independently configurable as USB host, USB peripheral, or USB DRD

#### General connectivity:

- 6× Inter-Integrated Circuit (I2C™) ports
- 5× configurable UART/IrDA/CIR modules
- Two simultaneous flash interfaces configured as
  - Two OSPI flash interfaces
  - or HyperBus™ and OSPI1 flash interface
- 2× 12-bit Analog-to-Digital Converters (ADC)
  - Up to 4 Msamples/s
  - Eight multiplexed analog inputs
- 8× Multichannel Serial Peripheral Interfaces (MCSPI) controllers
  - Two with internal connections
  - Six with external interfaces
- General-Purpose I/O (GPIO) pins

#### Control interfaces:

- 6× Enhanced High-Resolution Pulse-Width Modulator (EHRPWM) modules
- One Enhanced Capture (ECAP) module
- 3× Enhanced Quadrature Encoder Pulse (EQEP) modules

#### Automotive interfaces:

- 2× Modular Controller Area Network (MCAN) modules with full CAN-FD support

#### Audio interfaces:

- 3× Multichannel Audio Serial Port (MCASP) modules

#### Media and data storage:

- 2× Multimedia Card™/ Secure Digital® (MMC™/SD®) interfaces

**Simplified power management:**

- Simplified power sequence with full support for dual voltage I/O
- Integrated LDOs reduces power solution complexity
- Integrated SDIO LDO for handling automatic voltage transition for SD interface
- Integrated Power On Reset (POR) generation reducing power solution complexity
- Integrated voltage supervisor for functional safety monitoring
- Integrated power supply glitch detector for detecting fast power supply transients

**Analog/system integration:**

- Integrated USB VBUS detection
- Fail safe I/O for DDR RESET
- All I/O pins drivers disabled during reset to avoid bus conflicts
- Default I/O pulls disabled during reset to avoid system conflicts
- Support dynamic I/O pinmux configuration change

**System-on-Chip (SoC) architecture:**

- Supports primary boot from UART, I2C, OSPI, HyperBus, parallel NOR Flash, SD or eMMC™, USB, PCIe, and Ethernet interfaces
- 28-nm CMOS technology
- 23 mm × 23 mm, 0.8-mm pitch, 784-pin FCBGA (ACD)

**2 Applications**

- [Industrial Programmable Logic Controllers \(PLC\)](#)
- [Factory automation with safety functions](#)
- [Multi-protocol fieldbus communications](#)
- [Industrial PC](#)
- [Industrial robots](#)
- [Human Machine Interface \(HMI\)](#)
- [Grid infrastructure protection relays](#)
- [Robotic motor drives](#)

### 3 Description

AM654x and AM652x Sitara™ processors are Arm® applications processors built to meet the complex processing needs of modern industry 4.0 embedded products.

The AM654x and AM652x devices combine four or two Arm® Cortex®-A53 cores with a dual Arm® Cortex®-R5F MCU subsystem which includes features intended to help customers achieve their functional safety goals for their end products and three Gigabit industrial communications subsystems (PRU\_ICSSG) to create a SoC capable of high-performance industrial controls with industrial connectivity and processing for functional safety applications. AM65xx is currently undergoing assessment to be certified by TÜV SÜD according to IEC 61508.

The four Arm® Cortex®-A53 cores in the AM654x are arranged in two dual-core clusters with shared L2 memory to create two processing channels. The two Arm® Cortex®-A53 cores in the AM652x are available in a single dual-core cluster and two single-core cluster options. Extensive ECC is included on on-chip memory, peripherals, and interconnect for reliability. The SoC as a whole includes features intended to help customers design systems that can achieve their functional safety goals (assessment pending with TÜV SÜD). Cryptographic acceleration and secure boot are available on some AM654x and AM652x devices in addition to granular firewalls managed by the DMSC.

Programmability is provided by the Arm® Cortex®-A53 RISC CPUs with Arm® Neon™ extension, and the dual Arm® Cortex®-R5F MCU subsystem is available for general purpose use as two cores or it can be used in lockstep to help meet the needs of functional safety applications. The PRU\_ICSSG subsystems can be used to provide up to six ports of industrial Ethernet such as Profinet IRT, TSN, Ethernet/IP or EtherCAT® (among many others), or they can be used for standard Gigabit Ethernet connectivity.

TI provides a complete set of software and development tools for the Arm® cores including Processor SDK Linux, Linux-RT, RTOS, and Android as well as C compilers and a debugging interface for visibility into source code execution. Applicable functional safety and security documentation will be made available to assist customers in developing their functional safety or security related systems.

**Package Information**

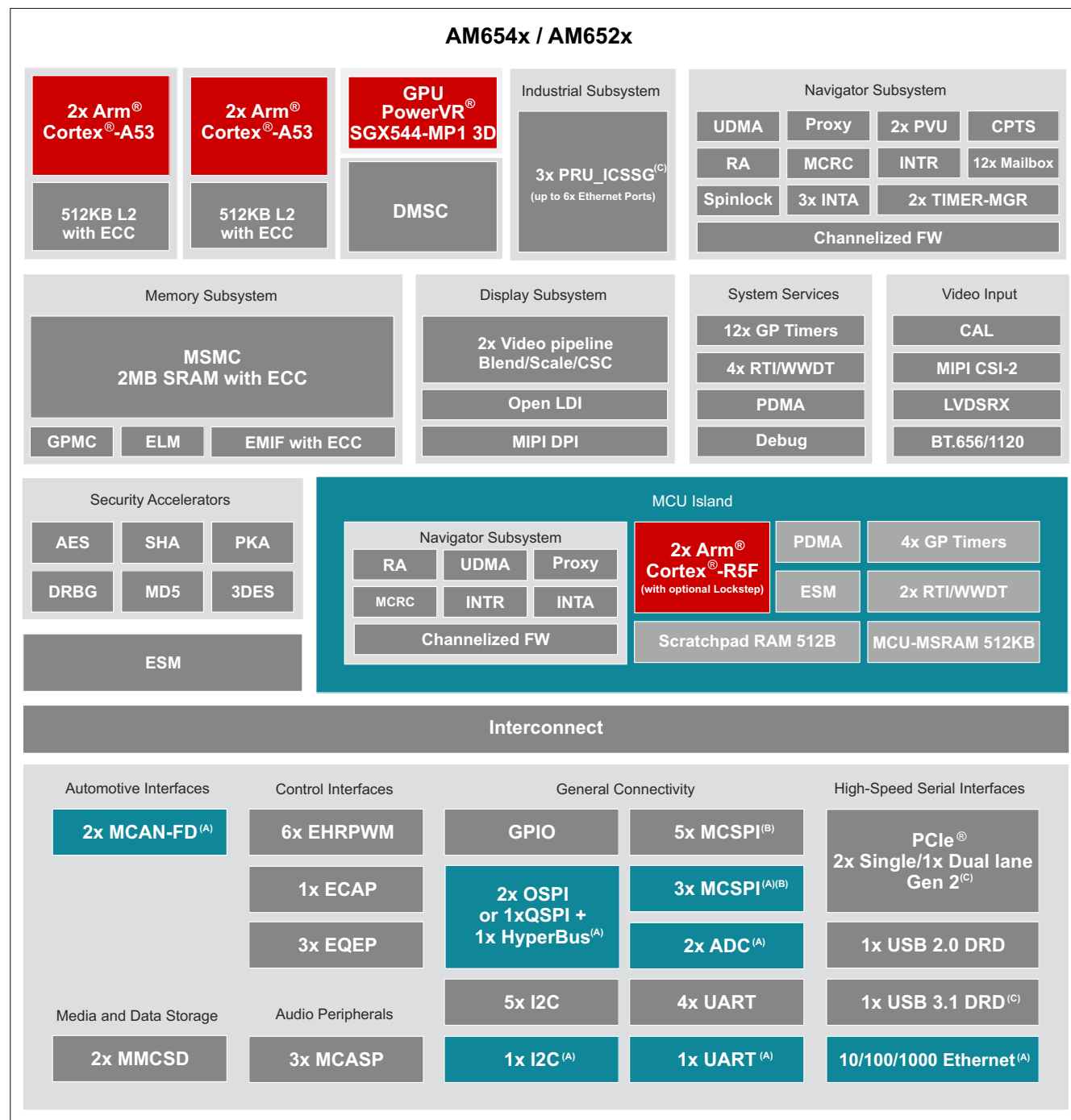
| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| AM6548      | ACD (FCBGA, 784)       | 23.0 mm × 23.0 mm           |
| AM6528      | ACD (FCBGA, 784)       | 23.0 mm × 23.0 mm           |
| AM6546      | ACD (FCBGA, 784)       | 23.0 mm × 23.0 mm           |
| AM6526      | ACD (FCBGA, 784)       | 23.0 mm × 23.0 mm           |

(1) For more information, see [Section 11, Mechanical, Packaging, and Orderable Information](#)

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

## 3.1 Functional Block Diagram

Figure 3-1 is functional block diagram for the device.



- A. This interface is located on the MCU Island but is available for the full system to access.  
 B. One port is internally connected only; not connected to any pins.  
 C. SGMII, USB3.1 and PCIe share a total of two SerDes lanes.

**Figure 3-1. AM654x, AM652x Block Diagram**

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## 4 Device Comparison

Table 4-1 shows a comparison between devices, highlighting the differences.

**Table 4-1. Device Comparison**

| FEATURES                                                                                     | REFERENCE NAME | AM6548                                       | AM6528                | AM6546                           | AM6526                |
|----------------------------------------------------------------------------------------------|----------------|----------------------------------------------|-----------------------|----------------------------------|-----------------------|
| FEATURES                                                                                     |                |                                              |                       |                                  |                       |
| CTRLMMR_WKUP_JTAG_DEVICE_ID [31:11] DEVICE_ID register bit field value <sup>(5)</sup>        |                | AM6548: 0x140FA                              | AM6528: 0x140BA       | AM6546: 0x14178                  | AM6526: 0x14138       |
|                                                                                              |                | AM6548-E: 0x140FB                            | AM6528-E: 0x140BB     | AM6546-E: 0x14179                | AM6526-E: 0x14139     |
|                                                                                              |                | AM6548-F: 0x140FE                            | AM6528-F: 0x140BE     | AM6546-F: 0x1417C                | AM6526-F: 0x1413C     |
|                                                                                              |                | AM6548-E,F: 0x140FF                          | AM6528-E,F: 0x140BF   | AM6546-E,F: 0x1417D              | AM6526-E,F: 0x1413D   |
| PROCESSORS AND ACCELERATORS                                                                  |                |                                              |                       |                                  |                       |
| Speed Grades                                                                                 |                | See Table 6-1, Speed Grade Maximum Frequency |                       |                                  |                       |
| Arm Cortex-A53 Microprocessor Subsystem                                                      | Arm A53        | Quad Core (Cluster 0, Cluster 1)             | Dual Core (Cluster 0) | Quad Core (Cluster 0, Cluster 1) | Dual Core (Cluster 0) |
| Dual-Core Arm Cortex-R5F                                                                     | Arm R5F        | Yes (optional lockstep <sup>(4)</sup> )      |                       |                                  |                       |
| Device Management Security Controller                                                        | DMSC           | Yes                                          |                       |                                  |                       |
| Graphics Accelerator (SGX544-MP1)                                                            | GPU            | Yes                                          |                       | Not Supported <sup>(1)</sup>     |                       |
| Safety Features                                                                              | Safety         | Optional <sup>(4)</sup>                      |                       | Optional <sup>(4)</sup>          |                       |
| PROGRAM AND DATA STORAGE                                                                     |                |                                              |                       |                                  |                       |
| On-Chip Shared Memory (RAM)                                                                  | MCU_MSRAM      | 512KB                                        |                       |                                  |                       |
| Multicore Shared Memory Controller                                                           | MSMC           | 2MB (On-Chip Shared SRAM with ECC)           |                       |                                  |                       |
| DDR4 DDR Subsystem <sup>(6)</sup>                                                            | DDRSS          | Up to 8GB (32-Bit data)                      |                       |                                  |                       |
|                                                                                              | SECEDED        | 7-Bit                                        |                       |                                  |                       |
| General-Purpose Memory Controller                                                            | GPMC           | Up to 1GB with ECC                           |                       |                                  |                       |
| Error Location Module                                                                        | ELM            | Yes                                          |                       |                                  |                       |
| PERIPHERALS                                                                                  |                |                                              |                       |                                  |                       |
| Display Subsystem                                                                            | DSS            | Yes                                          |                       |                                  |                       |
| Modular Controller Area Network Interface                                                    | MCAN           | 2                                            |                       |                                  |                       |
| Peripheral Direct Memory Access                                                              | PDMA           | Yes                                          |                       |                                  |                       |
| Navigator Subsystem                                                                          | NAVSS          | 2                                            |                       |                                  |                       |
| General-Purpose I/O                                                                          | GPIO           | Up to 242                                    |                       |                                  |                       |
| Inter-Integrated Circuit Interface                                                           | I2C            | 6                                            |                       |                                  |                       |
| Analog-to-Digital Converter                                                                  | ADC            | 2                                            |                       |                                  |                       |
| Camera Adaptation Layer (CAL) with Camera Serial Interface (CSI2) and Video Input Port (VIN) | CSI2           | 1 CLK + 4 Data                               |                       |                                  |                       |
|                                                                                              | VIN0           | Yes                                          |                       |                                  |                       |
| Multichannel Serial Peripheral Interface                                                     | MCSPi          | 8                                            |                       |                                  |                       |
| Multichannel Audio Serial Port                                                               | MCASP0         | 16 Serializers                               |                       |                                  |                       |
|                                                                                              | MCASP1         | 10 Serializers                               |                       |                                  |                       |
|                                                                                              | MCASP2         | 4 Serializers                                |                       |                                  |                       |
| MultiMedia Card/ Secure Digital Interface                                                    | MMCSd0         | 8-bits                                       |                       |                                  |                       |
|                                                                                              | MMCSd1         | 4-bits                                       |                       |                                  |                       |



**Table 4-1. Device Comparison (continued)**

| FEATURES                                                                            | REFERENCE NAME | AM6548                                           | AM6528 | AM6546 | AM6526 |
|-------------------------------------------------------------------------------------|----------------|--------------------------------------------------|--------|--------|--------|
| <b>FEATURES</b>                                                                     |                |                                                  |        |        |        |
| Flash Subsystem (FSS)                                                               | OSPI0          | 8-bits <sup>(3)</sup>                            |        |        |        |
|                                                                                     | OSPI1          | 4-bits                                           |        |        |        |
|                                                                                     | HyperBus       | Not Supported <sup>(1)</sup>                     |        |        |        |
| Security Accelerator                                                                | SA             | Yes                                              |        |        |        |
| Error Signalling Module                                                             | ESM            | Yes                                              |        |        |        |
| 2x PCI Express 3.1 Port with Integrated PHY                                         | PCIE0          | Up to Two Lanes <sup>(2)</sup>                   |        |        |        |
|                                                                                     | PCIE1          | Single Lane <sup>(2)</sup>                       |        |        |        |
| 3x Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem     | PRU_ICSSG0     | Yes (2× RGMII, 2× MII)                           |        |        |        |
|                                                                                     | PRU_ICSSG1     | Yes (2× RGMII, 2× MII)                           |        |        |        |
|                                                                                     | PRU_ICSSG2     | Yes (2× RGMII, 2× MII, 2× SGMII <sup>(2)</sup> ) |        |        |        |
| Gigabit Ethernet Interface                                                          | CPSW           | RMII or RGMII                                    |        |        |        |
| General-Purpose Timers                                                              | TIMER          | 16                                               |        |        |        |
| Enhanced High Resolution Pulse-Width Modulator Module                               | EHRPWM         | 6                                                |        |        |        |
| Enhanced Capture Module                                                             | ECAP           | 1                                                |        |        |        |
| Enhanced Quadrature Encoder Pulse Module                                            | EQEP           | 3                                                |        |        |        |
| Universal Asynchronous Receiver and Transmitter                                     | UART           | 5                                                |        |        |        |
| Universal Serial Bus (USB3.1) SuperSpeed Dual-Role-Device (DRD) Ports with SS PHY   | USB0           | Yes <sup>(2)</sup>                               |        |        |        |
| Universal Serial Bus (USB2.0) HighSpeed Dual-Role-Device (DRD) Ports with HS/FS PHY | USB1           | Yes                                              |        |        |        |

- (1) Features noted as “not supported”, must not be used. Their functionality is not supported by TI for this family of devices. These features are subject to removal without notice on future device revisions. Any information regarding the unsupported features has been retained in the documentation solely for the purpose of clarifying signal names or for consistency with previous feature descriptions.
- (2) SGMII0, SGMII1, USB3.1, PCIE0, and PCIE1 share total of two SerDes lanes.
- (3) Two simultaneous flash interfaces configured as OSPI0 and OSPI1, or HyperBus and OSPI1.
- (4) Device supports features to aid in functional safety system designs such as lockstep Arm R5F if the part number is designated with the F option.
- (5) For more details about the CTRLMMR\_WKUP\_JTAG\_DEVICE\_ID register and DEVICE\_ID bit field, see the device TRM.
- (6) Only DDR4 is supported. DDR3L and LPDDR4 are not supported.

## 4.1 Related Products

### Sitara™ processors

Scalable processors based on Arm Cortex-A cores with flexible peripherals, connectivity & unified software support – perfect for sensors to servers.

### Sitara™ processors – Applications

Sitara processors provide scalable solutions for a wide range of applications from HMIs and gateways to more complex equipment such as drives and substation automation equipment. Sitara Arm processors offer scalability and reliability as well as multi-protocol support for industrial communication protocols such as EtherCAT, Ethernet/IP and Profinet.

### Sitara™ processors – Reference designs

TI provides many reference designs containing ‘building block’ solutions to enable customers to rapidly development of their unique products and solutions.

### Companion Products for AM654x, AM652x

Review products that are frequently purchased or used in conjunction with this product.



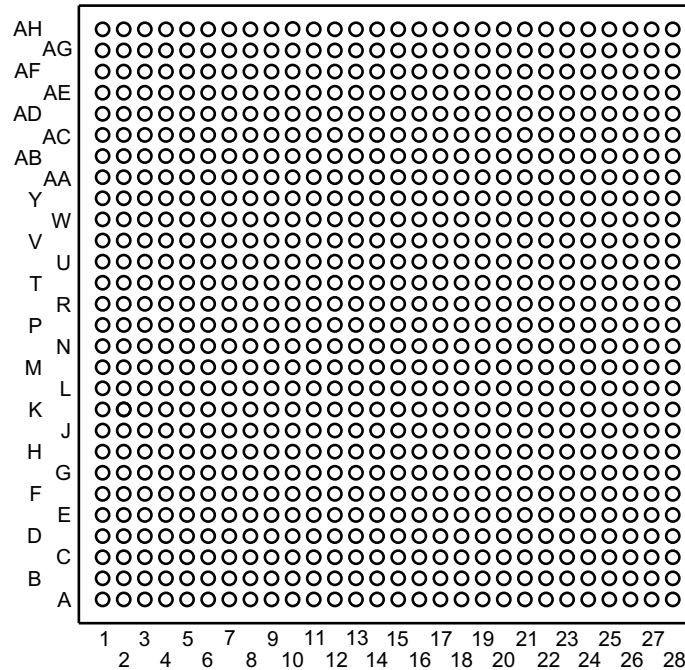
## 5 Terminal Configuration and Functions

### 5.1 Pin Diagram

#### Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

Figure 5-1 shows the ball locations for the 784 plastic ball grid array (FCBGA) package that are used in conjunction with Table 5-1 through Figure 5-1 to locate signal names and ball grid numbers.



**Figure 5-1. ACD FCBGA-N784 Package (Bottom View)**

## 5.2 Pin Attributes

Table 5-1 describes the terminal characteristics and the signals multiplexed on each ball.

**Table 5-1. Pin Attributes**

| BALL NUMBER [1] | BALL NAME [2]           | SIGNAL NAME [3]         | MUXMODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]      | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-------------------------|-------------------------|-------------|----------|----------------------|-----------------------------|-----------------------|----------------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| P17             | CAP_VDDAR_CORE0         | CAP_VDDAR_CORE0         |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| V17             | CAP_VDDAR_CORE1         | CAP_VDDAR_CORE1         |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| W16             | CAP_VDDAR_CORE2         | CAP_VDDAR_CORE2         |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| M14             | CAP_VDDAR_CORE3         | CAP_VDDAR_CORE3         |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| L15             | CAP_VDDAR_CORE4         | CAP_VDDAR_CORE4         |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| U10             | CAP_VDDAR_MCU           | CAP_VDDAR_MCU           |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| M12             | CAP_VDDAR_MPU0_0        | CAP_VDDAR_MPU0_0        |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| N12             | CAP_VDDAR_MPU0_1        | CAP_VDDAR_MPU0_1        |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| N18             | CAP_VDDAR_MPU1_0        | CAP_VDDAR_MPU1_0        |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| N15             | CAP_VDDAR_MPU1_1        | CAP_VDDAR_MPU1_1        |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| Y10             | CAP_VDDAR_WKUP          | CAP_VDDAR_WKUP          |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| AA8             | CAP_VDDA_1P8_IOLDO_WKUP | CAP_VDDA_1P8_IOLDO_WKUP |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| J17             | CAP_VDDA_1P8_SDIO       | CAP_VDDA_1P8_SDIO       |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| G19             | CAP_VDDA_1P8_IOLDO0     | CAP_VDDA_1P8_IOLDO0     |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| Y19             | CAP_VDDA_1P8_IOLDO1     | CAP_VDDA_1P8_IOLDO1     |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| H18             | CAP_VDDSHV_SDIO         | CAP_VDDSHV_SDIO         |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| V9              | CAP_VDD_WKUP            | CAP_VDD_WKUP            |             | CAP      |                      |                             |                       |                |          |                  |                        |           |                           |                     |
| G28             | CSI0_RXN0               | CSI0_RXN0               |             | I        | PD                   |                             | 1.8 V                 | VDDA_1P8_C SI0 |          | DPHY             | PU/PD                  |           |                           | No                  |
| H27             | CSI0_RXN1               | CSI0_RXN1               |             | I        | PD                   |                             | 1.8 V                 | VDDA_1P8_C SI0 |          | DPHY             | PU/PD                  |           |                           | No                  |
| F26             | CSI0_RXN2               | CSI0_RXN2               |             | I        | PD                   |                             | 1.8 V                 | VDDA_1P8_C SI0 |          | DPHY             | PU/PD                  |           |                           | No                  |
| H25             | CSI0_RXN3               | CSI0_RXN3               |             | I        | PD                   |                             | 1.8 V                 | VDDA_1P8_C SI0 |          | DPHY             | PU/PD                  |           |                           | No                  |
| G24             | CSI0_RXN4               | CSI0_RXN4               |             | I        | PD                   |                             | 1.8 V                 | VDDA_1P8_C SI0 |          | DPHY             | PU/PD                  |           |                           | No                  |
| F28             | CSI0_RXP0               | CSI0_RXP0               |             | I        | PD                   |                             | 1.8 V                 | VDDA_1P8_C SI0 |          | DPHY             | PU/PD                  |           |                           | No                  |
| G27             | CSI0_RXP1               | CSI0_RXP1               |             | I        | PD                   |                             | 1.8 V                 | VDDA_1P8_C SI0 |          | DPHY             | PU/PD                  |           |                           | No                  |
| G26             | CSI0_RXP2               | CSI0_RXP2               |             | I        | PD                   |                             | 1.8 V                 | VDDA_1P8_C SI0 |          | DPHY             | PU/PD                  |           |                           | No                  |
| G25             | CSI0_RXP3               | CSI0_RXP3               |             | I        | PD                   |                             | 1.8 V                 | VDDA_1P8_C SI0 |          | DPHY             | PU/PD                  |           |                           | No                  |
| F24             | CSI0_RXP4               | CSI0_RXP4               |             | I        | PD                   |                             | 1.8 V                 | VDDA_1P8_C SI0 |          | DPHY             | PU/PD                  |           |                           | No                  |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMOD<br>E [4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET<br>REL.<br>MUXMOD<br>E [7] | I/O<br>VOLTAGE<br>VALUE [8] | POWER [9] | HYS [10] | BUFFER<br>TYPE [11] | PULL UP/<br>DOWN<br>TYPE [12] | DSIS [13] | RXACTIVE<br>/<br>TXDISABL<br>E [14] | IO Daisy<br>Chain [15] |
|--------------------|---------------|-----------------|-----------------|----------|----------------------------|------------------------------------------|-----------------------------|-----------|----------|---------------------|-------------------------------|-----------|-------------------------------------|------------------------|
| A10                | DDR_AC0       | DDR_AC0         |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| D9                 | DDR_AC1       | DDR_AC1         |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| C9                 | DDR_AC2       | DDR_AC2         |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| E9                 | DDR_AC3       | DDR_AC3         |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| A9                 | DDR_AC4       | DDR_AC4         |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| E8                 | DDR_AC5       | DDR_AC5         |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| F8                 | DDR_AC6       | DDR_AC6         |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| C7                 | DDR_AC7       | DDR_AC7         |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| C8                 | DDR_AC8       | DDR_AC8         |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| D7                 | DDR_AC9       | DDR_AC9         |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| E7                 | DDR_AC10      | DDR_AC10        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| A6                 | DDR_AC11      | DDR_AC11        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| F7                 | DDR_AC12      | DDR_AC12        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| D6                 | DDR_AC13      | DDR_AC13        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| C6                 | DDR_AC14      | DDR_AC14        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| F6                 | DDR_AC15      | DDR_AC15        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| E6                 | DDR_AC16      | DDR_AC16        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| E5                 | DDR_AC17      | DDR_AC17        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| D8                 | DDR_AC18      | DDR_AC18        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| D10                | DDR_AC19      | DDR_AC19        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| E10                | DDR_AC20      | DDR_AC20        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| C10                | DDR_AC21      | DDR_AC21        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| F11                | DDR_AC22      | DDR_AC22        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|---------------|-----------------|-------------|----------|----------------------|-----------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| B10             | DDR_AC23      | DDR_AC23        |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| D11             | DDR_AC24      | DDR_AC24        |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| B11             | DDR_AC25      | DDR_AC25        |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| C11             | DDR_AC26      | DDR_AC26        |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| E11             | DDR_AC27      | DDR_AC27        |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| E12             | DDR_AC28      | DDR_AC28        |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| D12             | DDR_AC29      | DDR_AC29        |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| D5              | DDR_ALERTn    | DDR_ALERTn      |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| B8              | DDR_CK0N      | DDR_CK0N        |             | IO       | drive 1 (OFF)        |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| A8              | DDR_CK0P      | DDR_CK0P        |             | IO       | drive 0 (OFF)        |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| B7              | DDR_CK1N      | DDR_CK1N        |             | IO       | drive 1 (OFF)        |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| A7              | DDR_CK1P      | DDR_CK1P        |             | IO       | drive 0 (OFF)        |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| E1              | DDR_DM0       | DDR_DM0         |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| C5              | DDR_DM1       | DDR_DM1         |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| D14             | DDR_DM2       | DDR_DM2         |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| B17             | DDR_DM3       | DDR_DM3         |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| A3              | DDR_DQ0       | DDR_DQ0         |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| B2              | DDR_DQ1       | DDR_DQ1         |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| C2              | DDR_DQ2       | DDR_DQ2         |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| D2              | DDR_DQ3       | DDR_DQ3         |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| E2              | DDR_DQ4       | DDR_DQ4         |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| G1              | DDR_DQ5       | DDR_DQ5         |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |
| F2              | DDR_DQ6       | DDR_DQ6         |             | IO       | OFF                  |                             | 1.1 V/1.2 V/1.35 V    | VDDS_DDR  |          | DDR              | PU/PD                  |           |                           | No                  |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMOD<br>E [4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET<br>REL.<br>MUXMOD<br>E [7] | I/O<br>VOLTAGE<br>VALUE [8] | POWER [9] | HYS [10] | BUFFER<br>TYPE [11] | PULL UP/<br>DOWN<br>TYPE [12] | DSIS [13] | RXACTIVE<br>/<br>TXDISABL<br>E [14] | IO Daisy<br>Chain [15] |
|--------------------|---------------|-----------------|-----------------|----------|----------------------------|------------------------------------------|-----------------------------|-----------|----------|---------------------|-------------------------------|-----------|-------------------------------------|------------------------|
| F1                 | DDR_DQ7       | DDR_DQ7         |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| E3                 | DDR_DQ8       | DDR_DQ8         |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| C3                 | DDR_DQ9       | DDR_DQ9         |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| D3                 | DDR_DQ10      | DDR_DQ10        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| B3                 | DDR_DQ11      | DDR_DQ11        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| D4                 | DDR_DQ12      | DDR_DQ12        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| C4                 | DDR_DQ13      | DDR_DQ13        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| B4                 | DDR_DQ14      | DDR_DQ14        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| B5                 | DDR_DQ15      | DDR_DQ15        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| E13                | DDR_DQ16      | DDR_DQ16        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| C14                | DDR_DQ17      | DDR_DQ17        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| B14                | DDR_DQ18      | DDR_DQ18        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| A14                | DDR_DQ19      | DDR_DQ19        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| E14                | DDR_DQ20      | DDR_DQ20        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| B13                | DDR_DQ21      | DDR_DQ21        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| C13                | DDR_DQ22      | DDR_DQ22        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| D13                | DDR_DQ23      | DDR_DQ23        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| D15                | DDR_DQ24      | DDR_DQ24        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| C15                | DDR_DQ25      | DDR_DQ25        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| E16                | DDR_DQ26      | DDR_DQ26        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| E15                | DDR_DQ27      | DDR_DQ27        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| D16                | DDR_DQ28      | DDR_DQ28        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |
| B16                | DDR_DQ29      | DDR_DQ29        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                     | No                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER<br>[1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMOD<br>E [4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET<br>REL.<br>MUXMOD<br>E [7] | I/O<br>VOLTAGE<br>VALUE [8] | POWER [9] | HYS [10] | BUFFER<br>TYPE [11] | PULL UP/<br>DOWN<br>TYPE [12] | DSIS [13] | RXACTIVE<br>/ TXDISABL<br>E [14] | IO Daisy<br>Chain [15] |
|--------------------|---------------|-----------------|-----------------|----------|----------------------------|------------------------------------------|-----------------------------|-----------|----------|---------------------|-------------------------------|-----------|----------------------------------|------------------------|
| C16                | DDR_DQ30      | DDR_DQ30        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| A17                | DDR_DQ31      | DDR_DQ31        |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| C1                 | DDR_DQS0N     | DDR_DQS0N       |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| D1                 | DDR_DQS0P     | DDR_DQS0P       |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| A4                 | DDR_DQS1N     | DDR_DQS1N       |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| A5                 | DDR_DQS1P     | DDR_DQS1P       |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| A12                | DDR_DQS2N     | DDR_DQS2N       |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| A13                | DDR_DQS2P     | DDR_DQS2P       |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| A16                | DDR_DQS3N     | DDR_DQS3N       |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| A15                | DDR_DQS3P     | DDR_DQS3P       |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| B19                | DDR_ECC_D0    | DDR_ECC_D0      |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| B18                | DDR_ECC_D1    | DDR_ECC_D1      |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| C18                | DDR_ECC_D2    | DDR_ECC_D2      |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| D18                | DDR_ECC_D3    | DDR_ECC_D3      |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| E18                | DDR_ECC_D4    | DDR_ECC_D4      |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| E17                | DDR_ECC_D5    | DDR_ECC_D5      |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| D17                | DDR_ECC_D6    | DDR_ECC_D6      |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| C17                | DDR_ECC_DM    | DDR_ECC_DM      |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| A18                | DDR_ECC_DQSN  | DDR_ECC_DQSN    |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| A19                | DDR_ECC_DQSP  | DDR_ECC_DQSP    |                 | IO       | OFF                        |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| F16                | DDR_FS_RESETn | DDR_FS_RESETn   |                 | IO       | drive 0 (OFF)              |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | LVC MOS             | PD                            |           |                                  | No                     |
| A11                | DDR_RESETn    | DDR_RESETn      |                 | IO       | drive 0 (OFF)              |                                          | 1.1 V/1.2 V/1.35 V          | VDDS_DDR  |          | DDR                 | PU/PD                         |           |                                  | No                     |
| F12                | DDR_VREF0     | DDR_VREF0       |                 | A        |                            |                                          | 0.5*VDDS_DDR                | VDDS_DDR  |          | DDR                 |                               |           |                                  | No                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]     | SIGNAL NAME [3]               | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9]     | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-------------------|-------------------------------|--------------|----------|----------------------|------------------------------|-----------------------|---------------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| F15             | DDR_VREF_ZQ       | DDR_VREF_ZQ                   |              | A        |                      |                              |                       | VDDS_DDR      |          | DDR              |                         |           |                           | No                  |
| F13             | DDR_VTP           | DDR_VTP                       |              | A        |                      |                              | 1.1 V/1.2 V/1.35 V    | VDDS_DDR      |          | DDR              |                         |           |                           | No                  |
| D21             | ECAP0_IN_APWM_OUT | ECAP0_IN_APWM_OUT             | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0       | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | SYNC0_OUT                     | 1            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                   | CPTS0_RFT_CLK                 | 2            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | GPIO1_86                      | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AA2             | EMU0              | EMU0                          | 0            | IO       | PU                   | 0                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   |           | 1/1                       | Yes                 |
| AA1             | EMU1              | EMU1                          | 0            | IO       | PU                   | 0                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   |           | 1/1                       | Yes                 |
| A22             | EXT_REFCLK1       | EXT_REFCLK1                   | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0       | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | SYNC1_OUT                     | 1            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                   | GPIO1_87                      | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| P25             | GPMC0_ADVn_ALE    | GPMC0_ADVn_ALE                | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2       | Yes      | LVCMOS           | PU/PD                   |           | 1/1                       | Yes                 |
|                 |                   | VOUT1_DATA17                  | 1            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                   | GPIO0_17                      | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | BOOTMODE16                    | Bootstrap    | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| R28             | GPMC0_CLK         | GPMC0_CLK                     | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2       | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | VOUT1_DATA16                  | 1            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                   | VIN0_PCLK                     | 2            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | GPMC0_FCLK_MUX                | 3            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                   | GPIO0_16                      | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| T24             | GPMC0_DIR         | GPMC0_DIR                     | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2       | Yes      | LVCMOS           | PU/PD                   |           | 0/1                       | Yes                 |
|                 |                   | VOUT1_HSYNC                   | 1            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                   | VIN0_DATA8                    | 2            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | PRG2_PWM1_B0                  | 3            | IO       |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |                   | PRG2_IEP1_EDC_SYNC_OUT0       | 4            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                   | TIMER_IO6                     | 5            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | PRG2_IEP0_EDIO_DATA_IN_OUT2 9 | 6            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | GPIO0_25                      | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| P26             | GPMC0_OEn_REn     | GPMC0_OEn_REn                 | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2       | Yes      | LVCMOS           | PU/PD                   |           | 1/1                       | Yes                 |
|                 |                   | VOUT1_DATA18                  | 1            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                   | GPIO0_18                      | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | BOOTMODE17                    | Bootstrap    | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |



Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| U28             | GPMC0_WEn     | GPMC0_WEn       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                   |           | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA19    | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |               | GPIO0_19        | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | BOOTMODE18      | Bootstrap    | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| T25             | GPMC0_WPn     | GPMC0_WPn       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                   |           | 0/1                       | Yes                 |
|                 |               | VOUT1_VSYNC     | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |               | GPIO0_24        | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| M27             | GPMC0_AD0     | GPMC0_AD0       | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA0     | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |               | VIN0_DATA12     | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | GPIO0_0         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | BOOTMODE00      | Bootstrap    | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| M23             | GPMC0_AD1     | GPMC0_AD1       | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA1     | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |               | VIN0_DATA13     | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | GPIO0_1         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | BOOTMODE01      | Bootstrap    | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| M28             | GPMC0_AD2     | GPMC0_AD2       | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA2     | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |               | VIN0_DATA14     | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | GPIO0_2         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | BOOTMODE02      | Bootstrap    | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| M24             | GPMC0_AD3     | GPMC0_AD3       | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA3     | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |               | VIN0_DATA15     | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | GPIO0_3         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | BOOTMODE03      | Bootstrap    | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| N24             | GPMC0_AD4     | GPMC0_AD4       | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA4     | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |               | GPIO0_4         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | BOOTMODE04      | Bootstrap    | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| N27             | GPMC0_AD5     | GPMC0_AD5       | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA5     | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |               | GPIO0_5         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | BOOTMODE05      | Bootstrap    | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| N28             | GPMC0_AD6     | GPMC0_AD6       | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA6     | 1            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |               | GPIO0_6         | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | BOOTMODE06      | Bootstrap    | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| M25             | GPMC0_AD7     | GPMC0_AD7       | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA7     | 1            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |               | GPIO0_7         | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | BOOTMODE07      | Bootstrap    | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| N23             | GPMC0_AD8     | GPMC0_AD8       | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA8     | 1            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |               | VIN0_DATA0      | 2            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU0_GPO12 | 3            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU0_GPI12 | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PWM2_A0    | 5            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | GPIO0_8         | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | BOOTMODE08      | Bootstrap    | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| M26             | GPMC0_AD9     | GPMC0_AD9       | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA9     | 1            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |               | VIN0_DATA1      | 2            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU0_GPO13 | 3            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU0_GPI13 | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PWM2_B0    | 5            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                           |                     |
|                 |               | GPIO0_9         | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | BOOTMODE09      | Bootstrap    | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| P28             | GPMC0_AD10    | GPMC0_AD10      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA10    | 1            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |               | VIN0_DATA2      | 2            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU0_GPO14 | 3            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU0_GPI14 | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PWM0_TZ_IN | 6            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | GPIO0_10        | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | BOOTMODE10      | Bootstrap    | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3]  | MUXMODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|---------------|------------------|-------------|----------|----------------------|-----------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| P27             | GPMC0_AD11    | GPMC0_AD11       | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA11     | 1           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |               | VIN0_DATA3       | 2           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU0_GPO15  | 3           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU0_GPI15  | 4           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PWM2_A1     | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | GPIO0_11         | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | BOOTMODE11       | Bootstrap   | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| N26             | GPMC0_AD12    | GPMC0_AD12       | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA12     | 1           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |               | VIN0_DATA4       | 2           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU1_GPO12  | 3           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU1_GPI12  | 4           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PWM2_B1     | 5           | IO       |                      |                             |                       |           |          |                  |                        | 1         |                           |                     |
|                 |               | GPIO0_12         | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | BOOTMODE12       | Bootstrap   | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| N25             | GPMC0_AD13    | GPMC0_AD13       | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA13     | 1           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |               | VIN0_DATA5       | 2           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU1_GPO13  | 3           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU1_GPI13  | 4           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PWM2_A2     | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | GPIO0_13         | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | BOOTMODE13       | Bootstrap   | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| P24             | GPMC0_AD14    | GPMC0_AD14       | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 0         | 1/1                       | Yes                 |
|                 |               | VOUT1_DATA14     | 1           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |               | VIN0_DATA6       | 2           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU1_GPO14  | 3           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PRU1_GPI14  | 4           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_PWM0_TZ_OUT | 6           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |               | GPIO0_14         | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |               | BOOTMODE14       | Bootstrap   | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]  | SIGNAL NAME [3]  | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABL E [14] | IO Daisy Chain [15] |
|-----------------|----------------|------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|----------------------------|---------------------|
| R27             | GPMC0_AD15     | GPMC0_AD15       | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                        | Yes                 |
|                 |                | VOUT1_DATA15     | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                            |                     |
|                 |                | VIN0_DATA7       | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                | PRG2_PRU1_GPO15  | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                | PRG2_PRU1_GPI15  | 4            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                | PRG2_PWM2_B2     | 5            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                            |                     |
|                 |                | GPIO0_15         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                | BOOTMODE15       | Bootstrap    | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
| T28             | GPMC0_BE0n_CLE | GPMC0_BE0n_CLE   | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                   |           | 0/1                        | Yes                 |
|                 |                | VOUT1_DATA20     | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                            |                     |
|                 |                | GPIO0_20         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
| P23             | GPMC0_BE1n     | GPMC0_BE1n       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                   |           | 0/1                        | Yes                 |
|                 |                | VOUT1_DATA21     | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                            |                     |
|                 |                | VIN0_HD          | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                | PRG2_PRU0_GPO17  | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                | PRG2_PRU0_GPI17  | 4            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                | TIMER_IO2        | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                | PRG2_PWM2_TZ_IN  | 6            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                | GPIO0_21         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
| R24             | GPMC0_CSn0     | GPMC0_CSn0       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                   |           | 0/1                        | Yes                 |
|                 |                | VOUT1_PCLK       | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                            |                     |
|                 |                | GPIO0_26         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
| T23             | GPMC0_CSn1     | GPMC0_CSn1       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                   |           | 0/1                        | Yes                 |
|                 |                | VOUT1_DE         | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                            |                     |
|                 |                | VIN0_DATA9       | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                | PRG2_PRU1_GPO17  | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                | PRG2_PRU1_GPI17  | 4            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                | TIMER_IO7        | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                | PRG2_PWM2_TZ_OUT | 6            | O        |                      |                              |                       |           |          |                  |                         |           |                            |                     |
|                 |                | GPIO0_27         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]           | SIGNAL NAME [3]               | MUXMODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]    | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-------------------------|-------------------------------|-------------|----------|----------------------|-----------------------------|-----------------------|--------------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| R25             | GPMC0_CS <sub>n</sub> 2 | GPMC0_CS <sub>n</sub> 2       | 0           | O        | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV2      | Yes      | LVCMOS           | PU/PD                   |           | 0/1                       | Yes                 |
|                 |                         | VOUT1_EXTCLKIN                | 1           | I        |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
|                 |                         | VIN0_DATA10                   | 2           | I        |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
|                 |                         | GPMC0_A27                     | 3           | OZ       |                      |                             |                       |              |          |                  |                         |           |                           |                     |
|                 |                         | PRG2_IEP1_EDC_LATCH_IN1       | 4           | I        |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
|                 |                         | I2C2_SDA                      | 5           | IOD      |                      |                             |                       |              |          |                  |                         | 1         |                           |                     |
|                 |                         | PRG2_IEP0_EDIO_DATA_IN_OUT3 0 | 6           | IO       |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
|                 |                         | GPIO0_28                      | 7           | IO       |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
| T27             | GPMC0_CS <sub>n</sub> 3 | GPMC0_CS <sub>n</sub> 3       | 0           | O        | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV2      | Yes      | LVCMOS           | PU/PD                   |           | 0/1                       | Yes                 |
|                 |                         | VIN0_DATA11                   | 2           | I        |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
|                 |                         | GPMC0_A26                     | 3           | OZ       |                      |                             |                       |              |          |                  |                         |           |                           |                     |
|                 |                         | PRG2_IEP1_EDC_SYNC_OUT1       | 4           | O        |                      |                             |                       |              |          |                  |                         |           |                           |                     |
|                 |                         | I2C2_SCL                      | 5           | IOD      |                      |                             |                       |              |          |                  |                         | 1         |                           |                     |
|                 |                         | PRG2_IEP0_EDIO_DATA_IN_OUT3 1 | 6           | IO       |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
|                 |                         | GPIO0_29                      | 7           | IO       |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
| R26             | GPMC0_WAIT0             | GPMC0_WAIT0                   | 0           | I        | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV2      | Yes      | LVCMOS           | PU/PD                   | 1         | 0/1                       | Yes                 |
|                 |                         | VOUT1_DATA22                  | 1           | O        |                      |                             |                       |              |          |                  |                         |           |                           |                     |
|                 |                         | GPIO0_22                      | 7           | IO       |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
| R23             | GPMC0_WAIT1             | GPMC0_WAIT1                   | 0           | I        | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV2      | Yes      | LVCMOS           | PU/PD                   | 1         | 0/1                       | Yes                 |
|                 |                         | VOUT1_DATA23                  | 1           | O        |                      |                             |                       |              |          |                  |                         |           |                           |                     |
|                 |                         | VIN0_VD                       | 2           | I        |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
|                 |                         | PRG2_PWM1_A0                  | 3           | IO       |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
|                 |                         | PRG2_IEP1_EDC_LATCH_IN0       | 4           | I        |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
|                 |                         | TIMER_IO3                     | 5           | IO       |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
|                 |                         | PRG2_IEP0_EDIO_DATA_IN_OUT2 8 | 6           | IO       |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
|                 |                         | GPIO0_23                      | 7           | IO       |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
| D20             | I2C0_SCL                | I2C0_SCL                      | 0           | IOD      | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV0      | Yes      | LVCMOS-FS        | PU/PD                   | 1         | 1/1                       | Yes                 |
| C21             | I2C0_SDA                | I2C0_SDA                      | 0           | IOD      | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV0      | Yes      | LVCMOS-FS        | PU/PD                   | 1         | 1/1                       | Yes                 |
| B21             | I2C1_SCL                | I2C1_SCL                      | 0           | IOD      | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV0      | Yes      | LVCMOS-FS        | PU/PD                   | 1         | 1/1                       | Yes                 |
|                 |                         | CPTS0_HW1TSPUSH               | 1           | I        |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
| E21             | I2C1_SDA                | I2C1_SDA                      | 0           | IOD      | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV0      | Yes      | LVCMOS-FS        | PU/PD                   | 1         | 1/1                       | Yes                 |
|                 |                         | CPTS0_HW2TSPUSH               | 1           | I        |                      |                             |                       |              |          |                  |                         | 0         |                           |                     |
| K2              | MCU_ADC0_REFN           | MCU_ADC0_REFN                 |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                         |           |                           | No                  |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]    | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|---------------|-----------------|-------------|----------|----------------------|-----------------------------|-----------------------|--------------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| K3              | MCU_ADC0_REFP | MCU_ADC0_REFP   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| H3              | MCU_ADC1_REFN | MCU_ADC1_REFN   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| H2              | MCU_ADC1_REFP | MCU_ADC1_REFP   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| K5              | MCU_ADC0_AIN0 | MCU_ADC0_AIN0   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| J3              | MCU_ADC0_AIN1 | MCU_ADC0_AIN1   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| J1              | MCU_ADC0_AIN2 | MCU_ADC0_AIN2   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| J5              | MCU_ADC0_AIN3 | MCU_ADC0_AIN3   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| K4              | MCU_ADC0_AIN4 | MCU_ADC0_AIN4   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| J4              | MCU_ADC0_AIN5 | MCU_ADC0_AIN5   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| J2              | MCU_ADC0_AIN6 | MCU_ADC0_AIN6   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| J6              | MCU_ADC0_AIN7 | MCU_ADC0_AIN7   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| F4              | MCU_ADC1_AIN0 | MCU_ADC1_AIN0   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| G6              | MCU_ADC1_AIN1 | MCU_ADC1_AIN1   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| G4              | MCU_ADC1_AIN2 | MCU_ADC1_AIN2   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| H5              | MCU_ADC1_AIN3 | MCU_ADC1_AIN3   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| F5              | MCU_ADC1_AIN4 | MCU_ADC1_AIN4   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| G5              | MCU_ADC1_AIN5 | MCU_ADC1_AIN5   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| G3              | MCU_ADC1_AIN6 | MCU_ADC1_AIN6   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| H4              | MCU_ADC1_AIN7 | MCU_ADC1_AIN7   |             | A        |                      |                             | 1.8 V                 | VDDA_ADC_MCU |          | Analog           |                        |           |                           | No                  |
| V5              | MCU_BYP_POR   | MCU_BYP_POR     |             | I        | OFF                  |                             | 1.8 V/3.3 V           | VDDSHV0_WKUP | Yes      | LVC MOS          |                        |           |                           | No                  |
| AD8             | MCU_I2C0_SCL  | MCU_I2C0_SCL    | 0           | IOD      | OFF                  | 0                           | 1.8 V/3.3 V           | VDDSHV0_WKUP | Yes      | I2C OPEN DRAIN   |                        | 1         | 1/0                       | Yes                 |
| AD7             | MCU_I2C0_SDA  | MCU_I2C0_SDA    | 0           | IOD      | OFF                  | 0                           | 1.8 V/3.3 V           | VDDSHV0_WKUP | Yes      | I2C OPEN DRAIN   |                        | 1         | 1/0                       | Yes                 |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]              | SIGNAL NAME [3]                  | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9]     | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|----------------------------|----------------------------------|--------------|----------|----------------------|------------------------------|-----------------------|---------------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| W2              | MCU_MCAN0_RX               | MCU_MCAN0_RX                     | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                            | WKUP_GPIO0_55                    | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| W1              | MCU_MCAN0_TX               | MCU_MCAN0_TX                     | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                            | WKUP_GPIO0_54                    | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| L1              | MCU_MDIO0_MDC              | MCU_MDIO0_MDC                    | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                            | WKUP_GPIO0_47                    | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| L4              | MCU_MDIO0_MDIO             | MCU_MDIO0_MDIO                   | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                            | WKUP_GPIO0_46                    | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| V1              | MCU_OSPI0_CLK              | MCU_OSPI0_CLK                    | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                            | MCU_HYPERBUS0_CK                 | 1            | O        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                            | WKUP_GPIO0_12                    | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| U2              | MCU_OSPI0_DQS              | MCU_OSPI0_DQS                    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                            | MCU_HYPERBUS0_RWDS               | 1            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                            | WKUP_GPIO0_14                    | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| U1              | MCU_OSPI0_LBCLKO           | MCU_OSPI0_LBCLKO                 | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                            | MCU_HYPERBUS0_CK <sub>n</sub>    | 1            | O        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                            | WKUP_GPIO0_13                    | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| T1              | MCU_OSPI1_CLK              | MCU_OSPI1_CLK                    | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                            | WKUP_GPIO0_25                    | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| P2              | MCU_OSPI1_DQS              | MCU_OSPI1_DQS                    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                            | MCU_OSPI0_CS <sub>n3</sub>       | 1            | O        |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |                            | MCU_HYPERBUS0_INT <sub>n</sub>   | 2            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                            | WKUP_GPIO0_27                    | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| R1              | MCU_OSPI1_LBCLKO           | MCU_OSPI1_LBCLKO                 | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                            | MCU_OSPI0_CS <sub>n2</sub>       | 1            | O        |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |                            | MCU_HYPERBUS0_RESE <sub>Tn</sub> | 2            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                            | WKUP_GPIO0_26                    | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| R4              | MCU_OSPI0_CS <sub>n0</sub> | MCU_OSPI0_CS <sub>n0</sub>       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                            | MCU_HYPERBUS0_CS <sub>n0</sub>   | 1            | O        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                            | WKUP_GPIO0_23                    | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| R5              | MCU_OSPI0_CS <sub>n1</sub> | MCU_OSPI0_CS <sub>n1</sub>       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                            | MCU_HYPERBUS0_RESE <sub>Tn</sub> | 1            | O        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                            | WKUP_GPIO0_24                    | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| U4              | MCU_OSPI0_D0               | MCU_OSPI0_D0                     | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                            | MCU_HYPERBUS0_DQ0                | 1            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                            | WKUP_GPIO0_15                    | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3]   | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9]     | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|---------------|-------------------|--------------|----------|----------------------|------------------------------|-----------------------|---------------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| U5              | MCU_OSPI0_D1  | MCU_OSPI0_D1      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |               | MCU_HYPERBUS0_DQ1 | 1            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_16     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| T2              | MCU_OSPI0_D2  | MCU_OSPI0_D2      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |               | MCU_HYPERBUS0_DQ2 | 1            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_17     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| T3              | MCU_OSPI0_D3  | MCU_OSPI0_D3      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |               | MCU_HYPERBUS0_DQ3 | 1            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_18     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| T4              | MCU_OSPI0_D4  | MCU_OSPI0_D4      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |               | MCU_HYPERBUS0_DQ4 | 1            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_19     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| T5              | MCU_OSPI0_D5  | MCU_OSPI0_D5      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |               | MCU_HYPERBUS0_DQ5 | 1            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_20     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| R2              | MCU_OSPI0_D6  | MCU_OSPI0_D6      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |               | MCU_HYPERBUS0_DQ6 | 1            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_21     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| R3              | MCU_OSPI0_D7  | MCU_OSPI0_D7      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |               | MCU_HYPERBUS0_DQ7 | 1            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_22     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| N2              | MCU_OSPI1_CS0 | MCU_OSPI1_CS0     | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
| N3              | MCU_OSPI1_CS1 | MCU_OSPI1_CS1     | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |               | MCU_HYPERBUS0_WPn | 1            | O        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | MCU_TIMER_IO0     | 2            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | MCU_HYPERBUS0_CS1 | 3            | O        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | MCU_UART0_RTSn    | 4            | O        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | MCU_SPI0_CS2      | 5            | IO       |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |               | WKUP_GPIO0_33     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| P3              | MCU_OSPI1_D0  | MCU_OSPI1_D0      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |               | WKUP_GPIO0_28     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| P4              | MCU_OSPI1_D1  | MCU_OSPI1_D1      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |               | MCU_UART0_RXD     | 4            | I        |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |               | MCU_SPI1_CS1      | 5            | IO       |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |               | WKUP_GPIO0_29     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |



**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]     | SIGNAL NAME [3]   | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9]     | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-------------------|-------------------|--------------|----------|----------------------|------------------------------|-----------------------|---------------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| P5              | MCU_OSPI1_D2      | MCU_OSPI1_D2      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | MCU_UART0_TXD     | 4            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                   | MCU_SPI1_CS2      | 5            | IO       |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |                   | WKUP_GPIO0_30     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| P1              | MCU_OSPI1_D3      | MCU_OSPI1_D3      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | MCU_UART0_CTSn    | 4            | I        |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |                   | MCU_SPI0_CS1      | 5            | IO       |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |                   | WKUP_GPIO0_31     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| W5              | MCU_PORz          | MCU_PORz          |              | I        | OFF                  |                              | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           |                         |           |                           | No                  |
| V2              | MCU_PORz_OUT      | MCU_PORz_OUT      | 0            | O        | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   |           | 0/0                       | No                  |
| V3              | MCU_RESETSTATz    | MCU_RESETSTATz    | 0            | O        | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   |           | 0/0                       | No                  |
| W4              | MCU_RESETz        | MCU_RESETz        | 0            | I        | PU                   | 0                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   |           | 1/1                       | No                  |
| M1              | MCU_RGMII1_RXC    | MCU_RGMII1_RXC    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | MCU_RMII1_REF_CLK | 1            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | WKUP_GPIO0_41     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| N5              | MCU_RGMII1_RX_CTL | MCU_RGMII1_RX_CTL | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | MCU_RMII1_RX_ER   | 1            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | WKUP_GPIO0_35     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| N1              | MCU_RGMII1_TXC    | MCU_RGMII1_TXC    | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | MCU_RMII1_TX_EN   | 1            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                   | WKUP_GPIO0_40     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| N4              | MCU_RGMII1_TX_CTL | MCU_RGMII1_TX_CTL | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   |           | 0/1                       | Yes                 |
|                 |                   | MCU_RMII1_CRSDV   | 1            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | WKUP_GPIO0_34     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| L6              | MCU_RGMII1_RD0    | MCU_RGMII1_RD0    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | MCU_RMII1_RXD0    | 1            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | WKUP_GPIO0_45     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| M6              | MCU_RGMII1_RD1    | MCU_RGMII1_RD1    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | MCU_RMII1_RXD1    | 1            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | WKUP_GPIO0_44     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| L5              | MCU_RGMII1_RD2    | MCU_RGMII1_RD2    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | WKUP_GPIO0_43     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| L2              | MCU_RGMII1_RD3    | MCU_RGMII1_RD3    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | WKUP_GPIO0_42     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]     | SIGNAL NAME [3]         | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9]     | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-------------------|-------------------------|--------------|----------|----------------------|------------------------------|-----------------------|---------------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| M5              | MCU_RGMII1_TD0    | MCU_RGMII1_TD0          | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   |           | 0/1                       | Yes                 |
|                 |                   | MCU_RMII1_TXD0          | 1            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                   | WKUP_GPIO0_39           | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| M4              | MCU_RGMII1_TD1    | MCU_RGMII1_TD1          | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   |           | 0/1                       | Yes                 |
|                 |                   | MCU_RMII1_TXD1          | 1            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                   | WKUP_GPIO0_38           | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| M3              | MCU_RGMII1_TD2    | MCU_RGMII1_TD2          | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   |           | 0/1                       | Yes                 |
|                 |                   | WKUP_GPIO0_37           | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| M2              | MCU_RGMII1_TD3    | MCU_RGMII1_TD3          | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_WK UP | Yes      | LVCMOS           | PU/PD                   |           | 0/1                       | Yes                 |
|                 |                   | WKUP_GPIO0_36           | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| W3              | MCU_SAFETY_ERRORn | MCU_SAFETY_ERRORn       | 0            | IO       | PD                   | 0                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   |           | 1/0                       | No                  |
| Y1              | MCU_SPI0_CLK      | MCU_SPI0_CLK            | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |                   | WKUP_GPIO0_48           | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | MCU_BOOTMODE06          | Bootstrap    | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| Y4              | MCU_SPI0_CS0      | MCU_SPI0_CS0            | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 1         | 0/1                       | Yes                 |
|                 |                   | WKUP_GPIO0_51           | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| Y3              | MCU_SPI0_D0       | MCU_SPI0_D0             | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |                   | WKUP_GPIO0_49           | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | MCU_BOOTMODE07          | Bootstrap    | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| Y2              | MCU_SPI0_D1       | MCU_SPI0_D1             | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |                   | WKUP_GPIO0_50           | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                   | MCU_BOOTMODE05          | Bootstrap    | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| B25             | MMC0_CLK          | MMC0_CLK                | 0            | O        | PD                   | 7                            | 1.8 V/3.3 V           | VDDSHV6       |          | LVCMOS           |                         | 1         |                           | No                  |
|                 |                   | GPIO1_10                | 7            | O        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| B27             | MMC0_CMD          | MMC0_CMD                | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV6       |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |                   | GPIO1_11                | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| C25             | MMC0_DS           | MMC0_DS                 | 0            | I        | PD                   | 7                            | 1.8 V/3.3 V           | VDDSHV6       |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |                   | GPIO1_12                | 7            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| A23             | MMC0_SDCD         | MMC0_SDCD               | 0            | I        | OFF                  | 7                            | 1.8 V                 | VDDS_OSC1     | Yes      | LVCMOS           | PU/PD                   | 1         | 0/1                       | Yes                 |
|                 |                   | PRG2_IEP0_EDIO_OUTVALID | 6            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                   | GPIO1_13                | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| B23             | MMC0_SDWP         | MMC0_SDWP               | 0            | I        | OFF                  | 7                            | 1.8 V                 | VDDS_OSC1     | Yes      | LVCMOS           | PU/PD                   | 1         | 0/1                       | Yes                 |
|                 |                   | GPIO1_14                | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| C27             | MMC1_CLK          | MMC1_CLK                | 0            | O        | PD                   | 7                            | 1.8 V/3.3 V           | VDDSHV7       |          | LVCMOS           |                         | 1         |                           | No                  |
|                 |                   | GPIO1_77                | 7            | O        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| C28             | MMC1_CMD      | MMC1_CMD        | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV7   |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |               | GPIO1_78        | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| B24             | MMC1_SDCD     | MMC1_SDCD       | 0            | I        | OFF                  | 7                            | 1.8 V                 | VDDS_OSC1 | Yes      | LVCMOS           | PU/PD                   | 1         | 0/1                       | Yes                 |
|                 |               | GPIO1_79        | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| C24             | MMC1_SDWP     | MMC1_SDWP       | 0            | I        | OFF                  | 7                            | 1.8 V                 | VDDS_OSC1 | Yes      | LVCMOS           | PU/PD                   | 1         | 0/1                       | Yes                 |
|                 |               | GPIO1_80        | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| A26             | MMC0_DAT0     | MMC0_DAT0       | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV6   |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |               | GPIO1_9         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| E25             | MMC0_DAT1     | MMC0_DAT1       | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV6   |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |               | GPIO1_8         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| C26             | MMC0_DAT2     | MMC0_DAT2       | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV6   |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |               | GPIO1_7         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| A25             | MMC0_DAT3     | MMC0_DAT3       | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV6   |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |               | GPIO1_6         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| E24             | MMC0_DAT4     | MMC0_DAT4       | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV6   |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |               | UART0_RIN       | 1            | I        |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |               | EQEP2_S         | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | GPIO1_5         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| A24             | MMC0_DAT5     | MMC0_DAT5       | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV6   |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |               | UART0_DTRn      | 1            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |               | EQEP2_I         | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | GPIO1_4         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| B26             | MMC0_DAT6     | MMC0_DAT6       | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV6   |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |               | UART0_DSRn      | 1            | I        |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |               | EQEP2_B         | 5            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | GPIO1_3         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| D25             | MMC0_DAT7     | MMC0_DAT7       | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV6   |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |               | UART0_DCDn      | 1            | I        |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |               | EQEP2_A         | 5            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |               | GPIO1_2         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| D28             | MMC1_DAT0     | MMC1_DAT0       | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV7   |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |               | GPIO1_76        | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| E27             | MMC1_DAT1     | MMC1_DAT1       | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV7   |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |               | GPIO1_75        | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| D26             | MMC1_DAT2     | MMC1_DAT2       | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV7   |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |               | GPIO1_74        | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3] | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9]       | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-----------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| D27             | MMC1_DAT3       | MMC1_DAT3       | 0            | IO       | PU                   | 7                            | 1.8 V/3.3 V           | VDDSHV7         |          | LVCMOS           | PU/PD                   | 1         |                           | No                  |
|                 |                 | GPIO1_73        | 7            | IO       |                      |                              |                       |                 |          |                  |                         | 0         |                           |                     |
| F18             | NMIIn           | NMIIn           | 0            | I        | PU                   | 0                            | 1.8 V/3.3 V           | VDDSHV0         | Yes      | LVCMOS-FS        | PU/PD                   | 1         | 1/1                       | Yes                 |
|                 |                 | PRG2_PWM1_TZ_IN | 6            | I        |                      |                              |                       |                 |          |                  |                         | 0         |                           |                     |
| L25             | OLDI0_CLKN      | OLDI0_CLKN      |              | IO       | OFF                  |                              | 1.8 V                 | VDDA_1P8_O LDIO |          | OLDI_LVD S       |                         |           |                           | No                  |
| K25             | OLDI0_CLKP      | OLDI0_CLKP      |              | IO       | OFF                  |                              | 1.8 V                 | VDDA_1P8_O LDIO |          | OLDI_LVD S       |                         |           |                           | No                  |
| J28             | OLDI0_A0N       | OLDI0_A0N       |              | IO       | OFF                  |                              | 1.8 V                 | VDDA_1P8_O LDIO |          | OLDI_LVD S       |                         |           |                           | No                  |
| K28             | OLDI0_A0P       | OLDI0_A0P       |              | IO       | OFF                  |                              | 1.8 V                 | VDDA_1P8_O LDIO |          | OLDI_LVD S       |                         |           |                           | No                  |
| L27             | OLDI0_A1N       | OLDI0_A1N       |              | IO       | OFF                  |                              | 1.8 V                 | VDDA_1P8_O LDIO |          | OLDI_LVD S       |                         |           |                           | No                  |
| K27             | OLDI0_A1P       | OLDI0_A1P       |              | IO       | OFF                  |                              | 1.8 V                 | VDDA_1P8_O LDIO |          | OLDI_LVD S       |                         |           |                           | No                  |
| K24             | OLDI0_A2N       | OLDI0_A2N       |              | IO       | OFF                  |                              | 1.8 V                 | VDDA_1P8_O LDIO |          | OLDI_LVD S       |                         |           |                           | No                  |
| J24             | OLDI0_A2P       | OLDI0_A2P       |              | IO       | OFF                  |                              | 1.8 V                 | VDDA_1P8_O LDIO |          | OLDI_LVD S       |                         |           |                           | No                  |
| J26             | OLDI0_A3N       | OLDI0_A3N       |              | IO       | OFF                  |                              | 1.8 V                 | VDDA_1P8_O LDIO |          | OLDI_LVD S       |                         |           |                           | No                  |
| K26             | OLDI0_A3P       | OLDI0_A3P       |              | IO       | OFF                  |                              | 1.8 V                 | VDDA_1P8_O LDIO |          | OLDI_LVD S       |                         |           |                           | No                  |
| C22             | OSC1_XI         | OSC1_XI         |              | I        | OFF                  |                              | 1.8 V                 | VDDS_OSC1       |          | Analog           |                         |           |                           | No                  |
| E22             | OSC1_XO         | OSC1_XO         |              | O        | OFF                  |                              | 1.8 V                 | VDDS_OSC1       |          | Analog           |                         |           |                           | No                  |
| Y5              | PMIC_POWER_EN0  | PMIC_POWER_EN0  | 0            | O        | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_WK UP   | Yes      | LVCMOS           | PU/PD                   |           | 0/0                       | No                  |
| AA5             | PMIC_POWER_EN1  | PMIC_POWER_EN1  | 0            | O        | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_WK UP   | Yes      | LVCMOS           | PU/PD                   |           | 0/0                       | No                  |
| E19             | PORz            | PORz            | 0            | I        | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0         | Yes      | LVCMOS           |                         |           |                           | Yes                 |
| C19             | PORz_OUT        | PORz_OUT        | 0            | O        | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0         | Yes      | LVCMOS           | PU/PD                   |           | 0/0                       | Yes                 |
| AE28            | PRG0_MDIO0_MDC  | PRG0_MDIO0_MDC  | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3         | Yes      | LVCMOS           | PU/PD                   |           | 0/1                       | Yes                 |
|                 |                 | PRG2_PWM1_B2    | 3            | IO       |                      |                              |                       |                 |          |                  |                         | 1         |                           |                     |
|                 |                 | MCASP2_AXR3     | 5            | IO       |                      |                              |                       |                 |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO1_70        | 7            | IO       |                      |                              |                       |                 |          |                  |                         | 0         |                           |                     |
| AE26            | PRG0_MDIO0_MDIO | PRG0_MDIO0_MDIO | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3         | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PWM1_A2    | 3            | IO       |                      |                              |                       |                 |          |                  |                         | 0         |                           |                     |
|                 |                 | MCASP2_AXR2     | 5            | IO       |                      |                              |                       |                 |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO1_69        | 7            | IO       |                      |                              |                       |                 |          |                  |                         | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]  | SIGNAL NAME [3]    | MUXMODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|----------------|--------------------|-------------|----------|----------------------|-----------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| V24             | PRG0_PRU0_GPO0 | PRG0_PRU0_GPO0     | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                | PRG0_PRU0_GPI0     | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG0_RGMII1_RD0    | 2           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG0_PWM3_A0       | 3           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | MCASP0_ACLKX       | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | GPIO1_29           | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| W25             | PRG0_PRU0_GPO1 | PRG0_PRU0_GPO1     | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                | PRG0_PRU0_GPI1     | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG0_RGMII1_RD1    | 2           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG0_PWM3_B0       | 3           | IO       |                      |                             |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                | MCASP0_AFSX        | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | GPIO1_30           | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| W24             | PRG0_PRU0_GPO2 | PRG0_PRU0_GPO2     | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                | PRG0_PRU0_GPI2     | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG0_RGMII1_RD2    | 2           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG0_PWM2_A0       | 3           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | MCASP0_ACLKR       | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | GPIO1_31           | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| AA27            | PRG0_PRU0_GPO3 | PRG0_PRU0_GPO3     | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                | PRG0_PRU0_GPI3     | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG0_RGMII1_RD3    | 2           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG0_PWM3_A2       | 3           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | MCASP0_AFSR        | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | GPIO1_32           | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| Y24             | PRG0_PRU0_GPO4 | PRG0_PRU0_GPO4     | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                | PRG0_PRU0_GPI4     | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG0_RGMII1_RX_CTL | 2           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG0_PWM2_B0       | 3           | IO       |                      |                             |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                | MCASP0_AXR0        | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | GPIO1_33           | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| V28             | PRG0_PRU0_GPO5 | PRG0_PRU0_GPO5     | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                | PRG0_PRU0_GPI5     | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG0_PWM3_B2       | 3           | IO       |                      |                             |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                | MCASP0_AXR1        | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | GPIO1_34           | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3]               | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-----------------|-------------------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| Y25             | PRG0_PRU0_GPO6  | PRG0_PRU0_GPO6                | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG0_PRU0_GPI6                | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG0_RGMII1_RXC               | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG0_PWM3_A1                  | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | MCASP0_AXR2                   | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO1_35                      | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| U27             | PRG0_PRU0_GPO7  | PRG0_PRU0_GPO7                | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG0_PRU0_GPI7                | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG0_IEP0_EDC_LATCH_IN1       | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG0_PWM3_B1                  | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | PRG0_ECAP0_SYNC_IN            | 4            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | MCASP0_AXR3                   | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO1_36                      | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| V27             | PRG0_PRU0_GPO8  | PRG0_PRU0_GPO8                | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG0_PRU0_GPI8                | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG0_PWM2_A1                  | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | MCASP0_AXR4                   | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO1_37                      | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| V26             | PRG0_PRU0_GPO9  | PRG0_PRU0_GPO9                | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG0_PRU0_GPI9                | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG0_UART0_CTSn               | 2            | I        |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | PRG0_PWM3_TZ_IN               | 3            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | SPI3_CS1                      | 4            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | MCASP0_AXR5                   | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG0_IEP0_EDIO_DATA_IN_OUT2 8 | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO1_38                      | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| U25             | PRG0_PRU0_GPO10 | PRG0_PRU0_GPO10               | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG0_PRU0_GPI10               | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG0_UART0_RTSn               | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG0_PWM2_B1                  | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | SPI3_CS2                      | 4            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | MCASP0_AXR6                   | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG0_IEP0_EDIO_DATA_IN_OUT2 9 | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO1_39                      | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER<br>[1] | BALL NAME [2]   | SIGNAL NAME [3]    | MUXMOD<br>E [4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET<br>REL.<br>MUXMOD<br>E [7] | I/O<br>VOLTAGE<br>VALUE [8] | POWER [9] | HYS [10] | BUFFER<br>TYPE [11] | PULL UP/<br>DOWN<br>TYPE [12] | DSIS [13] | RXACTIVE<br>/ TXDISABL<br>E [14] | IO Daisy<br>Chain [15] |
|--------------------|-----------------|--------------------|-----------------|----------|----------------------------|------------------------------------------|-----------------------------|-----------|----------|---------------------|-------------------------------|-----------|----------------------------------|------------------------|
| AB25               | PRG0_PRU0_GPO11 | PRG0_PRU0_GPO11    | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV3   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                 | PRG0_PRU0_GPI11    | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_RGMII1_TX_CTL | 2               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                 | PRG0_PWM3_TZ_OUT   | 3               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                 | PRG0_PRU0_GPO15    | 4               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | MCASP0_AXR7        | 5               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | GPIO1_40           | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
| AD27               | PRG0_PRU0_GPO12 | PRG0_PRU0_GPO12    | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV3   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                 | PRG0_PRU0_GPI12    | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_RGMII1_TD0    | 2               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                 | PRG0_PWM0_A0       | 3               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_PRU0_GPO11    | 4               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | MCASP0_AXR8        | 5               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | GPIO1_41           | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
| AC26               | PRG0_PRU0_GPO13 | PRG0_PRU0_GPO13    | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV3   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                 | PRG0_PRU0_GPI13    | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_RGMII1_TD1    | 2               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                 | PRG0_PWM0_B0       | 3               | IO       |                            |                                          |                             |           |          |                     |                               | 1         |                                  |                        |
|                    |                 | PRG0_PRU0_GPO12    | 4               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | MCASP0_AXR9        | 5               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | GPIO1_42           | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
| AD26               | PRG0_PRU0_GPO14 | PRG0_PRU0_GPO14    | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV3   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                 | PRG0_PRU0_GPI14    | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_RGMII1_TD2    | 2               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                 | PRG0_PWM0_A1       | 3               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_PRU0_GPO13    | 4               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | MCASP0_AXR10       | 5               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | GPIO1_43           | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
| AA24               | PRG0_PRU0_GPO15 | PRG0_PRU0_GPO15    | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV3   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                 | PRG0_PRU0_GPI15    | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_RGMII1_TD3    | 2               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                 | PRG0_PWM0_B1       | 3               | IO       |                            |                                          |                             |           |          |                     |                               | 1         |                                  |                        |
|                    |                 | PRG0_PRU0_GPO14    | 4               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | MCASP0_AXR11       | 5               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | GPIO1_44           | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3]         | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABL E [14] | IO Daisy Chain [15] |
|-----------------|-----------------|-------------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|----------------------------|---------------------|
| AD28            | PRG0_PRU0_GPO16 | PRG0_PRU0_GPO16         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                        | Yes                 |
|                 |                 | PRG0_PRU0_GPI16         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | PRG0_RGMII1_TXC         | 2            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | PRG0_PWM0_A2            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | MCASP0_AXR12            | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | MCASP1_AHCLKR           | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | GPIO1_45                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
| U26             | PRG0_PRU0_GPO17 | PRG0_PRU0_GPO17         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                        | Yes                 |
|                 |                 | PRG0_PRU0_GPI17         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | PRG0_IEP0_EDC_SYNC_OUT1 | 2            | O        |                      |                              |                       |           |          |                  |                         | 1         |                            |                     |
|                 |                 | PRG0_PWM0_B2            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | PRG0_ECAP0_SYNC_OUT     | 4            | O        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | MCASP0_AXR13            | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | MCASP1_AHCLKX           | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
| V25             | PRG0_PRU0_GPO18 | PRG0_PRU0_GPO18         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                        | Yes                 |
|                 |                 | PRG0_PRU0_GPI18         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | PRG0_IEP0_EDC_LATCH_IN0 | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | PRG0_PWM0_TZ_IN         | 3            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | PRG0_ECAP0_IN_APWM_OUT  | 4            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | MCASP0_AXR14            | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | MCASP2_AHCLKR           | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
| U24             | PRG0_PRU0_GPO19 | PRG0_PRU0_GPO19         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                        | Yes                 |
|                 |                 | PRG0_PRU0_GPI19         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | PRG0_IEP0_EDC_SYNC_OUT0 | 2            | O        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | PRG0_PWM0_TZ_OUT        | 3            | O        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | MCASP0_AXR15            | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | MCASP2_AHCLKX           | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | GPIO1_48                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
| AB28            | PRG0_PRU1_GPO0  | PRG0_PRU1_GPO0          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                        | Yes                 |
|                 |                 | PRG0_PRU1_GPI0          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | PRG0_RGMII2_RD0         | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | MCASP1_ACLKX            | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |
|                 |                 | GPIO1_49                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                            |                     |



**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]  | SIGNAL NAME [3]    | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|----------------|--------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| AC28            | PRG0_PRU1_GPO1 | PRG0_PRU1_GPO1     | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG0_PRU1_GPI1     | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG0_RGMII2_RD1    | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | MCASP1_AFSX        | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO1_50           | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AC27            | PRG0_PRU1_GPO2 | PRG0_PRU1_GPO2     | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG0_PRU1_GPI2     | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG0_RGMII2_RD2    | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG0_PWM2_A2       | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | MCASP1_ACLKR       | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO1_51           | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AB26            | PRG0_PRU1_GPO3 | PRG0_PRU1_GPO3     | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG0_PRU1_GPI3     | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG0_RGMII2_RD3    | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | EQEP0_A            | 4            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | MCASP1_AFSR        | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO1_52           | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AA25            | PRG0_PRU1_GPO4 | PRG0_PRU1_GPO4     | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG0_PRU1_GPI4     | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG0_RGMII2_RX_CTL | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG0_PWM2_B2       | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                | EQEP0_B            | 4            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | MCASP1_AXR0        | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | MCASP0_AHCLKR      | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO1_53           | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| U23             | PRG0_PRU1_GPO5 | PRG0_PRU1_GPO5     | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG0_PRU1_GPI5     | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | EQEP0_S            | 4            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | MCASP1_AXR1        | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | MCASP0_AHCLKX      | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO1_54           | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AB27            | PRG0_PRU1_GPO6 | PRG0_PRU1_GPO6     | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG0_PRU1_GPI6     | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG0_RGMII2_RXC    | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | MCASP1_AXR2        | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO1_55           | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3]               | MUXMODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-----------------|-------------------------------|-------------|----------|----------------------|-----------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| W28             | PRG0_PRU1_GPO7  | PRG0_PRU1_GPO7                | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG0_PRU1_GPI7                | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG0_IEP1_EDC_LATCH_IN1       | 2           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | SPI3_CS0                      | 4           | IO       |                      |                             |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                 | MCASP1_AXR3                   | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | UART2_TXD                     | 6           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | GPIO1_56                      | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| W27             | PRG0_PRU1_GPO8  | PRG0_PRU1_GPO8                | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG0_PRU1_GPI8                | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG0_PWM2_TZ_OUT              | 3           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | MCASP1_AXR4                   | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | GPIO1_57                      | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| Y28             | PRG0_PRU1_GPO9  | PRG0_PRU1_GPO9                | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG0_PRU1_GPI9                | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG0_UART0_RXD                | 2           | I        |                      |                             |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                 | SPI3_CS3                      | 4           | IO       |                      |                             |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                 | MCASP1_AXR5                   | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG0_IEP0_EDIO_DATA_IN_OUT3 0 | 6           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | GPIO1_58                      | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| AA28            | PRG0_PRU1_GPO10 | PRG0_PRU1_GPO10               | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG0_PRU1_GPI10               | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG0_UART0_TXD                | 2           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | PRG0_PWM2_TZ_IN               | 3           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | EQEP0_I                       | 4           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | MCASP1_AXR6                   | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG0_IEP0_EDIO_DATA_IN_OUT3 1 | 6           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | GPIO1_59                      | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| AB24            | PRG0_PRU1_GPO11 | PRG0_PRU1_GPO11               | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG0_PRU1_GPI11               | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG0_RGMII2_TX_CTL            | 2           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | PRG0_PRU1_GPO15               | 4           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | MCASP1_AXR7                   | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | GPIO1_60                      | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER<br>[1] | BALL NAME [2]   | SIGNAL NAME [3] | MUXMOD<br>E [4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET<br>REL.<br>MUXMOD<br>E [7] | I/O<br>VOLTAGE<br>VALUE [8] | POWER [9] | HYS [10] | BUFFER<br>TYPE [11] | PULL UP/<br>DOWN<br>TYPE [12] | DSIS [13] | RXACTIVE<br>/ TXDISABL<br>E [14] | IO Daisy<br>Chain [15] |
|--------------------|-----------------|-----------------|-----------------|----------|----------------------------|------------------------------------------|-----------------------------|-----------|----------|---------------------|-------------------------------|-----------|----------------------------------|------------------------|
| AC25               | PRG0_PRU1_GPO12 | PRG0_PRU1_GPO12 | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV3   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                 | PRG0_PRU1_GPI12 | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_RGMII2_TD0 | 2               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                 | PRG0_PWM1_A0    | 3               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_PRU1_GPO11 | 4               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | MCASP1_AXR8     | 5               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | GPIO1_61        | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
| AD25               | PRG0_PRU1_GPO13 | PRG0_PRU1_GPO13 | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV3   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                 | PRG0_PRU1_GPI13 | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_RGMII2_TD1 | 2               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                 | PRG0_PWM1_B0    | 3               | IO       |                            |                                          |                             |           |          |                     |                               | 1         |                                  |                        |
|                    |                 | PRG0_PRU1_GPO12 | 4               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | MCASP1_AXR9     | 5               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | GPIO1_62        | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
| AD24               | PRG0_PRU1_GPO14 | PRG0_PRU1_GPO14 | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV3   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                 | PRG0_PRU1_GPI14 | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_RGMII2_TD2 | 2               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                 | PRG0_PWM1_A1    | 3               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_PRU1_GPO13 | 4               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | MCASP2_AFSR     | 5               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | GPIO1_63        | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
| AE27               | PRG0_PRU1_GPO15 | PRG0_PRU1_GPO15 | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV3   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                 | PRG0_PRU1_GPI15 | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_RGMII2_TD3 | 2               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                 | PRG0_PWM1_B1    | 3               | IO       |                            |                                          |                             |           |          |                     |                               | 1         |                                  |                        |
|                    |                 | PRG0_PRU1_GPO14 | 4               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | MCASP2_ACLKR    | 5               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | GPIO1_64        | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
| AC24               | PRG0_PRU1_GPO16 | PRG0_PRU1_GPO16 | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV3   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                 | PRG0_PRU1_GPI16 | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_RGMII2_TXC | 2               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | PRG0_PWM1_A2    | 3               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | MCASP2_AXR0     | 5               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                 | GPIO1_65        | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3]         | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-----------------|-------------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| Y27             | PRG0_PRU1_GPO17 | PRG0_PRU1_GPO17         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG0_PRU1_GPI17         | 1            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG0_IEP1_EDC_SYNC_OUT1 | 2            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | PRG0_PWM1_B2            | 3            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                 | SPI3_CLK                | 4            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | MCASP2_AXR1             | 5            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | UART2_RXD               | 6            | I        |                      |                              |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                 | GPIO1_66                | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| Y26             | PRG0_PRU1_GPO18 | PRG0_PRU1_GPO18         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG0_PRU1_GPI18         | 1            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG0_IEP1_EDC_LATCH_IN0 | 2            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG0_PWM1_TZ_IN         | 3            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | SPI3_D0                 | 4            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | MCASP2_AFSX             | 5            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | UART2_CTSn              | 6            | I        |                      |                              |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                 | GPIO1_67                | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| W26             | PRG0_PRU1_GPO19 | PRG0_PRU1_GPO19         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV3   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG0_PRU1_GPI19         | 1            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG0_IEP1_EDC_SYNC_OUT0 | 2            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | PRG0_PWM1_TZ_OUT        | 3            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | SPI3_D1                 | 4            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | MCASP2_ACLKX            | 5            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | UART2_RTSn              | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | GPIO1_68                | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| AH18            | PRG1_MDIO0_MDC  | PRG1_MDIO0_MDC          | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                  |           | 0/1                       | Yes                 |
|                 |                 | SPI1_CS3                | 1            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                 | PRG2_PWM1_B1            | 3            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                 | GPIO1_1                 | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| AD18            | PRG1_MDIO0_MDIO | PRG1_MDIO0_MDIO         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | SPI1_CS2                | 1            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                 | PRG2_PWM1_A1            | 3            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | GPIO1_0                 | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| AE22            | PRG1_PRU0_GPO0  | PRG1_PRU0_GPO0          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU0_GPI0          | 1            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG1_RGMII1_RD0         | 2            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG1_PWM3_A0            | 3            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | GPIO0_56                | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]  | SIGNAL NAME [3]         | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|----------------|-------------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| AG24            | PRG1_PRU0_GPO1 | PRG1_PRU0_GPO1          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU0_GPI1          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_RGMII1_RD1         | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_PWM3_B0            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                | GPIO0_57                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AF23            | PRG1_PRU0_GPO2 | PRG1_PRU0_GPO2          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU0_GPI2          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_RGMII1_RD2         | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_PWM2_A0            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO0_58                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AD21            | PRG1_PRU0_GPO3 | PRG1_PRU0_GPO3          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU0_GPI3          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_RGMII1_RD3         | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_PWM3_A2            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO0_59                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AG23            | PRG1_PRU0_GPO4 | PRG1_PRU0_GPO4          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU0_GPI4          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_RGMII1_RX_CTL      | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_PWM2_B0            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                | GPIO0_60                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AF27            | PRG1_PRU0_GPO5 | PRG1_PRU0_GPO5          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU0_GPI5          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_PWM3_B2            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                | GPIO0_61                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AF22            | PRG1_PRU0_GPO6 | PRG1_PRU0_GPO6          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU0_GPI6          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_RGMII1_RXC         | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_PWM3_A1            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO0_62                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AG27            | PRG1_PRU0_GPO7 | PRG1_PRU0_GPO7          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU0_GPI7          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_IEP0_EDC_LATCH_IN1 | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_PWM3_B1            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                | GPIO0_63                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3]               | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-----------------|-------------------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| AF28            | PRG1_PRU0_GPO8  | PRG1_PRU0_GPO8                | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU0_GPI8                | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_PWM2_A1                  | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_64                      | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AF26            | PRG1_PRU0_GPO9  | PRG1_PRU0_GPO9                | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU0_GPI9                | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_UART0_CTSn               | 2            | I        |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | PRG1_PWM3_TZ_IN               | 3            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | SPI2_CS1                      | 4            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | PRG1_IEP0_EDIO_DATA_IN_OUT2 8 | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_65                      | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AH25            | PRG1_PRU0_GPO10 | PRG1_PRU0_GPO10               | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU0_GPI10               | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_UART0_RTSn               | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG1_PWM2_B1                  | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | SPI2_CS2                      | 4            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | PRG1_IEP0_EDIO_DATA_IN_OUT2 9 | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_66                      | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AF21            | PRG1_PRU0_GPO11 | PRG1_PRU0_GPO11               | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU0_GPI11               | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_RGMII1_TX_CTL            | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG1_PWM3_TZ_OUT              | 3            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG1_PRU0_GPO15               | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_67                      | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AH20            | PRG1_PRU0_GPO12 | PRG1_PRU0_GPO12               | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU0_GPI12               | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_RGMII1_TD0               | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG1_PWM0_A0                  | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_PRU0_GPO11               | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_68                      | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AH21            | PRG1_PRU0_GPO13 | PRG1_PRU0_GPO13               | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU0_GPI13               | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_RGMII1_TD1               | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG1_PWM0_B0                  | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | PRG1_PRU0_GPO12               | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_69                      | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3]         | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-----------------|-------------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| AG20            | PRG1_PRU0_GPO14 | PRG1_PRU0_GPO14         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU0_GPI14         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_RGMII1_TD2         | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG1_PWM0_A1            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_PRU0_GPO13         | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_70                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AD19            | PRG1_PRU0_GPO15 | PRG1_PRU0_GPO15         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU0_GPI15         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_RGMII1_TD3         | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG1_PWM0_B1            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | PRG1_PRU0_GPO14         | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_71                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AD20            | PRG1_PRU0_GPO16 | PRG1_PRU0_GPO16         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU0_GPI16         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_RGMII1_TXC         | 2            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_PWM0_A2            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_72                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AH26            | PRG1_PRU0_GPO17 | PRG1_PRU0_GPO17         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU0_GPI17         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_IEP0_EDC_SYNC_OUT1 | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG1_PWM0_B2            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | GPIO0_73                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AG25            | PRG1_PRU0_GPO18 | PRG1_PRU0_GPO18         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU0_GPI18         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_IEP0_EDC_LATCH_IN0 | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_PWM0_TZ_IN         | 3            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_74                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AG26            | PRG1_PRU0_GPO19 | PRG1_PRU0_GPO19         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU0_GPI19         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_IEP0_EDC_SYNC_OUT0 | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG1_PWM0_TZ_OUT        | 3            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | GPIO0_75                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AH24            | PRG1_PRU1_GPO0  | PRG1_PRU1_GPO0          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU1_GPI0          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_RGMII2_RD0         | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_76                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]  | SIGNAL NAME [3]         | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|----------------|-------------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| AH23            | PRG1_PRU1_GPO1 | PRG1_PRU1_GPO1          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU1_GPI1          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_RGMII2_RD1         | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO0_77                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AG21            | PRG1_PRU1_GPO2 | PRG1_PRU1_GPO2          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU1_GPI2          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_RGMII2_RD2         | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_PWM2_A2            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO0_78                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AH22            | PRG1_PRU1_GPO3 | PRG1_PRU1_GPO3          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU1_GPI3          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_RGMII2_RD3         | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | EQEP1_A                 | 4            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO0_79                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AE21            | PRG1_PRU1_GPO4 | PRG1_PRU1_GPO4          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU1_GPI4          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_RGMII2_RX_CTL      | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_PWM2_B2            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                | EQEP1_B                 | 4            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO0_80                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AC22            | PRG1_PRU1_GPO5 | PRG1_PRU1_GPO5          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU1_GPI5          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | EQEP1_S                 | 4            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO0_81                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AG22            | PRG1_PRU1_GPO6 | PRG1_PRU1_GPO6          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU1_GPI6          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_RGMII2_RXC         | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | GPIO0_82                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AD23            | PRG1_PRU1_GPO7 | PRG1_PRU1_GPO7          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | PRG1_PRU1_GPI7          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | PRG1_IEP1_EDC_LATCH_IN1 | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                | SPI2_CS0                | 4            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                | UART1_TXD               | 6            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                | GPIO0_83                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |



**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3]               | MUXMODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-----------------|-------------------------------|-------------|----------|----------------------|-----------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| AE24            | PRG1_PRU1_GPO8  | PRG1_PRU1_GPO8                | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU1_GPI8                | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG1_PWM2_TZ_OUT              | 3           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | GPIO0_84                      | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| AF25            | PRG1_PRU1_GPO9  | PRG1_PRU1_GPO9                | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU1_GPI9                | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG1_UART0_RXD                | 2           | I        |                      |                             |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                 | PRG1_IEP0_EDIO_DATA_IN_OUT3_0 | 6           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | GPIO0_85                      | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| AF24            | PRG1_PRU1_GPO10 | PRG1_PRU1_GPO10               | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU1_GPI10               | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG1_UART0_TXD                | 2           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | PRG1_PWM2_TZ_IN               | 3           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | SPI2_CS3                      | 4           | IO       |                      |                             |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                 | PRG1_IEP0_EDIO_DATA_IN_OUT3_1 | 6           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | GPIO0_86                      | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| AC20            | PRG1_PRU1_GPO11 | PRG1_PRU1_GPO11               | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU1_GPI11               | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG1_RGMII2_TX_CTL            | 2           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | EQEP1_I                       | 4           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG1_PRU1_GPO15               | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | GPIO0_87                      | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| AE20            | PRG1_PRU1_GPO12 | PRG1_PRU1_GPO12               | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU1_GPI12               | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG1_RGMII2_TD0               | 2           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | PRG1_PWM1_A0                  | 3           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG1_PRU1_GPO11               | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | GPIO0_88                      | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
| AF19            | PRG1_PRU1_GPO13 | PRG1_PRU1_GPO13               | 0           | IO       | OFF                  | 7                           | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU1_GPI13               | 1           | I        |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG1_RGMII2_TD1               | 2           | O        |                      |                             |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | PRG1_PWM1_B0                  | 3           | IO       |                      |                             |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                 | PRG1_PRU1_GPO12               | 5           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | GPIO0_89                      | 7           | IO       |                      |                             |                       |           |          |                  |                        | 0         |                           |                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3]         | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-----------------|-------------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| AH19            | PRG1_PRU1_GPO14 | PRG1_PRU1_GPO14         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU1_GPI14         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_RGMII2_TD2         | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG1_PWM1_A1            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_PRU1_GPO13         | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_90                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AG19            | PRG1_PRU1_GPO15 | PRG1_PRU1_GPO15         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU1_GPI15         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_RGMII2_TD3         | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG1_PWM1_B1            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | PRG1_PRU1_GPO14         | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_91                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AE19            | PRG1_PRU1_GPO16 | PRG1_PRU1_GPO16         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU1_GPI16         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_RGMII2_TXC         | 2            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_PWM1_A2            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_92                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AE23            | PRG1_PRU1_GPO17 | PRG1_PRU1_GPO17         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU1_GPI17         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_IEP1_EDC_SYNC_OUT1 | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG1_PWM1_B2            | 3            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | SPI2_CLK                | 4            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_ECAP0_SYNC_OUT     | 5            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | UART1_RXD               | 6            | I        |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | GPIO0_93                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AD22            | PRG1_PRU1_GPO18 | PRG1_PRU1_GPO18         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU1_GPI18         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_IEP1_EDC_LATCH_IN0 | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_PWM1_TZ_IN         | 3            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | SPI2_D0                 | 4            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_ECAP0_SYNC_IN      | 5            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | UART1_CTSn              | 6            | I        |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | GPIO0_94                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3]         | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-----------------|-------------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| AC21            | PRG1_PRU1_GPO19 | PRG1_PRU1_GPO19         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV4   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG1_PRU1_GPI19         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_IEP1_EDC_SYNC_OUT0 | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG1_PWM1_TZ_OUT        | 3            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | SPI2_D1                 | 4            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG1_ECAP0_IN_APWM_OUT  | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | UART1_RTSn              | 6            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | GPIO0_95                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AF18            | PRG2_PRU0_GPO0  | PRG2_PRU0_GPO0          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU0_GPI0          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_RGMII1_RD0         | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPMC0_A25               | 3            | OZ       |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | TRC_CLK                 | 4            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | EHRPWM0_SYNCI           | 5            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_PWM3_A0            | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_30                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AE18            | PRG2_PRU0_GPO1  | PRG2_PRU0_GPO1          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU0_GPI1          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_RGMII1_RD1         | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPMC0_A24               | 3            | OZ       |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | TRC_CTL                 | 4            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | EHRPWM0_SYNCO           | 5            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | SYNC2_OUT               | 6            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | GPIO0_31                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AH17            | PRG2_PRU0_GPO2  | PRG2_PRU0_GPO2          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU0_GPI2          | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_RGMII1_RD2         | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPMC0_A23               | 3            | OZ       |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | TRC_DATA0               | 4            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | EHRPWM_TZn_IN0          | 5            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | SYNC3_OUT               | 6            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | GPIO0_32                | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]  | SIGNAL NAME [3]    | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|----------------|--------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| AG18            | PRG2_PRU0_GPO3 | PRG2_PRU0_GPO3     | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                | PRG2_PRU0_GPI3     | 1            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG2_RGMII1_RD3    | 2            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | GPMC0_A22          | 3            | OZ       |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                | TRC_DATA1          | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                | EHRPWM0_A          | 5            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG2_PWM3_B0       | 6            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                | GPIO0_33           | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| AG17            | PRG2_PRU0_GPO4 | PRG2_PRU0_GPO4     | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                | PRG2_PRU0_GPI4     | 1            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG2_RGMII1_RX_CTL | 2            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | GPMC0_A21          | 3            | OZ       |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                | TRC_DATA2          | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                | EHRPWM0_B          | 5            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG2_PWM0_A0       | 6            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | GPIO0_34           | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| AF17            | PRG2_PRU0_GPO5 | PRG2_PRU0_GPO5     | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                | PRG2_PRU0_GPI5     | 1            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG2_RGMII1_RXC    | 2            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | GPMC0_A20          | 3            | OZ       |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                | TRC_DATA3          | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                | EHRPWM1_A          | 5            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG2_PWM3_A1       | 6            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | GPIO0_35           | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| AE17            | PRG2_PRU0_GPO6 | PRG2_PRU0_GPO6     | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                | PRG2_PRU0_GPI6     | 1            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG2_RGMII1_TX_CTL | 2            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                | GPMC0_A19          | 3            | OZ       |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                | TRC_DATA4          | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                | EHRPWM1_B          | 5            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                | PRG2_PWM3_B1       | 6            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                | GPIO0_36           | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3] | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-----------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| AC19            | PRG2_PRU0_GPO7  | PRG2_PRU0_GPO7  | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU0_GPI7  | 1            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG2_MDIO0_MDIO | 2            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | GPMC0_A18       | 3            | OZ       |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | TRC_DATA5       | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | EHRPWM_TZn_IN1  | 5            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | EHRPWM_SOC_A    | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | GPIO0_37        | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| AH16            | PRG2_PRU0_GPO8  | PRG2_PRU0_GPO8  | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU0_GPI8  | 1            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG2_RGMII1_TD0 | 2            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | GPMC0_A17       | 3            | OZ       |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | TRC_DATA6       | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | EHRPWM2_A       | 5            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG2_PWM0_B0    | 6            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                           |                     |
|                 |                 | GPIO0_38        | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| AG16            | PRG2_PRU0_GPO9  | PRG2_PRU0_GPO9  | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU0_GPI9  | 1            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG2_RGMII1_TD1 | 2            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | GPMC0_A16       | 3            | OZ       |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | TRC_DATA7       | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | EHRPWM2_B       | 5            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | GPIO0_39        | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
| AF16            | PRG2_PRU0_GPO10 | PRG2_PRU0_GPO10 | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU0_GPI10 | 1            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG2_RGMII1_TD2 | 2            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | GPMC0_A15       | 3            | OZ       |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | TRC_DATA8       | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | EHRPWM_TZn_IN2  | 5            | I        |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |
|                 |                 | EHRPWM_SOCB     | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                           |                     |
|                 |                 | GPIO0_40        | 7            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                           |                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3]        | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-----------------|------------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| AE16            | PRG2_PRU0_GPO11 | PRG2_PRU0_GPO11        | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU0_GPI11        | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_RGMII1_TD3        | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | GPMC0_A14              | 3            | OZ       |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | TRC_DATA9              | 4            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG2_ECAP0_IN_APWM_OUT | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_41               | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AD16            | PRG2_PRU0_GPO16 | PRG2_PRU0_GPO16        | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU0_GPI16        | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_RGMII1_TXC        | 2            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPMC0_A13              | 3            | OZ       |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | TRC_DATA10             | 4            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | PRG2_PWM0_A1           | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_42               | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AH15            | PRG2_PRU1_GPO0  | PRG2_PRU1_GPO0         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU1_GPI0         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_RGMII2_RD0        | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPMC0_A12              | 3            | OZ       |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | TRC_DATA11             | 4            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | EHRPWM3_A              | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_PWM3_A2           | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AC16            | PRG2_PRU1_GPO1  | PRG2_PRU1_GPO1         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU1_GPI1         | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_RGMII2_RD1        | 2            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPMC0_A11              | 3            | OZ       |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | TRC_DATA12             | 4            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | EHRPWM3_B              | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_PWM3_B2           | 6            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | GPIO0_44               | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER<br>[1] | BALL NAME [2]  | SIGNAL NAME [3]     | MUXMOD<br>E [4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET<br>REL.<br>MUXMOD<br>E [7] | I/O<br>VOLTAGE<br>VALUE [8] | POWER [9] | HYS [10] | BUFFER<br>TYPE [11] | PULL UP/<br>DOWN<br>TYPE [12] | DSIS [13] | RXACTIVE<br>/ TXDISABL<br>E [14] | IO Daisy<br>Chain [15] |
|--------------------|----------------|---------------------|-----------------|----------|----------------------------|------------------------------------------|-----------------------------|-----------|----------|---------------------|-------------------------------|-----------|----------------------------------|------------------------|
| AD17               | PRG2_PRU1_GPO2 | PRG2_PRU1_GPO2      | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV5   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                | PRG2_PRU1_GPI2      | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                | PRG2_RGMII2_RD2     | 2               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                | GPMC0_A10           | 3               | OZ       |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                | TRC_DATA13          | 4               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                | EHRPWM3_SYNCI       | 5               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                | PRG2_PWM0_B1        | 6               | IO       |                            |                                          |                             |           |          |                     |                               | 1         |                                  |                        |
|                    |                | GPIO0_45            | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
| AH14               | PRG2_PRU1_GPO3 | PRG2_PRU1_GPO3      | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV5   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                | PRG2_PRU1_GPI3      | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                | PRG2_RGMII2_RD3     | 2               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                | GPMC0_A9            | 3               | OZ       |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                | TRC_DATA14          | 4               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                | EHRPWM3_SYNCO       | 5               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                | GPIO0_46            | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                |                     |                 |          |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
| AG14               | PRG2_PRU1_GPO4 | PRG2_PRU1_GPO4      | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV5   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                | PRG2_PRU1_GPI4      | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                | PRG2_RGMII2_RX_CTL  | 2               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                | GPMC0_A8            | 3               | OZ       |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                | TRC_DATA15          | 4               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                | EHRPWM_TZn_IN3      | 5               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                | PRG2_ECAP0_SYNC_OUT | 6               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                | GPIO0_47            | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
| AG15               | PRG2_PRU1_GPO5 | PRG2_PRU1_GPO5      | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV5   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                | PRG2_PRU1_GPI5      | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                | PRG2_RGMII2_RXC     | 2               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                | GPMC0_A7            | 3               | OZ       |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                | TRC_DATA16          | 4               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                | EHRPWM4_A           | 5               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                | GPIO0_48            | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                |                     |                 |          |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
| AC17               | PRG2_PRU1_GPO6 | PRG2_PRU1_GPO6      | 0               | IO       | OFF                        | 7                                        | 1.8 V/3.3 V                 | VDDSHV5   | Yes      | LVCMOS              | PU/PD                         | 0         | 0/1                              | Yes                    |
|                    |                | PRG2_PRU1_GPI6      | 1               | I        |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                | PRG2_RGMII2_TX_CTL  | 2               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                | GPMC0_A6            | 3               | OZ       |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                | TRC_DATA17          | 4               | O        |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |
|                    |                | EHRPWM4_B           | 5               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                | GPIO0_49            | 7               | IO       |                            |                                          |                             |           |          |                     |                               | 0         |                                  |                        |
|                    |                |                     |                 |          |                            |                                          |                             |           |          |                     |                               |           |                                  |                        |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3]  | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-----------------|------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| AE15            | PRG2_PRU1_GPO7  | PRG2_PRU1_GPO7   | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU1_GPI7   | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_MDIO0_MDC   | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | GPMC0_A5         | 3            | OZ       |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | TRC_DATA18       | 4            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | EHRPWM_TZn_IN4   | 5            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_PWM3_TZ_IN  | 6            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_50         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AD15            | PRG2_PRU1_GPO8  | PRG2_PRU1_GPO8   | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU1_GPI8   | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_RGMII2_TD0  | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | GPMC0_A4         | 3            | OZ       |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | TRC_DATA19       | 4            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | EHRPWM5_A        | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_PWM0_A2     | 6            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | GPIO0_51         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AF14            | PRG2_PRU1_GPO9  | PRG2_PRU1_GPO9   | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU1_GPI9   | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_RGMII2_TD1  | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | GPMC0_A3         | 3            | OZ       |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | TRC_DATA20       | 4            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | EHRPWM5_B        | 5            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_PWM3_TZ_OUT | 6            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | GPIO0_52         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
| AC15            | PRG2_PRU1_GPO10 | PRG2_PRU1_GPO10  | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU1_GPI10  | 1            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_RGMII2_TD2  | 2            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | GPMC0_A2         | 3            | OZ       |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | TRC_DATA21       | 4            | O        |                      |                              |                       |           |          |                  |                         |           |                           |                     |
|                 |                 | EHRPWM_TZn_IN5   | 5            | I        |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |
|                 |                 | PRG2_PWM0_B2     | 6            | IO       |                      |                              |                       |           |          |                  |                         | 1         |                           |                     |
|                 |                 | GPIO0_53         | 7            | IO       |                      |                              |                       |           |          |                  |                         | 0         |                           |                     |



**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]   | SIGNAL NAME [3]    | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9]         | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-----------------|--------------------|--------------|----------|----------------------|------------------------------|-----------------------|-------------------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| AD14            | PRG2_PRU1_GPO11 | PRG2_PRU1_GPO11    | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5           | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU1_GPI11    | 1            | I        |                      |                              |                       |                   |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG2_RGMII2_TD3    | 2            | O        |                      |                              |                       |                   |          |                  |                        |           |                           |                     |
|                 |                 | GPMC0_A1           | 3            | OZ       |                      |                              |                       |                   |          |                  |                        |           |                           |                     |
|                 |                 | TRC_DATA22         | 4            | O        |                      |                              |                       |                   |          |                  |                        |           |                           |                     |
|                 |                 | PRG2_ECAP0_SYNC_IN | 6            | I        |                      |                              |                       |                   |          |                  |                        | 0         |                           |                     |
|                 |                 | GPIO0_54           | 7            | IO       |                      |                              |                       |                   |          |                  |                        | 0         |                           |                     |
| AE14            | PRG2_PRU1_GPO16 | PRG2_PRU1_GPO16    | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5           | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |                 | PRG2_PRU1_GPI16    | 1            | I        |                      |                              |                       |                   |          |                  |                        | 0         |                           |                     |
|                 |                 | PRG2_RGMII2_TXC    | 2            | IO       |                      |                              |                       |                   |          |                  |                        | 0         |                           |                     |
|                 |                 | GPMC0_A0           | 3            | OZ       |                      |                              |                       |                   |          |                  |                        |           |                           |                     |
|                 |                 | TRC_DATA23         | 4            | O        |                      |                              |                       |                   |          |                  |                        |           |                           |                     |
|                 |                 | PRG2_PWM1_TZ_OUT   | 6            | O        |                      |                              |                       |                   |          |                  |                        |           |                           |                     |
|                 |                 | GPIO0_55           | 7            | IO       |                      |                              |                       |                   |          |                  |                        | 0         |                           |                     |
| AF9             | REFCLK0N        | REFCLK0N           |              | O        | OFF                  |                              | 1.8 V                 | VDDA_1P8_S ERDES0 |          | LJCB CLK         |                        |           |                           | No                  |
| AF10            | REFCLK0P        | REFCLK0P           |              | O        | OFF                  |                              | 1.8 V                 | VDDA_1P8_S ERDES0 |          | LJCB CLK         |                        |           |                           | No                  |
| AE8             | REFCLK1N        | REFCLK1N           |              | O        | OFF                  |                              | 1.8 V                 | VDDA_1P8_S ERDES0 |          | LJCB CLK         |                        |           |                           | No                  |
| AE9             | REFCLK1P        | REFCLK1P           |              | O        | OFF                  |                              | 1.8 V                 | VDDA_1P8_S ERDES0 |          | LJCB CLK         |                        |           |                           | No                  |
| D19             | RESETSTATz      | RESETSTATz         | 0            | O        | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0           | Yes      | LVCMOS           | PU/PD                  |           | 0/0                       | Yes                 |
| F17             | RESETz          | RESETz             | 0            | I        | PU                   | 0                            | 1.8 V/3.3 V           | VDDSHV0           | Yes      | LVCMOS           | PU/PD                  |           | 1/1                       | Yes                 |
| AG5             | SERDES0_REFCLKN | SERDES0_REFCLKN    |              | I        | OFF                  | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES0          |                        |           |                           | No                  |
| AG6             | SERDES0_REFCLKP | SERDES0_REFCLKP    |              | I        | OFF                  | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES0          |                        |           |                           | No                  |
| AC9             | SERDES0_REFRES  | SERDES0_REFRES     |              | A        |                      | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES0          |                        |           |                           | No                  |
| AH3             | SERDES0_RXN     | SERDES0_RXN        |              | I        | OFF                  | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES0          |                        |           |                           | No                  |
| AG2             | SERDES0_RXP     | SERDES0_RXP        |              | I        | OFF                  | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES0          |                        |           |                           | No                  |
| AH4             | SERDES0_TXN     | SERDES0_TXN        |              | O        | OFF                  | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES0          |                        |           |                           | No                  |
| AG3             | SERDES0_TXP     | SERDES0_TXP        |              | O        | OFF                  | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES0          |                        |           |                           | No                  |
| AH6             | SERDES1_REFCLKN | SERDES1_REFCLKN    |              | I        | OFF                  | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES1          |                        |           |                           | No                  |
| AH7             | SERDES1_REFCLKP | SERDES1_REFCLKP    |              | I        | OFF                  | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES1          |                        |           |                           | No                  |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]     | SIGNAL NAME [3]         | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9]         | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|-------------------|-------------------------|--------------|----------|----------------------|------------------------------|-----------------------|-------------------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| AC14            | SERDES1_REFRES    | SERDES1_REFRES          |              | A        |                      | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES1          |                         |           |                           | No                  |
| AG9             | SERDES1_RXN       | SERDES1_RXN             |              | I        | OFF                  | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES1          |                         |           |                           | No                  |
| AH10            | SERDES1_RXP       | SERDES1_RXP             |              | I        | OFF                  | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES1          |                         |           |                           | No                  |
| AH9             | SERDES1_TXN       | SERDES1_TXN             |              | O        | OFF                  | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES1          |                         |           |                           | No                  |
| AG8             | SERDES1_TXP       | SERDES1_TXP             |              | O        | OFF                  | 0                            | 1.8 V                 | VDDA_1P8_S ERDES0 |          | SERDES1          |                         |           |                           | No                  |
| E20             | SOC_SAFETY_ERRORn | SOC_SAFETY_ERRORn       | 0            | IO       | PD                   | 0                            | 1.8 V/3.3 V           | VDDSHV0           | Yes      | LVC MOS          | PU/PD                   |           | 1/0                       | Yes                 |
| AH13            | SPIO_CLK          | SPIO_CLK                | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1           | Yes      | LVC MOS          | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | GPIO1_17                | 7            | IO       |                      |                              |                       |                   |          |                  |                         | 0         |                           |                     |
| AH12            | SPI1_CLK          | SPI1_CLK                | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1           | Yes      | LVC MOS          | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | PRG2_IEP0_EDC_SYNC_OUT0 | 3            | O        |                      |                              |                       |                   |          |                  |                         |           |                           |                     |
|                 |                   | PRG2_UART0_RTSn         | 4            | O        |                      |                              |                       |                   |          |                  |                         |           |                           |                     |
|                 |                   | GPIO1_22                | 7            | IO       |                      |                              |                       |                   |          |                  |                         | 0         |                           |                     |
|                 |                   |                         |              |          |                      |                              |                       |                   |          |                  |                         |           |                           |                     |
| AG13            | SPIO_CS0          | SPIO_CS0                | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1           | Yes      | LVC MOS          | PU/PD                   | 1         | 0/1                       | Yes                 |
|                 |                   | GPIO1_15                | 7            | IO       |                      |                              |                       |                   |          |                  |                         | 0         |                           |                     |
| AF13            | SPIO_CS1          | SPIO_CS1                | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1           | Yes      | LVC MOS          | PU/PD                   | 1         | 0/1                       | Yes                 |
|                 |                   | CPTS0_TS_COMP           | 1            | O        |                      |                              |                       |                   |          |                  |                         |           |                           |                     |
|                 |                   | I2C3_SCL                | 2            | IOD      |                      |                              |                       |                   |          |                  |                         | 1         |                           |                     |
|                 |                   | PRG1_IEP0_EDIO_OUTVALID | 6            | O        |                      |                              |                       |                   |          |                  |                         |           |                           |                     |
|                 |                   | GPIO1_16                | 7            | IO       |                      |                              |                       |                   |          |                  |                         | 0         |                           |                     |
| AE13            | SPIO_D0           | SPIO_D0                 | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1           | Yes      | LVC MOS          | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | GPIO1_18                | 7            | IO       |                      |                              |                       |                   |          |                  |                         | 0         |                           |                     |
| AD13            | SPIO_D1           | SPIO_D1                 | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1           | Yes      | LVC MOS          | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                   | GPIO1_19                | 7            | IO       |                      |                              |                       |                   |          |                  |                         | 0         |                           |                     |
| AD12            | SPI1_CS0          | SPI1_CS0                | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1           | Yes      | LVC MOS          | PU/PD                   | 1         | 0/1                       | Yes                 |
|                 |                   | PRG2_IEP0_EDC_LATCH_IN0 | 3            | I        |                      |                              |                       |                   |          |                  |                         | 0         |                           |                     |
|                 |                   | PRG2_UART0_CTSn         | 4            | I        |                      |                              |                       |                   |          |                  |                         | 1         |                           |                     |
|                 |                   | PRG0_IEP0_EDIO_OUTVALID | 6            | O        |                      |                              |                       |                   |          |                  |                         |           |                           |                     |
|                 |                   | GPIO1_20                | 7            | IO       |                      |                              |                       |                   |          |                  |                         | 0         |                           |                     |
| AG12            | SPI1_CS1          | SPI1_CS1                | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1           | Yes      | LVC MOS          | PU/PD                   | 1         | 0/1                       | Yes                 |
|                 |                   | CPTS0_TS_SYNC           | 1            | O        |                      |                              |                       |                   |          |                  |                         |           |                           |                     |
|                 |                   | I2C3_SDA                | 2            | IOD      |                      |                              |                       |                   |          |                  |                         | 1         |                           |                     |
|                 |                   | GPIO1_21                | 7            | IO       |                      |                              |                       |                   |          |                  |                         | 0         |                           |                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3]         | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9]     | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|---------------|-------------------------|--------------|----------|----------------------|------------------------------|-----------------------|---------------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| AE12            | SPI1_D0       | SPI1_D0                 | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1       | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |               | PRG2_IEP0_EDC_LATCH_IN1 | 3            | I        |                      |                              |                       |               |          |                  |                        | 0         |                           |                     |
|                 |               | PRG2_UART0_RXD          | 4            | I        |                      |                              |                       |               |          |                  |                        | 1         |                           |                     |
|                 |               | GPIO1_23                | 7            | IO       |                      |                              |                       |               |          |                  |                        | 0         |                           |                     |
| AF12            | SPI1_D1       | SPI1_D1                 | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1       | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |               | PRG2_IEP0_EDC_SYNC_OUT1 | 3            | O        |                      |                              |                       |               |          |                  |                        |           |                           |                     |
|                 |               | PRG2_UART0_TXD          | 4            | O        |                      |                              |                       |               |          |                  |                        |           |                           |                     |
|                 |               | GPIO1_24                | 7            | IO       |                      |                              |                       |               |          |                  |                        | 0         |                           |                     |
| AA4             | TCK           | TCK                     | 0            | I        | PU                   | 0                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                  |           | 1/1                       | Yes                 |
| C20             | TDI           | TDI                     | 0            | I        | PU                   | 0                            | 1.8 V/3.3 V           | VDDSHV0       | Yes      | LVCMOS           | PU/PD                  |           | 1/1                       | Yes                 |
| A20             | TDO           | TDO                     | 0            | OZ       | PU                   | 0                            | 1.8 V/3.3 V           | VDDSHV0       |          | LVCMOS           | PU/PD                  |           | 0/0                       | Yes                 |
| W6              | TEMP_DIODE_P  | TEMP_DIODE_P            |              | A        |                      |                              | 1.8 V                 |               |          | Power            |                        |           |                           | No                  |
| B22             | TIMER_IO0     | TIMER_IO0               | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0       | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |               | SYSCLKOUT0              | 2            | O        |                      |                              |                       |               |          |                  |                        |           |                           |                     |
|                 |               | GPIO1_88                | 7            | IO       |                      |                              |                       |               |          |                  |                        | 0         |                           |                     |
| C23             | TIMER_IO1     | TIMER_IO1               | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0       | Yes      | LVCMOS           | PU/PD                  | 0         | 0/1                       | Yes                 |
|                 |               | OBSCCLK0                | 2            | O        |                      |                              |                       |               |          |                  |                        |           |                           |                     |
|                 |               | GPIO1_89                | 7            | IO       |                      |                              |                       |               |          |                  |                        | 0         |                           |                     |
| A21             | TMS           | TMS                     | 0            | I        | PU                   | 0                            | 1.8 V/3.3 V           | VDDSHV0       | Yes      | LVCMOS           | PU/PD                  |           | 1/1                       | Yes                 |
| AA3             | TRSTn         | TRSTn                   | 0            | I        | PD                   | 0                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                  |           | 1/1                       | Yes                 |
| AG11            | UART0_CTSn    | UART0_CTSn              | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1       | Yes      | LVCMOS           | PU/PD                  | 1         | 0/1                       | Yes                 |
|                 |               | TIMER_IO4               | 1            | IO       |                      |                              |                       |               |          |                  |                        | 0         |                           |                     |
|                 |               | SPI0_CS2                | 2            | IO       |                      |                              |                       |               |          |                  |                        | 1         |                           |                     |
|                 |               | GPIO1_27                | 7            | IO       |                      |                              |                       |               |          |                  |                        | 0         |                           |                     |
| AD11            | UART0_RTSn    | UART0_RTSn              | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1       | Yes      | LVCMOS           | PU/PD                  |           | 0/1                       | Yes                 |
|                 |               | TIMER_IO5               | 1            | IO       |                      |                              |                       |               |          |                  |                        | 0         |                           |                     |
|                 |               | SPI0_CS3                | 2            | IO       |                      |                              |                       |               |          |                  |                        | 1         |                           |                     |
|                 |               | GPIO1_28                | 7            | IO       |                      |                              |                       |               |          |                  |                        | 0         |                           |                     |
| AF11            | UART0_RXD     | UART0_RXD               | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1       | Yes      | LVCMOS           | PU/PD                  | 1         | 0/1                       | Yes                 |
|                 |               | GPIO1_25                | 7            | IO       |                      |                              |                       |               |          |                  |                        | 0         |                           |                     |
| AE11            | UART0_TXD     | UART0_TXD               | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1       | Yes      | LVCMOS           | PU/PD                  |           | 0/1                       | Yes                 |
|                 |               | GPIO1_26                | 7            | IO       |                      |                              |                       |               |          |                  |                        | 0         |                           |                     |
| AE2             | USB0_DM       | USB0_DM                 |              | IO       | OFF                  |                              | 3.3 V                 | VDDA_3P3_USB  |          | USBHS            |                        |           |                           | No                  |
| AF1             | USB0_DP       | USB0_DP                 |              | IO       | OFF                  |                              | 3.3 V                 | VDDA_3P3_USB  |          | USBHS            |                        |           |                           | No                  |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1]  | BALL NAME [2]       | SIGNAL NAME [3]     | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9]     | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|------------------|---------------------|---------------------|--------------|----------|----------------------|------------------------------|-----------------------|---------------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| AD9              | USB0_DRVVBUS        | USB0_DRVVBUS        | 0            | O        | PD                   | 0                            | 1.8 V/3.3 V           | VDDSHV8       | Yes      | LVCMOS           | PU/PD                   |           | 0/0                       | Yes                 |
|                  |                     | GPIO1_71            | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AF7              | USB0_ID             | USB0_ID             |              | A        |                      |                              | 3.3 V                 | VDDA_3P3_U SB |          | USBHS            |                         |           |                           | No                  |
| AE7              | USB0_VBUS           | USB0_VBUS           |              | A        |                      |                              |                       | VDDA_3P3_U SB |          | USBHS            |                         |           |                           | No                  |
| AD2              | USB1_DM             | USB1_DM             |              | IO       | OFF                  |                              | 3.3 V                 | VDDA_3P3_U SB |          | USBHS            |                         |           |                           | No                  |
| AE1              | USB1_DP             | USB1_DP             |              | IO       | OFF                  |                              | 3.3 V                 | VDDA_3P3_U SB |          | USBHS            |                         |           |                           | No                  |
| AC8              | USB1_DRVVBUS        | USB1_DRVVBUS        | 0            | O        | PD                   | 0                            | 1.8 V/3.3 V           | VDDSHV8       | Yes      | LVCMOS           | PU/PD                   |           | 0/0                       | Yes                 |
|                  |                     | GPIO1_72            | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AF5              | USB1_ID             | USB1_ID             |              | A        |                      |                              | 3.3 V                 | VDDA_3P3_U SB |          | USBHS            |                         |           |                           | No                  |
| AF6              | USB1_VBUS           | USB1_VBUS           |              | A        |                      |                              |                       | VDDA_3P3_U SB |          | USBHS            |                         |           |                           | No                  |
| AB6              | VDDA_1P8_MON_WKUP   | VDDA_1P8_MON0       |              | A        |                      |                              | 1.8 V                 |               |          | Power            |                         |           |                           | No                  |
| G17              | VDDA_1P8_SDIO       | VDDA_1P8_SDIO       |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| L20, M21         | VDDA_1P8_CSI0       | VDDA_1P8_CSI0       |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| AC6              | VDDA_1P8_MON0       | VDDA_1P8_MON0       |              | A        |                      |                              | 1.8 V                 |               |          | Power            |                         |           |                           | No                  |
| L22              | VDDA_1P8_OLDIO      | VDDA_1P8_OLDIO      |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| AA14, AB13, AB15 | VDDA_1P8_SERDES0    | VDDA_1P8_SERDES0    |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| AB9              | VDDA_3P3_IOLDO_WKUP | VDDA_3P3_IOLDO_WKUP |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| U6               | VDDA_3P3_MON_WKUP   | VDDA_3P3_MON0       |              | A        |                      |                              | 3.3 V                 |               |          | Power            |                         |           |                           | No                  |
| H17              | VDDA_3P3_SDIO       | VDDA_3P3_SDIO       |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| AC12             | VDDA_3P3_USB        | VDDA_3P3_USB        |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| G18              | VDDA_3P3_IOLDO0     | VDDA_3P3_IOLDO0     |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| AA21             | VDDA_3P3_IOLDO1     | VDDA_3P3_IOLDO1     |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| AC10             | VDDA_3P3_MON0       | VDDA_3P3_MON0       |              | A        |                      |                              | 3.3 V                 |               |          | Power            |                         |           |                           | No                  |
| M7, M9           | VDDA_ADC_MCU        | VDDA_ADC_MCU        |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| AB8              | VDDA_LDO_WKUP       | VDDA_LDO_WKUP       |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| U12              | VDDA_MCU            | VDDA_MCU            |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| H15              | VDDA_PLL0_DDR       | VDDA_PLL0_DDR       |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| H11              | VDDA_PLL1_DDR       | VDDA_PLL1_DDR       |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| Y17              | VDDA_PLL_CORE       | VDDA_PLL_CORE       |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| L21              | VDDA_PLL_DSS        | VDDA_PLL_DSS        |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| L12              | VDDA_PLL_MPU0       | VDDA_PLL_MPU0       |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| K15              | VDDA_PLL_MPU1       | VDDA_PLL_MPU1       |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |
| AB7              | VDDA_PLL_PER0       | VDDA_PLL_PER0       |              | PWR      |                      |                              |                       |               |          |                  |                         |           |                           |                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1]           | BALL NAME [2]   | SIGNAL NAME [3] | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|---------------------------|-----------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| Y9                        | VDDA_POR_WKUP   | VDDA_POR_WKUP   |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| M19                       | VDDA_SRAM_CORE0 | VDDA_SRAM_CORE0 |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| V16                       | VDDA_SRAM_CORE1 | VDDA_SRAM_CORE1 |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| K7                        | VDDA_SRAM_MPU0  | VDDA_SRAM_MPU0  |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| L18                       | VDDA_SRAM_MPU1  | VDDA_SRAM_MPU1  |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| AC11                      | VDDA_VSYS_MON   | VDDA_VSYS_MON   |              | A        |                      |                              | 0.5 V?                |           |          | Power            |                         |           |                           | No                  |
| AA9                       | VDDA_WKUP       | VDDA_WKUP       |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| G12                       | VDDS0           | VDDS0           |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| V8                        | VDDS0_WKUP      | VDDS0_WKUP      |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| AA16                      | VDDS1           | VDDS1           |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| T9                        | VDDS1_WKUP      | VDDS1_WKUP      |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| P20                       | VDDS2           | VDDS2           |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| N8                        | VDDS2_WKUP      | VDDS2_WKUP      |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| T20                       | VDDS3           | VDDS3           |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| Y20                       | VDDS4           | VDDS4           |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| AC18                      | VDDS5           | VDDS5           |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| F20                       | VDDS6           | VDDS6           |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| K20                       | VDDS7           | VDDS7           |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| AA10                      | VDDS8           | VDDS8           |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| G15, H16                  | VDDSHV0         | VDDSHV0         |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| U8, V7, W8, Y7            | VDDSHV0_WKUP    | VDDSHV0_WKUP    |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| AA18, AB17                | VDDSHV1         | VDDSHV1         |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| R6, R8, T7                | VDDSHV1_WKUP    | VDDSHV1_WKUP    |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| N20, N22, P21, R20, R22   | VDDSHV2         | VDDSHV2         |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| N6, P7, P9                | VDDSHV2_WKUP    | VDDSHV2_WKUP    |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| T21, U20, U22, V21, V23   | VDDSHV3         | VDDSHV3         |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| AA22, W20, W22, Y21, Y23  | VDDSHV4         | VDDSHV4         |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| AA20, AB19, AB21, AB23    | VDDSHV5         | VDDSHV5         |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| G20, H19, H21             | VDDSHV6         | VDDSHV6         |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| J20, J22, K21             | VDDSHV7         | VDDSHV7         |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| AB11                      | VDDSHV8         | VDDSHV8         |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| G10, G14, G8, H13, H7, H9 | VDDS_DDR        | VDDS_DDR        |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |
| J16                       | VDDS_OSC1       | VDDS_OSC1       |              | PWR      |                      |                              |                       |           |          |                  |                         |           |                           |                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER<br>[1]                                                                                                                                                                           | BALL NAME [2] | SIGNAL NAME [3] | MUXMOD<br>E [4] | TYPE [5] | BALL<br>RESET<br>STATE [6] | BALL<br>RESET<br>REL.<br>MUXMOD<br>E [7] | I/O<br>VOLTAGE<br>VALUE [8] | POWER [9] | HYS [10] | BUFFER<br>TYPE [11] | PULL UP/<br>DOWN<br>TYPE [12] | DSIS [13] | RXACTIVE<br>/<br>TXDISABL<br>E [14] | IO Daisy<br>Chain [15] |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-----------------|-----------------|----------|----------------------------|------------------------------------------|-----------------------------|-----------|----------|---------------------|-------------------------------|-----------|-------------------------------------|------------------------|
| AA12, J10, J12,<br>J14, J19, J8, K13,<br>L14, L19, M13,<br>N14, P13, P15,<br>P19, R14, R16,<br>R18, T13, T15,<br>T17, T19, U14,<br>U16, U18, V13,<br>V15, V19, W14,<br>W18, Y11, Y13,<br>Y15 | VDD_CORE      | VDD_CORE        |                 | PWR      |                            |                                          |                             |           |          |                     |                               |           |                                     |                        |
| G22                                                                                                                                                                                          | VDD_DLL_MMC0  | VDD_DLL_MMC0    |                 | PWR      |                            |                                          |                             |           |          |                     |                               |           |                                     |                        |
| H23                                                                                                                                                                                          | VDD_DLL_MMC1  | VDD_DLL_MMC1    |                 | PWR      |                            |                                          |                             |           |          |                     |                               |           |                                     |                        |
| N10, P11, R10,<br>R12, T11                                                                                                                                                                   | VDD_MCU       | VDD_MCU         |                 | PWR      |                            |                                          |                             |           |          |                     |                               |           |                                     |                        |
| K11, K9, L10, L8,<br>M11                                                                                                                                                                     | VDD_MPU0      | VDD_MPU0        |                 | PWR      |                            |                                          |                             |           |          |                     |                               |           |                                     |                        |
| K16, K18, L17,<br>M16, M18, N17                                                                                                                                                              | VDD_MPU1      | VDD_MPU1        |                 | PWR      |                            |                                          |                             |           |          |                     |                               |           |                                     |                        |
| V11, W10, W12                                                                                                                                                                                | VDD_WKUP0     | VDD_WKUP0       |                 | PWR      |                            |                                          |                             |           |          |                     |                               |           |                                     |                        |
| M22                                                                                                                                                                                          | VDD_WKUP1     | VDD_WKUP1       |                 | PWR      |                            |                                          |                             |           |          |                     |                               |           |                                     |                        |
| F21                                                                                                                                                                                          | VPP_CORE      | VPP_CORE        |                 | PWR      | OFF                        |                                          | 1.8 V                       |           |          | Power               |                               |           |                                     | No                     |
| T6                                                                                                                                                                                           | VPP_MCU       | VPP_MCU         |                 | PWR      | OFF                        |                                          | 1.8 V                       |           |          | Power               |                               |           |                                     | No                     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | BALL NAME [2] | SIGNAL NAME [3] | MUXMODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-----------------|-------------|----------|----------------------|-----------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|---------------------------|---------------------|
| A1, A2, A28,<br>AA11, AA13,<br>AA15, AA17,<br>AA19, AA23,<br>AA26, AA7,<br>AB10, AB12,<br>AB14, AB16,<br>AB18, AB20,<br>AB22, AD4,<br>AE10, AE25,<br>AE5, AF15, AF2,<br>AF20, AF8, AG1,<br>AG10, AG28,<br>AG4, AG7, AH1,<br>AH11, AH2,<br>AH27, AH28,<br>AH5, AH8, B12,<br>B15, B20, B6, B9,<br>D22, E26, E28,<br>E4, F14, F19,<br>F22, F25, F27,<br>F3, G11, G13,<br>G16, G2, G21,<br>G23, G7, G9, H1,<br>H10, H12, H14,<br>H20, H22, H24,<br>H26, H28, H6,<br>H8, J11, J13, J15,<br>J18, J21, J23,<br>J25, J27, J7, J9,<br>K1, K10, K12,<br>K14, K17, K19,<br>K22, K23, K6, K8,<br>L11, L13, L16,<br>L23, L24, L26,<br>L28, L3, L7, L9,<br>M10, M15, M17,<br>M20, M8, N11,<br>N13, N16, N19,<br>N21, N7, N9,<br>P10, P12, P14,<br>P16, P18, P22,<br>P6, P8, R11, R13,<br>R15, R17, R19,<br>R21, R7, R9, T10,<br>T12, T14, T16,<br>T18, T22, T26,<br>T8, U11, U13,<br>U15, U17, U19,<br>U21, U3, U7, U9,<br>V10, V12, V14,<br>V18, V20, V22,<br>V6, W11, W13,<br>W15, W17, W19,<br>W21, W23, W7,<br>W9, Y12, Y14,<br>Y16, Y18, Y22,<br>Y6, Y8 | VSS           | VSS             |             | GND      |                      |                             |                       |           |          |                  |                        |           |                           |                     |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3]      | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9]     | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|---------------|----------------------|--------------|----------|----------------------|------------------------------|-----------------------|---------------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| AF4             | WKUP_GPIO0_0  | WKUP_GPIO0_0         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |               | MCU_SPI1_CLK         | 1            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_0         | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | MCU_BOOTMODE00       | Bootstrap    | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AF3             | WKUP_GPIO0_1  | WKUP_GPIO0_1         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |               | MCU_SPI1_D0          | 1            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_1         | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | MCU_BOOTMODE01       | Bootstrap    | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AE3             | WKUP_GPIO0_2  | WKUP_GPIO0_2         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |               | MCU_SPI1_D1          | 1            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_2         | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | MCU_BOOTMODE02       | Bootstrap    | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AD1             | WKUP_GPIO0_3  | WKUP_GPIO0_3         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |               | MCU_SPI1_CS0         | 1            | IO       |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |               | WKUP_GPIO0_3         | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | MCU_BOOTMODE03       | Bootstrap    | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AC3             | WKUP_GPIO0_4  | WKUP_GPIO0_4         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |               | MCU_MCAN1_TX         | 1            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |               | MCU_SPI0_CS3         | 2            | IO       |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |               | MCU_ADC_EXT_TRIGGER0 | 3            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_4         | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | MCU_BOOTMODE04       | Bootstrap    | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AD3             | WKUP_GPIO0_5  | WKUP_GPIO0_5         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |               | MCU_MCAN1_RX         | 1            | I        |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |               | MCU_SPI1_CS3         | 2            | IO       |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |               | MCU_ADC_EXT_TRIGGER1 | 3            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_5         | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AC2             | WKUP_GPIO0_6  | WKUP_GPIO0_6         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |               | WKUP_UART0_CTSn      | 1            | I        |                      |                              |                       |               |          |                  |                         | 1         |                           |                     |
|                 |               | MCU_CPTS0_HW1TSPUSH  | 2            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_6         | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AC1             | WKUP_GPIO0_7  | WKUP_GPIO0_7         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |               | WKUP_UART0_RTSn      | 1            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |               | MCU_CPTS0_HW2TSPUSH  | 2            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |               | WKUP_GPIO0_7         | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |



**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]  | SIGNAL NAME [3]   | MUXMOD E [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUXMOD E [7] | I/O VOLTAGE VALUE [8] | POWER [9]     | HYS [10] | BUFFER TYPE [11] | PULL UP/ DOWN TYPE [12] | DSIS [13] | RXACTIVE / TXDISABLE [14] | IO Daisy Chain [15] |
|-----------------|----------------|-------------------|--------------|----------|----------------------|------------------------------|-----------------------|---------------|----------|------------------|-------------------------|-----------|---------------------------|---------------------|
| AC5             | WKUP_GPIO0_8   | WKUP_GPIO0_8      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |                | MCU_CPTS0_TS_SYNC | 2            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                | WKUP_GPIO0_8      | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                | MCU_BOOTMODE08    | Bootstrap    | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AB4             | WKUP_GPIO0_9   | WKUP_GPIO0_9      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 1/1                       | Yes                 |
|                 |                | MCU_CPTS0_TS_COMP | 2            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                | WKUP_GPIO0_9      | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                | MCU_BOOTMODE09    | Bootstrap    | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AB3             | WKUP_GPIO0_10  | WKUP_GPIO0_10     | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | MCU_EXT_REFCLK0   | 1            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                | MCU_CPTS0_RFT_CLK | 4            | I        |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                | MCU_SYCLKOUT0     | 5            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                | WKUP_GPIO0_10     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AB2             | WKUP_GPIO0_11  | WKUP_GPIO0_11     | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 0         | 0/1                       | Yes                 |
|                 |                | MCU_OBSCLK0       | 1            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                | MCU_TIMER_IO1     | 4            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
|                 |                | MCU_CLKOUT0       | 6            | O        |                      |                              |                       |               |          |                  |                         |           |                           |                     |
|                 |                | WKUP_GPIO0_11     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AC7             | WKUP_I2C0_SCL  | WKUP_I2C0_SCL     | 0            | IOD      | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | I2C OPEN DRAIN   |                         | 1         | 1/0                       | Yes                 |
| AD6             | WKUP_I2C0_SDA  | WKUP_I2C0_SDA     | 0            | IOD      | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | I2C OPEN DRAIN   |                         | 1         | 1/0                       | Yes                 |
| AE4             | WKUP_LFOSC0_XI | WKUP_LFOSC0_XI    |              | I        | OFF                  |                              | 1.8 V                 | VDDA_WKUP     |          | Analog           |                         |           |                           | No                  |
| AC4             | WKUP_LFOSC0_XO | WKUP_LFOSC0_XO    |              | O        | OFF                  |                              | 1.8 V                 | VDDA_WKUP     |          | Analog           |                         |           |                           | No                  |
| AD5             | WKUP_OSC0_XI   | WKUP_OSC0_XI      |              | I        | OFF                  |                              | 1.8 V                 | VDDA_WKUP     |          | Analog           |                         |           |                           | No                  |
| AE6             | WKUP_OSC0_XO   | WKUP_OSC0_XO      |              | O        | OFF                  |                              | 1.8 V                 | VDDA_WKUP     |          | Analog           |                         |           |                           | No                  |
| AB1             | WKUP_UART0_RXD | WKUP_UART0_RXD    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 1         | 0/1                       | Yes                 |
|                 |                | WKUP_GPIO0_52     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |
| AB5             | WKUP_UART0_TXD | WKUP_UART0_TXD    | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_WK UP | Yes      | LVCMOS           | PU/PD                   | 1         | 0/1                       | Yes                 |
|                 |                | WKUP_GPIO0_53     | 7            | IO       |                      |                              |                       |               |          |                  |                         | 0         |                           |                     |

The following list describes the table column headers:

- BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.
- BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
- SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).

### Note

Table 5-1, *Pin Attributes*, does not take into account the subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 5.3, *Signal Descriptions*.

4. **MUXMODE:** Multiplexing mode number:

- a. MUXMODE 0 is the primary muxmode. The primary muxmode is not necessarily the default muxmode.

### Note

The default muxmode is the mode at the release of the reset; also see the BALL RESET REL. MUXMODE column.

- b. MUXMODE 1 through 7 are possible muxmodes for alternate functions. On each pin, some muxmodes are effectively used for alternate functions, while some muxmodes are not used. Only MUXMODE values which correspond to defined functions should be used.
- c. Bootstrap are Special Configuration Pins, latched on rising edge of PORn / RESETFULLn. These are not programmable MUXMODE.
- d. An empty box means Not Applicable.
5. **TYPE:** This column describes functionality of the pin when configured for the given mux mode. It does not represent all capabilities of the pin, and as such, there may be other mux mode configurations where these pins operate as a push-pull driver:
  - I = Input
  - O = Output
  - IO = Input or Output
  - IOD = Open drain terminal - Input or Output
  - IOZ = Input, Output or Three-state terminal
  - OZ = Output or Three-state terminal
  - A = Analog
  - PWR = Power
  - GND = Ground
  - CAP = LDO Capacitor.
6. **BALL RESET STATE:** The state of the terminal at power-on reset:
  - DRIVE 0 (OFF): The buffer drives  $V_{OL}$  (pulldown or pullup resistor not activated).
  - DRIVE 1 (OFF): The buffer drives  $V_{OH}$  (pulldown or pullup resistor not activated).
  - OFF: High-impedance
  - PD: High-impedance with an active pulldown resistor
  - PU: High-impedance with an active pullup resistor
  - An empty box means Not Applicable.
7. **BALL RESET REL. MUXMODE:** This muxmode is automatically configured at the release of the rstoutn signal. An empty box means Not Applicable.
8. **I/O VOLTAGE VALUE:** This column describes the IO voltage value (the corresponding power supply). An empty box means Not Applicable.
9. **POWER:** The voltage supply that powers the terminal IO buffers. An empty box means Not Applicable.
10. **HYS:** Indicates if the input buffer has hysteresis:

- Yes: With hysteresis
- No: Without hysteresis

An empty box means No.

For more information, see the hysteresis values in [Section 6.6, Electrical Characteristics](#).

11. **BUFFER TYPE:** This column describes the associated output buffer type

An empty box means Not Applicable.

For drive strength of the associated output buffer, refer to [Section 6.6, Electrical Characteristics](#).

12. **PULL UP/DOWN TYPE:** indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
- PU: Internal pullup
  - PD: Internal pulldown
  - PU/PD: Internal pullup and pulldown
  - An empty box means No pull.
13. **DSIS:** The deselected input state (DSIS) indicates the state driven on the peripheral input (logic "0", logic "1", or "PIN" level) when the peripheral pin function is not selected by any of the PINCTLx registers.
- 0: Logic 0 driven on the input signal port of the peripheral.
  - 1: Logic 1 driven on the input signal port of the peripheral.
  - An empty box means Not Applicable.
14. **RXACTIVE / TXDISABLE:** This column indicates the default value of the RXACTIVE / TXDISABLE bits in the PADCONFIG register.
- RXACTIVE: 0 = receiver disabled, 1 = receiver enabled.
  - TXDISABLE: 0 = driver enabled, 1 = driver disabled.
  - An empty box means Not Applicable.
15. **IO Daisy Chain:** This column indicates which pins can be included in the daisy chain during low power modes.

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#### Note

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (HiZ mode is not an input signal).

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#### Note

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This should be avoided.

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## 5.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

### Note

In [Table 5-1](#) and [Table 5-76](#) are not described the subsystem multiplexing signals.

2. **DESCRIPTION:** Description of the signal
3. **PIN TYPE:** This column describes functionality of the pin when configured for the given mux mode. It does not represent all capabilities of the pin, and as such, there may be other mux mode configurations where these pins operate as a push-pull driver:
  - I = Input
  - O = Output
  - IO = Input or Output
  - IOD = Open drain terminal - Input or Output
  - IOZ = Input, Output or Three-state terminal
  - OZ = Output or Three-state terminal
  - A = Analog
  - PWR = Power
  - GND = Ground
  - CAP = LDO Capacitor
4. **BALL:** Associated balls bottom

For more information on the I/O cell configurations, see the *Pad Configuration Registers* section in the device TRM.

### 5.3.1 ADC

#### 5.3.1.1 MCU Domain

**Table 5-2. ADC Signal Descriptions**

| SIGNAL NAME [1]      | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|----------------------|-------------------|--------------|----------|
| MCU_ADC_EXT_TRIGGER0 | ADC Trigger Input | I            | AC3      |
| MCU_ADC_EXT_TRIGGER1 | ADC Trigger Input | I            | AD3      |

**Table 5-3. ADC0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------------------|--------------|----------|
| MCU_ADC0_REFN   | ADC Reference Input (negative) | A            | K2       |
| MCU_ADC0_REFP   | ADC Reference Input (positive) | A            | K3       |
| MCU_ADC0_AIN0   | ADC Analog Input 0             | A            | K5       |
| MCU_ADC0_AIN1   | ADC Analog Input 1             | A            | J3       |
| MCU_ADC0_AIN2   | ADC Analog Input 2             | A            | J1       |
| MCU_ADC0_AIN3   | ADC Analog Input 3             | A            | J5       |
| MCU_ADC0_AIN4   | ADC Analog Input 4             | A            | K4       |
| MCU_ADC0_AIN5   | ADC Analog Input 5             | A            | J4       |
| MCU_ADC0_AIN6   | ADC Analog Input 6             | A            | J2       |
| MCU_ADC0_AIN7   | ADC Analog Input 7             | A            | J6       |

**Table 5-4. ADC1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------------------|--------------|----------|
| MCU_ADC1_REFN   | ADC Reference Input (negative) | A            | H3       |
| MCU_ADC1_REFP   | ADC Reference Input (positive) | A            | H2       |
| MCU_ADC1_AIN0   | ADC Analog Input 0             | A            | F4       |
| MCU_ADC1_AIN1   | ADC Analog Input 1             | A            | G6       |
| MCU_ADC1_AIN2   | ADC Analog Input 2             | A            | G4       |
| MCU_ADC1_AIN3   | ADC Analog Input 3             | A            | H5       |
| MCU_ADC1_AIN4   | ADC Analog Input 4             | A            | F5       |
| MCU_ADC1_AIN5   | ADC Analog Input 5             | A            | G5       |
| MCU_ADC1_AIN6   | ADC Analog Input 6             | A            | G3       |
| MCU_ADC1_AIN7   | ADC Analog Input 7             | A            | H4       |

### 5.3.2 CAL

#### 5.3.2.1 MAIN Domain

**Table 5-5. CSI0 Signal Descriptions**

| SIGNAL NAME [1]          | DESCRIPTION [2]                           | PIN TYPE [3] | BALL [4] |
|--------------------------|-------------------------------------------|--------------|----------|
| CSI0_RXN0                | CSI Differential Receive Input (negative) | I            | G28      |
| CSI0_RXN1                | CSI Differential Receive Input (negative) | I            | H27      |
| CSI0_RXN2                | CSI Differential Receive Input (negative) | I            | F26      |
| CSI0_RXN3                | CSI Differential Receive Input (negative) | I            | H25      |
| CSI0_RXN4 <sup>(1)</sup> | CSI Differential Receive Input (negative) | I            | G24      |
| CSI0_RXP0                | CSI Differential Receive Input (positive) | I            | F28      |
| CSI0_RXP1                | CSI Differential Receive Input (positive) | I            | G27      |
| CSI0_RXP2                | CSI Differential Receive Input (positive) | I            | G26      |
| CSI0_RXP3                | CSI Differential Receive Input (positive) | I            | G25      |
| CSI0_RXP4 <sup>(1)</sup> | CSI Differential Receive Input (positive) | I            | F24      |

(1) Line 4 (position 5) supports only data. For more information, see the *Camera Adapter Layer (CAL) Subsystem* section in the device TRM.

**Table 5-6. VIN0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]             | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------|--------------|----------|
| VIN0_HD         | Video Input Horizontal Sync | I            | P23      |
| VIN0_PCLK       | Video Input Pixel Clock     | I            | R28      |
| VIN0_VD         | Video Input Vertical Sync   | I            | R23      |
| VIN0_DATA0      | Video Input Data 0          | I            | N23      |
| VIN0_DATA1      | Video Input Data 1          | I            | M26      |
| VIN0_DATA2      | Video Input Data 2          | I            | P28      |
| VIN0_DATA3      | Video Input Data 3          | I            | P27      |
| VIN0_DATA4      | Video Input Data 4          | I            | N26      |
| VIN0_DATA5      | Video Input Data 5          | I            | N25      |
| VIN0_DATA6      | Video Input Data 6          | I            | P24      |
| VIN0_DATA7      | Video Input Data 7          | I            | R27      |
| VIN0_DATA8      | Video Input Data 8          | I            | T24      |
| VIN0_DATA9      | Video Input Data 9          | I            | T23      |

**Table 5-6. VIN0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]     | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------|--------------|----------|
| VIN0_DATA10     | Video Input Data 10 | I            | R25      |
| VIN0_DATA11     | Video Input Data 11 | I            | T27      |
| VIN0_DATA12     | Video Input Data 12 | I            | M27      |
| VIN0_DATA13     | Video Input Data 13 | I            | M23      |
| VIN0_DATA14     | Video Input Data 14 | I            | M28      |
| VIN0_DATA15     | Video Input Data 15 | I            | M24      |

### 5.3.3 CPSW2G

#### 5.3.3.1 MCU Domain

**Table 5-7. CPSW2G0 Signal Descriptions**

| SIGNAL NAME       | DESCRIPTION [2]                 | PIN TYPE [3] | BALL [4] |
|-------------------|---------------------------------|--------------|----------|
| MCU_MDIO0_MDC     | MDIO Clock                      | O            | L1       |
| MCU_MDIO0_MDIO    | MDIO Data                       | IO           | L4       |
| MCU_RGMII1_RXC    | RGMII Receive Clock             | I            | M1       |
| MCU_RGMII1_RX_CTL | RGMII Receive Control           | I            | N5       |
| MCU_RGMII1_TXC    | RGMII Transmit Clock            | IO           | N1       |
| MCU_RGMII1_TX_CTL | RGMII Transmit Control          | O            | N4       |
| MCU_RGMII1_RD0    | RGMII Receive Data 0            | I            | L6       |
| MCU_RGMII1_RD1    | RGMII Receive Data 1            | I            | M6       |
| MCU_RGMII1_RD2    | RGMII Receive Data 2            | I            | L5       |
| MCU_RGMII1_RD3    | RGMII Receive Data 3            | I            | L2       |
| MCU_RGMII1_TD0    | RGMII Transmit Data 0           | O            | M5       |
| MCU_RGMII1_TD1    | RGMII Transmit Data 1           | O            | M4       |
| MCU_RGMII1_TD2    | RGMII Transmit Data 2           | O            | M3       |
| MCU_RGMII1_TD3    | RGMII Transmit Data 3           | O            | M2       |
| MCU_RMII1_CRD_DV  | RMII Carrier Sense / Data Valid | I            | N4       |
| MCU_RMII1_REF_CLK | RMII Reference Clock            | I            | M1       |
| MCU_RMII1_RX_ER   | RMII Receive Data Error         | I            | N5       |
| MCU_RMII1_TX_EN   | RMII Transmit Enable            | O            | N1       |
| MCU_RMII1_RXD0    | RMII Receive Data 0             | I            | L6       |
| MCU_RMII1_RXD1    | RMII Receive Data 1             | I            | M6       |
| MCU_RMII1_TXD0    | RMII Transmit Data 0            | O            | M5       |
| MCU_RMII1_TXD1    | RMII Transmit Data 1            | O            | M4       |

### 5.3.4 DDRSS

#### 5.3.4.1 MAIN Domain

**Table 5-8. DDRSS0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]               | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------------------|--------------|----------|
| DDR_AC0         | DDRSS Address and Command Bus | IO           | A10      |
| DDR_AC1         | DDRSS Address and Command Bus | IO           | D9       |
| DDR_AC2         | DDRSS Address and Command Bus | IO           | C9       |
| DDR_AC3         | DDRSS Address and Command Bus | IO           | E9       |
| DDR_AC4         | DDRSS Address and Command Bus | IO           | A9       |

**Table 5-8. DDRSS0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                     | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------------------------|--------------|----------|
| DDR_AC5         | DDRSS Address and Command Bus       | IO           | E8       |
| DDR_AC6         | DDRSS Address and Command Bus       | IO           | F8       |
| DDR_AC7         | DDRSS Address and Command Bus       | IO           | C7       |
| DDR_AC8         | DDRSS Address and Command Bus       | IO           | C8       |
| DDR_AC9         | DDRSS Address and Command Bus       | IO           | D7       |
| DDR_AC10        | DDRSS Address and Command Bus       | IO           | E7       |
| DDR_AC11        | DDRSS Address and Command Bus       | IO           | A6       |
| DDR_AC12        | DDRSS Address and Command Bus       | IO           | F7       |
| DDR_AC13        | DDRSS Address and Command Bus       | IO           | D6       |
| DDR_AC14        | DDRSS Address and Command Bus       | IO           | C6       |
| DDR_AC15        | DDRSS Address and Command Bus       | IO           | F6       |
| DDR_AC16        | DDRSS Address and Command Bus       | IO           | E6       |
| DDR_AC17        | DDRSS Address and Command Bus       | IO           | E5       |
| DDR_AC18        | DDRSS Address and Command Bus       | IO           | D8       |
| DDR_AC19        | DDRSS Address and Command Bus       | IO           | D10      |
| DDR_AC20        | DDRSS Address and Command Bus       | IO           | E10      |
| DDR_AC21        | DDRSS Address and Command Bus       | IO           | C10      |
| DDR_AC22        | DDRSS Address and Command Bus       | IO           | F11      |
| DDR_AC23        | DDRSS Address and Command Bus       | IO           | B10      |
| DDR_AC24        | DDRSS Address and Command Bus       | IO           | D11      |
| DDR_AC25        | DDRSS Address and Command Bus       | IO           | B11      |
| DDR_AC26        | DDRSS Address and Command Bus       | IO           | C11      |
| DDR_AC27        | DDRSS Address and Command Bus       | IO           | E11      |
| DDR_AC28        | DDRSS Address and Command Bus       | IO           | E12      |
| DDR_AC29        | DDRSS Address and Command Bus       | IO           | D12      |
| DDR_ALERTn      | DDRSS Parity Error                  | IO           | D5       |
| DDR_CK0N        | DDRSS Differential Clock (negative) | IO           | B8       |
| DDR_CK0P        | DDRSS Differential Clock (positive) | IO           | A8       |
| DDR_CK1N        | DDRSS Differential Clock (negative) | IO           | B7       |
| DDR_CK1P        | DDRSS Differential Clock (positive) | IO           | A7       |
| DDR_DM0         | DDRSS Data Mask                     | IO           | E1       |
| DDR_DM1         | DDRSS Data Mask                     | IO           | C5       |
| DDR_DM2         | DDRSS Data Mask                     | IO           | D14      |
| DDR_DM3         | DDRSS Data Mask                     | IO           | B17      |
| DDR_DQ0         | DDRSS Data                          | IO           | A3       |
| DDR_DQ1         | DDRSS Data                          | IO           | B2       |
| DDR_DQ2         | DDRSS Data                          | IO           | C2       |
| DDR_DQ3         | DDRSS Data                          | IO           | D2       |
| DDR_DQ4         | DDRSS Data                          | IO           | E2       |
| DDR_DQ5         | DDRSS Data                          | IO           | G1       |
| DDR_DQ6         | DDRSS Data                          | IO           | F2       |
| DDR_DQ7         | DDRSS Data                          | IO           | F1       |
| DDR_DQ8         | DDRSS Data                          | IO           | E3       |
| DDR_DQ9         | DDRSS Data                          | IO           | C3       |
| DDR_DQ10        | DDRSS Data                          | IO           | D3       |

**Table 5-8. DDRSS0 Signal Descriptions (continued)**

| SIGNAL NAME [1]              | DESCRIPTION [2]                                               | PIN TYPE [3] | BALL [4] |
|------------------------------|---------------------------------------------------------------|--------------|----------|
| DDR_DQ11                     | DDRSS Data                                                    | IO           | B3       |
| DDR_DQ12                     | DDRSS Data                                                    | IO           | D4       |
| DDR_DQ13                     | DDRSS Data                                                    | IO           | C4       |
| DDR_DQ14                     | DDRSS Data                                                    | IO           | B4       |
| DDR_DQ15                     | DDRSS Data                                                    | IO           | B5       |
| DDR_DQ16                     | DDRSS Data                                                    | IO           | E13      |
| DDR_DQ17                     | DDRSS Data                                                    | IO           | C14      |
| DDR_DQ18                     | DDRSS Data                                                    | IO           | B14      |
| DDR_DQ19                     | DDRSS Data                                                    | IO           | A14      |
| DDR_DQ20                     | DDRSS Data                                                    | IO           | E14      |
| DDR_DQ21                     | DDRSS Data                                                    | IO           | B13      |
| DDR_DQ22                     | DDRSS Data                                                    | IO           | C13      |
| DDR_DQ23                     | DDRSS Data                                                    | IO           | D13      |
| DDR_DQ24                     | DDRSS Data                                                    | IO           | D15      |
| DDR_DQ25                     | DDRSS Data                                                    | IO           | C15      |
| DDR_DQ26                     | DDRSS Data                                                    | IO           | E16      |
| DDR_DQ27                     | DDRSS Data                                                    | IO           | E15      |
| DDR_DQ28                     | DDRSS Data                                                    | IO           | D16      |
| DDR_DQ29                     | DDRSS Data                                                    | IO           | B16      |
| DDR_DQ30                     | DDRSS Data                                                    | IO           | C16      |
| DDR_DQ31                     | DDRSS Data                                                    | IO           | A17      |
| DDR_DQS0N                    | DDRSS Complimentary Data Strobe                               | IO           | C1       |
| DDR_DQS0P                    | DDRSS Data Strobe                                             | IO           | D1       |
| DDR_DQS1N                    | DDRSS Complimentary Data Strobe                               | IO           | A4       |
| DDR_DQS1P                    | DDRSS Data Strobe                                             | IO           | A5       |
| DDR_DQS2N                    | DDRSS Complimentary Data Strobe                               | IO           | A12      |
| DDR_DQS2P                    | DDRSS Data Strobe                                             | IO           | A13      |
| DDR_DQS3N                    | DDRSS Complimentary Data Strobe                               | IO           | A16      |
| DDR_DQS3P                    | DDRSS Data Strobe                                             | IO           | A15      |
| DDR_ECC_D0                   | DDRSS ECC Data                                                | IO           | B19      |
| DDR_ECC_D1                   | DDRSS ECC Data                                                | IO           | B18      |
| DDR_ECC_D2                   | DDRSS ECC Data                                                | IO           | C18      |
| DDR_ECC_D3                   | DDRSS ECC Data                                                | IO           | D18      |
| DDR_ECC_D4                   | DDRSS ECC Data                                                | IO           | E18      |
| DDR_ECC_D5                   | DDRSS ECC Data                                                | IO           | E17      |
| DDR_ECC_D6                   | DDRSS ECC Data                                                | IO           | D17      |
| DDR_ECC_DM                   | DDRSS ECC Data Mask                                           | IO           | C17      |
| DDR_ECC_DQSN                 | DDRSS ECC Complimentary Data Strobe                           | IO           | A18      |
| DDR_ECC_DQSP                 | DDRSS ECC Data Strobe                                         | IO           | A19      |
| DDR_FS_RESETn <sup>(3)</sup> | Reserved                                                      | IO           | F16      |
| DDR_RESETn                   | DDRSS Reset                                                   | IO           | A11      |
| DDR_VREF0                    | DDRSS I/O Voltage Reference <sup>(1)</sup>                    | A            | F12      |
| DDR_VREF_ZQ                  | DDRSS I/O Voltage Reference for ZQ calibration <sup>(1)</sup> | A            | F15      |



**Table 5-8. DDRSS0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                           | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------------------------------|--------------|----------|
| DDR_VTP         | DDRSS Calibration Resistor <sup>(2)</sup> | A            | F13      |

- (1) This pin is intended for observation purpose only. No external voltage should be applied to this pin.  
 (2) An external 240Ω ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.  
 (3) Do not connect any signal, test point, or board trace to this signal.

**5.3.4.2 DDRSS Mapping**

Table 5-9 presents DDRSS interface signal mapping per device memory type.

**Note**

DDR3L and LPDDR4 memory types are not supported on this SoC.

**Table 5-9. DDRSS Signal Mapping**

| SIGNAL NAME [1] | MEMORY TYPE          |                         |                       | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------|-------------------------|-----------------------|--------------|----------|
|                 | DDR3L <sup>(2)</sup> | DDR4 <sup>(1) (2)</sup> | LPDDR4 <sup>(1)</sup> |              |          |
| DDR_AC0         | A0                   | A0                      | CA0_A                 | IO           | A10      |
| DDR_AC1         | A1                   | A1                      | CA1_A                 | IO           | D9       |
| DDR_AC2         | A2                   | A2                      | CA2_A                 | IO           | C9       |
| DDR_AC3         | A3                   | A3                      | CA3_A                 | IO           | E9       |
| DDR_AC4         | A4                   | A4                      | CA4_A                 | IO           | A9       |
| DDR_AC5         | A5                   | A5                      | CA5_A                 | IO           | E8       |
| DDR_AC6         | A6                   | A6                      | CA0_B                 | IO           | F8       |
| DDR_AC7         | A7                   | A7                      | CA1_B                 | IO           | C7       |
| DDR_AC8         | A8                   | A8                      | CA2_B                 | IO           | C8       |
| DDR_AC9         | A9                   | A9                      | CA3_B                 | IO           | D7       |
| DDR_AC10        | A10                  | A10                     | CA4_B                 | IO           | E7       |
| DDR_AC11        | A11                  | A11                     | CA5_B                 | IO           | A6       |
| DDR_AC12        | A12                  | A12                     | CS0_B                 | IO           | F7       |
| DDR_AC13        | A13                  | A13                     | CKE0_B                | IO           | D6       |
| DDR_AC14        | A14                  | A14/WE_n                | CS1_B                 | IO           | C6       |
| DDR_AC15        | A15                  | A15/CAS_n               | CKE1_B                | IO           | F6       |
| DDR_AC16        | WE_n                 | A16/RAS_n               |                       | IO           | E6       |
| DDR_AC17        | CAS_n                | A17                     |                       | IO           | E5       |
| DDR_AC18        | RAS_n                | ACT_n                   |                       | IO           | D8       |
| DDR_AC19        | BA0                  | BA0                     |                       | IO           | D10      |
| DDR_AC20        | BA1                  | BA1                     |                       | IO           | E10      |
| DDR_AC21        | BA2                  | BG0                     |                       | IO           | C10      |
| DDR_AC22        |                      | BG1                     |                       | IO           | F11      |
| DDR_AC23        |                      | PAR                     |                       | IO           | B10      |
| DDR_AC24        | CS0_n                | CS0_n                   | CS0_A                 | IO           | D11      |
| DDR_AC25        | ODT0                 | ODT0                    |                       | IO           | B11      |
| DDR_AC26        | CKE0                 | CKE0                    | CKE0_A                | IO           | C11      |
| DDR_AC27        | CS1_n                | CS1_n                   | CS1_A                 | IO           | E11      |
| DDR_AC28        | ODT1                 | ODT1                    |                       | IO           | E12      |
| DDR_AC29        | CKE1                 | CKE1                    | CKE1_A                | IO           | D12      |
| DDR_ALERTn      |                      | ALERT_n                 |                       | IO           | D5       |
| DDR_CK0P        | CK0                  | CK0_t                   | CK_t_A                | IO           | A8       |

**Table 5-9. DDRSS Signal Mapping (continued)**

| SIGNAL NAME [1] | MEMORY TYPE          |                         |                       | PIN TYPE[3] | BALL[4] |
|-----------------|----------------------|-------------------------|-----------------------|-------------|---------|
|                 | DDR3L <sup>(2)</sup> | DDR4 <sup>(1) (2)</sup> | LPDDR4 <sup>(1)</sup> |             |         |
| DDR_CK0N        | CK0_n                | CK0_c                   | CK_c_A                | IO          | B8      |
| DDR_CK1P        | CK1                  | CK1_t                   | CK_t_B                | IO          | A7      |
| DDR_CK1N        | CK1_n                | CK1_c                   | CK_c_B                | IO          | B7      |
| DDR_DQ0         | DQ0                  | DQ0                     | DQ0                   | IO          | A3      |
| DDR_DQ1         | DQ1                  | DQ1                     | DQ1                   | IO          | B2      |
| DDR_DQ2         | DQ2                  | DQ2                     | DQ2                   | IO          | C2      |
| DDR_DQ3         | DQ3                  | DQ3                     | DQ3                   | IO          | D2      |
| DDR_DQ4         | DQ4                  | DQ4                     | DQ4                   | IO          | E2      |
| DDR_DQ5         | DQ5                  | DQ5                     | DQ5                   | IO          | G1      |
| DDR_DQ6         | DQ6                  | DQ6                     | DQ6                   | IO          | F2      |
| DDR_DQ7         | DQ7                  | DQ7                     | DQ7                   | IO          | F1      |
| DDR_DM0         | DM0                  | DM0_n                   | DMI0                  | IO          | E1      |
| DDR_DQ8         | DQ8                  | DQ8                     | DQ8                   | IO          | E3      |
| DDR_DQ9         | DQ9                  | DQ9                     | DQ9                   | IO          | C3      |
| DDR_DQ10        | DQ10                 | DQ10                    | DQ10                  | IO          | D3      |
| DDR_DQ11        | DQ11                 | DQ11                    | DQ11                  | IO          | B3      |
| DDR_DQ12        | DQ12                 | DQ12                    | DQ12                  | IO          | D4      |
| DDR_DQ13        | DQ13                 | DQ13                    | DQ13                  | IO          | C4      |
| DDR_DQ14        | DQ14                 | DQ14                    | DQ14                  | IO          | B4      |
| DDR_DQ15        | DQ15                 | DQ15                    | DQ15                  | IO          | B5      |
| DDR_DM1         | DM1                  | DM1_n                   | DMI1                  | IO          | C5      |
| DDR_DQ16        | DQ16                 | DQ16                    | DQ16                  | IO          | E13     |
| DDR_DQ17        | DQ17                 | DQ17                    | DQ17                  | IO          | C14     |
| DDR_DQ18        | DQ18                 | DQ18                    | DQ18                  | IO          | B14     |
| DDR_DQ19        | DQ19                 | DQ19                    | DQ19                  | IO          | A14     |
| DDR_DQ20        | DQ20                 | DQ20                    | DQ20                  | IO          | E14     |
| DDR_DQ21        | DQ21                 | DQ21                    | DQ21                  | IO          | B13     |
| DDR_DQ22        | DQ22                 | DQ22                    | DQ22                  | IO          | C13     |
| DDR_DQ23        | DQ23                 | DQ23                    | DQ23                  | IO          | D13     |
| DDR_DM2         | DM2                  | DM2_n                   | DMI2                  | IO          | D14     |
| DDR_DQ24        | DQ24                 | DQ24                    | DQ24                  | IO          | D15     |
| DDR_DQ25        | DQ25                 | DQ25                    | DQ25                  | IO          | C15     |
| DDR_DQ26        | DQ26                 | DQ26                    | DQ26                  | IO          | E16     |
| DDR_DQ27        | DQ27                 | DQ27                    | DQ27                  | IO          | E15     |
| DDR_DQ28        | DQ28                 | DQ28                    | DQ28                  | IO          | D16     |
| DDR_DQ29        | DQ29                 | DQ29                    | DQ29                  | IO          | B16     |
| DDR_DQ30        | DQ30                 | DQ30                    | DQ30                  | IO          | C16     |
| DDR_DQ31        | DQ31                 | DQ31                    | DQ31                  | IO          | A17     |
| DDR_DM3         | DM3                  | DM3_n                   | DMI3                  | IO          | B17     |
| DDR_ECC_D0      | DQ32                 | DQ32                    | DQ32                  | IO          | B19     |
| DDR_ECC_D1      | DQ33                 | DQ33                    | DQ33                  | IO          | B18     |
| DDR_ECC_D2      | DQ34                 | DQ34                    | DQ34                  | IO          | C18     |
| DDR_ECC_D3      | DQ35                 | DQ35                    | DQ35                  | IO          | D18     |
| DDR_ECC_D4      | DQ36                 | DQ36                    | DQ36                  | IO          | E18     |

**Table 5-9. DDRSS Signal Mapping (continued)**

| SIGNAL NAME [1] | MEMORY TYPE          |                         |                       | PIN TYPE[3] | BALL[4] |
|-----------------|----------------------|-------------------------|-----------------------|-------------|---------|
|                 | DDR3L <sup>(2)</sup> | DDR4 <sup>(1) (2)</sup> | LPDDR4 <sup>(1)</sup> |             |         |
| DDR_ECC_D5      | DQ37                 | DQ37                    | DQ37                  | IO          | E17     |
| DDR_ECC_D6      | DQ38                 | DQ38                    | DQ38                  | IO          | D17     |
| DDR_ECC_DM      | DM4                  | DM4_n                   | DM4                   | IO          | C17     |
| DDR_DQS0P       | DQS0                 | DQS0_t                  | DQS0                  | IO          | D1      |
| DDR_DQS0N       | DQS0_n               | DQS0_c                  | DQS0_n                | IO          | C1      |
| DDR_DQS1P       | DQS1                 | DQS1_t                  | DQS1                  | IO          | A5      |
| DDR_DQS1N       | DQS1_n               | DQS1_c                  | DQS1_n                | IO          | A4      |
| DDR_DQS2P       | DQS2                 | DQS2_t                  | DQS2                  | IO          | A13     |
| DDR_DQS2N       | DQS2_n               | DQS2_c                  | DQS2_n                | IO          | A12     |
| DDR_DQS3P       | DQS3                 | DQS3_t                  | DQS3                  | IO          | A15     |
| DDR_DQS3N       | DQS3_n               | DQS3_c                  | DQS3_n                | IO          | A16     |
| DDR_ECC_DQSP    | DQS4                 | DQS4_t                  | DQS4                  | IO          | A19     |
| DDR_ECC_DQSN    | DQS4_n               | DQS4_c                  | DQS4_n                | IO          | A18     |
| DDR_RESETh      | RESET_n              | RESET_n                 | RESET_n               | IO          | A11     |
| DDR_VREF0       | VREF0                | VREF0                   | VREF0                 | A           | F12     |
| DDR_VREF_ZQ     | VREF_ZQ              | VREF_ZQ                 | VREF_ZQ               | A           | F15     |
| DDR_VTP         | VTP                  | VTP                     | VTP                   | A           | F13     |

(1) This device cannot support two independent channels.

(2) Only single rank is supported for DDR3L and DDR4.

### 5.3.5 DMTIMER

#### 5.3.5.1 MAIN Domain

**Table 5-10. DMTIMER Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                                              | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------------------------------------------------|--------------|----------|
| TIMER_IO0       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | B22      |
| TIMER_IO1       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | C23      |
| TIMER_IO2       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | P23      |
| TIMER_IO3       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | R23      |
| TIMER_IO4       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | AG11     |
| TIMER_IO5       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | AD11     |
| TIMER_IO6       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | T24      |
| TIMER_IO7       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | T23      |

#### 5.3.5.2 MCU Domain

**Table 5-11. DMTIMER Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                                              | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------------------------------------------------|--------------|----------|
| MCU_TIMER_IO0   | Timer Inputs and Outputs (not tied to single timer instance) | IO           | N3       |

**Table 5-11. DMTIMER Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                                              | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------------------------------------------------|--------------|----------|
| MCU_TIMER_IO1   | Timer Inputs and Outputs (not tied to single timer instance) | IO           | AB2      |

### 5.3.6 DSS

#### 5.3.6.1 MAIN Domain

**Table 5-12. DSS0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                         | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------------------|--------------|----------|
| VOUT1_DE        | Video Output Data Enable                | O            | T23      |
| VOUT1_EXTCLKIN  | Video Output External Pixel Clock Input | I            | R25      |
| VOUT1_HSYNC     | Video Output Horizontal Sync            | O            | T24      |
| VOUT1_PCLK      | Video Output Pixel Clock Output         | O            | R24      |
| VOUT1_VSYNC     | Video Output Vertical Sync              | O            | T25      |
| VOUT1_DATA0     | Video Output Data 0                     | O            | M27      |
| VOUT1_DATA1     | Video Output Data 1                     | O            | M23      |
| VOUT1_DATA2     | Video Output Data 2                     | O            | M28      |
| VOUT1_DATA3     | Video Output Data 3                     | O            | M24      |
| VOUT1_DATA4     | Video Output Data 4                     | O            | N24      |
| VOUT1_DATA5     | Video Output Data 5                     | O            | N27      |
| VOUT1_DATA6     | Video Output Data 6                     | O            | N28      |
| VOUT1_DATA7     | Video Output Data 7                     | O            | M25      |
| VOUT1_DATA8     | Video Output Data 8                     | O            | N23      |
| VOUT1_DATA9     | Video Output Data 9                     | O            | M26      |
| VOUT1_DATA10    | Video Output Data 10                    | O            | P28      |
| VOUT1_DATA11    | Video Output Data 11                    | O            | P27      |
| VOUT1_DATA12    | Video Output Data 12                    | O            | N26      |
| VOUT1_DATA13    | Video Output Data 13                    | O            | N25      |
| VOUT1_DATA14    | Video Output Data 14                    | O            | P24      |
| VOUT1_DATA15    | Video Output Data 15                    | O            | R27      |
| VOUT1_DATA16    | Video Output Data 16                    | O            | R28      |
| VOUT1_DATA17    | Video Output Data 17                    | O            | P25      |
| VOUT1_DATA18    | Video Output Data 18                    | O            | P26      |
| VOUT1_DATA19    | Video Output Data 19                    | O            | U28      |
| VOUT1_DATA20    | Video Output Data 20                    | O            | T28      |
| VOUT1_DATA21    | Video Output Data 21                    | O            | P23      |
| VOUT1_DATA22    | Video Output Data 22                    | O            | R26      |
| VOUT1_DATA23    | Video Output Data 23                    | O            | R23      |

### 5.3.7 ECAP

#### 5.3.7.1 MAIN Domain

**Table 5-13. ECAP0 Signal Descriptions**

| SIGNAL NAME [1]   | DESCRIPTION [2]                                              | PIN TYPE [3] | BALL [4] |
|-------------------|--------------------------------------------------------------|--------------|----------|
| ECAP0_IN_APWM_OUT | Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | IO           | D21      |

### 5.3.8 EHRPWM

#### 5.3.8.1 MAIN Domain

**Table 5-14. EHRPWM Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                       | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------------|--------------|----------|
| EHRPWM_SOCA     | EHRPWM Start of Conversion A          | O            | AC19     |
| EHRPWM_SOCB     | EHRPWM Start of Conversion B          | O            | AF16     |
| EHRPWM_TZn_IN0  | EHRPWM Trip Zone Input 0 (active low) | I            | AH17     |
| EHRPWM_TZn_IN1  | EHRPWM Trip Zone Input 1 (active low) | I            | AC19     |
| EHRPWM_TZn_IN2  | EHRPWM Trip Zone Input 2 (active low) | I            | AF16     |
| EHRPWM_TZn_IN3  | EHRPWM Trip Zone Input 3 (active low) | I            | AG14     |
| EHRPWM_TZn_IN4  | EHRPWM Trip Zone Input 4 (active low) | I            | AE15     |
| EHRPWM_TZn_IN5  | EHRPWM Trip Zone Input 5 (active low) | I            | AC15     |

**Table 5-15. EHRPWM0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                                  | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------------------------------------|--------------|----------|
| EHRPWM0_A       | EHRPWM Output A                                  | IO           | AG18     |
| EHRPWM0_B       | EHRPWM Output B                                  | IO           | AG17     |
| EHRPWM0_SYNCI   | Sync Input to EHRPWM module from an external pin | I            | AF18     |
| EHRPWM0_SYNCO   | Sync Output to EHRPWM module to an external pin  | O            | AE18     |

**Table 5-16. EHRPWM1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| EHRPWM1_A       | EHRPWM Output A | IO           | AF17     |
| EHRPWM1_B       | EHRPWM Output B | IO           | AE17     |

**Table 5-17. EHRPWM2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| EHRPWM2_A       | EHRPWM Output A | IO           | AH16     |
| EHRPWM2_B       | EHRPWM Output B | IO           | AG16     |

**Table 5-18. EHRPWM3 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                                  | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------------------------------------|--------------|----------|
| EHRPWM3_A       | EHRPWM Output A                                  | IO           | AH15     |
| EHRPWM3_B       | EHRPWM Output B                                  | IO           | AC16     |
| EHRPWM3_SYNCI   | Sync Input to EHRPWM module from an external pin | I            | AD17     |
| EHRPWM3_SYNCO   | Sync Output to EHRPWM module to an external pin  | O            | AH14     |

**Table 5-19. EHRPWM4 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| EHRPWM4_A       | EHRPWM Output A | IO           | AG15     |
| EHRPWM4_B       | EHRPWM Output B | IO           | AC17     |

**Table 5-20. EHRPWM5 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| EHRPWM5_A       | EHRPWM Output A | IO           | AD15     |

**Table 5-20. EHRPWM5 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| EHRPWM5_B       | EHRPWM Output B | IO           | AF14     |

### 5.3.9 EQEP

#### 5.3.9.1 MAIN Domain

**Table 5-21. EQEP0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]         | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------------|--------------|----------|
| EQEP0_A         | EQEP Quadrature Input A | I            | AB26     |
| EQEP0_B         | EQEP Quadrature Input B | I            | AA25     |
| EQEP0_I         | EQEP Index              | IO           | AA28     |
| EQEP0_S         | EQEP Strobe             | IO           | U23      |

**Table 5-22. EQEP1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]         | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------------|--------------|----------|
| EQEP1_A         | EQEP Quadrature Input A | I            | AH22     |
| EQEP1_B         | EQEP Quadrature Input B | I            | AE21     |
| EQEP1_I         | EQEP Index              | IO           | AC20     |
| EQEP1_S         | EQEP Strobe             | IO           | AC22     |

**Table 5-23. EQEP2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]         | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------------|--------------|----------|
| EQEP2_A         | EQEP Quadrature Input A | I            | D25      |
| EQEP2_B         | EQEP Quadrature Input B | I            | B26      |
| EQEP2_I         | EQEP Index              | IO           | A24      |
| EQEP2_S         | EQEP Strobe             | IO           | E24      |

### 5.3.10 GPIO

#### 5.3.10.1 MAIN Domain

**Table 5-24. GPIO0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]              | PIN TYPE [3] | BALL [4] |
|-----------------|------------------------------|--------------|----------|
| GPIO0_0         | General Purpose Input/Output | IO           | M27      |
| GPIO0_1         | General Purpose Input/Output | IO           | M23      |
| GPIO0_2         | General Purpose Input/Output | IO           | M28      |
| GPIO0_3         | General Purpose Input/Output | IO           | M24      |
| GPIO0_4         | General Purpose Input/Output | IO           | N24      |
| GPIO0_5         | General Purpose Input/Output | IO           | N27      |
| GPIO0_6         | General Purpose Input/Output | IO           | N28      |
| GPIO0_7         | General Purpose Input/Output | IO           | M25      |
| GPIO0_8         | General Purpose Input/Output | IO           | N23      |
| GPIO0_9         | General Purpose Input/Output | IO           | M26      |
| GPIO0_10        | General Purpose Input/Output | IO           | P28      |
| GPIO0_11        | General Purpose Input/Output | IO           | P27      |
| GPIO0_12        | General Purpose Input/Output | IO           | N26      |
| GPIO0_13        | General Purpose Input/Output | IO           | N25      |

**Table 5-24. GPIO0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]              | PIN TYPE [3] | BALL [4] |
|-----------------|------------------------------|--------------|----------|
| GPIO0_14        | General Purpose Input/Output | IO           | P24      |
| GPIO0_15        | General Purpose Input/Output | IO           | R27      |
| GPIO0_16        | General Purpose Input/Output | IO           | R28      |
| GPIO0_17        | General Purpose Input/Output | IO           | P25      |
| GPIO0_18        | General Purpose Input/Output | IO           | P26      |
| GPIO0_19        | General Purpose Input/Output | IO           | U28      |
| GPIO0_20        | General Purpose Input/Output | IO           | T28      |
| GPIO0_21        | General Purpose Input/Output | IO           | P23      |
| GPIO0_22        | General Purpose Input/Output | IO           | R26      |
| GPIO0_23        | General Purpose Input/Output | IO           | R23      |
| GPIO0_24        | General Purpose Input/Output | IO           | T25      |
| GPIO0_25        | General Purpose Input/Output | IO           | T24      |
| GPIO0_26        | General Purpose Input/Output | IO           | R24      |
| GPIO0_27        | General Purpose Input/Output | IO           | T23      |
| GPIO0_28        | General Purpose Input/Output | IO           | R25      |
| GPIO0_29        | General Purpose Input/Output | IO           | T27      |
| GPIO0_30        | General Purpose Input/Output | IO           | AF18     |
| GPIO0_31        | General Purpose Input/Output | IO           | AE18     |
| GPIO0_32        | General Purpose Input/Output | IO           | AH17     |
| GPIO0_33        | General Purpose Input/Output | IO           | AG18     |
| GPIO0_34        | General Purpose Input/Output | IO           | AG17     |
| GPIO0_35        | General Purpose Input/Output | IO           | AF17     |
| GPIO0_36        | General Purpose Input/Output | IO           | AE17     |
| GPIO0_37        | General Purpose Input/Output | IO           | AC19     |
| GPIO0_38        | General Purpose Input/Output | IO           | AH16     |
| GPIO0_39        | General Purpose Input/Output | IO           | AG16     |
| GPIO0_40        | General Purpose Input/Output | IO           | AF16     |
| GPIO0_41        | General Purpose Input/Output | IO           | AE16     |
| GPIO0_42        | General Purpose Input/Output | IO           | AD16     |
| GPIO0_43        | General Purpose Input/Output | IO           | AH15     |
| GPIO0_44        | General Purpose Input/Output | IO           | AC16     |
| GPIO0_45        | General Purpose Input/Output | IO           | AD17     |
| GPIO0_46        | General Purpose Input/Output | IO           | AH14     |
| GPIO0_47        | General Purpose Input/Output | IO           | AG14     |
| GPIO0_48        | General Purpose Input/Output | IO           | AG15     |
| GPIO0_49        | General Purpose Input/Output | IO           | AC17     |
| GPIO0_50        | General Purpose Input/Output | IO           | AE15     |
| GPIO0_51        | General Purpose Input/Output | IO           | AD15     |
| GPIO0_52        | General Purpose Input/Output | IO           | AF14     |
| GPIO0_53        | General Purpose Input/Output | IO           | AC15     |
| GPIO0_54        | General Purpose Input/Output | IO           | AD14     |
| GPIO0_55        | General Purpose Input/Output | IO           | AE14     |
| GPIO0_56        | General Purpose Input/Output | IO           | AE22     |
| GPIO0_57        | General Purpose Input/Output | IO           | AG24     |
| GPIO0_58        | General Purpose Input/Output | IO           | AF23     |

**Table 5-24. GPIO0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]              | PIN TYPE [3] | BALL [4] |
|-----------------|------------------------------|--------------|----------|
| GPIO0_59        | General Purpose Input/Output | IO           | AD21     |
| GPIO0_60        | General Purpose Input/Output | IO           | AG23     |
| GPIO0_61        | General Purpose Input/Output | IO           | AF27     |
| GPIO0_62        | General Purpose Input/Output | IO           | AF22     |
| GPIO0_63        | General Purpose Input/Output | IO           | AG27     |
| GPIO0_64        | General Purpose Input/Output | IO           | AF28     |
| GPIO0_65        | General Purpose Input/Output | IO           | AF26     |
| GPIO0_66        | General Purpose Input/Output | IO           | AH25     |
| GPIO0_67        | General Purpose Input/Output | IO           | AF21     |
| GPIO0_68        | General Purpose Input/Output | IO           | AH20     |
| GPIO0_69        | General Purpose Input/Output | IO           | AH21     |
| GPIO0_70        | General Purpose Input/Output | IO           | AG20     |
| GPIO0_71        | General Purpose Input/Output | IO           | AD19     |
| GPIO0_72        | General Purpose Input/Output | IO           | AD20     |
| GPIO0_73        | General Purpose Input/Output | IO           | AH26     |
| GPIO0_74        | General Purpose Input/Output | IO           | AG25     |
| GPIO0_75        | General Purpose Input/Output | IO           | AG26     |
| GPIO0_76        | General Purpose Input/Output | IO           | AH24     |
| GPIO0_77        | General Purpose Input/Output | IO           | AH23     |
| GPIO0_78        | General Purpose Input/Output | IO           | AG21     |
| GPIO0_79        | General Purpose Input/Output | IO           | AH22     |
| GPIO0_80        | General Purpose Input/Output | IO           | AE21     |
| GPIO0_81        | General Purpose Input/Output | IO           | AC22     |
| GPIO0_82        | General Purpose Input/Output | IO           | AG22     |
| GPIO0_83        | General Purpose Input/Output | IO           | AD23     |
| GPIO0_84        | General Purpose Input/Output | IO           | AE24     |
| GPIO0_85        | General Purpose Input/Output | IO           | AF25     |
| GPIO0_86        | General Purpose Input/Output | IO           | AF24     |
| GPIO0_87        | General Purpose Input/Output | IO           | AC20     |
| GPIO0_88        | General Purpose Input/Output | IO           | AE20     |
| GPIO0_89        | General Purpose Input/Output | IO           | AF19     |
| GPIO0_90        | General Purpose Input/Output | IO           | AH19     |
| GPIO0_91        | General Purpose Input/Output | IO           | AG19     |
| GPIO0_92        | General Purpose Input/Output | IO           | AE19     |
| GPIO0_93        | General Purpose Input/Output | IO           | AE23     |
| GPIO0_94        | General Purpose Input/Output | IO           | AD22     |
| GPIO0_95        | General Purpose Input/Output | IO           | AC21     |



**Table 5-25. GPIO1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]              | PIN TYPE [3]      | ACD [4] |
|-----------------|------------------------------|-------------------|---------|
| GPIO1_0         | General Purpose Input/Output | IO                | AD18    |
| GPIO1_1         | General Purpose Input/Output | IO                | AH18    |
| GPIO1_2         | General Purpose Input/Output | IO                | D25     |
| GPIO1_3         | General Purpose Input/Output | IO                | B26     |
| GPIO1_4         | General Purpose Input/Output | IO                | A24     |
| GPIO1_5         | General Purpose Input/Output | IO                | E24     |
| GPIO1_6         | General Purpose Input/Output | IO                | A25     |
| GPIO1_7         | General Purpose Input/Output | IO                | C26     |
| GPIO1_8         | General Purpose Input/Output | IO                | E25     |
| GPIO1_9         | General Purpose Input/Output | IO                | A26     |
| GPIO1_10        | General Purpose Input/Output | O                 | B25     |
| GPIO1_11        | General Purpose Input/Output | IO                | B27     |
| GPIO1_12        | General Purpose Input/Output | I                 | C25     |
| GPIO1_13        | General Purpose Input/Output | IO <sup>(1)</sup> | A23     |
| GPIO1_14        | General Purpose Input/Output | IO <sup>(1)</sup> | B23     |
| GPIO1_15        | General Purpose Input/Output | IO                | AG13    |
| GPIO1_16        | General Purpose Input/Output | IO                | AF13    |
| GPIO1_17        | General Purpose Input/Output | IO                | AH13    |
| GPIO1_18        | General Purpose Input/Output | IO                | AE13    |
| GPIO1_19        | General Purpose Input/Output | IO                | AD13    |
| GPIO1_20        | General Purpose Input/Output | IO                | AD12    |
| GPIO1_21        | General Purpose Input/Output | IO                | AG12    |
| GPIO1_22        | General Purpose Input/Output | IO                | AH12    |
| GPIO1_23        | General Purpose Input/Output | IO                | AE12    |
| GPIO1_24        | General Purpose Input/Output | IO                | AF12    |
| GPIO1_25        | General Purpose Input/Output | IO                | AF11    |
| GPIO1_26        | General Purpose Input/Output | IO                | AE11    |
| GPIO1_27        | General Purpose Input/Output | IO                | AG11    |
| GPIO1_28        | General Purpose Input/Output | IO                | AD11    |
| GPIO1_29        | General Purpose Input/Output | IO                | V24     |
| GPIO1_30        | General Purpose Input/Output | IO                | W25     |
| GPIO1_31        | General Purpose Input/Output | IO                | W24     |
| GPIO1_32        | General Purpose Input/Output | IO                | AA27    |
| GPIO1_33        | General Purpose Input/Output | IO                | Y24     |
| GPIO1_34        | General Purpose Input/Output | IO                | V28     |
| GPIO1_35        | General Purpose Input/Output | IO                | Y25     |
| GPIO1_36        | General Purpose Input/Output | IO                | U27     |
| GPIO1_37        | General Purpose Input/Output | IO                | V27     |
| GPIO1_38        | General Purpose Input/Output | IO                | V26     |
| GPIO1_39        | General Purpose Input/Output | IO                | U25     |
| GPIO1_40        | General Purpose Input/Output | IO                | AB25    |
| GPIO1_41        | General Purpose Input/Output | IO                | AD27    |
| GPIO1_42        | General Purpose Input/Output | IO                | AC26    |
| GPIO1_43        | General Purpose Input/Output | IO                | AD26    |
| GPIO1_44        | General Purpose Input/Output | IO                | AA24    |

**Table 5-25. GPIO1 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]              | PIN TYPE [3]      | ACD [4] |
|-----------------|------------------------------|-------------------|---------|
| GPIO1_45        | General Purpose Input/Output | IO                | AD28    |
| GPIO1_46        | General Purpose Input/Output | IO                | U26     |
| GPIO1_47        | General Purpose Input/Output | IO                | V25     |
| GPIO1_48        | General Purpose Input/Output | IO                | U24     |
| GPIO1_49        | General Purpose Input/Output | IO                | AB28    |
| GPIO1_50        | General Purpose Input/Output | IO                | AC28    |
| GPIO1_51        | General Purpose Input/Output | IO                | AC27    |
| GPIO1_52        | General Purpose Input/Output | IO                | AB26    |
| GPIO1_53        | General Purpose Input/Output | IO                | AA25    |
| GPIO1_54        | General Purpose Input/Output | IO                | U23     |
| GPIO1_55        | General Purpose Input/Output | IO                | AB27    |
| GPIO1_56        | General Purpose Input/Output | IO                | W28     |
| GPIO1_57        | General Purpose Input/Output | IO                | W27     |
| GPIO1_58        | General Purpose Input/Output | IO                | Y28     |
| GPIO1_59        | General Purpose Input/Output | IO                | AA28    |
| GPIO1_60        | General Purpose Input/Output | IO                | AB24    |
| GPIO1_61        | General Purpose Input/Output | IO                | AC25    |
| GPIO1_62        | General Purpose Input/Output | IO                | AD25    |
| GPIO1_63        | General Purpose Input/Output | IO                | AD24    |
| GPIO1_64        | General Purpose Input/Output | IO                | AE27    |
| GPIO1_65        | General Purpose Input/Output | IO                | AC24    |
| GPIO1_66        | General Purpose Input/Output | IO                | Y27     |
| GPIO1_67        | General Purpose Input/Output | IO                | Y26     |
| GPIO1_68        | General Purpose Input/Output | IO                | W26     |
| GPIO1_69        | General Purpose Input/Output | IO                | AE26    |
| GPIO1_70        | General Purpose Input/Output | IO                | AE28    |
| GPIO1_71        | General Purpose Input/Output | IO                | AD9     |
| GPIO1_72        | General Purpose Input/Output | IO                | AC8     |
| GPIO1_73        | General Purpose Input/Output | IO                | D27     |
| GPIO1_74        | General Purpose Input/Output | IO                | D26     |
| GPIO1_75        | General Purpose Input/Output | IO                | E27     |
| GPIO1_76        | General Purpose Input/Output | IO                | D28     |
| GPIO1_77        | General Purpose Input/Output | O                 | C27     |
| GPIO1_78        | General Purpose Input/Output | IO                | C28     |
| GPIO1_79        | General Purpose Input/Output | IO <sup>(1)</sup> | B24     |
| GPIO1_80        | General Purpose Input/Output | IO <sup>(1)</sup> | C24     |
| GPIO1_86        | General Purpose Input/Output | IO                | D21     |
| GPIO1_87        | General Purpose Input/Output | IO                | A22     |
| GPIO1_88        | General Purpose Input/Output | IO                | B22     |
| GPIO1_89        | General Purpose Input/Output | IO                | C23     |

(1) When OSC1 is being used with an external crystal, this pin must only be used as an input. The output functionality must be disabled.

## 5.3.10.2 WKUP Domain

Table 5-26. GPIO0 Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2]              | PIN TYPE [3] | BALL [4] |
|-----------------|------------------------------|--------------|----------|
| WKUP_GPIO0_0    | General Purpose Input/Output | IO           | AF4      |
| WKUP_GPIO0_1    | General Purpose Input/Output | IO           | AF3      |
| WKUP_GPIO0_2    | General Purpose Input/Output | IO           | AE3      |
| WKUP_GPIO0_3    | General Purpose Input/Output | IO           | AD1      |
| WKUP_GPIO0_4    | General Purpose Input/Output | IO           | AC3      |
| WKUP_GPIO0_5    | General Purpose Input/Output | IO           | AD3      |
| WKUP_GPIO0_6    | General Purpose Input/Output | IO           | AC2      |
| WKUP_GPIO0_7    | General Purpose Input/Output | IO           | AC1      |
| WKUP_GPIO0_8    | General Purpose Input/Output | IO           | AC5      |
| WKUP_GPIO0_9    | General Purpose Input/Output | IO           | AB4      |
| WKUP_GPIO0_10   | General Purpose Input/Output | IO           | AB3      |
| WKUP_GPIO0_11   | General Purpose Input/Output | IO           | AB2      |
| WKUP_GPIO0_12   | General Purpose Input/Output | IO           | V1       |
| WKUP_GPIO0_13   | General Purpose Input/Output | IO           | U1       |
| WKUP_GPIO0_14   | General Purpose Input/Output | IO           | U2       |
| WKUP_GPIO0_15   | General Purpose Input/Output | IO           | U4       |
| WKUP_GPIO0_16   | General Purpose Input/Output | IO           | U5       |
| WKUP_GPIO0_17   | General Purpose Input/Output | IO           | T2       |
| WKUP_GPIO0_18   | General Purpose Input/Output | IO           | T3       |
| WKUP_GPIO0_19   | General Purpose Input/Output | IO           | T4       |
| WKUP_GPIO0_20   | General Purpose Input/Output | IO           | T5       |
| WKUP_GPIO0_21   | General Purpose Input/Output | IO           | R2       |
| WKUP_GPIO0_22   | General Purpose Input/Output | IO           | R3       |
| WKUP_GPIO0_23   | General Purpose Input/Output | IO           | R4       |
| WKUP_GPIO0_24   | General Purpose Input/Output | IO           | R5       |
| WKUP_GPIO0_25   | General Purpose Input/Output | IO           | T1       |
| WKUP_GPIO0_26   | General Purpose Input/Output | IO           | R1       |
| WKUP_GPIO0_27   | General Purpose Input/Output | IO           | P2       |
| WKUP_GPIO0_28   | General Purpose Input/Output | IO           | P3       |
| WKUP_GPIO0_29   | General Purpose Input/Output | IO           | P4       |
| WKUP_GPIO0_30   | General Purpose Input/Output | IO           | P5       |
| WKUP_GPIO0_31   | General Purpose Input/Output | IO           | P1       |
| WKUP_GPIO0_32   | General Purpose Input/Output | IO           | N2       |
| WKUP_GPIO0_33   | General Purpose Input/Output | IO           | N3       |
| WKUP_GPIO0_34   | General Purpose Input/Output | IO           | N4       |
| WKUP_GPIO0_35   | General Purpose Input/Output | IO           | N5       |
| WKUP_GPIO0_36   | General Purpose Input/Output | IO           | M2       |
| WKUP_GPIO0_37   | General Purpose Input/Output | IO           | M3       |
| WKUP_GPIO0_38   | General Purpose Input/Output | IO           | M4       |
| WKUP_GPIO0_39   | General Purpose Input/Output | IO           | M5       |
| WKUP_GPIO0_40   | General Purpose Input/Output | IO           | N1       |
| WKUP_GPIO0_41   | General Purpose Input/Output | IO           | M1       |
| WKUP_GPIO0_42   | General Purpose Input/Output | IO           | L2       |

**Table 5-26. GPIO0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]              | PIN TYPE [3] | BALL [4] |
|-----------------|------------------------------|--------------|----------|
| WKUP_GPIO0_43   | General Purpose Input/Output | IO           | L5       |
| WKUP_GPIO0_44   | General Purpose Input/Output | IO           | M6       |
| WKUP_GPIO0_45   | General Purpose Input/Output | IO           | L6       |
| WKUP_GPIO0_46   | General Purpose Input/Output | IO           | L4       |
| WKUP_GPIO0_47   | General Purpose Input/Output | IO           | L1       |
| WKUP_GPIO0_48   | General Purpose Input/Output | IO           | Y1       |
| WKUP_GPIO0_49   | General Purpose Input/Output | IO           | Y3       |
| WKUP_GPIO0_50   | General Purpose Input/Output | IO           | Y2       |
| WKUP_GPIO0_51   | General Purpose Input/Output | IO           | Y4       |
| WKUP_GPIO0_52   | General Purpose Input/Output | IO           | AB1      |
| WKUP_GPIO0_53   | General Purpose Input/Output | IO           | AB5      |
| WKUP_GPIO0_54   | General Purpose Input/Output | IO           | W1       |
| WKUP_GPIO0_55   | General Purpose Input/Output | IO           | W2       |

### 5.3.11 GPMC

#### 5.3.11.1 MAIN Domain

**Table 5-27. GPMC0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                                                                             | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------------------------------------------------------------------|--------------|----------|
| GPMC0_ADVn_ALE  | GPMC Address Valid (active low) or Address Latch Enable                                     | O            | P25      |
| GPMC0_CLK       | GPMC Clock Output                                                                           | O            | R28      |
| GPMC0_DIR       | GPMC Data Bus Signal Direction Control                                                      | O            | T24      |
| GPMC0_OEn_REn   | GPMC Output Enable (active low) or Read Enable (active low)                                 | O            | P26      |
| GPMC0_WEn       | GPMC Write Enable (active low)                                                              | O            | U28      |
| GPMC0_WPn       | GPMC Flash Write Protect (active low)                                                       | O            | T25      |
| GPMC0_A0        | GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories | OZ           | AE14     |
| GPMC0_A1        | GPMC address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode    | OZ           | AD14     |
| GPMC0_A2        | GPMC address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode    | OZ           | AC15     |
| GPMC0_A3        | GPMC address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode    | OZ           | AF14     |
| GPMC0_A4        | GPMC address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode    | OZ           | AD15     |
| GPMC0_A5        | GPMC address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode    | OZ           | AE15     |
| GPMC0_A6        | GPMC address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode    | OZ           | AC17     |
| GPMC0_A7        | GPMC address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode    | OZ           | AG15     |
| GPMC0_A8        | GPMC address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode    | OZ           | AG14     |
| GPMC0_A9        | GPMC address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode    | OZ           | AH14     |
| GPMC0_A10       | GPMC address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode   | OZ           | AD17     |

**Table 5-27. GPMC0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                                                                                                | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------------------------------------------------------------------------------------|--------------|----------|
| GPMC0_A11       | GPMC address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AC16     |
| GPMC0_A12       | GPMC address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AH15     |
| GPMC0_A13       | GPMC address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AD16     |
| GPMC0_A14       | GPMC address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AE16     |
| GPMC0_A15       | GPMC address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AF16     |
| GPMC0_A16       | GPMC address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AG16     |
| GPMC0_A17       | GPMC address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AH16     |
| GPMC0_A18       | GPMC address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AC19     |
| GPMC0_A19       | GPMC address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AE17     |
| GPMC0_A20       | GPMC address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AF17     |
| GPMC0_A21       | GPMC address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AG17     |
| GPMC0_A22       | GPMC address 22 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AG18     |
| GPMC0_A23       | GPMC address 23 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AH17     |
| GPMC0_A24       | GPMC address 24 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AE18     |
| GPMC0_A25       | GPMC address 25 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | AF18     |
| GPMC0_A26       | GPMC address 26 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | OZ           | T27      |
| GPMC0_A27       | GPMC address 27 in A/D non-multiplexed mode and Address 27 in A/D multiplexed mode                             | OZ           | R25      |
| GPMC0_AD0       | GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode | IO           | M27      |
| GPMC0_AD1       | GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode | IO           | M23      |
| GPMC0_AD2       | GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode | IO           | M28      |
| GPMC0_AD3       | GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode | IO           | M24      |
| GPMC0_AD4       | GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode | IO           | N24      |
| GPMC0_AD5       | GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode | IO           | N27      |

**Table 5-27. GPMC0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                                                                                                  | PIN TYPE [3] | BALL [4] |
|-----------------|------------------------------------------------------------------------------------------------------------------|--------------|----------|
| GPMC0_AD6       | GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode   | IO           | N28      |
| GPMC0_AD7       | GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode   | IO           | M25      |
| GPMC0_AD8       | GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode   | IO           | N23      |
| GPMC0_AD9       | GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode  | IO           | M26      |
| GPMC0_AD10      | GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode | IO           | P28      |
| GPMC0_AD11      | GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode | IO           | P27      |
| GPMC0_AD12      | GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode | IO           | N26      |
| GPMC0_AD13      | GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode | IO           | N25      |
| GPMC0_AD14      | GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode | IO           | P24      |
| GPMC0_AD15      | GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode | IO           | R27      |
| GPMC0_BE0n_CLE  | GPMC Lower-Byte Enable (active low) or Command Latch Enable                                                      | O            | T28      |
| GPMC0_BE1n      | GPMC Upper-Byte Enable (active low)                                                                              | O            | P23      |
| GPMC0_CS0       | GPMC Chip Select 0 (active low)                                                                                  | O            | R24      |
| GPMC0_CS1       | GPMC Chip Select 1 (active low)                                                                                  | O            | T23      |
| GPMC0_CS2       | GPMC Chip Select 2 (active low)                                                                                  | O            | R25      |
| GPMC0_CS3       | GPMC Chip Select 3 (active low)                                                                                  | O            | T27      |
| GPMC0_WAIT0     | GPMC External Indication of Wait                                                                                 | I            | R26      |
| GPMC0_WAIT1     | GPMC External Indication of Wait                                                                                 | I            | R23      |

### 5.3.12 HyperBus

#### Note

HyperBus is not available on this device.

#### 5.3.12.1 MCU Domain

**Table 5-28. HYPERBUS0 Signal Descriptions**

| SIGNAL NAME [1]    | DESCRIPTION [2]                        | PIN TYPE [3] | BALL [4] |
|--------------------|----------------------------------------|--------------|----------|
| MCU_HYPERBUS0_CK   | Hyperbus Differential Clock (positive) | O            | V1       |
| MCU_HYPERBUS0_CKn  | Hyperbus Differential Clock (negative) | O            | U1       |
| MCU_HYPERBUS0_INTn | Hyperbus Interrupt (active low)        | I            | P2       |

**Table 5-28. HYPERBUS0 Signal Descriptions (continued)**

| SIGNAL NAME [1]       | DESCRIPTION [2]                                                   | PIN TYPE [3] | BALL [4] |
|-----------------------|-------------------------------------------------------------------|--------------|----------|
| MCU_HYPERBUS0_RESETn  | Hyperbus Reset (active low) Output                                | O            | R5       |
| MCU_HYPERBUS0_RESETOn | Hyperbus Reset Status Indicator (active low) from Hyperbus Memory | I            | R1       |
| MCU_HYPERBUS0_RWDS    | Hyperbus Read-Write Data Strobe                                   | IO           | U2       |
| MCU_HYPERBUS0_WPn     | Hyperbus Write Protect (Not in use)                               | O            | N3       |
| MCU_HYPERBUS0_CS0     | Hyperbus Chip Select 0                                            | O            | R4       |
| MCU_HYPERBUS0_CS1     | Hyperbus Chip Select 1                                            | O            | N3       |
| MCU_HYPERBUS0_DQ0     | Hyperbus Data 0                                                   | IO           | U4       |
| MCU_HYPERBUS0_DQ1     | Hyperbus Data 1                                                   | IO           | U5       |
| MCU_HYPERBUS0_DQ2     | Hyperbus Data 2                                                   | IO           | T2       |
| MCU_HYPERBUS0_DQ3     | Hyperbus Data 3                                                   | IO           | T3       |
| MCU_HYPERBUS0_DQ4     | Hyperbus Data 4                                                   | IO           | T4       |
| MCU_HYPERBUS0_DQ5     | Hyperbus Data 5                                                   | IO           | T5       |
| MCU_HYPERBUS0_DQ6     | Hyperbus Data 6                                                   | IO           | R2       |
| MCU_HYPERBUS0_DQ7     | Hyperbus Data 7                                                   | IO           | R3       |

**5.3.13 I2C****5.3.13.1 MAIN Domain****Table 5-29. I2C0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| I2C0_SCL        | I2C Clock       | IOD          | D20      |
| I2C0_SDA        | I2C Data        | IOD          | C21      |

**Table 5-30. I2C1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| I2C1_SCL        | I2C Clock       | IOD          | B21      |
| I2C1_SDA        | I2C Data        | IOD          | E21      |

**Table 5-31. I2C2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| I2C2_SCL        | I2C Clock       | IOD          | T27      |
| I2C2_SDA        | I2C Data        | IOD          | R25      |

**Table 5-32. I2C3 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| I2C3_SCL        | I2C Clock       | IOD          | AF13     |
| I2C3_SDA        | I2C Data        | IOD          | AG12     |

**5.3.13.2 MCU Domain****Table 5-33. I2C0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| MCU_I2C0_SCL    | I2C Clock       | IOD          | AD8      |

**Table 5-33. I2C0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| MCU_I2C0_SDA    | I2C Data        | IOD          | AD7      |

### 5.3.13.3 WKUP Domain

**Table 5-34. I2C0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| WKUP_I2C0_SCL   | I2C Clock       | IOD          | AC7      |
| WKUP_I2C0_SDA   | I2C Data        | IOD          | AD6      |

### 5.3.14 MCAN

#### 5.3.14.1 MCU Domain

**Table 5-35. MCAN0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCU_MCAN0_RX    | MCAN Receive Data  | I            | W2       |
| MCU_MCAN0_TX    | MCAN Transmit Data | O            | W1       |

**Table 5-36. MCAN1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCU_MCAN1_RX    | MCAN Receive Data  | I            | AD3      |
| MCU_MCAN1_TX    | MCAN Transmit Data | O            | AC3      |

### 5.3.15 MCASP

#### 5.3.15.1 MAIN Domain

**Table 5-37. MCASP0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------|--------------|----------|
| MCASP0_ACLKR    | MCASP Receive Bit Clock          | IO           | W24      |
| MCASP0_ACLKX    | MCASP Transmit Bit Clock         | IO           | V24      |
| MCASP0_AFSR     | MCASP Receive Frame Sync         | IO           | AA27     |
| MCASP0_AFSX     | MCASP Transmit Frame Sync        | IO           | W25      |
| MCASP0_AHCLKR   | MCASP Receive Master Clock       | IO           | AA25     |
| MCASP0_AHCLKX   | MCASP Transmit Master Clock      | IO           | U23      |
| MCASP0_AXR0     | MCASP Serial Data (Input/Output) | IO           | Y24      |
| MCASP0_AXR1     | MCASP Serial Data (Input/Output) | IO           | V28      |
| MCASP0_AXR2     | MCASP Serial Data (Input/Output) | IO           | Y25      |
| MCASP0_AXR3     | MCASP Serial Data (Input/Output) | IO           | U27      |
| MCASP0_AXR4     | MCASP Serial Data (Input/Output) | IO           | V27      |
| MCASP0_AXR5     | MCASP Serial Data (Input/Output) | IO           | V26      |
| MCASP0_AXR6     | MCASP Serial Data (Input/Output) | IO           | U25      |
| MCASP0_AXR7     | MCASP Serial Data (Input/Output) | IO           | AB25     |
| MCASP0_AXR8     | MCASP Serial Data (Input/Output) | IO           | AD27     |
| MCASP0_AXR9     | MCASP Serial Data (Input/Output) | IO           | AC26     |
| MCASP0_AXR10    | MCASP Serial Data (Input/Output) | IO           | AD26     |
| MCASP0_AXR11    | MCASP Serial Data (Input/Output) | IO           | AA24     |



**Table 5-37. MCASP0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------|--------------|----------|
| MCASP0_AXR12    | MCASP Serial Data (Input/Output) | IO           | AD28     |
| MCASP0_AXR13    | MCASP Serial Data (Input/Output) | IO           | U26      |
| MCASP0_AXR14    | MCASP Serial Data (Input/Output) | IO           | V25      |
| MCASP0_AXR15    | MCASP Serial Data (Input/Output) | IO           | U24      |

**Table 5-38. MCASP1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------|--------------|----------|
| MCASP1_ACLKR    | MCASP Receive Bit Clock          | IO           | AC27     |
| MCASP1_ACLKX    | MCASP Transmit Bit Clock         | IO           | AB28     |
| MCASP1_AFSR     | MCASP Receive Frame Sync         | IO           | AB26     |
| MCASP1_AFSX     | MCASP Transmit Frame Sync        | IO           | AC28     |
| MCASP1_AHCLKR   | MCASP Receive Master Clock       | IO           | AD28     |
| MCASP1_AHCLKX   | MCASP Transmit Master Clock      | IO           | U26      |
| MCASP1_AXR0     | MCASP Serial Data (Input/Output) | IO           | AA25     |
| MCASP1_AXR1     | MCASP Serial Data (Input/Output) | IO           | U23      |
| MCASP1_AXR2     | MCASP Serial Data (Input/Output) | IO           | AB27     |
| MCASP1_AXR3     | MCASP Serial Data (Input/Output) | IO           | W28      |
| MCASP1_AXR4     | MCASP Serial Data (Input/Output) | IO           | W27      |
| MCASP1_AXR5     | MCASP Serial Data (Input/Output) | IO           | Y28      |
| MCASP1_AXR6     | MCASP Serial Data (Input/Output) | IO           | AA28     |
| MCASP1_AXR7     | MCASP Serial Data (Input/Output) | IO           | AB24     |
| MCASP1_AXR8     | MCASP Serial Data (Input/Output) | IO           | AC25     |
| MCASP1_AXR9     | MCASP Serial Data (Input/Output) | IO           | AD25     |

**Table 5-39. MCASP2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------|--------------|----------|
| MCASP2_ACLKR    | MCASP Receive Bit Clock          | IO           | AE27     |
| MCASP2_ACLKX    | MCASP Transmit Bit Clock         | IO           | W26      |
| MCASP2_AFSR     | MCASP Receive Frame Sync         | IO           | AD24     |
| MCASP2_AFSX     | MCASP Transmit Frame Sync        | IO           | Y26      |
| MCASP2_AHCLKR   | MCASP Receive Master Clock       | IO           | V25      |
| MCASP2_AHCLKX   | MCASP Transmit Master Clock      | IO           | U24      |
| MCASP2_AXR0     | MCASP Serial Data (Input/Output) | IO           | AC24     |
| MCASP2_AXR1     | MCASP Serial Data (Input/Output) | IO           | Y27      |
| MCASP2_AXR2     | MCASP Serial Data (Input/Output) | IO           | AE26     |
| MCASP2_AXR3     | MCASP Serial Data (Input/Output) | IO           | AE28     |

### 5.3.16 MCSPI

#### 5.3.16.1 MAIN Domain

**Table 5-40. MCSPI0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| SPI0_CLK        | SPI Clock         | IO           | AH13     |
| SPI0_CS0        | SPI Chip Select 0 | IO           | AG13     |

**Table 5-40. MCSPI0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| SPI0_CS1        | SPI Chip Select 1 | IO           | AF13     |
| SPI0_CS2        | SPI Chip Select 2 | IO           | AG11     |
| SPI0_CS3        | SPI Chip Select 3 | IO           | AD11     |
| SPI0_D0         | SPI Data 0        | IO           | AE13     |
| SPI0_D1         | SPI Data 1        | IO           | AD13     |

**Table 5-41. MCSPI1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| SPI1_CLK        | SPI Clock         | IO           | AH12     |
| SPI1_CS0        | SPI Chip Select 0 | IO           | AD12     |
| SPI1_CS1        | SPI Chip Select 1 | IO           | AG12     |
| SPI1_CS2        | SPI Chip Select 2 | IO           | AD18     |
| SPI1_CS3        | SPI Chip Select 3 | IO           | AH18     |
| SPI1_D0         | SPI Data 0        | IO           | AE12     |
| SPI1_D1         | SPI Data 1        | IO           | AF12     |

**Table 5-42. MCSPI2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| SPI2_CLK        | SPI Clock         | IO           | AE23     |
| SPI2_CS0        | SPI Chip Select 0 | IO           | AD23     |
| SPI2_CS1        | SPI Chip Select 1 | IO           | AF26     |
| SPI2_CS2        | SPI Chip Select 2 | IO           | AH25     |
| SPI2_CS3        | SPI Chip Select 3 | IO           | AF24     |
| SPI2_D0         | SPI Data 0        | IO           | AD22     |
| SPI2_D1         | SPI Data 1        | IO           | AC21     |

**Table 5-43. MCSPI3 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| SPI3_CLK        | SPI Clock         | IO           | Y27      |
| SPI3_CS0        | SPI Chip Select 0 | IO           | W28      |
| SPI3_CS1        | SPI Chip Select 1 | IO           | V26      |
| SPI3_CS2        | SPI Chip Select 2 | IO           | U25      |
| SPI3_CS3        | SPI Chip Select 3 | IO           | Y28      |
| SPI3_D0         | SPI Data 0        | IO           | Y26      |
| SPI3_D1         | SPI Data 1        | IO           | W26      |

### 5.3.16.2 MCU Domain

**Table 5-44. MCSPI0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| MCU_SPI0_CLK    | SPI Clock         | IO           | Y1       |
| MCU_SPI0_CS0    | SPI Chip Select 0 | IO           | Y4       |
| MCU_SPI0_CS1    | SPI Chip Select 1 | IO           | P1       |
| MCU_SPI0_CS2    | SPI Chip Select 2 | IO           | N3       |

**Table 5-44. MCSPI0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| MCU_SPIO_CS3    | SPI Chip Select 3 | IO           | AC3      |
| MCU_SPIO_D0     | SPI Data 0        | IO           | Y3       |
| MCU_SPIO_D1     | SPI Data 1        | IO           | Y2       |

**Table 5-45. MCSPI1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| MCU_SPI1_CLK    | SPI Clock         | IO           | AF4      |
| MCU_SPI1_CS0    | SPI Chip Select 0 | IO           | AD1      |
| MCU_SPI1_CS1    | SPI Chip Select 1 | IO           | P4       |
| MCU_SPI1_CS2    | SPI Chip Select 2 | IO           | P5       |
| MCU_SPI1_CS3    | SPI Chip Select 3 | IO           | AD3      |
| MCU_SPI1_D0     | SPI Data 0        | IO           | AF3      |
| MCU_SPI1_D1     | SPI Data 1        | IO           | AE3      |

### 5.3.17 MMCSD

#### 5.3.17.1 MAIN Domain

**Table 5-46. MMCSD0 Signal Descriptions**

| SIGNAL NAME [1]              | DESCRIPTION [2]             | PIN TYPE [3] | BALL [4] |
|------------------------------|-----------------------------|--------------|----------|
| MMC0_CLK <sup>(1) (2)</sup>  | MMC/SD Clock                | O            | B25      |
| MMC0_CMD <sup>(1) (2)</sup>  | MMC/SD Command              | IO           | B27      |
| MMC0_DS                      | MMC Data Strobe             | I            | C25      |
| MMC0_SDCD                    | SD Card Detect (active low) | I            | A23      |
| MMC0_SDWP                    | SD Write Protect            | I            | B23      |
| MMC0_DAT0 <sup>(1) (2)</sup> | MMC/SD Data                 | IO           | A26      |
| MMC0_DAT1 <sup>(1) (2)</sup> | MMC/SD Data                 | IO           | E25      |
| MMC0_DAT2 <sup>(1) (2)</sup> | MMC/SD Data                 | IO           | C26      |
| MMC0_DAT3 <sup>(1) (2)</sup> | MMC/SD Data                 | IO           | A25      |
| MMC0_DAT4 <sup>(1) (2)</sup> | MMC/SD Data                 | IO           | E24      |
| MMC0_DAT5 <sup>(1) (2)</sup> | MMC/SD Data                 | IO           | A24      |
| MMC0_DAT6 <sup>(1) (2)</sup> | MMC/SD Data                 | IO           | B26      |
| MMC0_DAT7 <sup>(1) (2)</sup> | MMC/SD Data                 | IO           | D25      |

- (1) When MMCSD0 or MMCSD1 is used, any non-MMC signal function multiplexed with the respective pins are not available. This is due to the MMC having an internal IO multiplexer which is controlled by MMCSD0/1\_SS\_PHY\_CTRL\_1\_REG[31] IOMUX\_ENABLE. This internal IO multiplexer is primary for the signal functions associated with MMCSD pins, and the PADCONFIG's MUXMODE is secondary. Additionally, the internal IO multiplexer affects all of the MMCSD0 or MMCSD1 pins, regardless of configured data bus width. Therefore, when MMCSD0/1\_SS\_PHY\_CTRL\_1\_REG[31] IOMUX\_ENABLE = 0, the respective MMCSD pins are configured for eMMC/SD functionality, regardless of the PADCONFIG [MUXMODE] setting.

- (2) Each of these signals should have an external 50kΩ pull-up resistor connected to the corresponding power supply.

**Table 5-47. MMCSD1 Signal Descriptions**

| SIGNAL NAME [1]             | DESCRIPTION [2]             | PIN TYPE [3] | BALL [4] |
|-----------------------------|-----------------------------|--------------|----------|
| MMC1_CLK <sup>(1) (2)</sup> | MMC/SD Clock                | O            | C27      |
| MMC1_CMD <sup>(1) (2)</sup> | MMC/SD Command              | IO           | C28      |
| MMC1_SDCD                   | SD Card Detect (active low) | I            | B24      |
| MMC1_SDWP                   | SD Write Protect            | I            | C24      |

**Table 5-47. MMCSD1 Signal Descriptions (continued)**

| SIGNAL NAME [1]              | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|------------------------------|-----------------|--------------|----------|
| MMC1_DAT0 <sup>(1) (2)</sup> | MMC/SD Data     | IO           | D28      |
| MMC1_DAT1 <sup>(1) (2)</sup> | MMC/SD Data     | IO           | E27      |
| MMC1_DAT2 <sup>(1) (2)</sup> | MMC/SD Data     | IO           | D26      |
| MMC1_DAT3 <sup>(1) (2)</sup> | MMC/SD Data     | IO           | D27      |

- (1) When MMCSD0 or MMCSD1 is used, any non-MMC signal function multiplexed with the respective pins are not available. This is due to the MMC having an internal IO multiplexer which is controlled by MMCSD0/1\_SS\_PHY\_CTRL\_1\_REG[31] IOMUX\_ENABLE. This internal IO multiplexer is primary for the signal functions associated with MMCSD pins, and the PADCONFIG's MUXMODE is secondary. Additionally, the internal IO multiplexer affects all of the MMCSD0 or MMCSD1 pins, regardless of configured data bus width. Therefore, when MMCSD0/1\_SS\_PHY\_CTRL\_1\_REG[31] IOMUX\_ENABLE = 0, the respective MMCSD pins are configured for eMMC/SD functionality, regardless of the PADCONFIG [MUXMODE] setting.
- (2) Each of these signals should have an external 50kΩ pull-up resistor connected to the corresponding power supply.

### 5.3.18 CPTS

#### Note

Some CPTS signals are connected directly to CPTS modules within the device. Other CPTS signals are connected to the Time Sync Router and fanned out to peripherals linked to the router. Input signals are sent to the peripherals while output signals are sourced from the peripherals. For more information, see the Time Sync and Compare Events section in the Time Sync chapter in the device TRM.

#### 5.3.18.1 MCU Domain

**Table 5-48. CPTS0 Signal Descriptions**

| SIGNAL NAME [1]     | DESCRIPTION [2]                                                               | PIN TYPE [3] | BALL [4] |
|---------------------|-------------------------------------------------------------------------------|--------------|----------|
| MCU_CPTS0_RFT_CLK   | CPTS Reference Clock                                                          | I            | AB3      |
| MCU_CPTS0_TS_COMP   | CPTS Time Stamp Counter Compare from MCU_CPSW0_CPTS0                          | O            | AB4      |
| MCU_CPTS0_TS_SYNC   | CPTS Time Stamp Counter Bit from MCU_CPSW0_CPTS0                              | O            | AC5      |
| MCU_CPTS0_HW1TSPUSH | CPTS Hardware Time Stamp Push 1 input to Time Sync Router and MCU_CPSW0_CPTS0 | I            | AC2      |
| MCU_CPTS0_HW2TSPUSH | CPTS Hardware Time Stamp Push 2 input to Time Sync Router and MCU_CPSW0_CPTS0 | I            | AC1      |

#### 5.3.18.2 MAIN Domain

**Table 5-49. CPTS0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                                           | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------------------------------------|--------------|----------|
| CPTS0_RFT_CLK   | CPTS Reference Clock                                      | I            | D21      |
| CPTS0_TS_COMP   | CPTS Time Stamp Counter Compare from NAVSS0_CPTS0         | O            | AF13     |
| CPTS0_TS_SYNC   | CPTS Time Stamp Counter Bit from NAVSS0_CPTS0             | O            | AG12     |
| CPTS0_HW1TSPUSH | CPTS Hardware Time Stamp Push 1 input to Time Sync Router | I            | B21      |
| CPTS0_HW2TSPUSH | CPTS Hardware Time Stamp Push 2 input to Time Sync Router | I            | E21      |
| SYNC0_OUT       | CPTS Time Stamp Generator Bit 0 from Time Sync Router     | O            | D21      |
| SYNC1_OUT       | CPTS Time Stamp Generator Bit 1 from Time Sync Router     | O            | A22      |

**Table 5-49. CPTS0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                                       | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------------------------------------------|--------------|----------|
| SYNC2_OUT       | CPTS Time Stamp Generator Bit 2 from Time Sync Router | O            | AE18     |
| SYNC3_OUT       | CPTS Time Stamp Generator Bit 3 from Time Sync Router | O            | AH17     |

**5.3.19 OLDI****5.3.19.1 MAIN Domain****Table 5-50. OLDI0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                    | PIN TYPE [3] | BALL [4] |
|-----------------|------------------------------------|--------------|----------|
| OLDI0_CLKN      | OLDI Differential Clock (negative) | IO           | L25      |
| OLDI0_CLKP      | OLDI Differential Clock (positive) | IO           | K25      |
| OLDI0_A0N       | OLDI Differential Data (negative)  | IO           | J28      |
| OLDI0_A0P       | OLDI Differential Data (positive)  | IO           | K28      |
| OLDI0_A1N       | OLDI Differential Data (negative)  | IO           | L27      |
| OLDI0_A1P       | OLDI Differential Data (positive)  | IO           | K27      |
| OLDI0_A2N       | OLDI Differential Data (negative)  | IO           | K24      |
| OLDI0_A2P       | OLDI Differential Data (positive)  | IO           | J24      |
| OLDI0_A3N       | OLDI Differential Data (negative)  | IO           | J26      |
| OLDI0_A3P       | OLDI Differential Data (positive)  | IO           | K26      |

### 5.3.20 OSPI

#### 5.3.20.1 MCU Domain

**Table 5-51. OSPI0 Signal Descriptions**

| SIGNAL NAME [1]  | DESCRIPTION [2]                                | PIN TYPE [3] | BALL [4] |
|------------------|------------------------------------------------|--------------|----------|
| MCU_OSPI0_CLK    | OSPI Clock                                     | O            | V1       |
| MCU_OSPI0_DQS    | OSPI Data Strobe (DQS) or Loopback Clock Input | I            | U2       |
| MCU_OSPI0_LBCLKO | OSPI Loopback Clock Output                     | IO           | U1       |
| MCU_OSPI0_CSn0   | OSPI Chip Select 0 (active low)                | O            | R4       |
| MCU_OSPI0_CSn1   | OSPI Chip Select 1 (active low)                | O            | R5       |
| MCU_OSPI0_CSn2   | OSPI Chip Select 2 (active low)                | O            | R1       |
| MCU_OSPI0_CSn3   | OSPI Chip Select 3 (active low)                | O            | P2       |
| MCU_OSPI0_D0     | OSPI Data 0                                    | IO           | U4       |
| MCU_OSPI0_D1     | OSPI Data 1                                    | IO           | U5       |
| MCU_OSPI0_D2     | OSPI Data 2                                    | IO           | T2       |
| MCU_OSPI0_D3     | OSPI Data 3                                    | IO           | T3       |
| MCU_OSPI0_D4     | OSPI Data 4                                    | IO           | T4       |
| MCU_OSPI0_D5     | OSPI Data 5                                    | IO           | T5       |
| MCU_OSPI0_D6     | OSPI Data 6                                    | IO           | R2       |
| MCU_OSPI0_D7     | OSPI Data 7                                    | IO           | R3       |

**Table 5-52. OSPI1 Signal Descriptions**

| SIGNAL NAME [1]  | DESCRIPTION [2]                                | PIN TYPE [3] | BALL [4] |
|------------------|------------------------------------------------|--------------|----------|
| MCU_OSPI1_CLK    | OSPI Clock                                     | O            | T1       |
| MCU_OSPI1_DQS    | OSPI Data Strobe (DQS) or Loopback Clock Input | I            | P2       |
| MCU_OSPI1_LBCLKO | OSPI Loopback Clock Output                     | IO           | R1       |
| MCU_OSPI1_CSn0   | OSPI Chip Select 0 (active low)                | O            | N2       |
| MCU_OSPI1_CSn1   | OSPI Chip Select 1 (active low)                | O            | N3       |
| MCU_OSPI1_D0     | OSPI Data 0                                    | IO           | P3       |
| MCU_OSPI1_D1     | OSPI Data 1                                    | IO           | P4       |
| MCU_OSPI1_D2     | OSPI Data 2                                    | IO           | P5       |
| MCU_OSPI1_D3     | OSPI Data 3                                    | IO           | P1       |

### 5.3.21 PRU\_ICSSG

#### 5.3.21.1 MAIN Domain

##### Note

The PRU\_ICSSG contains a second layer of multiplexing to enable additional functionality on the PRU GPO and GPI signals. This internal wrapper multiplexing is described in the PRU\_ICSSG chapter in the device TRM.

**Table 5-53. PRU\_ICSSG0 Signal Descriptions**

| SIGNAL NAME [1]              | DESCRIPTION [2]                                                        | PIN TYPE [3] | BALL [4] |
|------------------------------|------------------------------------------------------------------------|--------------|----------|
| PRG0_ECAP0_IN_APWM_OUT       | PRU_ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | IO           | V25      |
| PRG0_ECAP0_SYNC_IN           | PRU_ICSSG ECAP Sync Input                                              | I            | U27      |
| PRG0_ECAP0_SYNC_OUT          | PRU_ICSSG ECAP Sync Output                                             | O            | U26      |
| PRG0_IEP0_EDIO_OUTVALID      | PRU_ICSSG Industrial Ethernet Digital I/O Outvalid                     | O            | AD12     |
| PRG0_IEP0_EDC_LATCH_IN0      | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input            | I            | V25      |
| PRG0_IEP0_EDC_LATCH_IN1      | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input            | I            | U27      |
| PRG0_IEP0_EDC_SYNC_OUT0      | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output            | O            | U24      |
| PRG0_IEP0_EDC_SYNC_OUT1      | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output            | O            | U26      |
| PRG0_IEP0_EDIO_DATA_IN_OUT28 | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output            | IO           | V26      |
| PRG0_IEP0_EDIO_DATA_IN_OUT29 | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output            | IO           | U25      |
| PRG0_IEP0_EDIO_DATA_IN_OUT30 | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output            | IO           | Y28      |
| PRG0_IEP0_EDIO_DATA_IN_OUT31 | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output            | IO           | AA28     |
| PRG0_IEP1_EDC_LATCH_IN0      | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input            | I            | Y26      |
| PRG0_IEP1_EDC_LATCH_IN1      | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input            | I            | W28      |
| PRG0_IEP1_EDC_SYNC_OUT0      | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output            | O            | W26      |
| PRG0_IEP1_EDC_SYNC_OUT1      | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output            | O            | Y27      |
| PRG0_MDIO0_MDC               | PRU_ICSSG MDIO Clock                                                   | O            | AE28     |
| PRG0_MDIO0_MDIO              | PRU_ICSSG MDIO Data                                                    | IO           | AE26     |
| PRG0_PRU0_GPI0               | PRU_ICSSG PRU Data Input                                               | I            | V24      |
| PRG0_PRU0_GPI1               | PRU_ICSSG PRU Data Input                                               | I            | W25      |
| PRG0_PRU0_GPI2               | PRU_ICSSG PRU Data Input                                               | I            | W24      |
| PRG0_PRU0_GPI3               | PRU_ICSSG PRU Data Input                                               | I            | AA27     |
| PRG0_PRU0_GPI4               | PRU_ICSSG PRU Data Input                                               | I            | Y24      |
| PRG0_PRU0_GPI5               | PRU_ICSSG PRU Data Input                                               | I            | V28      |
| PRG0_PRU0_GPI6               | PRU_ICSSG PRU Data Input                                               | I            | Y25      |
| PRG0_PRU0_GPI7               | PRU_ICSSG PRU Data Input                                               | I            | U27      |
| PRG0_PRU0_GPI8               | PRU_ICSSG PRU Data Input                                               | I            | V27      |
| PRG0_PRU0_GPI9               | PRU_ICSSG PRU Data Input                                               | I            | V26      |

**Table 5-53. PRU\_ICSSG0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]           | PIN TYPE [3] | BALL [4]   |
|-----------------|---------------------------|--------------|------------|
| PRG0_PRU0_GPI10 | PRU_ICSSG PRU Data Input  | I            | U25        |
| PRG0_PRU0_GPI11 | PRU_ICSSG PRU Data Input  | I            | AB25       |
| PRG0_PRU0_GPI12 | PRU_ICSSG PRU Data Input  | I            | AD27       |
| PRG0_PRU0_GPI13 | PRU_ICSSG PRU Data Input  | I            | AC26       |
| PRG0_PRU0_GPI14 | PRU_ICSSG PRU Data Input  | I            | AD26       |
| PRG0_PRU0_GPI15 | PRU_ICSSG PRU Data Input  | I            | AA24       |
| PRG0_PRU0_GPI16 | PRU_ICSSG PRU Data Input  | I            | AD28       |
| PRG0_PRU0_GPI17 | PRU_ICSSG PRU Data Input  | I            | U26        |
| PRG0_PRU0_GPI18 | PRU_ICSSG PRU Data Input  | I            | V25        |
| PRG0_PRU0_GPI19 | PRU_ICSSG PRU Data Input  | I            | U24        |
| PRG0_PRU0_GPO0  | PRU_ICSSG PRU Data Output | IO           | V24        |
| PRG0_PRU0_GPO1  | PRU_ICSSG PRU Data Output | IO           | W25        |
| PRG0_PRU0_GPO2  | PRU_ICSSG PRU Data Output | IO           | W24        |
| PRG0_PRU0_GPO3  | PRU_ICSSG PRU Data Output | IO           | AA27       |
| PRG0_PRU0_GPO4  | PRU_ICSSG PRU Data Output | IO           | Y24        |
| PRG0_PRU0_GPO5  | PRU_ICSSG PRU Data Output | IO           | V28        |
| PRG0_PRU0_GPO6  | PRU_ICSSG PRU Data Output | IO           | Y25        |
| PRG0_PRU0_GPO7  | PRU_ICSSG PRU Data Output | IO           | U27        |
| PRG0_PRU0_GPO8  | PRU_ICSSG PRU Data Output | IO           | V27        |
| PRG0_PRU0_GPO9  | PRU_ICSSG PRU Data Output | IO           | V26        |
| PRG0_PRU0_GPO10 | PRU_ICSSG PRU Data Output | IO           | U25        |
| PRG0_PRU0_GPO11 | PRU_ICSSG PRU Data Output | IO           | AB25, AD27 |
| PRG0_PRU0_GPO12 | PRU_ICSSG PRU Data Output | IO           | AC26, AD27 |
| PRG0_PRU0_GPO13 | PRU_ICSSG PRU Data Output | IO           | AC26, AD26 |
| PRG0_PRU0_GPO14 | PRU_ICSSG PRU Data Output | IO           | AA24, AD26 |
| PRG0_PRU0_GPO15 | PRU_ICSSG PRU Data Output | IO           | AA24, AB25 |
| PRG0_PRU0_GPO16 | PRU_ICSSG PRU Data Output | IO           | AD28       |
| PRG0_PRU0_GPO17 | PRU_ICSSG PRU Data Output | IO           | U26        |
| PRG0_PRU0_GPO18 | PRU_ICSSG PRU Data Output | IO           | V25        |
| PRG0_PRU0_GPO19 | PRU_ICSSG PRU Data Output | IO           | U24        |
| PRG0_PRU1_GPI0  | PRU_ICSSG PRU Data Input  | I            | AB28       |
| PRG0_PRU1_GPI1  | PRU_ICSSG PRU Data Input  | I            | AC28       |
| PRG0_PRU1_GPI2  | PRU_ICSSG PRU Data Input  | I            | AC27       |
| PRG0_PRU1_GPI3  | PRU_ICSSG PRU Data Input  | I            | AB26       |
| PRG0_PRU1_GPI4  | PRU_ICSSG PRU Data Input  | I            | AA25       |
| PRG0_PRU1_GPI5  | PRU_ICSSG PRU Data Input  | I            | U23        |
| PRG0_PRU1_GPI6  | PRU_ICSSG PRU Data Input  | I            | AB27       |
| PRG0_PRU1_GPI7  | PRU_ICSSG PRU Data Input  | I            | W28        |
| PRG0_PRU1_GPI8  | PRU_ICSSG PRU Data Input  | I            | W27        |
| PRG0_PRU1_GPI9  | PRU_ICSSG PRU Data Input  | I            | Y28        |
| PRG0_PRU1_GPI10 | PRU_ICSSG PRU Data Input  | I            | AA28       |
| PRG0_PRU1_GPI11 | PRU_ICSSG PRU Data Input  | I            | AB24       |
| PRG0_PRU1_GPI12 | PRU_ICSSG PRU Data Input  | I            | AC25       |
| PRG0_PRU1_GPI13 | PRU_ICSSG PRU Data Input  | I            | AD25       |
| PRG0_PRU1_GPI14 | PRU_ICSSG PRU Data Input  | I            | AD24       |



**Table 5-53. PRU\_ICSSG0 Signal Descriptions (continued)**

| SIGNAL NAME [1]  | DESCRIPTION [2]                | PIN TYPE [3] | BALL [4]   |
|------------------|--------------------------------|--------------|------------|
| PRG0_PRU1_GPI15  | PRU_ICSSG PRU Data Input       | I            | AE27       |
| PRG0_PRU1_GPI16  | PRU_ICSSG PRU Data Input       | I            | AC24       |
| PRG0_PRU1_GPI17  | PRU_ICSSG PRU Data Input       | I            | Y27        |
| PRG0_PRU1_GPI18  | PRU_ICSSG PRU Data Input       | I            | Y26        |
| PRG0_PRU1_GPI19  | PRU_ICSSG PRU Data Input       | I            | W26        |
| PRG0_PRU1_GPO0   | PRU_ICSSG PRU Data Output      | IO           | AB28       |
| PRG0_PRU1_GPO1   | PRU_ICSSG PRU Data Output      | IO           | AC28       |
| PRG0_PRU1_GPO2   | PRU_ICSSG PRU Data Output      | IO           | AC27       |
| PRG0_PRU1_GPO3   | PRU_ICSSG PRU Data Output      | IO           | AB26       |
| PRG0_PRU1_GPO4   | PRU_ICSSG PRU Data Output      | IO           | AA25       |
| PRG0_PRU1_GPO5   | PRU_ICSSG PRU Data Output      | IO           | U23        |
| PRG0_PRU1_GPO6   | PRU_ICSSG PRU Data Output      | IO           | AB27       |
| PRG0_PRU1_GPO7   | PRU_ICSSG PRU Data Output      | IO           | W28        |
| PRG0_PRU1_GPO8   | PRU_ICSSG PRU Data Output      | IO           | W27        |
| PRG0_PRU1_GPO9   | PRU_ICSSG PRU Data Output      | IO           | Y28        |
| PRG0_PRU1_GPO10  | PRU_ICSSG PRU Data Output      | IO           | AA28       |
| PRG0_PRU1_GPO11  | PRU_ICSSG PRU Data Output      | IO           | AB24, AC25 |
| PRG0_PRU1_GPO12  | PRU_ICSSG PRU Data Output      | IO           | AC25, AD25 |
| PRG0_PRU1_GPO13  | PRU_ICSSG PRU Data Output      | IO           | AD24, AD25 |
| PRG0_PRU1_GPO14  | PRU_ICSSG PRU Data Output      | IO           | AD24, AE27 |
| PRG0_PRU1_GPO15  | PRU_ICSSG PRU Data Output      | IO           | AB24, AE27 |
| PRG0_PRU1_GPO16  | PRU_ICSSG PRU Data Output      | IO           | AC24       |
| PRG0_PRU1_GPO17  | PRU_ICSSG PRU Data Output      | IO           | Y27        |
| PRG0_PRU1_GPO18  | PRU_ICSSG PRU Data Output      | IO           | Y26        |
| PRG0_PRU1_GPO19  | PRU_ICSSG PRU Data Output      | IO           | W26        |
| PRG0_PWM0_TZ_IN  | PRU_ICSSG PWM Trip Zone Input  | I            | V25        |
| PRG0_PWM0_TZ_OUT | PRU_ICSSG PWM Trip Zone Output | O            | U24        |
| PRG0_PWM1_TZ_IN  | PRU_ICSSG PWM Trip Zone Input  | I            | Y26        |
| PRG0_PWM1_TZ_OUT | PRU_ICSSG PWM Trip Zone Output | O            | W26        |
| PRG0_PWM2_TZ_IN  | PRU_ICSSG PWM Trip Zone Input  | I            | AA28       |
| PRG0_PWM2_TZ_OUT | PRU_ICSSG PWM Trip Zone Output | O            | W27        |
| PRG0_PWM3_TZ_IN  | PRU_ICSSG PWM Trip Zone Input  | I            | V26        |
| PRG0_PWM3_TZ_OUT | PRU_ICSSG PWM Trip Zone Output | O            | AB25       |
| PRG0_PWM0_A0     | PRU_ICSSG PWM Output A         | IO           | AD27       |
| PRG0_PWM0_A1     | PRU_ICSSG PWM Output A         | IO           | AD26       |
| PRG0_PWM0_A2     | PRU_ICSSG PWM Output A         | IO           | AD28       |
| PRG0_PWM0_B0     | PRU_ICSSG PWM Output B         | IO           | AC26       |
| PRG0_PWM0_B1     | PRU_ICSSG PWM Output B         | IO           | AA24       |
| PRG0_PWM0_B2     | PRU_ICSSG PWM Output B         | IO           | U26        |
| PRG0_PWM1_A0     | PRU_ICSSG PWM Output A         | IO           | AC25       |
| PRG0_PWM1_A1     | PRU_ICSSG PWM Output A         | IO           | AD24       |
| PRG0_PWM1_A2     | PRU_ICSSG PWM Output A         | IO           | AC24       |
| PRG0_PWM1_B0     | PRU_ICSSG PWM Output B         | IO           | AD25       |
| PRG0_PWM1_B1     | PRU_ICSSG PWM Output B         | IO           | AE27       |
| PRG0_PWM1_B2     | PRU_ICSSG PWM Output B         | IO           | Y27        |

**Table 5-53. PRU\_ICSSG0 Signal Descriptions (continued)**

| SIGNAL NAME [1]    | DESCRIPTION [2]                             | PIN TYPE [3] | BALL [4] |
|--------------------|---------------------------------------------|--------------|----------|
| PRG0_PWM2_A0       | PRU_ICSSG PWM Output A                      | IO           | W24      |
| PRG0_PWM2_A1       | PRU_ICSSG PWM Output A                      | IO           | V27      |
| PRG0_PWM2_A2       | PRU_ICSSG PWM Output A                      | IO           | AC27     |
| PRG0_PWM2_B0       | PRU_ICSSG PWM Output B                      | IO           | Y24      |
| PRG0_PWM2_B1       | PRU_ICSSG PWM Output B                      | IO           | U25      |
| PRG0_PWM2_B2       | PRU_ICSSG PWM Output B                      | IO           | AA25     |
| PRG0_PWM3_A0       | PRU_ICSSG PWM Output A                      | IO           | V24      |
| PRG0_PWM3_A1       | PRU_ICSSG PWM Output A                      | IO           | Y25      |
| PRG0_PWM3_A2       | PRU_ICSSG PWM Output A                      | IO           | AA27     |
| PRG0_PWM3_B0       | PRU_ICSSG PWM Output B                      | IO           | W25      |
| PRG0_PWM3_B1       | PRU_ICSSG PWM Output B                      | IO           | U27      |
| PRG0_PWM3_B2       | PRU_ICSSG PWM Output B                      | IO           | V28      |
| PRG0_RGMII1_RXC    | PRU_ICSSG RGMII Receive Clock               | I            | Y25      |
| PRG0_RGMII1_RX_CTL | PRU_ICSSG RGMII Receive Control             | I            | Y24      |
| PRG0_RGMII1_TXC    | PRU_ICSSG RGMII Transmit Clock              | IO           | AD28     |
| PRG0_RGMII1_TX_CTL | PRU_ICSSG RGMII Transmit Control            | O            | AB25     |
| PRG0_RGMII2_RXC    | PRU_ICSSG RGMII Receive Clock               | I            | AB27     |
| PRG0_RGMII2_RX_CTL | PRU_ICSSG RGMII Receive Control             | I            | AA25     |
| PRG0_RGMII2_TXC    | PRU_ICSSG RGMII Transmit Clock              | IO           | AC24     |
| PRG0_RGMII2_TX_CTL | PRU_ICSSG RGMII Transmit Control            | O            | AB24     |
| PRG0_RGMII1_RD0    | PRU_ICSSG RGMII Receive Data                | I            | V24      |
| PRG0_RGMII1_RD1    | PRU_ICSSG RGMII Receive Data                | I            | W25      |
| PRG0_RGMII1_RD2    | PRU_ICSSG RGMII Receive Data                | I            | W24      |
| PRG0_RGMII1_RD3    | PRU_ICSSG RGMII Receive Data                | I            | AA27     |
| PRG0_RGMII1_TD0    | PRU_ICSSG RGMII Transmit Data               | O            | AD27     |
| PRG0_RGMII1_TD1    | PRU_ICSSG RGMII Transmit Data               | O            | AC26     |
| PRG0_RGMII1_TD2    | PRU_ICSSG RGMII Transmit Data               | O            | AD26     |
| PRG0_RGMII1_TD3    | PRU_ICSSG RGMII Transmit Data               | O            | AA24     |
| PRG0_RGMII2_RD0    | PRU_ICSSG RGMII Receive Data                | I            | AB28     |
| PRG0_RGMII2_RD1    | PRU_ICSSG RGMII Receive Data                | I            | AC28     |
| PRG0_RGMII2_RD2    | PRU_ICSSG RGMII Receive Data                | I            | AC27     |
| PRG0_RGMII2_RD3    | PRU_ICSSG RGMII Receive Data                | I            | AB26     |
| PRG0_RGMII2_TD0    | PRU_ICSSG RGMII Transmit Data               | O            | AC25     |
| PRG0_RGMII2_TD1    | PRU_ICSSG RGMII Transmit Data               | O            | AD25     |
| PRG0_RGMII2_TD2    | PRU_ICSSG RGMII Transmit Data               | O            | AD24     |
| PRG0_RGMII2_TD3    | PRU_ICSSG RGMII Transmit Data               | O            | AE27     |
| PRG0_UART0_CTSn    | PRU_ICSSG UART Clear to Send (active low)   | I            | V26      |
| PRG0_UART0_RTSn    | PRU_ICSSG UART Request to Send (active low) | O            | U25      |
| PRG0_UART0_RXD     | PRU_ICSSG UART Receive Data                 | I            | Y28      |
| PRG0_UART0_TXD     | PRU_ICSSG UART Transmit Data                | O            | AA28     |

**Table 5-54. PRU\_ICSSG1 Signal Descriptions**

| SIGNAL NAME [1]        | DESCRIPTION [2]                                                        | PIN TYPE [3] | BALL [4] |
|------------------------|------------------------------------------------------------------------|--------------|----------|
| PRG1_ECAP0_IN_APWM_OUT | PRU_ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | IO           | AC21     |

**Table 5-54. PRU\_ICSSG1 Signal Descriptions (continued)**

| SIGNAL NAME [1]              | DESCRIPTION [2]                                             | PIN TYPE [3] | BALL [4] |
|------------------------------|-------------------------------------------------------------|--------------|----------|
| PRG1_ECAP0_SYNC_IN           | PRU_ICSSG ECAP Sync Input                                   | I            | AD22     |
| PRG1_ECAP0_SYNC_OUT          | PRU_ICSSG ECAP Sync Output                                  | O            | AE23     |
| PRG1_IEP0_EDIO_OUTVALID      | PRU_ICSSG Industrial Ethernet Digital I/O Outvalid          | O            | AF13     |
| PRG1_IEP0_EDC_LATCH_IN0      | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input | I            | AG25     |
| PRG1_IEP0_EDC_LATCH_IN1      | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input | I            | AG27     |
| PRG1_IEP0_EDC_SYNC_OUT0      | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output | O            | AG26     |
| PRG1_IEP0_EDC_SYNC_OUT1      | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output | O            | AH26     |
| PRG1_IEP0_EDIO_DATA_IN_OUT28 | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output | IO           | AF26     |
| PRG1_IEP0_EDIO_DATA_IN_OUT29 | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output | IO           | AH25     |
| PRG1_IEP0_EDIO_DATA_IN_OUT30 | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output | IO           | AF25     |
| PRG1_IEP0_EDIO_DATA_IN_OUT31 | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output | IO           | AF24     |
| PRG1_IEP1_EDC_LATCH_IN0      | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input | I            | AD22     |
| PRG1_IEP1_EDC_LATCH_IN1      | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input | I            | AD23     |
| PRG1_IEP1_EDC_SYNC_OUT0      | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output | O            | AC21     |
| PRG1_IEP1_EDC_SYNC_OUT1      | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output | O            | AE23     |
| PRG1_MDIO0_MDC               | PRU_ICSSG MDIO Clock                                        | O            | AH18     |
| PRG1_MDIO0_MDIO              | PRU_ICSSG MDIO Data                                         | IO           | AD18     |
| PRG1_PRU0_GPI0               | PRU_ICSSG PRU Data Input                                    | I            | AE22     |
| PRG1_PRU0_GPI1               | PRU_ICSSG PRU Data Input                                    | I            | AG24     |
| PRG1_PRU0_GPI2               | PRU_ICSSG PRU Data Input                                    | I            | AF23     |
| PRG1_PRU0_GPI3               | PRU_ICSSG PRU Data Input                                    | I            | AD21     |
| PRG1_PRU0_GPI4               | PRU_ICSSG PRU Data Input                                    | I            | AG23     |
| PRG1_PRU0_GPI5               | PRU_ICSSG PRU Data Input                                    | I            | AF27     |
| PRG1_PRU0_GPI6               | PRU_ICSSG PRU Data Input                                    | I            | AF22     |
| PRG1_PRU0_GPI7               | PRU_ICSSG PRU Data Input                                    | I            | AG27     |
| PRG1_PRU0_GPI8               | PRU_ICSSG PRU Data Input                                    | I            | AF28     |
| PRG1_PRU0_GPI9               | PRU_ICSSG PRU Data Input                                    | I            | AF26     |
| PRG1_PRU0_GPI10              | PRU_ICSSG PRU Data Input                                    | I            | AH25     |
| PRG1_PRU0_GPI11              | PRU_ICSSG PRU Data Input                                    | I            | AF21     |
| PRG1_PRU0_GPI12              | PRU_ICSSG PRU Data Input                                    | I            | AH20     |
| PRG1_PRU0_GPI13              | PRU_ICSSG PRU Data Input                                    | I            | AH21     |
| PRG1_PRU0_GPI14              | PRU_ICSSG PRU Data Input                                    | I            | AG20     |
| PRG1_PRU0_GPI15              | PRU_ICSSG PRU Data Input                                    | I            | AD19     |
| PRG1_PRU0_GPI16              | PRU_ICSSG PRU Data Input                                    | I            | AD20     |
| PRG1_PRU0_GPI17              | PRU_ICSSG PRU Data Input                                    | I            | AH26     |
| PRG1_PRU0_GPI18              | PRU_ICSSG PRU Data Input                                    | I            | AG25     |

**Table 5-54. PRU\_ICSSG1 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]           | PIN TYPE [3] | BALL [4]   |
|-----------------|---------------------------|--------------|------------|
| PRG1_PRU0_GPI19 | PRU_ICSSG PRU Data Input  | I            | AG26       |
| PRG1_PRU0_GPO0  | PRU_ICSSG PRU Data Output | IO           | AE22       |
| PRG1_PRU0_GPO1  | PRU_ICSSG PRU Data Output | IO           | AG24       |
| PRG1_PRU0_GPO2  | PRU_ICSSG PRU Data Output | IO           | AF23       |
| PRG1_PRU0_GPO3  | PRU_ICSSG PRU Data Output | IO           | AD21       |
| PRG1_PRU0_GPO4  | PRU_ICSSG PRU Data Output | IO           | AG23       |
| PRG1_PRU0_GPO5  | PRU_ICSSG PRU Data Output | IO           | AF27       |
| PRG1_PRU0_GPO6  | PRU_ICSSG PRU Data Output | IO           | AF22       |
| PRG1_PRU0_GPO7  | PRU_ICSSG PRU Data Output | IO           | AG27       |
| PRG1_PRU0_GPO8  | PRU_ICSSG PRU Data Output | IO           | AF28       |
| PRG1_PRU0_GPO9  | PRU_ICSSG PRU Data Output | IO           | AF26       |
| PRG1_PRU0_GPO10 | PRU_ICSSG PRU Data Output | IO           | AH25       |
| PRG1_PRU0_GPO11 | PRU_ICSSG PRU Data Output | IO           | AF21, AH20 |
| PRG1_PRU0_GPO12 | PRU_ICSSG PRU Data Output | IO           | AH20, AH21 |
| PRG1_PRU0_GPO13 | PRU_ICSSG PRU Data Output | IO           | AG20, AH21 |
| PRG1_PRU0_GPO14 | PRU_ICSSG PRU Data Output | IO           | AD19, AG20 |
| PRG1_PRU0_GPO15 | PRU_ICSSG PRU Data Output | IO           | AD19, AF21 |
| PRG1_PRU0_GPO16 | PRU_ICSSG PRU Data Output | IO           | AD20       |
| PRG1_PRU0_GPO17 | PRU_ICSSG PRU Data Output | IO           | AH26       |
| PRG1_PRU0_GPO18 | PRU_ICSSG PRU Data Output | IO           | AG25       |
| PRG1_PRU0_GPO19 | PRU_ICSSG PRU Data Output | IO           | AG26       |
| PRG1_PRU1_GPI0  | PRU_ICSSG PRU Data Input  | I            | AH24       |
| PRG1_PRU1_GPI1  | PRU_ICSSG PRU Data Input  | I            | AH23       |
| PRG1_PRU1_GPI2  | PRU_ICSSG PRU Data Input  | I            | AG21       |
| PRG1_PRU1_GPI3  | PRU_ICSSG PRU Data Input  | I            | AH22       |
| PRG1_PRU1_GPI4  | PRU_ICSSG PRU Data Input  | I            | AE21       |
| PRG1_PRU1_GPI5  | PRU_ICSSG PRU Data Input  | I            | AC22       |
| PRG1_PRU1_GPI6  | PRU_ICSSG PRU Data Input  | I            | AG22       |
| PRG1_PRU1_GPI7  | PRU_ICSSG PRU Data Input  | I            | AD23       |
| PRG1_PRU1_GPI8  | PRU_ICSSG PRU Data Input  | I            | AE24       |
| PRG1_PRU1_GPI9  | PRU_ICSSG PRU Data Input  | I            | AF25       |
| PRG1_PRU1_GPI10 | PRU_ICSSG PRU Data Input  | I            | AF24       |
| PRG1_PRU1_GPI11 | PRU_ICSSG PRU Data Input  | I            | AC20       |
| PRG1_PRU1_GPI12 | PRU_ICSSG PRU Data Input  | I            | AE20       |
| PRG1_PRU1_GPI13 | PRU_ICSSG PRU Data Input  | I            | AF19       |
| PRG1_PRU1_GPI14 | PRU_ICSSG PRU Data Input  | I            | AH19       |
| PRG1_PRU1_GPI15 | PRU_ICSSG PRU Data Input  | I            | AG19       |
| PRG1_PRU1_GPI16 | PRU_ICSSG PRU Data Input  | I            | AE19       |
| PRG1_PRU1_GPI17 | PRU_ICSSG PRU Data Input  | I            | AE23       |
| PRG1_PRU1_GPI18 | PRU_ICSSG PRU Data Input  | I            | AD22       |
| PRG1_PRU1_GPI19 | PRU_ICSSG PRU Data Input  | I            | AC21       |
| PRG1_PRU1_GPO0  | PRU_ICSSG PRU Data Output | IO           | AH24       |
| PRG1_PRU1_GPO1  | PRU_ICSSG PRU Data Output | IO           | AH23       |
| PRG1_PRU1_GPO2  | PRU_ICSSG PRU Data Output | IO           | AG21       |
| PRG1_PRU1_GPO3  | PRU_ICSSG PRU Data Output | IO           | AH22       |

**Table 5-54. PRU\_ICSSG1 Signal Descriptions (continued)**

| SIGNAL NAME [1]  | DESCRIPTION [2]                | PIN TYPE [3] | BALL [4]   |
|------------------|--------------------------------|--------------|------------|
| PRG1_PRU1_GPO4   | PRU_ICSSG PRU Data Output      | IO           | AE21       |
| PRG1_PRU1_GPO5   | PRU_ICSSG PRU Data Output      | IO           | AC22       |
| PRG1_PRU1_GPO6   | PRU_ICSSG PRU Data Output      | IO           | AG22       |
| PRG1_PRU1_GPO7   | PRU_ICSSG PRU Data Output      | IO           | AD23       |
| PRG1_PRU1_GPO8   | PRU_ICSSG PRU Data Output      | IO           | AE24       |
| PRG1_PRU1_GPO9   | PRU_ICSSG PRU Data Output      | IO           | AF25       |
| PRG1_PRU1_GPO10  | PRU_ICSSG PRU Data Output      | IO           | AF24       |
| PRG1_PRU1_GPO11  | PRU_ICSSG PRU Data Output      | IO           | AC20, AE20 |
| PRG1_PRU1_GPO12  | PRU_ICSSG PRU Data Output      | IO           | AE20, AF19 |
| PRG1_PRU1_GPO13  | PRU_ICSSG PRU Data Output      | IO           | AF19, AH19 |
| PRG1_PRU1_GPO14  | PRU_ICSSG PRU Data Output      | IO           | AG19, AH19 |
| PRG1_PRU1_GPO15  | PRU_ICSSG PRU Data Output      | IO           | AC20, AG19 |
| PRG1_PRU1_GPO16  | PRU_ICSSG PRU Data Output      | IO           | AE19       |
| PRG1_PRU1_GPO17  | PRU_ICSSG PRU Data Output      | IO           | AE23       |
| PRG1_PRU1_GPO18  | PRU_ICSSG PRU Data Output      | IO           | AD22       |
| PRG1_PRU1_GPO19  | PRU_ICSSG PRU Data Output      | IO           | AC21       |
| PRG1_PWM0_TZ_IN  | PRU_ICSSG PWM Trip Zone Input  | I            | AG25       |
| PRG1_PWM0_TZ_OUT | PRU_ICSSG PWM Trip Zone Output | O            | AG26       |
| PRG1_PWM1_TZ_IN  | PRU_ICSSG PWM Trip Zone Input  | I            | AD22       |
| PRG1_PWM1_TZ_OUT | PRU_ICSSG PWM Trip Zone Output | O            | AC21       |
| PRG1_PWM2_TZ_IN  | PRU_ICSSG PWM Trip Zone Input  | I            | AF24       |
| PRG1_PWM2_TZ_OUT | PRU_ICSSG PWM Trip Zone Output | O            | AE24       |
| PRG1_PWM3_TZ_IN  | PRU_ICSSG PWM Trip Zone Input  | I            | AF26       |
| PRG1_PWM3_TZ_OUT | PRU_ICSSG PWM Trip Zone Output | O            | AF21       |
| PRG1_PWM0_A0     | PRU_ICSSG PWM Output A         | IO           | AH20       |
| PRG1_PWM0_A1     | PRU_ICSSG PWM Output A         | IO           | AG20       |
| PRG1_PWM0_A2     | PRU_ICSSG PWM Output A         | IO           | AD20       |
| PRG1_PWM0_B0     | PRU_ICSSG PWM Output B         | IO           | AH21       |
| PRG1_PWM0_B1     | PRU_ICSSG PWM Output B         | IO           | AD19       |
| PRG1_PWM0_B2     | PRU_ICSSG PWM Output B         | IO           | AH26       |
| PRG1_PWM1_A0     | PRU_ICSSG PWM Output A         | IO           | AE20       |
| PRG1_PWM1_A1     | PRU_ICSSG PWM Output A         | IO           | AH19       |
| PRG1_PWM1_A2     | PRU_ICSSG PWM Output A         | IO           | AE19       |
| PRG1_PWM1_B0     | PRU_ICSSG PWM Output B         | IO           | AF19       |
| PRG1_PWM1_B1     | PRU_ICSSG PWM Output B         | IO           | AG19       |
| PRG1_PWM1_B2     | PRU_ICSSG PWM Output B         | IO           | AE23       |
| PRG1_PWM2_A0     | PRU_ICSSG PWM Output A         | IO           | AF23       |
| PRG1_PWM2_A1     | PRU_ICSSG PWM Output A         | IO           | AF28       |
| PRG1_PWM2_A2     | PRU_ICSSG PWM Output A         | IO           | AG21       |
| PRG1_PWM2_B0     | PRU_ICSSG PWM Output B         | IO           | AG23       |
| PRG1_PWM2_B1     | PRU_ICSSG PWM Output B         | IO           | AH25       |
| PRG1_PWM2_B2     | PRU_ICSSG PWM Output B         | IO           | AE21       |
| PRG1_PWM3_A0     | PRU_ICSSG PWM Output A         | IO           | AE22       |
| PRG1_PWM3_A1     | PRU_ICSSG PWM Output A         | IO           | AF22       |
| PRG1_PWM3_A2     | PRU_ICSSG PWM Output A         | IO           | AD21       |

**Table 5-54. PRU\_ICSSG1 Signal Descriptions (continued)**

| SIGNAL NAME [1]    | DESCRIPTION [2]                             | PIN TYPE [3] | BALL [4] |
|--------------------|---------------------------------------------|--------------|----------|
| PRG1_PWM3_B0       | PRU_ICSSG PWM Output B                      | IO           | AG24     |
| PRG1_PWM3_B1       | PRU_ICSSG PWM Output B                      | IO           | AG27     |
| PRG1_PWM3_B2       | PRU_ICSSG PWM Output B                      | IO           | AF27     |
| PRG1_RGMII1_RXC    | PRU_ICSSG RGMII Receive Clock               | I            | AF22     |
| PRG1_RGMII1_RX_CTL | PRU_ICSSG RGMII Receive Control             | I            | AG23     |
| PRG1_RGMII1_TXC    | PRU_ICSSG RGMII Transmit Clock              | IO           | AD20     |
| PRG1_RGMII1_TX_CTL | PRU_ICSSG RGMII Transmit Control            | O            | AF21     |
| PRG1_RGMII2_RXC    | PRU_ICSSG RGMII Receive Clock               | I            | AG22     |
| PRG1_RGMII2_RX_CTL | PRU_ICSSG RGMII Receive Control             | I            | AE21     |
| PRG1_RGMII2_TXC    | PRU_ICSSG RGMII Transmit Clock              | IO           | AE19     |
| PRG1_RGMII2_TX_CTL | PRU_ICSSG RGMII Transmit Control            | O            | AC20     |
| PRG1_RGMII1_RD0    | PRU_ICSSG RGMII Receive Data                | I            | AE22     |
| PRG1_RGMII1_RD1    | PRU_ICSSG RGMII Receive Data                | I            | AG24     |
| PRG1_RGMII1_RD2    | PRU_ICSSG RGMII Receive Data                | I            | AF23     |
| PRG1_RGMII1_RD3    | PRU_ICSSG RGMII Receive Data                | I            | AD21     |
| PRG1_RGMII1_TD0    | PRU_ICSSG RGMII Transmit Data               | O            | AH20     |
| PRG1_RGMII1_TD1    | PRU_ICSSG RGMII Transmit Data               | O            | AH21     |
| PRG1_RGMII1_TD2    | PRU_ICSSG RGMII Transmit Data               | O            | AG20     |
| PRG1_RGMII1_TD3    | PRU_ICSSG RGMII Transmit Data               | O            | AD19     |
| PRG1_RGMII2_RD0    | PRU_ICSSG RGMII Receive Data                | I            | AH24     |
| PRG1_RGMII2_RD1    | PRU_ICSSG RGMII Receive Data                | I            | AH23     |
| PRG1_RGMII2_RD2    | PRU_ICSSG RGMII Receive Data                | I            | AG21     |
| PRG1_RGMII2_RD3    | PRU_ICSSG RGMII Receive Data                | I            | AH22     |
| PRG1_RGMII2_TD0    | PRU_ICSSG RGMII Transmit Data               | O            | AE20     |
| PRG1_RGMII2_TD1    | PRU_ICSSG RGMII Transmit Data               | O            | AF19     |
| PRG1_RGMII2_TD2    | PRU_ICSSG RGMII Transmit Data               | O            | AH19     |
| PRG1_RGMII2_TD3    | PRU_ICSSG RGMII Transmit Data               | O            | AG19     |
| PRG1_UART0_CTSn    | PRU_ICSSG UART Clear to Send (active low)   | I            | AF26     |
| PRG1_UART0_RTSn    | PRU_ICSSG UART Request to Send (active low) | O            | AH25     |
| PRG1_UART0_RXD     | PRU_ICSSG UART Receive Data                 | I            | AF25     |
| PRG1_UART0_TXD     | PRU_ICSSG UART Transmit Data                | O            | AF24     |

**Table 5-55. PRU\_ICSSG2 Signal Descriptions**

| SIGNAL NAME [1]         | DESCRIPTION [2]                                                        | PIN TYPE [3]     | BALL [4] |
|-------------------------|------------------------------------------------------------------------|------------------|----------|
| PRG2_ECAPH0_IN_APWM_OUT | PRU_ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | IO               | AE16     |
| PRG2_ECAPH0_SYNC_IN     | PRU_ICSSG ECAP Sync Input                                              | I                | AD14     |
| PRG2_ECAPH0_SYNC_OUT    | PRU_ICSSG ECAP Sync Output                                             | O                | AG14     |
| PRG2_IEP0_EDIO_OUTVALID | PRU_ICSSG Industrial Ethernet Digital I/O Outvalid                     | O <sup>(1)</sup> | A23      |
| PRG2_IEP0_EDC_LATCH_IN0 | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input            | I                | AD12     |
| PRG2_IEP0_EDC_LATCH_IN1 | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input            | I                | AE12     |
| PRG2_IEP0_EDC_SYNC_OUT0 | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output            | O                | AH12     |

**Table 5-55. PRU\_ICSSG2 Signal Descriptions (continued)**

| SIGNAL NAME [1]              | DESCRIPTION [2]                                             | PIN TYPE [3] | BALL [4] |
|------------------------------|-------------------------------------------------------------|--------------|----------|
| PRG2_IEP0_EDC_SYNC_OUT1      | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output | O            | AF12     |
| PRG2_IEP0_EDIO_DATA_IN_OUT28 | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output | IO           | R23      |
| PRG2_IEP0_EDIO_DATA_IN_OUT29 | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output | IO           | T24      |
| PRG2_IEP0_EDIO_DATA_IN_OUT30 | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output | IO           | R25      |
| PRG2_IEP0_EDIO_DATA_IN_OUT31 | PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output | IO           | T27      |
| PRG2_IEP1_EDC_LATCH_IN0      | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input | I            | R23      |
| PRG2_IEP1_EDC_LATCH_IN1      | PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input | I            | R25      |
| PRG2_IEP1_EDC_SYNC_OUT0      | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output | O            | T24      |
| PRG2_IEP1_EDC_SYNC_OUT1      | PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output | O            | T27      |
| PRG2_MDIO0_MDC               | PRU_ICSSG MDIO Clock                                        | O            | AE15     |
| PRG2_MDIO0_MDIO              | PRU_ICSSG MDIO Data                                         | IO           | AC19     |
| PRG2_PRU0_GPI0               | PRU_ICSSG PRU Data Input                                    | I            | AF18     |
| PRG2_PRU0_GPI1               | PRU_ICSSG PRU Data Input                                    | I            | AE18     |
| PRG2_PRU0_GPI2               | PRU_ICSSG PRU Data Input                                    | I            | AH17     |
| PRG2_PRU0_GPI3               | PRU_ICSSG PRU Data Input                                    | I            | AG18     |
| PRG2_PRU0_GPI4               | PRU_ICSSG PRU Data Input                                    | I            | AG17     |
| PRG2_PRU0_GPI5               | PRU_ICSSG PRU Data Input                                    | I            | AF17     |
| PRG2_PRU0_GPI6               | PRU_ICSSG PRU Data Input                                    | I            | AE17     |
| PRG2_PRU0_GPI7               | PRU_ICSSG PRU Data Input                                    | I            | AC19     |
| PRG2_PRU0_GPI8               | PRU_ICSSG PRU Data Input                                    | I            | AH16     |
| PRG2_PRU0_GPI9               | PRU_ICSSG PRU Data Input                                    | I            | AG16     |
| PRG2_PRU0_GPI10              | PRU_ICSSG PRU Data Input                                    | I            | AF16     |
| PRG2_PRU0_GPI11              | PRU_ICSSG PRU Data Input                                    | I            | AE16     |
| PRG2_PRU0_GPI12              | PRU_ICSSG PRU Data Input                                    | I            | N23      |
| PRG2_PRU0_GPI13              | PRU_ICSSG PRU Data Input                                    | I            | M26      |
| PRG2_PRU0_GPI14              | PRU_ICSSG PRU Data Input                                    | I            | P28      |
| PRG2_PRU0_GPI15              | PRU_ICSSG PRU Data Input                                    | I            | P27      |
| PRG2_PRU0_GPI16              | PRU_ICSSG PRU Data Input                                    | I            | AD16     |
| PRG2_PRU0_GPI17              | PRU_ICSSG PRU Data Input                                    | I            | P23      |
| PRG2_PRU0_GPO0               | PRU_ICSSG PRU Data Output                                   | IO           | AF18     |
| PRG2_PRU0_GPO1               | PRU_ICSSG PRU Data Output                                   | IO           | AE18     |
| PRG2_PRU0_GPO2               | PRU_ICSSG PRU Data Output                                   | IO           | AH17     |
| PRG2_PRU0_GPO3               | PRU_ICSSG PRU Data Output                                   | IO           | AG18     |
| PRG2_PRU0_GPO4               | PRU_ICSSG PRU Data Output                                   | IO           | AG17     |
| PRG2_PRU0_GPO5               | PRU_ICSSG PRU Data Output                                   | IO           | AF17     |
| PRG2_PRU0_GPO6               | PRU_ICSSG PRU Data Output                                   | IO           | AE17     |
| PRG2_PRU0_GPO7               | PRU_ICSSG PRU Data Output                                   | IO           | AC19     |
| PRG2_PRU0_GPO8               | PRU_ICSSG PRU Data Output                                   | IO           | AH16     |



**Table 5-55. PRU\_ICSSG2 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]           | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------|--------------|----------|
| PRG2_PRU0_GPO9  | PRU_ICSSG PRU Data Output | IO           | AG16     |
| PRG2_PRU0_GPO10 | PRU_ICSSG PRU Data Output | IO           | AF16     |
| PRG2_PRU0_GPO11 | PRU_ICSSG PRU Data Output | IO           | AE16     |
| PRG2_PRU0_GPO12 | PRU_ICSSG PRU Data Output | IO           | N23      |
| PRG2_PRU0_GPO13 | PRU_ICSSG PRU Data Output | IO           | M26      |
| PRG2_PRU0_GPO14 | PRU_ICSSG PRU Data Output | IO           | P28      |
| PRG2_PRU0_GPO15 | PRU_ICSSG PRU Data Output | IO           | P27      |
| PRG2_PRU0_GPO16 | PRU_ICSSG PRU Data Output | IO           | AD16     |
| PRG2_PRU0_GPO17 | PRU_ICSSG PRU Data Output | IO           | P23      |
| PRG2_PRU1_GPI0  | PRU_ICSSG PRU Data Input  | I            | AH15     |
| PRG2_PRU1_GPI1  | PRU_ICSSG PRU Data Input  | I            | AC16     |
| PRG2_PRU1_GPI2  | PRU_ICSSG PRU Data Input  | I            | AD17     |
| PRG2_PRU1_GPI3  | PRU_ICSSG PRU Data Input  | I            | AH14     |
| PRG2_PRU1_GPI4  | PRU_ICSSG PRU Data Input  | I            | AG14     |
| PRG2_PRU1_GPI5  | PRU_ICSSG PRU Data Input  | I            | AG15     |
| PRG2_PRU1_GPI6  | PRU_ICSSG PRU Data Input  | I            | AC17     |
| PRG2_PRU1_GPI7  | PRU_ICSSG PRU Data Input  | I            | AE15     |
| PRG2_PRU1_GPI8  | PRU_ICSSG PRU Data Input  | I            | AD15     |
| PRG2_PRU1_GPI9  | PRU_ICSSG PRU Data Input  | I            | AF14     |
| PRG2_PRU1_GPI10 | PRU_ICSSG PRU Data Input  | I            | AC15     |
| PRG2_PRU1_GPI11 | PRU_ICSSG PRU Data Input  | I            | AD14     |
| PRG2_PRU1_GPI12 | PRU_ICSSG PRU Data Input  | I            | N26      |
| PRG2_PRU1_GPI13 | PRU_ICSSG PRU Data Input  | I            | N25      |
| PRG2_PRU1_GPI14 | PRU_ICSSG PRU Data Input  | I            | P24      |
| PRG2_PRU1_GPI15 | PRU_ICSSG PRU Data Input  | I            | R27      |
| PRG2_PRU1_GPI16 | PRU_ICSSG PRU Data Input  | I            | AE14     |
| PRG2_PRU1_GPI17 | PRU_ICSSG PRU Data Input  | I            | T23      |
| PRG2_PRU1_GPO0  | PRU_ICSSG PRU Data Output | IO           | AH15     |
| PRG2_PRU1_GPO1  | PRU_ICSSG PRU Data Output | IO           | AC16     |
| PRG2_PRU1_GPO2  | PRU_ICSSG PRU Data Output | IO           | AD17     |
| PRG2_PRU1_GPO3  | PRU_ICSSG PRU Data Output | IO           | AH14     |
| PRG2_PRU1_GPO4  | PRU_ICSSG PRU Data Output | IO           | AG14     |
| PRG2_PRU1_GPO5  | PRU_ICSSG PRU Data Output | IO           | AG15     |
| PRG2_PRU1_GPO6  | PRU_ICSSG PRU Data Output | IO           | AC17     |
| PRG2_PRU1_GPO7  | PRU_ICSSG PRU Data Output | IO           | AE15     |
| PRG2_PRU1_GPO8  | PRU_ICSSG PRU Data Output | IO           | AD15     |
| PRG2_PRU1_GPO9  | PRU_ICSSG PRU Data Output | IO           | AF14     |
| PRG2_PRU1_GPO10 | PRU_ICSSG PRU Data Output | IO           | AC15     |
| PRG2_PRU1_GPO11 | PRU_ICSSG PRU Data Output | IO           | AD14     |
| PRG2_PRU1_GPO12 | PRU_ICSSG PRU Data Output | IO           | N26      |
| PRG2_PRU1_GPO13 | PRU_ICSSG PRU Data Output | IO           | N25      |
| PRG2_PRU1_GPO14 | PRU_ICSSG PRU Data Output | IO           | P24      |
| PRG2_PRU1_GPO15 | PRU_ICSSG PRU Data Output | IO           | R27      |
| PRG2_PRU1_GPO16 | PRU_ICSSG PRU Data Output | IO           | AE14     |
| PRG2_PRU1_GPO17 | PRU_ICSSG PRU Data Output | IO           | T23      |



**Table 5-55. PRU\_ICSSG2 Signal Descriptions (continued)**

| SIGNAL NAME [1]    | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|--------------------|----------------------------------|--------------|----------|
| PRG2_PWM0_TZ_IN    | PRU_ICSSG PWM Trip Zone Input    | I            | P28      |
| PRG2_PWM0_TZ_OUT   | PRU_ICSSG PWM Trip Zone Output   | O            | P24      |
| PRG2_PWM1_TZ_IN    | PRU_ICSSG PWM Trip Zone Input    | I            | F18      |
| PRG2_PWM1_TZ_OUT   | PRU_ICSSG PWM Trip Zone Output   | O            | AE14     |
| PRG2_PWM2_TZ_IN    | PRU_ICSSG PWM Trip Zone Input    | I            | P23      |
| PRG2_PWM2_TZ_OUT   | PRU_ICSSG PWM Trip Zone Output   | O            | T23      |
| PRG2_PWM3_TZ_IN    | PRU_ICSSG PWM Trip Zone Input    | I            | AE15     |
| PRG2_PWM3_TZ_OUT   | PRU_ICSSG PWM Trip Zone Output   | O            | AF14     |
| PRG2_PWM0_A0       | PRU_ICSSG PWM Output A           | IO           | AG17     |
| PRG2_PWM0_A1       | PRU_ICSSG PWM Output A           | IO           | AD16     |
| PRG2_PWM0_A2       | PRU_ICSSG PWM Output A           | IO           | AD15     |
| PRG2_PWM0_B0       | PRU_ICSSG PWM Output B           | IO           | AH16     |
| PRG2_PWM0_B1       | PRU_ICSSG PWM Output B           | IO           | AD17     |
| PRG2_PWM0_B2       | PRU_ICSSG PWM Output B           | IO           | AC15     |
| PRG2_PWM1_A0       | PRU_ICSSG PWM Output A           | IO           | R23      |
| PRG2_PWM1_A1       | PRU_ICSSG PWM Output A           | IO           | AD18     |
| PRG2_PWM1_A2       | PRU_ICSSG PWM Output A           | IO           | AE26     |
| PRG2_PWM1_B0       | PRU_ICSSG PWM Output B           | IO           | T24      |
| PRG2_PWM1_B1       | PRU_ICSSG PWM Output B           | IO           | AH18     |
| PRG2_PWM1_B2       | PRU_ICSSG PWM Output B           | IO           | AE28     |
| PRG2_PWM2_A0       | PRU_ICSSG PWM Output A           | IO           | N23      |
| PRG2_PWM2_A1       | PRU_ICSSG PWM Output A           | IO           | P27      |
| PRG2_PWM2_A2       | PRU_ICSSG PWM Output A           | IO           | N25      |
| PRG2_PWM2_B0       | PRU_ICSSG PWM Output B           | IO           | M26      |
| PRG2_PWM2_B1       | PRU_ICSSG PWM Output B           | IO           | N26      |
| PRG2_PWM2_B2       | PRU_ICSSG PWM Output B           | IO           | R27      |
| PRG2_PWM3_A0       | PRU_ICSSG PWM Output A           | IO           | AF18     |
| PRG2_PWM3_A1       | PRU_ICSSG PWM Output A           | IO           | AF17     |
| PRG2_PWM3_A2       | PRU_ICSSG PWM Output A           | IO           | AH15     |
| PRG2_PWM3_B0       | PRU_ICSSG PWM Output B           | IO           | AG18     |
| PRG2_PWM3_B1       | PRU_ICSSG PWM Output B           | IO           | AE17     |
| PRG2_PWM3_B2       | PRU_ICSSG PWM Output B           | IO           | AC16     |
| PRG2_RGMII1_RXC    | PRU_ICSSG RGMII Receive Clock    | I            | AF17     |
| PRG2_RGMII1_RX_CTL | PRU_ICSSG RGMII Receive Control  | I            | AG17     |
| PRG2_RGMII1_TXC    | PRU_ICSSG RGMII Transmit Clock   | IO           | AD16     |
| PRG2_RGMII1_TX_CTL | PRU_ICSSG RGMII Transmit Control | O            | AE17     |
| PRG2_RGMII2_RXC    | PRU_ICSSG RGMII Receive Clock    | I            | AG15     |
| PRG2_RGMII2_RX_CTL | PRU_ICSSG RGMII Receive Control  | I            | AG14     |
| PRG2_RGMII2_TXC    | PRU_ICSSG RGMII Transmit Clock   | IO           | AE14     |
| PRG2_RGMII2_TX_CTL | PRU_ICSSG RGMII Transmit Control | O            | AC17     |
| PRG2_RGMII1_RD0    | PRU_ICSSG RGMII Receive Data     | I            | AF18     |
| PRG2_RGMII1_RD1    | PRU_ICSSG RGMII Receive Data     | I            | AE18     |
| PRG2_RGMII1_RD2    | PRU_ICSSG RGMII Receive Data     | I            | AH17     |
| PRG2_RGMII1_RD3    | PRU_ICSSG RGMII Receive Data     | I            | AG18     |
| PRG2_RGMII1_TD0    | PRU_ICSSG RGMII Transmit Data    | O            | AH16     |

**Table 5-55. PRU\_ICSSG2 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                             | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------------------|--------------|----------|
| PRG2_RGMII1_TD1 | PRU_ICSSG RGMII Transmit Data               | O            | AG16     |
| PRG2_RGMII1_TD2 | PRU_ICSSG RGMII Transmit Data               | O            | AF16     |
| PRG2_RGMII1_TD3 | PRU_ICSSG RGMII Transmit Data               | O            | AE16     |
| PRG2_RGMII2_RD0 | PRU_ICSSG RGMII Receive Data                | I            | AH15     |
| PRG2_RGMII2_RD1 | PRU_ICSSG RGMII Receive Data                | I            | AC16     |
| PRG2_RGMII2_RD2 | PRU_ICSSG RGMII Receive Data                | I            | AD17     |
| PRG2_RGMII2_RD3 | PRU_ICSSG RGMII Receive Data                | I            | AH14     |
| PRG2_RGMII2_TD0 | PRU_ICSSG RGMII Transmit Data               | O            | AD15     |
| PRG2_RGMII2_TD1 | PRU_ICSSG RGMII Transmit Data               | O            | AF14     |
| PRG2_RGMII2_TD2 | PRU_ICSSG RGMII Transmit Data               | O            | AC15     |
| PRG2_RGMII2_TD3 | PRU_ICSSG RGMII Transmit Data               | O            | AD14     |
| PRG2_UART0_CTSn | PRU_ICSSG UART Clear to Send (active low)   | I            | AD12     |
| PRG2_UART0_RTSn | PRU_ICSSG UART Request to Send (active low) | O            | AH12     |
| PRG2_UART0_RXD  | PRU_ICSSG UART Receive Data                 | I            | AE12     |
| PRG2_UART0_TXD  | PRU_ICSSG UART Transmit Data                | O            | AF12     |

(1) When OSC1 is being used with an external crystal, this signal is unavailable. The output functionality must be disabled.

## 5.3.22 SERDES

### 5.3.22.1 MAIN Domain

**Table 5-56. SERDES0 Signal Descriptions**

see (1)

| SIGNAL NAME [1] | DESCRIPTION [2]                              | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------------------|--------------|----------|
| SERDES0_REFCLKN | SERDES Clock Input (negative)                | I            | AG5      |
| SERDES0_REFCLKP | SERDES Clock Input (positive)                | I            | AG6      |
| SERDES0_REFRES  | SERDES Reference Resistor <sup>(2)</sup>     | A            | AC9      |
| SERDES0_RXN     | SERDES Differential Receive Data (negative)  | I            | AH3      |
| SERDES0_RXP     | SERDES Differential Receive Data (positive)  | I            | AG2      |
| SERDES0_TXN     | SERDES Differential Transmit Data (negative) | O            | AH4      |
| SERDES0_TXP     | SERDES Differential Transmit Data (positive) | O            | AG3      |

(1) The functionality of these pins is controlled by CTRLMMR\_SERDES0\_CTRL[1:0] LANE\_FUNC\_SEL. 0x0 = USB3, 0x1 = PCIe0 Lane0, 0x2 = ICSS2 SGMII Lane0.

(2) The required resistor value is 3kΩ ±1%.

**Table 5-57. SERDES1 Signal Descriptions**

see (1)

| SIGNAL NAME [1] | DESCRIPTION [2]                              | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------------------|--------------|----------|
| SERDES1_REFCLKN | SERDES Clock Input (negative)                | I            | AH6      |
| SERDES1_REFCLKP | SERDES Clock Input (positive)                | I            | AH7      |
| SERDES1_REFRES  | SERDES Reference Resistor <sup>(2)</sup>     | A            | AC14     |
| SERDES1_RXN     | SERDES Differential Receive Data (negative)  | I            | AG9      |
| SERDES1_RXP     | SERDES Differential Receive Data (positive)  | I            | AH10     |
| SERDES1_TXN     | SERDES Differential Transmit Data (negative) | O            | AH9      |

**Table 5-57. SERDES1 Signal Descriptions (continued)**

see (1)

| SIGNAL NAME [1] | DESCRIPTION [2]                              | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------------------|--------------|----------|
| SERDES1_TXP     | SERDES Differential Transmit Data (positive) | O            | AG8      |

(1) The functionality of these pins is controlled by CTRLMMR\_SERDES1\_CTRL[1:0] LANE\_FUNC\_SEL. 0x0 = PCIe1 Lane0, 0x1 = PCIe0 Lane1, 0x2 = ICSS2 SGMII Lane1.

**5.3.23 UART****5.3.23.1 MAIN Domain****Table 5-58. UART0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                       | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------------|--------------|----------|
| UART0_CTSn      | UART Clear to Send (active low)       | I            | AG11     |
| UART0_DCDn      | UART Data Carrier Detect (active low) | I            | D25      |
| UART0_DSRn      | UART Data Set Ready (active low)      | I            | B26      |
| UART0_DTRn      | UART Data Terminal Ready (active low) | O            | A24      |
| UART0_RIN       | UART Ring Indicator                   | I            | E24      |
| UART0_RTSn      | UART Request to Send (active low)     | O            | AD11     |
| UART0_RXD       | UART Receive Data                     | I            | AF11     |
| UART0_TXD       | UART Transmit Data                    | O            | AE11     |

**Table 5-59. UART1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------------|--------------|----------|
| UART1_CTSn      | UART Clear to Send (active low)   | I            | AD22     |
| UART1_RTSn      | UART Request to Send (active low) | O            | AC21     |
| UART1_RXD       | UART Receive Data                 | I            | AE23     |
| UART1_TXD       | UART Transmit Data                | O            | AD23     |

**Table 5-60. UART2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------------|--------------|----------|
| UART2_CTSn      | UART Clear to Send (active low)   | I            | Y26      |
| UART2_RTSn      | UART Request to Send (active low) | O            | W26      |
| UART2_RXD       | UART Receive Data                 | I            | Y27      |
| UART2_TXD       | UART Transmit Data                | O            | W28      |

**5.3.23.2 MCU Domain****Table 5-61. UART0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------------|--------------|----------|
| MCU_UART0_CTSn  | UART Clear to Send (active low)   | I            | P1       |
| MCU_UART0_RTSn  | UART Request to Send (active low) | O            | N3       |
| MCU_UART0_RXD   | UART Receive Data                 | I            | P4       |
| MCU_UART0_TXD   | UART Transmit Data                | O            | P5       |

### 5.3.23.3 WKUP Domain

**Table 5-62. UART0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------------|--------------|----------|
| WKUP_UART0_CTSn | UART Clear to Send (active low)   | I            | AC2      |
| WKUP_UART0_RTSn | UART Request to Send (active low) | O            | AC1      |
| WKUP_UART0_RXD  | UART Receive Data                 | I            | AB1      |
| WKUP_UART0_TXD  | UART Transmit Data                | O            | AB5      |

### 5.3.24 USB

#### 5.3.24.1 MAIN Domain

**Table 5-63. USB0 Signal Descriptions**

| SIGNAL NAME [1]          | DESCRIPTION [2]                       | PIN TYPE [3] | BALL [4] |
|--------------------------|---------------------------------------|--------------|----------|
| USB0_DM                  | USB 2.0 Differential Data (negative)  | IO           | AE2      |
| USB0_DP                  | USB 2.0 Differential Data (positive)  | IO           | AF1      |
| USB0_DRVVBUS             | USB VBUS control output (active high) | O            | AD9      |
| USB0_ID                  | USB 2.0 Dual-Role Device Role Select  | A            | AF7      |
| USB0_VBUS <sup>(1)</sup> | USB Level-shifted VBUS Input          | A            | AE7      |

(1) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see [Section 8.2.3, USB Design Guidelines](#).

**Table 5-64. USB1 Signal Descriptions**

| SIGNAL NAME [1]          | DESCRIPTION [2]                       | PIN TYPE [3] | BALL [4] |
|--------------------------|---------------------------------------|--------------|----------|
| USB1_DM                  | USB 2.0 Differential Data (negative)  | IO           | AD2      |
| USB1_DP                  | USB 2.0 Differential Data (positive)  | IO           | AE1      |
| USB1_DRVVBUS             | USB VBUS control output (active high) | O            | AC8      |
| USB1_ID                  | USB 2.0 Dual-Role Device Role Select  | A            | AF5      |
| USB1_VBUS <sup>(1)</sup> | USB Level-shifted VBUS Input          | A            | AF6      |

(1) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see [Section 8.2.3, USB Design Guidelines](#).

### 5.3.25 Emulation and Debug

#### 5.3.25.1 MAIN Domain

**Table 5-65. Emulation and Debug 0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]             | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------|--------------|----------|
| EMU0            | Emulation Control 0         | IO           | AA2      |
| EMU1            | Emulation Control 1         | IO           | AA1      |
| TCK             | JTAG Test Clock Input       | I            | AA4      |
| TDI             | JTAG Test Data Input        | I            | C20      |
| TDO             | JTAG Test Data Output       | OZ           | A20      |
| TMS             | JTAG Test Mode Select Input | I            | A21      |
| TRSTn           | JTAG Reset                  | I            | AA3      |
| TRC_CLK         | Trace Clock                 | O            | AF18     |
| TRC_CTL         | Trace Control               | O            | AE18     |
| TRC_DATA0       | Trace Data 0                | O            | AH17     |
| TRC_DATA1       | Trace Data 1                | O            | AG18     |

**Table 5-65. Emulation and Debug 0 Signal Descriptions (continued)**

| <b>SIGNAL NAME [1]</b> | <b>DESCRIPTION [2]</b> | <b>PIN TYPE [3]</b> | <b>BALL [4]</b> |
|------------------------|------------------------|---------------------|-----------------|
| TRC_DATA2              | Trace Data 2           | O                   | AG17            |
| TRC_DATA3              | Trace Data 3           | O                   | AF17            |
| TRC_DATA4              | Trace Data 4           | O                   | AE17            |
| TRC_DATA5              | Trace Data 5           | O                   | AC19            |
| TRC_DATA6              | Trace Data 6           | O                   | AH16            |
| TRC_DATA7              | Trace Data 7           | O                   | AG16            |
| TRC_DATA8              | Trace Data 8           | O                   | AF16            |
| TRC_DATA9              | Trace Data 9           | O                   | AE16            |
| TRC_DATA10             | Trace Data 10          | O                   | AD16            |
| TRC_DATA11             | Trace Data 11          | O                   | AH15            |
| TRC_DATA12             | Trace Data 12          | O                   | AC16            |
| TRC_DATA13             | Trace Data 13          | O                   | AD17            |
| TRC_DATA14             | Trace Data 14          | O                   | AH14            |
| TRC_DATA15             | Trace Data 15          | O                   | AG14            |
| TRC_DATA16             | Trace Data 16          | O                   | AG15            |
| TRC_DATA17             | Trace Data 17          | O                   | AC17            |
| TRC_DATA18             | Trace Data 18          | O                   | AE15            |
| TRC_DATA19             | Trace Data 19          | O                   | AD15            |
| TRC_DATA20             | Trace Data 20          | O                   | AF14            |
| TRC_DATA21             | Trace Data 21          | O                   | AC15            |
| TRC_DATA22             | Trace Data 22          | O                   | AD14            |
| TRC_DATA23             | Trace Data 23          | O                   | AE14            |

## 5.3.26 System and Miscellaneous

### 5.3.26.1 Boot Mode Configuration

#### 5.3.26.1.1 MAIN Domain

**Table 5-66. Sysboot Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| BOOTMODE00      | Bootmode pin 00 | I            | M27      |
| BOOTMODE01      | Bootmode pin 01 | I            | M23      |
| BOOTMODE02      | Bootmode pin 02 | I            | M28      |
| BOOTMODE03      | Bootmode pin 03 | I            | M24      |
| BOOTMODE04      | Bootmode pin 04 | I            | N24      |
| BOOTMODE05      | Bootmode pin 05 | I            | N27      |
| BOOTMODE06      | Bootmode pin 06 | I            | N28      |
| BOOTMODE07      | Bootmode pin 07 | I            | M25      |
| BOOTMODE08      | Bootmode pin 08 | I            | N23      |
| BOOTMODE09      | Bootmode pin 09 | I            | M26      |
| BOOTMODE10      | Bootmode pin 10 | I            | P28      |
| BOOTMODE11      | Bootmode pin 11 | I            | P27      |
| BOOTMODE12      | Bootmode pin 12 | I            | N26      |
| BOOTMODE13      | Bootmode pin 13 | I            | N25      |
| BOOTMODE14      | Bootmode pin 14 | I            | P24      |
| BOOTMODE15      | Bootmode pin 15 | I            | R27      |
| BOOTMODE16      | Bootmode pin 16 | I            | P25      |
| BOOTMODE17      | Bootmode pin 17 | I            | P26      |
| BOOTMODE18      | Bootmode pin 18 | I            | U28      |

#### 5.3.26.1.2 MCU Domain

**Table 5-67. Sysboot Signal Descriptions**

| SIGNAL NAME [1]               | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-------------------------------|-----------------|--------------|----------|
| MCU_BOOTMODE00                | Bootmode pin 00 | I            | AF4      |
| MCU_BOOTMODE01                | Bootmode pin 01 | I            | AF3      |
| MCU_BOOTMODE02                | Bootmode pin 02 | I            | AE3      |
| MCU_BOOTMODE03 <sup>(1)</sup> | Bootmode pin 03 | I            | AD1      |
| MCU_BOOTMODE04 <sup>(1)</sup> | Bootmode pin 04 | I            | AC3      |
| MCU_BOOTMODE05 <sup>(1)</sup> | Bootmode pin 05 | I            | Y2       |
| MCU_BOOTMODE06 <sup>(1)</sup> | Bootmode pin 06 | I            | Y1       |
| MCU_BOOTMODE07 <sup>(1)</sup> | Bootmode pin 07 | I            | Y3       |
| MCU_BOOTMODE08 <sup>(1)</sup> | Bootmode pin 08 | I            | AC5      |
| MCU_BOOTMODE09                | Bootmode pin 09 | I            | AB4      |

(1) These signals must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low level.

### 5.3.26.2 Clock

#### 5.3.26.2.1 MAIN Domain

**Table 5-68. Clock1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------|--------------|----------|
| OSC1_XI         | High frequency oscillator input  | I            | C22      |
| OSC1_XO         | High frequency oscillator output | O            | E22      |

#### 5.3.26.2.2 WKUP Domain

**Table 5-69. Clock0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                              | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------------------|--------------|----------|
| WKUP_LFOSC0_XI  | Low frequency (32.768 kHz) oscillator input  | I            | AE4      |
| WKUP_LFOSC0_XO  | Low frequency (32.768 kHz) oscillator output | O            | AC4      |
| WKUP_OSC0_XI    | High frequency oscillator input              | I            | AD5      |
| WKUP_OSC0_XO    | High frequency oscillator output             | O            | AE6      |

### 5.3.26.3 System

#### 5.3.26.3.1 MAIN Domain

**Table 5-70. System0 Signal Descriptions**

| SIGNAL NAME [1]   | DESCRIPTION [2]                                                                                                                                                                    | PIN TYPE [3] | BALL [4] |
|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|----------|
| EXT_REFCLK1       | External clock input to Main Domain, routed to Timer clock muxes as one of the selectable input clock sources for Timer/WDT modules, or as reference clock to MAIN_PLL2 (PER1 PLL) | I            | A22      |
| GPMC0_FCLK_MUX    | GPMC functional clock output selected through a mux logic                                                                                                                          | O            | R28      |
| NMIIn             | External Interrupt                                                                                                                                                                 | I            | F18      |
| OBSCLK0           | Observation clock output for test and debug purposes only                                                                                                                          | O            | C23      |
| PORz              | Main Domain cold reset                                                                                                                                                             | I            | E19      |
| PORz_OUT          | Main Domain POR status output                                                                                                                                                      | O            | C19      |
| REFCLK0N          | SERDES Differential Clock Output (negative)                                                                                                                                        | O            | AF9      |
| REFCLK0P          | SERDES Differential Clock Output (positive)                                                                                                                                        | O            | AF10     |
| REFCLK1N          | SERDES Differential Clock Output (negative)                                                                                                                                        | O            | AE8      |
| REFCLK1P          | SERDES Differential Clock Output (positive)                                                                                                                                        | O            | AE9      |
| RESETSTATz        | Main Domain warm reset status output                                                                                                                                               | O            | D19      |
| RESETz            | Main Domain warm reset                                                                                                                                                             | I            | F17      |
| SOC_SAFETY_ERRORn | Error signal output from Main Domain ESM                                                                                                                                           | IO           | E20      |
| SYSCLKOUT0        | SYSCLK0 output from Main PLL controller (divided by 4) for test and debug purposes only                                                                                            | O            | B22      |

#### 5.3.26.3.2 WKUP Domain

**Table 5-71. System0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                                                                                   | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------------------------------------------------------------------------|--------------|----------|
| MCU_BYP_POR     | MCU Bypass reset circuitry input. 0 = Internal POR is used, 1 = External MCU_PORz signal is used. | I            | V5       |
| MCU_CLKOUT0     | Reference clock output for Ethernet PHYs (50MHz or 25MHz)                                         | O            | AB2      |

**Table 5-71. System0 Signal Descriptions (continued)**

| SIGNAL NAME [1]   | DESCRIPTION [2]                                                                | PIN TYPE [3] | BALL [4] |
|-------------------|--------------------------------------------------------------------------------|--------------|----------|
| MCU_EXT_REFCLK0   | External system clock input                                                    | I            | AB3      |
| MCU_OBSCLK0       | Observation clock output for test and debug purposes only                      | O            | AB2      |
| MCU_PORz          | MCU Domain cold reset                                                          | I            | W5       |
| MCU_PORz_OUT      | MCU Domain POR status output                                                   | O            | V2       |
| MCU_RESETSTATz    | MCU Domain warm reset status output                                            | O            | V3       |
| MCU_RESETz        | MCU Domain warm reset                                                          | I            | W4       |
| MCU_SAFETY_ERRORn | Error signal output from MCU Domain ESM                                        | IO           | W3       |
| MCU_SYSCCLKOUT0   | MCU Domain system clock output (divided by 4) for test and debug purposes only | O            | AB3      |
| PMIC_POWER_EN0    | Power enable output for MAIN Domain supplies                                   | O            | Y5       |
| PMIC_POWER_EN1    | Power enable output for MAIN Domain supplies                                   | O            | AA5      |

### 5.3.26.4 Miscellaneous

#### 5.3.26.4.1 WKUP Domain

**Table 5-72. Miscellaneous0 Signal Descriptions**

| SIGNAL NAME [1]             | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------------------|-----------------|--------------|----------|
| TEMP_DIODE_P <sup>(1)</sup> | Reserved        | A            | W6       |

(1) Do not connect any signal, test point, or board trace to this signal.

### 5.3.26.5 EFUSE

#### 5.3.26.5.1 MAIN Domain

**Table 5-73. EFUSE0 Signal Descriptions**

| SIGNAL NAME [1]         | DESCRIPTION [2]                            | PIN TYPE [3] | BALL [4] |
|-------------------------|--------------------------------------------|--------------|----------|
| VPP_CORE <sup>(1)</sup> | Programming voltage for MAIN Domain efuses | PWR          | F21      |

(1) This signal is valid only for High-Security devices. For more details, see [Section 6.7, VPP Specification for One-Time Programmable \(OTP\) eFUSES](#). For General Purpose devices do not connect any signal, test point, or board trace to this signal.

#### 5.3.26.5.2 MCU Domain

**Table 5-74. EFUSE0 Signal Descriptions**

| SIGNAL NAME [1]        | DESCRIPTION [2]                           | PIN TYPE [3] | BALL [4] |
|------------------------|-------------------------------------------|--------------|----------|
| VPP_MCU <sup>(1)</sup> | Programming voltage for MCU Domain efuses | PWR          | T6       |

(1) This signal is valid only for High-Security devices. For more details, see [Section 6.7, VPP Specification for One-Time Programmable \(OTP\) eFUSES](#). For General Purpose devices do not connect any signal, test point, or board trace to this signal.

### 5.3.27 Power Supply

**Table 5-75. Power Supply Signal Description**

| SIGNAL NAME [1]                | DESCRIPTION [2]                                  | PIN TYPE [3] | BALL [4] |
|--------------------------------|--------------------------------------------------|--------------|----------|
| CAP_VDDAR_CORE0 <sup>(1)</sup> | External capacitor connection for CORE SRAM LDOs | CAP          | P17      |
| CAP_VDDAR_CORE1 <sup>(1)</sup> | External capacitor connection for CORE SRAM LDOs | CAP          | V17      |
| CAP_VDDAR_CORE2 <sup>(1)</sup> | External capacitor connection for CORE SRAM LDOs | CAP          | W16      |
| CAP_VDDAR_CORE3 <sup>(1)</sup> | External capacitor connection for MSMC SRAM LDOs | CAP          | M14      |
| CAP_VDDAR_CORE4 <sup>(1)</sup> | External capacitor connection for MSMC SRAM LDOs | CAP          | L15      |



**Table 5-75. Power Supply Signal Description (continued)**

| SIGNAL NAME [1]                        | DESCRIPTION [2]                                                                            | PIN TYPE [3] | BALL [4]         |
|----------------------------------------|--------------------------------------------------------------------------------------------|--------------|------------------|
| CAP_VDDAR_MCU <sup>(1)</sup>           | External capacitor connection for MCU SRAM LDO                                             | CAP          | U10              |
| CAP_VDDAR_MPU0_0 <sup>(1)</sup>        | External capacitor connection for MPU SRAM LDOs                                            | CAP          | M12              |
| CAP_VDDAR_MPU0_1 <sup>(1)</sup>        | External capacitor connection for MPU SRAM LDOs                                            | CAP          | N12              |
| CAP_VDDAR_MPU1_0 <sup>(1)</sup>        | External capacitor connection for MPU SRAM LDOs                                            | CAP          | N18              |
| CAP_VDDAR_MPU1_1 <sup>(1)</sup>        | External capacitor connection for MPU SRAM LDOs                                            | CAP          | N15              |
| CAP_VDDAR_WKUP <sup>(1)</sup>          | External capacitor connection for WKUP SRAM LDO                                            | CAP          | Y10              |
| CAP_VDDA_1P8_IOLDO_WKUP <sup>(1)</sup> | External capacitor connection for IO Bias LDO in WKUP domain                               | CAP          | AA8              |
| CAP_VDDA_1P8_SDIO <sup>(2)</sup>       | External capacitor connection for SDIO LDO                                                 | CAP          | J17              |
| CAP_VDDA_1P8_IOLDO0 <sup>(1)</sup>     | External capacitor connection for IO Bias LDO                                              | CAP          | G19              |
| CAP_VDDA_1P8_IOLDO1 <sup>(1)</sup>     | External capacitor connection for IO Bias LDO                                              | CAP          | Y19              |
| CAP_VDDSHV_SDIO <sup>(2) (3)</sup>     | External capacitor connection for SDIO LDO                                                 | CAP          | H18              |
| CAP_VDD_WKUP <sup>(1)</sup>            | External capacitor connection for WKUP LDO                                                 | CAP          | V9               |
| VDDA_1P8_MON_WKUP                      | Supply monitor in WKUP domain                                                              | A            | AB6              |
| VDDA_1P8_SDIO <sup>(2)</sup>           | SDIO LDO analog power supply                                                               | PWR          | G17              |
| VDDA_1P8_CSI0                          | CSI PHY analog power supply                                                                | PWR          | L20, M21         |
| VDDA_1P8_MON0                          | Supply monitor in MAIN domain                                                              | A            | AC6              |
| VDDA_1P8_OLDIO                         | OLDI analog power supply                                                                   | PWR          | L22              |
| VDDA_1P8_SERDES0                       | SERDES0/1 (USB, PCIE) analog power supply                                                  | PWR          | AA14, AB13, AB15 |
| VDDA_3P3_IOLDO_WKUP                    | WKUP IO Bias LDO analog power supply                                                       | PWR          | AB9              |
| VDDA_3P3_MON_WKUP                      | Supply monitor in WKUP domain                                                              | A            | U6               |
| VDDA_3P3_SDIO <sup>(2)</sup>           | SDIO LDO analog power supply                                                               | PWR          | H17              |
| VDDA_3P3_USB                           | USB analog power supply                                                                    | PWR          | AC12             |
| VDDA_3P3_IOLDO0                        | IO Bias LDO analog power supply                                                            | PWR          | G18              |
| VDDA_3P3_IOLDO1                        | IO Bias LDO analog power supply                                                            | PWR          | AA21             |
| VDDA_3P3_MON0                          | Supply monitor in MAIN domain                                                              | A            | AC10             |
| VDDA_ADC_MCU                           | ADC0, ADC1 analog power supply                                                             | PWR          | M7, M9           |
| VDDA_LDO_WKUP                          | WKUP LDO analog power supply                                                               | PWR          | AB8              |
| VDDA_MCU                               | MCU SRAM LDO, MCU DPLL, CPSW DPLL analog power supply                                      | PWR          | U12              |
| VDDA_PLL0_DDR                          | DDR DPLL analog power supply                                                               | PWR          | H15              |
| VDDA_PLL1_DDR                          | DDR De-skew DPLL analog power supply                                                       | PWR          | H11              |
| VDDA_PLL_CORE                          | CORE DPLL, PER1 DPLL analog power supply                                                   | PWR          | Y17              |
| VDDA_PLL_DSS                           | DSS DPLL analog power supply                                                               | PWR          | L21              |
| VDDA_PLL_MPU0                          | MPU0 DPLL analog power supply                                                              | PWR          | L12              |
| VDDA_PLL_MPU1                          | MPU1 DPLL analog power supply                                                              | PWR          | K15              |
| VDDA_PLL_PER0                          | PER0 DPLL analog power supply                                                              | PWR          | AB7              |
| VDDA_POR_WKUP <sup>(5)</sup>           | WKUP POR/POK analog power supply                                                           | PWR          | Y9               |
| VDDA_SRAM_CORE0                        | CORE SRAM LDOs analog power supply                                                         | PWR          | M19              |
| VDDA_SRAM_CORE1                        | CORE SRAM LDOs analog power supply                                                         | PWR          | V16              |
| VDDA_SRAM_MPU0                         | MPU SRAM LDOs analog power supply                                                          | PWR          | K7               |
| VDDA_SRAM_MPU1                         | MPU SRAM LDOs analog power supply                                                          | PWR          | L18              |
| VDDA_VSYS_MON <sup>(6)</sup>           | Supply monitor for system                                                                  | A            | AC11             |
| VDDA_WKUP                              | WKUP High/Low Frequency Oscillator (WKUP_LFOSC0 / WKUP_OSC0), SRAM LDO analog power supply | PWR          | AA9              |

**Table 5-75. Power Supply Signal Description (continued)**

| SIGNAL NAME [1]          | DESCRIPTION [2]                                           | PIN TYPE [3] | BALL [4]                                                                                                                                                       |
|--------------------------|-----------------------------------------------------------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDDS0                    | IO bias supply for VDDSHV0                                | PWR          | G12                                                                                                                                                            |
| VDDS0_WKUP               | IO bias supply for VDDSHV0_WKUP                           | PWR          | V8                                                                                                                                                             |
| VDDS1                    | IO bias supply for VDDSHV1                                | PWR          | AA16                                                                                                                                                           |
| VDDS1_WKUP               | IO bias supply for VDDSHV1_WKUP                           | PWR          | T9                                                                                                                                                             |
| VDDS2                    | IO bias supply for VDDSHV2                                | PWR          | P20                                                                                                                                                            |
| VDDS2_WKUP               | IO bias supply for VDDSHV2_WKUP                           | PWR          | N8                                                                                                                                                             |
| VDDS3                    | IO bias supply for VDDSHV3                                | PWR          | T20                                                                                                                                                            |
| VDDS4                    | IO bias supply for VDDSHV4                                | PWR          | Y20                                                                                                                                                            |
| VDDS5                    | IO bias supply for VDDSHV5                                | PWR          | AC18                                                                                                                                                           |
| VDDS6                    | IO bias supply for VDDSHV6                                | PWR          | F20                                                                                                                                                            |
| VDDS7                    | IO bias supply for VDDSHV7                                | PWR          | K20                                                                                                                                                            |
| VDDS8                    | IO bias supply for VDDSHV8                                | PWR          | AA10                                                                                                                                                           |
| VDDSHV0                  | Dual-voltage IO domain power supply                       | PWR          | G15, H16                                                                                                                                                       |
| VDDSHV0_WKUP             | Dual-voltage IO domain power supply                       | PWR          | U8, V7, W8, Y7                                                                                                                                                 |
| VDDSHV1                  | Dual-voltage IO domain power supply                       | PWR          | AA18, AB17                                                                                                                                                     |
| VDDSHV1_WKUP             | Dual-voltage IO domain power supply                       | PWR          | R6, R8, T7                                                                                                                                                     |
| VDDSHV2                  | Dual-voltage IO domain power supply                       | PWR          | N20, N22, P21, R20, R22                                                                                                                                        |
| VDDSHV2_WKUP             | Dual-voltage IO domain power supply                       | PWR          | N6, P7, P9                                                                                                                                                     |
| VDDSHV3                  | Dual-voltage IO domain power supply                       | PWR          | T21, U20, U22, V21, V23                                                                                                                                        |
| VDDSHV4                  | Dual-voltage IO domain power supply                       | PWR          | AA22, W20, W22, Y21, Y23                                                                                                                                       |
| VDDSHV5                  | Dual-voltage IO domain power supply                       | PWR          | AA20, AB19, AB21, AB23                                                                                                                                         |
| VDDSHV6                  | Dual-voltage IO domain power supply                       | PWR          | G20, H19, H21                                                                                                                                                  |
| VDDSHV7                  | Dual-voltage IO domain power supply                       | PWR          | J20, J22, K21                                                                                                                                                  |
| VDDSHV8                  | Dual-voltage IO domain power supply                       | PWR          | AB11                                                                                                                                                           |
| VDDS_DDR                 | DDR IO domain power supply                                | PWR          | G10, G14, G8, H13, H7, H9                                                                                                                                      |
| VDDS_OSC1                | MAIN High Frequency Oscillator (OSC1) analog power supply | PWR          | J16                                                                                                                                                            |
| VDD_CORE                 | CORE voltage domain supply                                | PWR          | AA12, J10, J12, J14, J19, J8, K13, L14, L19, M13, N14, P13, P15, P19, R14, R16, R18, T13, T15, T17, T19, U14, U16, U18, V13, V15, V19, W14, W18, Y11, Y13, Y15 |
| VDD_DLL_MMC0             | MMC0 PHY DLL voltage supply                               | PWR          | G22                                                                                                                                                            |
| VDD_DLL_MMC1             | MMC1 PHY DLL voltage supply                               | PWR          | H23                                                                                                                                                            |
| VDD_MCU                  | MCU voltage domain supply                                 | PWR          | N10, P11, R10, R12, T11                                                                                                                                        |
| VDD_MPU0                 | MPU0 voltage domain supply                                | PWR          | K11, K9, L10, L8, M11                                                                                                                                          |
| VDD_MPU1                 | MPU1 voltage domain supply                                | PWR          | K16, K18, L17, M16, M18, N17                                                                                                                                   |
| VDD_WKUP0 <sup>(4)</sup> | WKUP voltage domain supply                                | PWR          | V11, W10, W12                                                                                                                                                  |
| VDD_WKUP1 <sup>(4)</sup> | WKUP voltage domain supply                                | PWR          | M22                                                                                                                                                            |

**Table 5-75. Power Supply Signal Description (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----------------|-----------------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VSS             | Ground          | GND          | A1, A2, A28, AA11,<br>AA13, AA15, AA17,<br>AA19, AA23, AA26,<br>AA7, AB10, AB12,<br>AB14, AB16, AB18,<br>AB20, AB22, AD4,<br>AE10, AE25, AE5,<br>AF15, AF2, AF20,<br>AF8, AG1, AG10,<br>AG28, AG4, AG7,<br>AH1, AH11, AH2,<br>AH27, AH28, AH5,<br>AH8, B12, B15, B20,<br>B6, B9, D22, E26,<br>E28, E4, F14, F19,<br>F22, F25, F27, F3,<br>G11, G13, G16, G2,<br>G21, G23, G7, G9,<br>H1, H10, H12, H14,<br>H20, H22, H24, H26,<br>H28, H6, H8, J11,<br>J13, J15, J18, J21,<br>J23, J25, J27, J7, J9,<br>K1, K10, K12, K14,<br>K17, K19, K22, K23,<br>K6, K8, L11, L13,<br>L16, L23, L24, L26,<br>L28, L3, L7, L9, M10,<br>M15, M17, M20, M8,<br>N11, N13, N16, N19,<br>N21, N7, N9, P10,<br>P12, P14, P16, P18,<br>P22, P6, P8, R11,<br>R13, R15, R17, R19,<br>R21, R7, R9, T10,<br>T12, T14, T16, T18,<br>T22, T26, T8, U11,<br>U13, U15, U17, U19,<br>U21, U3, U7, U9,<br>V10, V12, V14, V18,<br>V20, V22, V6, W11,<br>W13, W15, W17,<br>W19, W21, W23, W7,<br>W9, Y12, Y14, Y16,<br>Y18, Y22, Y6, Y8 |

- (1) This pin must always be connected via a 1- $\mu$ F capacitor to VSS.
- (2) The net connecting CAP\_VDDA\_1P8\_SDIO and VDDA\_1P8\_SDIO to VDDSHV6 or VDDSHV7 must be connected to a 3.3- $\mu$ F decoupling capacitor. VDDA\_1P8\_SDIO, CAP\_VDDA\_1P8\_SDIO, CAP\_VDDSHV\_SDIO, and VDDA\_3P3\_SDIO must be connected to VSS, when SDIO\_LDO is not used with either MMC0 or MMC1.
- (3) When CAP\_VDDSHV\_SDIO is connected to VDDSHV6 or VDDSHV7, the entire net which connects these pins should not exceed 6- $\mu$ F of decoupling capacitance. VDDA\_1P8\_SDIO, CAP\_VDDA\_1P8\_SDIO, CAP\_VDDSHV\_SDIO, and VDDA\_3P3\_SDIO must be connected to VSS, when SDIO\_LDO is not used with either MMC0 or MMC1.
- (4) These power rails should be connected together on the board level.
- (5) VDDA\_POR\_WKUP is preferred to be connected to CAP\_VDDA\_1P8\_IOLDO\_WKUP when using internal POR feature.
- (6) The VDDA\_VSYS\_MON pin provides a way to monitor the system power supply and is not fail-safe, unless implemented with the appropriate resistor voltage divider source. For more information, see [Section 8.2.5, System Power Supply Monitor Design Guidelines](#).

## 5.4 Pin Multiplexing

[Table 5-76](#) describes the device pin multiplexing associated with pins.

### Note

Many device pins support multiple signal functions. Some signal functions are selected via a single layer of multiplexers associated with pins. Other signal functions are selected via two or more layers of multiplexers, where one layer is associated with the pins and other layers are associated with peripheral logic functions.

[Table 5-76](#), *Pin Multiplexing* only describes signal multiplexing at the pins. For more information, related to signal multiplexing at the pins, see section *Pad Configuration Registers* in the device TRM. Refer to the respective peripheral chapter in the device TRM for information associated with peripheral signal multiplexing.

### Note

When a pad is set into a pin multiplexing mode which is not defined, that pad's behavior is undefined. This should be avoided.

### Note

[Table 5-76](#), *Pin Multiplexing* does not include SerDes signal functions. For more information, see section *Serializer/Deserializer (SerDes)* in the device TRM.

### Note

The PRU\_ICSSG contains a second layer of multiplexing to enable additional functionality on the PRU GPO and GPI signals. This internal wrapper multiplexing is described in the PRU\_ICSSG chapter in the device TRM.

For more information on the I/O cell configurations, see section *Pad Configuration Registers* in the device TRM.

**Table 5-76. Pin Multiplexing**

| ADDRESS    | REGISTER NAME      | BALL<br>NUMBER | MUXMODE[7:0] SETTINGS |             |             |   |   |   |   |         |            |
|------------|--------------------|----------------|-----------------------|-------------|-------------|---|---|---|---|---------|------------|
|            |                    |                | 0                     | 1           | 2           | 3 | 4 | 5 | 6 | 7       | Bootstrap  |
| 0x0011C000 | CTRLMMR_PADCONFIG0 | M27            | GPMC0_AD0             | VOUT1_DATA0 | VIN0_DATA12 |   |   |   |   | GPIO0_0 | BOOTMODE00 |
| 0x0011C004 | CTRLMMR_PADCONFIG1 | M23            | GPMC0_AD1             | VOUT1_DATA1 | VIN0_DATA13 |   |   |   |   | GPIO0_1 | BOOTMODE01 |
| 0x0011C008 | CTRLMMR_PADCONFIG2 | M28            | GPMC0_AD2             | VOUT1_DATA2 | VIN0_DATA14 |   |   |   |   | GPIO0_2 | BOOTMODE02 |
| 0x0011C00C | CTRLMMR_PADCONFIG3 | M24            | GPMC0_AD3             | VOUT1_DATA3 | VIN0_DATA15 |   |   |   |   | GPIO0_3 | BOOTMODE03 |
| 0x0011C010 | CTRLMMR_PADCONFIG4 | N24            | GPMC0_AD4             | VOUT1_DATA4 |             |   |   |   |   | GPIO0_4 | BOOTMODE04 |
| 0x0011C014 | CTRLMMR_PADCONFIG5 | N27            | GPMC0_AD5             | VOUT1_DATA5 |             |   |   |   |   | GPIO0_5 | BOOTMODE05 |
| 0x0011C018 | CTRLMMR_PADCONFIG6 | N28            | GPMC0_AD6             | VOUT1_DATA6 |             |   |   |   |   | GPIO0_6 | BOOTMODE06 |
| 0x0011C01C | CTRLMMR_PADCONFIG7 | M25            | GPMC0_AD7             | VOUT1_DATA7 |             |   |   |   |   | GPIO0_7 | BOOTMODE07 |

**Table 5-76. Pin Multiplexing (continued)**

| ADDRESS    | REGISTER NAME       | BALL NUMBER | MUXMODE[7:0] SETTINGS |                 |                 |                 |                         |                 |                              |          |            |
|------------|---------------------|-------------|-----------------------|-----------------|-----------------|-----------------|-------------------------|-----------------|------------------------------|----------|------------|
|            |                     |             | 0                     | 1               | 2               | 3               | 4                       | 5               | 6                            | 7        | Bootstrap  |
| 0x0011C020 | CTRLMMR_PADCONFIG8  | N23         | GPMC0_AD8             | VOUT1_DATA8     | VIN0_DATA0      | PRG2_PRU0_GPO12 | PRG2_PRU0_GPI12         | PRG2_PWM2_A0    |                              | GPIO0_8  | BOOTMODE08 |
| 0x0011C024 | CTRLMMR_PADCONFIG9  | M26         | GPMC0_AD9             | VOUT1_DATA9     | VIN0_DATA1      | PRG2_PRU0_GPO13 | PRG2_PRU0_GPI13         | PRG2_PWM2_B0    |                              | GPIO0_9  | BOOTMODE09 |
| 0x0011C028 | CTRLMMR_PADCONFIG10 | P28         | GPMC0_AD10            | VOUT1_DATA10    | VIN0_DATA2      | PRG2_PRU0_GPO14 | PRG2_PRU0_GPI14         |                 | PRG2_PWM0_TZ_IN              | GPIO0_10 | BOOTMODE10 |
| 0x0011C02C | CTRLMMR_PADCONFIG11 | P27         | GPMC0_AD11            | VOUT1_DATA11    | VIN0_DATA3      | PRG2_PRU0_GPO15 | PRG2_PRU0_GPI15         | PRG2_PWM2_A1    |                              | GPIO0_11 | BOOTMODE11 |
| 0x0011C030 | CTRLMMR_PADCONFIG12 | N26         | GPMC0_AD12            | VOUT1_DATA12    | VIN0_DATA4      | PRG2_PRU1_GPO12 | PRG2_PRU1_GPI12         | PRG2_PWM2_B1    |                              | GPIO0_12 | BOOTMODE12 |
| 0x0011C034 | CTRLMMR_PADCONFIG13 | N25         | GPMC0_AD13            | VOUT1_DATA13    | VIN0_DATA5      | PRG2_PRU1_GPO13 | PRG2_PRU1_GPI13         | PRG2_PWM2_A2    |                              | GPIO0_13 | BOOTMODE13 |
| 0x0011C038 | CTRLMMR_PADCONFIG14 | P24         | GPMC0_AD14            | VOUT1_DATA14    | VIN0_DATA6      | PRG2_PRU1_GPO14 | PRG2_PRU1_GPI14         |                 | PRG2_PWM0_TZ_OUT             | GPIO0_14 | BOOTMODE14 |
| 0x0011C03C | CTRLMMR_PADCONFIG15 | R27         | GPMC0_AD15            | VOUT1_DATA15    | VIN0_DATA7      | PRG2_PRU1_GPO15 | PRG2_PRU1_GPI15         | PRG2_PWM2_B2    |                              | GPIO0_15 | BOOTMODE15 |
| 0x0011C040 | CTRLMMR_PADCONFIG16 | R28         | GPMC0_CLK             | VOUT1_DATA16    | VIN0_PCLK       | GPMC0_FCLK_MUX  |                         |                 |                              | GPIO0_16 |            |
| 0x0011C044 | CTRLMMR_PADCONFIG17 | P25         | GPMC0_ADVn_AL E       | VOUT1_DATA17    |                 |                 |                         |                 |                              | GPIO0_17 | BOOTMODE16 |
| 0x0011C048 | CTRLMMR_PADCONFIG18 | P26         | GPMC0_OEn_REn         | VOUT1_DATA18    |                 |                 |                         |                 |                              | GPIO0_18 | BOOTMODE17 |
| 0x0011C04C | CTRLMMR_PADCONFIG19 | U28         | GPMC0_WEn             | VOUT1_DATA19    |                 |                 |                         |                 |                              | GPIO0_19 | BOOTMODE18 |
| 0x0011C050 | CTRLMMR_PADCONFIG20 | T28         | GPMC0_BE0n_CLE        | VOUT1_DATA20    |                 |                 |                         |                 |                              | GPIO0_20 |            |
| 0x0011C054 | CTRLMMR_PADCONFIG21 | P23         | GPMC0_BE1n            | VOUT1_DATA21    | VIN0_HD         | PRG2_PRU0_GPO17 | PRG2_PRU0_GPI17         | TIMER_IO2       | PRG2_PWM2_TZ_IN              | GPIO0_21 |            |
| 0x0011C058 | CTRLMMR_PADCONFIG22 | R26         | GPMC0_WAIT0           | VOUT1_DATA22    |                 |                 |                         |                 |                              | GPIO0_22 |            |
| 0x0011C05C | CTRLMMR_PADCONFIG23 | R23         | GPMC0_WAIT1           | VOUT1_DATA23    | VIN0_VD         | PRG2_PWM1_A0    | PRG2_IEP1_EDC_LATCH_IN0 | TIMER_IO3       | PRG2_IEP0_EDIO_DATA_IN_OUT28 | GPIO0_23 |            |
| 0x0011C060 | CTRLMMR_PADCONFIG24 | T25         | GPMC0_WPn             | VOUT1_VSYNC     |                 |                 |                         |                 |                              | GPIO0_24 |            |
| 0x0011C064 | CTRLMMR_PADCONFIG25 | T24         | GPMC0_DIR             | VOUT1_HSYNC     | VIN0_DATA8      | PRG2_PWM1_B0    | PRG2_IEP1_EDC_SYNC_OUT0 | TIMER_IO6       | PRG2_IEP0_EDIO_DATA_IN_OUT29 | GPIO0_25 |            |
| 0x0011C068 | CTRLMMR_PADCONFIG26 | R24         | GPMC0_CSn0            | VOUT1_PCLK      |                 |                 |                         |                 |                              | GPIO0_26 |            |
| 0x0011C06C | CTRLMMR_PADCONFIG27 | T23         | GPMC0_CSn1            | VOUT1_DE        | VIN0_DATA9      | PRG2_PRU1_GPO17 | PRG2_PRU1_GPI17         | TIMER_IO7       | PRG2_PWM2_TZ_OUT             | GPIO0_27 |            |
| 0x0011C070 | CTRLMMR_PADCONFIG28 | R25         | GPMC0_CSn2            | VOUT1_EXTPLCKIN | VIN0_DATA10     | GPMC0_A27       | PRG2_IEP1_EDC_LATCH_IN1 | I2C2_SDA        | PRG2_IEP0_EDIO_DATA_IN_OUT30 | GPIO0_28 |            |
| 0x0011C074 | CTRLMMR_PADCONFIG29 | T27         | GPMC0_CSn3            |                 | VIN0_DATA11     | GPMC0_A26       | PRG2_IEP1_EDC_SYNC_OUT1 | I2C2_SCL        | PRG2_IEP0_EDIO_DATA_IN_OUT31 | GPIO0_29 |            |
| 0x0011C078 | CTRLMMR_PADCONFIG30 | AF18        | PRG2_PRU0_GPO0        | PRG2_PRU0_GPI0  | PRG2_RGMII1_RD0 | GPMC0_A25       | TRC_CLK                 | EHRPWM0_SYNCI   | PRG2_PWM3_A0                 | GPIO0_30 |            |
| 0x0011C07C | CTRLMMR_PADCONFIG31 | AE18        | PRG2_PRU0_GPO1        | PRG2_PRU0_GPI1  | PRG2_RGMII1_RD1 | GPMC0_A24       | TRC_CTL                 | EHRPWM0_SYNC O  | SYNC2_OUT                    | GPIO0_31 |            |
| 0x0011C080 | CTRLMMR_PADCONFIG32 | AH17        | PRG2_PRU0_GPO2        | PRG2_PRU0_GPI2  | PRG2_RGMII1_RD2 | GPMC0_A23       | TRC_DATA0               | EHRPWM0_TZn_IN0 | SYNC3_OUT                    | GPIO0_32 |            |

Table 5-76. Pin Multiplexing (continued)

| ADDRESS    | REGISTER NAME       | BALL NUMBER | MUXMODE[7:0] SETTINGS |                     |                        |              |            |                    |                            |          | Bootstrap |
|------------|---------------------|-------------|-----------------------|---------------------|------------------------|--------------|------------|--------------------|----------------------------|----------|-----------|
|            |                     |             | 0                     | 1                   | 2                      | 3            | 4          | 5                  | 6                          | 7        |           |
| 0x0011C084 | CTRLMMR_PADCONFIG33 | AG18        | PRG2_PRU0_GPO<br>3    | PRG2_PRU0_GPI<br>3  | PRG2_RGMII1_RD<br>3    | GPMC0_A22    | TRC_DATA1  | EHRPWM0_A          | PRG2_PWM3_B0               | GPIO0_33 |           |
| 0x0011C088 | CTRLMMR_PADCONFIG34 | AG17        | PRG2_PRU0_GPO<br>4    | PRG2_PRU0_GPI<br>4  | PRG2_RGMII1_RX<br>_CTL | GPMC0_A21    | TRC_DATA2  | EHRPWM0_B          | PRG2_PWM0_A0               | GPIO0_34 |           |
| 0x0011C08C | CTRLMMR_PADCONFIG35 | AF17        | PRG2_PRU0_GPO<br>5    | PRG2_PRU0_GPI<br>5  | PRG2_RGMII1_RX<br>C    | GPMC0_A20    | TRC_DATA3  | EHRPWM1_A          | PRG2_PWM3_A1               | GPIO0_35 |           |
| 0x0011C090 | CTRLMMR_PADCONFIG36 | AE17        | PRG2_PRU0_GPO<br>6    | PRG2_PRU0_GPI<br>6  | PRG2_RGMII1_TX<br>_CTL | GPMC0_A19    | TRC_DATA4  | EHRPWM1_B          | PRG2_PWM3_B1               | GPIO0_36 |           |
| 0x0011C094 | CTRLMMR_PADCONFIG37 | AC19        | PRG2_PRU0_GPO<br>7    | PRG2_PRU0_GPI<br>7  | PRG2_MDIO0_MD<br>IO    | GPMC0_A18    | TRC_DATA5  | EHRPWM_TZn_IN<br>1 | EHRPWM_SOC_A               | GPIO0_37 |           |
| 0x0011C098 | CTRLMMR_PADCONFIG38 | AH16        | PRG2_PRU0_GPO<br>8    | PRG2_PRU0_GPI<br>8  | PRG2_RGMII1_TD<br>0    | GPMC0_A17    | TRC_DATA6  | EHRPWM2_A          | PRG2_PWM0_B0               | GPIO0_38 |           |
| 0x0011C09C | CTRLMMR_PADCONFIG39 | AG16        | PRG2_PRU0_GPO<br>9    | PRG2_PRU0_GPI<br>9  | PRG2_RGMII1_TD<br>1    | GPMC0_A16    | TRC_DATA7  | EHRPWM2_B          |                            | GPIO0_39 |           |
| 0x0011C0A0 | CTRLMMR_PADCONFIG40 | AF16        | PRG2_PRU0_GPO<br>10   | PRG2_PRU0_GPI<br>10 | PRG2_RGMII1_TD<br>2    | GPMC0_A15    | TRC_DATA8  | EHRPWM_TZn_IN<br>2 | EHRPWM_SOC_B               | GPIO0_40 |           |
| 0x0011C0A4 | CTRLMMR_PADCONFIG41 | AE16        | PRG2_PRU0_GPO<br>11   | PRG2_PRU0_GPI<br>11 | PRG2_RGMII1_TD<br>3    | GPMC0_A14    | TRC_DATA9  |                    | PRG2_ECAPH_IN_<br>APWM_OUT | GPIO0_41 |           |
| 0x0011C0A8 | CTRLMMR_PADCONFIG42 | AD16        | PRG2_PRU0_GPO<br>16   | PRG2_PRU0_GPI<br>16 | PRG2_RGMII1_TX<br>C    | GPMC0_A13    | TRC_DATA10 |                    | PRG2_PWM0_A1               | GPIO0_42 |           |
| 0x0011C0AC | CTRLMMR_PADCONFIG43 | AH15        | PRG2_PRU1_GPO<br>0    | PRG2_PRU1_GPI<br>0  | PRG2_RGMII2_RD<br>0    | GPMC0_A12    | TRC_DATA11 | EHRPWM3_A          | PRG2_PWM3_A2               | GPIO0_43 |           |
| 0x0011C0B0 | CTRLMMR_PADCONFIG44 | AC16        | PRG2_PRU1_GPO<br>1    | PRG2_PRU1_GPI<br>1  | PRG2_RGMII2_RD<br>1    | GPMC0_A11    | TRC_DATA12 | EHRPWM3_B          | PRG2_PWM3_B2               | GPIO0_44 |           |
| 0x0011C0B4 | CTRLMMR_PADCONFIG45 | AD17        | PRG2_PRU1_GPO<br>2    | PRG2_PRU1_GPI<br>2  | PRG2_RGMII2_RD<br>2    | GPMC0_A10    | TRC_DATA13 | EHRPWM3_SYNCI      | PRG2_PWM0_B1               | GPIO0_45 |           |
| 0x0011C0B8 | CTRLMMR_PADCONFIG46 | AH14        | PRG2_PRU1_GPO<br>3    | PRG2_PRU1_GPI<br>3  | PRG2_RGMII2_RD<br>3    | GPMC0_A9     | TRC_DATA14 | EHRPWM3_SYNC<br>O  |                            | GPIO0_46 |           |
| 0x0011C0BC | CTRLMMR_PADCONFIG47 | AG14        | PRG2_PRU1_GPO<br>4    | PRG2_PRU1_GPI<br>4  | PRG2_RGMII2_RX<br>_CTL | GPMC0_A8     | TRC_DATA15 | EHRPWM_TZn_IN<br>3 | PRG2_ECAPH_SY<br>NC_OUT    | GPIO0_47 |           |
| 0x0011C0C0 | CTRLMMR_PADCONFIG48 | AG15        | PRG2_PRU1_GPO<br>5    | PRG2_PRU1_GPI<br>5  | PRG2_RGMII2_RX<br>C    | GPMC0_A7     | TRC_DATA16 | EHRPWM4_A          |                            | GPIO0_48 |           |
| 0x0011C0C4 | CTRLMMR_PADCONFIG49 | AC17        | PRG2_PRU1_GPO<br>6    | PRG2_PRU1_GPI<br>6  | PRG2_RGMII2_TX<br>_CTL | GPMC0_A6     | TRC_DATA17 | EHRPWM4_B          |                            | GPIO0_49 |           |
| 0x0011C0C8 | CTRLMMR_PADCONFIG50 | AE15        | PRG2_PRU1_GPO<br>7    | PRG2_PRU1_GPI<br>7  | PRG2_MDIO0_MD<br>C     | GPMC0_A5     | TRC_DATA18 | EHRPWM_TZn_IN<br>4 | PRG2_PWM3_TZ_<br>IN        | GPIO0_50 |           |
| 0x0011C0CC | CTRLMMR_PADCONFIG51 | AD15        | PRG2_PRU1_GPO<br>8    | PRG2_PRU1_GPI<br>8  | PRG2_RGMII2_TD<br>0    | GPMC0_A4     | TRC_DATA19 | EHRPWM5_A          | PRG2_PWM0_A2               | GPIO0_51 |           |
| 0x0011C0D0 | CTRLMMR_PADCONFIG52 | AF14        | PRG2_PRU1_GPO<br>9    | PRG2_PRU1_GPI<br>9  | PRG2_RGMII2_TD<br>1    | GPMC0_A3     | TRC_DATA20 | EHRPWM5_B          | PRG2_PWM3_TZ_<br>OUT       | GPIO0_52 |           |
| 0x0011C0D4 | CTRLMMR_PADCONFIG53 | AC15        | PRG2_PRU1_GPO<br>10   | PRG2_PRU1_GPI<br>10 | PRG2_RGMII2_TD<br>2    | GPMC0_A2     | TRC_DATA21 | EHRPWM_TZn_IN<br>5 | PRG2_PWM0_B2               | GPIO0_53 |           |
| 0x0011C0D8 | CTRLMMR_PADCONFIG54 | AD14        | PRG2_PRU1_GPO<br>11   | PRG2_PRU1_GPI<br>11 | PRG2_RGMII2_TD<br>3    | GPMC0_A1     | TRC_DATA22 |                    | PRG2_ECAPH_SY<br>NC_IN     | GPIO0_54 |           |
| 0x0011C0DC | CTRLMMR_PADCONFIG55 | AE14        | PRG2_PRU1_GPO<br>16   | PRG2_PRU1_GPI<br>16 | PRG2_RGMII2_TX<br>C    | GPMC0_A0     | TRC_DATA23 |                    | PRG2_PWM1_TZ_<br>OUT       | GPIO0_55 |           |
| 0x0011C0E0 | CTRLMMR_PADCONFIG56 | AE22        | PRG1_PRU0_GPO<br>0    | PRG1_PRU0_GPI<br>0  | PRG1_RGMII1_RD<br>0    | PRG1_PWM3_A0 |            |                    |                            | GPIO0_56 |           |

**Table 5-76. Pin Multiplexing (continued)**

| ADDRESS    | REGISTER NAME       | BALL NUMBER | MUXMODE[7:0] SETTINGS |                  |                         |                  |          |                  |                              |          |           |
|------------|---------------------|-------------|-----------------------|------------------|-------------------------|------------------|----------|------------------|------------------------------|----------|-----------|
|            |                     |             | 0                     | 1                | 2                       | 3                | 4        | 5                | 6                            | 7        | Bootstrap |
| 0x0011C0E4 | CTRLMMR_PADCONFIG57 | AG24        | PRG1_PRU0_GPO_1       | PRG1_PRU0_GPI_1  | PRG1_RGMII1_RD_1        | PRG1_PWM3_B0     |          |                  |                              | GPIO0_57 |           |
| 0x0011C0E8 | CTRLMMR_PADCONFIG58 | AF23        | PRG1_PRU0_GPO_2       | PRG1_PRU0_GPI_2  | PRG1_RGMII1_RD_2        | PRG1_PWM2_A0     |          |                  |                              | GPIO0_58 |           |
| 0x0011C0EC | CTRLMMR_PADCONFIG59 | AD21        | PRG1_PRU0_GPO_3       | PRG1_PRU0_GPI_3  | PRG1_RGMII1_RD_3        | PRG1_PWM3_A2     |          |                  |                              | GPIO0_59 |           |
| 0x0011C0F0 | CTRLMMR_PADCONFIG60 | AG23        | PRG1_PRU0_GPO_4       | PRG1_PRU0_GPI_4  | PRG1_RGMII1_RX_CTL      | PRG1_PWM2_B0     |          |                  |                              | GPIO0_60 |           |
| 0x0011C0F4 | CTRLMMR_PADCONFIG61 | AF27        | PRG1_PRU0_GPO_5       | PRG1_PRU0_GPI_5  |                         | PRG1_PWM3_B2     |          |                  |                              | GPIO0_61 |           |
| 0x0011C0F8 | CTRLMMR_PADCONFIG62 | AF22        | PRG1_PRU0_GPO_6       | PRG1_PRU0_GPI_6  | PRG1_RGMII1_RX_C        | PRG1_PWM3_A1     |          |                  |                              | GPIO0_62 |           |
| 0x0011C0FC | CTRLMMR_PADCONFIG63 | AG27        | PRG1_PRU0_GPO_7       | PRG1_PRU0_GPI_7  | PRG1_IEP0_EDC_LATCH_IN1 | PRG1_PWM3_B1     |          |                  |                              | GPIO0_63 |           |
| 0x0011C100 | CTRLMMR_PADCONFIG64 | AF28        | PRG1_PRU0_GPO_8       | PRG1_PRU0_GPI_8  |                         | PRG1_PWM2_A1     |          |                  |                              | GPIO0_64 |           |
| 0x0011C104 | CTRLMMR_PADCONFIG65 | AF26        | PRG1_PRU0_GPO_9       | PRG1_PRU0_GPI_9  | PRG1_UART0_CT_Sn        | PRG1_PWM3_TZ_IN  | SPI2_CS1 |                  | PRG1_IEP0_EDIO_DATA_IN_OUT28 | GPIO0_65 |           |
| 0x0011C108 | CTRLMMR_PADCONFIG66 | AH25        | PRG1_PRU0_GPO_10      | PRG1_PRU0_GPI_10 | PRG1_UART0_RT_Sn        | PRG1_PWM2_B1     | SPI2_CS2 |                  | PRG1_IEP0_EDIO_DATA_IN_OUT29 | GPIO0_66 |           |
| 0x0011C10C | CTRLMMR_PADCONFIG67 | AF21        | PRG1_PRU0_GPO_11      | PRG1_PRU0_GPI_11 | PRG1_RGMII1_TX_CTL      | PRG1_PWM3_TZ_OUT |          | PRG1_PRU0_GPO_15 |                              | GPIO0_67 |           |
| 0x0011C110 | CTRLMMR_PADCONFIG68 | AH20        | PRG1_PRU0_GPO_12      | PRG1_PRU0_GPI_12 | PRG1_RGMII1_TD_0        | PRG1_PWM0_A0     |          | PRG1_PRU0_GPO_11 |                              | GPIO0_68 |           |
| 0x0011C114 | CTRLMMR_PADCONFIG69 | AH21        | PRG1_PRU0_GPO_13      | PRG1_PRU0_GPI_13 | PRG1_RGMII1_TD_1        | PRG1_PWM0_B0     |          | PRG1_PRU0_GPO_12 |                              | GPIO0_69 |           |
| 0x0011C118 | CTRLMMR_PADCONFIG70 | AG20        | PRG1_PRU0_GPO_14      | PRG1_PRU0_GPI_14 | PRG1_RGMII1_TD_2        | PRG1_PWM0_A1     |          | PRG1_PRU0_GPO_13 |                              | GPIO0_70 |           |
| 0x0011C11C | CTRLMMR_PADCONFIG71 | AD19        | PRG1_PRU0_GPO_15      | PRG1_PRU0_GPI_15 | PRG1_RGMII1_TD_3        | PRG1_PWM0_B1     |          | PRG1_PRU0_GPO_14 |                              | GPIO0_71 |           |
| 0x0011C120 | CTRLMMR_PADCONFIG72 | AD20        | PRG1_PRU0_GPO_16      | PRG1_PRU0_GPI_16 | PRG1_RGMII1_TX_C        | PRG1_PWM0_A2     |          |                  |                              | GPIO0_72 |           |
| 0x0011C124 | CTRLMMR_PADCONFIG73 | AH26        | PRG1_PRU0_GPO_17      | PRG1_PRU0_GPI_17 | PRG1_IEP0_EDC_SYNC_OUT1 | PRG1_PWM0_B2     |          |                  |                              | GPIO0_73 |           |
| 0x0011C128 | CTRLMMR_PADCONFIG74 | AG25        | PRG1_PRU0_GPO_18      | PRG1_PRU0_GPI_18 | PRG1_IEP0_EDC_LATCH_IN0 | PRG1_PWM0_TZ_IN  |          |                  |                              | GPIO0_74 |           |
| 0x0011C12C | CTRLMMR_PADCONFIG75 | AG26        | PRG1_PRU0_GPO_19      | PRG1_PRU0_GPI_19 | PRG1_IEP0_EDC_SYNC_OUT0 | PRG1_PWM0_TZ_OUT |          |                  |                              | GPIO0_75 |           |
| 0x0011C130 | CTRLMMR_PADCONFIG76 | AH24        | PRG1_PRU1_GPO_0       | PRG1_PRU1_GPI_0  | PRG1_RGMII2_RD_0        |                  |          |                  |                              | GPIO0_76 |           |
| 0x0011C134 | CTRLMMR_PADCONFIG77 | AH23        | PRG1_PRU1_GPO_1       | PRG1_PRU1_GPI_1  | PRG1_RGMII2_RD_1        |                  |          |                  |                              | GPIO0_77 |           |
| 0x0011C138 | CTRLMMR_PADCONFIG78 | AG21        | PRG1_PRU1_GPO_2       | PRG1_PRU1_GPI_2  | PRG1_RGMII2_RD_2        | PRG1_PWM2_A2     |          |                  |                              | GPIO0_78 |           |
| 0x0011C13C | CTRLMMR_PADCONFIG79 | AH22        | PRG1_PRU1_GPO_3       | PRG1_PRU1_GPI_3  | PRG1_RGMII2_RD_3        |                  | EQEP1_A  |                  |                              | GPIO0_79 |           |
| 0x0011C140 | CTRLMMR_PADCONFIG80 | AE21        | PRG1_PRU1_GPO_4       | PRG1_PRU1_GPI_4  | PRG1_RGMII2_RX_CTL      | PRG1_PWM2_B2     | EQEP1_B  |                  |                              | GPIO0_80 |           |

Table 5-76. Pin Multiplexing (continued)

| ADDRESS    | REGISTER NAME        | BALL NUMBER | MUXMODE[7:0] SETTINGS |                  |                          |                   |          |                         |                               |          |           |
|------------|----------------------|-------------|-----------------------|------------------|--------------------------|-------------------|----------|-------------------------|-------------------------------|----------|-----------|
|            |                      |             | 0                     | 1                | 2                        | 3                 | 4        | 5                       | 6                             | 7        | Bootstrap |
| 0x0011C144 | CTRLMMR_PADCONFIG81  | AC22        | PRG1_PRU1_GPO 5       | PRG1_PRU1_GPI 5  |                          |                   | EQEP1_S  |                         |                               | GPIO0_81 |           |
| 0x0011C148 | CTRLMMR_PADCONFIG82  | AG22        | PRG1_PRU1_GPO 6       | PRG1_PRU1_GPI 6  | PRG1_RGMII2_RX C         |                   |          |                         |                               | GPIO0_82 |           |
| 0x0011C14C | CTRLMMR_PADCONFIG83  | AD23        | PRG1_PRU1_GPO 7       | PRG1_PRU1_GPI 7  | PRG1_IEP1_EDC_ LATCH_IN1 |                   | SPI2_CS0 |                         | UART1_TXD                     | GPIO0_83 |           |
| 0x0011C150 | CTRLMMR_PADCONFIG84  | AE24        | PRG1_PRU1_GPO 8       | PRG1_PRU1_GPI 8  |                          | PRG1_PWM2_TZ_ OUT |          |                         |                               | GPIO0_84 |           |
| 0x0011C154 | CTRLMMR_PADCONFIG85  | AF25        | PRG1_PRU1_GPO 9       | PRG1_PRU1_GPI 9  | PRG1_UART0_RX D          |                   |          |                         | PRG1_IEP0_EDIO_ DATA_IN_OUT30 | GPIO0_85 |           |
| 0x0011C158 | CTRLMMR_PADCONFIG86  | AF24        | PRG1_PRU1_GPO 10      | PRG1_PRU1_GPI 10 | PRG1_UART0_TX D          | PRG1_PWM2_TZ_ IN  | SPI2_CS3 |                         | PRG1_IEP0_EDIO_ DATA_IN_OUT31 | GPIO0_86 |           |
| 0x0011C15C | CTRLMMR_PADCONFIG87  | AC20        | PRG1_PRU1_GPO 11      | PRG1_PRU1_GPI 11 | PRG1_RGMII2_TX_ CTL      |                   | EQEP1_I  | PRG1_PRU1_GPO 15        |                               | GPIO0_87 |           |
| 0x0011C160 | CTRLMMR_PADCONFIG88  | AE20        | PRG1_PRU1_GPO 12      | PRG1_PRU1_GPI 12 | PRG1_RGMII2_TD 0         | PRG1_PWM1_A0      |          | PRG1_PRU1_GPO 11        |                               | GPIO0_88 |           |
| 0x0011C164 | CTRLMMR_PADCONFIG89  | AF19        | PRG1_PRU1_GPO 13      | PRG1_PRU1_GPI 13 | PRG1_RGMII2_TD 1         | PRG1_PWM1_B0      |          | PRG1_PRU1_GPO 12        |                               | GPIO0_89 |           |
| 0x0011C168 | CTRLMMR_PADCONFIG90  | AH19        | PRG1_PRU1_GPO 14      | PRG1_PRU1_GPI 14 | PRG1_RGMII2_TD 2         | PRG1_PWM1_A1      |          | PRG1_PRU1_GPO 13        |                               | GPIO0_90 |           |
| 0x0011C16C | CTRLMMR_PADCONFIG91  | AG19        | PRG1_PRU1_GPO 15      | PRG1_PRU1_GPI 15 | PRG1_RGMII2_TD 3         | PRG1_PWM1_B1      |          | PRG1_PRU1_GPO 14        |                               | GPIO0_91 |           |
| 0x0011C170 | CTRLMMR_PADCONFIG92  | AE19        | PRG1_PRU1_GPO 16      | PRG1_PRU1_GPI 16 | PRG1_RGMII2_TX C         | PRG1_PWM1_A2      |          |                         |                               | GPIO0_92 |           |
| 0x0011C174 | CTRLMMR_PADCONFIG93  | AE23        | PRG1_PRU1_GPO 17      | PRG1_PRU1_GPI 17 | PRG1_IEP1_EDC_ SYNC_OUT1 | PRG1_PWM1_B2      | SPI2_CLK | PRG1_ECAP0_SY NC_OUT    | UART1_RXD                     | GPIO0_93 |           |
| 0x0011C178 | CTRLMMR_PADCONFIG94  | AD22        | PRG1_PRU1_GPO 18      | PRG1_PRU1_GPI 18 | PRG1_IEP1_EDC_ LATCH_IN0 | PRG1_PWM1_TZ_ IN  | SPI2_D0  | PRG1_ECAP0_SY NC_IN     | UART1_CTSn                    | GPIO0_94 |           |
| 0x0011C17C | CTRLMMR_PADCONFIG95  | AC21        | PRG1_PRU1_GPO 19      | PRG1_PRU1_GPI 19 | PRG1_IEP1_EDC_ SYNC_OUT0 | PRG1_PWM1_TZ_ OUT | SPI2_D1  | PRG1_ECAP0_IN_ APWM_OUT | UART1_RTSn                    | GPIO0_95 |           |
| 0x0011C180 | CTRLMMR_PADCONFIG96  | AD18        | PRG1_MDIO0_MD IO      | SPI1_CS2         |                          | PRG2_PWM1_A1      |          |                         |                               | GPIO1_0  |           |
| 0x0011C184 | CTRLMMR_PADCONFIG97  | AH18        | PRG1_MDIO0_MD C       | SPI1_CS3         |                          | PRG2_PWM1_B1      |          |                         |                               | GPIO1_1  |           |
| 0x0011C188 | CTRLMMR_PADCONFIG98  | D25         | MMC0_DAT7             | UART0_DCDn       |                          |                   |          | EQEP2_A                 |                               | GPIO1_2  |           |
| 0x0011C18C | CTRLMMR_PADCONFIG99  | B26         | MMC0_DAT6             | UART0_DSRn       |                          |                   |          | EQEP2_B                 |                               | GPIO1_3  |           |
| 0x0011C190 | CTRLMMR_PADCONFIG100 | A24         | MMC0_DAT5             | UART0_DTRn       |                          |                   |          | EQEP2_I                 |                               | GPIO1_4  |           |
| 0x0011C194 | CTRLMMR_PADCONFIG101 | E24         | MMC0_DAT4             | UART0_RIN        |                          |                   |          | EQEP2_S                 |                               | GPIO1_5  |           |
| 0x0011C198 | CTRLMMR_PADCONFIG102 | A25         | MMC0_DAT3             |                  |                          |                   |          |                         |                               | GPIO1_6  |           |
| 0x0011C19C | CTRLMMR_PADCONFIG103 | C26         | MMC0_DAT2             |                  |                          |                   |          |                         |                               | GPIO1_7  |           |
| 0x0011C1A0 | CTRLMMR_PADCONFIG104 | E25         | MMC0_DAT1             |                  |                          |                   |          |                         |                               | GPIO1_8  |           |
| 0x0011C1A4 | CTRLMMR_PADCONFIG105 | A26         | MMC0_DAT0             |                  |                          |                   |          |                         |                               | GPIO1_9  |           |
| 0x0011C1A8 | CTRLMMR_PADCONFIG106 | B25         | MMC0_CLK              |                  |                          |                   |          |                         |                               | GPIO1_10 |           |
| 0x0011C1AC | CTRLMMR_PADCONFIG107 | B27         | MMC0_CMD              |                  |                          |                   |          |                         |                               | GPIO1_11 |           |
| 0x0011C1B0 | CTRLMMR_PADCONFIG108 | C25         | MMC0_DS               |                  |                          |                   |          |                         |                               | GPIO1_12 |           |



**Table 5-76. Pin Multiplexing (continued)**

| ADDRESS     | REGISTER NAME        | BALL NUMBER          | MUXMODE[7:0] SETTINGS |                  |                         |                         |                    |              |                              |          |           |
|-------------|----------------------|----------------------|-----------------------|------------------|-------------------------|-------------------------|--------------------|--------------|------------------------------|----------|-----------|
|             |                      |                      | 0                     | 1                | 2                       | 3                       | 4                  | 5            | 6                            | 7        | Bootstrap |
| 0x0011C1B4  | CTRLMMR_PADCONFIG109 | <a href="#">A23</a>  | MMC0_SDCD             |                  |                         |                         |                    |              | PRG2_IEP0_EDIO_OUTVALID      | GPIO1_13 |           |
| 0x0011C1B8  | CTRLMMR_PADCONFIG110 | <a href="#">B23</a>  | MMC0_SDWP             |                  |                         |                         |                    |              |                              | GPIO1_14 |           |
| 0x0011C1BC  | CTRLMMR_PADCONFIG111 | <a href="#">AG13</a> | SPI0_CS0              |                  |                         |                         |                    |              |                              | GPIO1_15 |           |
| 0x0011C1C0  | CTRLMMR_PADCONFIG112 | <a href="#">AF13</a> | SPI0_CS1              | CPTS0_TS_COMP    | I2C3_SCL                |                         |                    |              | PRG1_IEP0_EDIO_OUTVALID      | GPIO1_16 |           |
| 0x0011C1C4  | CTRLMMR_PADCONFIG113 | <a href="#">AH13</a> | SPI0_CLK              |                  |                         |                         |                    |              |                              | GPIO1_17 |           |
| 0x0011C1C8  | CTRLMMR_PADCONFIG114 | <a href="#">AE13</a> | SPI0_D0               |                  |                         |                         |                    |              |                              | GPIO1_18 |           |
| 0x0011C1C C | CTRLMMR_PADCONFIG115 | <a href="#">AD13</a> | SPI0_D1               |                  |                         |                         |                    |              |                              | GPIO1_19 |           |
| 0x0011C1D0  | CTRLMMR_PADCONFIG116 | <a href="#">AD12</a> | SPI1_CS0              |                  |                         | PRG2_IEP0_EDC_LATCH_IN0 | PRG2_UART0_CT_Sn   |              | PRG0_IEP0_EDIO_OUTVALID      | GPIO1_20 |           |
| 0x0011C1D4  | CTRLMMR_PADCONFIG117 | <a href="#">AG12</a> | SPI1_CS1              | CPTS0_TS_SYNC    | I2C3_SDA                |                         |                    |              |                              | GPIO1_21 |           |
| 0x0011C1D8  | CTRLMMR_PADCONFIG118 | <a href="#">AH12</a> | SPI1_CLK              |                  |                         | PRG2_IEP0_EDC_SYNC_OUT0 | PRG2_UART0_RT_Sn   |              |                              | GPIO1_22 |           |
| 0x0011C1D C | CTRLMMR_PADCONFIG119 | <a href="#">AE12</a> | SPI1_D0               |                  |                         | PRG2_IEP0_EDC_LATCH_IN1 | PRG2_UART0_RX_D    |              |                              | GPIO1_23 |           |
| 0x0011C1E0  | CTRLMMR_PADCONFIG120 | <a href="#">AF12</a> | SPI1_D1               |                  |                         | PRG2_IEP0_EDC_SYNC_OUT1 | PRG2_UART0_TX_D    |              |                              | GPIO1_24 |           |
| 0x0011C1E4  | CTRLMMR_PADCONFIG121 | <a href="#">AF11</a> | UART0_RXD             |                  |                         |                         |                    |              |                              | GPIO1_25 |           |
| 0x0011C1E8  | CTRLMMR_PADCONFIG122 | <a href="#">AE11</a> | UART0_TXD             |                  |                         |                         |                    |              |                              | GPIO1_26 |           |
| 0x0011C1EC  | CTRLMMR_PADCONFIG123 | <a href="#">AG11</a> | UART0_CTSn            | TIMER_IO4        | SPI0_CS2                |                         |                    |              |                              | GPIO1_27 |           |
| 0x0011C1F0  | CTRLMMR_PADCONFIG124 | <a href="#">AD11</a> | UART0_RTSn            | TIMER_IO5        | SPI0_CS3                |                         |                    |              |                              | GPIO1_28 |           |
| 0x0011C1F4  | CTRLMMR_PADCONFIG125 | <a href="#">V24</a>  | PRG0_PRU0_GPO_0       | PRG0_PRU0_GPI_0  | PRG0_RGMII1_RD_0        | PRG0_PWM3_A0            |                    | MCASP0_ACLKX |                              | GPIO1_29 |           |
| 0x0011C1F8  | CTRLMMR_PADCONFIG126 | <a href="#">W25</a>  | PRG0_PRU0_GPO_1       | PRG0_PRU0_GPI_1  | PRG0_RGMII1_RD_1        | PRG0_PWM3_B0            |                    | MCASP0_AFSX  |                              | GPIO1_30 |           |
| 0x0011C1FC  | CTRLMMR_PADCONFIG127 | <a href="#">W24</a>  | PRG0_PRU0_GPO_2       | PRG0_PRU0_GPI_2  | PRG0_RGMII1_RD_2        | PRG0_PWM2_A0            |                    | MCASP0_ACLKR |                              | GPIO1_31 |           |
| 0x0011C200  | CTRLMMR_PADCONFIG128 | <a href="#">AA27</a> | PRG0_PRU0_GPO_3       | PRG0_PRU0_GPI_3  | PRG0_RGMII1_RD_3        | PRG0_PWM3_A2            |                    | MCASP0_AFSR  |                              | GPIO1_32 |           |
| 0x0011C204  | CTRLMMR_PADCONFIG129 | <a href="#">Y24</a>  | PRG0_PRU0_GPO_4       | PRG0_PRU0_GPI_4  | PRG0_RGMII1_RX_CTL      | PRG0_PWM2_B0            |                    | MCASP0_AXR0  |                              | GPIO1_33 |           |
| 0x0011C208  | CTRLMMR_PADCONFIG130 | <a href="#">V28</a>  | PRG0_PRU0_GPO_5       | PRG0_PRU0_GPI_5  |                         | PRG0_PWM3_B2            |                    | MCASP0_AXR1  |                              | GPIO1_34 |           |
| 0x0011C20C  | CTRLMMR_PADCONFIG131 | <a href="#">Y25</a>  | PRG0_PRU0_GPO_6       | PRG0_PRU0_GPI_6  | PRG0_RGMII1_RX_C        | PRG0_PWM3_A1            |                    | MCASP0_AXR2  |                              | GPIO1_35 |           |
| 0x0011C210  | CTRLMMR_PADCONFIG132 | <a href="#">U27</a>  | PRG0_PRU0_GPO_7       | PRG0_PRU0_GPI_7  | PRG0_IEP0_EDC_LATCH_IN1 | PRG0_PWM3_B1            | PRG0_ECAP0_SYNC_IN | MCASP0_AXR3  |                              | GPIO1_36 |           |
| 0x0011C214  | CTRLMMR_PADCONFIG133 | <a href="#">V27</a>  | PRG0_PRU0_GPO_8       | PRG0_PRU0_GPI_8  |                         | PRG0_PWM2_A1            |                    | MCASP0_AXR4  |                              | GPIO1_37 |           |
| 0x0011C218  | CTRLMMR_PADCONFIG134 | <a href="#">V26</a>  | PRG0_PRU0_GPO_9       | PRG0_PRU0_GPI_9  | PRG0_UART0_CT_Sn        | PRG0_PWM3_TZ_IN         | SPI3_CS1           | MCASP0_AXR5  | PRG0_IEP0_EDIO_DATA_IN_OUT28 | GPIO1_38 |           |
| 0x0011C21C  | CTRLMMR_PADCONFIG135 | <a href="#">U25</a>  | PRG0_PRU0_GPO_10      | PRG0_PRU0_GPI_10 | PRG0_UART0_RT_Sn        | PRG0_PWM2_B1            | SPI3_CS2           | MCASP0_AXR6  | PRG0_IEP0_EDIO_DATA_IN_OUT29 | GPIO1_39 |           |

Table 5-76. Pin Multiplexing (continued)

| ADDRESS    | REGISTER NAME        | BALL NUMBER | MUXMODE[7:0] SETTINGS |                  |                         |                  |                        |              |                              |          |           |
|------------|----------------------|-------------|-----------------------|------------------|-------------------------|------------------|------------------------|--------------|------------------------------|----------|-----------|
|            |                      |             | 0                     | 1                | 2                       | 3                | 4                      | 5            | 6                            | 7        | Bootstrap |
| 0x0011C220 | CTRLMMR_PADCONFIG136 | AB25        | PRG0_PRU0_GPO_11      | PRG0_PRU0_GPI_11 | PRG0_RGMII1_TX_CTL      | PRG0_PWM3_TZ_OUT | PRG0_PRU0_GPO_15       | MCASP0_AXR7  |                              | GPIO1_40 |           |
| 0x0011C224 | CTRLMMR_PADCONFIG137 | AD27        | PRG0_PRU0_GPO_12      | PRG0_PRU0_GPI_12 | PRG0_RGMII1_TD_0        | PRG0_PWM0_A0     | PRG0_PRU0_GPO_11       | MCASP0_AXR8  |                              | GPIO1_41 |           |
| 0x0011C228 | CTRLMMR_PADCONFIG138 | AC26        | PRG0_PRU0_GPO_13      | PRG0_PRU0_GPI_13 | PRG0_RGMII1_TD_1        | PRG0_PWM0_B0     | PRG0_PRU0_GPO_12       | MCASP0_AXR9  |                              | GPIO1_42 |           |
| 0x0011C22C | CTRLMMR_PADCONFIG139 | AD26        | PRG0_PRU0_GPO_14      | PRG0_PRU0_GPI_14 | PRG0_RGMII1_TD_2        | PRG0_PWM0_A1     | PRG0_PRU0_GPO_13       | MCASP0_AXR10 |                              | GPIO1_43 |           |
| 0x0011C230 | CTRLMMR_PADCONFIG140 | AA24        | PRG0_PRU0_GPO_15      | PRG0_PRU0_GPI_15 | PRG0_RGMII1_TD_3        | PRG0_PWM0_B1     | PRG0_PRU0_GPO_14       | MCASP0_AXR11 |                              | GPIO1_44 |           |
| 0x0011C234 | CTRLMMR_PADCONFIG141 | AD28        | PRG0_PRU0_GPO_16      | PRG0_PRU0_GPI_16 | PRG0_RGMII1_TX_C        | PRG0_PWM0_A2     |                        | MCASP0_AXR12 | MCASP1_AHCLKR                | GPIO1_45 |           |
| 0x0011C238 | CTRLMMR_PADCONFIG142 | U26         | PRG0_PRU0_GPO_17      | PRG0_PRU0_GPI_17 | PRG0_IEP0_EDC_SYNC_OUT1 | PRG0_PWM0_B2     | PRG0_ECAP0_SYNC_OUT    | MCASP0_AXR13 | MCASP1_AHCLKX                | GPIO1_46 |           |
| 0x0011C23C | CTRLMMR_PADCONFIG143 | V25         | PRG0_PRU0_GPO_18      | PRG0_PRU0_GPI_18 | PRG0_IEP0_EDC_LATCH_IN0 | PRG0_PWM0_TZ_IN  | PRG0_ECAP0_IN_APWM_OUT | MCASP0_AXR14 | MCASP2_AHCLKR                | GPIO1_47 |           |
| 0x0011C240 | CTRLMMR_PADCONFIG144 | U24         | PRG0_PRU0_GPO_19      | PRG0_PRU0_GPI_19 | PRG0_IEP0_EDC_SYNC_OUT0 | PRG0_PWM0_TZ_OUT |                        | MCASP0_AXR15 | MCASP2_AHCLKX                | GPIO1_48 |           |
| 0x0011C244 | CTRLMMR_PADCONFIG145 | AB28        | PRG0_PRU1_GPO_0       | PRG0_PRU1_GPI_0  | PRG0_RGMII2_RD_0        |                  |                        | MCASP1_ACLKX |                              | GPIO1_49 |           |
| 0x0011C248 | CTRLMMR_PADCONFIG146 | AC28        | PRG0_PRU1_GPO_1       | PRG0_PRU1_GPI_1  | PRG0_RGMII2_RD_1        |                  |                        | MCASP1_AFSX  |                              | GPIO1_50 |           |
| 0x0011C24C | CTRLMMR_PADCONFIG147 | AC27        | PRG0_PRU1_GPO_2       | PRG0_PRU1_GPI_2  | PRG0_RGMII2_RD_2        | PRG0_PWM2_A2     |                        | MCASP1_ACLKR |                              | GPIO1_51 |           |
| 0x0011C250 | CTRLMMR_PADCONFIG148 | AB26        | PRG0_PRU1_GPO_3       | PRG0_PRU1_GPI_3  | PRG0_RGMII2_RD_3        |                  | EQEP0_A                | MCASP1_AFSR  |                              | GPIO1_52 |           |
| 0x0011C254 | CTRLMMR_PADCONFIG149 | AA25        | PRG0_PRU1_GPO_4       | PRG0_PRU1_GPI_4  | PRG0_RGMII2_RX_CTL      | PRG0_PWM2_B2     | EQEP0_B                | MCASP1_AXR0  | MCASP0_AHCLKR                | GPIO1_53 |           |
| 0x0011C258 | CTRLMMR_PADCONFIG150 | U23         | PRG0_PRU1_GPO_5       | PRG0_PRU1_GPI_5  |                         |                  | EQEP0_S                | MCASP1_AXR1  | MCASP0_AHCLKX                | GPIO1_54 |           |
| 0x0011C25C | CTRLMMR_PADCONFIG151 | AB27        | PRG0_PRU1_GPO_6       | PRG0_PRU1_GPI_6  | PRG0_RGMII2_RX_C        |                  |                        | MCASP1_AXR2  |                              | GPIO1_55 |           |
| 0x0011C260 | CTRLMMR_PADCONFIG152 | W28         | PRG0_PRU1_GPO_7       | PRG0_PRU1_GPI_7  | PRG0_IEP1_EDC_LATCH_IN1 |                  | SPI3_CS0               | MCASP1_AXR3  | UART2_TXD                    | GPIO1_56 |           |
| 0x0011C264 | CTRLMMR_PADCONFIG153 | W27         | PRG0_PRU1_GPO_8       | PRG0_PRU1_GPI_8  |                         | PRG0_PWM2_TZ_OUT |                        | MCASP1_AXR4  |                              | GPIO1_57 |           |
| 0x0011C268 | CTRLMMR_PADCONFIG154 | Y28         | PRG0_PRU1_GPO_9       | PRG0_PRU1_GPI_9  | PRG0_UART0_RX_D         |                  | SPI3_CS3               | MCASP1_AXR5  | PRG0_IEP0_EDIO_DATA_IN_OUT30 | GPIO1_58 |           |
| 0x0011C26C | CTRLMMR_PADCONFIG155 | AA28        | PRG0_PRU1_GPO_10      | PRG0_PRU1_GPI_10 | PRG0_UART0_TX_D         | PRG0_PWM2_TZ_IN  | EQEP0_I                | MCASP1_AXR6  | PRG0_IEP0_EDIO_DATA_IN_OUT31 | GPIO1_59 |           |
| 0x0011C270 | CTRLMMR_PADCONFIG156 | AB24        | PRG0_PRU1_GPO_11      | PRG0_PRU1_GPI_11 | PRG0_RGMII2_TX_CTL      |                  | PRG0_PRU1_GPO_15       | MCASP1_AXR7  |                              | GPIO1_60 |           |
| 0x0011C274 | CTRLMMR_PADCONFIG157 | AC25        | PRG0_PRU1_GPO_12      | PRG0_PRU1_GPI_12 | PRG0_RGMII2_TD_0        | PRG0_PWM1_A0     | PRG0_PRU1_GPO_11       | MCASP1_AXR8  |                              | GPIO1_61 |           |
| 0x0011C278 | CTRLMMR_PADCONFIG158 | AD25        | PRG0_PRU1_GPO_13      | PRG0_PRU1_GPI_13 | PRG0_RGMII2_TD_1        | PRG0_PWM1_B0     | PRG0_PRU1_GPO_12       | MCASP1_AXR9  |                              | GPIO1_62 |           |
| 0x0011C27C | CTRLMMR_PADCONFIG159 | AD24        | PRG0_PRU1_GPO_14      | PRG0_PRU1_GPI_14 | PRG0_RGMII2_TD_2        | PRG0_PWM1_A1     | PRG0_PRU1_GPO_13       | MCASP2_AFSR  |                              | GPIO1_63 |           |

**Table 5-76. Pin Multiplexing (continued)**

| ADDRESS    | REGISTER NAME        | BALL NUMBER | MUXMODE[7:0] SETTINGS |                  |                         |                  |                 |              |                 |          |  | Bootstrap |
|------------|----------------------|-------------|-----------------------|------------------|-------------------------|------------------|-----------------|--------------|-----------------|----------|--|-----------|
|            |                      |             | 0                     | 1                | 2                       | 3                | 4               | 5            | 6               | 7        |  |           |
| 0x0011C280 | CTRLMMR_PADCONFIG160 | AE27        | PRG0_PRU1_GPO15       | PRG0_PRU1_GPI15  | PRG0_RGMII2_TD3         | PRG0_PWM1_B1     | PRG0_PRU1_GPO14 | MCASP2_ACLKR |                 | GPIO1_64 |  |           |
| 0x0011C284 | CTRLMMR_PADCONFIG161 | AC24        | PRG0_PRU1_GPO16       | PRG0_PRU1_GPI16  | PRG0_RGMII2_TXC         | PRG0_PWM1_A2     |                 | MCASP2_AXR0  |                 | GPIO1_65 |  |           |
| 0x0011C288 | CTRLMMR_PADCONFIG162 | Y27         | PRG0_PRU1_GPO17       | PRG0_PRU1_GPI17  | PRG0_IEP1_EDC_SYNC_OUT1 | PRG0_PWM1_B2     | SPI3_CLK        | MCASP2_AXR1  | UART2_RXD       | GPIO1_66 |  |           |
| 0x0011C28C | CTRLMMR_PADCONFIG163 | Y26         | PRG0_PRU1_GPO18       | PRG0_PRU1_GPI18  | PRG0_IEP1_EDC_LATCH_IN0 | PRG0_PWM1_TZ_IN  | SPI3_D0         | MCASP2_AFSX  | UART2_CTSn      | GPIO1_67 |  |           |
| 0x0011C290 | CTRLMMR_PADCONFIG164 | W26         | PRG0_PRU1_GPO19       | PRG0_PRU1_GPI19  | PRG0_IEP1_EDC_SYNC_OUT0 | PRG0_PWM1_TZ_OUT | SPI3_D1         | MCASP2_ACLKX | UART2_RTSn      | GPIO1_68 |  |           |
| 0x0011C294 | CTRLMMR_PADCONFIG165 | AE26        | PRG0_MDIO0_MDIO       |                  |                         | PRG2_PWM1_A2     |                 | MCASP2_AXR2  |                 | GPIO1_69 |  |           |
| 0x0011C298 | CTRLMMR_PADCONFIG166 | AE28        | PRG0_MDIO0_MD_C       |                  |                         | PRG2_PWM1_B2     |                 | MCASP2_AXR3  |                 | GPIO1_70 |  |           |
| 0x0011C29C | CTRLMMR_PADCONFIG167 | F18         | NMIIn                 |                  |                         |                  |                 |              | PRG2_PWM1_TZ_IN |          |  |           |
| 0x0011C2A0 | CTRLMMR_PADCONFIG168 | F17         | RESETz                |                  |                         |                  |                 |              |                 |          |  |           |
| 0x0011C2A4 | CTRLMMR_PADCONFIG169 | D19         | RESETSTATz            |                  |                         |                  |                 |              |                 |          |  |           |
| 0x0011C2A8 | CTRLMMR_PADCONFIG170 | C19         | PORz_OUT              |                  |                         |                  |                 |              |                 |          |  |           |
| 0x0011C2AC | CTRLMMR_PADCONFIG171 | E20         | SOC_SAFETY_ER_RORn    |                  |                         |                  |                 |              |                 |          |  |           |
| 0x0011C2B0 | CTRLMMR_PADCONFIG172 | C20         | TDI                   |                  |                         |                  |                 |              |                 |          |  |           |
| 0x0011C2B4 | CTRLMMR_PADCONFIG173 | A20         | TDO                   |                  |                         |                  |                 |              |                 |          |  |           |
| 0x0011C2B8 | CTRLMMR_PADCONFIG174 | A21         | TMS                   |                  |                         |                  |                 |              |                 |          |  |           |
| 0x0011C2BC | CTRLMMR_PADCONFIG175 | AD9         | USB0_DRVVBUS          |                  |                         |                  |                 |              |                 | GPIO1_71 |  |           |
| 0x0011C2C0 | CTRLMMR_PADCONFIG176 | AC8         | USB1_DRVVBUS          |                  |                         |                  |                 |              |                 | GPIO1_72 |  |           |
| 0x0011C2C4 | CTRLMMR_PADCONFIG177 | D27         | MMC1_DAT3             |                  |                         |                  |                 |              |                 | GPIO1_73 |  |           |
| 0x0011C2C8 | CTRLMMR_PADCONFIG178 | D26         | MMC1_DAT2             |                  |                         |                  |                 |              |                 | GPIO1_74 |  |           |
| 0x0011C2CC | CTRLMMR_PADCONFIG179 | E27         | MMC1_DAT1             |                  |                         |                  |                 |              |                 | GPIO1_75 |  |           |
| 0x0011C2D0 | CTRLMMR_PADCONFIG180 | D28         | MMC1_DAT0             |                  |                         |                  |                 |              |                 | GPIO1_76 |  |           |
| 0x0011C2D4 | CTRLMMR_PADCONFIG181 | C27         | MMC1_CLK              |                  |                         |                  |                 |              |                 | GPIO1_77 |  |           |
| 0x0011C2D8 | CTRLMMR_PADCONFIG182 | C28         | MMC1_CMD              |                  |                         |                  |                 |              |                 | GPIO1_78 |  |           |
| 0x0011C2DC | CTRLMMR_PADCONFIG183 | B24         | MMC1_SDCD             |                  |                         |                  |                 |              |                 | GPIO1_79 |  |           |
| 0x0011C2E0 | CTRLMMR_PADCONFIG184 | C24         | MMC1_SDWP             |                  |                         |                  |                 |              |                 | GPIO1_80 |  |           |
| 0x0011C2E8 | CTRLMMR_PADCONFIG186 | D20         | I2C0_SCL              |                  |                         |                  |                 |              |                 |          |  |           |
| 0x0011C2EC | CTRLMMR_PADCONFIG187 | C21         | I2C0_SDA              |                  |                         |                  |                 |              |                 |          |  |           |
| 0x0011C2F0 | CTRLMMR_PADCONFIG188 | B21         | I2C1_SCL              | CPTS0_HW1TSPU_SH |                         |                  |                 |              |                 |          |  |           |
| 0x0011C2F4 | CTRLMMR_PADCONFIG189 | E21         | I2C1_SDA              | CPTS0_HW2TSPU_SH |                         |                  |                 |              |                 |          |  |           |
| 0x0011C2F8 | CTRLMMR_PADCONFIG190 | D21         | ECAP0_IN_APWM_OUT     | SYNCO_OUT        | CPTS0_RFT_CLK           |                  |                 |              |                 | GPIO1_86 |  |           |

Table 5-76. Pin Multiplexing (continued)

| ADDRESS    | REGISTER NAME             | BALL NUMBER | MUXMODE[7:0] SETTINGS       |                                   |                                   |   |                            |              |   |               |           |
|------------|---------------------------|-------------|-----------------------------|-----------------------------------|-----------------------------------|---|----------------------------|--------------|---|---------------|-----------|
|            |                           |             | 0                           | 1                                 | 2                                 | 3 | 4                          | 5            | 6 | 7             | Bootstrap |
| 0x0011C2FC | CTRLMMR_PADCONFIG191      | A22         | EXT_REFCLK1                 | SYNC1_OUT                         |                                   |   |                            |              |   | GPIO1_87      |           |
| 0x0011C300 | CTRLMMR_PADCONFIG192      | B22         | TIMER_IO0                   |                                   | SYSCLKOUT0                        |   |                            |              |   | GPIO1_88      |           |
| 0x0011C304 | CTRLMMR_PADCONFIG193      | C23         | TIMER_IO1                   |                                   | OBSCLK0                           |   |                            |              |   | GPIO1_89      |           |
| 0x0011C308 | CTRLMMR_PADCONFIG194      | E19         | PORz                        |                                   |                                   |   |                            |              |   |               |           |
| 0x4301C000 | CTRLMMR_WKUP_PADCON FIG0  | V1          | MCU_OSPI0_CLK               | MCU_HYPERBUS 0_CK                 |                                   |   |                            |              |   | WKUP_GPIO0_12 |           |
| 0x4301C004 | CTRLMMR_WKUP_PADCON FIG1  | U1          | MCU_OSPI0_LBC LKO           | MCU_HYPERBUS 0_CK <sub>n</sub>    |                                   |   |                            |              |   | WKUP_GPIO0_13 |           |
| 0x4301C008 | CTRLMMR_WKUP_PADCON FIG2  | U2          | MCU_OSPI0_DQS               | MCU_HYPERBUS 0_RWDS               |                                   |   |                            |              |   | WKUP_GPIO0_14 |           |
| 0x4301C00C | CTRLMMR_WKUP_PADCON FIG3  | U4          | MCU_OSPI0_D0                | MCU_HYPERBUS 0_DQ0                |                                   |   |                            |              |   | WKUP_GPIO0_15 |           |
| 0x4301C010 | CTRLMMR_WKUP_PADCON FIG4  | U5          | MCU_OSPI0_D1                | MCU_HYPERBUS 0_DQ1                |                                   |   |                            |              |   | WKUP_GPIO0_16 |           |
| 0x4301C014 | CTRLMMR_WKUP_PADCON FIG5  | T2          | MCU_OSPI0_D2                | MCU_HYPERBUS 0_DQ2                |                                   |   |                            |              |   | WKUP_GPIO0_17 |           |
| 0x4301C018 | CTRLMMR_WKUP_PADCON FIG6  | T3          | MCU_OSPI0_D3                | MCU_HYPERBUS 0_DQ3                |                                   |   |                            |              |   | WKUP_GPIO0_18 |           |
| 0x4301C01C | CTRLMMR_WKUP_PADCON FIG7  | T4          | MCU_OSPI0_D4                | MCU_HYPERBUS 0_DQ4                |                                   |   |                            |              |   | WKUP_GPIO0_19 |           |
| 0x4301C020 | CTRLMMR_WKUP_PADCON FIG8  | T5          | MCU_OSPI0_D5                | MCU_HYPERBUS 0_DQ5                |                                   |   |                            |              |   | WKUP_GPIO0_20 |           |
| 0x4301C024 | CTRLMMR_WKUP_PADCON FIG9  | R2          | MCU_OSPI0_D6                | MCU_HYPERBUS 0_DQ6                |                                   |   |                            |              |   | WKUP_GPIO0_21 |           |
| 0x4301C028 | CTRLMMR_WKUP_PADCON FIG10 | R3          | MCU_OSPI0_D7                | MCU_HYPERBUS 0_DQ7                |                                   |   |                            |              |   | WKUP_GPIO0_22 |           |
| 0x4301C02C | CTRLMMR_WKUP_PADCON FIG11 | R4          | MCU_OSPI0_CS <sub>n</sub> 0 | MCU_HYPERBUS 0_CS <sub>n</sub> 0  |                                   |   |                            |              |   | WKUP_GPIO0_23 |           |
| 0x4301C030 | CTRLMMR_WKUP_PADCON FIG12 | R5          | MCU_OSPI0_CS <sub>n</sub> 1 | MCU_HYPERBUS 0_RESE <sub>Tn</sub> |                                   |   |                            |              |   | WKUP_GPIO0_24 |           |
| 0x4301C034 | CTRLMMR_WKUP_PADCON FIG13 | T1          | MCU_OSPI1_CLK               |                                   |                                   |   |                            |              |   | WKUP_GPIO0_25 |           |
| 0x4301C038 | CTRLMMR_WKUP_PADCON FIG14 | R1          | MCU_OSPI1_LBC LKO           | MCU_OSPI0_CS <sub>n</sub> 2       | MCU_HYPERBUS 0_RESE <sub>Tn</sub> |   |                            |              |   | WKUP_GPIO0_26 |           |
| 0x4301C03C | CTRLMMR_WKUP_PADCON FIG15 | P2          | MCU_OSPI1_DQS               | MCU_OSPI0_CS <sub>n</sub> 3       | MCU_HYPERBUS 0_INT <sub>n</sub>   |   |                            |              |   | WKUP_GPIO0_27 |           |
| 0x4301C040 | CTRLMMR_WKUP_PADCON FIG16 | P3          | MCU_OSPI1_D0                |                                   |                                   |   |                            |              |   | WKUP_GPIO0_28 |           |
| 0x4301C044 | CTRLMMR_WKUP_PADCON FIG17 | P4          | MCU_OSPI1_D1                |                                   |                                   |   | MCU_UART0_RXD              | MCU_SPI1_CS1 |   | WKUP_GPIO0_29 |           |
| 0x4301C048 | CTRLMMR_WKUP_PADCON FIG18 | P5          | MCU_OSPI1_D2                |                                   |                                   |   | MCU_UART0_TXD              | MCU_SPI1_CS2 |   | WKUP_GPIO0_30 |           |
| 0x4301C04C | CTRLMMR_WKUP_PADCON FIG19 | P1          | MCU_OSPI1_D3                |                                   |                                   |   | MCU_UART0_CTS <sub>n</sub> | MCU_SPI0_CS1 |   | WKUP_GPIO0_31 |           |
| 0x4301C050 | CTRLMMR_WKUP_PADCON FIG20 | N2          | MCU_OSPI1_CS <sub>n</sub> 0 |                                   |                                   |   |                            |              |   | WKUP_GPIO0_32 |           |

**Table 5-76. Pin Multiplexing (continued)**

| ADDRESS    | REGISTER NAME             | BALL NUMBER | MUXMODE[7:0] SETTINGS |                    |               |                     |                |              |   |               |                 |
|------------|---------------------------|-------------|-----------------------|--------------------|---------------|---------------------|----------------|--------------|---|---------------|-----------------|
|            |                           |             | 0                     | 1                  | 2             | 3                   | 4              | 5            | 6 | 7             | Bootstrap       |
| 0x4301C054 | CTRLMMR_WKUP_PADCON FIG21 | N3          | MCU_OSPI1_CSn1        | MCU_HYPERBUS_0_WPn | MCU_TIMER_IO0 | MCU_HYPERBUS_0_CSn1 | MCU_UART0_RTSn | MCU_SPI0_CS2 |   | WKUP_GPIO0_33 |                 |
| 0x4301C058 | CTRLMMR_WKUP_PADCON FIG22 | N4          | MCU_RGMII1_TX_CTL     | MCU_RMII1_CRSDV    |               |                     |                |              |   | WKUP_GPIO0_34 |                 |
| 0x4301C05C | CTRLMMR_WKUP_PADCON FIG23 | N5          | MCU_RGMII1_RX_CTL     | MCU_RMII1_RX_ER    |               |                     |                |              |   | WKUP_GPIO0_35 |                 |
| 0x4301C060 | CTRLMMR_WKUP_PADCON FIG24 | M2          | MCU_RGMII1_TD3        |                    |               |                     |                |              |   | WKUP_GPIO0_36 |                 |
| 0x4301C064 | CTRLMMR_WKUP_PADCON FIG25 | M3          | MCU_RGMII1_TD2        |                    |               |                     |                |              |   | WKUP_GPIO0_37 |                 |
| 0x4301C068 | CTRLMMR_WKUP_PADCON FIG26 | M4          | MCU_RGMII1_TD1        | MCU_RMII1_TXD1     |               |                     |                |              |   | WKUP_GPIO0_38 |                 |
| 0x4301C06C | CTRLMMR_WKUP_PADCON FIG27 | M5          | MCU_RGMII1_TD0        | MCU_RMII1_TXD0     |               |                     |                |              |   | WKUP_GPIO0_39 |                 |
| 0x4301C070 | CTRLMMR_WKUP_PADCON FIG28 | N1          | MCU_RGMII1_TX_C       | MCU_RMII1_TX_EN    |               |                     |                |              |   | WKUP_GPIO0_40 |                 |
| 0x4301C074 | CTRLMMR_WKUP_PADCON FIG29 | M1          | MCU_RGMII1_RX_C       | MCU_RMII1_REF_CLK  |               |                     |                |              |   | WKUP_GPIO0_41 |                 |
| 0x4301C078 | CTRLMMR_WKUP_PADCON FIG30 | L2          | MCU_RGMII1_RD3        |                    |               |                     |                |              |   | WKUP_GPIO0_42 |                 |
| 0x4301C07C | CTRLMMR_WKUP_PADCON FIG31 | L5          | MCU_RGMII1_RD2        |                    |               |                     |                |              |   | WKUP_GPIO0_43 |                 |
| 0x4301C080 | CTRLMMR_WKUP_PADCON FIG32 | M6          | MCU_RGMII1_RD1        | MCU_RMII1_RXD1     |               |                     |                |              |   | WKUP_GPIO0_44 |                 |
| 0x4301C084 | CTRLMMR_WKUP_PADCON FIG33 | L6          | MCU_RGMII1_RD0        | MCU_RMII1_RXD0     |               |                     |                |              |   | WKUP_GPIO0_45 |                 |
| 0x4301C088 | CTRLMMR_WKUP_PADCON FIG34 | L4          | MCU_MDIO0_MDI_O       |                    |               |                     |                |              |   | WKUP_GPIO0_46 |                 |
| 0x4301C08C | CTRLMMR_WKUP_PADCON FIG35 | L1          | MCU_MDIO0_MD_C        |                    |               |                     |                |              |   | WKUP_GPIO0_47 |                 |
| 0x4301C090 | CTRLMMR_WKUP_PADCON FIG36 | Y1          | MCU_SPI0_CLK          |                    |               |                     |                |              |   | WKUP_GPIO0_48 | MCU_BOOTMODE 06 |
| 0x4301C094 | CTRLMMR_WKUP_PADCON FIG37 | Y3          | MCU_SPI0_D0           |                    |               |                     |                |              |   | WKUP_GPIO0_49 | MCU_BOOTMODE 07 |
| 0x4301C098 | CTRLMMR_WKUP_PADCON FIG38 | Y2          | MCU_SPI0_D1           |                    |               |                     |                |              |   | WKUP_GPIO0_50 | MCU_BOOTMODE 05 |
| 0x4301C09C | CTRLMMR_WKUP_PADCON FIG39 | Y4          | MCU_SPI0_CS0          |                    |               |                     |                |              |   | WKUP_GPIO0_51 |                 |
| 0x4301C0A0 | CTRLMMR_WKUP_PADCON FIG40 | AB1         | WKUP_UART0_RX_D       |                    |               |                     |                |              |   | WKUP_GPIO0_52 |                 |
| 0x4301C0A4 | CTRLMMR_WKUP_PADCON FIG41 | AB5         | WKUP_UART0_TX_D       |                    |               |                     |                |              |   | WKUP_GPIO0_53 |                 |
| 0x4301C0A8 | CTRLMMR_WKUP_PADCON FIG42 | W1          | MCU_MCAN0_TX          |                    |               |                     |                |              |   | WKUP_GPIO0_54 |                 |
| 0x4301C0AC | CTRLMMR_WKUP_PADCON FIG43 | W2          | MCU_MCAN0_RX          |                    |               |                     |                |              |   | WKUP_GPIO0_55 |                 |
| 0x4301C0B0 | CTRLMMR_WKUP_PADCON FIG44 | AF4         | WKUP_GPIO0_0          | MCU_SPI1_CLK       |               |                     |                |              |   | WKUP_GPIO0_0  | MCU_BOOTMODE 00 |

Table 5-76. Pin Multiplexing (continued)

| ADDRESS    | REGISTER NAME             | BALL NUMBER | MUXMODE[7:0] SETTINGS |                  |                      |                       |                    |                 |             |               | Bootstrap       |
|------------|---------------------------|-------------|-----------------------|------------------|----------------------|-----------------------|--------------------|-----------------|-------------|---------------|-----------------|
|            |                           |             | 0                     | 1                | 2                    | 3                     | 4                  | 5               | 6           | 7             |                 |
| 0x4301C0B4 | CTRLMMR_WKUP_PADCON FIG45 | AF3         | WKUP_GPIO0_1          | MCU_SPI1_D0      |                      |                       |                    |                 |             | WKUP_GPIO0_1  | MCU_BOOTMODE 01 |
| 0x4301C0B8 | CTRLMMR_WKUP_PADCON FIG46 | AE3         | WKUP_GPIO0_2          | MCU_SPI1_D1      |                      |                       |                    |                 |             | WKUP_GPIO0_2  | MCU_BOOTMODE 02 |
| 0x4301C0BC | CTRLMMR_WKUP_PADCON FIG47 | AD1         | WKUP_GPIO0_3          | MCU_SPI1_CS0     |                      |                       |                    |                 |             | WKUP_GPIO0_3  | MCU_BOOTMODE 03 |
| 0x4301C0C0 | CTRLMMR_WKUP_PADCON FIG48 | AC3         | WKUP_GPIO0_4          | MCU_MCAN1_TX     | MCU_SPI0_CS3         | MCU_ADC_EXT_T RIGGER0 |                    |                 |             | WKUP_GPIO0_4  | MCU_BOOTMODE 04 |
| 0x4301C0C4 | CTRLMMR_WKUP_PADCON FIG49 | AD3         | WKUP_GPIO0_5          | MCU_MCAN1_RX     | MCU_SPI1_CS3         | MCU_ADC_EXT_T RIGGER1 |                    |                 |             | WKUP_GPIO0_5  |                 |
| 0x4301C0C8 | CTRLMMR_WKUP_PADCON FIG50 | AC2         | WKUP_GPIO0_6          | WKUP_UART0_CT Sn | MCU_CPTS0_HW 1TSPUSH |                       |                    |                 |             | WKUP_GPIO0_6  |                 |
| 0x4301C0CC | CTRLMMR_WKUP_PADCON FIG51 | AC1         | WKUP_GPIO0_7          | WKUP_UART0_RT Sn | MCU_CPTS0_HW 2TSPUSH |                       |                    |                 |             | WKUP_GPIO0_7  |                 |
| 0x4301C0D0 | CTRLMMR_WKUP_PADCON FIG52 | AC5         | WKUP_GPIO0_8          |                  | MCU_CPTS0_TS_ SYNC   |                       |                    |                 |             | WKUP_GPIO0_8  | MCU_BOOTMODE 08 |
| 0x4301C0D4 | CTRLMMR_WKUP_PADCON FIG53 | AB4         | WKUP_GPIO0_9          |                  | MCU_CPTS0_TS_ COMP   |                       |                    |                 |             | WKUP_GPIO0_9  | MCU_BOOTMODE 09 |
| 0x4301C0D8 | CTRLMMR_WKUP_PADCON FIG54 | AB3         | WKUP_GPIO0_10         | MCU_EXT_REFCL K0 |                      |                       | MCU_CPTS0_RFT _CLK | MCU_SYSCLKOU T0 |             | WKUP_GPIO0_10 |                 |
| 0x4301C0DC | CTRLMMR_WKUP_PADCON FIG55 | AB2         | WKUP_GPIO0_11         | MCU_OBSCLK0      |                      |                       | MCU_TIMER_IO1      |                 | MCU_CLKOUT0 | WKUP_GPIO0_11 |                 |
| 0x4301C0E0 | CTRLMMR_WKUP_PADCON FIG56 | AC7         | WKUP_I2C0_SCL         |                  |                      |                       |                    |                 |             |               |                 |
| 0x4301C0E4 | CTRLMMR_WKUP_PADCON FIG57 | AD6         | WKUP_I2C0_SDA         |                  |                      |                       |                    |                 |             |               |                 |
| 0x4301C0E8 | CTRLMMR_WKUP_PADCON FIG58 | AD8         | MCU_I2C0_SCL          |                  |                      |                       |                    |                 |             |               |                 |
| 0x4301C0EC | CTRLMMR_WKUP_PADCON FIG59 | AD7         | MCU_I2C0_SDA          |                  |                      |                       |                    |                 |             |               |                 |
| 0x4301C0F0 | CTRLMMR_WKUP_PADCON FIG60 | AA5         | PMIC_POWER_EN 1       |                  |                      |                       |                    |                 |             |               |                 |
| 0x4301C0F4 | CTRLMMR_WKUP_PADCON FIG61 | W3          | MCU_SAFETY_ER RORn    |                  |                      |                       |                    |                 |             |               |                 |
| 0x4301C0F8 | CTRLMMR_WKUP_PADCON FIG62 | W4          | MCU_RESETh            |                  |                      |                       |                    |                 |             |               |                 |
| 0x4301C0FC | CTRLMMR_WKUP_PADCON FIG63 | V3          | MCU_RESETh            |                  |                      |                       |                    |                 |             |               |                 |
| 0x4301C100 | CTRLMMR_WKUP_PADCON FIG64 | V2          | MCU_PORz_OUT          |                  |                      |                       |                    |                 |             |               |                 |
| 0x4301C104 | CTRLMMR_WKUP_PADCON FIG65 | AA4         | TCK                   |                  |                      |                       |                    |                 |             |               |                 |
| 0x4301C108 | CTRLMMR_WKUP_PADCON FIG66 | AA3         | TRSTn                 |                  |                      |                       |                    |                 |             |               |                 |
| 0x4301C10C | CTRLMMR_WKUP_PADCON FIG67 | AA2         | EMU0                  |                  |                      |                       |                    |                 |             |               |                 |
| 0x4301C110 | CTRLMMR_WKUP_PADCON FIG68 | AA1         | EMU1                  |                  |                      |                       |                    |                 |             |               |                 |

Table 5-76. Pin Multiplexing (continued)

| ADDRESS    | REGISTER NAME                | BALL<br>NUMBER | MUXMODE[7:0] SETTINGS |   |   |   |   |   |   |   |           |
|------------|------------------------------|----------------|-----------------------|---|---|---|---|---|---|---|-----------|
|            |                              |                | 0                     | 1 | 2 | 3 | 4 | 5 | 6 | 7 | Bootstrap |
| 0x4301C114 | CTRLMMR_WKUP_PADCON<br>FIG69 | Y5             | PMIC_POWER_EN<br>0    |   |   |   |   |   |   |   |           |

## 5.5 Connections for Unused Pins

This section describes the Unused/Reserved balls connection requirements.

### Note

All power balls must be supplied with the voltages specified in [Section 6.4, Recommended Operating Conditions](#), unless otherwise specified in [Section 5.3, Signal Descriptions](#).

**Table 5-77. Unused Balls Specific Connection Requirements**

| BALL NUMBER | BALL NAME      | CONNECTION REQUIREMENTS                                                                                                                                     |
|-------------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C22         | OSC1_XI        | Each of these balls must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low level if unused. |
| AE4         | WKUP_LFOSC0_XI |                                                                                                                                                             |
| AA3         | TRSTn          |                                                                                                                                                             |
| K2          | MCU_ADC0_REFN  |                                                                                                                                                             |
| K3          | MCU_ADC0_REFP  |                                                                                                                                                             |
| V5          | MCU_BYP_POR    |                                                                                                                                                             |
| H2          | MCU_ADC1_REFP  |                                                                                                                                                             |
| H3          | MCU_ADC1_REFN  |                                                                                                                                                             |
| K5          | MCU_ADC0_AIN0  |                                                                                                                                                             |
| J3          | MCU_ADC0_AIN1  |                                                                                                                                                             |
| J1          | MCU_ADC0_AIN2  |                                                                                                                                                             |
| J5          | MCU_ADC0_AIN3  |                                                                                                                                                             |
| K4          | MCU_ADC0_AIN4  |                                                                                                                                                             |
| J4          | MCU_ADC0_AIN5  |                                                                                                                                                             |
| J2          | MCU_ADC0_AIN6  |                                                                                                                                                             |
| J6          | MCU_ADC0_AIN7  |                                                                                                                                                             |
| F4          | MCU_ADC1_AIN0  |                                                                                                                                                             |
| G6          | MCU_ADC1_AIN1  |                                                                                                                                                             |
| G4          | MCU_ADC1_AIN2  |                                                                                                                                                             |
| H5          | MCU_ADC1_AIN3  |                                                                                                                                                             |
| F5          | MCU_ADC1_AIN4  |                                                                                                                                                             |
| G5          | MCU_ADC1_AIN5  |                                                                                                                                                             |
| G3          | MCU_ADC1_AIN6  |                                                                                                                                                             |
| H4          | MCU_ADC1_AIN7  |                                                                                                                                                             |



**Table 5-77. Unused Balls Specific Connection Requirements (continued)**

| BALL NUMBER | BALL NAME       | CONNECTION REQUIREMENTS                                                                                                                                                                                |
|-------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F17         | RESETz          | Each of these balls must be connected to the corresponding power supply through a separate external pull resistor to ensure these balls are held to a valid logic high level if unused. <sup>(1)</sup> |
| W4          | MCU_RESETz      |                                                                                                                                                                                                        |
| W5          | MCU_PORz        |                                                                                                                                                                                                        |
| E19         | PORz            |                                                                                                                                                                                                        |
| AA4         | TCK             |                                                                                                                                                                                                        |
| A21         | TMS             |                                                                                                                                                                                                        |
| AC7         | WKUP_I2C0_SCL   |                                                                                                                                                                                                        |
| AD6         | WKUP_I2C0_SDA   |                                                                                                                                                                                                        |
| AD7         | MCU_I2C0_SDA    |                                                                                                                                                                                                        |
| AD8         | MCU_I2C0_SCL    |                                                                                                                                                                                                        |
| F18         | NMIIn           |                                                                                                                                                                                                        |
| C20         | TDI             |                                                                                                                                                                                                        |
| A20         | TDO             |                                                                                                                                                                                                        |
| AA1         | EMU1            |                                                                                                                                                                                                        |
| AA2         | EMU0            |                                                                                                                                                                                                        |
| F21         | VPP_CORE        | This ball must be left unconnected if unused.                                                                                                                                                          |
| T6          | VPP_MCU         |                                                                                                                                                                                                        |
| AG5         | SERDES0_REFCLKN |                                                                                                                                                                                                        |
| AG6         | SERDES0_REFCLKP |                                                                                                                                                                                                        |
| AC9         | SERDES0_REFRES  |                                                                                                                                                                                                        |
| AH3         | SERDES0_RXN     |                                                                                                                                                                                                        |
| AG2         | SERDES0_RXP     |                                                                                                                                                                                                        |
| AH4         | SERDES0_TXN     |                                                                                                                                                                                                        |
| AG3         | SERDES0_TXP     |                                                                                                                                                                                                        |
| AH6         | SERDES1_REFCLKN |                                                                                                                                                                                                        |
| AH7         | SERDES1_REFCLKP |                                                                                                                                                                                                        |
| AC14        | SERDES1_REFRES  |                                                                                                                                                                                                        |
| AG9         | SERDES1_RXN     |                                                                                                                                                                                                        |
| AH10        | SERDES1_RXP     |                                                                                                                                                                                                        |
| AH9         | SERDES1_TXN     |                                                                                                                                                                                                        |
| AG8         | SERDES1_TXP     |                                                                                                                                                                                                        |

(1) To determine which power supply is associated with any IO refer to [Table 5-1, Pin Attributes](#).

**Table 5-78. Reserved Balls Specific Connection Requirements**

| BALLS                                                                                                                                                                                                                             | CONNECTION REQUIREMENTS                                                                                                                   |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| AA6 (RSV2), B1 (RSV3), AC23 (RSV4), C12 (RSV5), F9 (RSV6), F10 (RSV7), AD10 (RSV8), AC13 (RSV9), B28 (RSV10), A27 (RSV11), D23 (RSV12), E23 (RSV13), W6 (TEMP_DIODE_P), F16 (DDR_FS_RESETh), D24 (MMC0_CALPAD), F23 (MMC1_CALPAD) | These balls must be left unconnected.                                                                                                     |
| V4 (RSV1)                                                                                                                                                                                                                         | These balls must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low level. |

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### Note

All other unused signal balls **with** a Pad Configuration Register can be left unconnected with their multiplexing mode set to GPIO input and internal pulldown resistor enabled.

Unused balls are defined as those which only connect to a PCB solder pad. This is the only use case where internal pull resistors are allowed as the only source/sink to hold a valid logic level.

Any balls connected to a via, test point, or PCB trace are considered used and must not depend on the internal pull resistor to hold a valid logic level.

Internal pull resistors are weak and may not source enough current to maintain a valid logic level for some operating conditions. This may be the case when connected to components with leakage to the opposite logic level, or when external noise sources couple to signal traces attached to balls which are only pulled to a valid logic level by the internal resistor. Therefore, external pull resistors may be required to hold a valid logic level on balls with external connections.

If balls are allowed to float between valid logic levels, the input buffer may enter a high-current state which could damage the IO cell.

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## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETERS          |                                                                    | MIN  | MAX | UNIT |
|---------------------|--------------------------------------------------------------------|------|-----|------|
| VDD_CORE            | Supply voltage range for CORE domain                               | -0.3 | 1.3 | V    |
| VDD_MCU             | Supply voltage range for R5F MCU domain                            | -0.3 | 1.3 | V    |
| VDD_MPU0            | Supply voltage range for A53 MPU0 domain                           | -0.3 | 1.3 | V    |
| VDD_MPU1            | Supply voltage range for A53 MPU1 domain                           | -0.3 | 1.3 | V    |
| VDD_WKUP0           | Supply voltage range for WKUP domain                               | -0.3 | 1.3 | V    |
| VDD_WKUP1           | Supply voltage range for WKUP domain                               | -0.3 | 1.3 | V    |
| VDD_DLL_MMC0        | Supply voltage range for MMC0 DLL                                  | -0.3 | 1.3 | V    |
| VDD_DLL_MMC1        | Supply voltage range for MMC1 DLL                                  | -0.3 | 1.3 | V    |
| VDDA_1P8_CSI0       | Supply voltage range for CSI PHY, Analog, 1.8 V                    | -0.3 | 2.2 | V    |
| VDDA_1P8_OLDIO      | Supply voltage range for OLDIO, Analog, 1.8 V                      | -0.3 | 2.2 | V    |
| VDDA_1P8_SDIO       | Supply voltage range for SDIO LDO, Analog, 1.8 V                   | -0.3 | 2.2 | V    |
| VDDA_1P8_SERDES0    | Supply voltage range for USB, PCIE, Analog, 1.8 V                  | -0.3 | 2.2 | V    |
| VDDA_3P3_IOLDO_WKUP | Supply voltage range for WKUP IO Bias LDO, Analog, 3.3 V           | -0.3 | 3.8 | V    |
| VDDA_3P3_IOLDO0     | Supply voltage range for IO Bias LDO, Analog 3.3 V                 | -0.3 | 3.8 | V    |
| VDDA_3P3_IOLDO1     | Supply voltage range for IO Bias LDO, Analog 3.3 V                 | -0.3 | 3.8 | V    |
| VDDA_3P3_SDIO       | Supply voltage range for SDIO LDO, Analog, 3.3 V                   | -0.3 | 3.8 | V    |
| VDDA_3P3_USB        | Supply voltage range for USBPHY, Analog, 3.3 V                     | -0.3 | 3.8 | V    |
| VDDA_ADC_MCU        | Supply voltage range for ADC0, ADC1, Analog                        | -0.3 | 2.2 | V    |
| VDDA_PLL0_DDR       | Supply voltage range for DDR DPLL, Analog                          | -0.3 | 2.2 | V    |
| VDDA_PLL1_DDR       | Supply voltage range for DDR De-skew DPLL, Analog                  | -0.3 | 2.2 | V    |
| VDDA_LDO_WKUP       | Supply voltage range for WKUP LDO, Analog                          | -0.3 | 2.2 | V    |
| VDDA_MCU            | Supply voltage range for MCU SRAM LDO, MCU DPLL, CPSW DPLL, Analog | -0.3 | 2.2 | V    |
| VDDA_PLL_CORE       | Supply voltage range for CORE DPLL, PER1 DPLL, Analog              | -0.3 | 2.2 | V    |
| VDDA_PLL_DSS        | Supply voltage range for DSS DPLL, Analog                          | -0.3 | 2.2 | V    |
| VDDA_PLL_MPU0       | Supply voltage range for MPU0 DPLL, Analog                         | -0.3 | 2.2 | V    |
| VDDA_PLL_MPU1       | Supply voltage range for MPU1 DPLL, Analog                         | -0.3 | 2.2 | V    |
| VDDA_PLL_PER0       | Supply voltage range for PER0 DPLL, Analog                         | -0.3 | 2.2 | V    |
| VDDA_POR_WKUP       | Supply voltage range for WKUP POR, Analog                          | -0.3 | 2.2 | V    |
| VDDA_SRAM_CORE0     | Supply voltage range for CORE SRAM LDOs, Analog                    | -0.3 | 2.2 | V    |
| VDDA_SRAM_CORE1     | Supply voltage range for CORE SRAM LDOs, Analog                    | -0.3 | 2.2 | V    |
| VDDA_SRAM_MPU0      | Supply voltage range for MPU SRAM LDOs, Analog                     | -0.3 | 2.2 | V    |
| VDDA_SRAM_MPU1      | Supply voltage range for MPU SRAM LDOs, Analog                     | -0.3 | 2.2 | V    |
| VDDA_WKUP           | Supply voltage range for WKUP OSC, SRAM LDO, Analog                | -0.3 | 2.2 | V    |
| VDDS_DDR            | Supply voltage range for DDR IO domain                             | -0.3 | 2.2 | V    |
| VDDS_OSC1           | Supply voltage range for CORE HFOSC, Analog                        | -0.3 | 2.2 | V    |
| VDDS0               | Supply voltage range for VDDSHV0 IO bias                           | -0.3 | 2.2 | V    |
| VDDS0_WKUP          | Supply voltage range for VDDSHV0_WKUP IO bias                      | -0.3 | 2.2 | V    |
| VDDS1               | Supply voltage range for VDDSHV1 IO bias                           | -0.3 | 2.2 | V    |
| VDDS1_WKUP          | Supply voltage range for VDDSHV1_WKUP IO bias                      | -0.3 | 2.2 | V    |
| VDDS2               | Supply voltage range for VDDSHV2 IO bias                           | -0.3 | 2.2 | V    |

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

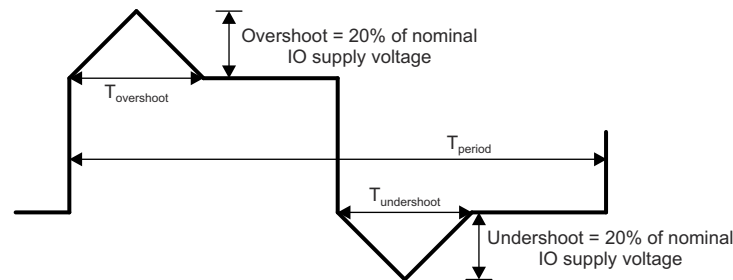
| PARAMETERS                                                    |                                                                                                                        | MIN   | MAX                      | UNIT  |
|---------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-------|--------------------------|-------|
| VDDS2_WKUP                                                    | Supply voltage range for VDDSHV2_WKUP IO bias                                                                          | -0.3  | 2.2                      | V     |
| VDDS3                                                         | Supply voltage range for VDDSHV3 IO bias                                                                               | -0.3  | 2.2                      | V     |
| VDDS4                                                         | Supply voltage range for VDDSHV4 IO bias                                                                               | -0.3  | 2.2                      | V     |
| VDDS5                                                         | Supply voltage range for VDDSHV5 IO bias                                                                               | -0.3  | 2.2                      | V     |
| VDDS6                                                         | Supply voltage range for VDDSHV6 IO bias                                                                               | -0.3  | 2.2                      | V     |
| VDDS7                                                         | Supply voltage range for VDDSHV7 IO bias                                                                               | -0.3  | 2.2                      | V     |
| VDDS8                                                         | Supply voltage range for VDDSHV8 IO bias                                                                               | -0.3  | 2.2                      | V     |
| VDDSHV0                                                       | Supply voltage range for dual-voltage IO domain                                                                        | 1.8 V | -0.3                     | 2.2 V |
|                                                               |                                                                                                                        | 3.3 V | -0.3                     | 3.8 V |
| VDDSHV0_WKUP                                                  | Supply voltage range for dual-voltage IO domain                                                                        | 1.8 V | -0.3                     | 2.2 V |
|                                                               |                                                                                                                        | 3.3 V | -0.3                     | 3.8 V |
| VDDSHV1                                                       | Supply voltage range for dual-voltage IO domain                                                                        | 1.8 V | -0.3                     | 2.2 V |
|                                                               |                                                                                                                        | 3.3 V | -0.3                     | 3.8 V |
| VDDSHV1_WKUP                                                  | Supply voltage range for dual-voltage IO domain                                                                        | 1.8 V | -0.3                     | 2.2 V |
|                                                               |                                                                                                                        | 3.3 V | -0.3                     | 3.8 V |
| VDDSHV2                                                       | Supply voltage range for dual-voltage IO domain                                                                        | 1.8 V | -0.3                     | 2.2 V |
|                                                               |                                                                                                                        | 3.3 V | -0.3                     | 3.8 V |
| VDDSHV2_WKUP                                                  | Supply voltage range for dual-voltage IO domain                                                                        | 1.8 V | -0.3                     | 2.2 V |
|                                                               |                                                                                                                        | 3.3 V | -0.3                     | 3.8 V |
| VDDSHV3                                                       | Supply voltage range for dual-voltage IO domain                                                                        | 1.8 V | -0.3                     | 2.2 V |
|                                                               |                                                                                                                        | 3.3 V | -0.3                     | 3.8 V |
| VDDSHV4                                                       | Supply voltage range for dual-voltage IO domain                                                                        | 1.8 V | -0.3                     | 2.2 V |
|                                                               |                                                                                                                        | 3.3 V | -0.3                     | 3.8 V |
| VDDSHV5                                                       | Supply voltage range for dual-voltage IO domain                                                                        | 1.8 V | -0.3                     | 2.2 V |
|                                                               |                                                                                                                        | 3.3 V | -0.3                     | 3.8 V |
| VDDSHV6                                                       | Supply voltage range for dual-voltage IO domain                                                                        | 1.8 V | -0.3                     | 2.2 V |
|                                                               |                                                                                                                        | 3.3 V | -0.3                     | 3.8 V |
| VDDSHV7                                                       | Supply voltage range for dual-voltage IO domain                                                                        | 1.8 V | -0.3                     | 2.2 V |
|                                                               |                                                                                                                        | 3.3 V | -0.3                     | 3.8 V |
| VDDSHV8                                                       | Supply voltage range for dual-voltage IO domain                                                                        | 1.8 V | -0.3                     | 2.2 V |
|                                                               |                                                                                                                        | 3.3 V | -0.3                     | 3.8 V |
| VPP_CORE                                                      | Supply voltage range for CORE EFUSE domain                                                                             |       | NC <sup>(8)</sup>        | V     |
| VPP_MCU                                                       | Supply voltage range for MCU EFUSE domain                                                                              | -0.3  | 1.89                     | V     |
| USB0_VBUS                                                     | Voltage range for USB VBUS comparator input                                                                            | -0.3  | 1.89                     | V     |
| USB1_VBUS                                                     | Voltage range for USB VBUS comparator input                                                                            | -0.3  | 1.89                     | V     |
| Steady State Max. Voltage at all fail-safe IO pins            | I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA, NMI <sub>in</sub> , VDDA_3P3_MON_WKUP, VDDA_3P3_MON0                           | -0.3  | 3.8                      | V     |
|                                                               | VDDA_1P8_MON_WKUP, VDDA_1P8_MON0                                                                                       | -0.3  | 2.2                      | V     |
|                                                               | DDR_FS_RESETE <sub>n</sub>                                                                                             | -0.3  | 2.2                      | V     |
| Steady State Max. Voltage at all other IO pins <sup>(3)</sup> | VDDA_VSYS_MON <sup>(4)</sup>                                                                                           | -0.3  | 2.2 <sup>(7)</sup>       | V     |
|                                                               | All other IO pins                                                                                                      | -0.3  | IO supply voltage + 0.3  | V     |
| Transient Overshoot and Undershoot specification at IO pins   | 20% of IO supply voltage for up to 20% of signal period (see <a href="#">Figure 6-1, IO Transient Voltage Ranges</a> ) |       | 0.2 × VDD <sup>(5)</sup> | V     |

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETERS               |                     | MIN | MAX  | UNIT |
|--------------------------|---------------------|-----|------|------|
| $T_{STG}$ <sup>(6)</sup> | Storage temperature | -55 | +150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 6.4, Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to their associated VSS or VSSA\_x, unless otherwise noted.
- (3) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be -0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.
- (4) The VDDA\_VSYS\_MON pin provides a way to monitor the system power supply and is not fail-safe, unless implemented with the appropriate resistor voltage divider source. For more information, see [Section 8.2.5, System Power Supply Monitor Design Guidelines](#).
- (5) VDD is the voltage on the corresponding power-supply pin(s) for the IO.
- (6) For tape and reel the storage temperature range is [-10°C; +50°C] with a maximum relative humidity of 70%. TI recommends returning to ambient room temperature before usage.
- (7) The voltage on the VDDA\_VSYS\_MON pin should never exceed VDDA\_POR\_WKUP's voltage.
- (8) NC stands for No Connect.

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The I2C0\_SCL, I2C0\_SDA, I2C1\_SCL, I2C1\_SDA, DDR\_FS\_RESETn, NMI<sub>n</sub>, VDDA\_1P8\_MON\_WKUP, VDDA\_1P8\_MON0, VDDA\_3P3\_MON\_WKUP, and VDDA\_3P3\_MON0 are the only fail-safe IO terminals. All other IO terminals are not fail-safe and the voltage applied to them should be limited to the value defined by the Steady State Max. Voltage at all IO pins parameter in [Section 6.1, Absolute Maximum Ratings](#).



A.  $T_{\text{overshoot}} + T_{\text{undershoot}} < 20\% \text{ of } T_{\text{period}}$

**Figure 6-1. IO Transient Voltage Ranges**

## 6.2 ESD Ratings

|             |                               |                                                                                           | VALUE  | UNIT |
|-------------|-------------------------------|-------------------------------------------------------------------------------------------|--------|------|
| $V_{(ESD)}$ | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>                         | ± 1000 | V    |
|             |                               | Charged-device model (CDM), per JEDEC specification ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | ± 250  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Power-On Hours (POH)

| OPERATING CONDITION <sup>(1) (2) (3)</sup> | COMMERCIAL TEMPERATURE RANGE           |                | EXTENDED TEMPERATURE RANGE      |                |
|--------------------------------------------|----------------------------------------|----------------|---------------------------------|----------------|
| OPP                                        | JUNCTION TEMPERATURE (T <sub>J</sub> ) | LIFETIME (POH) | JUNCTION TEMP (T <sub>J</sub> ) | LIFETIME (POH) |
| OPP_NOM                                    | 0°C to 90°C                            | 100k           | -40°C to 105°C                  | 100k           |
| OPP_OD                                     |                                        | 100k           |                                 | 100k           |
| OPP_TURBO                                  |                                        | 100k           |                                 | 55k            |

- (1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
- (2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.
- (3) POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH.

## 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(2)</sup>

| SUPPLY NAME             | DESCRIPTION                                           | MIN <sup>(1)</sup> | NOM                             | MAX <sup>(1)</sup> | UNIT                |
|-------------------------|-------------------------------------------------------|--------------------|---------------------------------|--------------------|---------------------|
| VDD_CORE <sup>(3)</sup> | CORE voltage domain supply                            | 1.05               | 1.1                             | 1.15               | V                   |
| VDD_MCU <sup>(3)</sup>  | MCU voltage domain supply                             | 1.05               | 1.1                             | 1.15               | V                   |
| VDD_MPU0 <sup>(3)</sup> | MPU0 voltage domain supply                            | OPP_NOM            | See <a href="#">Section 6.5</a> |                    | V                   |
|                         |                                                       | OPP_OD             | See <a href="#">Section 6.5</a> |                    | V                   |
|                         |                                                       | OPP_TURBO          | See <a href="#">Section 6.5</a> |                    | V                   |
| VDD_MPU1 <sup>(3)</sup> | MPU1 voltage domain supply                            | OPP_NOM            | See <a href="#">Section 6.5</a> |                    | V                   |
|                         |                                                       | OPP_OD             | See <a href="#">Section 6.5</a> |                    | V                   |
|                         |                                                       | OPP_TURBO          | See <a href="#">Section 6.5</a> |                    | V                   |
| VDD_WKUP0               | WKUP voltage domain supply                            | 1.05               | 1.1                             | 1.15               | V                   |
| VDD_WKUP1               | WKUP voltage domain supply                            | 1.05               | 1.1                             | 1.15               | V                   |
| VDD_DLL_MMC0            | MMC0 PHY DLL voltage supply                           | 1.05               | 1.1                             | 1.15               | V                   |
| VDD_DLL_MMC1            | MMC1 PHY DLL voltage supply                           | 1.05               | 1.1                             | 1.15               | V                   |
| VDDA_1P8_CSI0           | CSI PHY analog power supply                           | 1.71               | 1.8                             | 1.89               | V                   |
| VDDA_1P8_SDIO           | SDIO LDO analog power supply                          | 1.71               | 1.8                             | 1.89               | V                   |
| VDDA_1P8_OLDI0          | OLDI analog power supply                              | 1.71               | 1.8                             | 1.89               | V                   |
| VDDA_1P8_SERDES0        | SERDES0/1 (USB, PCIE, SGMII) analog power supply      | 1.71               | 1.8                             | 1.89               | V                   |
|                         | Maximum peak-to-peak supply noise                     |                    |                                 | 30                 | mV <sub>PPmax</sub> |
| VDDA_3P3_IOLDO_WKUP     | WKUP IO Bias LDO analog power supply                  | 3.14               | 3.3                             | 3.46               | V                   |
| VDDA_3P3_IOLDO0         | IO Bias LDO analog power supply                       | 3.14               | 3.3                             | 3.46               | V                   |
| VDDA_3P3_IOLDO1         | IO Bias LDO analog power supply                       | 3.14               | 3.3                             | 3.46               | V                   |
| VDDA_3P3_SDIO           | SDIO LDO analog power supply                          | 3.14               | 3.3                             | 3.46               | V                   |
| VDDA_3P3_USB            | USB analog power supply                               | 3.14               | 3.3                             | 3.46               | V                   |
| VDDA_1P8_MON_WKUP       | 1.8V supply monitor in WKUP domain                    | 1.71               | 1.8                             | 1.89               | V                   |
| VDDA_1P8_MON0           | 1.8V supply monitor in MAIN domain                    | 1.71               | 1.8                             | 1.89               | V                   |
| VDDA_3P3_MON_WKUP       | 3.3V supply monitor in WKUP domain                    | 3.14               | 3.3                             | 3.46               | V                   |
| VDDA_3P3_MON0           | 3.3V supply monitor in MAIN domain                    | 3.14               | 3.3                             | 3.46               | V                   |
| VDDA_VSYS_MON           | Supply monitor for system                             | 0                  | see <sup>(6)</sup>              | 1                  | V                   |
| VDDA_ADC_MCU            | ADC0, ADC1 analog power supply                        | 1.71               | 1.8                             | 1.89               | V                   |
| VDDA_LDO_WKUP           | WKUP LDO analog power supply                          | 1.71               | 1.8                             | 1.89               | V                   |
| VDDA_MCU                | MCU SRAM LDO, MCU DPLL, CPSW DPLL analog power supply | 1.71               | 1.8                             | 1.89               | V                   |

over operating free-air temperature range (unless otherwise noted)<sup>(2)</sup>

| SUPPLY NAME             | DESCRIPTION                                                                                |                 | MIN <sup>(1)</sup> | NOM  | MAX <sup>(1)</sup> | UNIT                |
|-------------------------|--------------------------------------------------------------------------------------------|-----------------|--------------------|------|--------------------|---------------------|
| VDDA_PLL_CORE           | CORE DPLL, PER1 DPLL analog power supply                                                   |                 | 1.71               | 1.8  | 1.89               | V                   |
|                         | Maximum peak-to-peak supply noise                                                          |                 |                    |      | 50                 | mV <sub>PPmax</sub> |
| VDDA_PLL0_DDR           | DDR DPLL analog power supply                                                               |                 | 1.71               | 1.8  | 1.89               | V                   |
|                         | Maximum peak-to-peak supply noise                                                          |                 |                    |      | 50                 | mV <sub>PPmax</sub> |
| VDDA_PLL1_DDR           | DDR De-skew DPLL analog power supply                                                       |                 | 1.71               | 1.8  | 1.89               | V                   |
|                         | Maximum peak-to-peak supply noise                                                          |                 |                    |      | 50                 | mV <sub>PPmax</sub> |
| VDDA_PLL_DSS            | DSS DPLL analog power supply                                                               |                 | 1.71               | 1.8  | 1.89               | V                   |
|                         | Maximum peak-to-peak supply noise                                                          |                 |                    |      | 50                 | mV <sub>PPmax</sub> |
| VDDA_PLL_MPU0           | MPU0 DPLL analog power supply                                                              |                 | 1.71               | 1.8  | 1.89               | V                   |
|                         | Maximum peak-to-peak supply noise                                                          |                 |                    |      | 50                 | mV <sub>PPmax</sub> |
| VDDA_PLL_MPU1           | MPU1 DPLL analog power supply                                                              |                 | 1.71               | 1.8  | 1.89               | V                   |
|                         | Maximum peak-to-peak supply noise                                                          |                 |                    |      | 50                 | mV <sub>PPmax</sub> |
| VDDA_PLL_PER0           | PER0 DPLL analog power supply                                                              |                 | 1.71               | 1.8  | 1.89               | V                   |
|                         | Maximum peak-to-peak supply noise                                                          |                 |                    |      | 50                 | mV <sub>PPmax</sub> |
| VDDA_POR_WKUP           | WKUP POR/POK analog power supply                                                           |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDA_SRAM_CORE0         | CORE SRAM LDOs analog power supply                                                         |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDA_SRAM_CORE1         | CORE SRAM LDOs analog power supply                                                         |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDA_SRAM_MPU0          | MPU SRAM LDOs analog power supply                                                          |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDA_SRAM_MPU1          | MPU SRAM LDOs analog power supply                                                          |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDA_WKUP               | WKUP High/Low Frequency Oscillator (WKUP_LFOSC0 / WKUP_OSC0), SRAM LDO analog power supply |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDS_DDR <sup>(4)</sup> | DDR IO domain power supply (DDR3L)                                                         |                 | 1.28               | 1.35 | 1.42               | V                   |
|                         | DDR IO domain power supply (DDR4)                                                          |                 | 1.14               | 1.2  | 1.26               | V                   |
|                         | DDR IO domain power supply (LPDDR4)                                                        |                 | 1.05               | 1.1  | 1.15               | V                   |
| VDDS_OSC1               | MAIN High Frequency Oscillator (OSC1) analog power supply                                  |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDS0                   | IO bias supply for VDDSHV0                                                                 |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDS0_WKUP              | IO bias supply for VDDSHV0_WKUP                                                            |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDS1                   | IO bias supply for VDDSHV1                                                                 |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDS1_WKUP              | IO bias supply for VDDSHV1_WKUP                                                            |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDS2                   | IO bias supply for VDDSHV2                                                                 |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDS2_WKUP              | IO bias supply for VDDSHV2_WKUP                                                            |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDS3                   | IO bias supply for VDDSHV3                                                                 |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDS4                   | IO bias supply for VDDSHV4                                                                 |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDS5                   | IO bias supply for VDDSHV5                                                                 |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDS6                   | IO bias supply for VDDSHV6                                                                 |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDS7                   | IO bias supply for VDDSHV7                                                                 |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDS8                   | IO bias supply for VDDSHV8                                                                 |                 | 1.71               | 1.8  | 1.89               | V                   |
| VDDSHV0                 | Dual-voltage IO domain power supply                                                        | 1.8-V operation | 1.71               | 1.8  | 1.89               | V                   |
|                         |                                                                                            | 3.3-V operation | 3.14               | 3.3  | 3.46               | V                   |
| VDDSHV0_WKUP            | Dual-voltage IO domain power supply                                                        | 1.8-V operation | 1.71               | 1.8  | 1.89               | V                   |
|                         |                                                                                            | 3.3-V operation | 3.14               | 3.3  | 3.46               | V                   |
| VDDSHV1                 | Dual-voltage IO domain power supply                                                        | 1.8-V operation | 1.71               | 1.8  | 1.89               | V                   |
|                         |                                                                                            | 3.3-V operation | 3.14               | 3.3  | 3.46               | V                   |
| VDDSHV1_WKUP            | Dual-voltage IO domain power supply                                                        | 1.8-V operation | 1.71               | 1.8  | 1.89               | V                   |
|                         |                                                                                            | 3.3-V operation | 3.14               | 3.3  | 3.46               | V                   |

over operating free-air temperature range (unless otherwise noted)<sup>(2)</sup>

| SUPPLY NAME    | DESCRIPTION                                 |                 | MIN <sup>(1)</sup> | NOM                | MAX <sup>(1)</sup> | UNIT |
|----------------|---------------------------------------------|-----------------|--------------------|--------------------|--------------------|------|
| VDDSHV2        | Dual-voltage IO domain power supply         | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                |                                             | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| VDDSHV2_WKUP   | Dual-voltage IO domain power supply         | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                |                                             | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| VDDSHV3        | Dual-voltage IO domain power supply         | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                |                                             | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| VDDSHV4        | Dual-voltage IO domain power supply         | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                |                                             | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| VDDSHV5        | Dual-voltage IO domain power supply         | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                |                                             | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| VDDSHV6        | Dual-voltage IO domain power supply         | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                |                                             | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| VDDSHV7        | Dual-voltage IO domain power supply         | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                |                                             | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| VDDSHV8        | Dual-voltage IO domain power supply         | 1.8-V operation | 1.71               | 1.8                | 1.89               | V    |
|                |                                             | 3.3-V operation | 3.14               | 3.3                | 3.46               | V    |
| USB0_VBUS      | Voltage range for USB VBUS comparator input |                 | 0                  | see <sup>(7)</sup> | 1.89               | V    |
| USB1_VBUS      | Voltage range for USB VBUS comparator input |                 | 0                  | see <sup>(7)</sup> | 1.89               | V    |
| USB0_ID        | Voltage range for the USB ID input          |                 |                    | see <sup>(5)</sup> |                    | V    |
| USB1_ID        | Voltage range for the USB ID input          |                 |                    | see <sup>(5)</sup> |                    | V    |
| VSS            | Ground                                      |                 |                    | 0                  |                    | V    |
| T <sub>J</sub> | Operating junction temperature range        | Extended        | -40                |                    | 105                | °C   |
|                |                                             | Commercial      | 0                  |                    | 90                 | °C   |

- (1) The voltage at the device ball must never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, and so forth.
- (2) Refer to *Power-On-Hour (POH) Limits* for limitations.
- (3) This value is without AVS. The AVS Voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the VTM\_DEVINFO\_VDn. For information about VTM\_DEVINFO\_VDn registers address, please refer to section *Voltage and Thermal Manager (VTM)* in the device TRM. The power supply should be adjustable over the following ranges for each required OPP:
  - OPP\_NOM: 0.9 V – 1.1 V
  - OPP\_OD: 0.9 V – 1.2 V
  - OPP\_TURBO: 0.9 V – 1.24 V
 The AVS Voltages will be within the above specified ranges.
- (4) VDDS\_DDR is required to still be powered with either DDR4 voltage ranges, even if DDR interface is unused.
- (5) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSS with a resistance less than 10 Ω or greater than 100 kΩ. The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.
- (6) The VDDA\_VSYS\_MON pin provides a way to monitor the system power supply and is not fail-safe, unless implemented with the appropriate resistor voltage divider source. For more information, see [Section 8.2.5, System Power Supply Monitor Design Guidelines](#).
- (7) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see [Section 8.2.3, USB Design Guidelines](#).



## 6.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each operating performance point for processor clocks and device core clocks.

### Note

The OPP voltage and frequency values may change following the silicon characterization result.

Table 6-1 describes the maximum supported frequency per speed grade for the device.

**Table 6-1. Speed Grade Maximum Frequency**

| DEVICE <sup>(1)</sup> | MAXIMUM FREQUENCY (MHz) |     |      |     |        |       |                |
|-----------------------|-------------------------|-----|------|-----|--------|-------|----------------|
|                       | MPU                     | MCU | DMSC | GPU | CBASS0 | ICSSG | DDR4           |
| AM6548xxX             | 1100                    | 400 | 200  | 450 | 250    | 250   | 800 (DDR-1600) |
| AM6528xxX             | 1100                    | 400 | 200  | 450 | 250    | 250   | 800 (DDR-1600) |
| AM6546xxX             | 1100                    | 400 | 200  | N/A | 250    | 250   | 800 (DDR-1600) |
| AM6526xxX             | 1100                    | 400 | 200  | N/A | 250    | 250   | 800 (DDR-1600) |

(1) N/A stands for Not Applicable.

### 6.5.1 Voltage and Core Clock Specifications

Table 6-2 through Table 6-3 defines the device Operating Performance Points (OPPs). As shown in these tables, each OPP defines a voltage and frequency pair for a given voltage domain supply.

### Note

This device, when used in a production system, only supports one static OPP over the lifetime of the device. When designing a production system, a fixed OPP should be selected based on the maximum frequency required by the system. The corresponding OPP voltage must then be exclusively used by the device.

**Table 6-2. VDD\_MPU0 OPPs**

| VDD_MPU0 OPPs <sup>(1)</sup> | VDD_MPU0 |      |      | MPU0    |
|------------------------------|----------|------|------|---------|
|                              | MIN      | NOM  | MAX  |         |
| OPP_NOM                      | 1.06     | 1.1  | 1.16 | 800 MHz |
| OPP_OD                       | 1.14     | 1.2  | 1.26 | 1 GHz   |
| OPP_TURBO                    | 1.2      | 1.24 | 1.28 | 1.1 GHz |

(1) For additional details about supported AVS Voltages, refer to the footnotes associated with Section 6.4, *Recommended Operating Conditions*.

**Table 6-3. VDD\_MPU1 OPPs**

| VDD_MPU1 OPPs <sup>(1)</sup> | VDD_MPU1 |      |      | MPU1    |
|------------------------------|----------|------|------|---------|
|                              | MIN      | NOM  | MAX  |         |
| OPP_NOM                      | 1.06     | 1.1  | 1.16 | 800 MHz |
| OPP_OD                       | 1.14     | 1.2  | 1.26 | 1 GHz   |
| OPP_TURBO                    | 1.2      | 1.24 | 1.28 | 1.1 GHz |

(1) For additional details about supported AVS Voltages, refer to the footnotes associated with Section 6.4, *Recommended Operating Conditions*.

Table 6-4 describes the standard processor clocks speed characteristics vs OPP of the device.

**Table 6-4. Supported OPP vs Max Frequency**

| CLOCK <sup>(1) (2)</sup> | OPP_NOM                 | OPP_OD                  | OPP_TURBO               |
|--------------------------|-------------------------|-------------------------|-------------------------|
|                          | MAXIMUM FREQUENCY (MHz) | MAXIMUM FREQUENCY (MHz) | MAXIMUM FREQUENCY (MHz) |
| <b>VD_CORE</b>           |                         |                         |                         |
| GPU                      | 450                     | N/A                     | N/A                     |
| DDR4                     | 800 (DDR-1600)          | N/A                     | N/A                     |
| CBASS0                   | 250                     | N/A                     | N/A                     |
| ICSSG                    | 250                     | N/A                     | N/A                     |
| <b>VD_MPU0</b>           |                         |                         |                         |
| MPU0                     | 800                     | 1000                    | 1100                    |
| <b>VD_MPU1</b>           |                         |                         |                         |
| MPU1                     | 800                     | 1000                    | 1100                    |
| <b>VD_MCU</b>            |                         |                         |                         |
| MCU                      | 400                     | N/A                     | N/A                     |
| <b>VD_WKUP</b>           |                         |                         |                         |
| DMSC                     | 200                     | N/A                     | N/A                     |

(1) N/A stands for Not Applicable.

(2) Maximum supported frequency is limited to the device speed grade (see [Table 6-1, Speed Grade Maximum Frequency](#)).

## 6.6 Electrical Characteristics

### Note

The interfaces or signals described in [Section 6.6.1](#) through [Section 6.6.5.1](#) correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

### 6.6.1 I2C OPEN DRAIN DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER                                                                         |                                                                                                                                                                                                                                                                                                               | MIN                 | TYP | MAX | UNIT |
|-----------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-----|-----|------|
| BALL NAMES in Mode 0: WKUP_I2C0_SCL / WKUP_I2C0_SDA / MCU_I2C0_SCL / MCU_I2C0_SDA |                                                                                                                                                                                                                                                                                                               |                     |     |     |      |
| BALL NUMBERS: AC7 / AD6 / AD7 / AD8                                               |                                                                                                                                                                                                                                                                                                               |                     |     |     |      |
| I2C STANDARD MODE / FAST MODE - VDDSHV0_WKUP = 1.8 V                              |                                                                                                                                                                                                                                                                                                               |                     |     |     |      |
| V <sub>IH</sub>                                                                   | High-level input threshold                                                                                                                                                                                                                                                                                    | 0.7 × VDDSHV0_WKUP  |     |     | V    |
| V <sub>IL</sub>                                                                   | Low-level input threshold                                                                                                                                                                                                                                                                                     | 0.3 × VDDSHV0_WKUP  |     |     | V    |
| V <sub>IHSS</sub>                                                                 | Input high-level Steady State <sup>(1)</sup>                                                                                                                                                                                                                                                                  | 0.70 × VDDSHV0_WKUP |     |     | V    |
| V <sub>ILSS</sub>                                                                 | Input low-level Steady State <sup>(2)</sup>                                                                                                                                                                                                                                                                   | 0.30 × VDDSHV0_WKUP |     |     | V    |
| V <sub>HYS</sub>                                                                  | Hysteresis                                                                                                                                                                                                                                                                                                    | 0.1 × VDDSHV0_WKUP  |     |     | V    |
| I <sub>IN</sub>                                                                   | Input leakage current. This value represents the maximum current flowing in or out of the pin while the output driver is disabled and the input is swept from VSS to VDD.                                                                                                                                     | 12                  |     |     | μA   |
| I <sub>OZ</sub>                                                                   | Total leakage current through the driver/receiver combination, which may include an internal pull-up or pull-down. This value represents the maximum current flowing in or out of the pin while the output driver is disabled, the pull-up or pull-down is inhibited, and the input is swept from VSS to VDD. | 12                  |     |     | μA   |
| V <sub>OL</sub>                                                                   | Low-level output voltage at 3-mA sink current                                                                                                                                                                                                                                                                 | 0.2 × VDDSHV0_WKUP  |     |     | V    |
| I2C STANDARD MODE / FAST MODE - VDDSHV0_WKUP = 3.3 V                              |                                                                                                                                                                                                                                                                                                               |                     |     |     |      |
| V <sub>IH</sub>                                                                   | High-level input voltage                                                                                                                                                                                                                                                                                      | 0.7 × VDDSHV0_WKUP  |     |     | V    |
| V <sub>IL</sub>                                                                   | Low-level input voltage                                                                                                                                                                                                                                                                                       | 0.3 × VDDSHV0_WKUP  |     |     | V    |
| V <sub>IHSS</sub>                                                                 | Input high-level Steady State <sup>(1)</sup>                                                                                                                                                                                                                                                                  | 0.70 × VDDSHV0_WKUP |     |     | V    |
| V <sub>ILSS</sub>                                                                 | Input low-level Steady State <sup>(2)</sup>                                                                                                                                                                                                                                                                   | 0.21 × VDDSHV0_WKUP |     |     | V    |
| V <sub>HYS</sub>                                                                  | Hysteresis                                                                                                                                                                                                                                                                                                    | 0.05 × VDDSHV0_WKUP |     |     | V    |
| I <sub>IN</sub>                                                                   | Input leakage current. This value represents the maximum current flowing in or out of the pin while the output driver is disabled and the input is swept from VSS to VDD.                                                                                                                                     | 80                  |     |     | μA   |

over recommended operating conditions (unless otherwise noted)

| PARAMETER       |                                                                                                                                                                                                                                                                                                               | MIN | TYP | MAX | UNIT |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| I <sub>OZ</sub> | Total leakage current through the driver/receiver combination, which may include an internal pull-up or pull-down. This value represents the maximum current flowing in or out of the pin while the output driver is disabled, the pull-up or pull-down is inhibited, and the input is swept from VSS to VDD. |     |     | 80  | μA   |
| V <sub>OL</sub> | Low-level output voltage at 3-mA sink current                                                                                                                                                                                                                                                                 |     |     | 0.4 | V    |

- (1) Voltage Input High Steady State (V<sub>IHSS</sub>) should be maintained when the signal is not transitioning.  
(2) Voltage Input Low Steady State (V<sub>ILSS</sub>) should be maintained when the signal is not transitioning.

## 6.6.2 Analog OSC Buffers DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER <sup>(1)</sup>           |                          | MIN                                    | TYP | MAX | UNIT |
|------------------------------------|--------------------------|----------------------------------------|-----|-----|------|
| BALL NAMES: OSC1_XI / WKUP_OSC0_XI |                          |                                        |     |     |      |
| BALL NUMBERS: C22 / AD5            |                          |                                        |     |     |      |
| HIGH FREQUENCY OSCILLATOR          |                          |                                        |     |     |      |
| V <sub>IH</sub>                    | High-level input voltage | 0.65 × VDD <sub>S</sub> <sup>(1)</sup> |     |     | V    |
| V <sub>IL</sub>                    | Low-level input voltage  | 0.35 × VDD <sub>S</sub> <sup>(1)</sup> |     |     | V    |
| BALL NAMES: WKUP_LFOSC0_XI         |                          |                                        |     |     |      |
| BALL NUMBERS: AE4                  |                          |                                        |     |     |      |
| LOW FREQUENCY OSCILLATOR           |                          |                                        |     |     |      |
| V <sub>IH</sub>                    | High-level input voltage | 0.65 × VDDA_WKUP                       |     |     | V    |
| V <sub>IL</sub>                    | Low-level input voltage  | 0.35 × VDDA_WKUP                       |     |     | V    |

- (1) VDD<sub>S</sub> stands for corresponding power supply. For WKUP\_OSC0\_XI, the corresponding power supply is VDDA\_WKUP. For OSC1\_XI, the corresponding power supply is VDD<sub>S</sub>\_OSC1.

### 6.6.3 Analog ADC DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER                                                                                                              | TEST CONDITIONS                   | MIN                                                                                                             | TYP                         | MAX                         | UNIT            |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------|-----------------------------------------------------------------------------------------------------------------|-----------------------------|-----------------------------|-----------------|
| <b>BALL NAMES in Mode 0:</b> MCU_ADC0_AIN[7:0] / MCU_ADC0_REFP/N / MCU_ADC1_AIN[7:0] / MCU_ADC1_REFP/N                 |                                   |                                                                                                                 |                             |                             |                 |
| <b>BALL NUMBERS:</b> F4 / F5 / G3 / G4 / G5 / G6 / H2 / H3 / H4 / H5 / J1 / J2 / J3 / J4 / J5 / J6 / K2 / K3 / K4 / K5 |                                   |                                                                                                                 |                             |                             |                 |
| <b>Analog Input</b>                                                                                                    |                                   |                                                                                                                 |                             |                             |                 |
| V <sub>MCU_ADC0/1_REFP</sub>                                                                                           | MCU_ADC0/1_REFP                   |                                                                                                                 | (0.5 × VDDA_ADC_MCU) + 0.25 | VDDA_ADC_MCU                | V               |
| V <sub>MCU_ADC0/1_REFN</sub>                                                                                           | MCU_ADC0/1_REFN                   |                                                                                                                 | 0                           | (0.5 × VDDA_ADC_MCU) - 0.25 | V               |
| V <sub>MCU_ADC0/1_REFP</sub> + V <sub>MCU_ADC0/1_REFN</sub>                                                            | MCU_ADC0/1_REFP + MCU_ADC0/1_REFN |                                                                                                                 |                             | VDDA_ADC_MCU                | V               |
| V <sub>MCU_ADC0/1_AIN[7:0]</sub>                                                                                       | Full-scale Input Range            |                                                                                                                 |                             | MCU_ADC0/1_REFN             | MCU_ADC0/1_REFP |
| DNL                                                                                                                    | Differential Non-Linearity        | MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS                                                        | -1                          | 0.5                         | 4               |
| INL                                                                                                                    | Integral Non-Linearity            | MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS                                                        |                             | ±1                          | ±4              |
| LSB <sub>GAIN-ERROR</sub>                                                                                              | Gain Error                        | MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS                                                        |                             | ±2                          |                 |
| LSB <sub>OFFSET-ERROR</sub>                                                                                            | Offset Error                      | MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS                                                        |                             | ±2                          |                 |
| C <sub>IN</sub>                                                                                                        | Input Sampling Capacitance        |                                                                                                                 |                             | 5.5                         | pF              |
| SNR                                                                                                                    | Signal-to-Noise Ratio             | Input Signal: 200 kHz sine wave at -0.5 dB Full Scale, MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS |                             | 70                          | dB              |
| THD                                                                                                                    | Total Harmonic Distortion         | Input Signal: 200 kHz sine wave at -0.5 dB Full Scale, MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS |                             | 75                          | dB              |

over recommended operating conditions (unless otherwise noted)

| PARAMETER                                               |                                                                        | TEST CONDITIONS                                                                                                 | MIN | TYP                                                               | MAX  | UNIT                   |
|---------------------------------------------------------|------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------|------|------------------------|
| SFDR                                                    | Spurious Free Dynamic Range                                            | Input Signal: 200 kHz sine wave at -0.5 dB Full Scale, MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS |     | 80                                                                |      | dB                     |
| SNR <sub>(PLUS)</sub>                                   | Signal-to-Noise Plus Distortion                                        | Input Signal: 200 kHz sine wave at -0.5 dB Full Scale, MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS |     | 69                                                                |      | dB                     |
| R <sub>static</sub> (MCU_ADC0/1_REFP, MCU_ADC0/1_REFN)  | Static Input Impedance of MCU_ADC0/1_REFP relative to MCU_ADC0/1_REFN  |                                                                                                                 |     | 2.2                                                               |      | kΩ                     |
| R <sub>dynamic</sub> (MCU_ADC0/1_REFP, MCU_ADC0/1_REFN) | Dynamic Input Impedance of MCU_ADC0/1_REFP relative to MCU_ADC0/1_REFN |                                                                                                                 |     | $[1/((65.97 \times 10^{-12}) \times f_{\text{SMPL\_CLK}})]^{(1)}$ |      | Ω                      |
| R <sub>MCU_ADC0/1_AIN[0:7]</sub>                        | Input Impedance of MCU_ADC0/1_AIN[7:0]                                 | f = input frequency                                                                                             |     | $[1/((65.97 \times 10^{-12}) \times f_{\text{SMPL\_CLK}})]$       |      | Ω                      |
| I <sub>IN</sub>                                         | ADC0 Input Leakage                                                     | MCU_ADC0_AIN[7:0] = VSS                                                                                         |     |                                                                   | -23  | μA                     |
|                                                         |                                                                        | MCU_ADC0_AIN[7:0] = VDDA_MCU_ADC0                                                                               |     |                                                                   | 27   | μA                     |
| I <sub>IN</sub>                                         | ADC1 Input Leakage                                                     | MCU_ADC1_AIN[7:0] = VSS                                                                                         |     |                                                                   | -126 | μA                     |
|                                                         |                                                                        | MCU_ADC1_AIN[7:0] = VDDA_MCU_ADC1                                                                               |     |                                                                   | 572  | μA                     |
| Sampling Dynamics                                       |                                                                        |                                                                                                                 |     |                                                                   |      |                        |
| F <sub>SMPL_CLK</sub>                                   | SMPL_CLK Frequency                                                     |                                                                                                                 |     | 60                                                                |      | MHz                    |
| t <sub>C</sub>                                          | Conversion Time                                                        |                                                                                                                 |     | 13                                                                |      | ADC0/1 SMPL_CLK Cycles |
| t <sub>ACQ</sub>                                        | Acquisition time                                                       |                                                                                                                 | 2   |                                                                   | 257  | ADC0/1 SMPL_CLK Cycles |
| T <sub>R</sub>                                          | Sampling Rate                                                          | ADC0/1 SMPL_CLK = 60 MHz                                                                                        |     |                                                                   | 4    | MSPS                   |
| CCISO                                                   | Channel to Channel Isolation                                           |                                                                                                                 |     | 100                                                               |      | dB                     |

- (1) The MCU\_ADC0/1\_REFP and MCU\_ADC0/1\_REFN source impedance should be  $\leq 1/10 \times (R_{\text{dynamic}}(\text{MCU\_ADC0/1\_REFP}, \text{MCU\_ADC0/1\_REFN}))$ . For example, for a 60 MHz clock, this source should be  $\leq 25 \Omega$  on each reference input.

### 6.6.4 DPHY CSI2 Buffers DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                                                                                                          |                                    | MIN | NOM | MAX | UNIT |
|----------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|-----|-----|-----|------|
| <b>BALL NAMES in Mode 0:</b> CSI0_RXN0 / CSI0_RXN3 / CSI0_RXN4 / CSI0_RXP0 / CSI0_RXP3 / CSI0_RXP4 / CSI0_RXN1 / CSI0_RXN2 / CSI0_RXP1 / CSI0_RXP2 |                                    |     |     |     |      |
| <b>BALL NUMBERS:</b> F24 / F26 / F28 / G24 / G25 / G26 / G27 / G28 / H25 / H27                                                                     |                                    |     |     |     |      |
| <b>Low-Power Receiver (LP-RX)</b>                                                                                                                  |                                    |     |     |     |      |
| V <sub>IH</sub>                                                                                                                                    | High-level input voltage           | 880 |     |     | mV   |
| V <sub>IL</sub>                                                                                                                                    | Low-level input voltage            |     |     | 550 | mV   |
| V <sub>HYS</sub>                                                                                                                                   | Hysteresis                         | 25  |     |     | mV   |
| <b>Ultra-Low Power Receiver (ULP-RX)</b>                                                                                                           |                                    |     |     |     |      |
| V <sub>ITH</sub>                                                                                                                                   | High-level input voltage           | 880 |     |     | mV   |
| V <sub>ITL-ULPM</sub>                                                                                                                              | Low-level input voltage            |     |     | 300 | mV   |
| V <sub>HYS</sub>                                                                                                                                   | Hysteresis                         | 25  |     |     | mV   |
| <b>High Speed Receiver (HS-RX)</b>                                                                                                                 |                                    |     |     |     |      |
| V <sub>IDTH</sub>                                                                                                                                  | Differential input high threshold  | 70  |     |     | mV   |
| V <sub>IDTL</sub>                                                                                                                                  | Differential input low threshold   |     |     | -70 | mV   |
| V <sub>IDMAX</sub>                                                                                                                                 | Maximum differential input voltage |     |     | 270 | mV   |
| V <sub>ILHS</sub>                                                                                                                                  | Single-ended input low voltage     | -40 |     |     | mV   |
| V <sub>IHHS</sub>                                                                                                                                  | Single-ended input high voltage    |     |     | 460 | mV   |
| V <sub>CMRXDC</sub>                                                                                                                                | Common-mode voltage                | 70  |     | 330 | mV   |

### 6.6.5 OLDI LVDS Buffers DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER                                                                                         |                                                                           | TEST CONDITIONS                               | MIN   | TYP  | MAX   | UNIT |
|---------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|-----------------------------------------------|-------|------|-------|------|
| <b>1.8-V MODE</b>                                                                                 |                                                                           |                                               |       |      |       |      |
| <b>BALL NAMES in Mode 0:</b> OLDI0_A0P/N / OLDI0_A1P/N / OLDI0_A2P/N / OLDI0_A3P/N / OLDI0_CLKP/N |                                                                           |                                               |       |      |       |      |
| <b>BALL NUMBERS:</b> J24 / J26 / J28 / K24 / K25 / K26 / K27 / K28 / L25 / L27                    |                                                                           |                                               |       |      |       |      |
| <b>OLDI LVDS TRANSMITTER</b>                                                                      |                                                                           |                                               |       |      |       |      |
| V <sub>OH</sub>                                                                                   | High Level Output Voltage                                                 | Differential Load = 100Ω                      |       | 1.3  | 1.6   | V    |
| V <sub>OL</sub>                                                                                   | Low Level Output Voltage                                                  |                                               | 0.9   | 1.01 |       | V    |
| V <sub>CM</sub>                                                                                   | Common Mode Voltage (OLDI)                                                |                                               | 1.125 | 1.25 | 1.375 | V    |
|                                                                                                   | Common Mode Voltage (sub-LVDS)                                            |                                               |       | 0.9  |       | V    |
| ΔV <sub>CM</sub>                                                                                  | Difference in Common Mode Output Voltage, between high/low steady-states  |                                               |       |      | 35    | mV   |
| V <sub>OD</sub>                                                                                   | Differential Output Voltage                                               | PAD/PADN = 0,<br>Differential Load = 100Ω     | 250   | 380  | 450   | mV   |
|                                                                                                   | Reduced Differential Output Voltage                                       |                                               | 100   | 200  | 300   | mV   |
| ΔV <sub>OD</sub>                                                                                  | Difference in Differential Output Voltage, between high/low steady states |                                               |       |      | 50    | mV   |
| I <sub>OS</sub>                                                                                   | Output Short Circuit Current                                              | PAD/PADN = 0,<br>Differential Load = 100Ω     |       |      | -5    | mA   |
| I <sub>OZ</sub>                                                                                   | Output Tri-State Current                                                  | PAD/PADN = 0/V <sub>DD</sub> S <sup>(1)</sup> | -10   | 4    | 40    | μA   |

- (1) V<sub>DD</sub>S stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see [Table 5-1, POWER \[9\]](#) column.

### 6.6.5.1 LVC MOS Buffers DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                               |                         | SPECIFIC BALL                                                                                           | MIN                                    | TYP | MAX | UNIT |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|---------------------------------------------------------------------------------------------------------|----------------------------------------|-----|-----|------|
| <b>BALL NAMES:</b> ALL LVC MOS IOs as defined in <a href="#">Table 5-1, Pin Attributes</a> except those listed in <a href="#">Section 6.6.5.1, LVC MOS Buffers DC Electrical Characteristics</a>   |                                                                                                                                                                                                                                                                                                               |                         |                                                                                                         |                                        |     |     |      |
| <b>BALL NUMBERS:</b> ALL LVC MOS IOs as defined in <a href="#">Table 5-1, Pin Attributes</a> except those listed in <a href="#">Section 6.6.5.1, LVC MOS Buffers DC Electrical Characteristics</a> |                                                                                                                                                                                                                                                                                                               |                         |                                                                                                         |                                        |     |     |      |
| <b>1.8-V MODE</b>                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                               |                         |                                                                                                         |                                        |     |     |      |
| V <sub>IH</sub>                                                                                                                                                                                    | Input high-level threshold                                                                                                                                                                                                                                                                                    |                         | TCK ( <a href="#">AA4</a> )                                                                             | 0.60 × VDD <sub>S</sub> <sup>(1)</sup> |     |     | V    |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               |                         | All other IOs                                                                                           | 0.65 × VDD <sub>S</sub> <sup>(1)</sup> |     |     |      |
| V <sub>IL</sub>                                                                                                                                                                                    | Input low-level threshold                                                                                                                                                                                                                                                                                     |                         | TCK ( <a href="#">AA4</a> )                                                                             | 0.30 × VDD <sub>S</sub> <sup>(1)</sup> |     |     | V    |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               |                         | All other IOs                                                                                           | 0.35 × VDD <sub>S</sub> <sup>(1)</sup> |     |     |      |
| V <sub>IHSS</sub>                                                                                                                                                                                  | Input high-level Steady State                                                                                                                                                                                                                                                                                 |                         |                                                                                                         | 0.75 × VDD <sub>S</sub> <sup>(1)</sup> |     |     | V    |
| V <sub>ILSS</sub>                                                                                                                                                                                  | Input low-level Steady State                                                                                                                                                                                                                                                                                  |                         |                                                                                                         | 0.35 × VDD <sub>S</sub> <sup>(1)</sup> |     |     | V    |
| V <sub>HYS</sub>                                                                                                                                                                                   | Input hysteresis voltage                                                                                                                                                                                                                                                                                      |                         | TCK ( <a href="#">AA4</a> )                                                                             | 400                                    |     |     | mV   |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               |                         | PORz ( <a href="#">E19</a> ),<br>MCU_PORz ( <a href="#">W5</a> ),<br>MCU_BYP_POR ( <a href="#">V5</a> ) | 50                                     |     |     |      |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               |                         | All other IOs                                                                                           | 100                                    |     |     |      |
| V <sub>OH</sub>                                                                                                                                                                                    | Output high-level threshold                                                                                                                                                                                                                                                                                   | I <sub>OH</sub> = 100μA |                                                                                                         | VDD <sub>S</sub> <sup>(1)</sup> - 0.1  |     |     | V    |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               | I <sub>OH</sub> = 2mA   |                                                                                                         | VDD <sub>S</sub> <sup>(1)</sup> - 0.2  |     |     |      |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               | I <sub>OH</sub> = 4mA   |                                                                                                         | VDD <sub>S</sub> <sup>(1)</sup> - 0.3  |     |     |      |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               | I <sub>OH</sub> = 6mA   |                                                                                                         | VDD <sub>S</sub> <sup>(1)</sup> - 0.4  |     |     |      |
| V <sub>OL</sub>                                                                                                                                                                                    | Output low-level threshold                                                                                                                                                                                                                                                                                    | I <sub>OL</sub> = 100μA |                                                                                                         | 0.1                                    |     |     | V    |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               | I <sub>OL</sub> = 2mA   |                                                                                                         | 0.2                                    |     |     |      |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               | I <sub>OL</sub> = 4mA   |                                                                                                         | 0.3                                    |     |     |      |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               | I <sub>OL</sub> = 6mA   |                                                                                                         | 0.4                                    |     |     |      |
| I <sub>IN</sub>                                                                                                                                                                                    | Input leakage current, pull-up or pull-down inhibited                                                                                                                                                                                                                                                         |                         |                                                                                                         | 11.5                                   |     |     | μA   |
|                                                                                                                                                                                                    | Input leakage current, pull-down enabled, V <sub>I</sub> = VDD <sub>S</sub> <sup>(1)</sup>                                                                                                                                                                                                                    |                         |                                                                                                         | 65                                     | 96  | 153 |      |
|                                                                                                                                                                                                    | Input leakage current, pull-up enabled, V <sub>I</sub> = VSS                                                                                                                                                                                                                                                  |                         |                                                                                                         | 64                                     | 97  | 154 |      |
| I <sub>OZ</sub>                                                                                                                                                                                    | Total leakage current through the driver/receiver combination, which may include an internal pull-up or pull-down. This value represents the maximum current flowing in or out of the pin while the output driver is disabled, the pull-up or pull-down is inhibited, and the input is swept from VSS to VDD. |                         |                                                                                                         | 11.5                                   |     |     | μA   |
| <b>3.3-V MODE</b>                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                               |                         |                                                                                                         |                                        |     |     |      |
| V <sub>IH</sub>                                                                                                                                                                                    | Input high-level threshold                                                                                                                                                                                                                                                                                    |                         | TCK ( <a href="#">AA4</a> )                                                                             | 2                                      |     |     | V    |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               |                         | MMC0_*, MMC1_*                                                                                          | 0.625 * VDDSHV <sub>n</sub>            |     |     |      |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               |                         | All other IOs                                                                                           | 2                                      |     |     |      |
| V <sub>IL</sub>                                                                                                                                                                                    | Input low-level threshold                                                                                                                                                                                                                                                                                     |                         | TCK ( <a href="#">AA4</a> )                                                                             | 0.7                                    |     |     | V    |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               |                         | MMC0_*, MMC1_*                                                                                          | 0.25 * VDDSHV <sub>n</sub>             |     |     |      |
|                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                               |                         | All other IOs                                                                                           | 0.8                                    |     |     |      |
| V <sub>IHSS</sub>                                                                                                                                                                                  | Input high-level Steady State                                                                                                                                                                                                                                                                                 |                         |                                                                                                         | 2.00                                   |     |     | V    |



over recommended operating conditions (unless otherwise noted)<sup>(1)</sup>

| PARAMETER         |                                                                                                                                                                                                                                                                                                               | SPECIFIC BALL                                     | MIN                         | TYP   | MAX  | UNIT |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|-----------------------------|-------|------|------|
| V <sub>ILSS</sub> | Input low-level Steady State                                                                                                                                                                                                                                                                                  |                                                   |                             |       | 0.75 | V    |
| V <sub>HYS</sub>  | Input hysteresis voltage                                                                                                                                                                                                                                                                                      | TCK (AA4)                                         | 400                         |       |      | mV   |
|                   |                                                                                                                                                                                                                                                                                                               | PORz (E19),<br>MCU_PORz (W5),<br>MCU_BYP_POR (V5) | 50                          |       |      |      |
|                   |                                                                                                                                                                                                                                                                                                               | All other IOs                                     | 100                         |       |      |      |
| V <sub>OH</sub>   | Output high-level threshold                                                                                                                                                                                                                                                                                   | I <sub>OH</sub> = 100μA                           | VDDSD <sup>(1)</sup> - 0.1  |       |      | V    |
|                   |                                                                                                                                                                                                                                                                                                               | I <sub>OH</sub> = 2mA                             | VDDSD <sup>(1)</sup> - 0.2  |       |      |      |
|                   |                                                                                                                                                                                                                                                                                                               | I <sub>OH</sub> = 4mA                             | VDDSD <sup>(1)</sup> - 0.3  |       |      |      |
|                   |                                                                                                                                                                                                                                                                                                               | I <sub>OH</sub> = 6mA                             | VDDSD <sup>(1)</sup> - 0.45 |       |      |      |
| V <sub>OL</sub>   | Output low-level threshold                                                                                                                                                                                                                                                                                    | I <sub>OL</sub> = 100μA                           |                             |       | 0.1  | V    |
|                   |                                                                                                                                                                                                                                                                                                               | I <sub>OL</sub> = 2mA                             |                             |       | 0.2  |      |
|                   |                                                                                                                                                                                                                                                                                                               | I <sub>OL</sub> = 4mA                             |                             |       | 0.3  |      |
|                   |                                                                                                                                                                                                                                                                                                               | I <sub>OL</sub> = 6mA                             |                             |       | 0.45 |      |
| I <sub>IN</sub>   | Input leakage current, pull-up or pull-down inhibited                                                                                                                                                                                                                                                         |                                                   |                             |       | 64   | μA   |
|                   | Input leakage current, pull-down enabled, V <sub>I</sub> = VDDSD <sup>(1)</sup>                                                                                                                                                                                                                               |                                                   | 67                          | 100.7 | 198  |      |
|                   | Input leakage current, pull-up enabled, V <sub>I</sub> = VSS                                                                                                                                                                                                                                                  |                                                   | 63                          | 100.3 | 160  |      |
| I <sub>OZ</sub>   | Total leakage current through the driver/receiver combination, which may include an internal pull-up or pull-down. This value represents the maximum current flowing in or out of the pin while the output driver is disabled, the pull-up or pull-down is inhibited, and the input is swept from VSS to VDD. |                                                   |                             |       | 64   | μA   |

(1) VDDSD stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see [Table 5-1, Pin Attributes](#), POWER [9] column.

### 6.6.6 USBHS Buffers DC Electrical Characteristics

#### Note

USB0 and USB1 Electrical Characteristics are compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

### 6.6.7 SERDES Buffers DC Electrical Characteristics

#### Note

The PCIe interfaces are compliant with the electrical parameters specified in PCI Express® Base Specification Revision 3.1.

#### Note

USB0 instance is compliant with the USB3.1 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the Universal Serial Bus 3.1 Specification, Revision 1.0, July 26, 2013.

## 6.7 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for High-Security Devices.

### 6.7.1 Recommended Operating Conditions for OTP eFuse Programming

over operating free-air temperature range (unless otherwise noted)

| PARAMETER <sup>(2)</sup> | DESCRIPTION                                                                         | MIN                             | NOM | MAX  | UNIT |
|--------------------------|-------------------------------------------------------------------------------------|---------------------------------|-----|------|------|
| VDD_MCU                  | Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)       | See <a href="#">Section 6.4</a> |     |      | V    |
| VPP_CORE                 | Supply voltage range for the eFuse ROM domain during normal operation               |                                 | NC  |      | V    |
|                          | Supply voltage range for the eFuse ROM domain during OTP programming <sup>(1)</sup> |                                 | NC  |      | V    |
| VPP_MCU                  | Supply voltage range for the eFuse ROM domain during normal operation               |                                 | NC  |      | V    |
|                          | Supply voltage range for the eFuse ROM domain during OTP programming <sup>(1)</sup> | 1.71                            | 1.8 | 1.89 | V    |
| I <sub>(VPP_MCU)</sub>   |                                                                                     |                                 |     | 100  | mA   |
| T <sub>j</sub>           | Temperature (junction)                                                              | 0                               | 25  | 85   | °C   |

(1) Supply voltage range includes DC errors and peak-to-peak noise. TI power management solutions [TLV70718](#) from the TLV707x family meet the supply voltage range needed for VPP\_MCU.

(2) NC stands for No Connect.

### 6.7.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP\_MCU power supply must be disabled when not programming OTP registers.
- The VPP\_MCU power supply must be ramped up after the proper device power-up sequence (for more details, see [Section 6.9.2, Power Supply Sequencing](#)).

### 6.7.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP\_MCU terminal during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP\_MCU terminal according to the specification in [Section 6.7.1](#).
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP\_MCU terminal.

### 6.7.4 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse.

CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

## 6.8 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the Device has to be at or below the  $T_J$  value identified in [Section 6.4, Recommended Operating Conditions](#).

### 6.8.1 Thermal Resistance Characteristics

It is recommended to perform thermal simulations at the system level with the worst case device power consumption

| NO. | NAME           | DESCRIPTION             | ACD<br>°C/W <sup>(1) (3)</sup> | AIR FLOW<br>(m/s) <sup>(2)</sup> |
|-----|----------------|-------------------------|--------------------------------|----------------------------------|
| T1  | $R\theta_{JC}$ | Junction-to-case        | 0.2                            | N/A                              |
| T2  | $R\theta_{JB}$ | Junction-to-board       | 3.1                            | N/A                              |
| T3  | $R\theta_{JA}$ | Junction-to-free air    | 12.8                           | 0                                |
| T4  |                | Junction-to-moving air  | 7.4                            | 1                                |
| T5  |                |                         | 6.5                            | 2                                |
| T6  |                |                         | 6                              | 3                                |
| T7  | $\Psi_{JT}$    | Junction-to-package top | 0.1                            | 0                                |
| T8  |                |                         | 0.1                            | 1                                |
| T9  |                |                         | 0.1                            | 2                                |
| T10 |                |                         | 0.1                            | 3                                |
| T11 | $\Psi_{JB}$    | Junction-to-board       | 2.9                            | 0                                |
| T12 |                |                         | 2.4                            | 1                                |
| T13 |                |                         | 2.3                            | 2                                |
| T14 |                |                         | 2.3                            | 3                                |

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [ $R\theta_{JC}$ ] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second.

(3) °C/W = degrees Celsius per watt.

## 6.9 Timing and Switching Characteristics

### Note

The Timing Requirements and Switching Characteristics values may change following the silicon characterization result.

### Note

The default SLEWRATE settings in each pad configuration register must be used to ensure timings, unless specific instructions are given otherwise.

### 6.9.1 Timing Parameters and Information

The timing parameter symbols used in [Section 6.9](#) are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in [Table 6-5](#):

**Table 6-5. Timing Parameters Subscripts**

| SYMBOL | PARAMETER                              |
|--------|----------------------------------------|
| c      | Cycle time (period)                    |
| d      | Delay time                             |
| dis    | Disable time                           |
| en     | Enable time                            |
| h      | Hold time                              |
| su     | Setup time                             |
| START  | Start bit                              |
| t      | Transition time                        |
| v      | Valid time                             |
| w      | Pulse duration (width)                 |
| X      | Unknown, changing, or don't care level |
| F      | Fall time                              |
| H      | High                                   |
| L      | Low                                    |
| R      | Rise time                              |
| V      | Valid                                  |
| IV     | Invalid                                |
| AE     | Active Edge                            |
| FE     | First Edge                             |
| LE     | Last Edge                              |
| Z      | High impedance                         |

## 6.9.2 Power Supply Sequencing

This section describes the power-up sequence required to ensure proper device operation. The power supply names described in this section comprise a superset of a family of compatible devices. Some members of this family will not include a subset of these power supplies and their associated device modules.

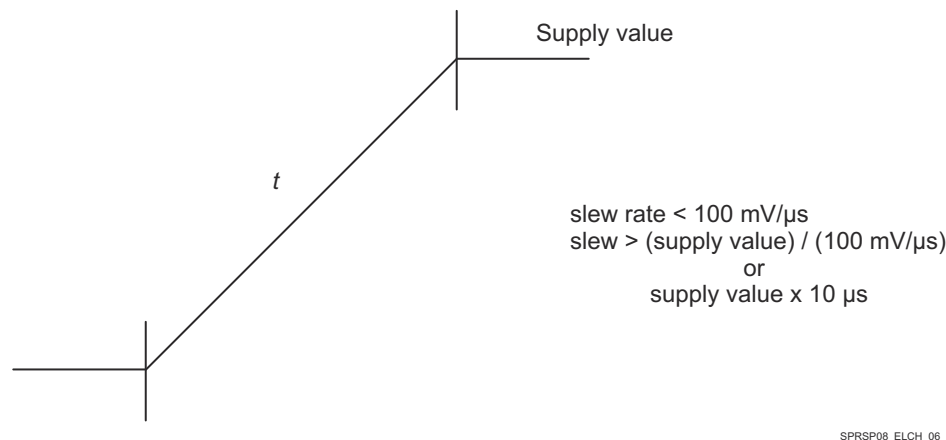
### Note

All timing requirements and switching characteristics in [Section 6.9.3](#) should be strictly followed unless otherwise specified.

### 6.9.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 100 mV/μs. For instance, as shown in [Figure 6-2](#), TI recommends having the supply ramp slew for a 1.8-V supply of more than 18 μs.

[Figure 6-2](#) describes the Power Supply Slew Rate Requirement of the device.



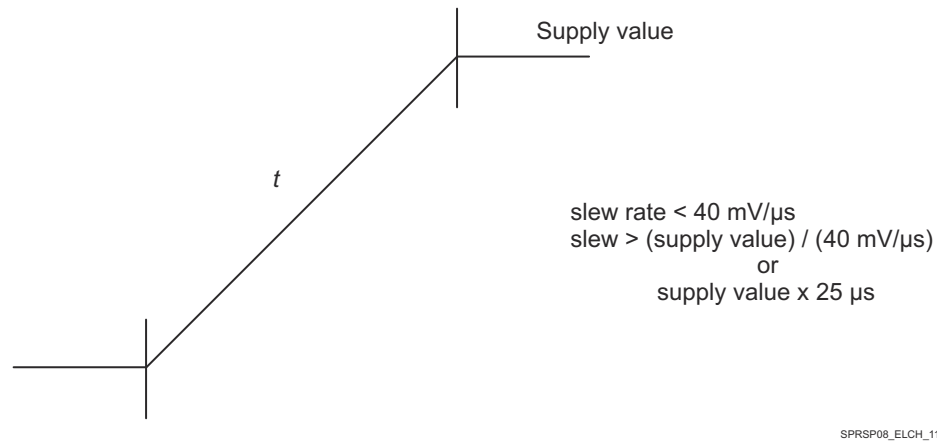
SPRSP08\_ELCH\_06

**Figure 6-2. Power Supply Slew and Slew Rate**

### 6.9.2.2 VDDA\_1P8\_SERDES0 Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of VDDA\_1P8\_SERDES0 supplies to be less than 40 mV/μs. For instance, as shown in [Figure 6-3](#), TI recommends having the supply ramp slew for a 1.8-V supply of more than 45 μs.

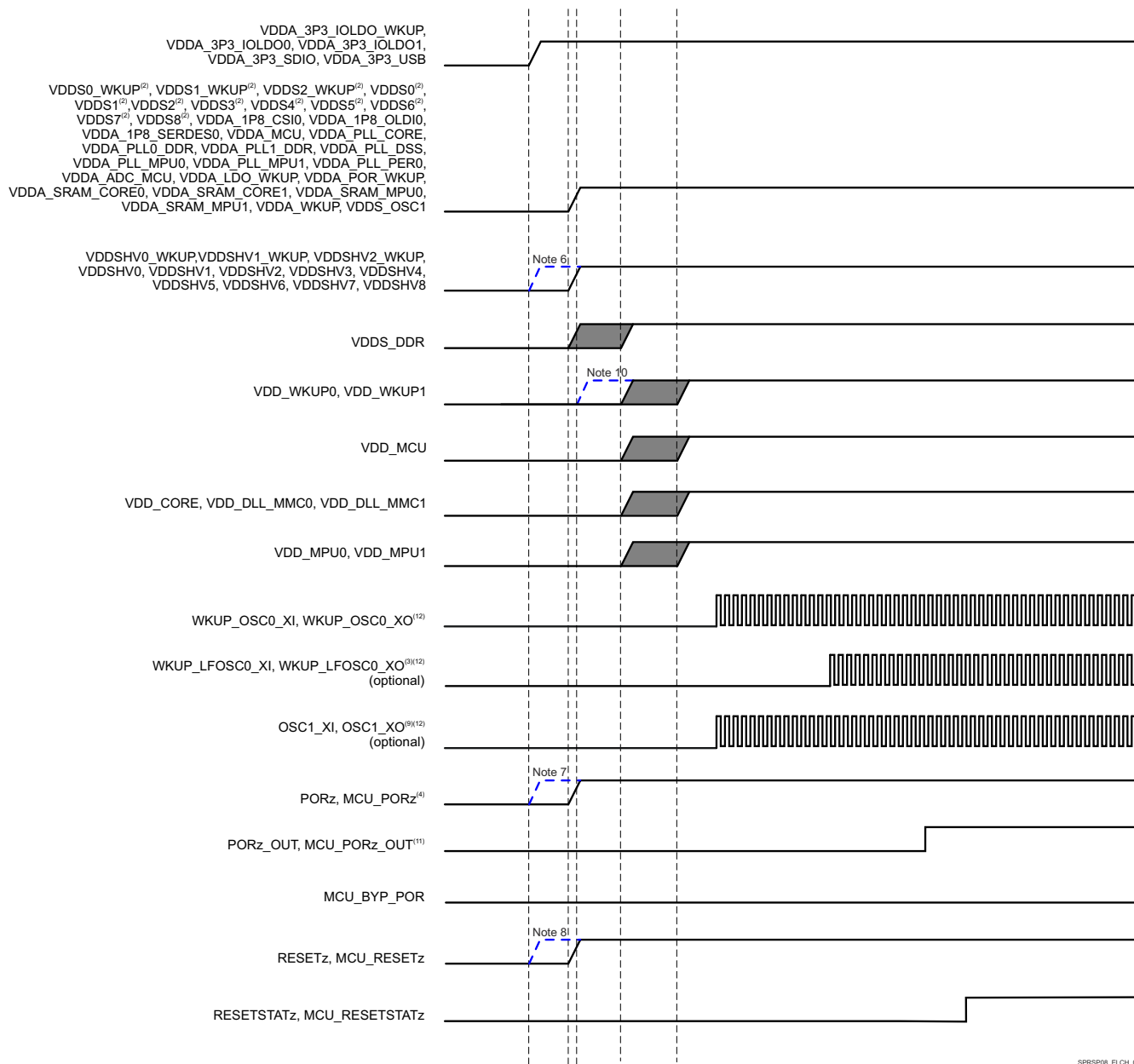
[Figure 6-3](#) describes the VDDA\_1P8\_SERDES0 Supply Slew Rate Requirement of the device.



**Figure 6-3. VDDA\_1P8\_SERDES0 Supply Slew and Slew Rate**

### 6.9.2.3 Power-Up Sequencing

Figure 6-4 describes the Power-Up Sequencing using On Chip Power-on-reset (POR) of the device.



**Figure 6-4. Power-Up Sequencing using On Chip Power-on-reset (POR)**

Figure 6-5 describes the Power-Up Sequencing using External Power-on-reset (POR), bypassing on-chip POR circuit of the device.



**Figure 6-5. Power-Up Sequencing using External Power-on-reset (POR), bypassing on-chip POR circuit**

#### 6.9.2.4 Power-Down Sequencing

A typical power down sequence is to have the Power-on-Reset asserted, clock shut down, and ramp down all the power supplies sequentially in the exact reverse order of the power-up sequencing. In other words, the power supply that has been ramped up first should be the last one that is ramped down.

For AM654x/AM652x, there are no specific power-down sequencing requirements, except for asserting Power-on-Reset before ramping down the rails while bypassing internal POR.



### 6.9.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

**Table 6-6. System Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.5 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 3   | 30  | pF   |

#### 6.9.3.1 Reset Electrical Data/Timing

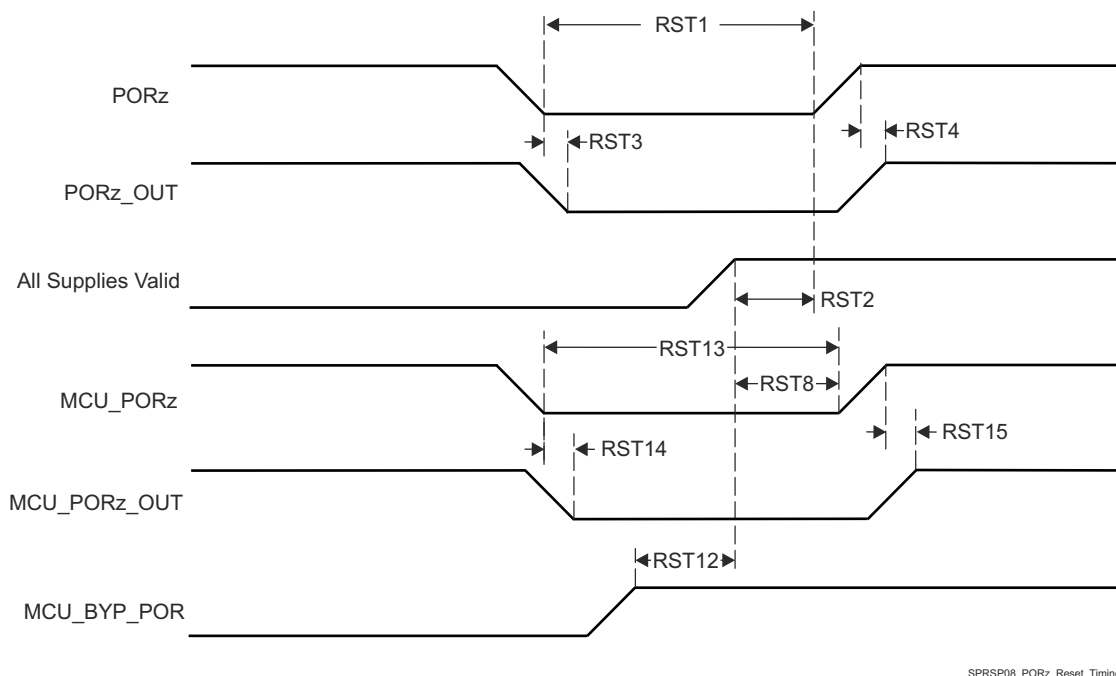
[Table 6-7](#), [Table 6-8](#), [Figure 6-6](#), [Figure 6-7](#), and [Figure 6-8](#) present the reset timing requirements and switching characteristics.

**Table 6-7. Reset Timing Requirements**

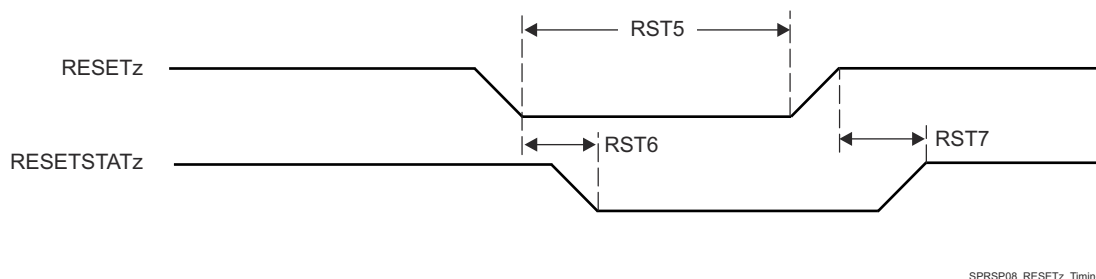
| NO.                    | PARAMETER                                  | DESCRIPTION                                                         | MIN     | MAX | UNIT |
|------------------------|--------------------------------------------|---------------------------------------------------------------------|---------|-----|------|
| <b>PORz Pin</b>        |                                            |                                                                     |         |     |      |
| RST1                   | t <sub>w</sub> (PORzL)                     | Pulse Width minimum, PORz low                                       | 2000    |     | ns   |
| RST2                   | t <sub>h</sub> (SUPPLIES VALID - PORz)     | Hold time, PORz active (low) after all supplies valid               | 2000000 |     | ns   |
| <b>RESETz Pin</b>      |                                            |                                                                     |         |     |      |
| RST5                   | t <sub>w</sub> (RESETzL)                   | Pulse Width minimum, RESETz low                                     | 400     |     | ns   |
| <b>MCU_PORz Pin</b>    |                                            |                                                                     |         |     |      |
| RST13                  | t <sub>w</sub> (MCU_PORzL)                 | Pulse Width minimum, MCU_PORz                                       | 2000    |     | ns   |
| RST8                   | t <sub>h</sub> (SUPPLIES VALID - MCU_PORz) | Hold time, MCU_PORz active (low) after all supplies valid           | 2000000 |     | ns   |
| <b>MCU_RESETz Pin</b>  |                                            |                                                                     |         |     |      |
| RST9                   | t <sub>w</sub> (MCU_RESETzL)               | Pulse Width minimum, MCU_RESETz                                     | 400     |     | ns   |
| <b>MCU_BYP_POR Pin</b> |                                            |                                                                     |         |     |      |
| RST12                  | t <sub>su</sub> (MCU_BYP_POR-MCU_PORz)     | Setup time, MCU_BYP_POR active (high) before all supplies are valid | 1000000 |     | ns   |

**Table 6-8. Reset Switching Characteristics**

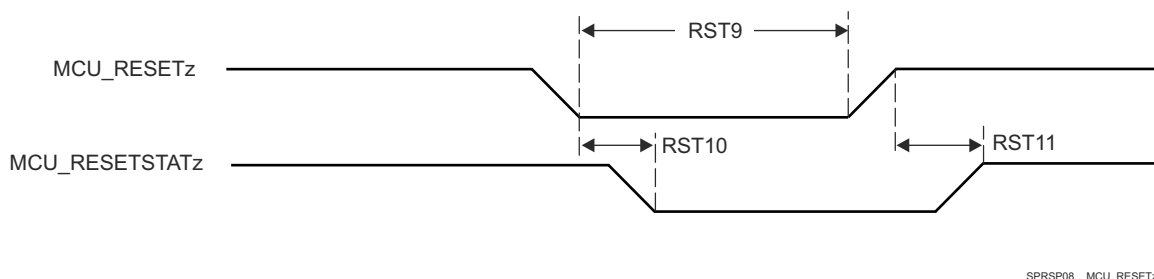
| NO.                       | PARAMETER                                       | DESCRIPTION                                                              | MIN    | MAX | UNIT |
|---------------------------|-------------------------------------------------|--------------------------------------------------------------------------|--------|-----|------|
| <b>PORz Pin</b>           |                                                 |                                                                          |        |     |      |
| RST3                      | t <sub>d</sub> (PORz-PORz_OUT low)              | Delay time, PORz active (low) to PORz_OUT active (low)                   | 0      |     | ns   |
| RST4                      | t <sub>d</sub> (PORz-PORz_OUT high)             | Delay time, PORz inactive (high) to PORz_OUT inactive (high)             | 0      |     | ns   |
| <b>RESETz Pin</b>         |                                                 |                                                                          |        |     |      |
| RST6                      | t <sub>d</sub> (RESETz-RESETSTATz low)          | Delay time, RESETz active (low) to RESETSTATz active (low)               | 4106   |     | ns   |
| RST7                      | t <sub>d</sub> (RESETz-RESETSTATz high)         | Delay time, RESETz inactive (high) to RESETSTATz inactive (high)         | 380000 |     | ns   |
| <b>MCU_RESETSTATz Pin</b> |                                                 |                                                                          |        |     |      |
| RST10                     | t <sub>d</sub> (MCU_RESETz-MCU_RESETSTATz low)  | Delay time, MCU_RESETz active (low) to MCU_RESETSTATz active (low)       | 4106   |     | ns   |
| RST11                     | t <sub>d</sub> (MCU_RESETz-MCU_RESETSTATz high) | Delay time, MCU_RESETz inactive (high) to MCU_RESETSTATz inactive (high) | 289000 |     | ns   |
| <b>MCU_PORz Pin</b>       |                                                 |                                                                          |        |     |      |
| RST14                     | t <sub>d</sub> (MCU_PORz-MCU_PORz_OUT low)      | Delay time, MCU_PORz active (low) to MCU_PORz_OUT active (low)           | 0      |     | ns   |
| RST15                     | t <sub>d</sub> (MCU_PORz-MCU_PORz_OUT high)     | Delay time, MCU_PORz inactive (high) to MCU_PORz_OUT inactive (high)     | 0      |     | ns   |



**Figure 6-6. PORz Reset Timing**



**Figure 6-7. RESETz and RESETSTATz Timing**



**Figure 6-8. MCU\_RESETz and MCU\_RESETSTATz Timing**

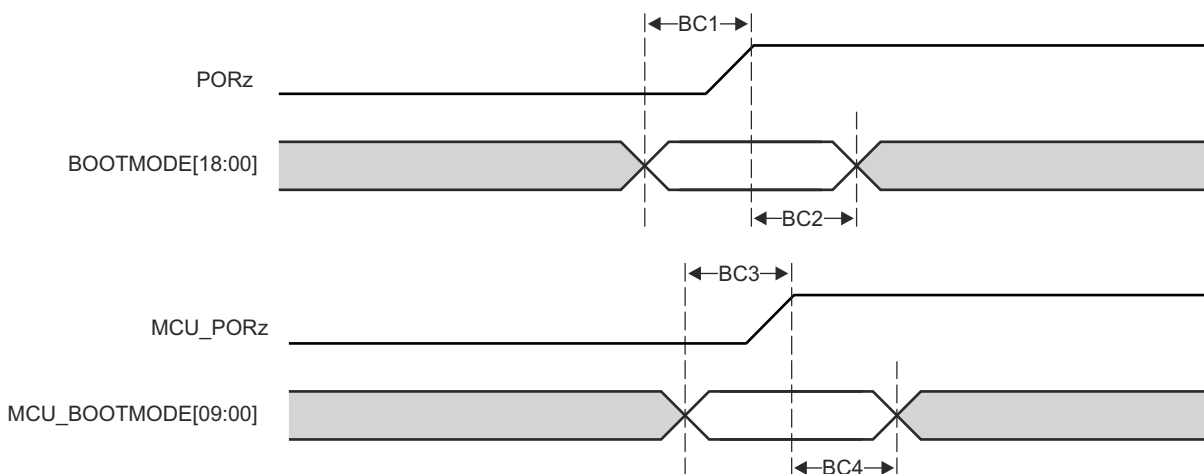
Table 6-9 and Figure 6-9 present the boot configuration timing requirements.

**Table 6-9. Boot Configuration Timing Requirements**

| NO. | PARAMETER                              |                                                                  | MIN  | MAX | UNIT |
|-----|----------------------------------------|------------------------------------------------------------------|------|-----|------|
| BC1 | $t_{su}(\text{BOOTMODE-PORz})$         | Setup time, All Bootmode pins active to PORz inactive (high)     | 2000 |     | ns   |
| BC2 | $t_h(\text{PORz - BOOTMODE})$          | Hold time, All Bootmode pins active after PORz inactive (high)   | 0    |     | ns   |
| BC3 | $t_{su}(\text{MCU_BOOTMODE-MCU_PORz})$ | Setup time, All Bootmode pins active to MCU_PORz inactive (high) | 2000 |     | ns   |

**Table 6-9. Boot Configuration Timing Requirements (continued)**

| NO. | PARAMETER                          |                                                                    | MIN | MAX | UNIT |
|-----|------------------------------------|--------------------------------------------------------------------|-----|-----|------|
| BC4 | $t_{h(MCU\_PORz - MCU\_BOOTMODE)}$ | Hold time, All Bootmode pins active after MCU_PORz inactive (high) | 0   |     | ns   |

**Figure 6-9. Boot Configuration Timing**

### 6.9.3.2 Safety Signal Timing

Tables and figures provided in this section define switching characteristics for MCU\_SAFETY\_ERRORn and SOC\_SAFETY\_ERRORn.

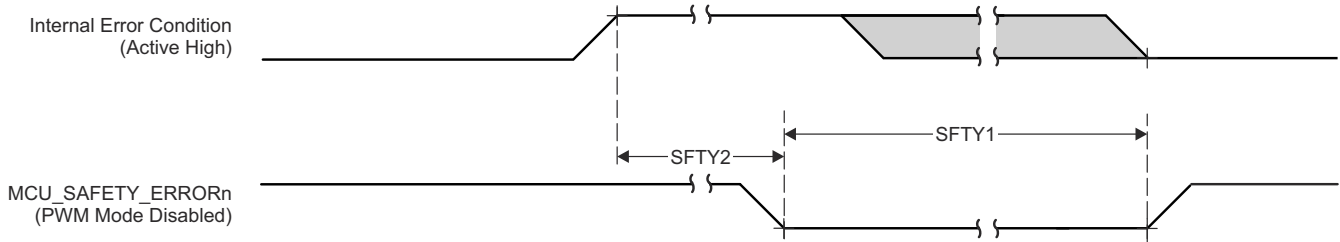
**Table 6-10. MCU\_SAFETY\_ERRORn Switching Characteristics**

see [Figure 6-10](#)

| NO.   | PARAMETER                                                                                                 | MIN                  | MAX | UNIT |
|-------|-----------------------------------------------------------------------------------------------------------|----------------------|-----|------|
| SFTY1 | $t_{w(MCU\_SAFETY\_ERRORn)}$<br>Pulse width, MCU_SAFETY_ERRORn active                                     | $P \cdot R^{(1)(2)}$ |     | ns   |
| SFTY2 | $t_{d(ERROR\_CONDITION-MCU\_SAFETY\_ERRORnL)}$<br>Delay time, ERROR CONDITION to MCU_SAFETY_ERRORn active | $50 \cdot P^{(1)}$   |     | ns   |

(1) P = ESM functional clock.

(2) R = Error Pin Counter Pre-Load Register count value.



**Figure 6-10. MCU\_SAFETY\_ERRORn Switching Characteristics**

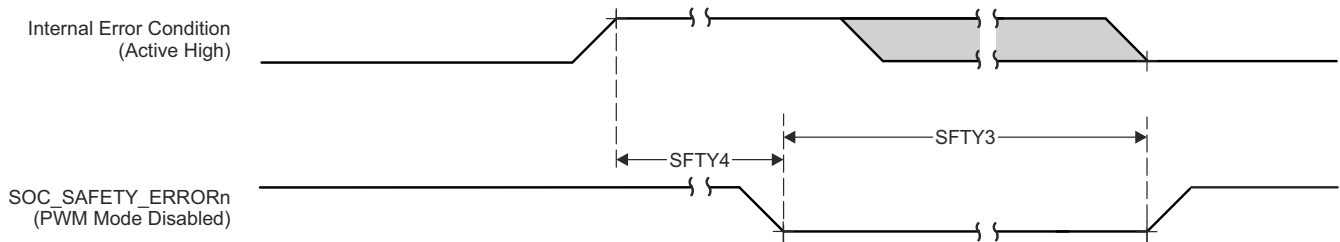
**Table 6-11. SOC\_SAFETY\_ERRORn Switching Characteristics**

see [Figure 6-11](#)

| NO.   | PARAMETER                                                                                                 | MIN                  | MAX | UNIT |
|-------|-----------------------------------------------------------------------------------------------------------|----------------------|-----|------|
| SFTY3 | $t_{w(SOC\_SAFETY\_ERRORn)}$<br>Pulse width, SOC_SAFETY_ERRORn active                                     | $P \cdot R^{(1)(2)}$ |     | ns   |
| SFTY4 | $t_{d(ERROR\_CONDITION-SOC\_SAFETY\_ERRORnL)}$<br>Delay time, ERROR CONDITION to SOC_SAFETY_ERRORn active | $50 \cdot P^{(1)}$   |     | ns   |

(1) P = ESM functional clock.

(2) R = Error Pin Counter Pre-Load Register count value.



**Figure 6-11. SOC\_SAFETY\_ERRORn Switching Characteristics**

### 6.9.3.3 Clock Timing

Tables and figures provided in this section define timing requirements and switching characteristics for clock signals.

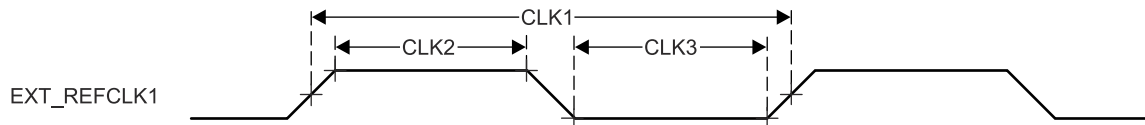
**Table 6-12. Clock Timing Requirements**

see [Figure 6-12](#)

| NO.   |                             |                                      | MIN            | MAX            | UNIT |
|-------|-----------------------------|--------------------------------------|----------------|----------------|------|
| CLK1  | $t_{c(EXT\_REFCLK1)}$       | Cycle time, EXT_REFCLK1              | 18.52          |                | ns   |
| CLK2  | $t_{w(EXT\_REFCLK1H)}$      | Pulse Duration, EXT_REFCLK1 high     | $E*0.45^{(1)}$ | $E*0.55^{(1)}$ | ns   |
| CLK3  | $t_{w(EXT\_REFCLK1L)}$      | Pulse Duration, EXT_REFCLK1 low      | $E*0.45^{(1)}$ | $E*0.55^{(1)}$ | ns   |
| CLK13 | $t_{c(MCU\_EXT\_REFCLK0)}$  | Cycle time, MCU_EXT_REFCLK0          | 18.52          |                | ns   |
| CLK14 | $t_{w(MCU\_EXT\_REFCLK0H)}$ | Pulse Duration, MCU_EXT_REFCLK0 high | $F*0.45^{(2)}$ | $F*0.55^{(2)}$ | ns   |
| CLK15 | $t_{w(MCU\_EXT\_REFCLK0L)}$ | Pulse Duration, MCU_EXT_REFCLK0 low  | $F*0.45^{(2)}$ | $F*0.55^{(2)}$ | ns   |

(1) E = EXT\_REFCLK1 cycle time.

(2) F = MCU\_EXT\_REFCLK0 cycle time.



**Figure 6-12. Clock Timing Requirements**

**Table 6-13. Clock Switching Characteristics**

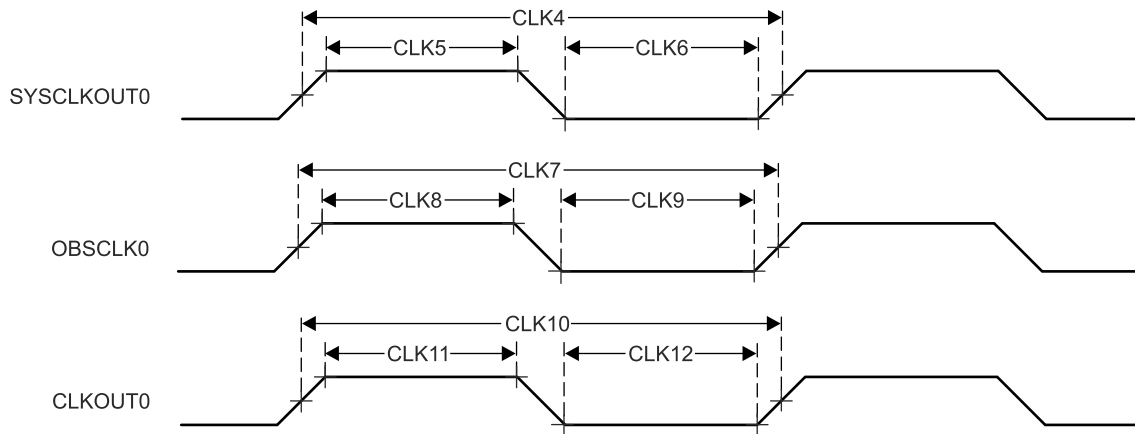
see [Figure 6-13](#)

| NO.   |                           | PARAMETER                                   | MIN            | MAX            | UNIT |
|-------|---------------------------|---------------------------------------------|----------------|----------------|------|
| CLK4  | $t_{c(SYSCLKOUT0)}$       | Cycle time minimum, SYSCLKOUT0              | 6              |                | ns   |
| CLK5  | $t_{w(SYSCLKOUT0H)}$      | Pulse Duration minimum, SYSCLKOUT0 high     | $A*0.4^{(1)}$  | $A*0.6^{(1)}$  | ns   |
| CLK6  | $t_{w(SYSCLKOUT0L)}$      | Pulse Duration minimum, SYSCLKOUT0 low      | $A*0.4^{(1)}$  | $A*0.6^{(1)}$  | ns   |
| CLK7  | $t_{c(OBSCLK0)}$          | Cycle time minimum, OBSCLK0                 | 5              |                | ns   |
| CLK8  | $t_{w(OBSCLK0H)}$         | Pulse Duration minimum, OBSCLK0 high        | $B*0.45^{(2)}$ | $B*0.55^{(2)}$ | ns   |
| CLK9  | $t_{w(OBSCLK0L)}$         | Pulse Duration minimum, OBSCLK0 low         | $B*0.45^{(2)}$ | $B*0.55^{(2)}$ | ns   |
| CLK10 | $t_{c(CLKOUT0)}$          | Cycle time minimum, MCU_CLKOUT0             | 20             | 40             | ns   |
| CLK11 | $t_{w(CLKOUT0H)}$         | Pulse Duration minimum, MCU_CLKOUT0 high    | $C*0.4^{(3)}$  | $C*0.6^{(3)}$  | ns   |
| CLK12 | $t_{w(CLKOUT0L)}$         | Pulse Duration minimum, MCU_CLKOUT0 low     | $C*0.4^{(3)}$  | $C*0.6^{(3)}$  | ns   |
| CLK16 | $t_{c(MCU\_SYSCLKOUT0)}$  | Cycle time minimum, MCU_SYSCLKOUT0          | 6              |                | ns   |
| CLK17 | $t_{w(MCU\_SYSCLKOUT0H)}$ | Pulse Duration minimum, MCU_SYSCLKOUT0 high | $A*0.4^{(1)}$  | $A*0.6^{(1)}$  | ns   |
| CLK18 | $t_{w(MCU\_SYSCLKOUT0L)}$ | Pulse Duration minimum, MCU_SYSCLKOUT0 low  | $A*0.4^{(1)}$  | $A*0.6^{(1)}$  | ns   |
| CLK19 | $t_{c(MCU\_OBSCLK0)}$     | Cycle time minimum, MCU_OBSCLK0             | 5              |                | ns   |
| CLK20 | $t_{w(MCU\_OBSCLK0H)}$    | Pulse Duration minimum, MCU_OBSCLK0 high    | $B*0.45^{(2)}$ | $B*0.55^{(2)}$ | ns   |
| CLK21 | $t_{w(MCU\_OBSCLK0L)}$    | Pulse Duration minimum, MCU_OBSCLK0 low     | $B*0.45^{(2)}$ | $B*0.55^{(2)}$ | ns   |

(1) A = SYSCLKOUT0 cycle time in MAIN domain; A = MCU\_SYSCLKOUT0 in MCU domain.

(2) B = OBSCLK0 cycle time in MAIN domain; B = MCU\_OBSCLK0 in MCU domain.

(3) C = MCU\_CLKOUT0 cycle time.



**Figure 6-13. Clock Switching Characteristics**

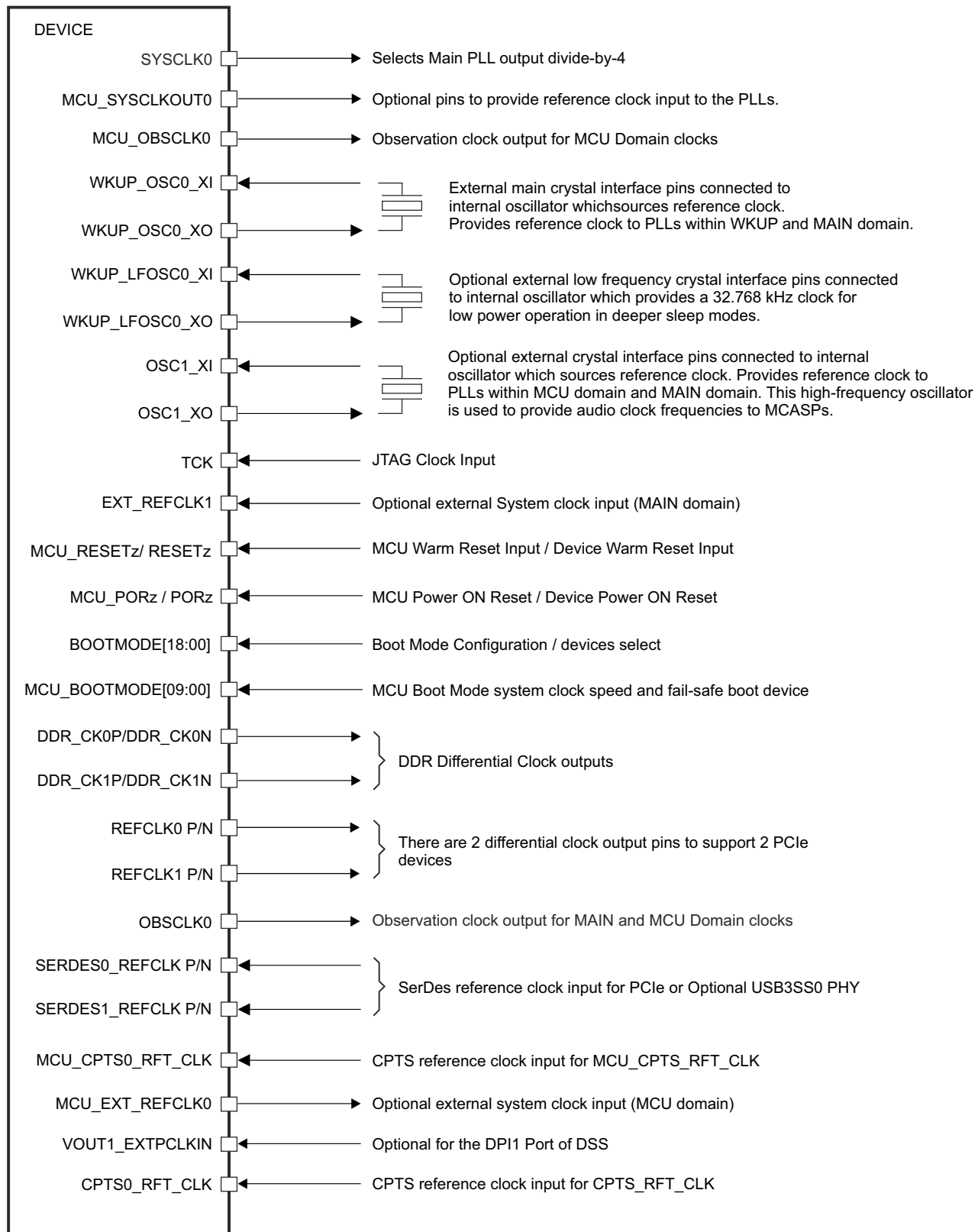
## 6.9.4 Clock Specifications

### 6.9.4.1 Input Clocks / Oscillators

Various external clock inputs are needed to drive the device. Summary of these input clock signals are:

- OSC1\_XO/OSC1\_XI — External main crystal interface pins connected to internal oscillator which sources reference clock and provides reference clock to PLLs within MAIN domain. Also, for audio applications, high-frequency oscillator 0 is used to provide audio clock frequencies to MCASPs.
- WKUP\_OSC0\_XO/WKUP\_OSC0\_XI — External main crystal interface pins connected to internal oscillator which sources reference clock and provides reference clock to PLLs within MCU domain and MAIN domain.
- WKUP\_LFOSC\_XO/WKUP\_LFOSC\_XI — External main crystal interface pins connected to internal oscillator which sources reference clock provides a clock for low power operation in deeper sleep modes.
- MCU\_EXT\_REFCLK0 — Optional external system clock input (MCU domain).
- EXT\_REFCLK1 — Optional external System clock input (MAIN domain). Optionally PLL2 (PER1) and MCASP can be sourced by EXT\_REFCLK1 (sourced externally).
- SERDES0\_REFCLK P/N and SERDES1\_REFCLK P/N — SerDes reference clock for PCIe or Optional USB3.0 PHY.
- MCU\_CPTS0\_RFT\_CLK — CPTS reference clock inputs for MCU\_CPTS0\_RFT\_CLK.
- CPTS\_RFT0\_CLK — CPTS reference clock inputs for CPTS0\_RFT\_CLK.
- VOUT1\_EXTCLKIN — Optional for the DPI1 Port of DSS.
- REFCLK0 P/N and REFCLK1 P/N — There are 2 differential clock output pins to support 2 PCIe devices.

Figure 6-14 shows the external input clock sources to peripherals.



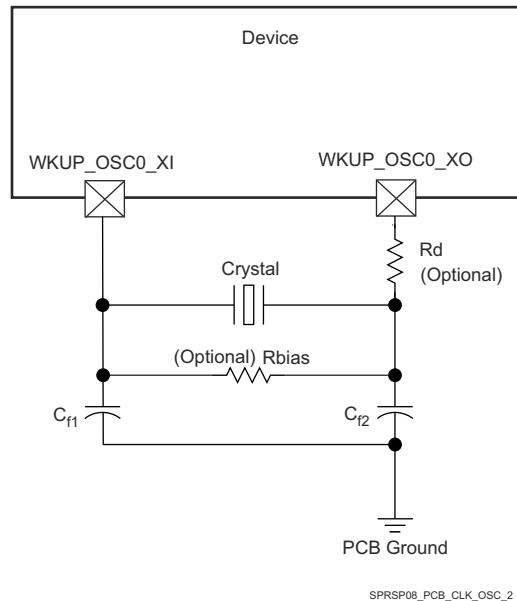
SPRSP08\_CLOCK\_01

**Figure 6-14. Input Clocks Interface**

For more information about Input clock interfaces, see the *Clocking* section in the device TRM.

#### 6.9.4.1.1 WKUP\_OSC0 Internal Oscillator Clock Source

Figure 6-15 shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors  $R_{bias}$  and  $R_d$  in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases,  $R_{bias}$  is not required and  $R_d$  is a 0-Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.



**Figure 6-15. WKUP\_OSC0 Crystal Implementation**

#### Note

The load capacitors,  $C_{f1}$  and  $C_{f2}$  in the load capacitance equation (1) below, should be chosen such that the below equation is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator WKUP\_OSC0\_XI, WKUP\_OSC0\_XO, and VSS pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})} \quad (1)$$

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-14 summarizes the required electrical constraints.



**Table 6-14. WKUP\_OSC0 Crystal Electrical Characteristics**

| NAME                                   | DESCRIPTION                                                                                            |                                |                                                  | MIN                      | TYP | MAX | UNIT     |
|----------------------------------------|--------------------------------------------------------------------------------------------------------|--------------------------------|--------------------------------------------------|--------------------------|-----|-----|----------|
| f <sub>p</sub>                         | Parallel resonance crystal frequency                                                                   |                                |                                                  | 19.2, 20, 24, 25, 26, 27 |     |     | MHz      |
| C <sub>f1</sub>                        | C <sub>f1</sub> load capacitance for crystal parallel resonance with C <sub>f1</sub> = C <sub>f2</sub> |                                |                                                  | 12                       |     |     | 24<br>pF |
| C <sub>f2</sub>                        | C <sub>f2</sub> load capacitance for crystal parallel resonance with C <sub>f1</sub> = C <sub>f2</sub> |                                |                                                  | 12                       |     |     | 24<br>pF |
| ESR(C <sub>f1</sub> ,C <sub>f2</sub> ) | Crystal ESR                                                                                            |                                |                                                  | 100                      |     |     | Ω        |
| C <sub>O</sub>                         | Crystal shunt capacitance                                                                              | ESR = 30 Ω<br>ESR = 40 Ω       | 19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz | 7                        |     |     | pF       |
|                                        |                                                                                                        |                                | ESR = 50 Ω                                       | 19.2 MHz, 20 MHz         | 7   |     |          |
|                                        |                                                                                                        | ESR = 60 Ω                     | 24 MHz, 25 MHz, 26 MHz, 27 MHz                   | 5                        |     |     | pF       |
|                                        |                                                                                                        |                                | 19.2 MHz, 20 MHz                                 | 7                        |     |     | pF       |
|                                        |                                                                                                        | ESR = 80 Ω                     | 24 MHz, 25 MHz, 26 MHz, 27 MHz                   | Not Supported            |     |     | -        |
|                                        |                                                                                                        |                                | 19.2 MHz, 20 MHz                                 | 5                        |     |     | pF       |
|                                        |                                                                                                        | ESR = 100 Ω                    | 24 MHz, 25 MHz, 26 MHz, 27 MHz                   | Not Supported            |     |     | -        |
|                                        |                                                                                                        |                                | 19.2 MHz, 20 MHz                                 | 3                        |     |     | pF       |
|                                        |                                                                                                        | 24 MHz, 25 MHz, 26 MHz, 27 MHz | Not Supported                                    |                          |     | -   |          |
|                                        |                                                                                                        |                                |                                                  |                          |     |     |          |
| L <sub>M</sub>                         | Crystal motional inductance for f <sub>p</sub> = 20 MHz                                                |                                |                                                  | 10.16                    |     |     | mH       |
| C <sub>M</sub>                         | Crystal motional capacitance                                                                           |                                |                                                  | 3.42                     |     |     | fF       |
| f <sub>j</sub> (WKUP_OSC0_XI)          | Frequency accuracy, WKUP_OSC0_XI                                                                       |                                | Ethernet RGMII and RMII not used                 | ±100                     |     |     | ppm      |
|                                        |                                                                                                        |                                | Ethernet RGMII and RMII using derived clock      | ±50                      |     |     |          |

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

Table 6-15 details the switching characteristics of the oscillator and the requirements of the input clock.

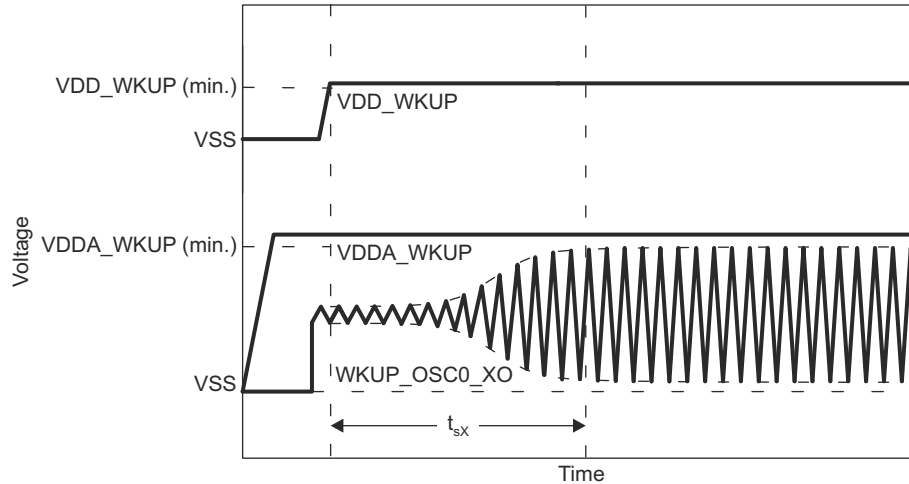
**Table 6-15. WKUP\_OSC0 Switching Characteristics – Crystal Mode**

| NAME     | DESCRIPTION           | MIN                      | TYP | MAX | UNIT |
|----------|-----------------------|--------------------------|-----|-----|------|
| $f_p$    | Oscillation frequency | 19.2, 20, 24, 25, 26, 27 |     |     | MHz  |
| $t_{sX}$ | Start-up time         | $2^{(1)}$                |     |     | ms   |

(1) In order to meet the start-up time defined in this table, the crystal needs to be selected according to the following equation:

$$T_{su} = K \times L_m / (R_o - ESR) + \Delta t$$

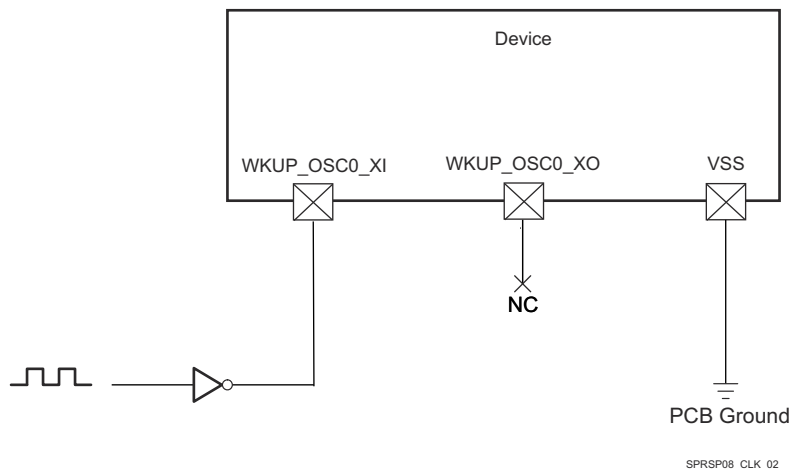
where  $L_m$  is crystal motional inductance,  $R_o$  is the negative resistance of amplifier, ESR is the crystal Effective series resistance and K is a constant which represents the initial conditions.  $\Delta t$  is the time amplifier takes to reach its bias point after power down is released.



**Figure 6-16. WKUP\_OSC0 Start-up Time**

#### 6.9.4.1.2 WKUP\_OSC0 LVC MOS Digital Clock Source

Figure 6-17 shows the recommended oscillator connections when WKUP\_OSC0 is connected to an LVC MOS square-wave digital clock source. The 1.8-V LVC MOS-Compatible clock source is connected to the WKUP\_OSC0\_XI pin. In this mode of operation, the WKUP\_OSC0\_XO pin is left unconnected and should not be used to source any external components.



**Figure 6-17. 1.8-V LVC MOS-Compatible Clock Input**

Table 6-16 summarizes the WKUP\_OSC0 input clock electrical characteristics

**Table 6-16. WKUP\_OSC0 Switching Characteristics – Crystal Mode**

| NAME            | DESCRIPTION               | MIN                      | TYP   | MAX   | UNIT |
|-----------------|---------------------------|--------------------------|-------|-------|------|
| f               | Frequency                 | 19.2, 20, 24, 25, 26, 27 |       |       | MHz  |
| C <sub>IN</sub> | Input capacitance         | 2.184                    | 2.384 | 2.584 | pF   |
| I <sub>IN</sub> | Input current (3.3V mode) | 4                        | 6     | 10    | μA   |

Table 6-17 details the WKUP\_OSC0 input clock timing requirements.

**Table 6-17. WKUP\_OSC0 Input Clock Timing Requirements**

| NAME | DESCRIPTION                                               | MIN                      | TYP | MAX | UNIT |
|------|-----------------------------------------------------------|--------------------------|-----|-----|------|
| CK0  | 1 / t <sub>c</sub> (WKUP_OSC0_XI) Frequency, WKUP_OSC0_XI | 19.2, 20, 24, 25, 26, 27 |     |     | MHz  |

**Table 6-17. WKUP\_OSC0 Input Clock Timing Requirements (continued)**

| NAME | DESCRIPTION             |                                          | MIN                                         | TYP | MAX                                 | UNIT |
|------|-------------------------|------------------------------------------|---------------------------------------------|-----|-------------------------------------|------|
| CK1  | $t_{W(WKUP\_OSC0\_XI)}$ | Pulse duration, WKUP_OSC0_XI low or high | $0.45 \times t_{c(WKUP\_OSC0\_XI)}$         |     | $0.55 \times t_{c(WKUP\_OSC0\_XI)}$ | ns   |
|      | $t_{j(WKUP\_OSC0\_XI)}$ | Period jitter, WKUP_OSC0_XI              |                                             |     | $0.01 \times t_{c(WKUP\_OSC0\_XI)}$ | ns   |
|      | $t_{R(WKUP\_OSC0\_XI)}$ | Rise time, WKUP_OSC0_XI                  |                                             |     | 5                                   | ns   |
|      | $t_{F(WKUP\_OSC0\_XI)}$ | Fall time, WKUP_OSC0_XI                  |                                             |     | 5                                   | ns   |
|      | $t_{j(WKUP\_OSC0\_XI)}$ | Frequency accuracy, WKUP_OSC0_XI         | Ethernet RGMII and RMII not used            |     | $\pm 100$                           | ppm  |
|      |                         |                                          | Ethernet RGMII and RMII using derived clock |     | $\pm 50$                            |      |

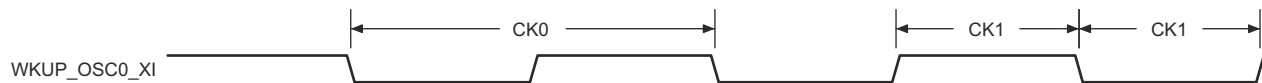
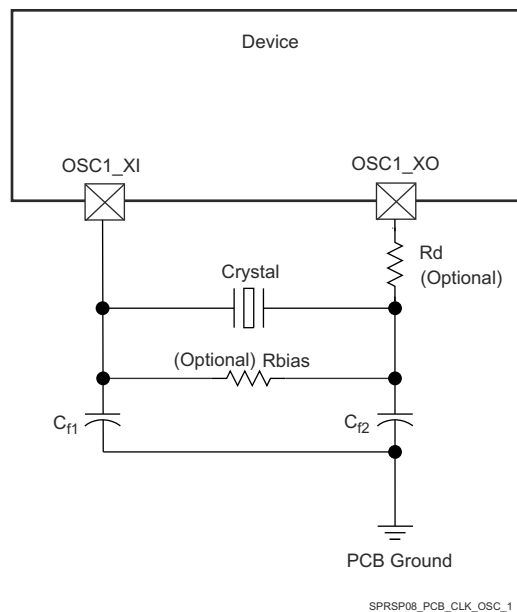
**Figure 6-18. WKUP\_OSC0\_XI Input Clock****6.9.4.1.3 Auxiliary OSC1 Internal Oscillator Clock Source**

Figure 6-19 shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors  $R_{bias}$  and  $R_d$  in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases,  $R_{bias}$  is not required and  $R_d$  is a 0- $\Omega$  resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

**Figure 6-19. OSC1 Crystal Implementation****Note**

The load capacitors,  $C_{f1}$  and  $C_{f2}$  in Figure 6-20, should be chosen such that the below equation is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator OSC1\_XI, OSC1\_XO, and VSS pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

SPRSP52C\_CLOCK\_01

**Figure 6-20. Load Capacitance Equation**

The crystal must be in the fundamental mode of operation and parallel resonant. [Table 6-18](#) summarizes the required electrical constraints.

**Table 6-18. OSC1 Crystal Electrical Characteristics**

| NAME                                   | DESCRIPTION                                                                                            |                                |                                                  | MIN                      | TYP | MAX | UNIT     |
|----------------------------------------|--------------------------------------------------------------------------------------------------------|--------------------------------|--------------------------------------------------|--------------------------|-----|-----|----------|
| f <sub>p</sub>                         | Parallel resonance crystal frequency                                                                   |                                |                                                  | 19.2, 20, 24, 25, 26, 27 |     |     | MHz      |
| C <sub>f1</sub>                        | C <sub>f1</sub> load capacitance for crystal parallel resonance with C <sub>f1</sub> = C <sub>f2</sub> |                                |                                                  | 12                       |     |     | 24<br>pF |
| C <sub>f2</sub>                        | C <sub>f2</sub> load capacitance for crystal parallel resonance with C <sub>f1</sub> = C <sub>f2</sub> |                                |                                                  | 12                       |     |     | 24<br>pF |
| ESR(C <sub>f1</sub> ,C <sub>f2</sub> ) | Crystal ESR                                                                                            |                                |                                                  | 100                      |     |     | Ω        |
| C <sub>O</sub>                         | Crystal shunt capacitance                                                                              | ESR = 30 Ω<br>ESR = 40 Ω       | 19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz | 7                        |     |     | pF       |
|                                        |                                                                                                        |                                | ESR = 50 Ω                                       | 19.2 MHz, 20 MHz         | 7   |     |          |
|                                        |                                                                                                        | 24 MHz, 25 MHz, 26 MHz, 27 MHz |                                                  | 5                        |     |     | pF       |
|                                        |                                                                                                        | ESR = 60 Ω                     | 19.2 MHz, 20 MHz                                 | 7                        |     |     | pF       |
|                                        |                                                                                                        |                                | 24 MHz, 25 MHz, 26 MHz, 27 MHz                   | Not Supported            |     |     | -        |
|                                        |                                                                                                        | ESR = 80 Ω                     | 19.2 MHz, 20 MHz                                 | 5                        |     |     | pF       |
|                                        |                                                                                                        |                                | 24 MHz, 25 MHz, 26 MHz, 27 MHz                   | Not Supported            |     |     | -        |
|                                        |                                                                                                        | ESR = 100 Ω                    | 19.2 MHz, 20 MHz                                 | 3                        |     |     | pF       |
| 24 MHz, 25 MHz, 26 MHz, 27 MHz         | Not Supported                                                                                          |                                |                                                  | -                        |     |     |          |
| L <sub>M</sub>                         | Crystal motional inductance for f <sub>p</sub> = 20 MHz                                                |                                |                                                  | 10.16                    |     |     | mH       |
| C <sub>M</sub>                         | Crystal motional capacitance                                                                           |                                |                                                  | 3.42                     |     |     | fF       |
| f <sub>j</sub> (OSC1_X1)               | Frequency accuracy, OSC1_X1                                                                            |                                | Ethernet RGMII and RMII not used                 | ±100                     |     |     | ppm      |
|                                        |                                                                                                        |                                | Ethernet RGMII and RMII using derived clock      | ±50                      |     |     |          |

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

[Table 6-19](#) details the switching characteristics of the oscillator and the requirements of the input clock.

**Table 6-19. OSC1 Switching Characteristics – Crystal Mode**

| NAME            | DESCRIPTION           | MIN                      | TYP | MAX | UNIT |
|-----------------|-----------------------|--------------------------|-----|-----|------|
| f <sub>p</sub>  | Oscillation frequency | 19.2, 20, 24, 25, 26, 27 |     |     | MHz  |
| t <sub>sX</sub> | Start-up time         | 2 <sup>(1)</sup>         |     |     | ms   |

- (1) In order to meet the start-up time defined in this table, the crystal needs to be selected according to the following equation:  
 $T_{su} = K \times L_m / (R_o - ESR) + \Delta t$   
 where L<sub>m</sub> is crystal motional inductance, R<sub>O</sub> is the negative resistance of amplifier, ESR is the crystal Effective series resistance and K is a constant which represents the initial conditions. Δt is the time amplifier takes to reach its bias point after power down is released.

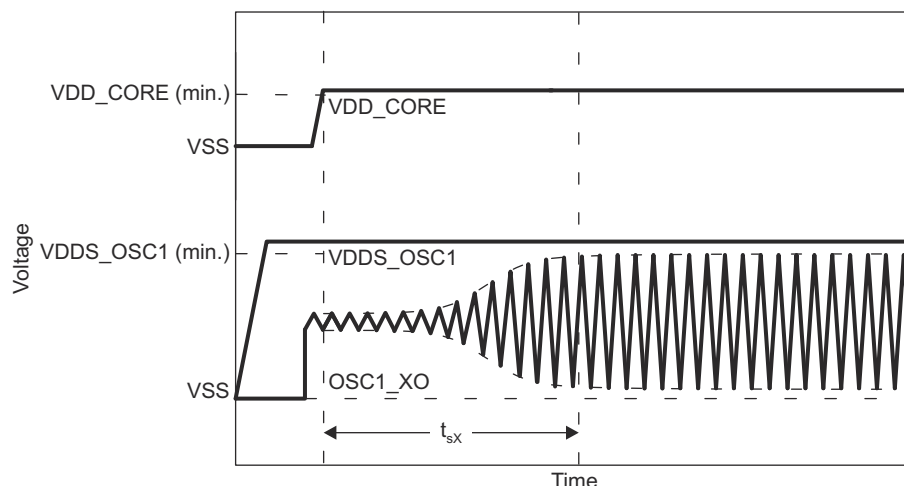


Figure 6-21. OSC1 Start-up Time

#### 6.9.4.1.4 Auxiliary OSC1 LVCMOS Digital Clock Source

Figure 6-22 shows the recommended oscillator connections when OSC1 is connected to an LVCMOS square-wave digital clock source. The 1.8-V LVCMOS-Compatible clock source is connected to the OSC1\_XI pin. In this mode of operation, the OSC1\_XO pin is left unconnected and should not be used to source any external components.

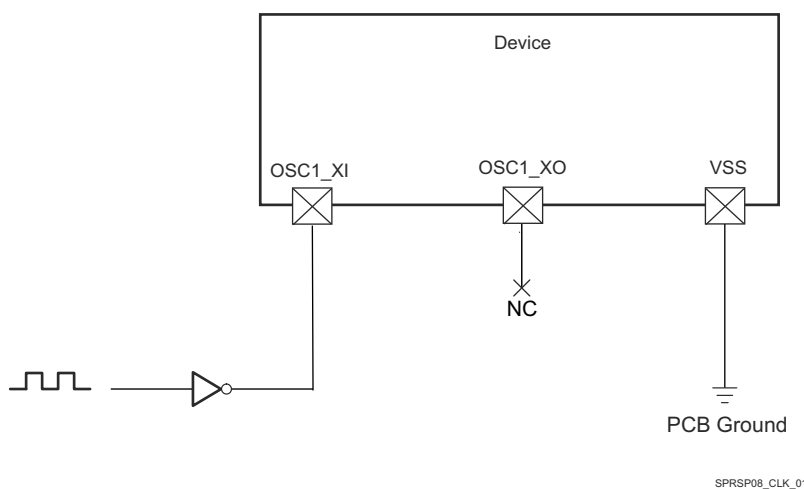


Figure 6-22. 1.8-V LVCMOS-Compatible Clock Input

Table 6-20 summarizes the OSC1 input clock electrical characteristics.

Table 6-20. OSC1 Switching Characteristics – Crystal Mode

| NAME            | DESCRIPTION               | MIN                      | TYP   | MAX   | UNIT |
|-----------------|---------------------------|--------------------------|-------|-------|------|
| f               | Frequency                 | 19.2, 20, 24, 25, 26, 27 |       |       | MHz  |
| C <sub>IN</sub> | Input capacitance         | 2.184                    | 2.384 | 2.584 | pF   |
| I <sub>IN</sub> | Input current (3.3V mode) | 4                        | 6     | 10    | μA   |

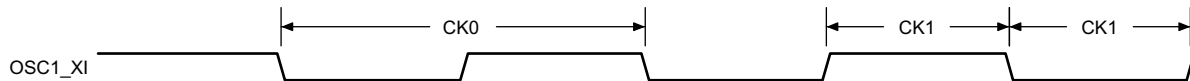
Table 6-21 details the OSC1 input clock timing requirements.

Table 6-21. OSC1 Input Clock Timing Requirements

| NAME | DESCRIPTION                                     | MIN                      | TYP | MAX | UNIT |
|------|-------------------------------------------------|--------------------------|-----|-----|------|
| CK0  | 1 / t <sub>c</sub> (OSC1_XI) Frequency, OSC1_XI | 19.2, 20, 24, 25, 26, 27 |     |     | MHz  |

**Table 6-21. OSC1 Input Clock Timing Requirements (continued)**

| NAME | DESCRIPTION       |                                     | MIN                                         | TYP | MAX                           | UNIT |
|------|-------------------|-------------------------------------|---------------------------------------------|-----|-------------------------------|------|
| CK1  | $t_{w(OSC1\_XI)}$ | Pulse duration, OSC1_XI low or high | $0.45 \times t_{c(OSC1\_XI)}$               |     | $0.55 \times t_{c(OSC1\_XI)}$ | ns   |
|      | $t_{j(OSC1\_XI)}$ | Period jitter, OSC1_XI              |                                             |     | $0.01 \times t_{c(OSC1\_XI)}$ | ns   |
|      | $t_{R(OSC1\_XI)}$ | Rise time, OSC1_XI                  |                                             |     | 5                             | ns   |
|      | $t_{F(OSC1\_XI)}$ | Fall time, OSC1_XI                  |                                             |     | 5                             | ns   |
|      | $t_{j(OSC1\_XI)}$ | Frequency accuracy, OSC1_XI         | Ethernet RGMII and RMII not used            |     | $\pm 100$                     | ppm  |
|      |                   |                                     | Ethernet RGMII and RMII using derived clock |     | $\pm 50$                      |      |



**Figure 6-23. OSC1\_XI Input Clock**

#### 6.9.4.1.5 Auxiliary OSC1 Not Used

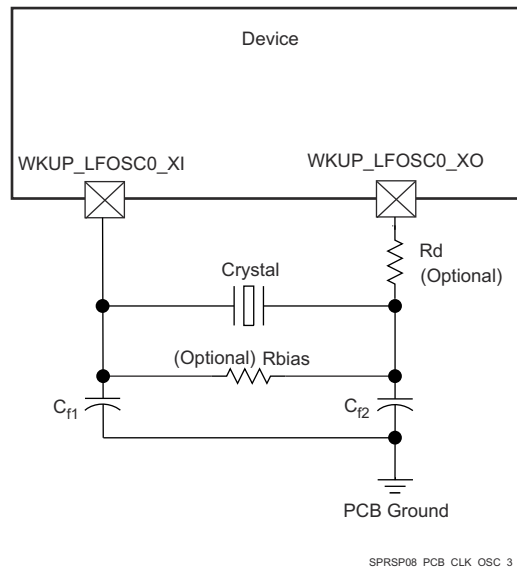
For more Information see [Section 5.5, Connections for Unused Pins](#).

#### 6.9.4.1.6 WKUP\_LFOSC0 Internal Oscillator Clock Source

##### Note

WKUP\_LFOSC\_XO/WKUP\_LFOSC\_XI - External main crystal interface pins connected to internal oscillator which sources reference clock provides a clock for low power operation in deeper sleep modes. For a list of supported low power modes for this device, please refer to *Overview of Device Low-Power Modes* section in the device TRM.

[Figure 6-24](#) shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors  $R_{bias}$  and  $R_d$  in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases,  $R_{bias}$  is not required and  $R_d$  is a 0 ohm resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.



**Figure 6-24. WKUP\_LFOSC0 Crystal Implementation**

**Note**

The load capacitors,  $C_{f1}$  and  $C_{f2}$  in [Figure 6-25](#), should be chosen such that the below equation is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator WKUP\_LFOSC0\_XI, WKUP\_LFOSC0\_XO, and VSS pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

SPRSP52C\_0000\_03

**Figure 6-25. Load Capacitance Equation**

The crystal must be in the fundamental mode of operation and parallel resonant. [Table 6-22](#) summarizes the required electrical constraints

**Table 6-22. WKUP\_LFOSC0 Crystal Electrical Characteristics**

| NAME        | DESCRIPTION                                                                     | MIN | TYP   | MAX  | UNIT |
|-------------|---------------------------------------------------------------------------------|-----|-------|------|------|
| $f_p$       | Parallel resonance crystal frequency                                            |     | 32768 |      | Hz   |
| $C_{f1}$    | $C_{f1}$ load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | 12  |       | 24   | pF   |
| $C_{f2}$    | $C_{f2}$ load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$ | 12  |       | 24   | pF   |
| $C_{shunt}$ | Shunt capacitance                                                               |     |       | 1.35 | pF   |
| ESR         | Crystal effective series resistance                                             |     |       | 65   | kΩ   |

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

[Table 6-23](#) details the switching characteristics of the oscillator and the requirements of the input clock.

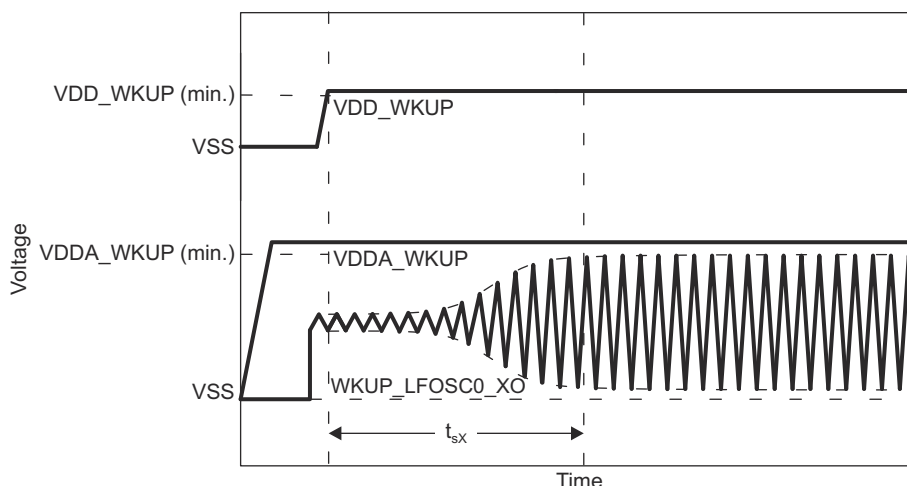
**Table 6-23. WKUP\_LFOSC0 Switching Characteristics – Crystal Mode**

| NAME       | DESCRIPTION           | MIN | TYP   | MAX | UNIT |
|------------|-----------------------|-----|-------|-----|------|
| $f_{xtal}$ | Oscillation frequency |     | 32768 |     | Hz   |
| $t_{SX}$   | Start-up time         |     |       | (1) | s    |

- (1) In order to meet the start-up time defined in this table, the crystal needs to be selected according to the following equation:

$$T_{su} = K \times L_m / (R_o - ESR) + \Delta t$$

where  $L_m$  is crystal motional inductance,  $R_o$  is the negative resistance of amplifier, ESR is the crystal Effective series resistance and  $K$  is a constant which represents the initial conditions.  $\Delta t$  is the time amplifier takes to reach its bias point after power down is released.

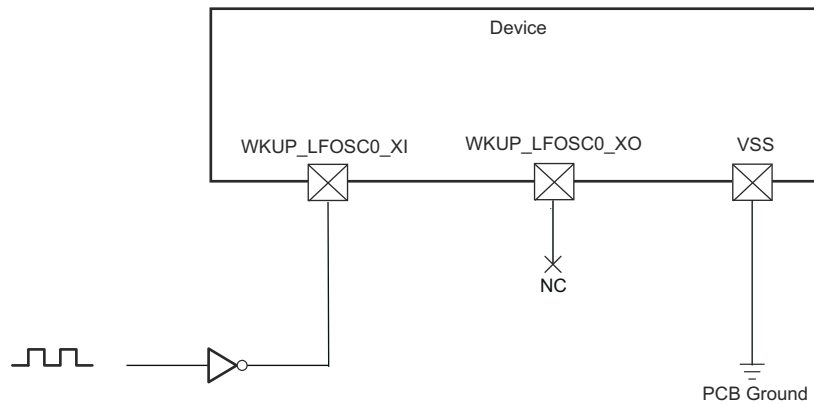
**Figure 6-26. WKUP\_LFOSC0 Start-up Time**

#### 6.9.4.1.7 WKUP\_LFOSC0 LVC MOS Digital Clock Source

##### Note

WKUP\_LFOSC\_XO/WKUP\_LFOSC\_XI - External main crystal interface pins connected to internal oscillator which sources reference clock provides a clock for low power operation in deeper sleep modes. For a list of supported low power modes for this device, please refer to *Overview of Device Low-Power Modes* section in the device TRM.

Figure 6-27 shows the recommended oscillator connections when WKUP\_LFOSC0 is connected to an LVC MOS square-wave digital clock source. The 1.8-V LVC MOS-Compatible clock source is connected to the WKUP\_LFOSC0\_XI pin. In this mode of operation, the WKUP\_LFOSC0\_XO pin is left unconnected and should not be used to source any external components.



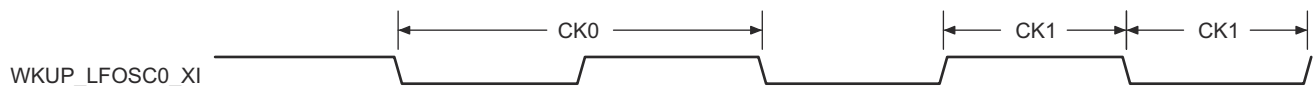
**Figure 6-27. 1.8-V LVC MOS-Compatible Clock Input**

Table 6-24 summarizes the WKUP\_LFOSC0 input clock electrical characteristics.

**Table 6-24. WKUP\_LFOSC0 Oscillator Input Clock Electrical Characteristics—Bypass Mode**

| NAME | DESCRIPTION                                                             | MIN                                   | TYP   | MAX                                   | UNIT    |
|------|-------------------------------------------------------------------------|---------------------------------------|-------|---------------------------------------|---------|
| CK0  | $1/t_{c(WKUP\_LFOSC0\_XI)}$<br>Frequency, WKUP_LFOSC0_XI                |                                       |       | 32.768                                | kHz     |
| CK1  | $t_{w(WKUP\_LFOSC0\_XI)}$<br>Pulse duration, WKUP_LFOSC0_XI low or high | $0.45 \times t_{c(WKUP\_LFOSC0\_XI)}$ |       | $0.55 \times t_{c(WKUP\_LFOSC0\_XI)}$ | ns      |
|      | $C_{IN}$<br>Input capacitance                                           | 2.178                                 | 2.378 | 2.578                                 | pF      |
|      | $I_{IN}$<br>Input current (3.3V mode)                                   | 4                                     | 6     | 10                                    | $\mu A$ |
|      | $t_{sX}$<br>Start-up time                                               |                                       |       | see <sup>(1)</sup>                    | ms      |

- (1) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a wave. The switching time in this case is about 100  $\mu s$ .



**Figure 6-28. WKUP\_LFOSC0\_XI Input Clock**

#### 6.9.4.1.8 WKUP\_LFOSC0 Not Used

For more Information see [Section 5.5, Connections for Unused Pins](#).



#### 6.9.4.2 Output Clocks

The device provides several system clock outputs. Summary of these output clocks are as follows:

- **MCU\_SYSCLKOUT0**
  - SYSCLK0 of WKUP\_PLLCTRL0 is divided by 4 and then sent out of the device as a LVCMOS clock signal (MCU\_SYSCLKOUT0). This signal can be used to test if the main chip clock is functioning or not.
- **MCU\_OBSCLK0**
  - On the clock output MCU\_OBSCLK0, oscillators and PLLs clocks can be observed for tests and debug.
- **SYSCLKOUT0**
  - SYSCLK0 from the MAIN\_PLL controller is divided by 4 and then sent out of the device as a LVCMOS clock signal (SYSCLKOUT0). This signal can be used to test if the main chip clock is functioning or not.
- **OBSCLK0**
  - On the clock output OBSCLK0, oscillators and PLLs clocks can be observed for tests and debug.

### 6.9.4.3 PLLs

Power is supplied to the PLL by internal regulators that derive power from the off-chip power-supply.

There are total nine Phase Locked Loops (PLLs) in the device:

- MCU\_PLL0 (MCU PLL) with WKUP\_PLL\_CTRL0: The MCU PLL — which is used to drive the switch fabrics, accelerators, and a majority of the peripheral clocks — requires a PLL controller to manage the various clock divisions, gating, and synchronization in WKUP domain and MCU domain.
- MCU\_PLL1 (CPSW PLL): The MCU\_PLL1, which is used to drive the CPSW.
- PLL0 (MAIN PLL) with PLL\_CTRL0: The Main PLL — which is used to drive the switch fabrics, accelerators, and a majority of the peripheral clocks — requires a PLL controller to manage the various clock divisions, gating, and synchronization in MAIN domain.
- PLL1 (PER0 PLL): The PER0 PLL, which is used to drive the Peripherals in MAIN Domain.
- PLL2 (PER1 PLL): The PER1 PLL, which is used to drive the PRU\_ICSSG.
- PLL3 (DDR PLL): The DDR PLL is used to drive the DDR PHY for the DDRSS.
- PLL4 (DSS PLL): The DSS PLL, which is used to drive the Display Subsystem.
- PLL6 (ARM0 PLL): The ARM0 PLL, which is used to drive the ARM0.
- PLL7 (ARM1 PLL): The ARM1 PLL, which is used to drive the ARM1.

Most of the Device is driven by the output from the main PLL except the following items:

- Arm subsystem has its own dedicated PLL.
- MCU subsystem has its own dedicated PLL.
- EMIF DDR subsystem has its own dedicated PLL to drive DDR PHY and DDRSS.
- PRU\_ICSSG has clocks sourced from several PLLs:
  - PER0 PLL to generate UART clock,
  - PER1 PLL to generate Core clock,
  - MAIN PLL to generate Industrial Ethernet Peripheral clock,
  - CPSW PLL to generate Ethernet clocks.
- DSS has its own dedicated PLL, to generate Pixel Clock.
- PCIESS require separate reference clocks to drive SERDES PHYs.

---

#### Note

For more information, see the:

- *Device Configuration, Clocking, and PLLs* sections of the device TRM
  - *Peripherals and Display Subsystem Overview* sections of the device TRM
  - *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU\_ICSSG)* section of the device TRM
- 

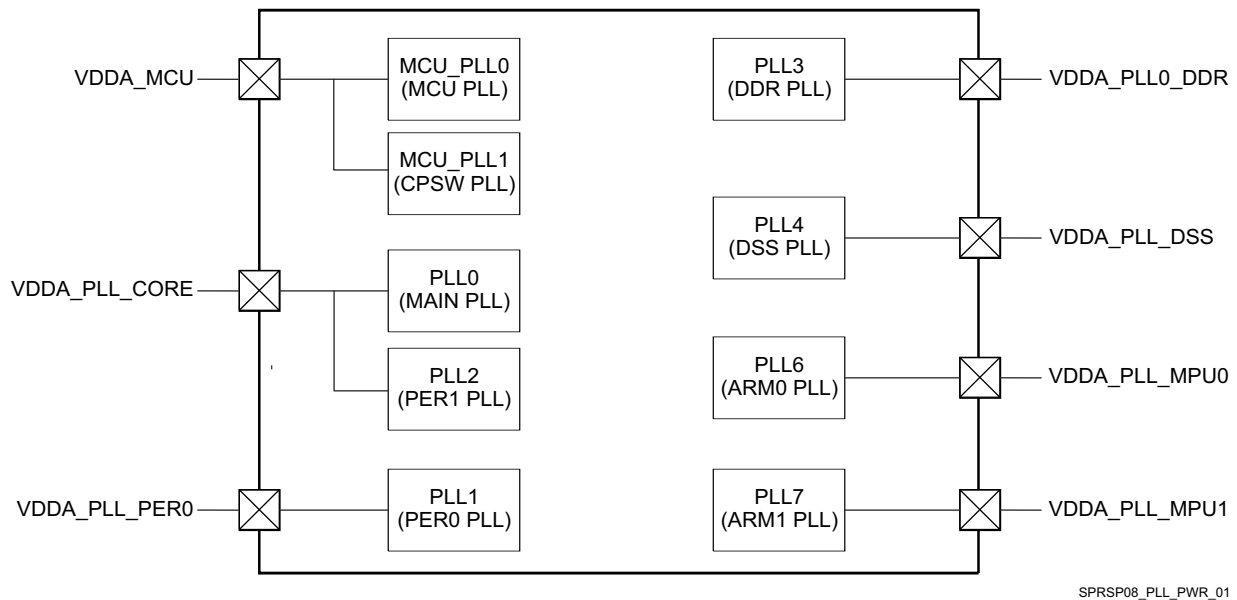
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#### Note

The input reference clock (OSC1\_XI/OSC1\_XO) are specified and the lock time is ensured by the PLL controller, as documented in the *Device Configuration* chapter of the device TRM.

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Figure 6-29 shows the power supply connectivity implemented in the device.



**Figure 6-29. PLL Power Supply Connectivity**

#### 6.9.4.4 Recommended Clock and Control Signal Transition Behavior

All clocks and strobe signals must transition between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner. Monotonic transitions are more easily ensured with faster switching signals. Slower input transitions are more susceptible to glitches due to noise, and special care must be taken for slow input clocks.

#### 6.9.4.5 Module and Peripheral Clock Frequencies

The maximum operating frequency associated with module functional and interface clocks internal to the device is managed by the DMSC firmware. For more details about the clocking structure for a specific module or peripheral, see *Device Configurations* chapter in the device TRM.

Section 6.9.5, *Peripherals* documents the maximum frequency associated with the peripheral clocks in and out of the device.

## 6.9.5 Peripherals

### 6.9.5.1 VIN

Table 6-26, Figure 6-30, and Figure 6-31 present timing requirements for LVDSRX interface.

Table 6-25 presents timing conditions for LVDSRX.

**Table 6-25. LVDSRX Timing Conditions**

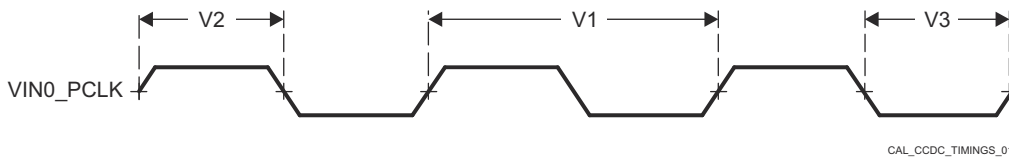
| PARAMETER                             |                                              | MODE  | MIN | MAX  | UNIT |
|---------------------------------------|----------------------------------------------|-------|-----|------|------|
| INPUT CONDITIONS                      |                                              |       |     |      |      |
| SR <sub>i</sub>                       | Input slew rate                              | 1.8 V | 1.3 | 2.64 | V/ns |
|                                       |                                              | 3.3 V | 1.5 | 2.64 | V/ns |
| PCB CONNECTIVITY REQUIREMENTS         |                                              |       |     |      |      |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces |       |     | 50   | ps   |

**Table 6-26. Timing Requirements for LVDSRX**

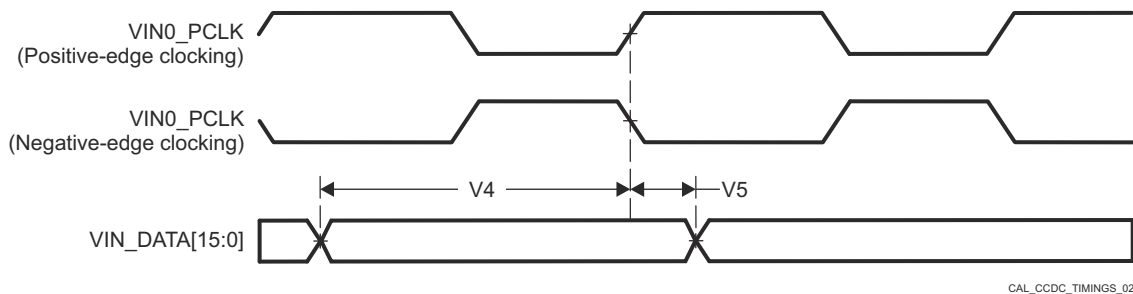
| NO. | PARAMETER                       | DESCRIPTION                                                                                           | MIN                     | MAX | UNIT |
|-----|---------------------------------|-------------------------------------------------------------------------------------------------------|-------------------------|-----|------|
| V1  | t <sub>c</sub> (PCLK)           | Cycle time, VIN0_PCLK                                                                                 | 5.76 <sup>(1)</sup>     |     | ns   |
| V2  | t <sub>w</sub> (PCLKH)          | Pulse duration, VIN0_PCLK high                                                                        | 0.45 × P <sup>(2)</sup> |     | ns   |
| V3  | t <sub>w</sub> (PCLKL)          | Pulse duration, VIN0_PCLK low                                                                         | 0.45 × P <sup>(2)</sup> |     | ns   |
| V4  | t <sub>su</sub> (PCLK-CTL/DATA) | Input setup time, control (VIN0_HD, VIN0_VD) and data (VIN0_DATA[15:0]) valid to VIN0_PCLK transition | 2.42                    |     | ns   |
| V5  | t <sub>h</sub> (CTL/DAT-PCLK)   | Input hold time, VIN0_PCLK transition to control (VIN0_HD, VIN0_VD) valid                             | 0.52                    |     | ns   |

(1) For maximum frequency of 165 MHz

(2) P = VIN0\_PCLK period



**Figure 6-30. LVDSRX Input Clock Signal**



**Figure 6-31. LVDSRX Input Timings**

### 6.9.5.2 CPSW2G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

#### 6.9.5.2.1 CPSW2G MDIO Interface Timings

Table 6-28, Table 6-29, and Figure 6-32 present timing requirements for MDIO.

Table 6-27 presents timing conditions for CPSW2G MDIO.

**Table 6-27. CPSW2G MDIO Timing Conditions**

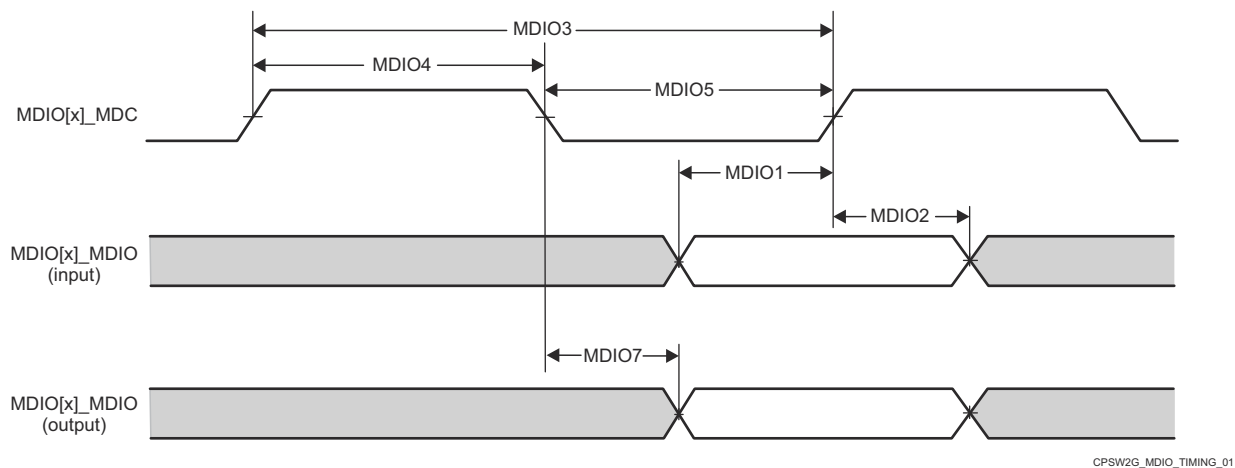
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.9 | 3.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 10  | 470 | pF   |

**Table 6-28. Timing Requirements for MDIO Input**

| NO.   | PARAMETER                  |                                                  | MIN | MAX | UNIT |
|-------|----------------------------|--------------------------------------------------|-----|-----|------|
| MDIO1 | t <sub>su</sub> (MDIO_MDC) | Setup time, MDIO_MDIO valid before MDIO_MDC high | 90  |     | ns   |
| MDIO2 | t <sub>h</sub> (MDIO_MDC)  | Hold time, MDIO_MDIO valid after MDIO_MDC high   | 0   |     | ns   |

**Table 6-29. Switching Characteristics Over Recommended Operating Conditions for MDIO Output**

| NO.   | PARAMETER                 |                                             | MIN  | MAX | UNIT |
|-------|---------------------------|---------------------------------------------|------|-----|------|
| MDIO3 | t <sub>c</sub> (MDC)      | Cycle time, MDIO_MDC                        | 400  |     | ns   |
| MDIO4 | t <sub>w</sub> (MDCH)     | Pulse Duration, MDIO_MDC high               | 160  |     | ns   |
| MDIO5 | t <sub>w</sub> (MDCL)     | Pulse Duration, MDIO_MDC low                | 160  |     | ns   |
| MDIO7 | t <sub>d</sub> (MDC_MDIO) | Delay time, MDIO_MDC low to MDIO_MDIO valid | -150 | 150 | ns   |

**Figure 6-32. CPSW2G MDIO Diagrams Receive and Transmit****6.9.5.2.2 CPSW2G RMII Timings**

Section 6.9.5.2.2.1, Section 6.9.5.2.2.2, Figure 6-33, and Figure 6-34 present timing requirements for CPSW2G RMII receive.

Table 6-30 presents timing conditions for CPSW2G RMII.

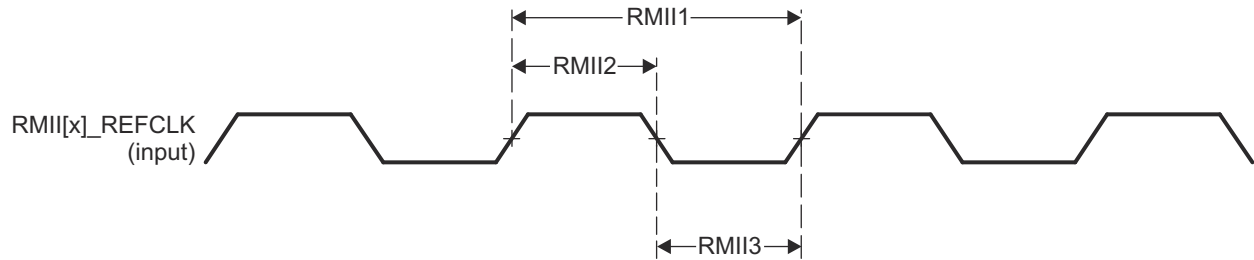
**Table 6-30. CPSW2G RMII Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.9 | 3.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 3   | 25  | pF   |

**6.9.5.2.2.1 Timing Requirements for RMII[x]\_REFCLK - RMII Mode**

| NO.   | PARAMETER                | DESCRIPTION         | MIN    | TYP | MAX    | UNIT |
|-------|--------------------------|---------------------|--------|-----|--------|------|
| RMII1 | t <sub>c</sub> (REF_CLK) | Cycle time, REF_CLK | 19.999 |     | 20.001 | ns   |

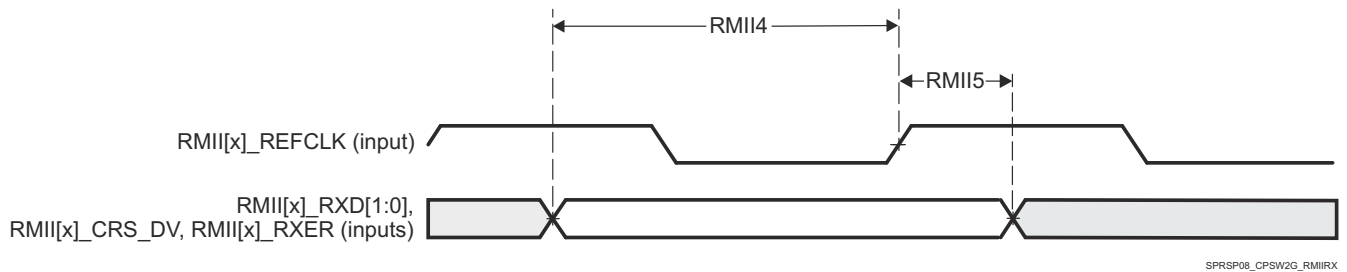
| NO.   | PARAMETER          | DESCRIPTION                  | MIN | TYP | MAX | UNIT |
|-------|--------------------|------------------------------|-----|-----|-----|------|
| RMII2 | $t_{w(REF\_CLKH)}$ | Pulse Duration, REF_CLK High | 7   |     | 13  | ns   |
| RMII3 | $t_{w(REF\_CLKL)}$ | Pulse Duration, REF_CLK Low  | 7   |     | 13  | ns   |



**Figure 6-33. RMII[x]\_REFCLK Timing - RMII Mode**

#### 6.9.5.2.2.2 Timing Requirements for RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, and RMII[x]\_RXER - RMII Mode

| NO.   | PARAMETER                  | DESCRIPTION                               | MIN | TYP | MAX | UNIT |
|-------|----------------------------|-------------------------------------------|-----|-----|-----|------|
| RMII4 | $t_{su(RXD-REF\_CLK)}$     | Setup time, RXD[1:0] valid before REF_CLK | 4   |     |     | ns   |
|       | $t_{su(CRS\_DV-REF\_CLK)}$ | Setup time, CRS_DV valid before REF_CLK   | 4   |     |     | ns   |
|       | $t_{su(RX\_ER-REF\_CLK)}$  | Setup time, RX_ER valid before REF_CLK    | 4   |     |     | ns   |
| RMII5 | $t_{h(REF\_CLK-RXD)}$      | Hold time RXD[1:0] valid after REF_CLK    | 2   |     |     | ns   |
|       | $t_{h(REF\_CLK-CRS\_DV)}$  | Hold time, CRS_DV valid after REF_CLK     | 2   |     |     | ns   |
|       | $t_{h(REF\_CLK-RX\_ER)}$   | Hold time, RX_ER valid after REF_CLK      | 2   |     |     | ns   |



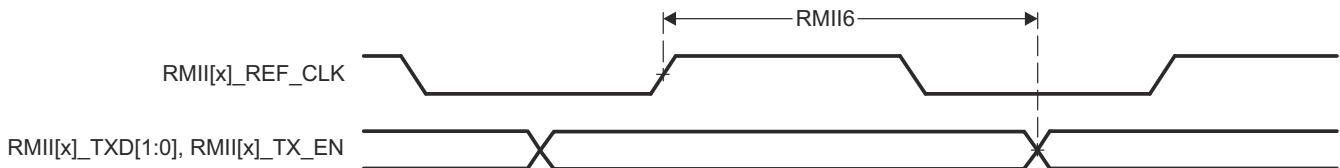
SPRSP08\_CPSW2G\_RMIIRX

**Figure 6-34. RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, RMII[x]\_RXER Timing - RMII Mode**

Section 6.9.5.2.2.3, and Section 6.9.5.2.2.3 present switching characteristics for CPSW2G RMII Transmit.

#### 6.9.5.2.2.3 Switching Characteristics for RMII[x]\_TXD[1:0], and RMII[x]\_TXEN - RMII Mode

| NO.   | PARAMETER            | DESCRIPTION                                | MIN | TYP | MAX | UNIT |
|-------|----------------------|--------------------------------------------|-----|-----|-----|------|
| RMII6 | $t_d(REF\_CLK-TXD)$  | Delay time, REF_CLK High to TXD[1:0] valid | 2   |     | 13  | ns   |
|       | $t_d(REF\_CLK-TXEN)$ | Delay time, REF_CLK to TXEN valid          | 2   |     | 13  | ns   |



**Figure 6-35. RMII[x]\_TXD[1:0], and RMII[x]\_TX\_EN Switching Characteristics – RMII Mode**

### 6.9.5.2.3 CPSW2G RGMII Timings

Section 6.9.5.2.3.1, Section 6.9.5.2.3.2, and Figure 6-36 present timing requirements for receive RGMII operation.

Table 6-31 presents timing conditions for CPSW2G RGMII.

**Table 6-31. CPSW2G RGMII Timing Conditions**

| PARAMETER                             |                                              |                                                       | MIN  | MAX | UNIT |
|---------------------------------------|----------------------------------------------|-------------------------------------------------------|------|-----|------|
| <b>INPUT CONDITIONS</b>               |                                              |                                                       |      |     |      |
| SR <sub>I</sub>                       | Input slew rate                              |                                                       | 2.64 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                              |                                                       |      |     |      |
| C <sub>L</sub>                        | Output load capacitance                      |                                                       | 2    | 20  | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                              |                                                       |      |     |      |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces | RGMII[x]_RXC,<br>RGMII[x]_RD[3:0],<br>RGMII[x]_RX_CTL |      | 50  | ps   |
|                                       |                                              | RGMII[x]_TXC,<br>RGMII[x]_TD[3:0],<br>RGMII[x]_TX_CTL |      | 50  | ps   |

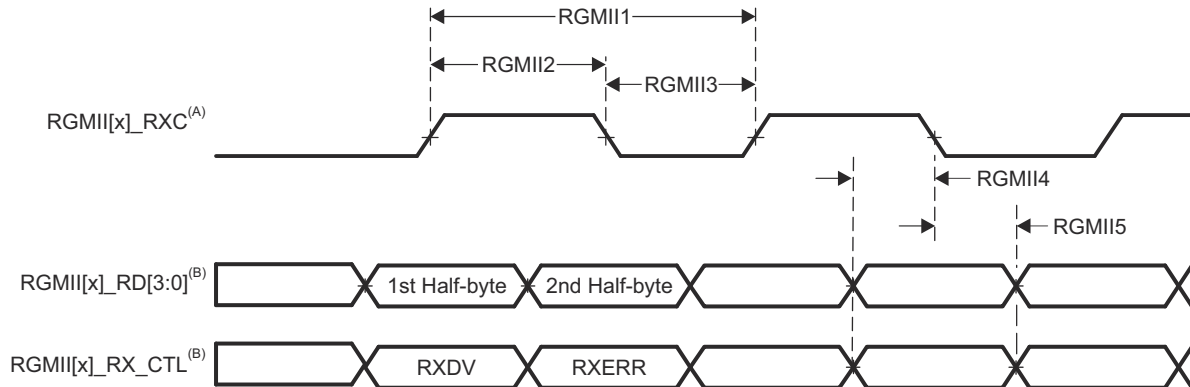
#### 6.9.5.2.3.1 Timing Requirements for RGMII[x]\_RCLK - RGMII Mode

| NO.    | PARAMETER             | DESCRIPTION              | MODE     | MIN | TYP | MAX | UNIT |
|--------|-----------------------|--------------------------|----------|-----|-----|-----|------|
| RGMII1 | t <sub>c</sub> (RXC)  | Cycle time, RXC          | 10Mbps   | 360 |     | 440 | ns   |
|        |                       |                          | 100Mbps  | 36  |     | 44  | ns   |
|        |                       |                          | 1000Mbps | 7.2 |     | 8.8 | ns   |
| RGMII2 | t <sub>w</sub> (RXCH) | Pulse duration, RXC high | 10Mbps   | 160 |     | 240 | ns   |
|        |                       |                          | 100Mbps  | 16  |     | 24  | ns   |
|        |                       |                          | 1000Mbps | 3.6 |     | 4.4 | ns   |
| RGMII3 | t <sub>w</sub> (RXCL) | Pulse duration, RXC low  | 10Mbps   | 160 |     | 240 | ns   |
|        |                       |                          | 100Mbps  | 16  |     | 24  | ns   |
|        |                       |                          | 1000Mbps | 3.6 |     | 4.4 | ns   |

#### 6.9.5.2.3.2 Timing Requirements for RGMII[x]\_RD[3:0], and RGMII[x]\_RCTL - RGMII Mode

| NO.    | PARAMETER                    | DESCRIPTION                                   | MODE     | MIN | TYP | MAX | UNIT |
|--------|------------------------------|-----------------------------------------------|----------|-----|-----|-----|------|
| RGMII4 | t <sub>su</sub> (RD-RXC)     | Setup time, RD[3:0] valid before RXC high/low | 10Mbps   | 1   |     |     | ns   |
|        |                              |                                               | 100Mbps  | 1   |     |     | ns   |
|        |                              |                                               | 1000Mbps | 1   |     |     | ns   |
|        | t <sub>su</sub> (RX_CTL-RXC) | Setup time, RX_CTL valid before RXC high/low  | 10Mbps   | 1   |     |     | ns   |
|        |                              |                                               | 100Mbps  | 1   |     |     | ns   |
|        |                              |                                               | 1000Mbps | 1   |     |     | ns   |

| NO.    | PARAMETER            | DESCRIPTION                                 | MODE     | MIN  | TYP | MAX | UNIT |
|--------|----------------------|---------------------------------------------|----------|------|-----|-----|------|
| RGMII5 | $t_{h(RXC-RD)}$      | Hold time, RD[3:0] valid after RXC high/low | 10Mbps   | 1    |     |     | ns   |
|        |                      |                                             | 100Mbps  | 1    |     |     | ns   |
|        |                      |                                             | 1000Mbps | 1.15 |     |     | ns   |
|        | $t_{h(RXC-RX\_CTL)}$ | Hold time, RX_CTL valid after RXC high/low  | 10Mbps   | 1    |     |     | ns   |
|        |                      |                                             | 100Mbps  | 1    |     |     | ns   |
|        |                      |                                             | 1000Mbps | 1.15 |     |     | ns   |



- A. RGMII\_RXC must be externally delayed relative to the data and control pins.
- B. Data and control information is received using both edges of the clocks. RGMII\_RXD[3:0] carries data bits 3-0 on the rising edge of RGMII\_RXC and data bits 7-4 on the falling edge of RGMII\_RXC. Similarly, RGMII\_RXCTL carries RXDV on rising edge of RGMII\_RXC and RXERR on falling edge of RGMII\_RXC.

**Figure 6-36. CPSW2G Receive Interface Timing, RGMII operation**

Section 6.9.5.2.3.3, Section 6.9.5.2.3.4, and Figure 6-37 present switching characteristics for transmit - RGMII for 10 Mbps, 100 Mbps, and 1000 Mbps.

#### 6.9.5.2.3.3 Switching Characteristics for RGMII[x]\_TCLK - RGMII Mode

| NO.    | PARAMETER     | DESCRIPTION              | MODE     | MIN | TYP | MAX | UNIT |
|--------|---------------|--------------------------|----------|-----|-----|-----|------|
| RGMII1 | $t_{c(TXC)}$  | Cycle time, TXC          | 10Mbps   | 360 |     | 440 | ns   |
|        |               |                          | 100Mbps  | 36  |     | 44  | ns   |
|        |               |                          | 1000Mbps | 7.2 |     | 8.8 | ns   |
| RGMII2 | $t_{w(TXCH)}$ | Pulse duration, TXC high | 10Mbps   | 160 |     | 240 | ns   |
|        |               |                          | 100Mbps  | 16  |     | 24  | ns   |
|        |               |                          | 1000Mbps | 3.6 |     | 4.4 | ns   |
| RGMII3 | $t_{w(TXCL)}$ | Pulse duration, TXC low  | 10Mbps   | 160 |     | 240 | ns   |
|        |               |                          | 100Mbps  | 16  |     | 24  | ns   |
|        |               |                          | 1000Mbps | 3.6 |     | 4.4 | ns   |

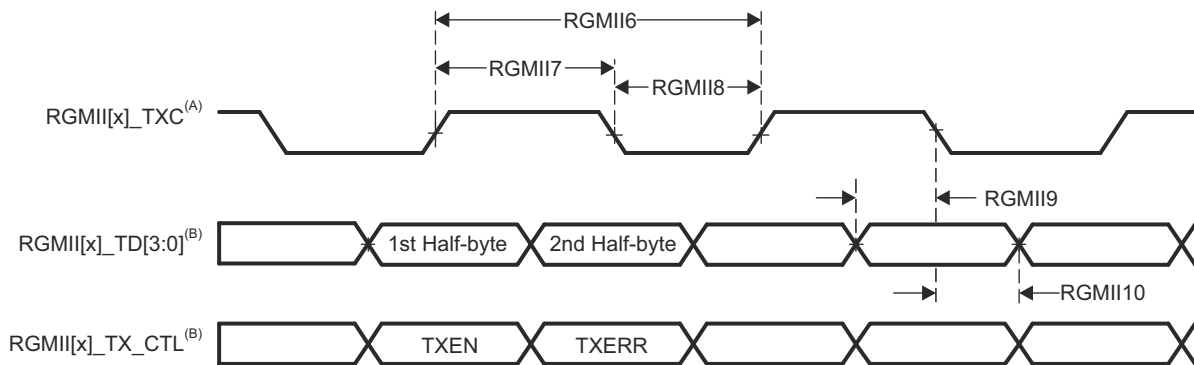
#### 6.9.5.2.3.4 Switching Characteristics for RGMII[x]\_TD[3:0], and RGMII[x]\_TX\_CTL - RGMII Mode

| NO.    | PARAMETER              | DESCRIPTION                                                        | MODE        | MIN                 | TYP | MAX | UNIT |
|--------|------------------------|--------------------------------------------------------------------|-------------|---------------------|-----|-----|------|
| RGMII9 | $t_{osu(TD-TXC)}$      | Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low | 10/100 Mbps | 1.2                 |     |     | ns   |
|        |                        |                                                                    | 1000 Mbps   | 1.05 <sup>(1)</sup> |     |     | ns   |
|        | $t_{osu(TX\_CTL-TXC)}$ | Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low  | 10/100 Mbps | 1.2                 |     |     | ns   |
|        |                        |                                                                    | 1000 Mbps   | 1.05 <sup>(1)</sup> |     |     | ns   |



| NO.     | PARAMETER             | MODE                                                                 | MIN         | TYP                 | MAX | UNIT |
|---------|-----------------------|----------------------------------------------------------------------|-------------|---------------------|-----|------|
| RGMII10 | $t_{oh(TD-TXC)}$      | Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low | 10/100 Mbps | 1.2                 |     | ns   |
|         |                       |                                                                      | 1000 Mbps   | 1.05 <sup>(1)</sup> |     | ns   |
|         | $t_{oh(TX\_CTL-TXC)}$ | Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low  | 10/100 Mbps | 1.2                 |     | ns   |
|         |                       |                                                                      | 1000 Mbps   | 1.05 <sup>(1)</sup> |     | ns   |

(1) 1000Mbps operation requires that the 4 data pins (RGMII[x]\_TD[3:0]) and RGMII[x]\_TX\_CTL have their board propagation delays matched to within 50 ps of RGMII[x]\_TXC.



- A. TXC is delayed internally before being driven to the RGMII[x]\_TXC pin. This internal delay is always enabled.
- B. Data and control information is received using both edges of the clocks. RGMII\_TD[3:0] carries data bits 3-0 on the rising edge of RGMII\_TXC and data bits 7-4 on the falling edge of RGMII\_TXC. Similarly, RGMII\_TX\_CTL carries TXDV on rising edge of RGMII\_TXC and RTXERR on falling edge of RGMII\_TXC.

**Figure 6-37. CPSW2G Transmit Interface Timing RGMII Mode**

For more information, see section *Gigabit Ethernet MAC (MCU\_CPSW0)* in the device TRM.

### 6.9.5.3 CSI2

#### Note

For more information, see section *Camera Adapter Layer (CAL) Subsystem* in the device TRM.

The camera adaptation layer (CAL) delays with the processing of pixel data coming from an external image sensor and data from memory. It is a key component for the following multimedia applications: camera viewfinder, video record, and still image capture.

The device includes one instantiation of CAL Subsystem named CALSS0, with a single companion CAMERARX0 instance.

CALSS0 is a very flexible subsystem that enables 3 different connections to cameras. It supports MIPI CSI-2 over D-PHY serial interface; a LVDS serial interface; and a traditional parallel interface.

The CALSS0 is compliant with the MIPI D-PHY RX specification v1.01.00 and the MIPI CSI-2 specification, with 4 data differential lanes plus 1 clock differential lane in synchronous mode, double data rate:

- 1.2 Gbps (600 MHz) for each lane.

### 6.9.5.4 DDRSS

For more details about features and additional description information on the device DDR4 Memory Interfaces, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

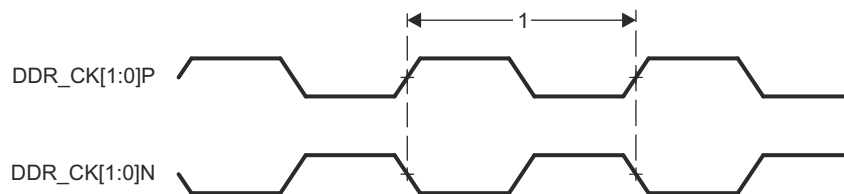
The device has dedicated interfaces to DDR4 SDRAM. It supports JESD79-4B standard-compliant DDR4 SDRAM devices with the following features:

- 16-bit or 32-bit data path to external SDRAM memory
- Memory device capacity: Up to 8 GB address space available over one chip select

[Table 6-32](#) and [Figure 6-38](#) present switching characteristics for DDRSS.

**Table 6-32. Switching Characteristics for DDRSS**

| NO. | PARAMETER                  |                                 | DDR TYPE | MODE | MIN  | MAX | UNIT |
|-----|----------------------------|---------------------------------|----------|------|------|-----|------|
| 1   | $t_{c(DDR\_CKP/DDR\_CKN)}$ | Cycle time, DDR_CKP and DDR_CKN | DDR4     |      | 1.25 | 1.6 | ns   |



**Figure 6-38. DDRSS Memory Interface Clock Timing**

For more information, see section *DDR Subsystem (DDRSS)* in the device TRM.

### 6.9.5.5 DSS

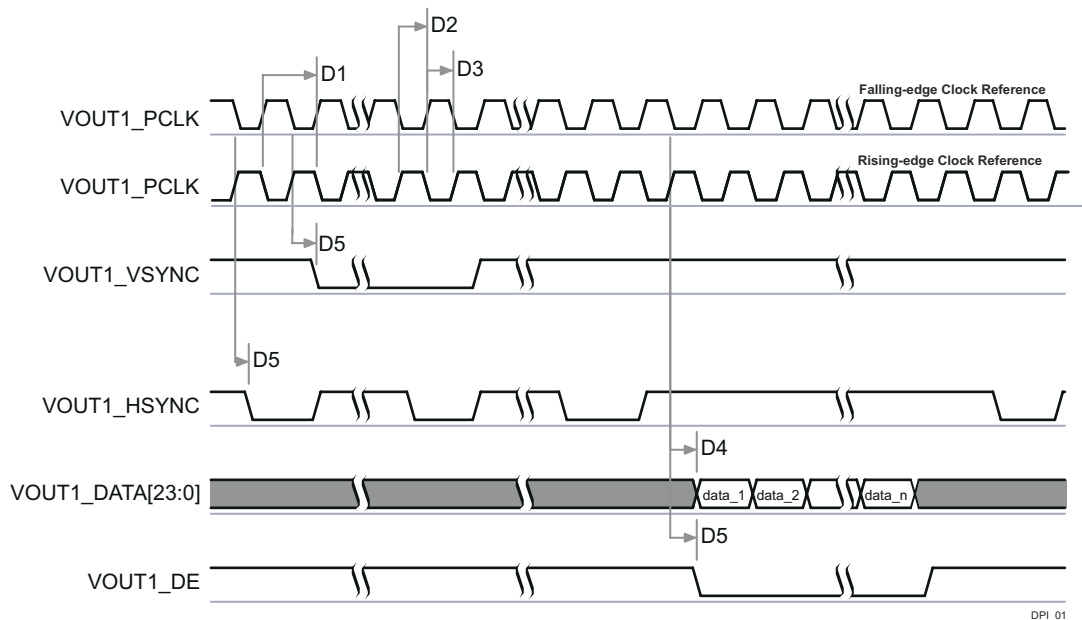
For more details about features and additional description information on the device Display Subsystem – Video Output Ports, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

[Table 6-33](#), [Table 6-34](#), [Figure 6-39](#) and [Figure 6-40](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-33. DPI Video Output Switching Characteristics**

| NO. | PARAMETER                             |                                                              | MIN               | MAX  | UNIT |
|-----|---------------------------------------|--------------------------------------------------------------|-------------------|------|------|
| D1  | $t_c(\text{VOUT1\_PCLK})$             | Cycle time, VOUT1_PCLK                                       | 6.06              |      | ns   |
| D2  | $t_w(\text{VOUT1\_PCLKL})$            | Pulse duration, VOUT1_PCLK low                               | $0.475 * P^{(1)}$ |      | ns   |
| D3  | $t_w(\text{VOUT1\_PCLKH})$            | Pulse duration, VOUT1_PCLK high                              | $0.475 * P^{(1)}$ |      | ns   |
| D4  | $t_d(\text{VOUT1\_PCLK- VOUT\_DATA})$ | Delay time, VOUT1_PCLK to VOUT1_DATA[23:0]                   | -0.68             | 1.78 | ns   |
| D5  | $t_d(\text{VOUT1\_PCLK- VOUT\_CTRL})$ | Delay time, VOUT1_PCLK to VOUT1_VSYNC, VOUT1_HSYNC, VOUT1_DE | -0.68             | 1.78 | ns   |

(1) P = output VOUT1\_PCLK period in ns.



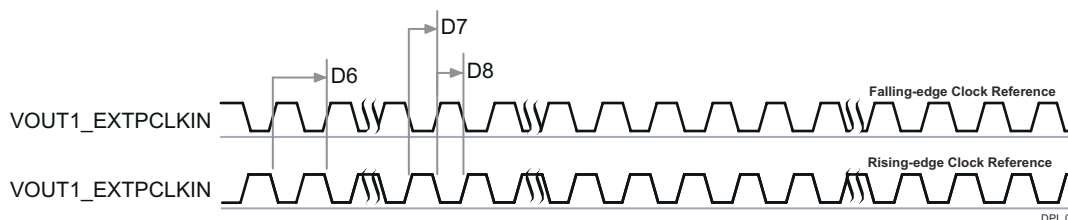
- The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.
- The polarity and the pulse width of VOUT1\_HSYNC and VOUT1\_VSYNC are programmable, refer to section *Display Subsystem (DSS)* in the device TRM.
- The VOUT1\_PCLK frequency can be configured, refer to section *Display Subsystem (DSS)* in the device TRM.

**Figure 6-39. DPI Video Output**

**Table 6-34. DPI External Pixel Clock Input Timing Requirements**

| NO. |                          |                                     | MIN               | MAX | UNIT |
|-----|--------------------------|-------------------------------------|-------------------|-----|------|
| D6  | $t_{c}(VOUT1\_EXTCLKIN)$ | Cycle time, VOUT1_EXTCLKIN          | 6.06              |     | ns   |
| D7  | $t_{w}(VOUT1\_EXTCLKIN)$ | Pulse duration, VOUT1_EXTCLKIN low  | $0.475 * P^{(1)}$ |     | ns   |
| D8  | $t_{w}(VOUT1\_EXTCLKIN)$ | Pulse duration, VOUT1_EXTCLKIN high | $0.475 * P^{(1)}$ |     | ns   |

(1) P = output VOUT1\_PCLK period in ns.



**Figure 6-40. DPI External Pixel Clock Input**

For more information, see section *Display Subsystem (DSS)* in the device TRM.

#### 6.9.5.6 eCAP

The supported features by the device eCAP are:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Independent edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt capabilities on any of the four capture events
- Input capture signal pre-scaling (from 1 to 16)
- Support of different capture modes (single shot capture, continuous mode capture, absolute timestamp capture or difference mode time-stamp capture)

Table 6-35 represents eCAP timing conditions.

**Table 6-35. eCAP Timing Conditions**

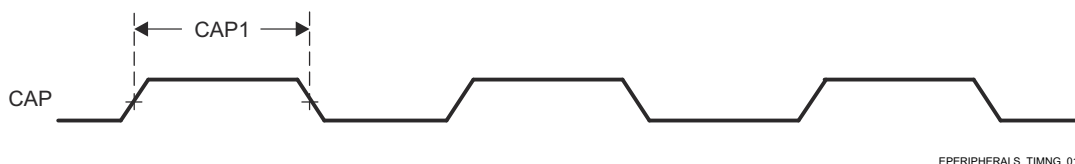
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>i</sub>          | Input slew rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 7   | pF   |

Section 6.9.5.6.1 and Section 6.9.5.6.2 present timing and switching characteristics for eCAP (see Figure 6-41 and Figure 6-42).

#### 6.9.5.6.1 eCAP Timing Requirements

| NO.  | PARAMETER    | DESCRIPTION                        | MIN            | MAX | UNIT |
|------|--------------|------------------------------------|----------------|-----|------|
| CAP1 | $t_{w}(CAP)$ | Pulse duration, CAP (asynchronous) | $3 + 2P^{(1)}$ |     | ns   |

(1) P = sysclk period in ns.



**Figure 6-41. eCAP Timing Requirements**

### 6.9.5.6.2 eCAP Switching Characteristics

| NO.  | PARAMETER     | DESCRIPTION           | MIN             | MAX | UNIT |
|------|---------------|-----------------------|-----------------|-----|------|
| CAP2 | $t_{w(APWM)}$ | Pulse duration, APWMx | $-3 + 2P^{(1)}$ |     | ns   |

(1) P = sysclk period in ns.



**Figure 6-42. eCAP Switching Characteristics**

For more information, see section *Enhanced Capture (ECAP) Module* in the device TRM.

### 6.9.5.7 ePWM

The supported features by the device ePWM are:

- Dedicated 16-bit time-base counter with period and frequency control
- Two independent PWM outputs which can be used in different configurations (with single-edge operation, with dual-edge symmetric operation or one independent PWM output with dual-edge asymmetric operation)
- Asynchronous override control of PWM signals during fault conditions
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both latched and un-latched fault conditions
- Events enabling to trigger both CPU interrupts and start of ADC conversions

Table 6-36 represents ePWM timing conditions.

**Table 6-36. ePWM Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>i</sub>          | Input slew rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 7   | pF   |

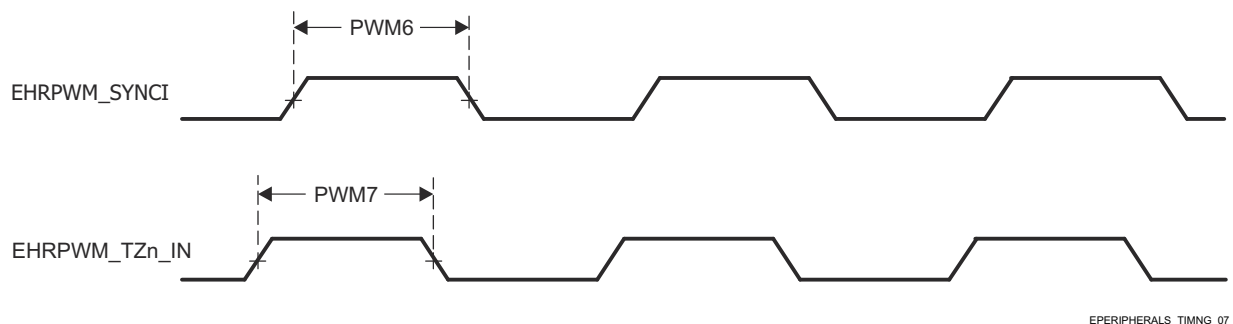
Section 6.9.5.7.1 and Section 6.9.5.7.2 present timing and switching characteristics for eHRPWM (see Figure 6-43, Figure 6-44, Figure 6-45, and Figure 6-46).

#### 6.9.5.7.1 ePWM Timing Requirements

| NO.  | PARAMETER       | DESCRIPTION                  | MIN            | MAX | UNIT |
|------|-----------------|------------------------------|----------------|-----|------|
| PWM6 | $t_{w(SYNCIN)}$ | Pulse duration, eHRPWM_SYNCI | $3 + 2P^{(1)}$ |     | ns   |

| NO.  | PARAMETER   | DESCRIPTION                       | MIN            | MAX | UNIT |
|------|-------------|-----------------------------------|----------------|-----|------|
| PWM7 | $t_{w(TZ)}$ | Pulse duration, eHRPWM_TZn_IN low | $3 + 3P^{(1)}$ |     | ns   |

(1) P = sysclk period in ns



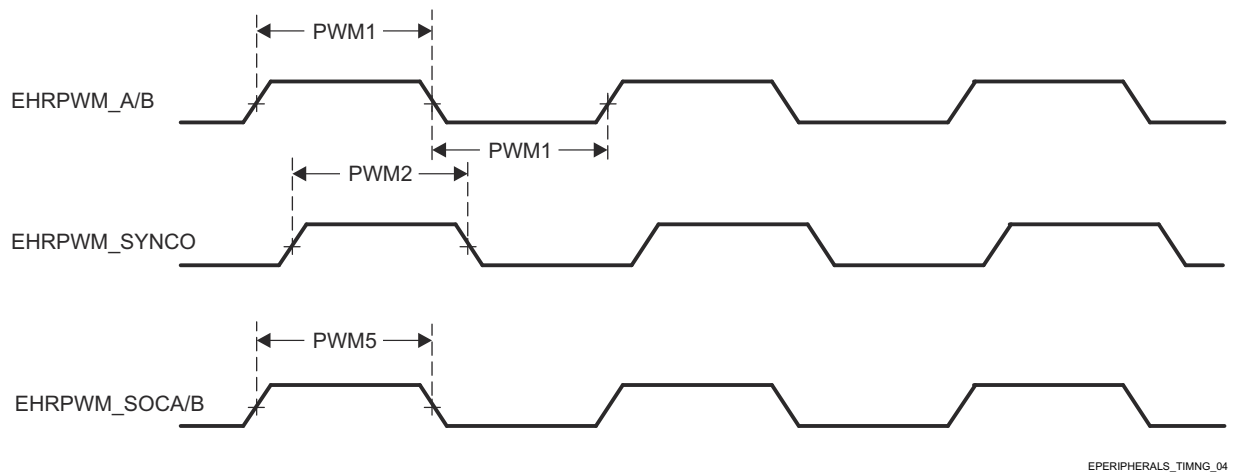
**Figure 6-43. ePWM Timing Requirements**

#### 6.9.5.7.2 ePWM Switching Characteristics

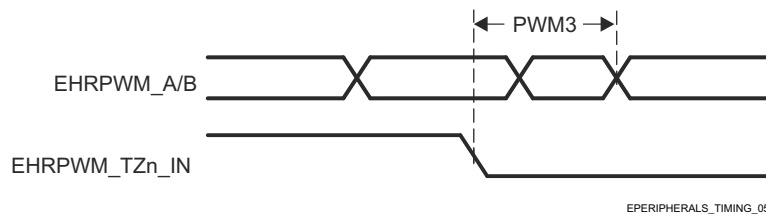
| NO.  | PARAMETER        | DESCRIPTION                                                    | MIN            | MAX | UNIT |
|------|------------------|----------------------------------------------------------------|----------------|-----|------|
| PWM1 | $t_{w(PWM)}$     | Pulse duration, EHRPWM_A/B high/low                            | $-3 + P^{(1)}$ |     | ns   |
| PWM2 | $t_{w(SYNCOU)}$  | Pulse duration, EHRPWM_SYNCO                                   | $-3 + P^{(1)}$ |     | ns   |
| PWM3 | $t_{d(TZ-PWM)}$  | Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B forced high/low |                | 11  | ns   |
| PWM4 | $t_{d(TZ-PWMZ)}$ | Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B Hi-Z            |                | 11  | ns   |

| NO.  | PARAMETER    | DESCRIPTION                           | MIN            | MAX | UNIT |
|------|--------------|---------------------------------------|----------------|-----|------|
| PWM5 | $t_{w(SOC)}$ | Pulse duration, EHRPWM_SOC/A/B output | $-3 + P^{(1)}$ |     | ns   |

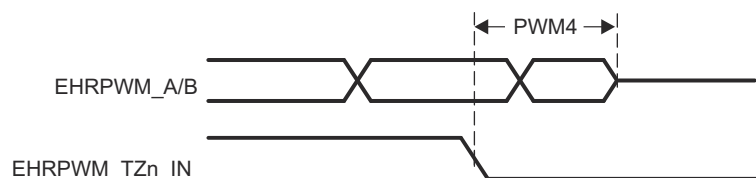
(1) P = sysclk period in ns



**Figure 6-44. EHRPWM Switching Characteristics**



**Figure 6-45. EHRPWM\_TZn\_IN to EHRPWM\_A/B Forced Switching Characteristics**



**Figure 6-46. EHRPWM\_TZn\_IN to EHRPWM\_A/B Hi-Z Switching Characteristics**

For more information, see section *Enhanced Pulse Width Modulation (EPWM) Module* in the device TRM.

#### 6.9.5.8 eQEP

The supported features by the device eQEP are:

- Input Synchronization
- Three Stage/Six Stage Digital Noise Filter
- Quadrature Decoder Unit
- Position Counter and Control unit for position measurement
- Quadrature Edge Capture unit for low speed measurement
- Unit Time base for speed/frequency measurement
- Watchdog Timer for detecting stalls

Table 6-37 represents eQEP timing conditions.

**Table 6-37. eQEP Timing Conditionns**

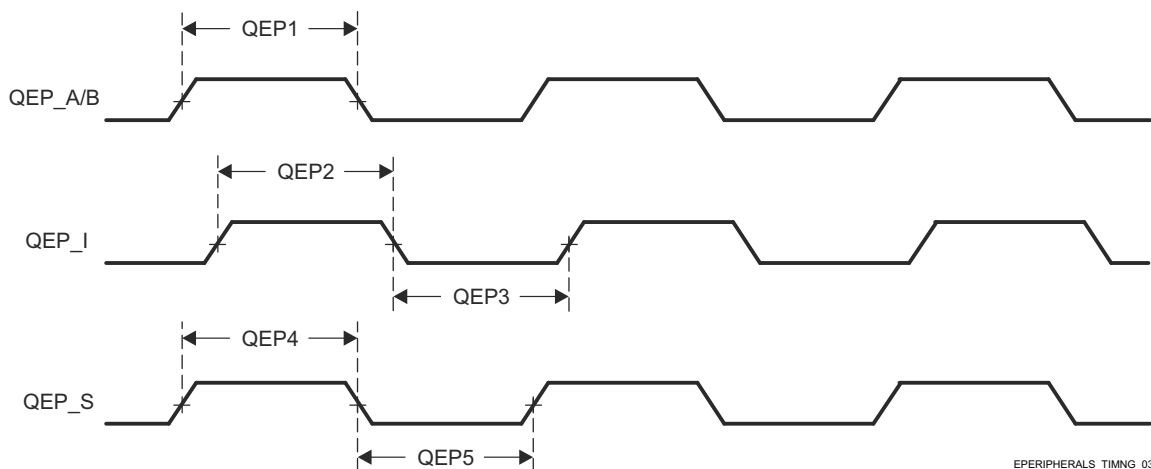
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 7   | pF   |

Section 6.9.5.8.1 and Section 6.9.5.8.2 present Timing Requirements and Switching Characteristics for eQEP (see Figure 6-47).

#### 6.9.5.8.1 eQEP Timing Requirements

| NO.  | PARAMETER                           | DESCRIPTION                | MIN                   | MAX | UNIT |
|------|-------------------------------------|----------------------------|-----------------------|-----|------|
| QEP1 | t <sub>w</sub> (QEP)                | Pulse duration, QEP_A/B    | 3 + 2P <sup>(1)</sup> |     | ns   |
| QEP2 | t <sub>w</sub> (QEP <sub>I</sub> H) | Pulse duration, QEP_I high | 3 + 2P <sup>(1)</sup> |     | ns   |
| QEP3 | t <sub>w</sub> (QEP <sub>I</sub> L) | Pulse duration, QEP_I low  | 3 + 2P <sup>(1)</sup> |     | ns   |
| QEP4 | t <sub>w</sub> (QEP <sub>S</sub> H) | Pulse duration, QEP_S high | 3 + 2P <sup>(1)</sup> |     | ns   |
| QEP5 | t <sub>w</sub> (QEP <sub>S</sub> L) | Pulse duration, QEP_S low  | 3 + 2P <sup>(1)</sup> |     | ns   |

(1) P = sysclk period in ns.



**Figure 6-47. eQEP Timing Requirements**

#### 6.9.5.8.2 eQEP Switching Characteristics

| NO.  | PARAMETER                 | DESCRIPTION                                     | MIN | MAX | UNIT |
|------|---------------------------|-------------------------------------------------|-----|-----|------|
| QEP6 | t <sub>d</sub> (QEP-CNTR) | Delay time, external clock to counter increment |     | 24  | ns   |

For more information, see section *Enhanced Quadrature Encoder Pulse (EQEP) Module* in the device TRM.

#### 6.9.5.9 GPIO

The device has three instances of GPIO144 modules. The GPIO pins are grouped into banks (16 pins per bank), which means that each GPIO module provides up to 144 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 432 (3 instances × (9 banks × 16 pins)) pins. Since WKUP\_GPIO0\_[56:143], GPIO0\_[96:143], and GPIO1\_[90:143] are reserved in this Device, general purpose interface supports up to 242 pins.

For more details about features and additional description information on the device General-Purpose Interface, see the corresponding sections within Section 5.3, *Signal Descriptions* and Section 7, *Detailed Description*.



**Note**

The general-purpose input/output  $i$  ( $i = 0$  to  $1$ ) is also referred to as GPIOi.

Table 6-38 presents timing conditions of the GPIO interface.

**Table 6-38. GPIO Timing Conditions**

| PARAMETER                | DESCRIPTION             | MIN  | MAX | UNIT |
|--------------------------|-------------------------|------|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |      |     |      |
| $SR_i$                   | Input slew rate         | 0.75 | 6.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |      |     |      |
| $C_L$                    | Output load capacitance | 3    | 10  | pF   |

Section 6.9.5.9.1 and Section 6.9.5.9.2 present timings and switching characteristics of the GPIO Interface.

**6.9.5.9.1 GPIO Timing Requirements**

| NO. | PARAMETER         | DESCRIPTION               | MIN              | MAX | UNIT |
|-----|-------------------|---------------------------|------------------|-----|------|
| GP2 | $t_{w(GPIO\_IN)}$ | Minimum Input Pulse Width | $3.6 + 2P^{(1)}$ |     | ns   |

(1)  $P$  = functional clock period in ns.

**6.9.5.9.2 GPIO Switching Characteristics**

| NO. | PARAMETER          | DESCRIPTION                | MIN                   | MAX | UNIT |
|-----|--------------------|----------------------------|-----------------------|-----|------|
| GP1 | $t_{w(GPIO\_OUT)}$ | Minimum Output Pulse Width | $-4.6 + 0.975P^{(1)}$ |     | ns   |

(1)  $P$  = functional clock period in ns.

For more information, see section *General-Purpose Interface (GPIO)* in the device TRM.

**6.9.5.10 GPMC**

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding sections within Section 5.3, *Signal Descriptions* and Section 7, *Detailed Description*.

Table 6-39 presents the timing conditions for GPMC.

**Table 6-39. GPMC Timing Conditions**

| PARAMETER                | DESCRIPTION             | MIN  | MAX | UNIT |
|--------------------------|-------------------------|------|-----|------|
| <b>Input Conditions</b>  |                         |      |     |      |
| $SR_i$                   | Input slew rate         | 1.65 | 4   | V/ns |
| <b>Output Conditions</b> |                         |      |     |      |
| $C_L$                    | Output load capacitance | 5    | 20  | pF   |

**6.9.5.10.1 GPMC and NOR Flash—Synchronous Mode**

Section 6.9.5.10.1.1 and Section 6.9.5.10.1.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-48 through Figure 6-52).

#### 6.9.5.10.1.1 GPMC and NOR Flash Timing Requirements—Synchronous Mode

| NO. | PARAMETER            | DESCRIPTION                                                                                | MODE <sup>(2)</sup>                                                | MIN  | MAX | UNIT |
|-----|----------------------|--------------------------------------------------------------------------------------------|--------------------------------------------------------------------|------|-----|------|
| F12 | $t_{su(dV-clkH)}$    | Setup time, input data GPMC_AD[15:0] valid before output clock GPMC_CLK high               | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1     | 2.17 |     | ns   |
|     |                      |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1 | 3.46 |     | ns   |
| F13 | $t_h(clkH-dV)$       | Hold time, input data GPMC_AD[15:0] valid after output clock GPMC_CLK high                 | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1     | 1.78 |     | ns   |
|     |                      |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1 | 1.78 |     | ns   |
| F21 | $t_{su(waitV-clkH)}$ | Setup time, input wait GPMC_WAIT[x] valid before output clock GPMC_CLK high <sup>(1)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1     | 2.17 |     | ns   |
|     |                      |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1 | 3.46 |     | ns   |
| F22 | $t_h(clkH-waitV)$    | Hold time, input wait GPMC_WAIT[x] valid after output clock GPMC_CLK high <sup>(1)</sup>   | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1     | 1.78 |     | ns   |
|     |                      |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1 | 1.78 |     | ns   |

(1) In GPMC\_WAIT[x], x is equal to 0 or 1.

(2) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency

For not\_div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 1h to 3h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency / (2 to 4)

For GPMC\_FCLK\_MUX\_100:

- gpmc\_fclk\_sel[1:0] = 01 = PER1\_PLL\_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

#### 6.9.5.10.1.2 GPMC and NOR Flash Switching Characteristics—Synchronous Mode

| NO. <sup>(2)</sup> | PARAMETER   | DESCRIPTION                                        | MODE <sup>(19)</sup>                                           | MIN                              | MAX | UNIT |
|--------------------|-------------|----------------------------------------------------|----------------------------------------------------------------|----------------------------------|-----|------|
| F0                 | $t_c(clk)$  | Period, output clock GPMC_CLK <sup>(18)</sup>      | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1 | 10                               |     | ns   |
| F1                 | $t_w(clkH)$ | Typical pulse duration, output clock GPMC_CLK high | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1 | -0.3+0.4<br>75°P <sup>(15)</sup> |     | ns   |
| F1                 | $t_w(clkL)$ | Typical pulse duration, output clock GPMC_CLK low  | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1 | -0.3+0.4<br>75°P <sup>(15)</sup> |     | ns   |

| NO. <sup>(2)</sup> | PARAMETER                     | DESCRIPTION                                                                                                                                                                  | MODE <sup>(19)</sup>                                                              | MIN                    | MAX                   | UNIT |
|--------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|------------------------|-----------------------|------|
| F2                 | $t_{d(\text{clkH-csnV})}$     | Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CS[n] transition <sup>(14)</sup>                                                                    | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.2+F <sup>(6)</sup>  | 4.5+F <sup>(6)</sup>  | ns   |
| F3                 | $t_{d(\text{clkH-csnIV})}$    | Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CS[n] invalid <sup>(14)</sup>                                                                       | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.2+E <sup>(5)</sup>  | 4.5+E <sup>(5)</sup>  | ns   |
| F4                 | $t_{d(aV-clk)}$               | Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge                                                                                            | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1                    | -2.3+B <sup>(2)</sup>  | 4.5+B <sup>(2)</sup>  | ns   |
| F5                 | $t_{d(\text{clkH-aIV})}$      | Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid                                                                                         | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1                    | -2.3                   | 4.5                   | ns   |
| F6                 | $t_{d(\text{be[x]nV-clk})}$   | Delay time, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n valid to output clock GPMC_CLK first edge                    | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1                    | -2.3+B <sup>(2)</sup>  | 1.9+B <sup>(2)</sup>  | ns   |
| F7                 | $t_{d(\text{clkH-be[x]nIV})}$ | Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n invalid <sup>(11)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1                    | -2.3+D <sup>(4)</sup>  | 1.9+D <sup>(4)</sup>  | ns   |
| F7                 | $t_{d(\text{clkL-be[x]nIV})}$ | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid <sup>(12)</sup>                                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1                    | -2.3+D <sup>(4)</sup>  | 1.9+D <sup>(4)</sup>  | ns   |
| F7                 | $t_{d(\text{clkL-be[x]nIV})}$ | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid <sup>(13)</sup>                                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1                    | -2.3+D <sup>(4)</sup>  | 1.9+D <sup>(4)</sup>  | ns   |
| F8                 | $t_{d(\text{clkH-advn})}$     | Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE transition                                                      | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.3+G <sup>(7)</sup>  | 4.5+G <sup>(7)</sup>  | ns   |
| F9                 | $t_{d(\text{clkH-advnIV})}$   | Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE invalid                                                         | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.3+D <sup>(4)</sup>  | 4.5+D <sup>(4)</sup>  | ns   |
| F10                | $t_{d(\text{clkH-oen})}$      | Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition                                                                                       | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.3H <sup>(8)</sup>   | 3.5+H <sup>(8)</sup>  | ns   |
| F11                | $t_{d(\text{clkH-oenIV})}$    | Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn invalid                                                                                          | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.3+E <sup>(8)</sup>  | 3.5+E <sup>(8)</sup>  | ns   |
| F14                | $t_{d(\text{clkH-wen})}$      | Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition                                                                                     | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.3+I <sup>(9)</sup>  | 4.5+I <sup>(9)</sup>  | ns   |
| F15                | $t_{d(\text{clkH-do})}$       | Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[15:0] transition <sup>(11)</sup>                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1                    | -2.3+J <sup>(10)</sup> | 2.7+J <sup>(10)</sup> | ns   |
| F15                | $t_{d(\text{clkL-do})}$       | Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition <sup>(12)</sup>                                                                                       | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1                    | -2.3+J <sup>(10)</sup> | 2.7+J <sup>(10)</sup> | ns   |
| F15                | $t_{d(\text{clkL-do})}$       | Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition <sup>(13)</sup>                                                                                       | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1                    | -2.3+J <sup>(10)</sup> | 2.7+J <sup>(10)</sup> | ns   |
| F17                | $t_{d(\text{clkH-be[x]n})}$   | Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition <sup>(11)</sup>                                  | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1                    | -2.3+J <sup>(10)</sup> | 1.9+J <sup>(10)</sup> | ns   |

| NO. <sup>(2)</sup> | PARAMETER                   | DESCRIPTION                                                                                                             | MODE <sup>(19)</sup>                                           | MIN                       | MAX                   | UNIT |
|--------------------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------|---------------------------|-----------------------|------|
| F17                | $t_{d(\text{clkL-be}[x]n)}$ | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition <sup>(12)</sup>                                | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1 | -2.3+J<br><sup>(10)</sup> | 1.9+J <sup>(10)</sup> | ns   |
| F17                | $t_{d(\text{clkL-be}[x]n)}$ | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition <sup>(13)</sup>                                | div_by_1_mode;<br>GPMC_FCLK_MUX_100;<br>TIMEPARAGRANULARITY_X1 | -2.3+J<br><sup>(10)</sup> | 1.9+J <sup>(10)</sup> | ns   |
| F18                | $t_{w(\text{csnV})}$        | Pulse duration, output chip select GPMC_CS[n] low <sup>(14)</sup>                                                       | Read                                                           | 0+A <sup>(1)</sup>        |                       | ns   |
|                    |                             |                                                                                                                         | Write                                                          | 0+A <sup>(1)</sup>        |                       | ns   |
| F19                | $t_{w(\text{be}[x]nV)}$     | Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low | Read                                                           | 0+C <sup>(3)</sup>        |                       | ns   |
|                    |                             |                                                                                                                         | Write                                                          | 0+C <sup>(3)</sup>        |                       | ns   |
| F20                | $t_{w(\text{advnV})}$       | Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low                                         | Read                                                           | 0+K <sup>(16)</sup>       |                       | ns   |
|                    |                             |                                                                                                                         | Write                                                          | 0+K <sup>(16)</sup>       |                       | ns   |

- (1) For single read:  $A = (\text{CSRdOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
For burst read:  $A = (\text{CSRdOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
For burst write:  $A = (\text{CSWrOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
With n being the page burst access number.
- (2)  $B = \text{ClkActivationTime} \times \text{GPMC\_FCLK}^{(17)}$
- (3) For single read:  $C = \text{RdCycleTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
For burst read:  $C = (\text{RdCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
For burst write:  $C = (\text{WrCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
With n being the page burst access number.
- (4) For single read:  $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
For burst read:  $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
For burst write:  $D = (\text{WrCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$
- (5) For single read:  $E = (\text{CSRdOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
For burst read:  $E = (\text{CSRdOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
For burst write:  $E = (\text{CSWrOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$
- (6) For csn falling edge (CS activated):
- Case GpmcFCLKDivider = 0:
    - $F = 0.5 \times \text{CSExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
  - Case GpmcFCLKDivider = 1:
    - $F = 0.5 \times \text{CSExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
    - $F = (1 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
  - Case GpmcFCLKDivider = 2:
    - $F = 0.5 \times \text{CSExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((CSOnTime - ClkActivationTime) is a multiple of 3)
    - $F = (1 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
    - $F = (2 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)
- (7) For ADV falling edge (ADV activated):
- Case GpmcFCLKDivider = 0:
    - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
  - Case GpmcFCLKDivider = 1:
    - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
    - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
  - Case GpmcFCLKDivider = 2:
    - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
    - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
    - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)
- For ADV rising edge (ADV deactivated) in Reading mode:
- Case GpmcFCLKDivider = 0:
    - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
  - Case GpmcFCLKDivider = 1:

- $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
- $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GpmcFCLKDivider = 2:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

- Case GpmcFCLKDivider = 0:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GpmcFCLKDivider = 1:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GpmcFCLKDivider = 2:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GpmcFCLKDivider = 0:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GpmcFCLKDivider = 1:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GpmcFCLKDivider = 2:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((OEOnTime - ClkActivationTime) is a multiple of 3)
  - $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $H = (2 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

For OE rising edge (OE deactivated):

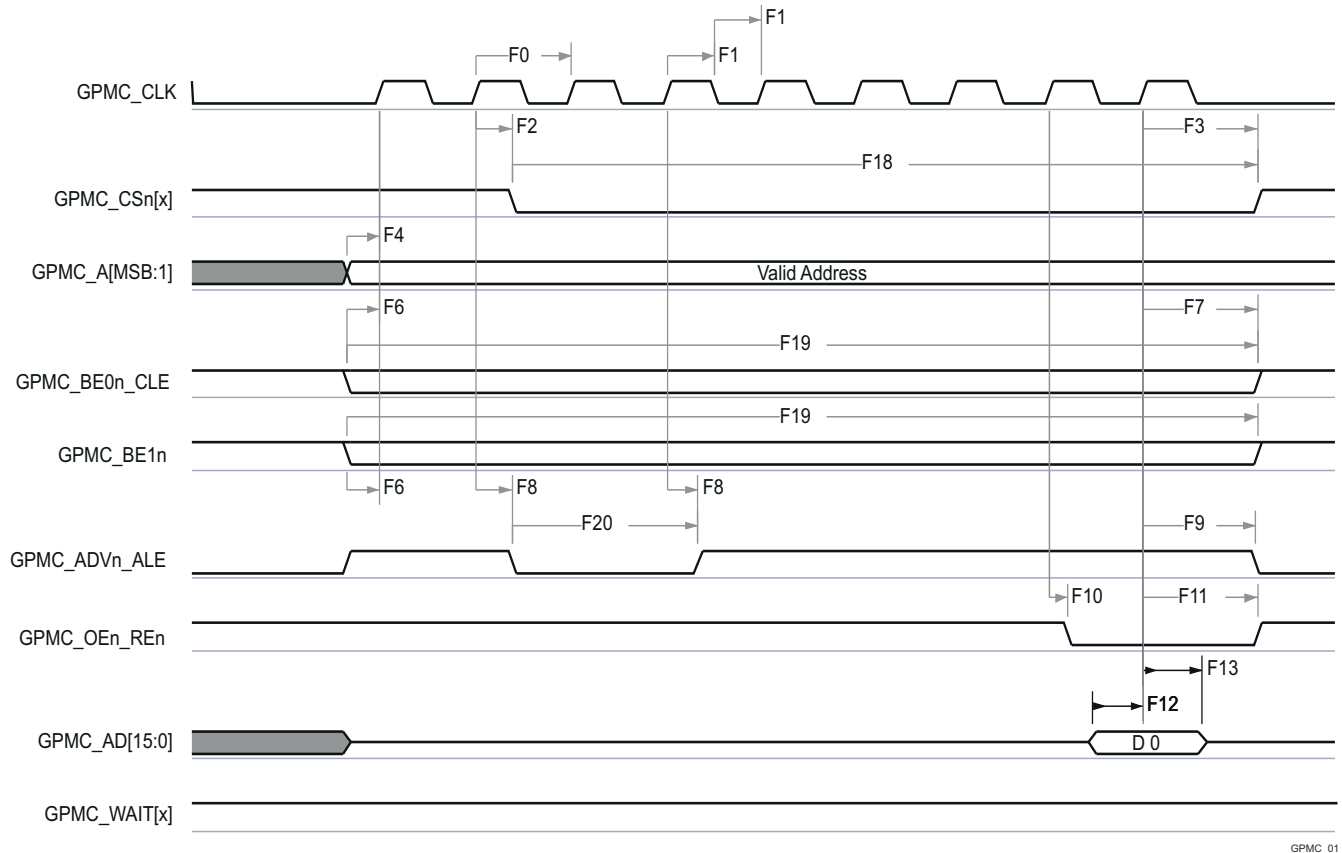
- Case GpmcFCLKDivider = 0:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GpmcFCLKDivider = 1:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GpmcFCLKDivider = 2:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((OEOffTime - ClkActivationTime) is a multiple of 3)
  - $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $H = (2 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

(9) For WE falling edge (WE activated):

- Case GpmcFCLKDivider = 0:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GpmcFCLKDivider = 1:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  - $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GpmcFCLKDivider = 2:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOnTime - ClkActivationTime) is a multiple of 3)
  - $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $I = (2 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)

For WE rising edge (WE deactivated):

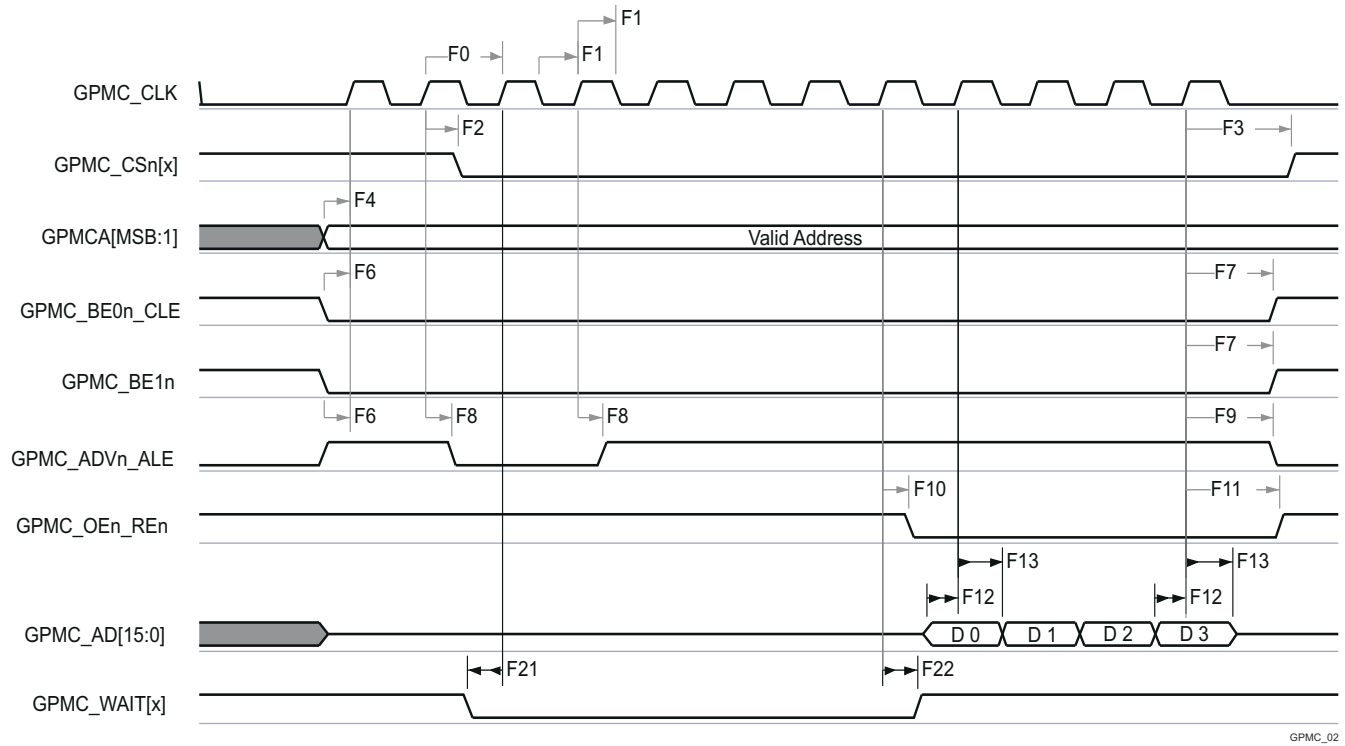
- Case GpmcFCLKDivider = 0:
    - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
  - Case GpmcFCLKDivider = 1:
    - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
    - $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
  - Case GpmcFCLKDivider = 2:
    - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOffTime - ClkActivationTime) is a multiple of 3)
    - $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
    - $I = (2 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)
- (10)  $J = \text{GPMC\_FCLK}^{(17)}$
- (11) First transfer only for CLK DIV 1 mode.
- (12) Half cycle; for all data after initial transfer for CLK DIV 1 mode.
- (13) Half cycle of GPMC\_CLK\_OUT; for all data for modes other than CLK DIV 1 mode. GPMC\_CLK\_OUT divide down from GPMC\_FCLK.
- (14) In GPMC\_CS[n], x is equal to 0, 1, 2 or 3. In GPMC\_WAIT[x], x is equal to 0 or 1.
- (15)  $P = \text{GPMC\_CLK}$  period in ns
- (16) For read:  $K = (\text{ADVrdOffTime} - \text{ADVOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
For write:  $K = (\text{ADVWrOffTime} - \text{ADVOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$
- (17) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.
- (18) Related to the GPMC\_CLK output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC\_CONFIG1\_CSx configuration register bit field GpmcFCLKDivider.
- (19) For div\_by\_1\_mode:
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
    - GPMC\_CLK frequency = GPMC\_FCLK frequency
- For GPMC\_FCLK\_MUX\_100:
- $\text{gpmc\_fclk\_sel}[1:0] = 01 = \text{PER1\_PLL\_CLKOUT} / 3 = 300 / 3 = 100\text{MHz}$
- For TIMEPARAGRANULARITY\_X1:
- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)
- For no extra\_delay:
- GPMC\_CONFIG2\_i Register : CSEXTRADELAY = 0h = CS i Timing control signal is not delayed
  - GPMC\_CONFIG4\_i Register : WEEXTRADELAY = 0h = nWE timing control signal is not delayed
  - GPMC\_CONFIG4\_i Register : OEEXTRADELAY = 0h = nOE timing control signal is not delayed
  - GPMC\_CONFIG3\_i Register: ADVEXTRADELAY = 0h = nADV timing control signal is not delayed



GPMC\_01

- A. In GPMC\_CS[n], x is equal to 0, 1, 2 or 3.  
 B. In GPMC\_WAIT[x], x is equal to 0 or 1.

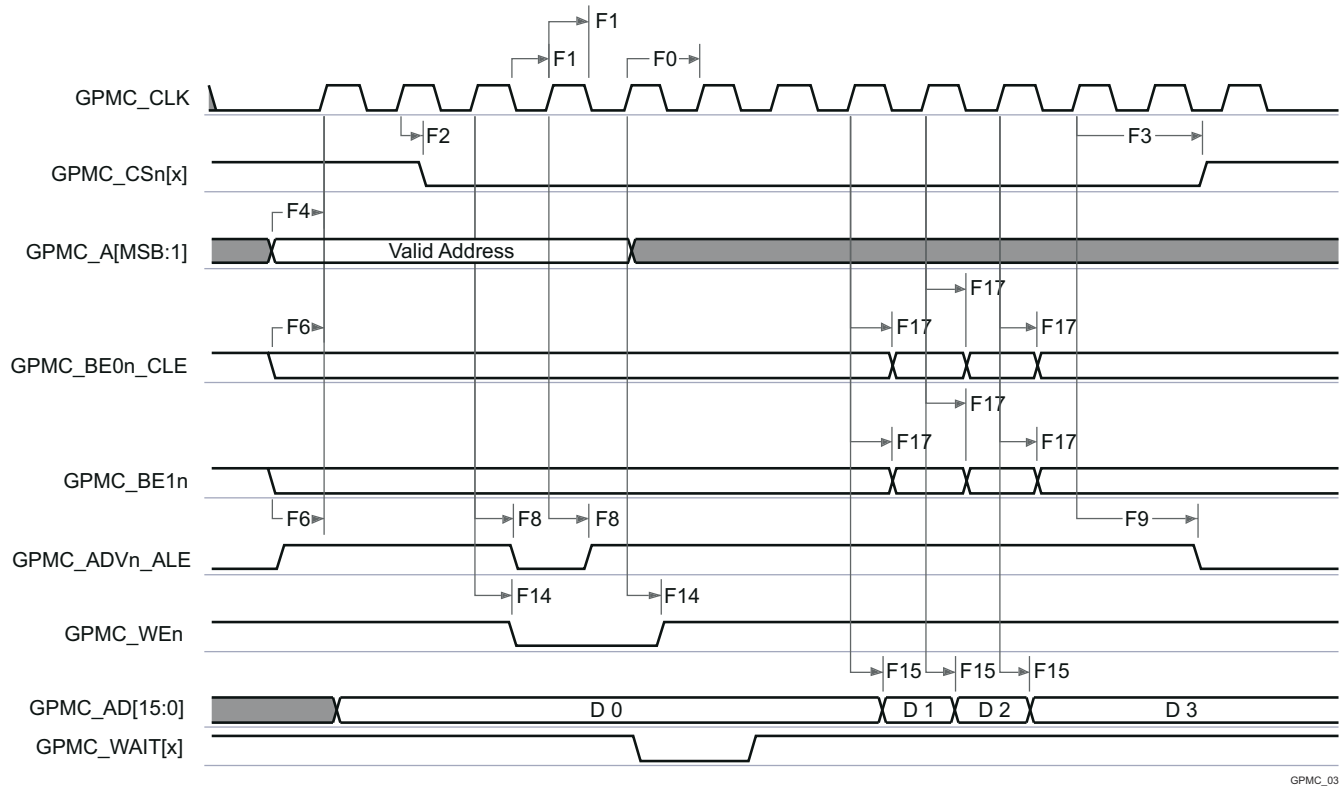
**Figure 6-48. GPMC and NOR Flash—Synchronous Single Read—(GpmcFCLKDivider = 0)**



- A. In GPMC\_CS[x], x is equal to 0, 1, 2 or 3.  
B. In GPMC\_WAIT[x], x is equal to 0 or 1.

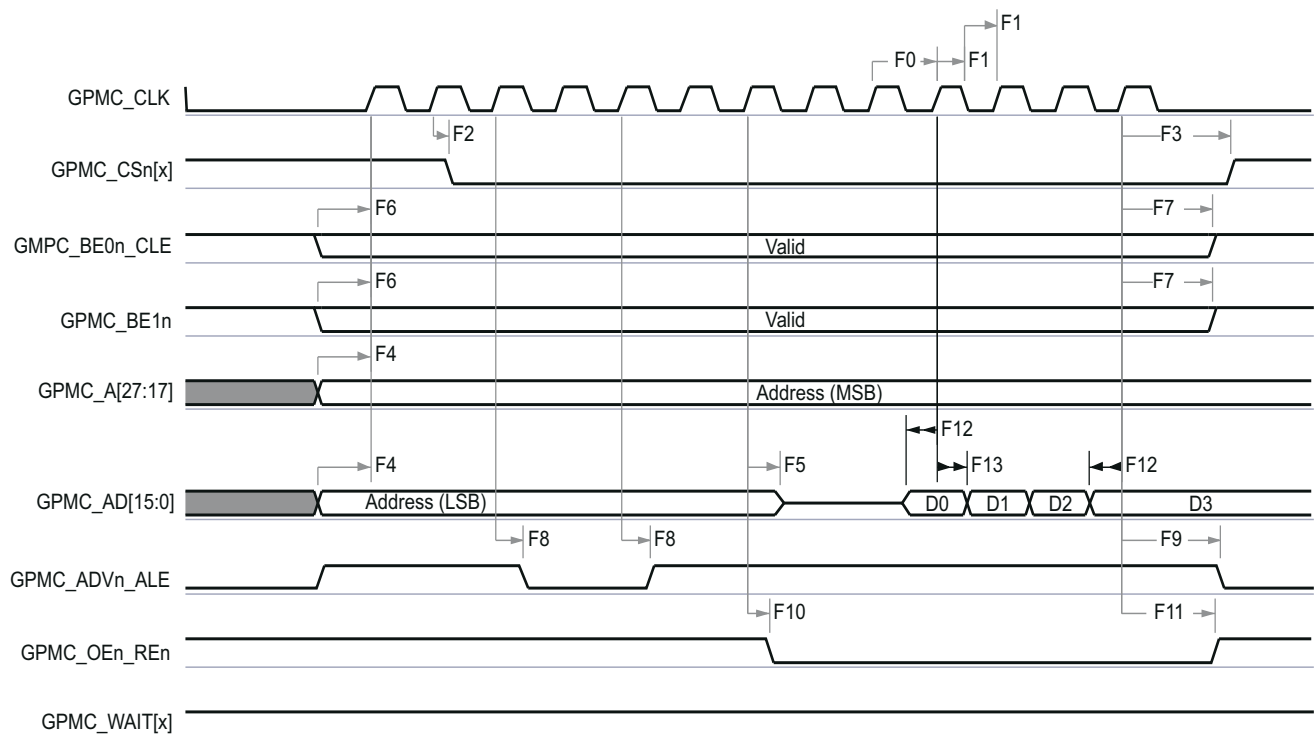
**Figure 6-49. GPMC and NOR Flash—Synchronous Burst Read—4x16-bit (GpmcCLKDivider = 0)**





GPMC\_03

**Figure 6-50. GPMC and NOR Flash—Synchronous Burst Write—(GpmcFCLKDivider > 0)**

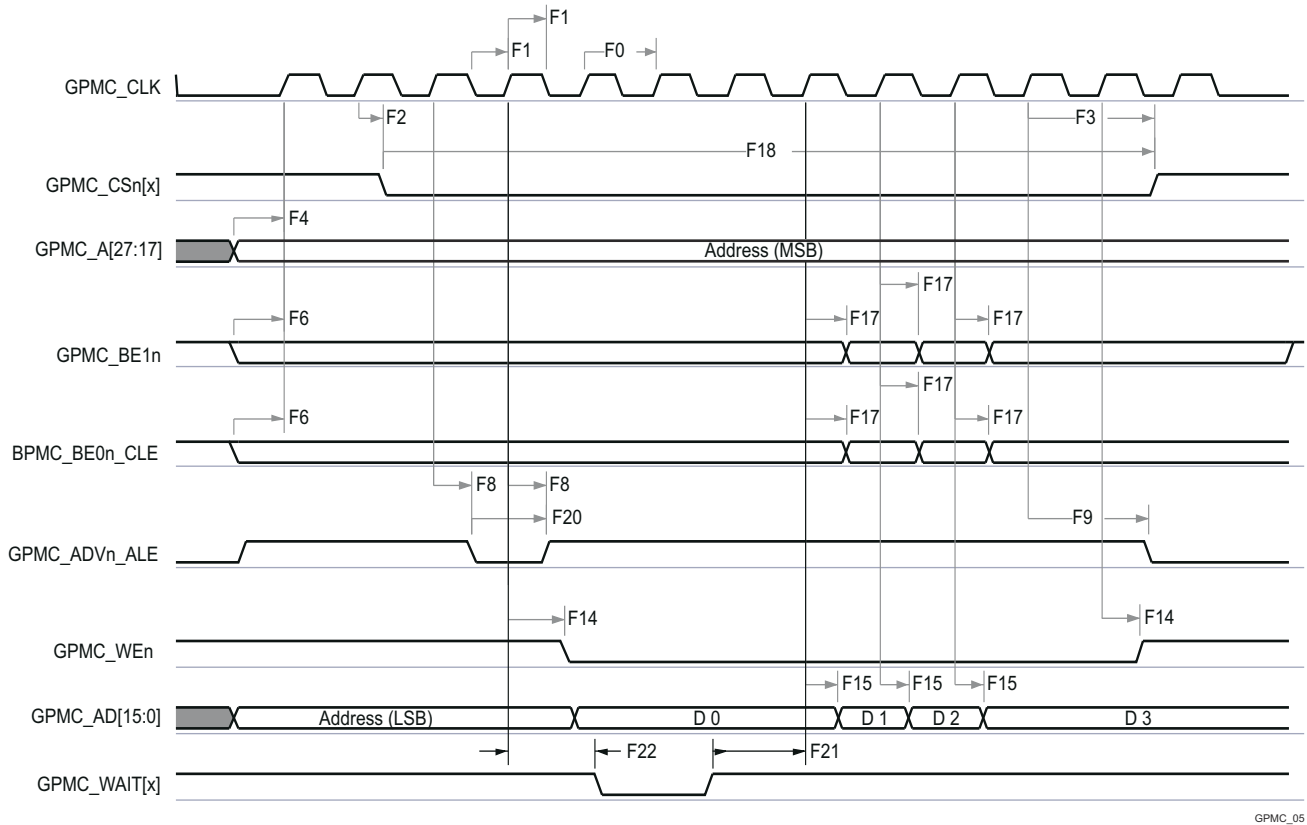


GPMC\_04

- A. In GPMC\_CS[n], x is equal to 0, 1, 2 or 3.

B. In GPMC\_WAIT[x], x is equal to 0 or 1.

**Figure 6-51. GPMC and Multiplexed NOR Flash—Synchronous Burst Read**



GPMC\_05

A. In GPMC\_CS[x], x is equal to 0, 1, 2 or 3.

B. In GPMC\_WAIT[x], x is equal to 0 or 1.

**Figure 6-52. GPMC and Multiplexed NOR Flash—Synchronous Burst Write**

#### 6.9.5.10.2 GPMC and NOR Flash—Asynchronous Mode

Section 6.9.5.10.2.1 and Section 6.9.5.10.2.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-53 through Figure 6-58).

##### 6.9.5.10.2.1 GPMC and NOR Flash Timing Requirements—Asynchronous Mode

| NO.                 | PARAMETER            | DESCRIPTION                           | MODE                                                           | MIN | MAX              | UNIT |
|---------------------|----------------------|---------------------------------------|----------------------------------------------------------------|-----|------------------|------|
| FA5 <sup>(1)</sup>  | $t_{acc(d)}$         | Data access time                      | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 |     | H <sup>(4)</sup> | ns   |
| FA20 <sup>(2)</sup> | $t_{acc1-pgmode(d)}$ | Page mode successive data access time | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 |     | P <sup>(3)</sup> | ns   |
| FA21 <sup>(1)</sup> | $t_{acc2-pgmode(d)}$ | Page mode first data access time      | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 |     | H <sup>(4)</sup> | ns   |

- (1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
- (2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
- (3)  $P = \text{PageBurstAccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(5)}$

(4)  $H = \text{AccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(5)}$

(5) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

#### 6.9.5.10.2.2 GPMC and NOR Flash Switching Characteristics—Asynchronous Mode

| NO.  | PARAMETER                    | DESCRIPTION                                                                                                                                                                  | MODE <sup>(15)</sup>                                           | MIN                  | MAX                 | UNIT |
|------|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------|----------------------|---------------------|------|
| FA0  | $t_{w(\text{be}[x]nV)}$      | Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time                                               | Read                                                           | 0+N <sup>(12)</sup>  |                     | ns   |
|      |                              |                                                                                                                                                                              | Write                                                          | 0+N <sup>(12)</sup>  |                     |      |
| FA1  | $t_{w(\text{csnV})}$         | Pulse duration, output chip select GPMC_CS[n] <sup>(13)</sup> low                                                                                                            | Read                                                           | 0+A <sup>(1)</sup>   |                     | ns   |
|      |                              |                                                                                                                                                                              | Write                                                          | 0+A <sup>(1)</sup>   |                     |      |
| FA3  | $t_{d(\text{csnV-advnIV})}$  | Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output address valid and address latch enable GPMC_ADVn_ALE invalid                                       | Read                                                           | -2+B <sup>(2)</sup>  | 2+B <sup>(2)</sup>  | ns   |
|      |                              |                                                                                                                                                                              | Write                                                          | -2+B <sup>(2)</sup>  | 2+B <sup>(2)</sup>  |      |
| FA4  | $t_{d(\text{csnV-oenIV})}$   | Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output enable GPMC_OEn_REn invalid (Single read)                                                          | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+C <sup>(3)</sup>  | 2+C <sup>(3)</sup>  | ns   |
| FA9  | $t_{d(\text{aV-csnV})}$      | Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CS[n] <sup>(13)</sup> valid                                                                         | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+J <sup>(9)</sup>  | 2+J <sup>(9)</sup>  | ns   |
| FA10 | $t_{d(\text{be}[x]nV-csnV)}$ | Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CS[n] <sup>(13)</sup> valid | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+J <sup>(9)</sup>  | 2+J <sup>(9)</sup>  | ns   |
| FA12 | $t_{d(\text{csnV-advnV})}$   | Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output address valid and address latch enable GPMC_ADVn_ALE valid                                         | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+K <sup>(10)</sup> | 2+K <sup>(10)</sup> | ns   |
| FA13 | $t_{d(\text{csnV-oenV})}$    | Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output enable GPMC_OEn_REn valid                                                                          | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+L <sup>(11)</sup> | 2+L <sup>(11)</sup> | ns   |
| FA16 | $t_{w(\text{aIV})}$          | Pulse duration output address GPMC_A[26:1] invalid between 2 successive read and write accesses                                                                              | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | 0+G <sup>(7)</sup>   |                     | ns   |
| FA18 | $t_{d(\text{csnV-oenIV})}$   | Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output enable GPMC_OEn_REn invalid (Burst read)                                                           | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+I <sup>(8)</sup>  | 2+I <sup>(8)</sup>  | ns   |
| FA20 | $t_{w(\text{aV})}$           | Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses                                                                                               | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | 0+D <sup>(4)</sup>   |                     | ns   |
| FA25 | $t_{d(\text{csnV-wenV})}$    | Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output write enable GPMC_WEn valid                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+E <sup>(5)</sup>  | 2+E <sup>(5)</sup>  | ns   |
| FA27 | $t_{d(\text{csnV-wenIV})}$   | Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output write enable GPMC_WEn invalid                                                                      | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+F <sup>(6)</sup>  | 2+F <sup>(6)</sup>  | ns   |
| FA28 | $t_{d(\text{wenV-dV})}$      | Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid                                                                                            | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 |                      | 2.8                 | ns   |
| FA29 | $t_{d(\text{dV-csnV})}$      | Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CS[n] <sup>(13)</sup> valid                                                                           | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+J <sup>(9)</sup>  | 2+J <sup>(9)</sup>  | ns   |
| FA37 | $t_{d(\text{oenV-aIV})}$     | Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end                                                                                       | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 |                      | 2.8                 | ns   |

(1) For single read:  $A = (\text{CSRdOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$

For single write:  $A = (\text{CSWrOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$

For burst read:  $A = (\text{CSRdOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$

For burst write:  $A = (\text{CSWrOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$

with n being the page burst access number

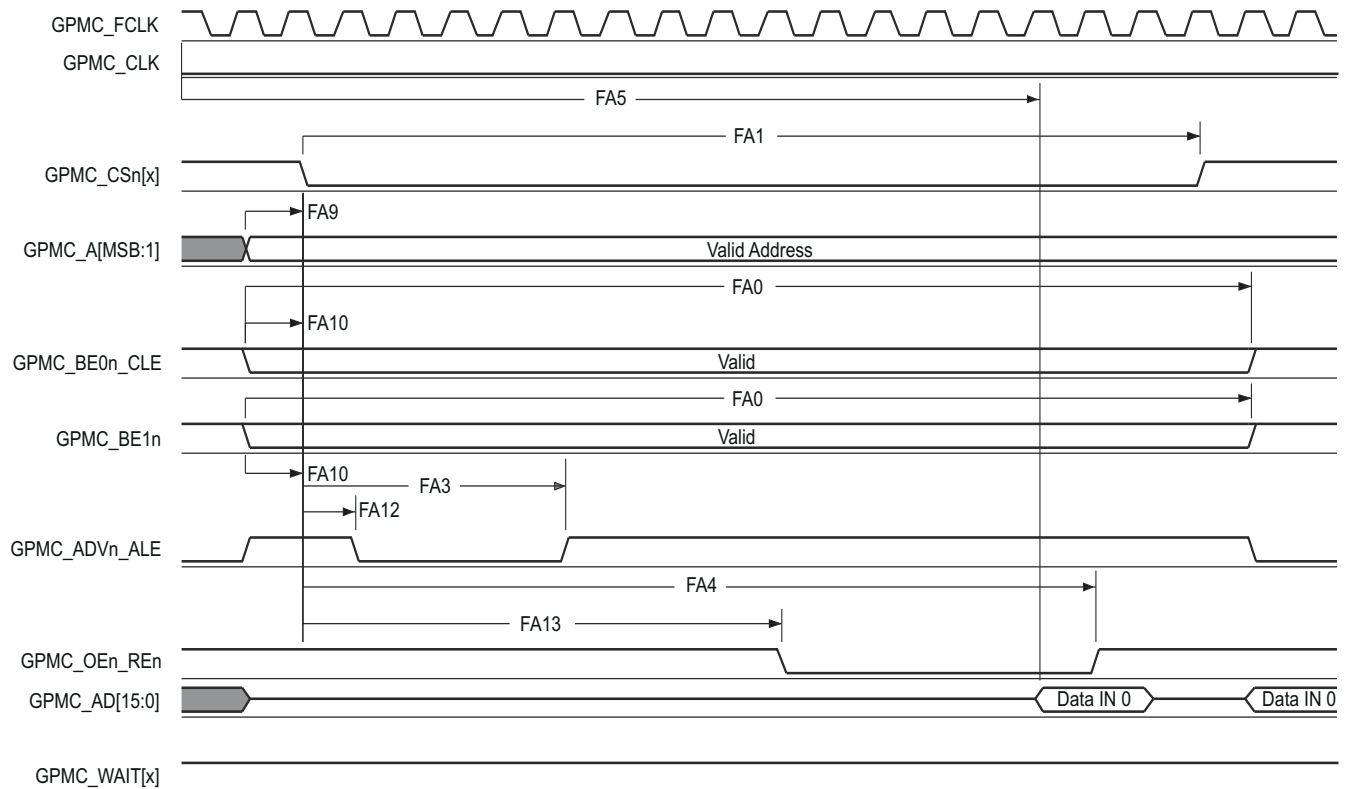
- (2) For reading:  $B = ((\text{ADVRdOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{ADVExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}^{(14)}$   
For writing:  $B = ((\text{ADVWrOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{ADVExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}^{(14)}$
- (3)  $C = ((\text{OEOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{OEExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}^{(14)}$
- (4)  $D = \text{PageBurstAccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$
- (5)  $E = ((\text{WEOnTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{WEEExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}^{(14)}$
- (6)  $F = ((\text{WEOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{WEEExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}^{(14)}$
- (7)  $G = \text{Cycle2CycleDelay} \times \text{GPMC\_FCLK}^{(14)}$
- (8)  $I = ((\text{OEOffTime} + (n - 1) \times \text{PageBurstAccessTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{OEExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}^{(14)}$
- (9)  $J = (\text{CSOnTime} \times (\text{TimeParaGranularity} + 1) + 0.5 \times \text{CSEExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$
- (10)  $K = ((\text{ADVOnTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{ADVExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}^{(14)}$
- (11)  $L = ((\text{OEOnTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{OEExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}^{(14)}$
- (12) For single read:  $N = \text{RdCycleTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
For single write:  $N = \text{WrCycleTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
For burst read:  $N = (\text{RdCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
For burst write:  $N = (\text{WrCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$
- (13) In GPMC\_CS[n], n is equal to 0, 1, 2 or 3.
- (14) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.
- (15) For div\_by\_1\_mode:
  - GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
    - GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX\_133:

  - gpmc\_fclk\_sel[1:0] = 00 = CPSWHSDIV\_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY\_X1:

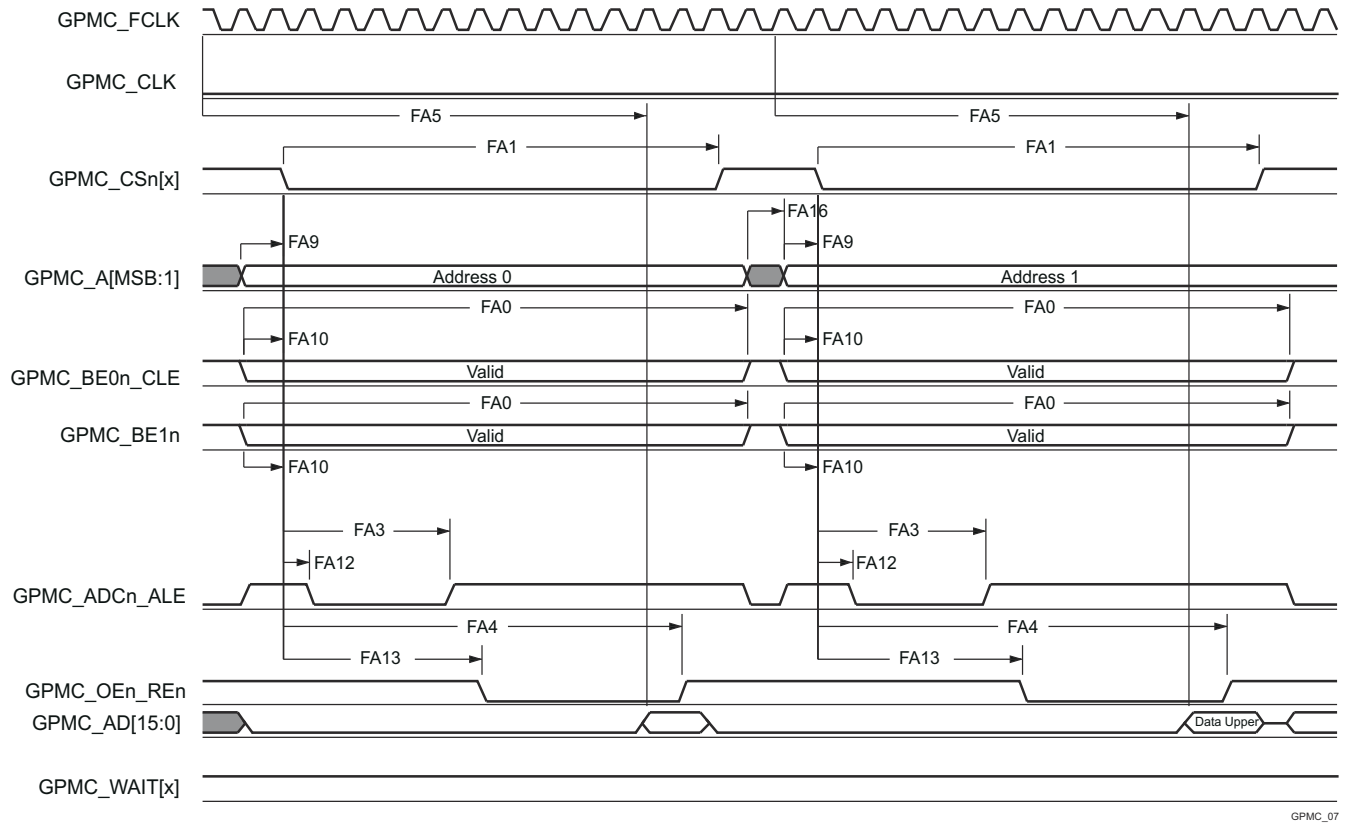
  - GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



GPMC\_06

- In GPMC\_CS[x], x is equal to 0, 1, 2 or 3. In GPMC\_WAIT[x], x is equal to 0 or 1.
- FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

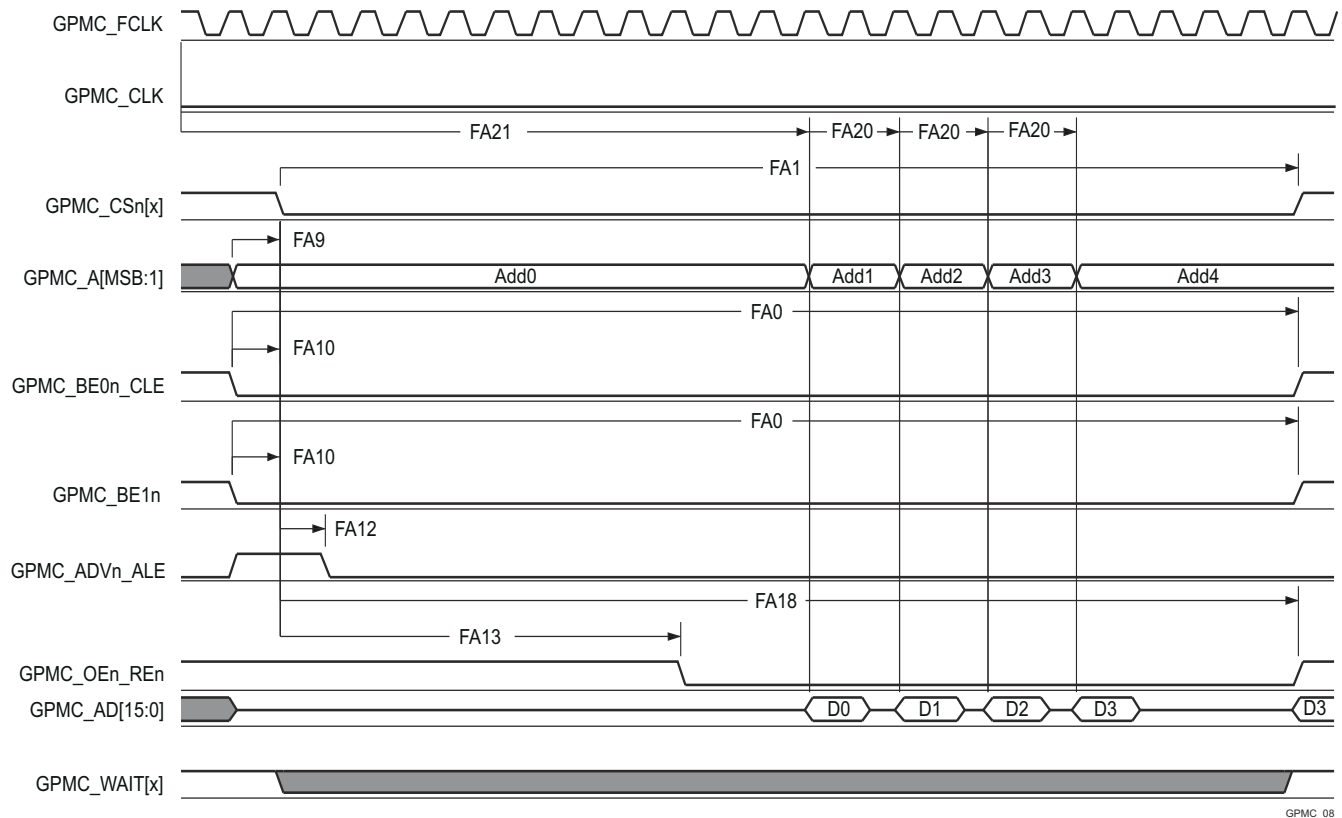
**Figure 6-53. GPMC and NOR Flash—Asynchronous Read—Single Word**



GPMC\_07

- In GPMC\_CS[x], x is equal to 0, 1, 2 or 3. In GPMC\_WAIT[x], x is equal to 0 or 1.
- FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

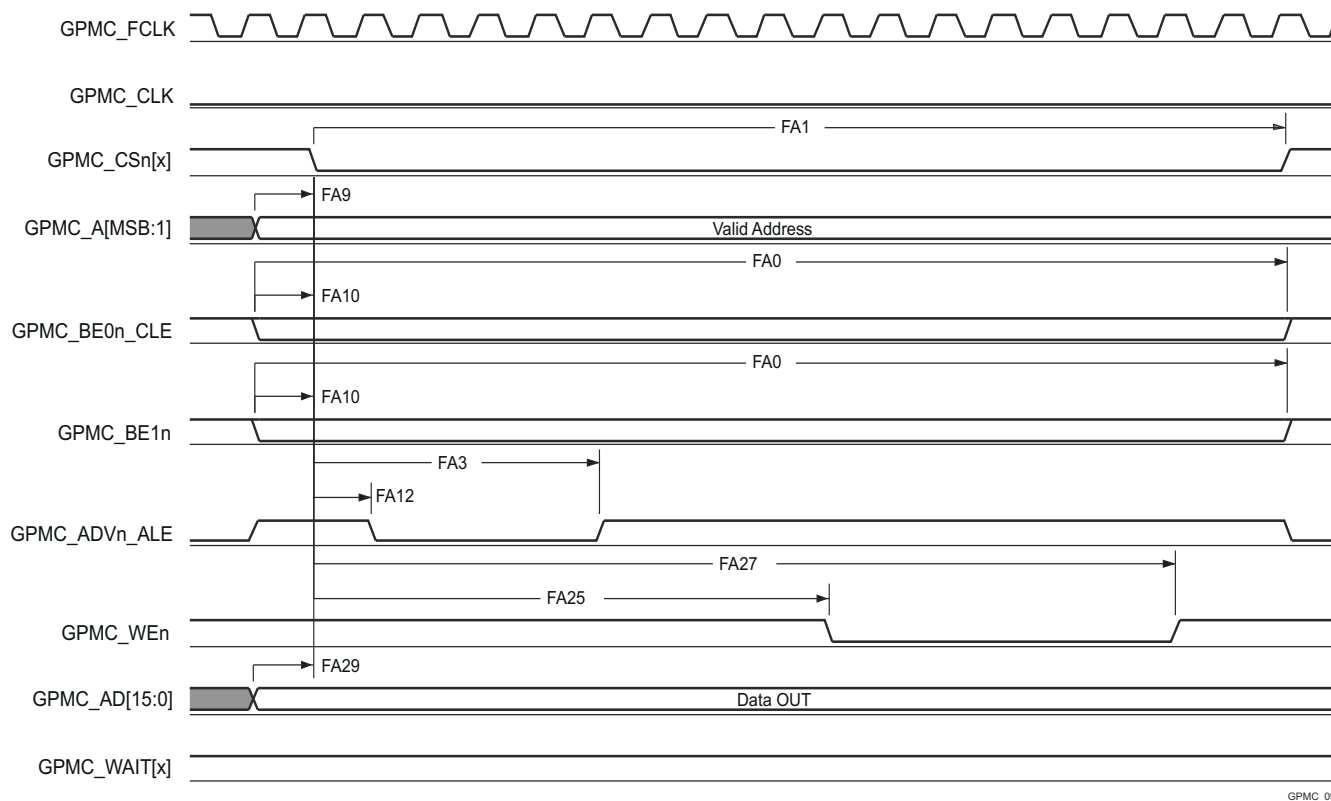
**Figure 6-54. GPMC and NOR Flash—Asynchronous Read—32-Bit**



GPMC\_08

- In GPMC\_CS[x], x is equal to 0, 1, 2 or 3. In GPMC\_WAIT[x], x is equal to 0 or 1.
- FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.
- FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

**Figure 6-55. GPMC and NOR Flash—Asynchronous Read—Page Mode 4x16-Bit**

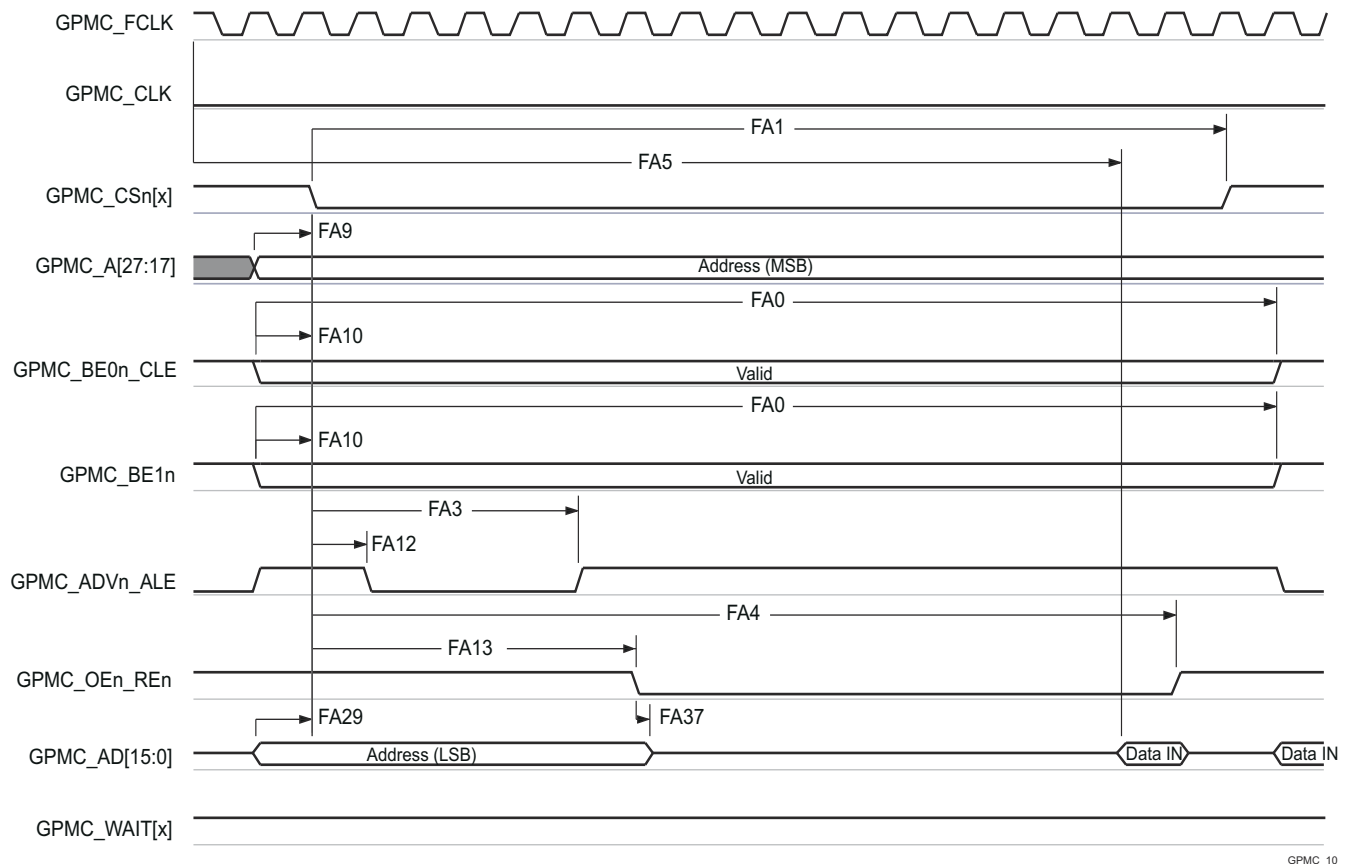


GPMC\_09

A. In GPMC\_CS[n], x is equal to 0, 1, 2 or 3. In GPMC\_WAIT[x], x is equal to 0 or 1.

**Figure 6-56. GPMC and NOR Flash—Asynchronous Write—Single Word**

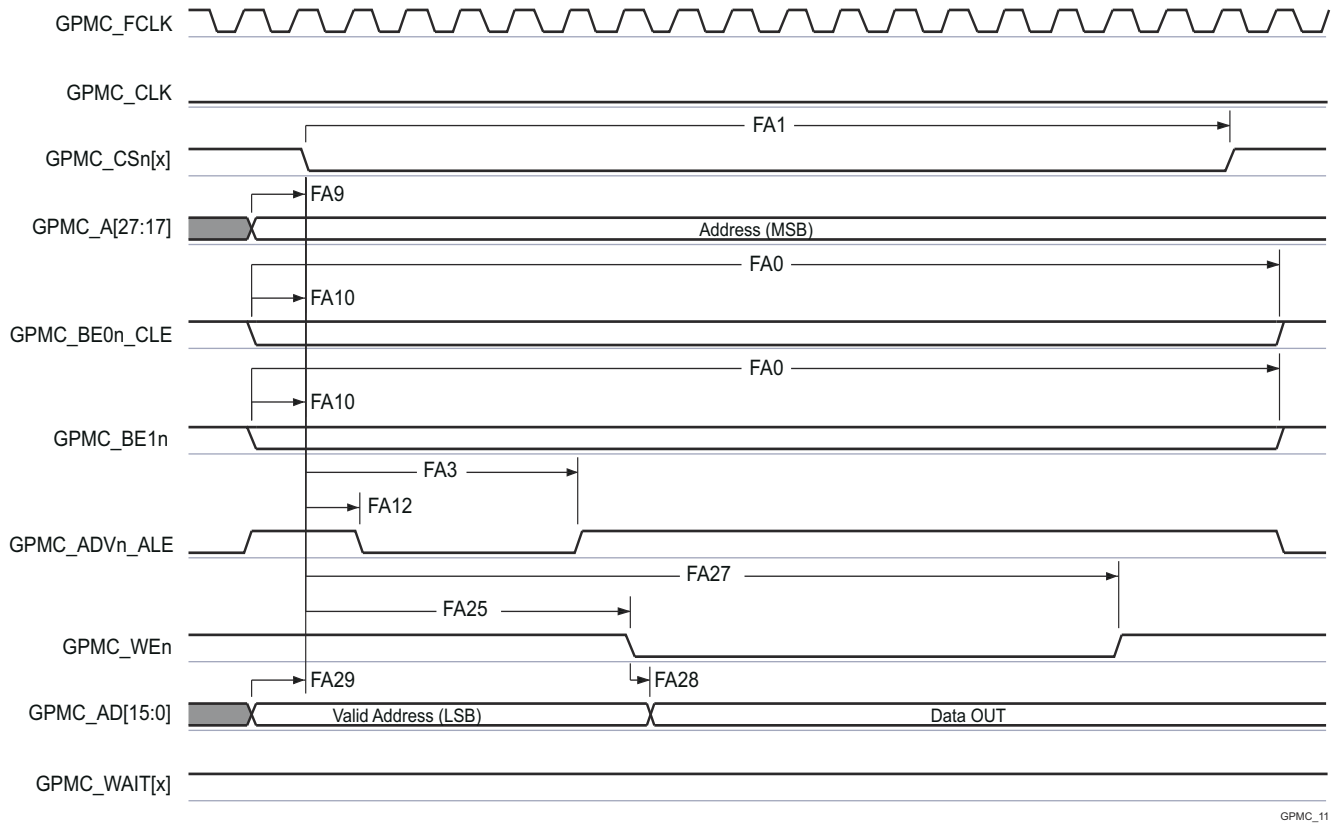




GPMC\_10

- In GPMC\_CS[n], x is equal to 0, 1, 2 or 3. In GPMC\_WAIT[x], x is equal to 0 or 1.
- FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

**Figure 6-57. GPMC and Multiplexed NOR Flash—Asynchronous Read—Single Word**



A. In GPMC\_CS[n], x is equal to 0, 1, 2 or 3. In GPMC\_WAIT[x], x is equal to 0 or 1.

**Figure 6-58. GPMC and Multiplexed NOR Flash—Asynchronous Write—Single Word**

### 6.9.5.10.3 GPMC and NAND Flash—Asynchronous Mode

Section 6.9.5.10.3.1 and Section 6.9.5.10.3.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-59 through Figure 6-62).

#### 6.9.5.10.3.1 GPMC and NAND Flash Timing Requirements—Asynchronous Mode

| NO.                  | PARAMETER    | DESCRIPTION                                          | MODE <sup>(4)</sup>                                            | MIN | MAX              | UNIT |
|----------------------|--------------|------------------------------------------------------|----------------------------------------------------------------|-----|------------------|------|
| GNF12 <sup>(1)</sup> | $t_{acc(d)}$ | Access time, input data GPMC_AD[15:0] <sup>(3)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 |     | J <sup>(2)</sup> | ns   |

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.

(2)  $J = \text{AccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}$ <sup>(3)</sup>

(3) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

(4) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:  
– GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX\_133:

- gpmc\_fclk\_sel[1:0] = 00 = CPSWHS DIV\_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

#### 6.9.5.10.3.2 GPMC and NAND Flash Switching Characteristics—Asynchronous Mode

| NO.  | PARAMETER            | DESCRIPTION                                                                                                                 | MODE <sup>(15)</sup>                                           | MIN                 | MAX                  | UNIT |
|------|----------------------|-----------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------|---------------------|----------------------|------|
|      | $t_{R(d)}$           | Rise time, output data GPMC_AD[15:0]                                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 |                     | 2                    | ns   |
|      | $t_{F(d)}$           | Fall time, output data GPMC_AD[15:0]                                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 |                     | 2                    | ns   |
| GNF0 | $t_{w(wenV)}$        | Pulse duration, output write enable GPMC_WEn valid                                                                          | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | 0+A <sup>(1)</sup>  |                      | ns   |
| GNF1 | $t_{d(csnV-wenV)}$   | Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output write enable GPMC_WEn valid                       | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+B <sup>(2)</sup> | 2+B <sup>(2)</sup>   | ns   |
| GNF2 | $t_{w(cleH-wenV)}$   | Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE high to output write enable GPMC_WEn valid      | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+C <sup>(3)</sup> | 2+C <sup>(3)</sup>   | ns   |
| GNF3 | $t_{w(wenV-dV)}$     | Delay time, output data GPMC_AD[15:0] valid to output write enable GPMC_WEn valid                                           | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+D <sup>(4)</sup> | 2.8+D <sup>(4)</sup> | ns   |
| GNF4 | $t_{w(wenIV-dIV)}$   | Delay time, output write enable GPMC_WEn invalid to output data GPMC_AD[15:0] invalid                                       | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+E <sup>(5)</sup> | 2.8+E <sup>(5)</sup> | ns   |
| GNF5 | $t_{w(wenIV-cleIV)}$ | Delay time, output write enable GPMC_WEn invalid to output lower-byte enable and command latch enable GPMC_BE0n_CLE invalid | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+F <sup>(6)</sup> | 2+F <sup>(6)</sup>   | ns   |
| GNF6 | $t_{w(wenIV-csnIV)}$ | Delay time, output write enable GPMC_WEn invalid to output chip select GPMC_CS[n] <sup>(13)</sup> invalid                   | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+G <sup>(7)</sup> | 2+G <sup>(7)</sup>   | ns   |

| NO.   | PARAMETER            |                                                                                                                         | MODE <sup>(15)</sup>                                           | MIN                  | MAX                 | UNIT |
|-------|----------------------|-------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------|----------------------|---------------------|------|
| GNF7  | $t_{w(aleH-wenV)}$   | Delay time, output address valid and address latch enable GPMC_ADVn_ALE high to output write enable GPMC_WEn valid      | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+C <sup>(3)</sup>  | 2+C <sup>(3)</sup>  | ns   |
| GNF8  | $t_{w(wenIV-aleIV)}$ | Delay time, output write enable GPMC_WEn invalid to output address valid and address latch enable GPMC_ADVn_ALE invalid | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+F <sup>(6)</sup>  | 2+F <sup>(6)</sup>  | ns   |
| GNF9  | $t_{c(wen)}$         | Cycle time, write                                                                                                       | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 |                      | 0+H <sup>(8)</sup>  | ns   |
| GNF10 | $t_{d(csnV-oenV)}$   | Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output enable GPMC_OEn_REn valid                     | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+I <sup>(9)</sup>  | 2+I <sup>(9)</sup>  | ns   |
| GNF13 | $t_{w(oenV)}$        | Pulse duration, output enable GPMC_OEn_REn valid                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 |                      | 0+K <sup>(10)</sup> | ns   |
| GNF14 | $t_{c(oen)}$         | Cycle time, read                                                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | 0+L <sup>(11)</sup>  |                     | ns   |
| GNF15 | $t_{w(oenIV-csnIV)}$ | Delay time, output enable GPMC_OEn_REn invalid to output chip select GPMC_CS[n] <sup>(13)</sup> invalid                 | div_by_1_mode;<br>GPMC_FCLK_MUX_133;<br>TIMEPARAGRANULARITY_X1 | -2+M <sup>(12)</sup> | 2+M <sup>(12)</sup> | ns   |

- (1)  $A = (WEOffTime - WEOntime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
(2)  $B = ((WEOntime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(3)  $C = ((WEOntime - ADVOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - ADVExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(4)  $D = (WEOntime \times (TimeParaGranularity + 1) + 0.5 \times WEEExtraDelay) \times GPMC\_FCLK^{(14)}$   
(5)  $E = ((WrCycleTime - WEOffTime) \times (TimeParaGranularity + 1) - 0.5 \times WEEExtraDelay) \times GPMC\_FCLK^{(14)}$   
(6)  $F = ((ADVWrOffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - WEEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(7)  $G = ((CSWrOffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - WEEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(8)  $H = WrCycleTime \times (1 + TimeParaGranularity) \times GPMC\_FCLK^{(14)}$   
(9)  $I = ((OEOntime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(10)  $K = (OEOffTime - OEOntime) \times (1 + TimeParaGranularity) \times GPMC\_FCLK^{(14)}$   
(11)  $L = RdCycleTime \times (1 + TimeParaGranularity) \times GPMC\_FCLK^{(14)}$   
(12)  $M = ((CSRdOffTime - OEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - OEEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(13) In GPMC\_CS[n], x is equal to 0, 1, 2 or 3.  
(14) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.  
(15) For div\_by\_1\_mode:

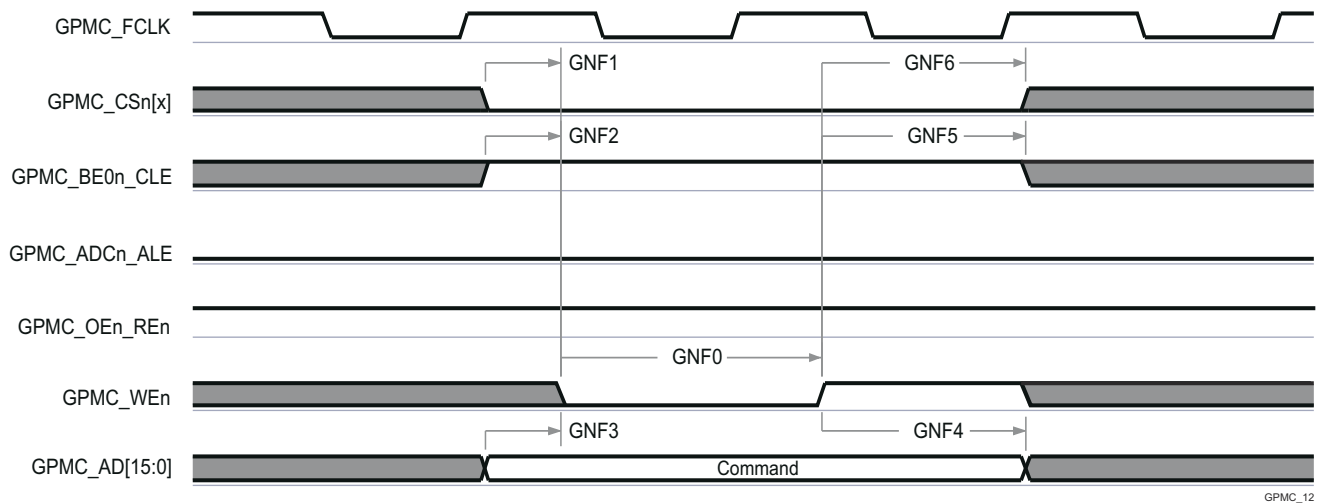
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:  
– GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX\_133:

- gpmc\_fclk\_sel[1:0] = 00 = CPSWHS DIV\_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY\_X1:

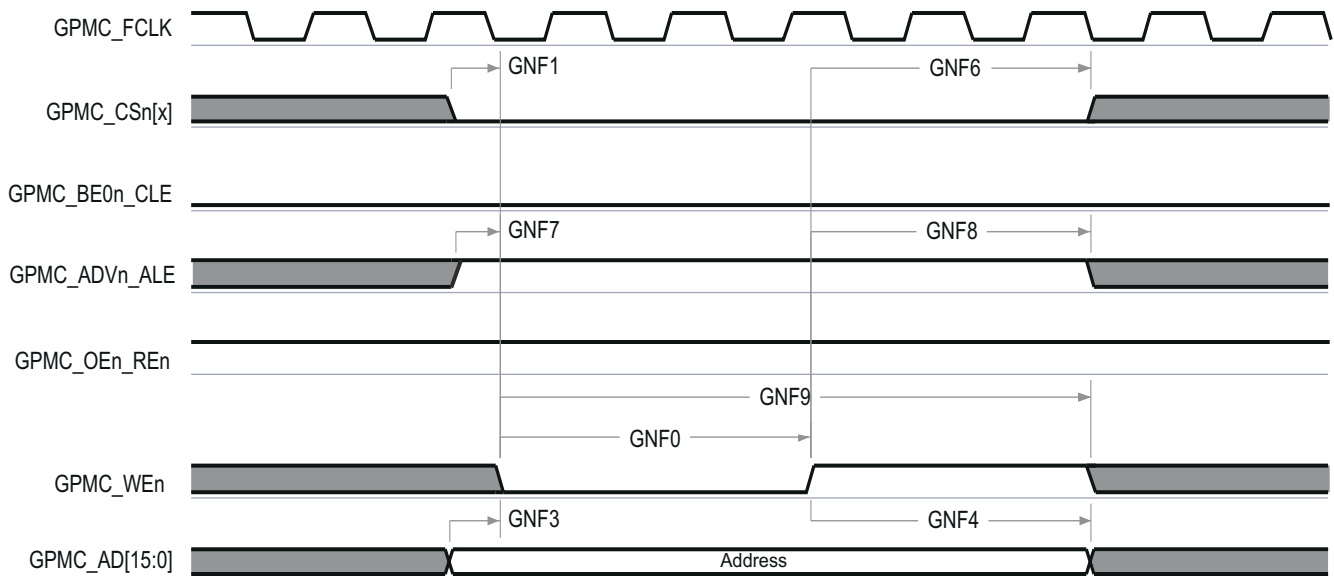
- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WR CYCLE TIME, RD/WR ACCESS TIME, PAGE BURST ACCESS TIME, CS ON TIME, CS RD/WROFF TIME, ADV ON TIME, ADV RD/WROFF TIME, OE ON TIME, OE OFF TIME, WE ON TIME, WE OFF TIME, CYCLE2CYCLE DELAY, BUSTURN AROUND, TIMEOUT START VALUE, WR DATA ON ADMUX BUS)



GPMC\_12

A. In GPMC\_CS[n], x is equal to 0, 1, 2 or 3.

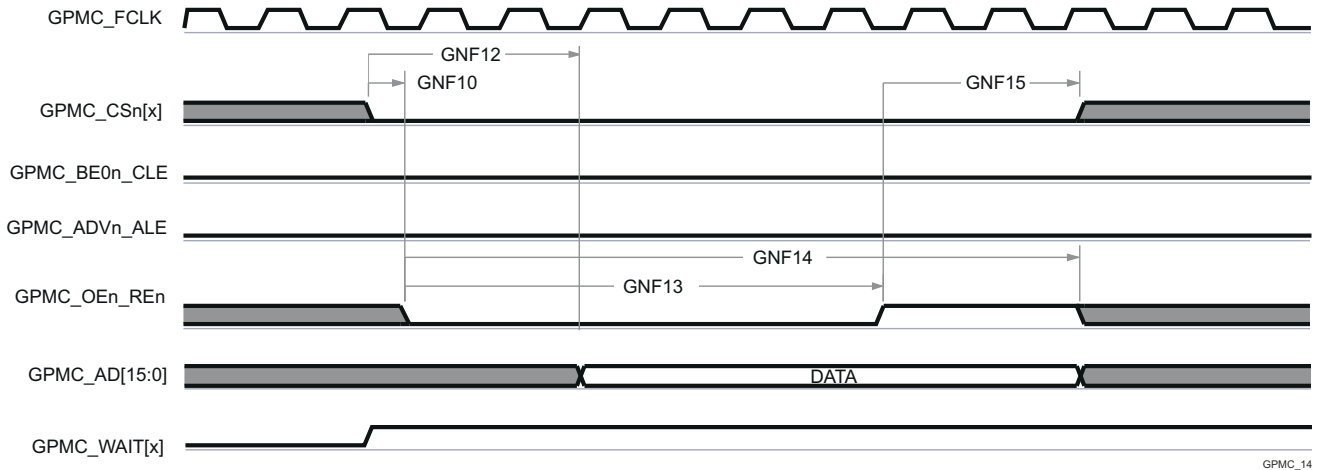
**Figure 6-59. GPMC and NAND Flash—Command Latch Cycle**



GPMC\_13

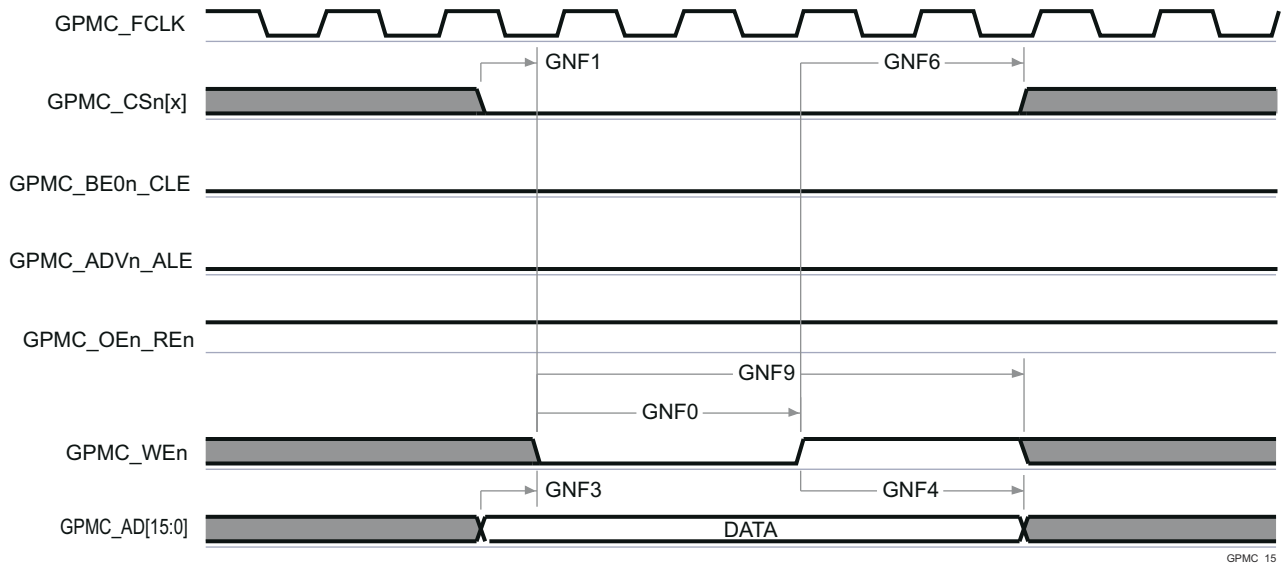
A. In GPMC\_CS[n], x is equal to 0, 1, 2 or 3.

**Figure 6-60. GPMC and NAND Flash—Address Latch Cycle**



- GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.
- In GPMC\_CS[n], x is equal to 0, 1, 2 or 3. In GPMC\_WAIT[x], x is equal to 0 or 1.

**Figure 6-61. GPMC and NAND Flash—Data Read Cycle**



- In GPMC\_CS[n], x is equal to 0, 1, 2 or 3.

**Figure 6-62. GPMC and NAND Flash—Data Write Cycle**

For more information, see section *General-Purpose Memory Controller (GPMC)* in the device TRM.

#### 6.9.5.11 HyperBus

##### Note

HyperBus is not available on this device.

For more details about features and additional description information on the device Hyperbus, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

[Section 6.9.5.11.1](#), [Section 6.9.5.11.2](#), and [Section 6.9.5.11.3](#) assume testing over the recommended operating conditions and electrical characteristic conditions (see [Figure 6-63](#), [Figure 6-64](#), and [Figure 6-65](#)).

Table 6-40 presents timing conditions for HyperBus.

**Table 6-40. HyperBus Timing Conditions**

| PARAMETER                             | DESCRIPTION                               | MIN                                | MAX | UNIT |
|---------------------------------------|-------------------------------------------|------------------------------------|-----|------|
| <b>INPUT CONDITIONS</b>               |                                           |                                    |     |      |
| SR <sub>i</sub>                       | Input slew rate                           | 2                                  | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                           |                                    |     |      |
| C <sub>L</sub>                        | Output load capacitance                   | 1.5                                | 10  | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                           |                                    |     |      |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch between traces | CK and CKn;<br>RWDS and DQ[7:0]    | 10  | ps   |
|                                       |                                           | CK/CKn and RWDS;<br>CK/CKn and CSn | 260 | ps   |
|                                       |                                           | CK/CKn and DQ[7:0]                 | 80  | ps   |
|                                       |                                           | RESETn and CSn[1:0]                | 340 | ps   |

#### 6.9.5.11.1 Timing Requirements for HyperBus Initialization

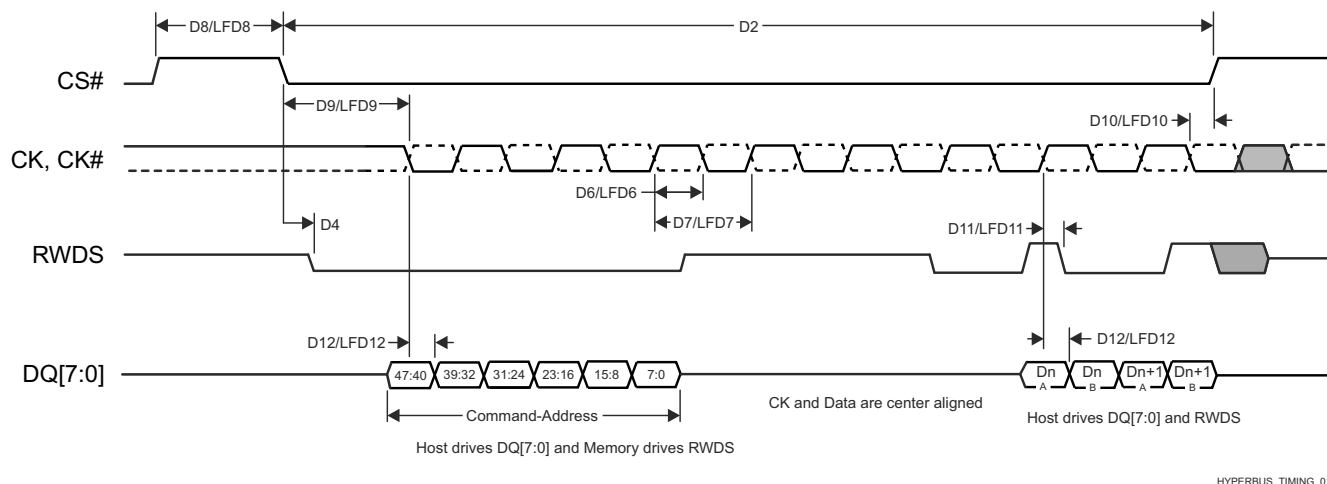
| NO.  | PARAMETER                     | DESCRIPTION                                   | MODE    | MIN    | MAX  | UNIT |
|------|-------------------------------|-----------------------------------------------|---------|--------|------|------|
| D1   | t <sub>w</sub> (RESETn)       | RESETn Pulse Width                            |         | 200    |      | ns   |
| D2   | t <sub>w</sub> (csnL)         | Chip Select Pulse Width                       |         |        | 1000 | ns   |
| D3   | t <sub>d</sub> (RESETnH-csnL) | Delay time, RESETn inactive to CSn active     |         | 200.34 |      | ns   |
| D4   | t <sub>d</sub> (csnL-RWDSL)   | Delay time, CSn active to RWDS falling        | 166 MHz |        | 186  | ns   |
|      |                               |                                               | 100 MHz |        | 182  | ns   |
| D5   | t <sub>skn</sub> (rwdX-dV)    | Input skew, RWDS transitioning to D0:D7 valid | 166 MHz | -0.46  | 0.46 | ns   |
| LFD5 |                               |                                               | 100 MHz | -0.81  | 0.81 | ns   |

#### 6.9.5.11.2 HyperBus 166 MHz Switching Characteristics

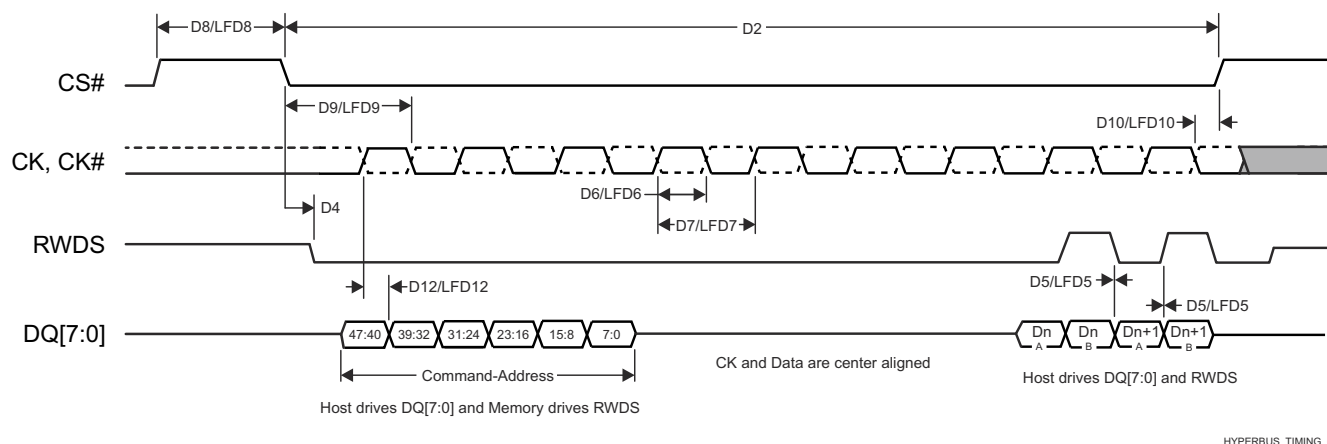
| NO. | PARAMETER                              | DESCRIPTION                                                                | MIN  | MAX   | UNIT |
|-----|----------------------------------------|----------------------------------------------------------------------------|------|-------|------|
| D6  | t <sub>c</sub> (clk/clk <sub>n</sub> ) | CLK period, CLK/CLK <sub>n</sub>                                           | 6    |       | ns   |
| D7  | t <sub>w</sub> (clk/clk <sub>n</sub> ) | Pulse width, CLK/CLK <sub>n</sub>                                          | 2.7  |       | ns   |
| D8  | t <sub>w</sub> (csIV)                  | Pulse width, CS0 invalid between operations                                | 6    |       | ns   |
| D9  | t <sub>d</sub> (clkH-csL)              | Delay time, CS0 active to CLK rising/ CLK <sub>n</sub> falling             |      | -3.34 | ns   |
| D10 | t <sub>d</sub> (clkL[LE]-csH)          | Delay time, last falling CLK/ rising CLK <sub>n</sub> edge to CS0 inactive | 0.34 |       | ns   |
| D11 | t <sub>d</sub> (clkX-rwdsV)            | Delay time, CLK transition to RWDS valid                                   | 0.94 | 2.08  | ns   |
| D12 | t <sub>d</sub> (clkX-d[0:7]V)          | Delay time, CLK transitioning to D0:7 valid                                | 0.76 | 2.26  | ns   |

#### 6.9.5.11.3 HyperBus 100 MHz Switching Characteristics

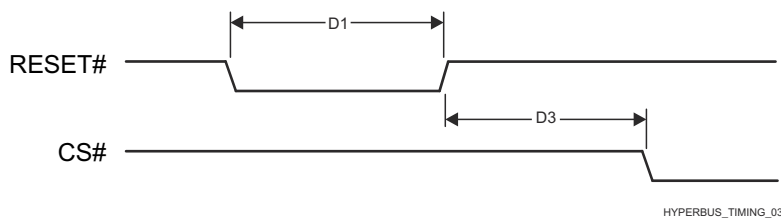
| NO.   | PARAMETER                     | DESCRIPTION                                       | MIN  | MAX   | UNIT |
|-------|-------------------------------|---------------------------------------------------|------|-------|------|
| LFD6  | t <sub>c</sub> (clk)          | CLK period, CLK                                   | 10   |       | ns   |
| LFD7  | t <sub>w</sub> (clk)          | Pulse width, CLK                                  | 4.5  |       | ns   |
| LFD8  | t <sub>w</sub> (csIV)         | Pulse width, CS0 invalid between operations       | 10   |       | ns   |
| LFD9  | t <sub>d</sub> (clkH-csL)     | Delay time, CS0 active to CLK rising              |      | -3.39 | ns   |
| LFD10 | t <sub>d</sub> (clkL[LE]-csH) | Delay time, last falling CLK edge to CS0 inactive | 0.39 |       | ns   |
| LFD11 | t <sub>d</sub> (clkX-rwdsV)   | Delay time, CLK transition to RWDS valid          | 1.39 | 3.62  | ns   |
| LFD12 | t <sub>d</sub> (clkX-d[0:7]V) | Delay time, CLK transitioning to D0:7 valid       | 1.21 | 3.8   | ns   |



**Figure 6-63. HyperBus Timing Diagrams - Transmitter Mode**



**Figure 6-64. HyperBus Timing Diagrams - Receiver Mode**



**Figure 6-65. HyperBus Timing Diagrams - Reset**

For more information, see section *HyperBus Interface* in the device TRM.

#### 6.9.5.12 I2C

The device includes 6 inter-integrated circuit (I2C) modules which provide an interface to other devices compliant with the Philips Semiconductors Inter-IC bus (I2C BUS™) specification version 2.1.

#### Note

HS-mode is only supported on MAIN\_I2C[0:3]. HS-mode is not supported on MCU\_I2C0 and WKUP\_I2C0.



**Note**

Philips I2C specification rise/fall timings apply only to MCU\_I2C0 and WKUP\_I2C0. MAIN\_I2C[0:3] use standard LVCMOS buffers to emulate open-drain buffers, and their rise/fall times should be referenced using the device IBIS model.

**Note**

I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

**6.9.5.13 MCAN**

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

[Table 6-41](#) presents timing conditions for MCANi interface. [Table 6-42](#) presents timing parameters for MCANi Interface.

**Table 6-41. MCAN Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 2   | 15  | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 5   | 20  | pF   |

**Table 6-42. MCAN Register to Pin Timings**

| NO. | PARAMETER                 | DESCRIPTION                                             | MIN | MAX | UNIT |
|-----|---------------------------|---------------------------------------------------------|-----|-----|------|
| M1  | t <sub>p</sub> (MCANi_TX) | Delay Time Max, Transmit Shift Register to MCANi_TX pin |     | 15  | ns   |
| M2  | t <sub>p</sub> (MCANi_RX) | Delay Time Max, MCANi_RX pin to receive shift register  |     | 15  | ns   |

For more information, see section *Controller Area Network (MCAN)* in the device TRM.

**6.9.5.14 MCASP**

For more details about features and additional description information on the device Multichannel Audio Serial Port, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

[Table 6-43](#) presents timing conditions for MCASP0 to MCASP2.

[Section 6.9.5.14.1](#) present timing requirements and switching characteristics for MCASP0 to MCASP2.

**Table 6-43. MCASP Timing Conditions**

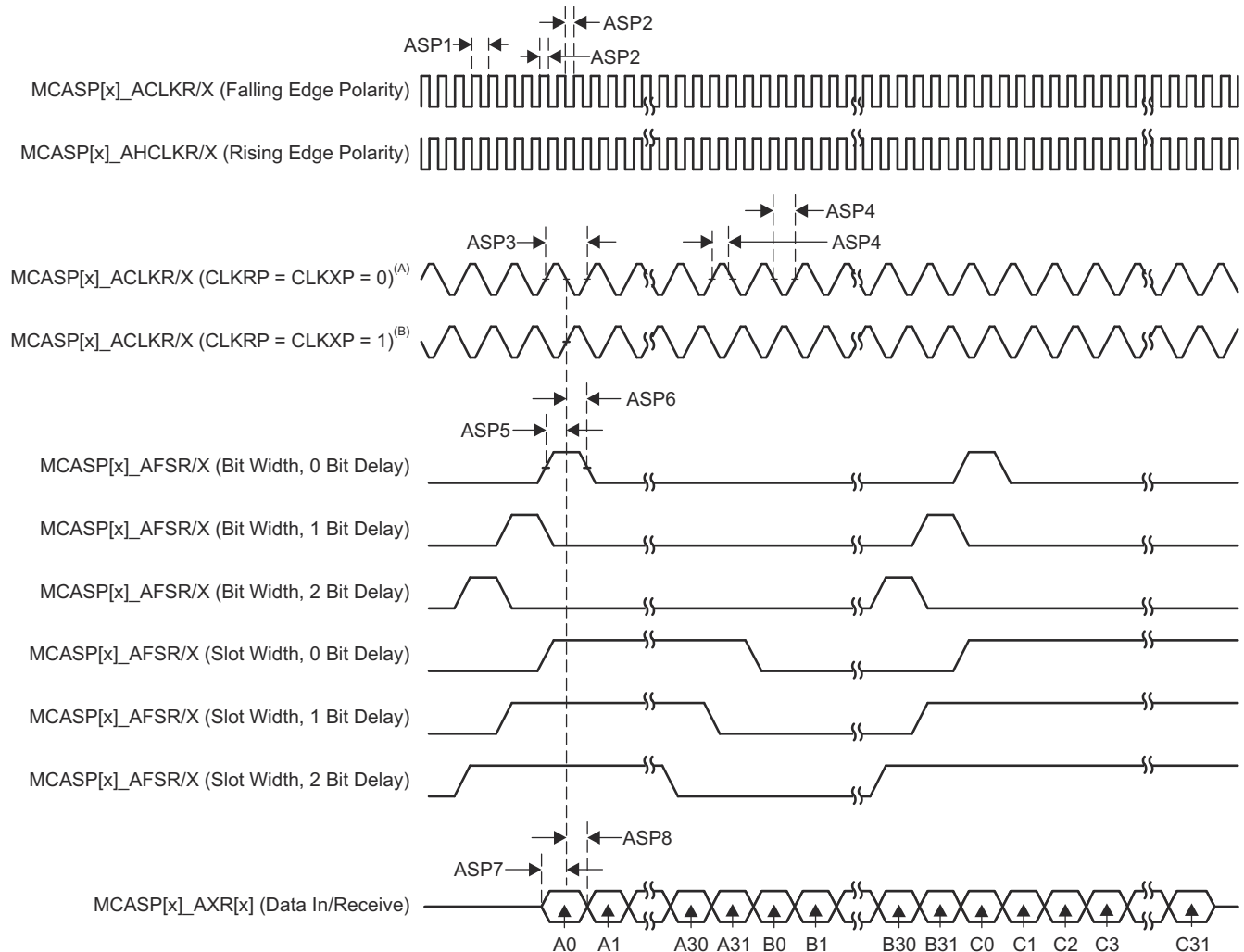
| PARAMETER                             |                                              | MIN | MAX  | UNIT |
|---------------------------------------|----------------------------------------------|-----|------|------|
| <b>INPUT CONDITIONS</b>               |                                              |     |      |      |
| SR <sub>I</sub>                       | Input slew rate                              | 0.7 | 5    | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                              |     |      |      |
| C <sub>L</sub>                        | Output load capacitance                      | 1   | 10   | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                              |     |      |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | 140 | 1080 | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces |     | 100  | ps   |

#### 6.9.5.14.1 MCASP Timing Requirements and Switching Characteristics

**Table 6-44. MCASP Timing Requirements**

| NO.  | PARAMETER                     | DESCRIPTION <sup>(1)</sup>                    | Mode               | MIN                       | MAX | UNIT |
|------|-------------------------------|-----------------------------------------------|--------------------|---------------------------|-----|------|
| ASP1 | $t_c(\text{AHCLKRX})$         | Cycle time, AHCLKR/X                          |                    | 15.25                     |     | ns   |
| ASP2 | $t_w(\text{AHCLKRX})$         | Pulse duration, AHCLKR/X high or low          |                    | 0.5P - 2.5 <sup>(2)</sup> |     | ns   |
| ASP3 | $t_c(\text{ACLKRX})$          | Cycle time, ACLKR/X                           |                    | 15.25                     |     | ns   |
| ASP4 | $t_w(\text{ACLKRX})$          | Pulse duration, ACLKR/X high or low           |                    | 0.5R - 2.5 <sup>(3)</sup> |     | ns   |
| ASP5 | $t_{su}(\text{AFSRX-ACLKRX})$ | Setup time, AFSR/X input valid before ACLKR/X | ACLKR/X int        | 10.995                    |     | ns   |
|      |                               |                                               | ACLKR/X ext in/out | 4                         |     |      |
| ASP6 | $t_h(\text{ACLKRX-AFSRX})$    | Hold time, AFSR/X input valid after ACLKR/X   | ACLKR/X int        | -1                        |     | ns   |
|      |                               |                                               | ACLKR/X ext in/out | 1.6                       |     |      |
| ASP7 | $t_{su}(\text{AXR-ACLKRX})$   | Setup time, AXR input valid before ACLKR/X    | ACLKR/X int        | 10.995                    |     | ns   |
|      |                               |                                               | ACLKR/X ext in/out | 4                         |     |      |
| ASP8 | $t_h(\text{ACLKRX-AXR})$      | Hold time, AXR input valid after ACLKR/X      | ACLKR/X int        | -1                        |     | ns   |
|      |                               |                                               | ACLKR/X ext in/out | 1.6                       |     |      |

- (1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1  
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0  
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1  
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1  
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0  
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
- (2) P = AHCLKR/X period in ns.
- (3) R = ACLKR/X period in ns.



- A. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).
- B. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

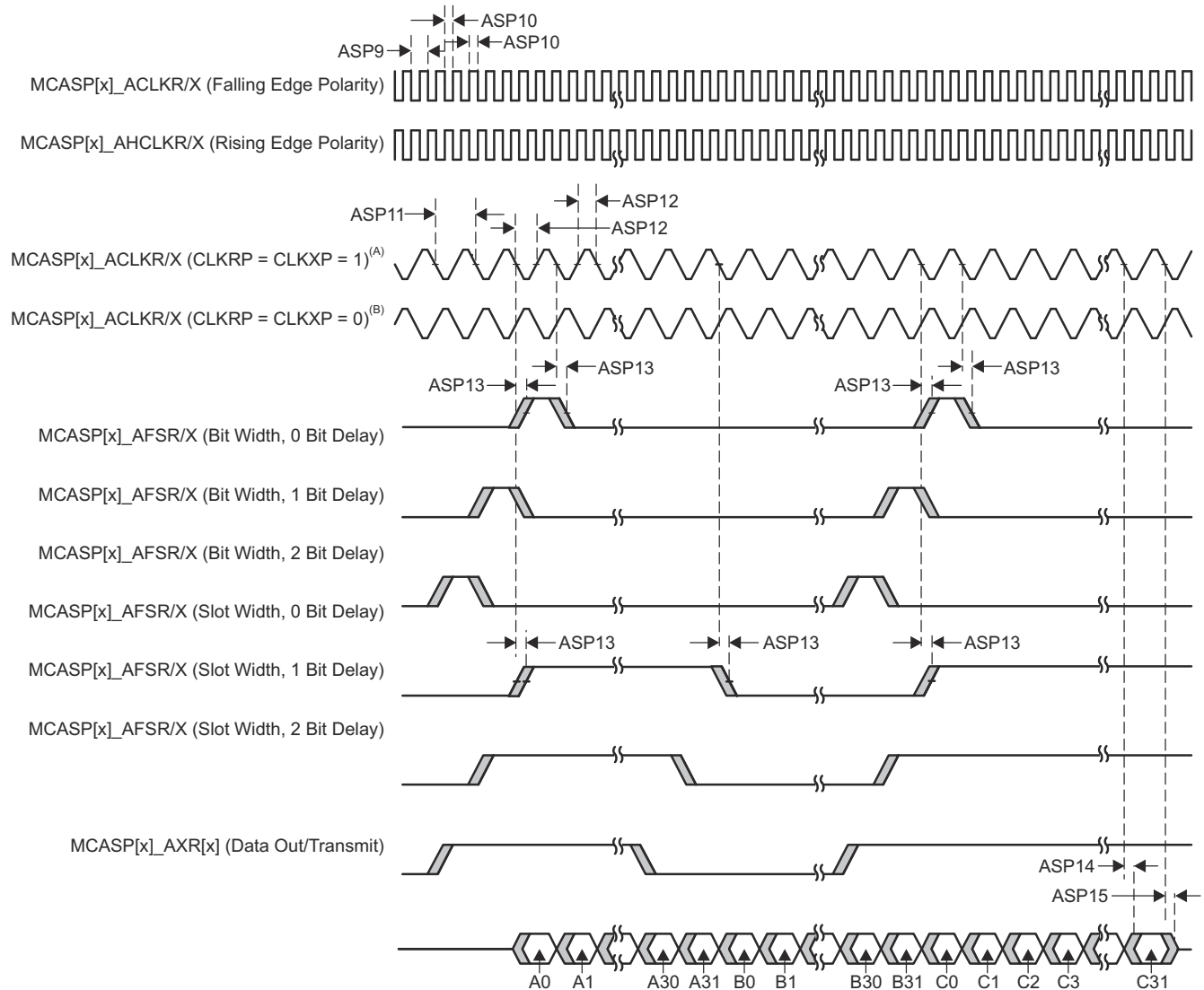
**Figure 6-66. MCASP Input Timing**

Table 6-45 and Figure 6-67 present switching characteristics over recommended operating conditions for MCASP0 to MCASP2.

**Table 6-45. MCASP Switching Characteristics**

| NO.   | PARAMETER             | DESCRIPTION <sup>(1)</sup>                                     | Mode              | MIN                       | MAX    | UNIT |
|-------|-----------------------|----------------------------------------------------------------|-------------------|---------------------------|--------|------|
| ASP9  | $t_{c(AHCLKRX)}$      | Cycle time, AHCLKR/X                                           |                   | 20                        |        | ns   |
| ASP10 | $t_{w(AHCLKRX)}$      | Pulse duration, AHCLKR/X high or low                           |                   | 0.5P - 2.5 <sup>(2)</sup> |        | ns   |
| ASP11 | $t_{c(ACLKRX)}$       | Cycle time, ACLKR/X                                            |                   | 20                        |        | ns   |
| ASP12 | $t_{w(ACLKRX)}$       | Pulse duration, ACLKR/X high or low                            |                   | 0.5R - 2.5 <sup>(3)</sup> |        | ns   |
| ASP13 | $t_{d(ACLKRX-AFSRX)}$ | Delay time, ACLKR/X transmit edge to AFSR/X output valid       | ACLKRX int        | 0                         | 6.5    | ns   |
|       |                       |                                                                | ACLKRX ext in/out | 2                         | 14     |      |
| ASP14 | $t_{d(ACLKX-AXR)}$    | Delay time, ACLKX transmit edge to AXR output valid            | ACLKRX int        | 0                         | 6.5    | ns   |
|       |                       |                                                                | ACLKRX ext in/out | 2                         | 14     |      |
| ASP15 | $t_{dis(ACLKX-AXR)}$  | Disable time, ACLKX transmit edge to AXR output high impedance | ACLKRX int        | - 0.2                     | 6.61   | ns   |
|       |                       |                                                                | ACLKRX ext in/out | 1.71                      | 15.383 |      |

- (1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1  
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0  
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1  
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1  
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0  
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
- (2) P = AHCLKR/X period in ns.
- (3) R = ACLKR/X period in ns.



- A. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).
- B. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

**Figure 6-67. MCASP Output Timing**

For more information, see section *Controller Area Network (MCAN)* in the device TRM.

#### 6.9.5.15 MCSPI

For more details about features and additional description information on the device Serial Port Interface, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

[Table 6-46](#) presents the timing conditions of SPI.

**Table 6-46. SPI Timing Conditions**

| PARAMETER                |                 | MIN | MAX | UNIT |
|--------------------------|-----------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                 |     |     |      |
| SR <sub>I</sub>          | Input slew rate | 2   | 8.5 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                 |     |     |      |

**Table 6-46. SPI Timing Conditions (continued)**

| PARAMETER      |                         | MIN | MAX | UNIT |
|----------------|-------------------------|-----|-----|------|
| C <sub>L</sub> | Output load capacitance | 2   | 24  | pF   |

#### 6.9.5.15.1 SPI—Master Mode

Table 6-47, Table 6-48, Figure 6-68, Figure 6-69 present Timing Requirements and Switching Characteristics for SPI - Master Mode.

**Table 6-47. SPI Timing Requirements - Master Mode**

| NO. |                               |                                                       | MIN | MAX | UNIT |
|-----|-------------------------------|-------------------------------------------------------|-----|-----|------|
| SM4 | t <sub>su</sub> (MISO-SPICLK) | Setup time, SPI_D[x] valid before SPI_CLK active edge | 2   |     | ns   |
| SM5 | t <sub>h</sub> (SPICLK-MISO)  | Hold time, SPI_D[x] valid after SPI_CLK active edge   | 3   |     | ns   |

**Table 6-48. SPI Switching Characteristics - Master Mode**

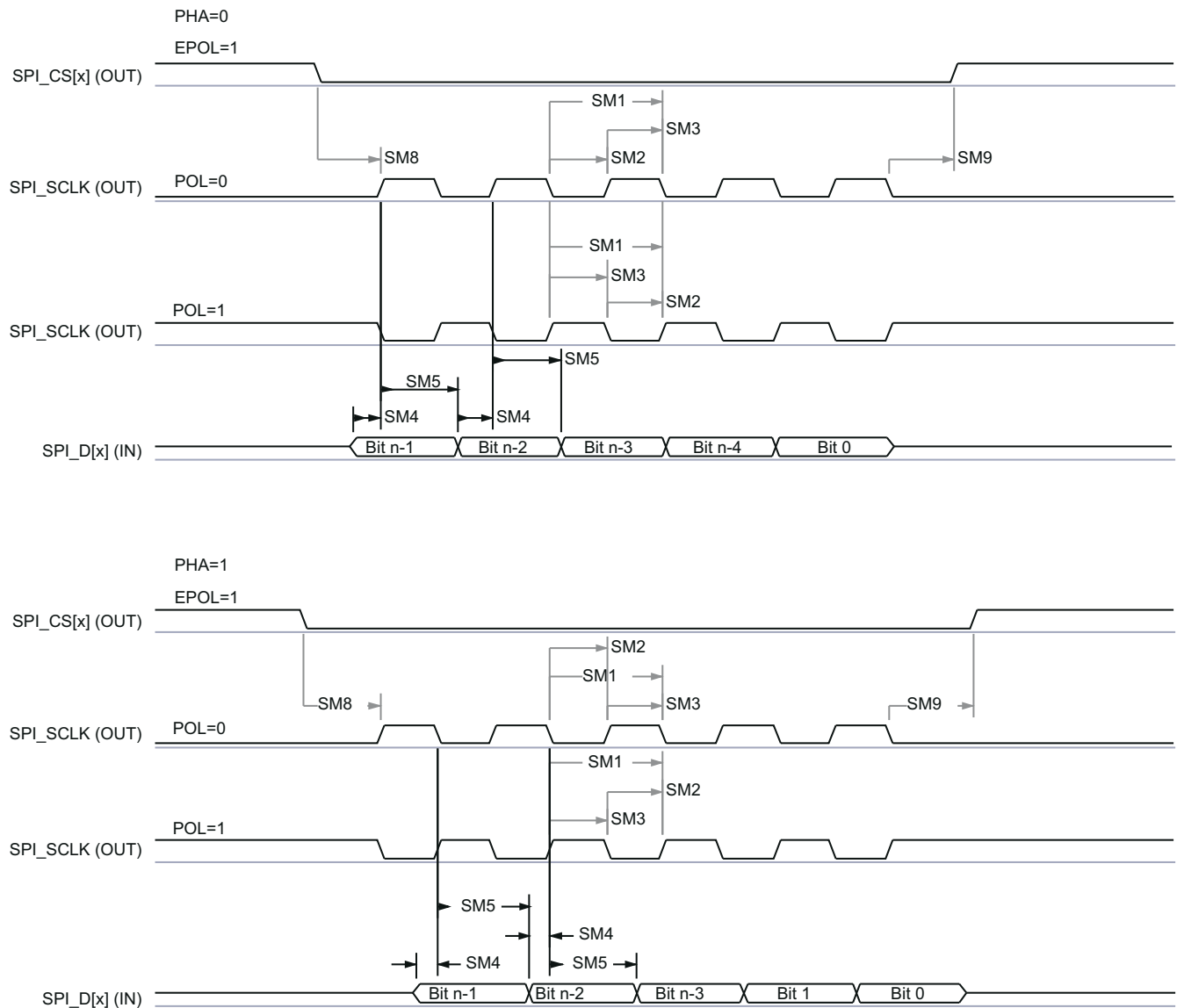
| NO. | DESCRIPTION                  |                                                        | MODE                                   | MIN                         | MAX | UNIT |
|-----|------------------------------|--------------------------------------------------------|----------------------------------------|-----------------------------|-----|------|
| SM1 | t <sub>c</sub> (SPICLK)      | Cycle time, SPI_CLK                                    |                                        | 20.8                        |     | ns   |
| SM2 | t <sub>w</sub> (SPICLKL)     | Typical Pulse duration, SPI_CLK low                    |                                        | -1 +<br>0.5P <sup>(1)</sup> |     | ns   |
| SM3 | t <sub>w</sub> (SPICLKH)     | Typical Pulse duration, SPI_CLK high                   |                                        | -1 +<br>0.5P <sup>(1)</sup> |     | ns   |
| SM6 | t <sub>d</sub> (SPICLK-SIMO) | Delay time, SPI_CLK active edge to SPI_D[x] transition |                                        | -3                          | 2   | ns   |
| SM7 | t <sub>sk</sub> (CS-SIMO)    | Delay time, SPI_CS[x] active to SPI_D[x] transition    |                                        | 5                           |     | ns   |
| SM8 | t <sub>d</sub> (SPICLK-CS)   | Delay time, SPI_CS[x] active to SPI_CLK first edge     | Master_PHA0_POL0;<br>Master_PHA0_POL1; | -4 + B <sup>(2)</sup>       |     | ns   |
|     |                              |                                                        | Master_PHA1_POL0;<br>Master_PHA1_POL1; | -4 + A <sup>(3)</sup>       |     | ns   |
| SM9 | t <sub>d</sub> (SPICLK-CS)   | Delay time, SPI_CLK last edge to SPI_CS[x] inactive    | Master_PHA0_POL0;<br>Master_PHA0_POL1; | -4 + A <sup>(3)</sup>       |     | ns   |
|     |                              |                                                        | Master_PHA1_POL0;<br>Master_PHA1_POL1; | -4 + B <sup>(2)</sup>       |     | ns   |

(1) P = SPICLK period

(2) B = (TCS + .5) × TSPICLKREF × Fratio, where TCS is a bit field of the SPI\_CH(i)CONF register and Fratio = Even >= 2.

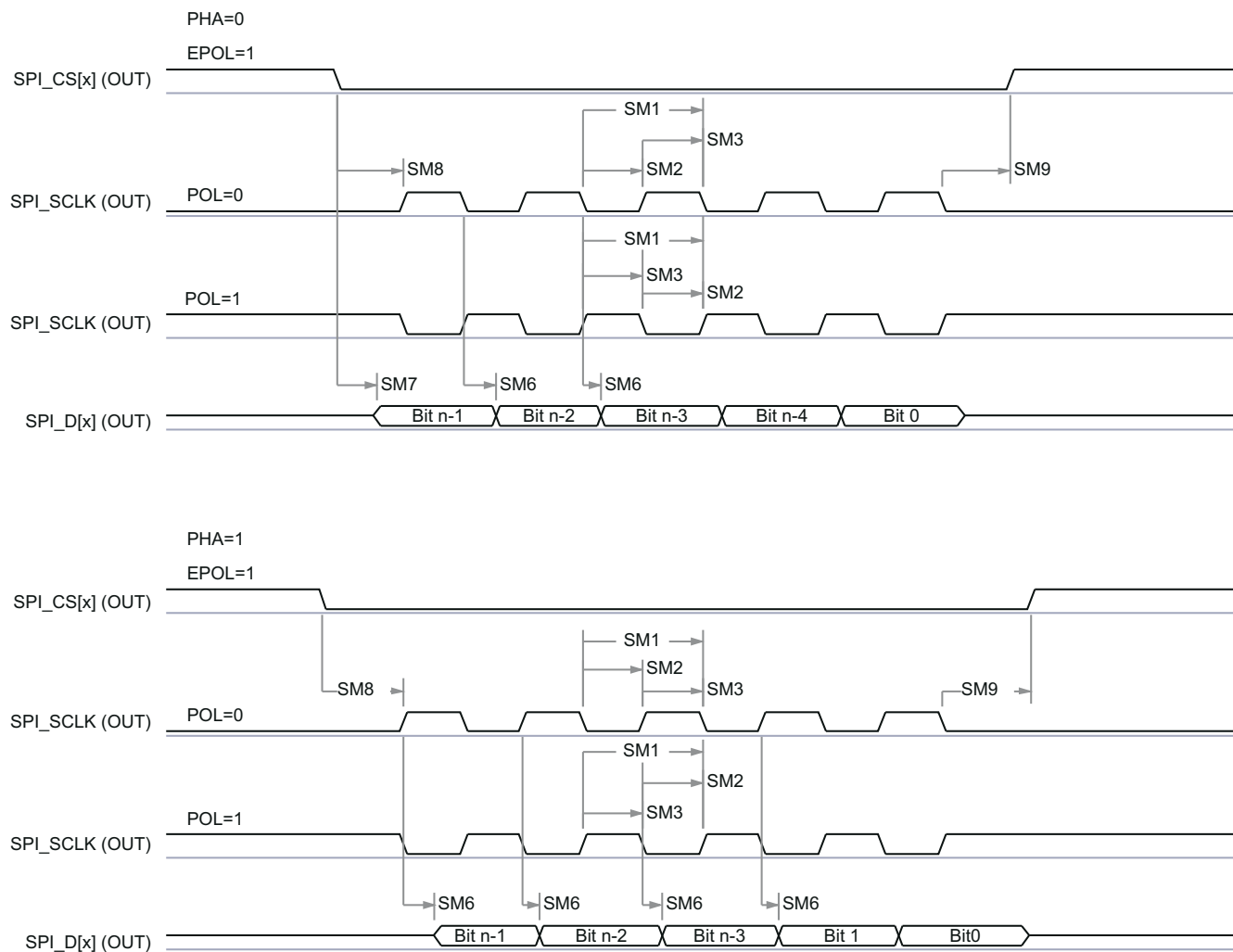
(3) When P = 20.8 ns, A = (TCS + 1) × TSPICLKREF, where TCS is a bit field of the SPI\_CH(i)CONF register.

When P > 20.8 ns, A = (TCS + 0.5) × Fratio × TSPICLKREF, where TCS is a bit field of the SPI\_CH(i)CONF register.



SPRSP08\_TIMING\_McSPI\_02

**Figure 6-68. SPI Timing Requirements - Master Mode**



SPRSP08\_TIMING\_McSPI\_01

**Figure 6-69. SPI Switching Characteristics - Master Mode**



### 6.9.5.15.2 SPI—Slave Mode

Table 6-49, Table 6-50, Figure 6-70 and Figure 6-71 present Timing Requirements and Switching Characteristics for SPI - Slave Mode.

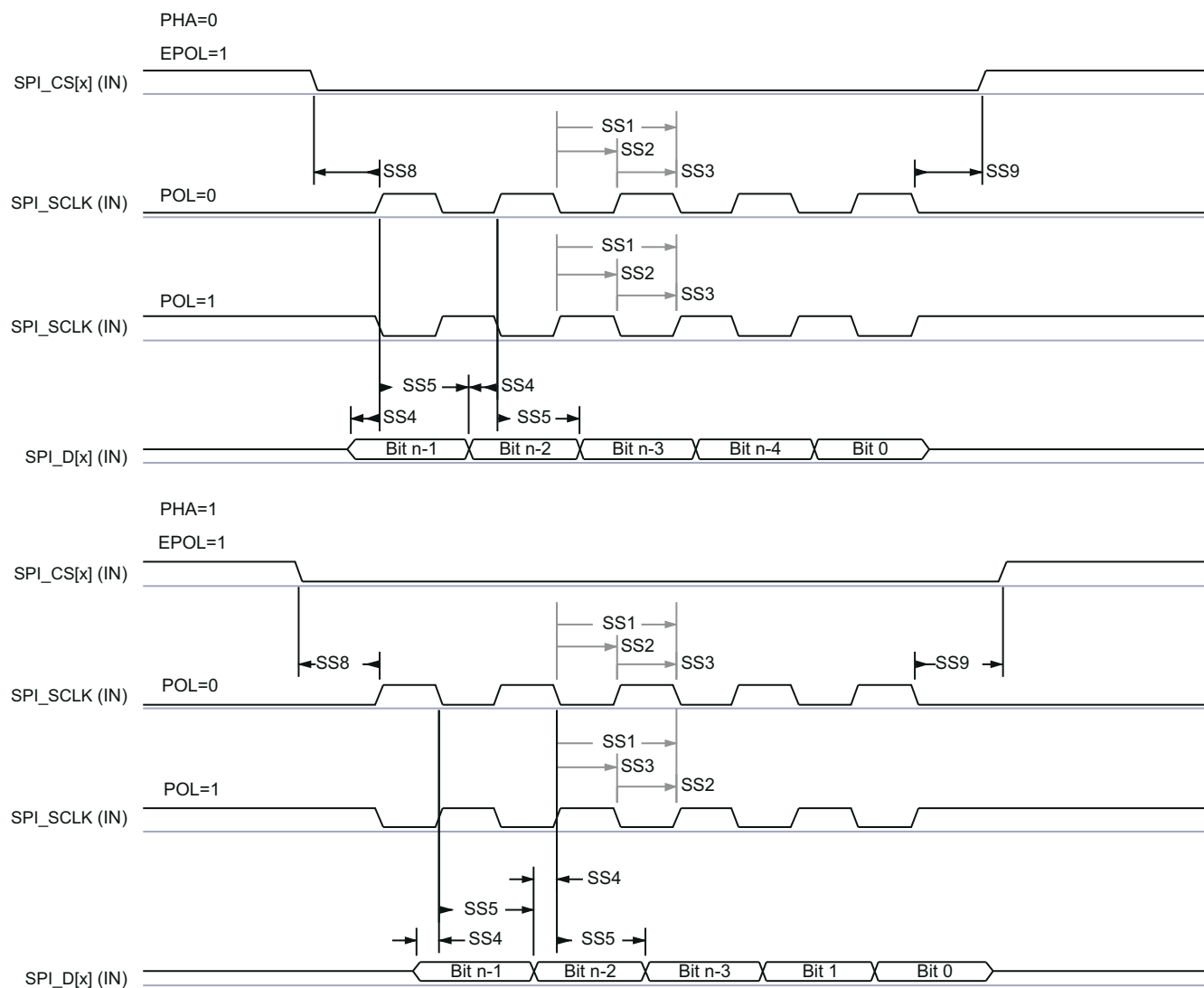
**Table 6-49. SPI Timing Requirements - Slave Mode**

| NO. | PARAMETER                    | DESCRIPTION                                           | MIN                  | MAX | UNIT |
|-----|------------------------------|-------------------------------------------------------|----------------------|-----|------|
| SS1 | $t_c(\text{SPICLK})$         | Cycle time, SPI_CLK                                   | 20.8                 |     | ns   |
| SS2 | $t_w(\text{SPICLK}_L)$       | Typical Pulse duration, SPI_CLK low                   | 0.45P <sup>(1)</sup> |     | ns   |
| SS3 | $t_w(\text{SPICLK}_H)$       | Typical Pulse duration, SPI_CLK high                  | 0.45P <sup>(1)</sup> |     | ns   |
| SS4 | $t_{su}(\text{SIMO-SPICLK})$ | Setup time, SPI_D[x] valid before SPI_CLK active edge | 5                    |     | ns   |
| SS5 | $t_h(\text{SPICLK-SIMO})$    | Hold time, SPI_D[x] valid after SPI_CLK active edge   | 5                    |     | ns   |
| SS8 | $t_{su}(\text{CS-SPICLK})$   | Setup time, SPI_CS[x] valid before SPI_CLK first edge | 5                    |     | ns   |
| SS9 | $t_h(\text{SPICLK-CS})$      | Hold time, SPI_CS[x] valid after SPI_CLK last edge    | 5                    |     | ns   |

**Table 6-50. SPI Switching Characteristics - Slave Mode**

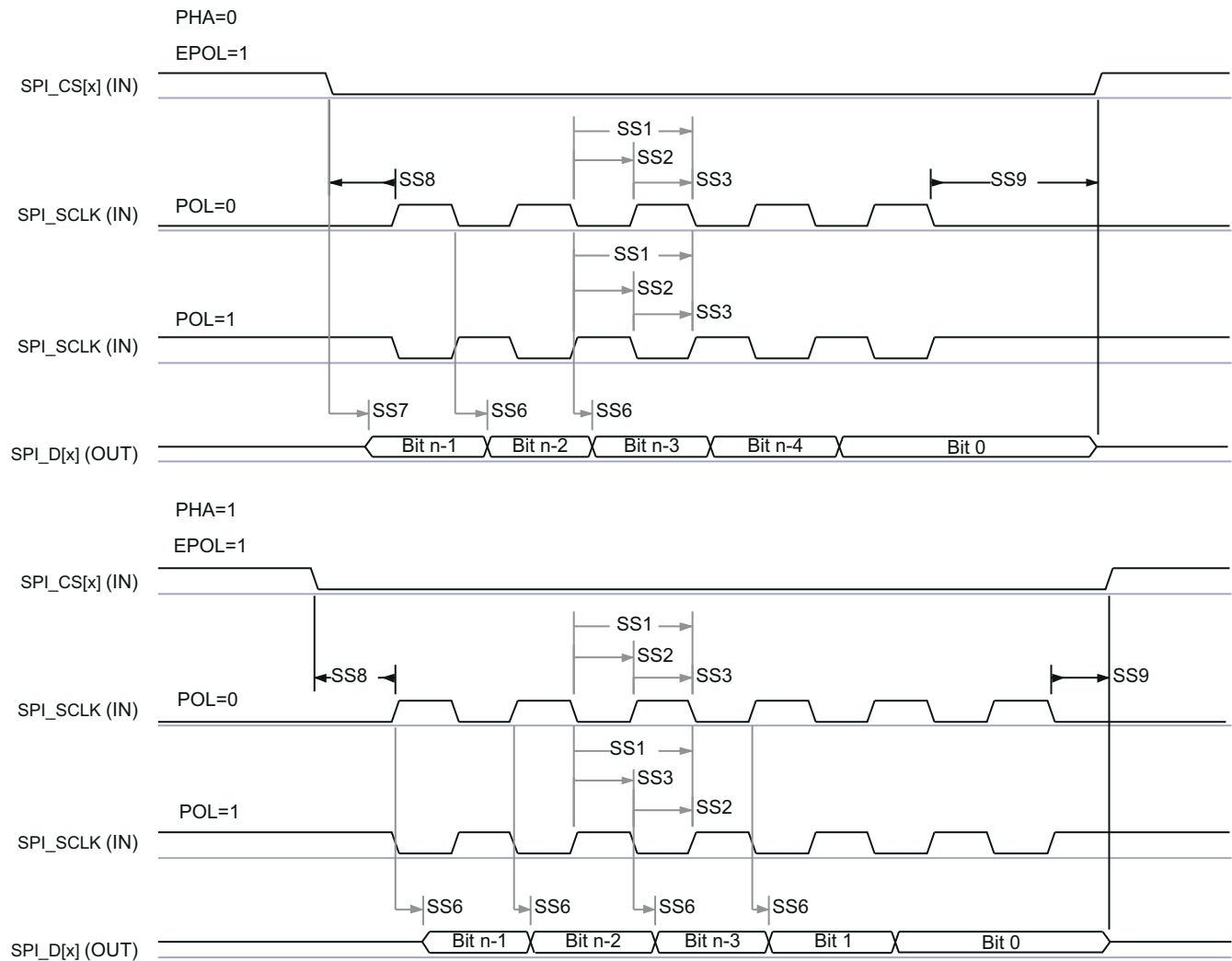
| NO. | PARAMETER                 | DESCRIPTION                                                | MIN   | MAX | UNIT |
|-----|---------------------------|------------------------------------------------------------|-------|-----|------|
| SS6 | $t_d(\text{SPICLK-SOMI})$ | Delay time, SPI_CLK active edge to mcspi_somi transition   | 2     | 5   | ns   |
| SS7 | $t_{sk}(\text{CS-SOMI})$  | Delay time, SPI_CS[x] active edge to mcspi_somi transition | 20.95 |     | ns   |

(1) P = SPICLK period.



SPRSP08\_TIMING\_McSPI\_04

**Figure 6-70. SPI Timing Requirements - Slave Mode**



SPRSP08\_TIMING\_McSPI\_03

**Figure 6-71. SPI Switching Characteristics - Slave Mode**

For more information, see section *Multichannel Serial Peripheral Interface (MCSPi)* in the device TRM.

### 6.9.5.16 MMCSD

#### Note

The I/O Timings provided in this section are valid only when the corresponding DLL Delays are configured for some MMC usage modes, as described in [Table 6-52](#).

#### Note

The MMCi (i = 0 to 1) controller is also referred to as MMCi.

For more details about features and additional description information on the device Multi Media Card, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

#### 6.9.5.16.1 MMCSDi — eMMC/SD/SDIO Card Interface

MMCi interface is compliant with the SD Standard v3.01 as well as JEDEC eMMC standard v4.5 and it supports the following SD Card and eMMC applications:

- SD Default Speed; JEDEC 3.3V Legacy SDR
- SD High speed; JEDEC 3.3V High Speed SDR
- SD UHS-I SDR12; JEDEC 1.8V Legacy SDR
- SD UHS-I SDR25; JEDEC 1.8V High Speed SDR
- SD UHS-I SDR50
- SD UHS-I SDR104; JEDEC HS200
- UHS-I DDR50; JEDEC High Speed DDR (DDR52)

#### Note

For more information, see section *Multimedia Card/Secure Digital () Interface* in the device TRM.

[Table 6-51](#) presents the timing conditions for MMC interface.

**Table 6-51. MMC Timing Conditions**

| PARAMETER                     |                         |                                          | MIN  | MAX  | UNIT |
|-------------------------------|-------------------------|------------------------------------------|------|------|------|
| INPUT CONDITIONS              |                         |                                          |      |      |      |
| SR <sub>i</sub>               | Input slew rate         | Default Speed; 3.3V Legacy SDR           | 0.26 | 2.64 | V/ns |
|                               |                         | High Speed; 3.3V High Speed SDR          | 0.69 | 2.06 | V/ns |
|                               |                         | UHS-I SDR12; 1.8V Legacy SDR             | 0.14 | 1.44 | V/ns |
|                               |                         | UHS-I SDR25; 1.8V High Speed SDR         | 0.3  | 1.34 | V/ns |
|                               |                         | 3.3V High Speed DDR CMD                  | 0.69 | 2.06 | V/ns |
|                               |                         | 3.3V High Speed DDR DAT                  | 1.03 | 2.06 | V/ns |
|                               |                         | UHS-I DDR50 CMD; 1.8V High Speed DDR CMD | 0.3  | 1.34 | V/ns |
|                               |                         | UHS-I DDR50 CMD; 1.8V High Speed DDR DAT | 0.34 | 1.34 | V/ns |
| OUTPUT CONDITIONS             |                         |                                          |      |      |      |
| C <sub>L</sub>                | Output load capacitance | SDR50                                    | 1    | 10   | pF   |
|                               |                         | SDR104; HS200                            | 1    | 6    | pF   |
|                               |                         | All other modes                          | 1    | 12   | pF   |
| PCB CONNECTIVITY REQUIREMENTS |                         |                                          |      |      |      |

**Table 6-51. MMC Timing Conditions (continued)**

| PARAMETER                    |                                                    |                                                             | MIN | MAX   | UNIT |
|------------------------------|----------------------------------------------------|-------------------------------------------------------------|-----|-------|------|
| $t_d$ (Trace Delay)          | Propagation delay of each trace - SD Specification | Default Speed; SDR12 SDR50; SDR104                          | 134 | 1474  | ps   |
|                              |                                                    | High Speed; SDR25                                           | 134 | 1139  | ps   |
|                              |                                                    | DDR50                                                       | 255 | 11394 | ps   |
|                              | Propagation delay of each trace - JEDEC eMMC       | 1.8V, 3.3V Legacy SDR<br>1.8V, 3.3V High Speed SDR<br>HS200 | 134 | 670   | ps   |
|                              |                                                    | 1.8V/ 3.3 V High Speed DDR (DDR52)                          | 168 | 670   | ps   |
| $t_d$ (Trace Mismatch Delay) | Propagation delay mismatch across all traces       | Default Speed; 3.3V Legacy SDR                              |     | 100   | ps   |
|                              |                                                    | 3.3V High Speed SDR; HS400 DAT                              |     | 8     | ps   |
|                              |                                                    | All other modes                                             |     | 20    | ps   |

Table 6-52 shows the required DLL software configuration settings for MMC timing modes.

**Table 6-52. MMC DLL Delay Mapping for All Timing Modes**

| REGISTER NAME          |                                               | MMCSDn_SS_PHY_CTRL_4_REG |                     |                    |                    |                   | MMCSDn_SS_PHY_CTRL_5_REG   |                   |                       |
|------------------------|-----------------------------------------------|--------------------------|---------------------|--------------------|--------------------|-------------------|----------------------------|-------------------|-----------------------|
| BIT FIELD              |                                               | [27:24]                  | [20]                | [15:12]            | [8]                | [4:0]             | [17:16]                    | [9:8]             | [2:0]                 |
| BIT FIELD NAME         |                                               | STRBSEL                  | OTAPDLYENA          | OTAPDLYSEL         | ITAPDLYENA         | ITAPDLYSEL        | SELDLYTXCLK<br>SELDLYRXCLK | SEL100SEL50       | CLKBUFSSEL            |
| MODE                   | DESCRIPTION                                   | STROBE DELAY             | OUTPUT DELAY ENABLE | OUTPUT DELAY VALUE | INPUT DELAY ENABLE | INPUT DELAY VALUE | DLL DELAY CHAIN SELECT     | DLL REF FREQUENCY | DELAY BUFFER DURATION |
| Default Speed          | 4- or 8-bit PHY operating 3.3 V, 25 MHz mode  | 0x0                      | 0x0                 | 0x0                | 0x1                | 0xA               | 0x3                        | 0x0               | 0x7                   |
| High Speed             | 4- or 8-bit PHY operating 3.3 V, 50 MHz mode  | 0x0                      | 0x0                 | 0x0                | 0x1                | 0x1               | 0x3                        | 0x0               | 0x7                   |
| SDR12                  | 4- or 8-bit PHY operating 1.8 V, 25 MHz mode  | 0x0                      | 0x1                 | 0xF                | 0x1                | 0xA               | 0x3                        | 0x0               | 0x7                   |
| SDR25                  | 4- or 8-bit PHY operating 1.8 V, 50 MHz mode  | 0x0                      | 0x1                 | 0xF                | 0x1                | 0x1               | 0x3                        | 0x0               | 0x7                   |
| SDR50                  | 4- or 8-bit PHY operating 1.8 V, 100 MHz      | 0x0                      | 0x1                 | 0x8                | 0x1                | Tuning            | 0x0                        | 0x2               | 0x7                   |
| High Speed DDR (DDR52) | 4- or 8-bit PHY, 1.8V or 3.3V, JEDEC 50 MHz   | 0x0                      | 0x1                 | 0x5                | 0x1                | 0x0               | 0x0                        | 0x1               | 0x7                   |
| DDR50                  | 4- or 8-bit PHY, 1.8V or 3.3V, SD/SDIO 50 MHz | 0x0                      | 0x1                 | 0x4                | 0x1                | Tuning            | 0x0                        | 0x1               | 0x7                   |

**Table 6-52. MMC DLL Delay Mapping for All Timing Modes (continued)**

| REGISTER NAME  |                                                  | MMCSDn_SS_PHY_CTRL_4_REG |                     |                    |                    |                   | MMCSDn_SS_PHY_CTRL_5_REG   |                   |                       |
|----------------|--------------------------------------------------|--------------------------|---------------------|--------------------|--------------------|-------------------|----------------------------|-------------------|-----------------------|
| BIT FIELD      |                                                  | [27:24]                  | [20]                | [15:12]            | [8]                | [4:0]             | [17:16]                    | [9:8]             | [2:0]                 |
| BIT FIELD NAME |                                                  | STRBSEL                  | OTAPDLYENA          | OTAPDLYSEL         | ITAPDLYENA         | ITAPDLYSEL        | SELDLYTXCLK<br>SELDLYRXCLK | SEL100SEL50       | CLKBUFSSEL            |
| MODE           | DESCRIPTION                                      | STROBE DELAY             | OUTPUT DELAY ENABLE | OUTPUT DELAY VALUE | INPUT DELAY ENABLE | INPUT DELAY VALUE | DLL DELAY CHAIN SELECT     | DLL REF FREQUENCY | DELAY BUFFER DURATION |
| SDR104         | 4- or 8-bit PHY operating 1.8 V, SD/SDIO 200 MHz | 0x0                      | 0x1                 | 0x7                | 0x1                | Tuning            | 0x0                        | 0x0               | 0x7                   |
| HS200          | 4- or 8-bit PHY operating 1.8 V, JEDEC 200 MHz   | 0x0                      | 0x1                 | 0x5                | 0x1                | Tuning            | 0x0                        | 0x0               | 0x7                   |

For more information, see section *Multimedia Card/Secure Digital (eMMC/SD/SDIO) Interface* in the device TRM.

#### 6.9.5.16.1.1 Default Speed, 3.3V Legacy SDR Mode

Table 6-53 and Table 6-54 present Timing requirements and Switching characteristics for MMCi - Default Speed, 3.3V Legacy SDR in receiver and transmitter mode (see Figure 6-72 and Figure 6-73)

**Table 6-53. Timing Requirements for MMCi - Default Speed Mode**

| NO.   | PARAMETER           | DESCRIPTION                                                       | MIN   | MAX | UNIT |
|-------|---------------------|-------------------------------------------------------------------|-------|-----|------|
| DSSD5 | $t_{su(cmdV-clkH)}$ | Setup time, MMCi_CMD valid before MMCi_CLK rising clock edge      | 2.15  |     | ns   |
| DSSD6 | $t_{h(clkH-cmdV)}$  | Hold time, MMCi_CMD valid after MMCi_CLK rising clock edge        | 19.67 |     | ns   |
| DSSD7 | $t_{su(dV-clkH)}$   | Setup time, MMCi_DAT[j:0] valid before MMCi_CLK rising clock edge | 2.15  |     | ns   |
| DSSD8 | $t_{h(clkH-dV)}$    | Hold time, MMCi_DAT[j:0] valid after MMCi_CLK rising clock edge   | 19.67 |     | ns   |

**Table 6-54. Switching Characteristics for MMCi - Default Speed Mode**

| NO.   | PARAMETER          | DESCRIPTION                                                         | MIN   | MAX  | UNIT |
|-------|--------------------|---------------------------------------------------------------------|-------|------|------|
| DSSD0 | $f_{op(clk)}$      | Operating frequency, MMCi_CLK                                       |       | 25   | MHz  |
| DSSD1 | $t_{w(clkH)}$      | Pulse duration, MMCi_CLK high                                       | 18.7  |      | ns   |
| DSSD2 | $t_{w(clkL)}$      | Pulse duration, MMCi_CLK low                                        | 18.7  |      | ns   |
| DSSD3 | $t_{d(clkL-cmdV)}$ | Delay time, MMCi_CLK falling clock edge to MMCi_CMD transition      | -14.1 | 14.1 | ns   |
| DSSD4 | $t_{d(clkL-dV)}$   | Delay time, MMCi_CLK falling clock edge to MMCi_DAT[j:0] transition | -14.1 | 14.1 | ns   |

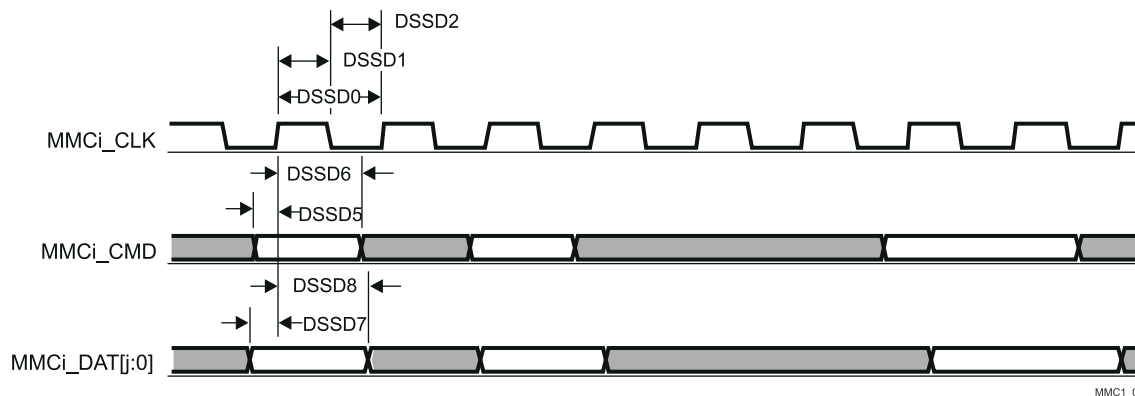


Figure 6-72. eMMC/SD/SDIO in - Default Speed - Receiver Mode



Figure 6-73. eMMC/SD/SDIO in - Default Speed - Transmitter Mode

#### 6.9.5.16.1.2 High Speed, 3.3V High Speed SDR Mode

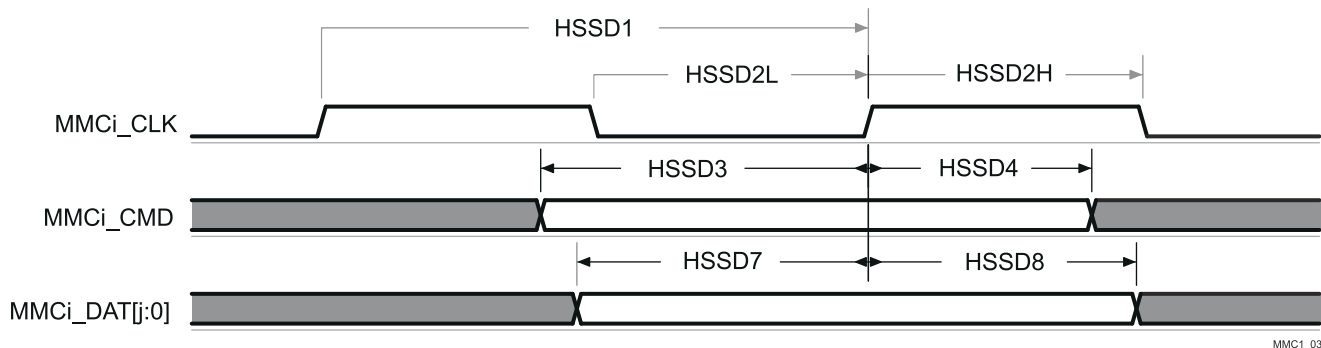
Table 6-55 and Table 6-56 present Timing requirements and Switching characteristics for MMCi - High Speed and 3.3V High Speed SDR in receiver and transmitter mode (see Figure 6-74 and Figure 6-75).

Table 6-55. Timing Requirements for MMCi - High Speed Mode

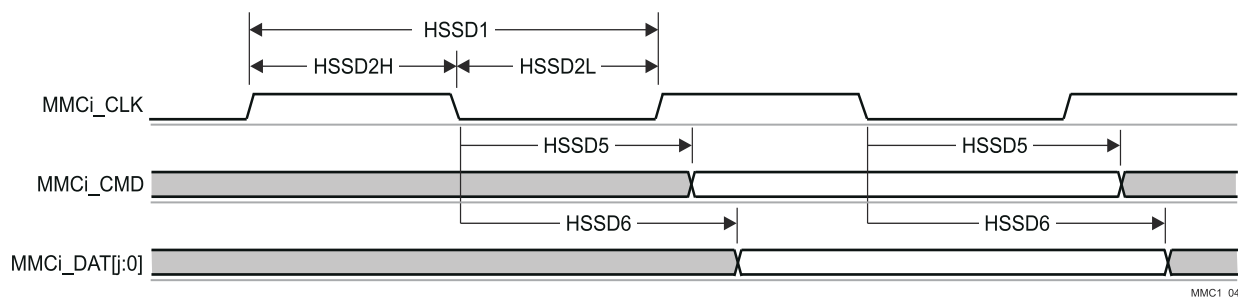
| NO.   | PARAMETER           | DESCRIPTION                                                       | MIN  | MAX | UNIT |
|-------|---------------------|-------------------------------------------------------------------|------|-----|------|
| HSSD3 | $t_{su(cmdV-clkH)}$ | Setup time, MMCi_CMD valid before MMCi_CLK rising clock edge      | 2.91 |     | ns   |
| HSSD4 | $t_{h(clkH-cmdV)}$  | Hold time, MMCi_CMD valid after MMCi_CLK rising clock edge        | 2.76 |     | ns   |
| HSSD7 | $t_{su(dV-clkH)}$   | Setup time, MMCi_DAT[j:0] valid before MMCi_CLK rising clock edge | 2.91 |     | ns   |
| HSSD8 | $t_{h(clkH-dV)}$    | Hold time, MMCi_DAT[j:0] valid after MMCi_CLK rising clock edge   | 2.76 |     | ns   |

Table 6-56. Switching Characteristics for MMCi - High Speed Mode

| NO.    | PARAMETER          | DESCRIPTION                                                         | MIN   | MAX  | UNIT |
|--------|--------------------|---------------------------------------------------------------------|-------|------|------|
| HSSD1  | $f_{op(clk)}$      | Operating frequency, MMCi_CLK                                       |       | 50   | MHz  |
| HSSD2H | $t_{w(clkH)}$      | Pulse duration, MMCi_CLK high                                       | 9.2   |      | ns   |
| HSSD2L | $t_{w(clkL)}$      | Pulse duration, MMCi_CLK low                                        | 9.2   |      | ns   |
| HSSD5  | $t_{d(clkL-cmdV)}$ | Delay time, MMCi_CLK falling clock edge to MMCi_CMD transition      | -6.44 | 3.44 | ns   |
| HSSD6  | $t_{d(clkL-dV)}$   | Delay time, MMCi_CLK falling clock edge to MMCi_DAT[j:0] transition | -6.44 | 3.44 | ns   |



**Figure 6-74. eMMC/SD/SDIO in - High Speed - Receiver Mode**



**Figure 6-75. eMMC/SD/SDIO in - High Speed - Transmitter Mode**

#### 6.9.5.16.1.3 UHS-I SDR12, 1.8-V Legacy SDR Mode

Table 6-57 and Table 6-58 present Timing requirements and Switching characteristics for MMCi - SDR12, 1.8V Legacy SDR in receiver and transmitter mode (see Figure 6-76 and Figure 6-77).

**Table 6-57. Timing Requirements for MMCi - SDR12, 1.8-V Legacy SDR Mode**

| NO.    | PARAMETER           | DESCRIPTION                                                       | MIN   | MAX | UNIT |
|--------|---------------------|-------------------------------------------------------------------|-------|-----|------|
| SDR121 | $t_{su(cmdV-clkH)}$ | Setup time, MMCi_CMD valid before MMCi_CLK rising clock edge      | 10.04 |     | ns   |
| SDR122 | $t_{h(clkH-cmdV)}$  | Hold time, MMCi_CMD valid after MMCi_CLK rising clock edge        | 1.75  |     | ns   |
| SDR123 | $t_{su(dV-clkH)}$   | Setup time, MMCi_DAT[j:0] valid before MMCi_CLK rising clock edge | 10.04 |     | ns   |
| SDR124 | $t_{h(clkH-dV)}$    | Hold time, MMCi_DAT[j:0] valid after MMCi_CLK rising clock edge   | 1.75  |     | ns   |

**Table 6-58. Switching Characteristics for MMCi - SDR12, 1.8-V Legacy SDR Mode**

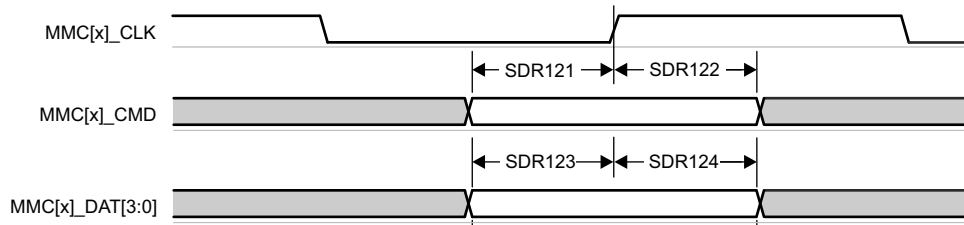
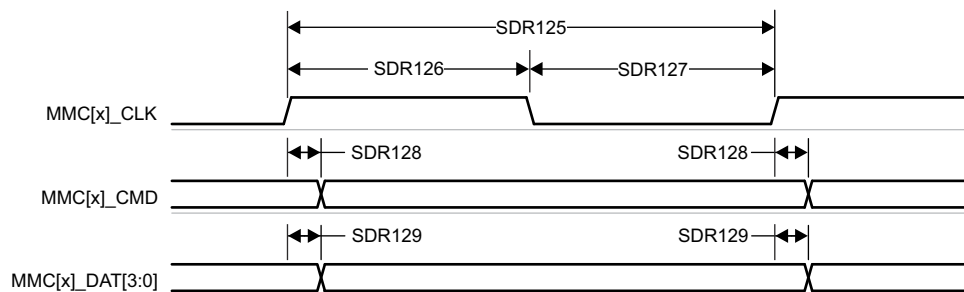
| NO.    | PARAMETER          | DESCRIPTION                                                   | MIN  | MAX   | UNIT |
|--------|--------------------|---------------------------------------------------------------|------|-------|------|
| SDR125 | $f_{op(clk)}$      | Operating frequency, MMCi_CLK                                 |      | 25    | MHz  |
| SDR126 | $t_{w(clkH)}$      | Pulse duration, MMCi_CLK high                                 | 18.7 |       | ns   |
| SDR127 | $t_{w(clkL)}$      | Pulse duration, MMCi_CLK low                                  | 18.7 |       | ns   |
| SDR128 | $t_{d(clkH-cmdV)}$ | Delay time, MMCi_CLK rising clock edge to MMCi_CMD transition | 1.12 | 35.68 | ns   |



**Table 6-58. Switching Characteristics for MMCi - SDR12, 1.8-V Legacy SDR Mode (continued)**

| NO.    | PARAMETER               | DESCRIPTION                                                        | MIN  | MAX   | UNIT |
|--------|-------------------------|--------------------------------------------------------------------|------|-------|------|
| SDR129 | $t_{d(\text{clkH-dV})}$ | Delay time, MMCi_CLK rising clock edge to MMCi_DAT[j:0] transition | 1.12 | 35.68 | ns   |

A. There are two modules in MMCi: MMC0 and MMC1

**Figure 6-76. eMMC/SD/SDIO in - SDR12, 1.8-V Legacy SDR - Receiver Mode****Figure 6-77. eMMC/SD/SDIO in - SDR12, 1.8-V Legacy SDR - Transmitter Mode**

#### 6.9.5.16.1.4 UHS-I SDR25 Mode

Table 6-59 and Table 6-60 present Timing requirements and Switching characteristics for MMCi - SDR25, 1.8V High Speed SDR in receiver and transmitter mode (see Figure 6-78 and Figure 6-79).

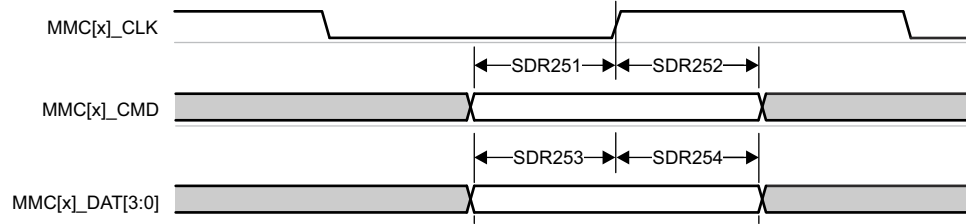
**Table 6-59. Timing Requirements for MMCi - SDR25, 1.8-V High-Speed SDR Mode**

| NO.    | PARAMETER                  | DESCRIPTION                                                       | MIN  | MAX | UNIT |
|--------|----------------------------|-------------------------------------------------------------------|------|-----|------|
| SDR251 | $t_{su(\text{cmdV-clkH})}$ | Setup time, MMCi_CMD valid before MMCi_CLK rising clock edge      | 2.9  |     | ns   |
| SDR252 | $t_{h(\text{clkH-cmdV})}$  | Hold time, MMCi_CMD valid after MMCi_CLK rising clock edge        | 1.75 |     | ns   |
| SDR253 | $t_{su(\text{dV-clkH})}$   | Setup time, MMCi_DAT[j:0] valid before MMCi_CLK rising clock edge | 2.9  |     | ns   |
| SDR254 | $t_{h(\text{clkH-dV})}$    | Hold time, MMCi_DAT[j:0] valid after MMCi_CLK rising clock edge   | 1.75 |     | ns   |

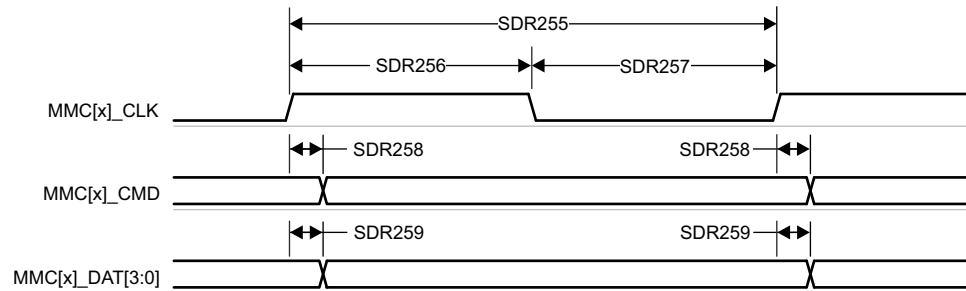
**Table 6-60. Switching Characteristics for MMCi - SDR25, 1.8-V High-Speed SDR Mode**

| NO.    | PARAMETER                 | DESCRIPTION                                                        | MIN  | MAX   | UNIT |
|--------|---------------------------|--------------------------------------------------------------------|------|-------|------|
| SDR255 | $f_{op(\text{clk})}$      | Operating frequency, MMCi_CLK                                      |      | 50    | MHz  |
| SDR256 | $t_{w(\text{clkH})}$      | Pulse duration, MMCi_CLK high                                      | 9.2  |       | ns   |
| SDR257 | $t_{w(\text{clkL})}$      | Pulse duration, MMCi_CLK low                                       | 9.2  |       | ns   |
| SDR258 | $t_{d(\text{clkH-cmdV})}$ | Delay time, MMCi_CLK rising clock edge to MMCi_CMD transition      | 2.32 | 13.18 | ns   |
| SDR259 | $t_{d(\text{clkH-dV})}$   | Delay time, MMCi_CLK rising clock edge to MMCi_DAT[j:0] transition | 2.32 | 13.18 | ns   |

A. There are two MMCi modules: MMC0 and MMC1



**Figure 6-78. eMMC/SD/SDIO in - SDR25, 1.8-V High-Speed SDR - Receiver Mode**



**Figure 6-79. eMMC/SD/SDIO in - SDR25, 1.8-V High-Speed SDR - Transmitter Mode**

#### 6.9.5.16.1.5 UHS-I DDR50 Mode

Table 6-61 and Table 6-62 present Timing requirements and Switching characteristics for MMCi - DDR50, 1.8-V and 3.3-V High-Speed DDR in receiver and transmitter mode (see Figure 6-80 and Figure 6-81).

**Table 6-61. MMCi - 1.8-V, 3.3-V High-Speed DDR Timing Requirements**

| NO. <sup>(1)</sup> | PARAMETER <sup>(2)</sup> |                                                              | MIN  | MAX | UNIT |
|--------------------|--------------------------|--------------------------------------------------------------|------|-----|------|
| DDR505             | $t_{su(cmdV-clkH)}$      | Setup time, MMCi_CMD valid before MMCi_CLK rising clock edge | 8.08 |     | ns   |
| DDR506             | $t_{h(clkH-cmdV)}$       | Hold time, MMCi_CMD valid after MMCi_CLK rising clock edge   | 1.99 |     | ns   |
| DDR507             | $t_{su(dV-clk)}$         | Setup time, MMCi_DAT[j:0] valid before MMCi_CLK transition   | 2.59 |     | ns   |
| DDR508             | $t_{h(clk-dV)}$          | Hold time, MMCi_DAT[j:0] valid after MMCi_CLK transition     | 1.75 |     | ns   |

(1) j in [j:0] is equal to 7 (for MMC0).

(2) Timing requirements for 50 MHz DDR is only applicable when interfacing with JEDEC eMMC devices. Tuning should be done if interfacing to SD/SDIO devices.

**Table 6-62. MMCi - DDR50, 1.8-V/3.3-V High-Speed DDR Switching Characteristics**

| NO.    | PARAMETER         | DESCRIPTION                                                   | MIN   | MAX   | UNIT |
|--------|-------------------|---------------------------------------------------------------|-------|-------|------|
| DDR500 | $f_{op(clk)}$     | Operating frequency, MMCi_CLK                                 |       | 40    | MHz  |
| DDR501 | $t_{w(clkH)}$     | Pulse duration, MMCi_CLK high                                 | 11.58 |       | ns   |
| DDR502 | $t_{w(clkL)}$     | Pulse duration, MMCi_CLK low                                  | 11.58 |       | ns   |
| DDR503 | $t_{d(clk-cmdV)}$ | Delay time, MMCi_CLK rising clock edge to MMCi_CMD transition | 3.32  | 18.06 | ns   |
| DDR504 | $t_{d(clk-dV)}$   | Delay time, MMCi_CLK transition to MMCi_DAT[j:0] transition   | 2.82  | 8.87  | ns   |

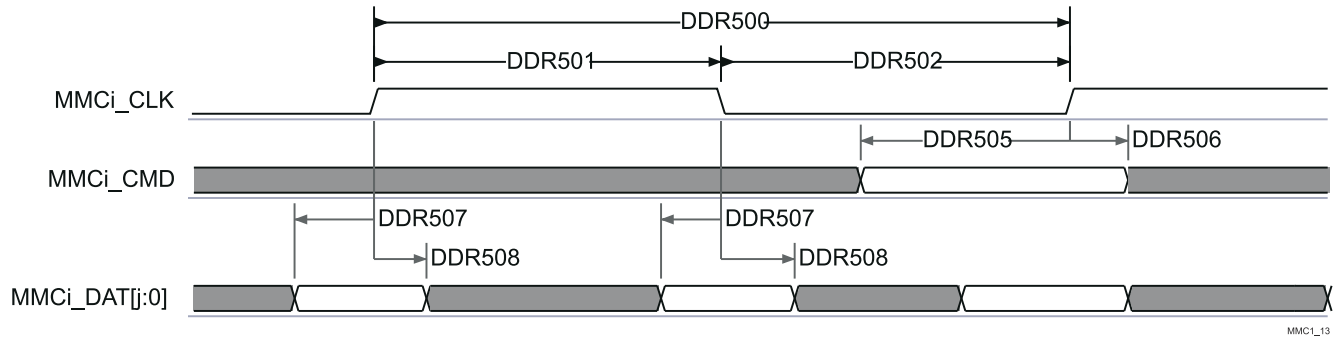


Figure 6-80. eMMC/SD/SDIO - High-Speed DDR - Receive Mode

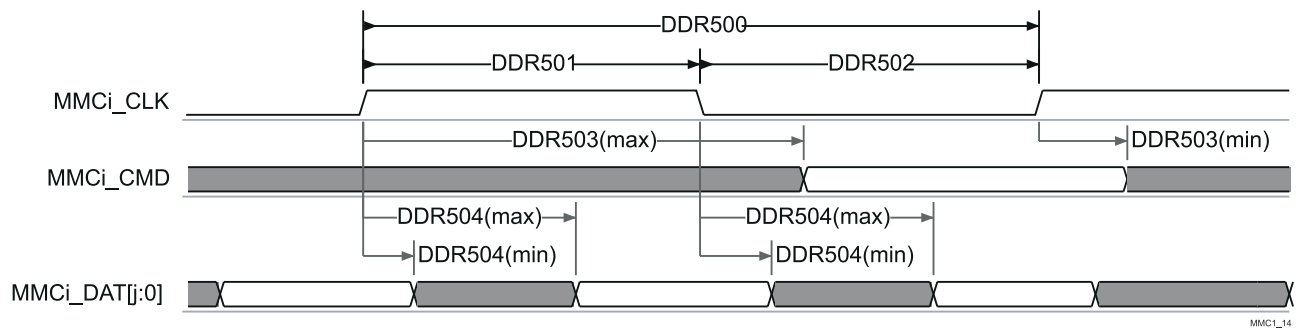


Figure 6-81. eMMC/SD/SDIO - High-Speed DDR - DDR50 - Transmit Mode

#### 6.9.5.16.1.6 UHS-I SDR50 Mode

Table 6-63 present Switching Characteristics for MMCi - SDR50 in transmitter mode (see Figure 6-82).

Table 6-63. Switching Characteristics for MMCi - SDR50 Mode

| NO.     | PARAMETER          | DESCRIPTION                                                        | MIN  | MAX  | UNIT |
|---------|--------------------|--------------------------------------------------------------------|------|------|------|
| SDR501  | $f_{op}(clk)$      | Operating frequency, MMCi_CLK                                      |      | 100  | MHz  |
| SDR502H | $t_{w}(clkH)$      | Pulse duration, MMCi_CLK high                                      | 4.45 |      | ns   |
| SDR502L | $t_{w}(clkL)$      | Pulse duration, MMCi_CLK low                                       | 4.45 |      | ns   |
| SDR505  | $t_{d}(clkH-cmdV)$ | Delay time, MMCi_CLK rising clock edge to MMCi_CMD transition      | 1.12 | 6.43 | ns   |
| SDR506  | $t_{d}(clkH-dV)$   | Delay time, MMCi_CLK rising clock edge to MMCi_DAT[j:0] transition | 1.12 | 6.43 | ns   |

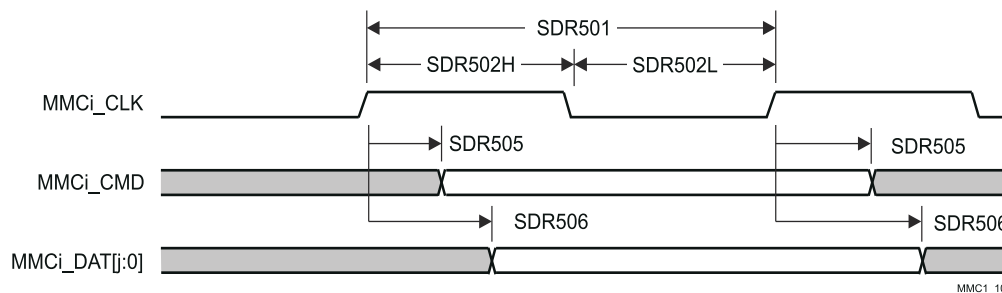


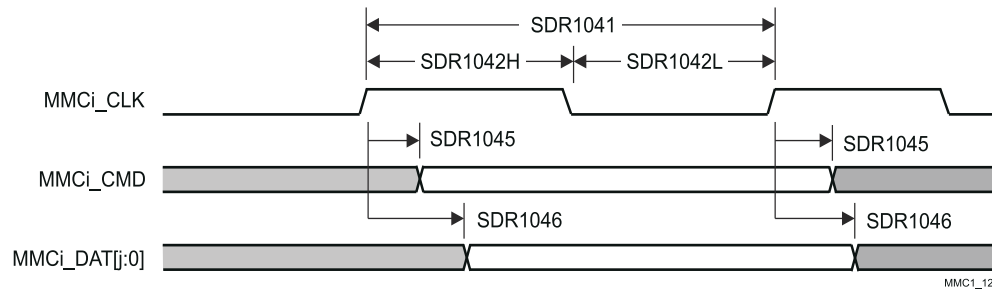
Figure 6-82. eMMC/SD/SDIO in - High Speed SDR50 - Transmitter Mode

#### 6.9.5.16.1.7 UHS-I SDR104 / HS200 Mode

Table 6-64 presents Switching characteristics for MMCi - SDR104, HS200 in transmitter mode (see Figure 6-83)

**Table 6-64. Switching Characteristics for MMCi - SDR104, HS200 Mode**

| NO.      | PARAMETER          | DESCRIPTION                                                        | MIN  | MAX  | UNIT |
|----------|--------------------|--------------------------------------------------------------------|------|------|------|
| SDR1041  | $f_{op}(clk)$      | Operating frequency, MMCi_CLK                                      |      | 200  | MHz  |
| SDR1042H | $t_{w}(clkH)$      | Pulse duration, MMCi_CLK high                                      | 2.08 |      | ns   |
| SDR1042L | $t_{w}(clkL)$      | Pulse duration, MMCi_CLK low                                       | 2.08 |      | ns   |
| SDR1045  | $t_{d}(clkH-cmdV)$ | Delay time, MMCi_CLK rising clock edge to MMCi_CMD transition      | 1.12 | 3.16 | ns   |
| SDR1046  | $t_{d}(clkH-dV)$   | Delay time, MMCi_CLK rising clock edge to MMCi_DAT[j:0] transition | 1.12 | 3.16 | ns   |



**Figure 6-83. eMMC/SD/SDIO in - High Speed SDR104, HS200 - Transmitter Mode**

For more information, see section *Multimedia Card/Secure Digital (eMMC/SD/SDIO) Interface* in the device TRM.

#### 6.9.5.17 CPTS

Table 6-65 presents CPTS Timing Conditions.

**Table 6-65. CPTS Timing Conditions**

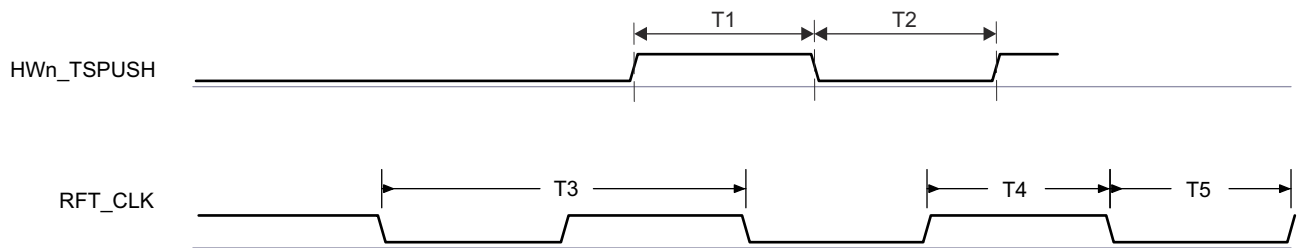
| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| $SR_i$                   | Input slew rate         | 0.5 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| $C_L$                    | Output load capacitance | 2   | 10  | pF   |

Section 6.9.5.17.1, Section 6.9.5.17.2, Figure 6-84, and Figure 6-85 present timing requirement and switching characteristics of the CPTS interface.

##### 6.9.5.17.1 CPTS Timing Requirements

| NO. | PARAMETER          | DESCRIPTION                                   | MIN              | MAX | UNIT |
|-----|--------------------|-----------------------------------------------|------------------|-----|------|
| T1  | $t_{w}(HWTSPUSHH)$ | HWnTSPUSH <sup>(2)</sup> pulse duration, high | $6 + 12P^{(1)}$  |     | ns   |
| T2  | $t_{w}(HWTSPUSHL)$ | HWnTSPUSH <sup>(2)</sup> pulse duration, low  | $6 + 12P^{(1)}$  |     | ns   |
| T3  | $t_c(RFT\_CLK)$    | RFT_CLK cycle time                            | 5                | 8   | ns   |
| T4  | $t_w(RFT\_CLKH)$   | RFT_CLK pulse duration, high                  | $0.45 * T^{(3)}$ |     | ns   |
| T5  | $t_w(RFT\_CLKL)$   | RFT_CLK pulse duration, low                   | $0.45 * T^{(3)}$ |     | ns   |

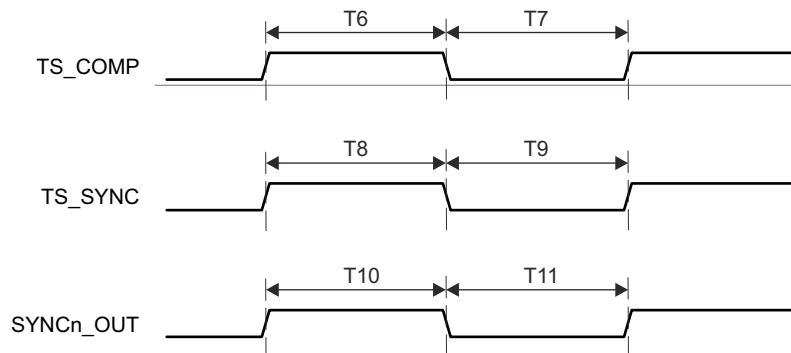
- (1) P = functional clock period in ns.  
(2) In HWnTSPUSH, n = 1 to 2.  
(3) T = RFT\_CLK period in ns.

**Figure 6-84. CPTS Input Timing****6.9.5.17.2 CPTS Switching Characteristics**

| NO. | PARAMETER            | DESCRIPTION                                   | SOURCE  | MIN            | MAX | UNIT |
|-----|----------------------|-----------------------------------------------|---------|----------------|-----|------|
| T6  | $t_{w(TS\_COMP)}$    | Pulse duration, TS_COMP high                  |         | $-6+36P^{(1)}$ |     | ns   |
| T7  | $t_{w(TS\_COMPL)}$   | Pulse duration, TS_COMP low                   |         | $-6+36P^{(1)}$ |     | ns   |
| T8  | $t_{w(TS\_SYNCH)}$   | Pulse duration, TS_SYNC high                  |         | $-6+36P^{(1)}$ |     | ns   |
| T9  | $t_{w(TS\_SYNCL)}$   | Pulse duration, TS_SYNC low                   |         | $-6+36P^{(1)}$ |     | ns   |
| T10 | $t_{w(SYNCL\_OUTH)}$ | Pulse duration, SYNCn_OUT <sup>(2)</sup> high | TS_SYNC | $-6+36P^{(1)}$ |     | ns   |
|     |                      |                                               | TS_GENF | $-6+5P^{(1)}$  |     | ns   |
| T11 | $t_{w(SYNCL\_OUTL)}$ | Pulse duration, SYNCn_OUT <sup>(2)</sup> low  | TS_SYNC | $-6+36P^{(1)}$ |     | ns   |
|     |                      |                                               | TS_GENF | $-6+5P^{(1)}$  |     | ns   |

(1) P = functional clock period in ns.

(2) n = 0 to 3 in SYNCn\_OUT

**Figure 6-85. CPTS Switching Characteristics**

For more information, see section *Navigator Subsystem (NAVSS)* section in *Data Movement Architecture (DMA)* chapter in the device TRM.

### 6.9.5.18 OSPI

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

[Table 6-66](#) presents timing conditions for OSPI.

**Table 6-66. OSPI Timing Conditions**

| PARAMETER                             |                                                                                                   |                                             | MIN                    | MAX                    | UNIT |
|---------------------------------------|---------------------------------------------------------------------------------------------------|---------------------------------------------|------------------------|------------------------|------|
| <b>INPUT CONDITIONS</b>               |                                                                                                   |                                             |                        |                        |      |
| SR <sub>I</sub>                       | Input slew rate                                                                                   | All modes                                   | 1                      | 6                      | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                                                                                   |                                             |                        |                        |      |
| C <sub>L</sub>                        | Output load capacitance                                                                           | All modes                                   | 3                      | 10                     | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                                                                                   |                                             |                        |                        |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay OSPI_CLK trace                                                                  | Internal Loopback;<br>Internal Pad Loopback |                        | 450                    | ps   |
|                                       | Propagation delay OSPI_LBCLKO trace                                                               | External Board Loopback                     | 2*L <sup>(2)</sup> .30 | 2*L <sup>(2)</sup> +30 | ps   |
|                                       | Propagation delay OSPI_DQS trace                                                                  | DQS                                         | L <sup>(2)</sup> .30   | L <sup>(2)</sup> +30   | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch OSPI_D[i:0] <sup>(1)</sup> , OSPI_CS <sub>n</sub> relative to OSPI_CLK | All modes                                   |                        | 60                     | ps   |

(1) i in D[i:0] = 0 to 7 for OSPI0; i in [i:0] = 3 for OSPI1

(2) L = Propagation delay of OSPI\_CLK trace

#### 6.9.5.18.1 OSPI with Data Training

##### Note

I/O timing requirements and switching characteristics are not applicable when OSPI is used with data training. Follow the [Section 8.2.2, OSPI and QSPI Board Design and Layout Guidelines](#) to ensure proper operation.

##### 6.9.5.18.1.1 OSPI Switching Characteristics - Data Training

| PARAMETER            |                 | MODE      | MIN  | MAX | UNIT |
|----------------------|-----------------|-----------|------|-----|------|
| t <sub>c</sub> (CLK) | Cycle time, CLK | 1.8V, SDR | 5.00 |     | ns   |
|                      |                 | 3.3V, SDR | 7.52 |     | ns   |
|                      |                 | 1.8V, DDR | 6.02 |     | ns   |
|                      |                 | 3.3V, DDR | 7.52 |     | ns   |

#### 6.9.5.18.2 OSPI without Data Training

##### Note

The I/O Timings provided in this section are only applicable when data training is not implemented. Additionally, the I/O Timings are valid only for some OSPI usage modes when the corresponding DLL Delays are configured as described in [Table 6-67](#) found in this section.

[Section 6.9.5.18.2.4](#), [Section 6.9.5.18.2.2](#), [Figure 6-90](#), and [Figure 6-88](#) present switching characteristics for OSPI DDR and SDR Mode.

### 6.9.5.18.2.1 OSPI Timing Requirements - SDR Mode

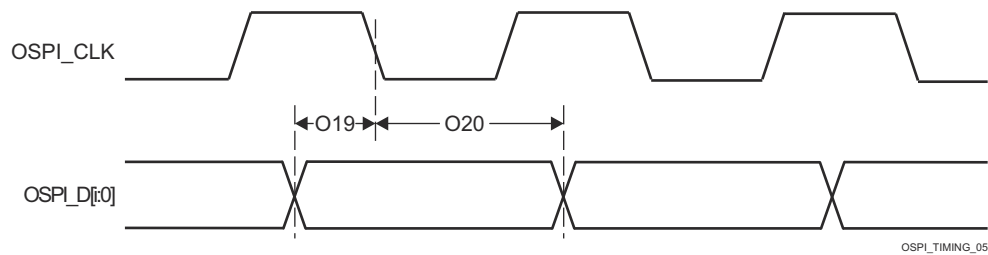
**Table 6-67. OSPI DLL Delay Mapping - SDR Timing Modes**

| MODE      | OSPI_PHY_CONFIGURATION_REG<br>BIT FIELD | DELAY VALUE |
|-----------|-----------------------------------------|-------------|
| All modes | PHY_CONFIG_TX_DLL_DELAY_FLD             | 0x0         |
|           | PHY_CONFIG_RX_DLL_DELAY_FLD             | 0x0         |

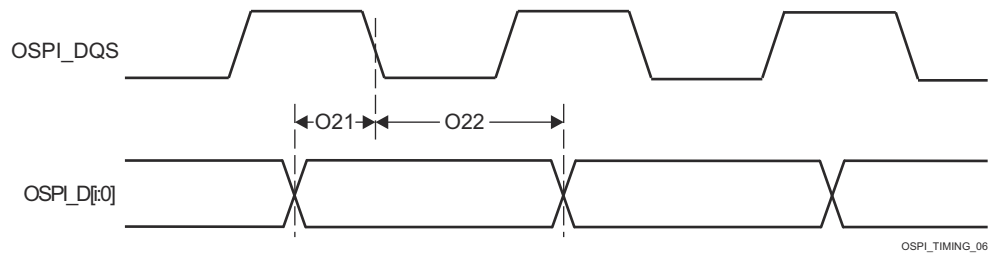
see [Figure 6-86](#) and [Figure 6-87](#)

| NO. |                   |                                                                              | MODE                          | MIN   | MAX | UNIT |
|-----|-------------------|------------------------------------------------------------------------------|-------------------------------|-------|-----|------|
| O19 | $t_{su}(D-CLK)$   | Setup time, D[i:0] valid before active CLK edge <sup>(1)</sup>               | 1.8V, Internal Loopback       | -2.18 |     | ns   |
|     |                   |                                                                              | 3.3V, Internal Loopback       | -1.7  |     | ns   |
| O20 | $t_h(CLK-D)$      | Hold time, D[i:0] valid after active CLK edge <sup>(1)</sup>                 | 1.8V, Internal Loopback       | 7.62  |     | ns   |
|     |                   |                                                                              | 3.3V, Internal Loopback       | 8.1   |     | ns   |
| O21 | $t_{su}(D-LBCLK)$ | Setup time, D[i:0] valid before active LBCLK input (DQS) edge <sup>(1)</sup> | 1.8V, External Board Loopback | -3.24 |     | ns   |
|     |                   |                                                                              | 3.3V, External Board Loopback | -2.72 |     | ns   |
| O22 | $t_h(LBCLK-D)$    | Hold time, D[i:0] valid after active LBCLK input (DQS) edge <sup>(1)</sup>   | 1.8V, External Board Loopback | 3.81  |     | ns   |
|     |                   |                                                                              | 3.3V, External Board Loopback | 4.33  |     | ns   |

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1



**Figure 6-86. OSPI Timing Requirements - SDR, Internal Clock and Internal Pad Loopback Clock**



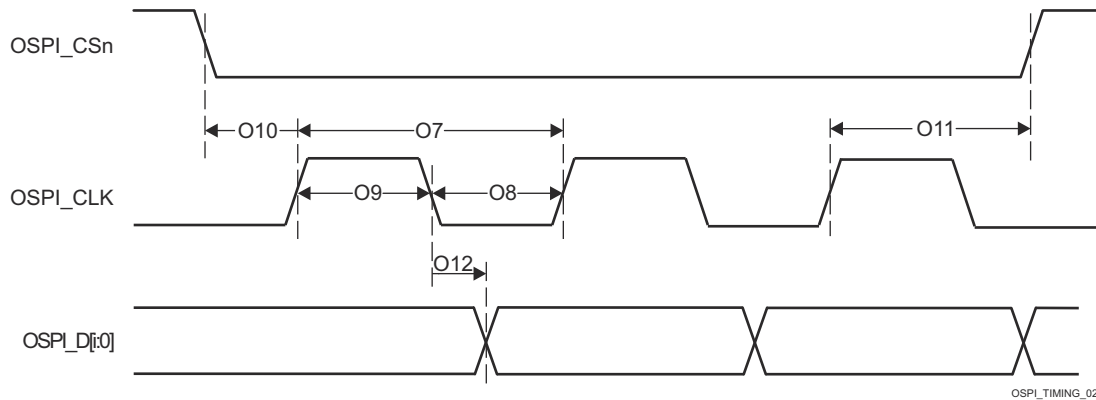
**Figure 6-87. OSPI Timing Requirements - SDR, External Loopback Clock**

### 6.9.5.18.2.2 OSPI Switching Characteristics - SDR Mode

| NO. |             | DESCRIPTION <sup>(1)</sup> | MODE | MIN                          | MAX | UNIT |
|-----|-------------|----------------------------|------|------------------------------|-----|------|
| O7  | $t_c(CLK)$  | Cycle time, CLK            | 1.8V | 7                            |     | ns   |
|     |             |                            | 3.3V | 7.52                         |     | ns   |
| O8  | $t_w(CLKL)$ | Pulse duration, CLK low    |      | $-0.3+0.475 \times P$<br>(1) |     | ns   |
| O9  | $t_w(CLKH)$ | Pulse duration, CLK high   |      | $-0.3+0.475 \times P$<br>(1) |     | ns   |

| NO. | DESCRIPTION <sup>(1)</sup> |                                                  | MODE | MIN                                                          | MAX                                                          | UNIT |
|-----|----------------------------|--------------------------------------------------|------|--------------------------------------------------------------|--------------------------------------------------------------|------|
| O10 | $t_{d(CLK-CSn)}$           | Delay time, CLK rising edge to CSn active edge   | 1.8V | $0.475 \times P + 0.975 \times N \times R - 1^{(1) (2) (4)}$ | $0.475 \times P + 0.975 \times N \times R + 1^{(1) (2) (4)}$ | ns   |
|     |                            |                                                  | 3.3V | $0.475 \times P + 0.975 \times N \times R - 1^{(1) (2) (4)}$ | $0.475 \times P + 0.975 \times N \times R + 1^{(1) (2) (4)}$ | ns   |
| O11 | $t_{d(CLK-CSn)}$           | Delay time, CLK rising edge to CSn inactive edge | 1.8V | $0.475 \times P + 0.975 \times N \times R - 1^{(1) (3) (4)}$ | $0.475 \times P + 0.975 \times N \times R + 1^{(1) (3) (4)}$ | ns   |
|     |                            |                                                  | 3.3V | $0.475 \times P + 0.975 \times N \times R - 1^{(1) (3) (4)}$ | $0.475 \times P + 0.975 \times N \times R + 1^{(1) (3) (4)}$ | ns   |
| O12 | $t_{d(CLK-D)}$             | Delay time, CLK active edge to D[i:0] transition | 1.8V | -1.15                                                        | 1.25                                                         | ns   |
|     |                            |                                                  | 3.3V | -1.33                                                        | 1.51                                                         | ns   |

- (1) P = CLK cycle time = SCLK period  
(2) N = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]  
(3) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]  
(4) R = refclk



**Figure 6-88. OSPI Switching Characteristics - SDR**

Section 6.9.5.18.2.3, Section 6.9.5.18.2.1, Figure 6-89, and Figure 6-87 presents timing requirements for OSPI DDR and SDR Mode.

#### 6.9.5.18.2.3 OSPI Timing Requirements - DDR Mode

**Table 6-68. OSPI DLL Delay Mapping - DDR Timing Modes**

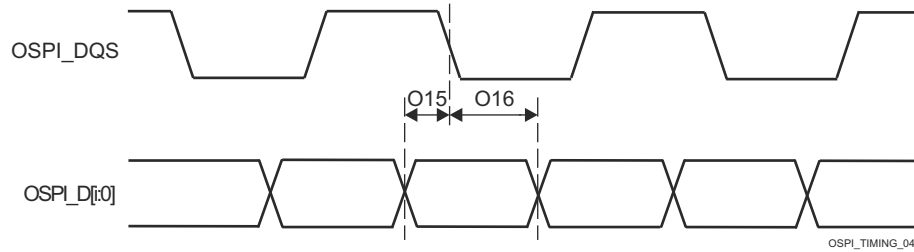
| OSPI Instance | MODE         | OSPI_PHY_CONFIGURATION_REG BIT FIELD | DELAY VALUE |
|---------------|--------------|--------------------------------------|-------------|
| OSPI0         | 1.8V         | PHY_CONFIG_TX_DLL_DELAY_FLD          | 0x41        |
|               | 3.3V         | PHY_CONFIG_TX_DLL_DELAY_FLD          | 0x46        |
|               | 1.8V DQS     | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x16        |
|               | 3.3V DQS     | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x3E        |
|               | Non-PHY mode | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x0         |
| OSPI1         | 1.8V         | PHY_CONFIG_TX_DLL_DELAY_FLD          | 0x44        |
|               | 3.3V         | PHY_CONFIG_TX_DLL_DELAY_FLD          | 0x4C        |
|               | 1.8V DQS     | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x16        |
|               | 3.3V DQS     | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x40        |
|               | Non-PHY mode | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x0         |



**Table 6-69. OSPI Timing Requirements - DDR Mode**see [Figure 6-89](#)

| NO. |                   |                                                                        | MODE                          | MIN                 | MAX | UNIT |
|-----|-------------------|------------------------------------------------------------------------|-------------------------------|---------------------|-----|------|
| O15 | $t_{su(D-LBCLK)}$ | Setup time, D[i:0] <sup>(1)</sup> valid before active LBCLK (DQS) edge | 1.8V, External Board Loopback | 0.52                |     | ns   |
|     |                   |                                                                        | 3.3V, External Board Loopback | 1.97                |     | ns   |
| O16 | $t_{h(LBCLK-D)}$  | Hold time, D[i:0] <sup>(1)</sup> valid after active LBCLK (DQS) edge   | 1.8V, External Board Loopback | 1.24 <sup>(2)</sup> |     | ns   |
|     |                   |                                                                        | 3.3V, External Board Loopback | 1.44 <sup>(2)</sup> |     | ns   |
| O17 | $t_{su(D-DQS)}$   | Setup time, D[i:0] <sup>(1)</sup> valid before active DQS edge         | 1.8V, DQS                     | -0.46               |     | ns   |
|     |                   |                                                                        | 3.3V, DQS                     | -0.66               |     | ns   |
| O18 | $t_{h(DQS-D)}$    | Hold time, D[i:0] <sup>(1)</sup> valid after active DQS edge           | 1.8V, DQS                     | 3.59                |     | ns   |
|     |                   |                                                                        | 3.3V, DQS                     | 8.89                |     | ns   |

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1

(2) This Hold time requirement is larger than the Hold time provided by a typical flash device. Therefore, the trace length between the SoC and flash device must be sufficiently long enough to ensure that the Hold time is met at the SoC. Refer to [Section 8.2.2](#) for more details.**Figure 6-89. OSPI Timing Requirements - DDR, External Loopback Clock and DQS****6.9.5.18.2.4 OSPI Switching Characteristics - DDR Mode**

| NO. | PARAMETER        | DESCRIPTION                                                     | MODE  | MIN                                                             | MAX                                                             | UNIT |
|-----|------------------|-----------------------------------------------------------------|-------|-----------------------------------------------------------------|-----------------------------------------------------------------|------|
| O1  | $t_{c(CLK)}$     | Cycle time, CLK                                                 |       | 19                                                              |                                                                 | ns   |
| O2  | $t_{w(CLKL)}$    | Pulse duration, CLK low                                         |       | $-0.3 + 0.475 \times P$<br>(2)                                  |                                                                 | ns   |
| O3  | $t_{w(CLKH)}$    | Pulse duration, CLK high                                        |       | $-0.3 + 0.475 \times P$<br>(2)                                  |                                                                 | ns   |
| O4  | $t_{d(CLK-CSn)}$ | Delay time, CSn active edge to CLK rising edge                  | 1.8 V | $0.475 \times P + 0.975 \times N \times R$<br>(2) (3) (5)       | $0.475 \times P + 0.975 \times N \times R + 7.7$<br>(2) (3) (5) | ns   |
|     |                  |                                                                 | 3.3 V | $0.475 \times P + 0.975 \times N \times R$<br>(2) (3) (5)       | $0.475 \times P + 0.975 \times N \times R + 8$<br>(2) (3) (5)   | ns   |
| O5  | $t_{d(CLK-CSn)}$ | Delay time, CLK rising edge to CSn inactive edge                | 1.8 V | $0.475 \times P + 0.975 \times N \times R - 7.7$<br>(2) (4) (5) | $0.475 \times P + 0.975 \times N \times R$<br>(2) (4) (5)       | ns   |
|     |                  |                                                                 | 3.3 V | $0.475 \times P + 0.975 \times N \times R - 8$<br>(2) (4) (5)   | $0.475 \times P + 0.975 \times N \times R$<br>(2) (4) (5)       | ns   |
| O6  | $t_{d(CLK-D)}$   | Delay time, CLK active edge to D[i:0] <sup>(1)</sup> transition | 1.8 V | -7.7                                                            | -1.56                                                           | ns   |
|     |                  |                                                                 | 3.3 V | -7.7                                                            | -1.56                                                           | ns   |

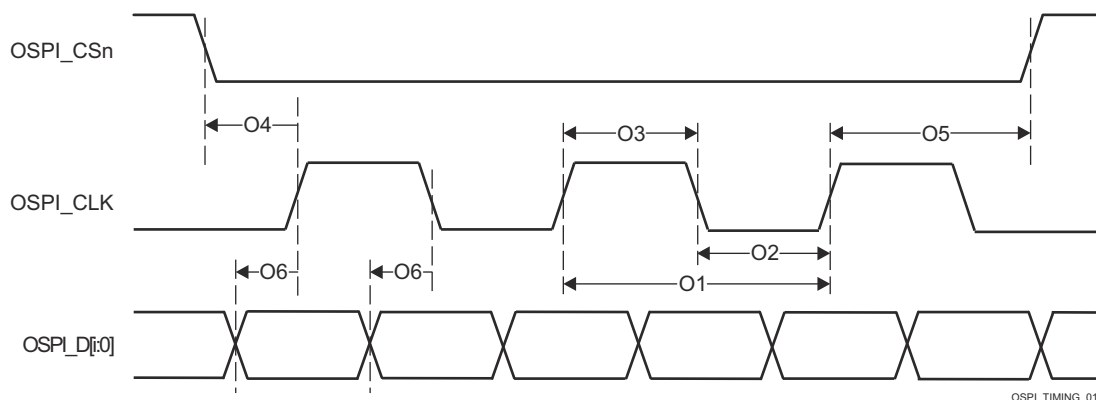
(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1

(2) P = CLK cycle time = SCLK period

(3) N = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]

(4) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]

(5) R = refclk



**Figure 6-90. OSPI Switching Characteristics - DDR**

For more information, see section *Octal Serial Peripheral Interface (OSPI)* in the device TRM.

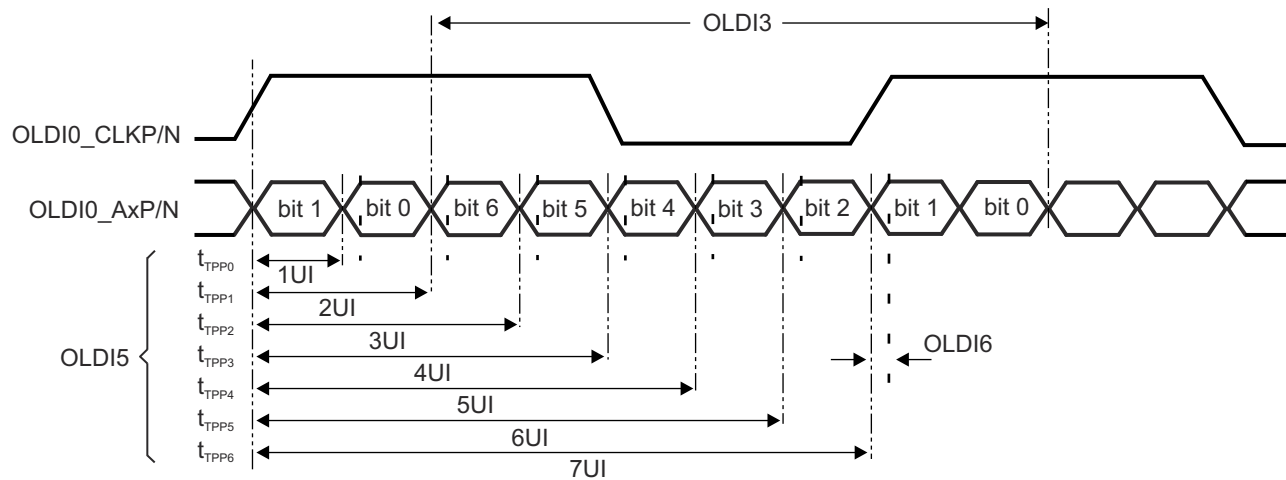
### 6.9.5.19 OLDI

#### 6.9.5.19.1 OLDI Switching Characteristics

| NO.   | PARAMETER              | DESCRIPTION <sup>(1)</sup>                                                                                                                         | MIN  | TYP | MAX    | UNIT              |
|-------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|------|-----|--------|-------------------|
| OLDI1 | $t_{i(LHTT)}$          | Low-to-high transition time of LVDS differential signals:<br>OLDI0_CLKP/N, OLDI0_AxP/N, x = [3:0], with BOOSTA_EN = 0<br>(Fast rise/fall disabled) |      |     | 0.5    | ns                |
|       |                        | Low-to-high transition time of LVDS differential signals:<br>OLDI0_CLKP/N, OLDI0_AxP/N, x = [3:0], with BOOSTA_EN = 1<br>(Fast rise/fall enabled)  |      |     | 0.25   | ns                |
| OLDI2 | $t_{i(HLTT)}$          | High-to-low transition time of LVDS differential signals:<br>OLDI0_CLKP/N, OLDI0_AxP/N, x = [3:0], with BOOSTA_EN = 0<br>(Fast rise/fall disabled) |      |     | 0.5    | ns                |
|       |                        | High-to-low transition time of LVDS differential signals:<br>OLDI0_CLKP/N, OLDI0_AxP/N, x = [3:0], with BOOSTA_EN = 1<br>(Fast rise/fall enabled)  |      |     | 0.25   | ns                |
| OLDI3 | $t_{c(CLK)}$           | Output pixel clock period (OLDI0_CLKP/N)                                                                                                           | 6.06 |     | 110.01 | ns                |
| OLDI4 | $t_{w(BIT)}$           | Output bit width (OLDI0_AxP/N, x = [3:0])                                                                                                          |      | 1   |        | UI <sup>(2)</sup> |
| OLDI5 | $t_{i(TPPx, x=[6:0])}$ | Output pulse positions normalized for each bit (OLDI0_AxP/N, x = [3:0])                                                                            |      | 7-1 |        | UI <sup>(2)</sup> |
| OLDI6 | $\Delta t_{i(TPP)}$    | Variation of pulse positions for each bit from their normalized center (OLDI0_AxP/N, x = [3:0])                                                    |      |     | 0.1    | UI <sup>(2)</sup> |
| OLDI7 | $t_{sk(TCCS)}$         | Output channel to channel skew (OLDI0_CLKP/N, OLDI0_AxP/N, x = [3:0])                                                                              |      |     | 50     | ps                |
| OLDI8 | $t_{j(TJCC)}$          | Output jitter cycle-to-cycle (OLDI0_CLKP/N, OLDI0_AxP/N, x = [3:0])                                                                                |      |     | 0.04   | UI <sup>(2)</sup> |
| OLDI9 | $t_{j(IJIT)}$          | Total jitter tolerance (Includes data to clock skew, pulse position variation from normalized edges (OLDI0_AxP/N, x = [3:0])                       |      |     | 0.25   | UI <sup>(2)</sup> |

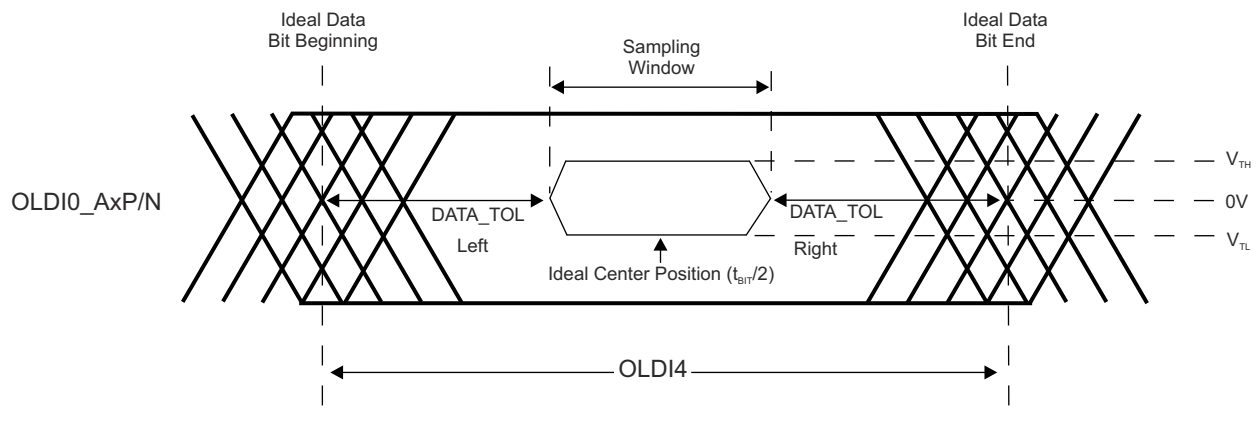
(1) Measured based on 20% - 80% transitions and PCB trace of ~2in with 100  $\Omega$  termination on differential lines.

(2) UI =  $t_{c(CLK)} / 7$



A. x in OLDI0\_AxP/N = [3:0]

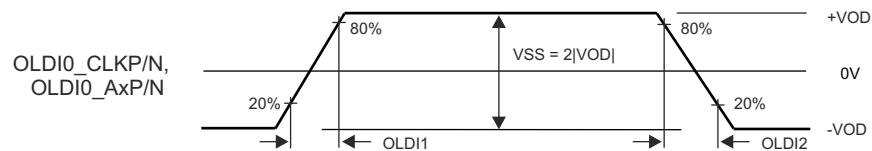
**Figure 6-91. OLDI Output Pulse Positions**



A.  $OLDI9 = DATA\_TOL (Left + Right)$

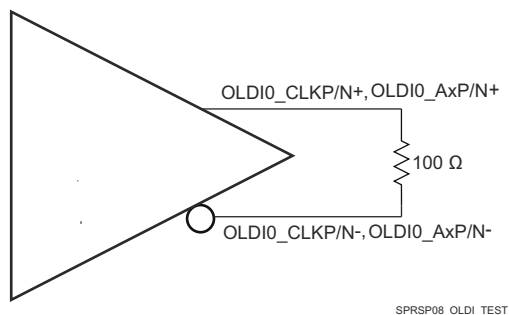
B. x in OLDI0\_AxP/N = [3:0]

**Figure 6-92. OLDI Data Output Jitter**



A. x in OLDI0\_AxP/N = [3:0]

**Figure 6-93. LVDS Output Transition Times**



A. x in OLDI0\_AxP/N = [3:0]

**Figure 6-94. LVDS Output Load**

For more information, see section *Display Subsystem (DSS)* in the device TRM.

### 6.9.5.20 PCIe

The PCI-Express Subsystem is compliant with the PCI Express Base Specification, revision 3.1. Refer to the specification for timing details.

For more details about features and additional description information on the device Peripheral Component Interconnect Express, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

### 6.9.5.21 PRU\_ICSSG

The device has integrated three identical PRU\_ICSSG subsystems (PRU\_ICSSG0, PRU\_ICSSG1 and PRU\_ICSSG2). The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

For more details about features and additional description information on the device Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

#### 6.9.5.21.1 Programmable Real-Time Unit (PRU\_ICSSG PRU)

##### Note

The PRU\_ICSSG PRU signals have different functionality depending on the mode of operation. The signal naming in this section matches the naming used in the PRU Module Interface section in the device TRM.

[Table 6-70](#) presents the PRU timing conditions.

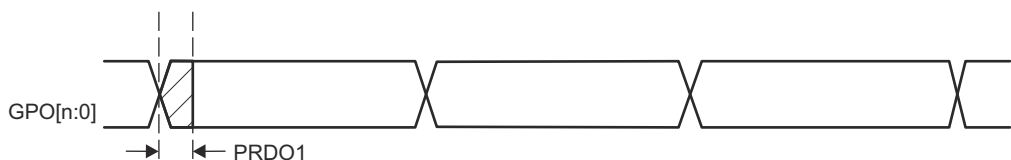
**Table 6-70. PRU\_ICSSG PRU Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 1.5 | 3   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 30  | pF   |

#### 6.9.5.21.1.1 PRU\_ICSSG PRU Direct Input/Output Mode Electrical Data and Timing

##### 6.9.5.21.1.1.1 PRU\_ICSSG PRU Switching Characteristics - Direct Output Mode

| NO.   | PARAMETER                 |                  | MIN | MAX | UNIT |
|-------|---------------------------|------------------|-----|-----|------|
| PRDO1 | t <sub>sk</sub> (GPO-GPO) | Skew, GPO to GPO |     | 4   | ns   |



SPRS91x\_TIMING\_PRU\_02

**Figure 6-95. PRU\_ICSSG PRU Direct Output Timing**

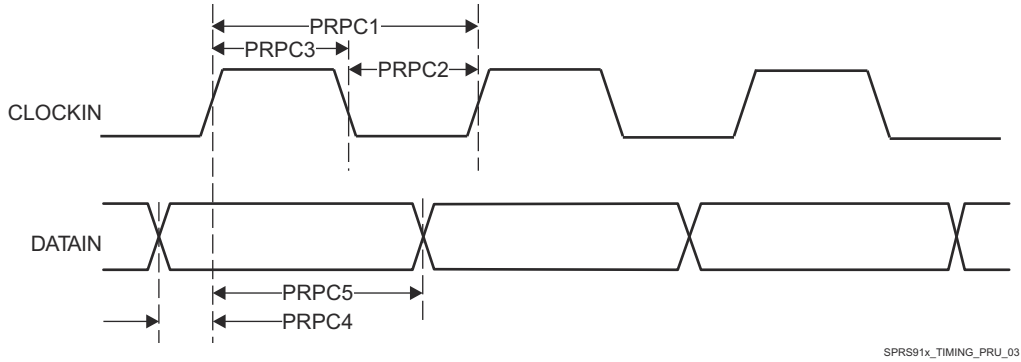
A. n in GPO[n:0] = 19.

### 6.9.5.21.1.2 PRU\_ICSSG PRU Parallel Capture Mode Electrical Data and Timing

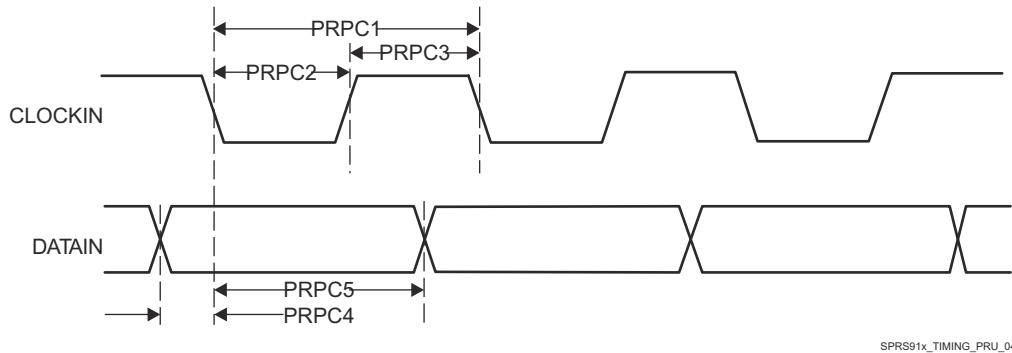
#### 6.9.5.21.1.2.1 PRU\_ICSSG PRU Timing Requirements - Parallel Capture Mode

See Figure 6-96 and Figure 6-97

| NO.   |                        |                                                     | MIN | MAX | UNIT |
|-------|------------------------|-----------------------------------------------------|-----|-----|------|
| PRPC1 | $t_{c(CLOCK)}$         | Cycle time, CLOCKIN                                 | 20  |     | ns   |
| PRPC2 | $t_{w(CLOCKL)}$        | Pulse Duration, CLOCKIN Low                         | 10  |     | ns   |
| PRPC3 | $t_{w(CLOCKH)}$        | Pulse Duration, CLOCKIN High                        | 10  |     | ns   |
| PRPC4 | $t_{su(DATAIN-CLOCK)}$ | Setup time, DATAIN valid before CLOCKIN active edge | 4   |     | ns   |
| PRPC5 | $t_{h(CLOCK-DATAIN)}$  | Hold time, DATAIN valid after CLOCKIN active edge   | 0.6 |     | ns   |



**Figure 6-96. PRU\_ICSSG PRU Parallel Capture Timing – Rising Edge Mode**



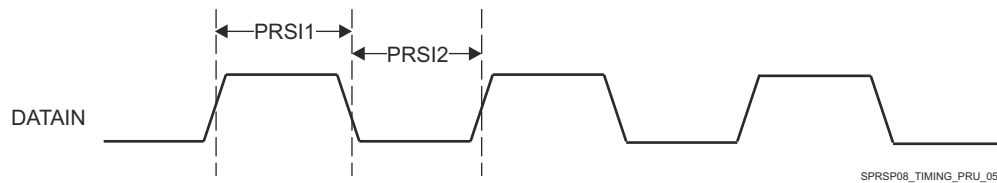
**Figure 6-97. PRU\_ICSSG PRU Parallel Capture Timing – Falling Edge Mode**

### 6.9.5.21.1.3 PRU\_ICSSG PRU Shift Mode Electrical Data and Timing

#### 6.9.5.21.1.3.1 PRU\_ICSSG PRU Timing Requirements - Shift In Mode

| NO.   |                       |                                 | MIN                  | MAX | UNIT |
|-------|-----------------------|---------------------------------|----------------------|-----|------|
| PRSI1 | $t_{w(PRU\_DATAINL)}$ | Pulse Duration, PRU_DATAIN Low  | 2+2×P <sup>(1)</sup> |     | ns   |
| PRSI2 | $t_{w(PRU\_DATAINH)}$ | Pulse Duration, PRU_DATAIN High | 2+2×P <sup>(1)</sup> |     | ns   |

(1) P = Internal shift in clock period, defined by PRU0\_GPI\_DIV0 and PRU0\_GPI\_DIV1 bit fields in the ICSSG\_GPCFGn\_REG register.

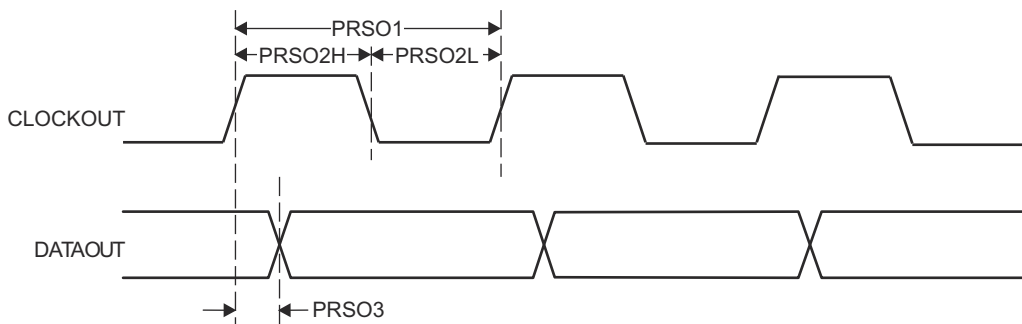


**Figure 6-98. PRU\_ICSSG PRU Shift In Timing**

### 6.9.5.21.1.3.2 PRU\_ICSSG PRU Switching Characteristics - Shift Out Mode

| NO.   | PARAMETER                      |                                     | MIN                                         | MAX | UNIT |
|-------|--------------------------------|-------------------------------------|---------------------------------------------|-----|------|
| PRSO1 | $t_{c}(\text{CLKOUT})$         | Cycle time, CLKOUT                  | 10                                          |     | ns   |
| PRSO2 | $t_{w}(\text{CLKOUTL})$        | Pulse Duration, CLKOUT Low          | $-0.3 + 0.475 \times P \times Z$<br>(1) (2) |     | ns   |
| PRSO3 | $t_{w}(\text{CLKOUTH})$        | Pulse Duration, CLKOUT High         | $-0.3 + 0.475 \times P \times Y$<br>(1) (3) |     | ns   |
| PRSO4 | $t_{d}(\text{CLKOUT-DATAOUT})$ | Delay time, CLKOUT to DATAOUT Valid | -1                                          | 4   | ns   |

- (1) P = Software programmable shift out clock period, defined by PRU0\_GPO\_DIV0 and PRU0\_GPO\_DIV1 bit fields in the GPCFGn register.
- (2) The Z parameter is defined as follows: If PRU0\_GPI\_DIV0 and PRU0\_GPI\_DIV1 are INTEGERS -or- if PRU0\_GPI\_DIV0 is a NON-INTEGERS and PRU0\_GPI\_DIV1 is an EVEN INTEGER then, Z equals  $(\text{PRU0\_GPI\_DIV0} \times \text{PRU0\_GPI\_DIV1})$ . If PRU0\_GPI\_DIV0 is a NON-INTEGERS and PRU0\_GPI\_DIV1 is an ODD INTEGER then, Z equals  $(\text{PRU0\_GPI\_DIV0} \times \text{PRU0\_GPI\_DIV1} + 0.5)$ . If PRU0\_GPI\_DIV0 is an INTEGER and PRU0\_GPI\_DIV1 is a NON-INTEGERS then, Z equals  $(\text{PRU0\_GPI\_DIV0} \times \text{PRU0\_GPI\_DIV1} + 0.5 \times \text{PRU0\_GPI\_DIV0})$ . If PRU0\_GPI\_DIV0 and PRU0\_GPI\_DIV1 are NON-INTEGERS then, Z equals  $(\text{PRU0\_GPI\_DIV0} \times \text{PRU0\_GPI\_DIV1} + 0.25 \times \text{PRU0\_GPI\_DIV0})$ .
- (3) The Y parameter is defined as follows: If PRU0\_GPI\_DIV0 and PRU0\_GPI\_DIV1 are INTEGERS -or- if PRU0\_GPI\_DIV0 is a NON-INTEGERS and PRU0\_GPI\_DIV1 is an EVEN INTEGER then, Y equals  $(\text{PRU0\_GPI\_DIV0} \times \text{PRU0\_GPI\_DIV1})$ . If PRU0\_GPI\_DIV0 is a NON-INTEGERS and PRU0\_GPI\_DIV1 is an ODD INTEGER then, Y equals  $(\text{PRU0\_GPI\_DIV0} \times \text{PRU0\_GPI\_DIV1} - 0.5)$ . If PRU0\_GPI\_DIV0 is an INTEGER and PRU0\_GPI\_DIV1 is a NON-INTEGERS then, Y equals  $(\text{PRU0\_GPI\_DIV0} \times \text{PRU0\_GPI\_DIV1} - 0.5 \times \text{PRU0\_GPI\_DIV0})$ . If PRU0\_GPI\_DIV0 and PRU0\_GPI\_DIV1 are NON-INTEGERS then, Y1 equals  $(\text{PRU0\_GPI\_DIV0} \times \text{PRU0\_GPI\_DIV1} - 0.25 \times \text{PRU0\_GPI\_DIV0})$  and Y2 equals  $(\text{PRU0\_GPI\_DIV0} \times \text{PRU0\_GPI\_DIV1} + 0.25 \times \text{PRU0\_GPI\_DIV0})$ , where Y1 is the first high pulse and Y2 is the second high pulse.



SPRSP08\_TIMING\_PRU\_06

**Figure 6-99. PRU\_ICSSG PRU Shift Out Timing**

### 6.9.5.21.1.4 PRU\_ICSSG PRU Sigma Delta and Peripheral Interface Modes Electrical Data and Timing

Table 6-71 presents PRU Sigma Delta and Peripheral timing conditions.

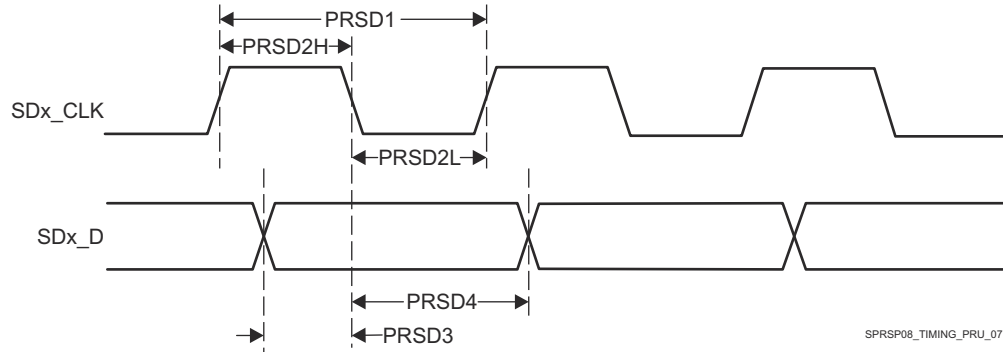
**Table 6-71. PRU\_ICSSG PRU Sigma Delta and Peripheral Interface Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>i</sub>          | Input slew rate         | 1   | 3   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 18  | pF   |

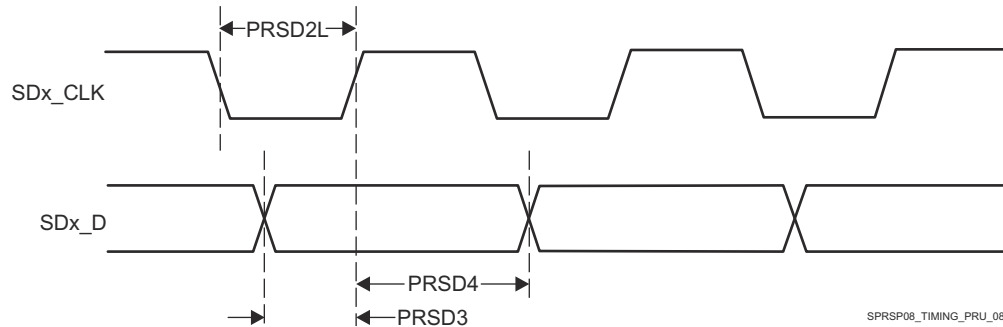
### 6.9.5.21.1.4.1 PRU\_ICSSG PRU Timing Requirements - Sigma Delta Mode

| NO.    | PARAMETER                         |                                                     | MIN | MAX | UNIT |
|--------|-----------------------------------|-----------------------------------------------------|-----|-----|------|
| PRSD1  | $t_{c}(\text{SD\_CLK})$           | Cycle time, SD_CLK                                  | 40  |     | ns   |
| PRSD2L | $t_{w}(\text{SD\_CLKL})$          | Pulse Duration, SD_CLK Low                          | 20  |     | ns   |
| PRSD2H | $t_{w}(\text{SD\_CLKH})$          | Pulse Duration, SD_CLK High                         | 20  |     | ns   |
| PRSD3  | $t_{su}(\text{SD\_DATA-SD\_CLK})$ | Setup time, SD_DATA valid before SD_CLK active edge | 10  |     | ns   |

| NO.   |                           |                                                    | MIN | MAX | UNIT |
|-------|---------------------------|----------------------------------------------------|-----|-----|------|
| PRSD4 | $t_{h(SD\_CLK-SD\_DATA)}$ | Hold time, SD_DATA valid before SD_CLK active edge | 5   |     | ns   |



**Figure 6-100. PRU\_ICSSG PRU SD\_CLK Falling Active Edge**

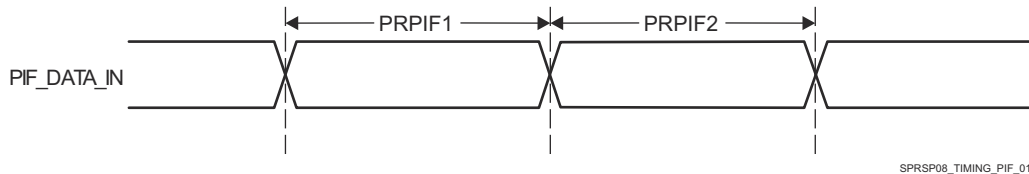


**Figure 6-101. PRU\_ICSSG PRU SD\_CLK Rising Active Edge**

#### 6.9.5.21.1.4.2 PRU\_ICSSG PRU Timing Requirements - Peripheral Interface Mode

| NO.    | PARAMETER               | DESCRIPTION                      | MIN                                   | MAX | UNIT |
|--------|-------------------------|----------------------------------|---------------------------------------|-----|------|
| PRPIF1 | $t_{w(PIF\_DATA\_INH)}$ | Pulse Duration, PIF_DATA_IN High | $2 + 0.475 \times (4 \times P)^{(1)}$ |     | ns   |
| PRPIF2 | $t_{w(PIF\_DATA\_INL)}$ | Pulse Duration, PIF_DATA_IN Low  | $2 + 0.475 \times (4 \times P)^{(1)}$ |     | ns   |

(1) P = 1x (or TX) clock period, defined by TX\_DIV\_FACTOR and TX\_DIV\_FACTOR\_FRAC in the CFG\_ED\_Pn\_TXCFG register.



**Figure 6-102. PRU\_ICSSG PRU Peripheral Interface Timing**

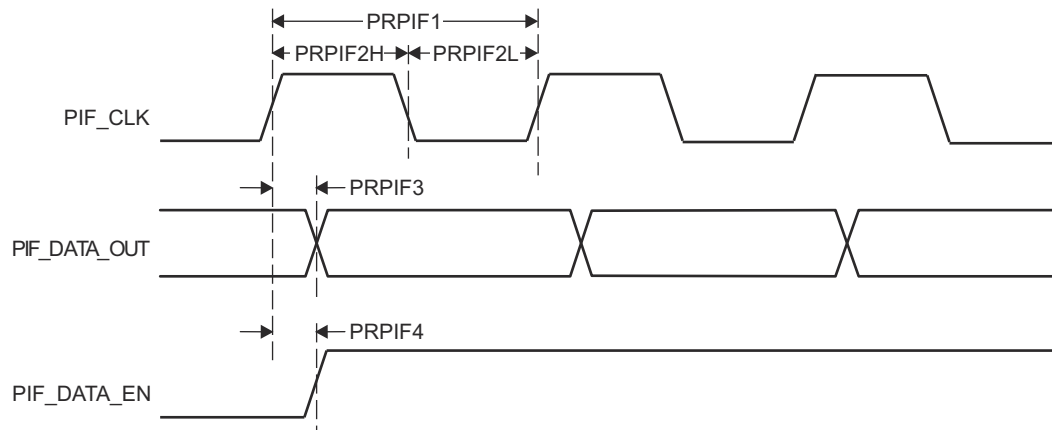
#### 6.9.5.21.1.4.3 PRU\_ICSSG PRU Switching Characteristics - Peripheral Interface Mode

| NO.     |                                  | DESCRIPTION                              | MIN                        | MAX | UNIT |
|---------|----------------------------------|------------------------------------------|----------------------------|-----|------|
| PRPIF1  | $t_{c(PIF\_CLK)}$                | Cycle time, PIF_CLK                      | 30                         |     | ns   |
| PRPIF2H | $t_{w(PIF\_DATA\_INH)}$          | Pulse Duration, PIF_CLK High             | $0 + 0.475 \times P^{(1)}$ |     | ns   |
| PRPIF2L | $t_{w(PIF\_DATA\_INL)}$          | Pulse Duration, PIF_CLK Low              | $0 + 0.475 \times P^{(1)}$ |     | ns   |
| PRPIF3  | $t_{d(PIF\_CLK-PIF\_DATA\_OUT)}$ | Delay time, PIF_CLK fall to PIF_DATA_OUT | -5                         | 5   | ns   |



| NO.    | DESCRIPTION                                                                  | MIN | MAX | UNIT |
|--------|------------------------------------------------------------------------------|-----|-----|------|
| PRPIF4 | $t_d(\text{PIF\_CLK-PIF\_DATA\_EN})$ Delay time, PIF_CLK fall to PIF_DATA_EN | -5  | 5   | ns   |

- (1)  $P = 1x$  (or TX) clock period, defined by TX\_DIV\_FACTOR and TX\_DIV\_FACTOR\_FRAC in the ICSSG\_PRUn\_ED\_TX\_CFG\_REG, where  $n = 0$  or 1.



SPRSP08\_TIMING\_PIF\_02

**Figure 6-103. PRU\_ICSSG PRU Peripheral Interface Switching Characteristics**

#### 6.9.5.21.2 PRU\_ICSSG Pulse Width Modulation (PWM)

##### 6.9.5.21.2.1 PRU\_ICSSG PWM Electrical Data and Timing

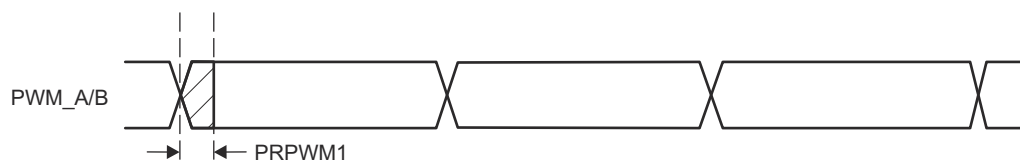
Table 6-72 presents the PRU\_ICSSG PWM timing conditions.

**Table 6-72. PRU\_ICSSG PWM Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| $SR_i$                   | Input slew rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| $C_L$                    | Output load capacitance | 2   | 7   | pF   |

##### 6.9.5.21.2.1.1 PRU\_ICSSG PWM Switching Characteristics

| NO.    | PARAMETER                 | DESCRIPTION  | MIN | MAX | UNIT |
|--------|---------------------------|--------------|-----|-----|------|
| PRPWM1 | $t_{sk}(\text{PWM\_A/B})$ | PWM_A/B skew |     | 5   | ns   |



SPRSP08\_TIMING\_PRU\_PWM\_01

**Figure 6-104. PRU\_ICSSG PRU PWM Timing**

#### 6.9.5.21.3 PRU\_ICSSG Industrial Ethernet Peripheral (PRU\_ICSSG IEP)

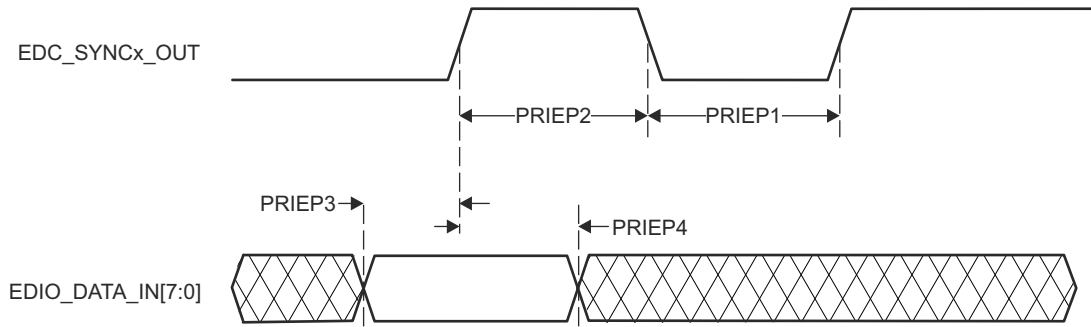
##### 6.9.5.21.3.1 PRU\_ICSSG IEP Electrical Data and Timing

##### 6.9.5.21.3.1.1 PRU\_ICSSG IEP Timing Requirements - Input Validated with SYNCx

| NO.    | PARAMETER                      | DESCRIPTION                        | MIN                    | MAX | UNIT |
|--------|--------------------------------|------------------------------------|------------------------|-----|------|
| PRIEP1 | $t_w(\text{EDC\_SYNCx\_OUTL})$ | Pulse Duration, EDC_SYNCx_OUT Low  | $-2+20 \times P^{(1)}$ |     | ns   |
| PRIEP2 | $t_w(\text{EDC\_SYNCx\_OUTH})$ | Pulse Duration, EDC_SYNCx_OUT High | $-2+20 \times P^{(1)}$ |     | ns   |

| NO.    |                                          |                                                                 | MIN | MAX | UNIT |
|--------|------------------------------------------|-----------------------------------------------------------------|-----|-----|------|
| PRIEP3 | $t_{su}(EDIO\_DATA\_IN-EDC\_SYNCx\_OUT)$ | Setup time, EDIO_DATA_IN valid before EDC_SYNCx_OUT active edge | 20  |     | ns   |
| PRIEP4 | $t_h(EDC\_SYNCx\_OUT-EDIO\_DATA\_IN)$    | Hold time, EDIO_DATA_IN valid after EDC_SYNCx_OUT active edge   | 20  |     | ns   |

(1) P = PRU-ICSS IEP clock source period.



SPRSP08\_TIMING\_PRU\_IEP\_01

**Figure 6-105. PRU\_ICSSG PRU IEP SYNCx Timing**

#### 6.9.5.21.3.1.2 PRU\_ICSSG IEP Timing Requirements - Digital IOs

| NO.    |                                       |                                            | MIN                    | MAX                   | UNIT |
|--------|---------------------------------------|--------------------------------------------|------------------------|-----------------------|------|
| IEPIO1 | $t_w(EDIO\_OUTVALIDL)$                | Pulse Duration, EDIO_OUTVALID Low          | $-2+14 \times P^{(1)}$ |                       | ns   |
| IEPIO2 | $t_w(EDIO\_OUTVALIDH)$                | Pulse Duration, EDIO_OUTVALID High         | $-2+32 \times P^{(1)}$ |                       | ns   |
| IEPIO3 | $t_d(EDIO\_OUTVALID-EDIO\_DATA\_OUT)$ | Delay time, EDIO_OUTVALID to EDIO_DATA_OUT | 0                      | $0+18 \times P^{(1)}$ | ns   |
| IEPIO4 | $t_{sk}(EDIO\_DATA\_OUT)$             | EDIO_DATA_OUT skew                         | 5                      |                       | ns   |

(1) P = PRU-ICSS IEP clock source period.



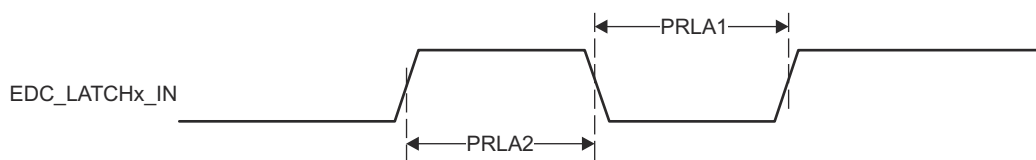
SPRSP08\_TIMING\_PRU\_EDIO\_DATA\_OUT

**Figure 6-106. PRU\_ICSSG PRU IEP Digital IOs Timing**

#### 6.9.5.21.3.1.3 PRU\_ICSSG IEP Timing Requirements - LATCHx\_IN

| NO.   |                         |                                    | MIN                  | MAX | UNIT |
|-------|-------------------------|------------------------------------|----------------------|-----|------|
| PRLA1 | $t_w(EDC\_LATCHx\_INL)$ | Pulse Duration, EDC_LATCHx_IN Low  | $2+3 \times P^{(1)}$ |     | ns   |
| PRLA2 | $t_w(EDC\_LATCHx\_INH)$ | Pulse Duration, EDC_LATCHx_IN High | $2+3 \times P^{(1)}$ |     | ns   |

(1) P = PRU-ICSS IEP clock source period.



SPRSP08\_TIMING\_PRU\_IEP\_02

**Figure 6-107. PRU\_ICSSG PRU IEP LATCHx\_IN Timing**

#### 6.9.5.21.4 PRU\_ICSSG Universal Asynchronous Receiver Transmitter (PRU-ICSS UART)

##### 6.9.5.21.4.1 PRU\_ICSSG UART Electrical Data and Timing

Table 6-73 presents the PRU\_ICSSG UART timing conditions.

**Table 6-73. PRU\_ICSSG UART Timing Conditions**

| PARAMETER                |                         | MIN  | MAX  | UNIT |
|--------------------------|-------------------------|------|------|------|
| <b>INPUT CONDITIONS</b>  |                         |      |      |      |
| SR <sub>I</sub>          | Input slew rate         | 0.01 | 0.33 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |      |      |      |
| C <sub>L</sub>           | Output load capacitance | 1    | 30   | pF   |

##### 6.9.5.21.4.1.1 PRU\_ICSSG UART Timing Requirements

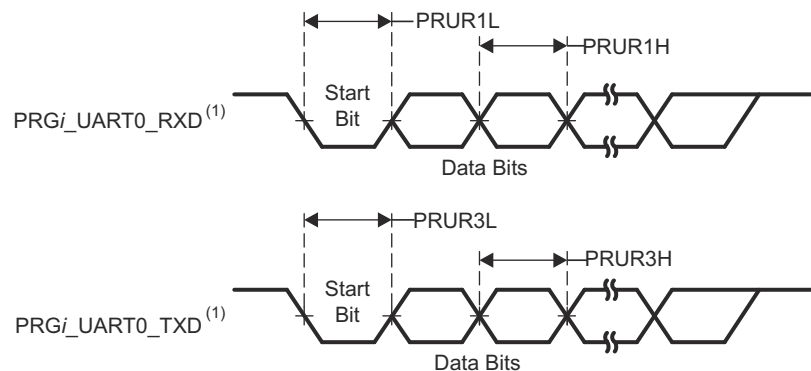
| NO.    | PARAMETER            | DESCRIPTION                                        | MIN                     | MAX | UNIT |
|--------|----------------------|----------------------------------------------------|-------------------------|-----|------|
| PRUR1H | t <sub>w</sub> (RXH) | Pulse Duration, Receive start, stop, data bit High | 2+0.95*U <sup>(1)</sup> |     | ns   |
| PRUR1L | t <sub>w</sub> (RXL) | Pulse Duration, Receive start, stop, data bit Low  | 2+0.95*U <sup>(1)</sup> |     | ns   |

(1) U = UART baud time = 1/programmed baud rate.

##### 6.9.5.21.4.1.2 PRU\_ICSSG UART Switching Characteristics

| NO.    | PARAMETER            | DESCRIPTION                                         | MIN                 | MAX | UNIT |
|--------|----------------------|-----------------------------------------------------|---------------------|-----|------|
|        | f(baud)              | Programmable baud rate                              |                     | 12  | MHz  |
| PRUR3L | t <sub>w</sub> (TXH) | Pulse Duration, Transmit start, stop, data bit High | -2+U <sup>(1)</sup> |     | ns   |
| PRUR3H | t <sub>w</sub> (TXL) | Pulse Duration, Transmit start, stop, data bit Low  | -2+U <sup>(1)</sup> |     | ns   |

(1) U = UART baud time = 1/programmed baud rate.



(1) i in PRGi\_UART0\_RXD and PRGi\_UART0\_TXD = 0, 1 or 2

SPRS91x\_TIMING\_PRU\_UART\_01

**Figure 6-108. PRU\_ICSSG UART Timing**

#### 6.9.5.21.5 PRU\_ICSSG Enhanced Capture Peripheral (PRU-ICSS ECAP)

##### 6.9.5.21.5.1 PRU\_ICSSG ECAP Electrical Data and Timing

Table 6-74 presents ECAP timing conditions.

**Table 6-74. PRU\_ICSSG ECAP Timing Conditions**

| PARAMETER                |                 | MIN | MAX | UNIT |
|--------------------------|-----------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                 |     |     |      |
| SR <sub>I</sub>          | Input slew rate | 1   | 3   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                 |     |     |      |

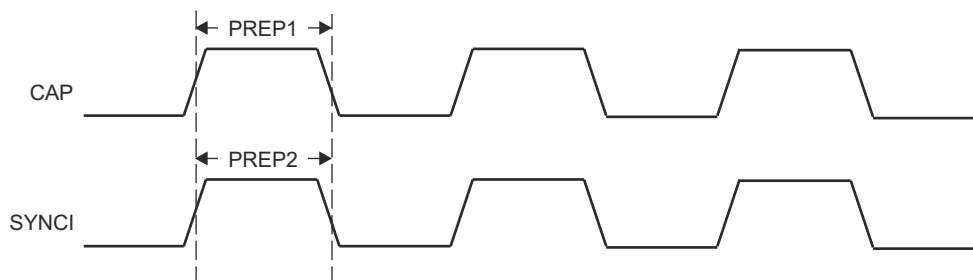
**Table 6-74. PRU\_ICSSG ECAP Timing Conditions (continued)**

| PARAMETER |                         | MIN | MAX | UNIT |
|-----------|-------------------------|-----|-----|------|
| $C_L$     | Output load capacitance | 2   | 7   | pF   |

#### 6.9.5.21.5.1.1 PRU\_ICSSG ECAP Timing Requirements

| NO.   | PARAMETER      | DESCRIPTION                                  | MIN                  | MAX | UNIT |
|-------|----------------|----------------------------------------------|----------------------|-----|------|
| PREP1 | $t_{w(CAP)}$   | Pulse Duration, Capture input (asynchronous) | $2+2 \times P^{(1)}$ |     | ns   |
| PREP2 | $t_{w(SYNCI)}$ | Pulse Duration, Sync input (asynchronous)    | $2+2 \times P^{(1)}$ |     | ns   |

(1) P = core\_clk period



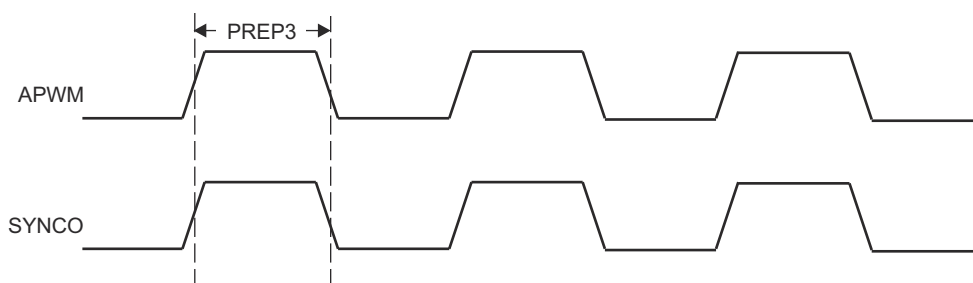
SPRSP08\_TIMING\_ECAPH\_01

**Figure 6-109. PRU\_ICSSG ECAP Timing**

#### 6.9.5.21.5.1.2 PRU\_ICSSG ECAP Switching Characteristics

| NO.   | PARAMETER      | DESCRIPTION                          | MIN                   | MAX | UNIT |
|-------|----------------|--------------------------------------|-----------------------|-----|------|
| PREP3 | $t_{w(APWM)}$  | Pulse Duration, APWM high/low        | $-2+2 \times P^{(1)}$ |     | ns   |
| PREP4 | $t_{w(SYNCO)}$ | Pulse Duration, SYNCO (asynchronous) | $-2+P^{(1)}$          |     | ns   |

(1) P = CORE\_CLK period in ns



SPRSP08\_TIMING\_ECAPH\_02

**Figure 6-110. PRU\_ICSSG ECAP Switching Characteristics**

### 6.9.5.21.6 PRU\_ICSSG RGMII, MII\_RT, and Switch

#### 6.9.5.21.6.1 PRU\_ICSSG MDIO Electrical Data and Timing

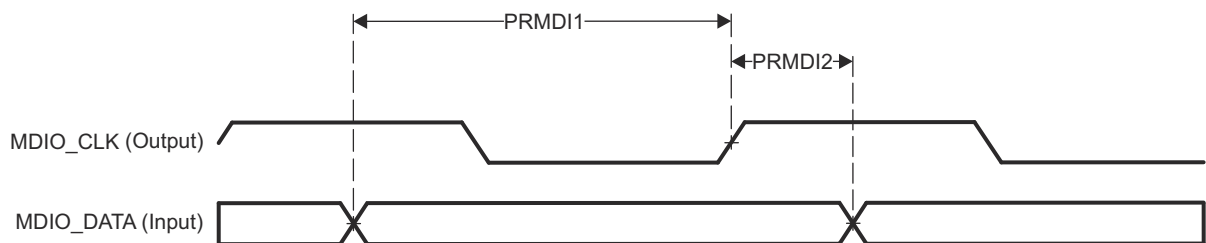
Table 6-75 presents MDIO timing conditions.

**Table 6-75. PRU\_ICSSG MDIO Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.9 | 3.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 10  | 470 | pF   |

#### 6.9.5.21.6.1.1 PRU\_ICSSG MDIO Timing Requirements

| NO.    | PARAMETER                  | DESCRIPTION                            | MIN | MAX | UNIT |
|--------|----------------------------|----------------------------------------|-----|-----|------|
| PRMDI1 | t <sub>su</sub> (MDIO-MDC) | Setup time, MDIO valid before MDC High | 90  |     | ns   |
| PRMDI2 | t <sub>h</sub> (MDC-MDIO)  | Hold time, MDIO valid after MDC High   | 0   |     | ns   |

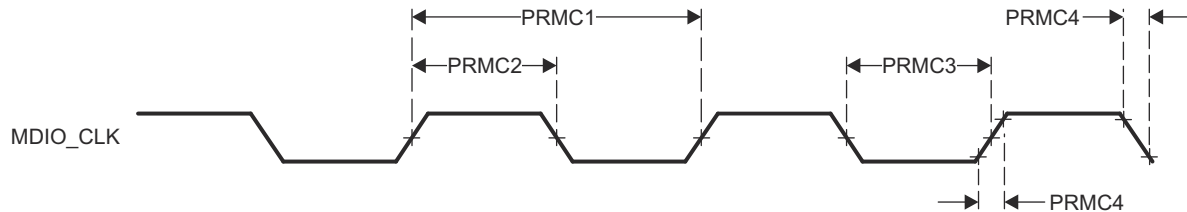


SPRS91x\_TIMING\_PRU\_MII\_RT\_01

**Figure 6-111. PRU\_ICSSG MDIO\_DATA Timing – Input Mode**

#### 6.9.5.21.6.1.2 PRU\_ICSSG MDIO Switching Characteristics - MDIO\_CLK

| NO.   | PARAMETER          | DESCRIPTION              | MIN | MAX | UNIT |
|-------|--------------------|--------------------------|-----|-----|------|
| PRMC1 | $t_c(\text{MDC})$  | Cycle time, MDC          | 400 |     | ns   |
| PRMC2 | $t_w(\text{MDCH})$ | Pulse Duration, MDC High | 160 |     | ns   |
| PRMC3 | $t_w(\text{MDCL})$ | Pulse Duration, MDC Low  | 160 |     | ns   |

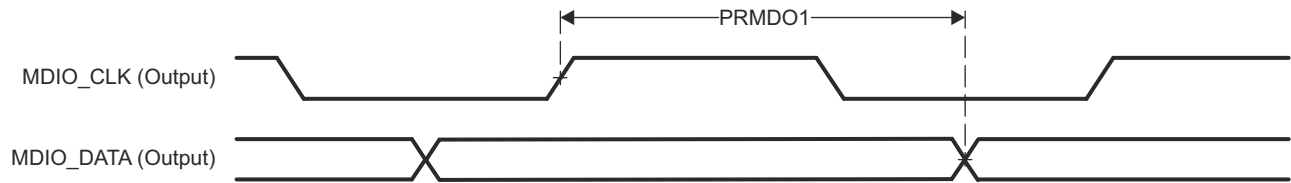


SPRS91x\_TIMING\_PRU\_MII\_RT\_02

**Figure 6-112. PRU\_ICSSG MDIO\_CLK Switching Characteristics**

#### 6.9.5.21.6.1.3 PRU\_ICSSG MDIO Switching Characteristics – MDIO\_DATA

| NO.    | PARAMETER              | DESCRIPTION                       | MIN  | MAX | UNIT |
|--------|------------------------|-----------------------------------|------|-----|------|
| PRMDO1 | $t_d(\text{MDC-MDIO})$ | Delay time, MDC low to MDIO valid | -150 | 150 | MHz  |



SPRS91x\_TIMING\_PRU\_MII\_RT\_03

**Figure 6-113. PRU\_ICSSG MDIO\_DATA Switching Characteristics**

#### 6.9.5.21.6.2 PRU\_ICSSG RGMII Electrical Data and Timing

Table 6-76 presents the PRU\_ICSSG RGMII timing conditions.

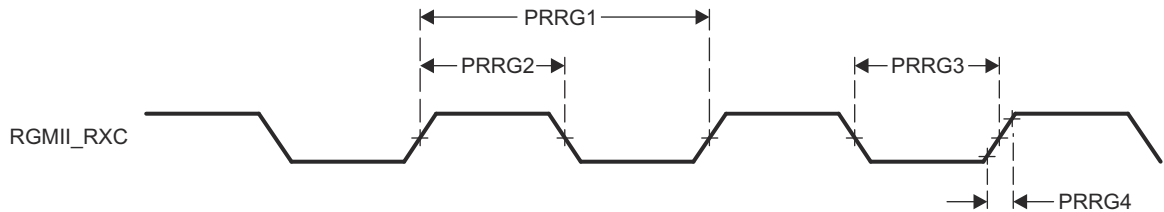
**Table 6-76. PRU\_ICSSG RGMII Timing Conditions**

| PARAMETER                            |                                              | MODE                | MIN  | MAX | UNIT |
|--------------------------------------|----------------------------------------------|---------------------|------|-----|------|
| <b>INPUT CONDITIONS</b>              |                                              |                     |      |     |      |
| $SR_i$                               | Input slew rate                              |                     | 2.65 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b>             |                                              |                     |      |     |      |
| $C_L$                                | Output load capacitance                      |                     | 2    | 20  | pF   |
| <b>PCB Connectivity Requirements</b> |                                              |                     |      |     |      |
| $t_d(\text{Trace Mismatch Delay})$   | Propagation delay mismatch across all traces | RXC, RD[3:0],RX_CTL |      | 50  | ps   |
|                                      |                                              | TXC, TD[3:0],TX_CTL |      | 50  | ps   |

#### 6.9.5.21.6.2.1 PRU\_ICSSG RGMII Timing Requirements - RGMII\_RXC

| NO.   |                   |                 | MODE      | MIN | MAX | UNIT |
|-------|-------------------|-----------------|-----------|-----|-----|------|
| PRRG1 | $t_c(\text{RXC})$ | Cycle time, RXC | 10 Mbps   | 360 | 440 | ns   |
|       |                   |                 | 100 Mbps  | 36  | 44  | ns   |
|       |                   |                 | 1000 Mbps | 7.2 | 8.8 | ns   |

| NO.   |               |                          | MODE      | MIN | MAX | UNIT |
|-------|---------------|--------------------------|-----------|-----|-----|------|
| PRRG2 | $t_{w(RXCH)}$ | Pulse duration, RXC high | 10 Mbps   | 160 | 240 | ns   |
|       |               |                          | 100 Mbps  | 16  | 24  | ns   |
|       |               |                          | 1000 Mbps | 3.6 | 4.4 | ns   |
| PRRG3 | $t_{w(RXCL)}$ | Pulse duration, RXC low  | 10 Mbps   | 160 | 240 | ns   |
|       |               |                          | 100 Mbps  | 16  | 24  | ns   |
|       |               |                          | 1000 Mbps | 3.6 | 4.4 | ns   |

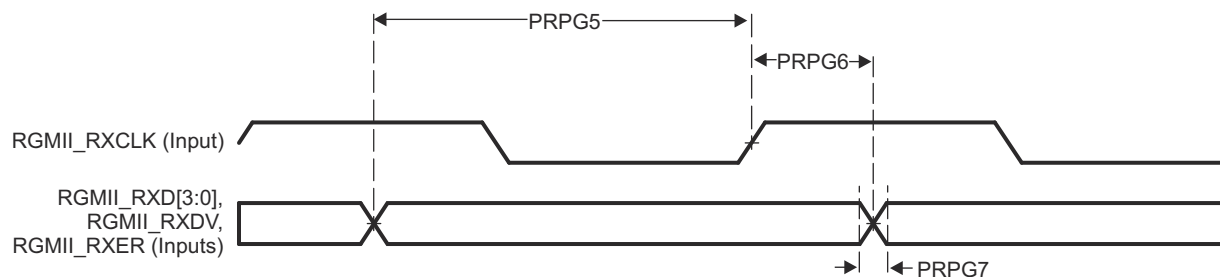


SPRS91x\_TIMING\_PRU\_RGMII\_RT\_04

Figure 6-114. PRU\_ICSSG RGMII\_RCLK Timing Requirements

## 6.9.5.21.6.2.2 PRU\_ICSSG RGMII Timing Requirements - RGMII\_RD[3:0] and RGMII\_RX\_CTL

| NO.   | PARAMETER             | DESCRIPTION                                   | MODE                             | MIN  | MAX | UNIT |
|-------|-----------------------|-----------------------------------------------|----------------------------------|------|-----|------|
| PRRG5 | $t_{su(RD-RXC)}$      | Setup time, RD[3:0] valid before RXC high/low | 10 Mbps<br>100 Mbps<br>1000 Mbps | 1    |     | ns   |
|       | $t_{su(RX\_CTL-RXC)}$ | Setup time, RX_CTL valid before RXC high/low  | 10 Mbps<br>100 Mbps<br>1000 Mbps | 1    |     | ns   |
| PRRG6 | $t_h(RXC-RD)$         | Hold time, RD[3:0] valid after RXC high/low   | 10 Mbps<br>100 Mbps<br>1000 Mbps | 1.15 |     | ns   |
|       | $t_h(RXC-RX\_CTL)$    | Hold time, RX_CTL valid after RXC high/low    | 10 Mbps<br>100 Mbps<br>1000 Mbps | 1.15 |     | ns   |



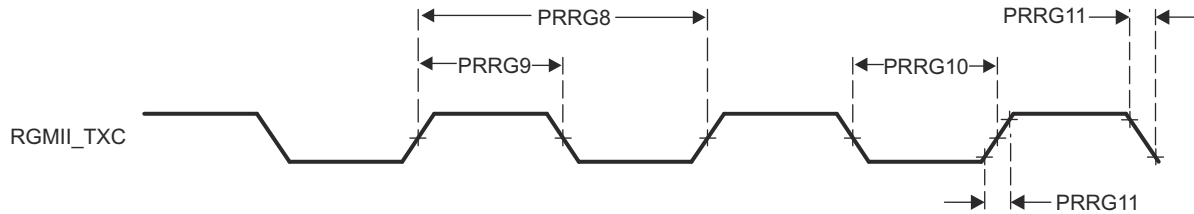
SPRS91x\_TIMING\_PRU\_RGMII\_RT\_05

Figure 6-115. PRU\_ICSSG RGMII\_RD[3:0] and RGMII\_RX\_CTL Timing Requirements

## 6.9.5.21.6.2.3 PRU\_ICSSG RGMII Switching Characteristics - RGMII\_TXC

| NO.   | PARAMETER   | DESCRIPTION              | MODE      | MIN | MAX | UNIT |
|-------|-------------|--------------------------|-----------|-----|-----|------|
| PRRG8 | $t_c(TXC)$  | Cycle time, TXC          | 10 Mbps   | 360 | 440 | ns   |
|       |             |                          | 100 Mbps  | 36  | 44  | ns   |
|       |             |                          | 1000 Mbps | 7.2 | 8.8 | ns   |
| PRRG9 | $t_w(TXCH)$ | Pulse duration, TXC high | 10 Mbps   | 160 | 240 | ns   |
|       |             |                          | 100 Mbps  | 16  | 24  | ns   |
|       |             |                          | 1000 Mbps | 3.6 | 4.4 | ns   |

| NO.    | PARAMETER     | DESCRIPTION             | MODE      | MIN | MAX | UNIT |
|--------|---------------|-------------------------|-----------|-----|-----|------|
| PRRG10 | $t_{w(TXCL)}$ | Pulse duration, TXC low | 10 Mbps   | 160 | 240 | ns   |
|        |               |                         | 100 Mbps  | 16  | 24  | ns   |
|        |               |                         | 1000 Mbps | 3.6 | 4.4 | ns   |



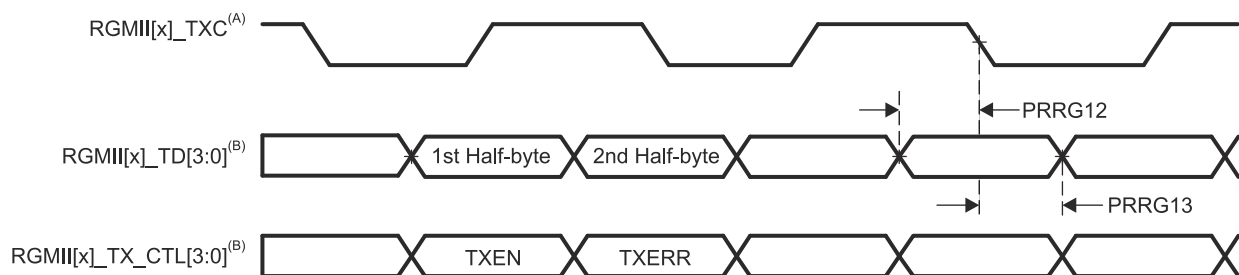
SPRS91X\_TIMING\_PRU\_RGMII\_RT\_06

**Figure 6-116. PRU\_ICSSG RGMII\_TXC Switching Characteristics**

#### 6.9.5.21.6.2.4 PRU\_ICSSG RGMII Switching Characteristics - RGMII\_TD[3:0] and RGMII\_TX\_CTL

| NO.    | PARAMETER             | DESCRIPTION                                                          | MODE                | MIN                 | TYP | MAX | UNIT |
|--------|-----------------------|----------------------------------------------------------------------|---------------------|---------------------|-----|-----|------|
| PRRG12 | $t_{osu(TD-TXC)}$     | Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low   | 10 Mbps<br>100 Mbps | 1.2                 |     |     | ns   |
|        |                       |                                                                      | 1000 Mbps           | 1.05 <sup>(1)</sup> |     |     | ns   |
|        | $t_{osu(TX_CTL-TXC)}$ | Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low    | 10 Mbps<br>100 Mbps | 1.2                 |     |     | ns   |
|        |                       |                                                                      | 1000 Mbps           | 1.05 <sup>(1)</sup> |     |     | ns   |
| PRRG13 | $t_{oh(TD-TXC)}$      | Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low | 10 Mbps<br>100 Mbps | 1.2                 |     |     | ns   |
|        |                       |                                                                      | 1000 Mbps           | 1.05 <sup>(1)</sup> |     |     | ns   |
|        | $t_{oh(TX_CTL-TXC)}$  | Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low  | 10 Mbps<br>100 Mbps | 1.2                 |     |     | ns   |
|        |                       |                                                                      | 1000 Mbps           | 1.05 <sup>(1)</sup> |     |     | ns   |

- (1) 1000Mbps operation requires that the 4 data pins (RGMII[x]\_TD[3:0]) and RGMII[x]\_TX\_CTL have their board propagation delays matched to within 50 ps of RGMII[x]\_TXC.



SPRS08\_TIMING\_PRU\_RGMII\_RT\_07

- A. TXC is delayed internally before being driven to the RGMII[x]\_TXC pin. This internal delay is always enabled.  
B. Data and control information is received using both edges of the clocks. RGMII\_TD[3:0] carries data bits 3-0 on the rising edge of RGMII\_TXC and data bits 7-4 on the falling edge of RGMII\_TXC. Similarly, RGMII\_TX\_CTL carries TXDV on rising edge of RGMII\_TXC and RTXERR on falling edge of RGMII\_TXC.

**Figure 6-117. PRU\_ICSSG Transmit Interface Timing RGMII Mode**



### 6.9.5.21.6.3 PRU\_ICSSG MII\_RT Electrical Data and Timing

#### Note

The PRU\_ICSSG are contains a second layer of multiplexing to enable additional functionality (including MII functionality) on the PRU GPO and GPI signals. This internal wrapper multiplexing is described in the *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU\_ICSSG)* section in *Peripherals* chapter in the device TRM.

#### Note

In order to ensure the MII\_G\_RT I/O timing values published in the device data sheet, the PRU\_ICSSG ICSSGn\_CORE\_CLK (where n = 0 to 2) core clock must be configured for 200 MHz, 225 MHz, or 250 MHz and the TX\_CLK\_DELAYn (where n = 0 or 1) bit field in the ICSSG\_TXCFG0/1 register must be set to 0h (default value).

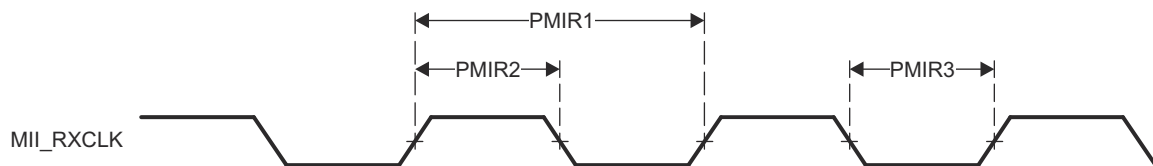
Table 6-77 presents PRU\_ICSSG MII timing conditions.

**Table 6-77. PRU\_ICSSG MII Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.9 | 3.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 20  | pF   |

#### 6.9.5.21.6.3.1 PRU\_ICSSG MII\_RT Timing Requirements – MII\_RX\_CLK

| NO.   | PARAMETER                | DESCRIPTION                 | MODE     | MIN    | MAX    | UNIT |
|-------|--------------------------|-----------------------------|----------|--------|--------|------|
| PMIR1 | t <sub>c</sub> (RX_CLK)  | Cycle time, RX_CLK          | 10 Mbps  | 399.96 | 400.04 | ns   |
|       |                          |                             | 100 Mbps | 39.996 | 40.004 | ns   |
| PMIR2 | t <sub>w</sub> (RX_CLKH) | Pulse Duration, RX_CLK High | 10 Mbps  | 140    | 260    | ns   |
|       |                          |                             | 100 Mbps | 14     | 26     | ns   |
| PMIR3 | t <sub>w</sub> (RX_CLKL) | Pulse Duration, RX_CLK Low  | 10 Mbps  | 140    | 260    | ns   |
|       |                          |                             | 100 Mbps | 14     | 26     | ns   |

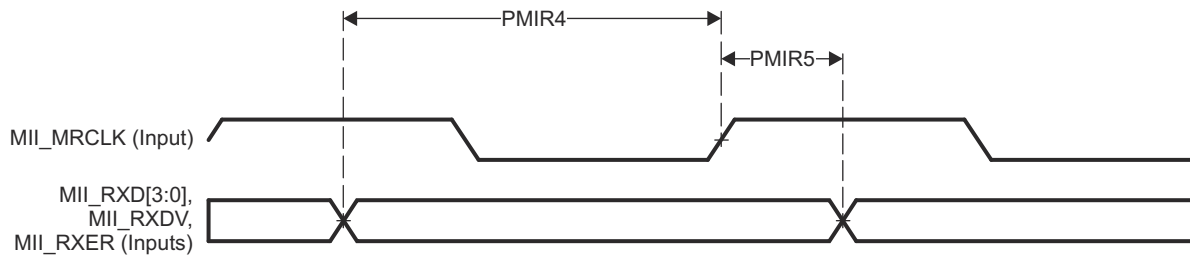


SPRS91x\_TIMING\_PRU\_MII\_RT\_04

**Figure 6-118. PRU\_ICSSG MII\_RXCLK Timing**

#### 6.9.5.21.6.3.2 PRU\_ICSSG MII\_RT Timing Requirements – MII\_RXD[3:0], MII\_RX\_DV, and MII\_RX\_ER

| NO.   | PARAMETER                | DESCRIPTION                              | MODE     | MIN | MAX | UNIT |
|-------|--------------------------|------------------------------------------|----------|-----|-----|------|
| PMIR4 | $t_{su}(RXD-RX\_CLK)$    | Setup time, RXD[3:0] valid before RX_CLK | 10 Mbps  | 8   |     | ns   |
|       | $t_{su}(RX\_DV-RX\_CLK)$ | Setup time, RX_DV valid before RX_CLK    |          | 8   |     | ns   |
|       | $t_{su}(RX\_ER-RX\_CLK)$ | Setup time, RX_ER valid before RX_CLK    |          | 8   |     | ns   |
|       | $t_{su}(RXD-RX\_CLK)$    | Setup time, RXD[3:0] valid before RX_CLK | 100 Mbps | 8   |     | ns   |
|       | $t_{su}(RX\_DV-RX\_CLK)$ | Setup time, RX_DV valid before RX_CLK    |          | 8   |     | ns   |
|       | $t_{su}(RX\_ER-RX\_CLK)$ | Setup time, RX_ER valid before RX_CLK    |          | 8   |     | ns   |
| PMIR5 | $t_h(RX\_CLK-RXD)$       | Hold time, RXD[3:0] valid after RX_CLK   | 10 Mbps  | 8   |     | ns   |
|       | $t_h(RX\_CLK-RX\_DV)$    | Hold time, RX_DV valid after RX_CLK      |          | 8   |     | ns   |
|       | $t_h(RX\_CLK-RX\_ER)$    | Hold time, RX_ER valid after RX_CLK      |          | 8   |     | ns   |
|       | $t_h(RX\_CLK-RXD)$       | Hold time, RXD[3:0] valid after RX_CLK   | 100 Mbps | 8   |     | ns   |
|       | $t_h(RX\_CLK-RX\_DV)$    | Hold time, RX_DV valid after RX_CLK      |          | 8   |     | ns   |
|       | $t_h(RX\_CLK-RX\_ER)$    | Hold time, RX_ER valid after RX_CLK      |          | 8   |     | ns   |

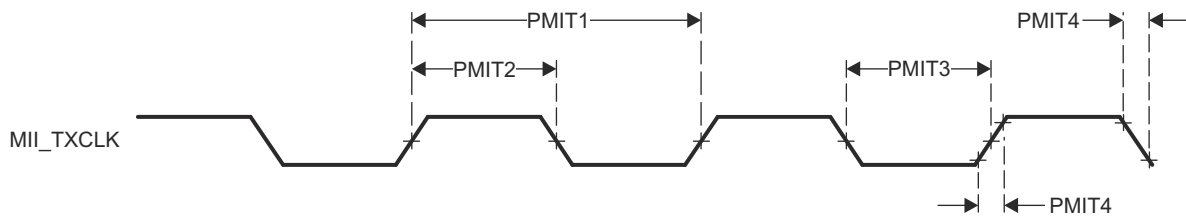


SPRS91x\_TIMING\_PRU\_MII\_RT\_06

**Figure 6-119. PRU\_ICSSG MII\_RXD[3:0], MII\_RXDV, and MII\_RXER Timing**

#### 6.9.5.21.6.3.3 PRU\_ICSSG MII\_RT Switching Characteristics – MII\_TX\_CLK

| NO.   | PARAMETER       | DESCRIPTION                 | MODE     | MIN    | MAX    | UNIT |
|-------|-----------------|-----------------------------|----------|--------|--------|------|
| PMIT1 | $t_c(TX\_CLK)$  | Cycle time, TX_CLK          | 10 Mbps  | 399.96 | 400.04 | ns   |
|       |                 |                             | 100 Mbps | 39.996 | 40.004 | ns   |
| PMIT2 | $t_w(TX\_CLKH)$ | Pulse Duration, TX_CLK High | 10 Mbps  | 140    | 260    | ns   |
|       |                 |                             | 100 Mbps | 14     | 26     | ns   |
| PMIT3 | $t_w(TX\_CLKL)$ | Pulse Duration, TX_CLK Low  | 10 Mbps  | 140    | 260    | ns   |
|       |                 |                             | 100 Mbps | 14     | 26     | ns   |

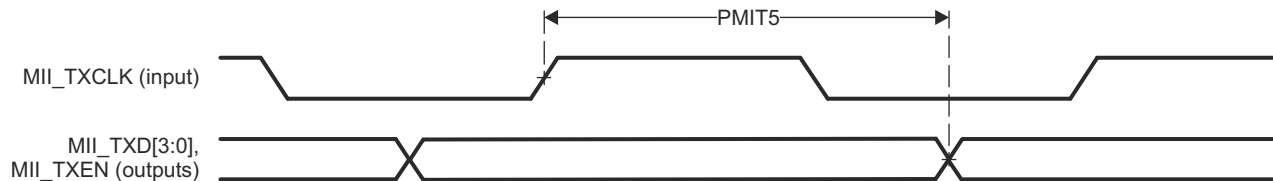


SPRS91x\_TIMING\_PRU\_MII\_RT\_05

**Figure 6-120. PRU\_ICSSG MII\_TX\_CLK Switching Characteristics**

#### 6.9.5.21.6.3.4 PRU\_ICSSG MII\_RT Switching Characteristics – MII\_TXD[3:0] and MII\_TXEN

| NO.   | PARAMETER                    | DESCRIPTION                               | MODE     | MIN | MAX | UNIT |
|-------|------------------------------|-------------------------------------------|----------|-----|-----|------|
| PMIT5 | $t_d(\text{TX\_CLK-TXD})$    | Delay time, TX_CLK High to TXD[3:0] valid | 10 Mbps  | 0   | 25  | ns   |
|       | $t_d(\text{TX\_CLK-TX\_EN})$ | Delay time, TX_CLK to TX_EN valid         |          | 0   | 25  | ns   |
|       | $t_d(\text{TX\_CLK-TXD})$    | Delay time, TX_CLK High to TXD[3:0] valid | 100 Mbps | 0   | 25  | ns   |
|       | $t_d(\text{TX\_CLK-TX\_EN})$ | Delay time, TX_CLK to TX_EN valid         |          | 0   | 25  | ns   |



SPRS91x\_TIMING\_PRU\_MII\_RT\_07

**Figure 6-121. PRU\_ICSSG MII\_TXD[3:0], MII\_TXEN Timing**

For more information, see section *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU\_ICSSG)* in the device TRM.

#### 6.9.5.22 Timers

For more details about features and additional description information on the device Timers, see the corresponding sections within [Section 5.3](#), *Signal Descriptions* and [Section 7](#), *Detailed Description*.

[Section 6.9.5.22.1](#), [Section 6.9.5.22.2](#) and [Figure 6-122](#) present timings and switching characteristics of the Timers.

##### 6.9.5.22.1 Timing Requirements for Timers

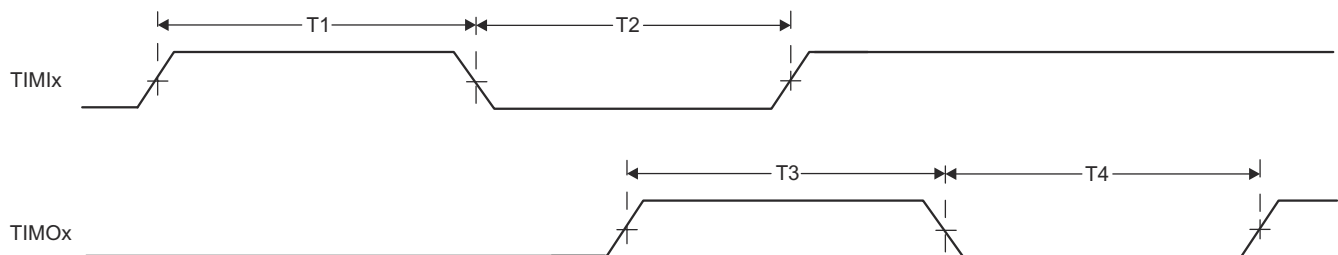
| NO. | PARAMETER           | DESCRIPTION          | MODE    | MIN            | MAX | UNIT |
|-----|---------------------|----------------------|---------|----------------|-----|------|
| T1  | $t_w(\text{TINPH})$ | Pulse duration, high | CAPTURE | $5 + 4P^{(1)}$ |     | ns   |
| T2  | $t_w(\text{TINPL})$ | Pulse duration, low  | CAPTURE | $5 + 4P^{(1)}$ |     | ns   |

(1) P = functional clock period in ns.

##### 6.9.5.22.2 Switching Characteristics for Timers

| NO. | PARAMETER            | DESCRIPTION          | MODE | MIN             | MAX | UNIT |
|-----|----------------------|----------------------|------|-----------------|-----|------|
| T3  | $t_w(\text{TOUTH})$  | Pulse duration, high | PWM  | $-3 + 4P^{(1)}$ |     | ns   |
| T4  | $t_w(\text{TOU TL})$ | Pulse duration, low  | PWM  | $-3 + 4P^{(1)}$ |     | ns   |

(1) P = functional clock period in ns.



TIMER\_01

**Figure 6-122. Timer Timing**

For more information, see section *Timers* in the device TRM.

### 6.9.5.23 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

[Section 6.9.5.23.1](#), [Section 6.9.5.23.2](#), and [Figure 6-123](#) present Timing Requirements and Switching Characteristics for UART interface.

#### 6.9.5.23.1 Timing Requirements for UART

| NO. | PARAMETER     | DESCRIPTION                                          | MIN           | MAX           | UNIT |
|-----|---------------|------------------------------------------------------|---------------|---------------|------|
| 4   | $t_{w(RX)}$   | Pulse width, receive data bit, 15/30 pF high or low  | $0.95U^{(1)}$ | $1.05U^{(1)}$ | ns   |
| 5   | $t_{w(CTS)}$  | Pulse width, receive start bit, 15/30 pF high or low | $0.95U^{(1)}$ | $1.05U^{(1)}$ | ns   |
|     | $t_d(RTS-TX)$ | Delay time, transmit start bit to transmit data      | $P^{(2)}$     |               | ns   |
|     | $t_d(CTS-TX)$ | Delay time, receive start bit to transmit data       | $P^{(2)}$     |               | ns   |

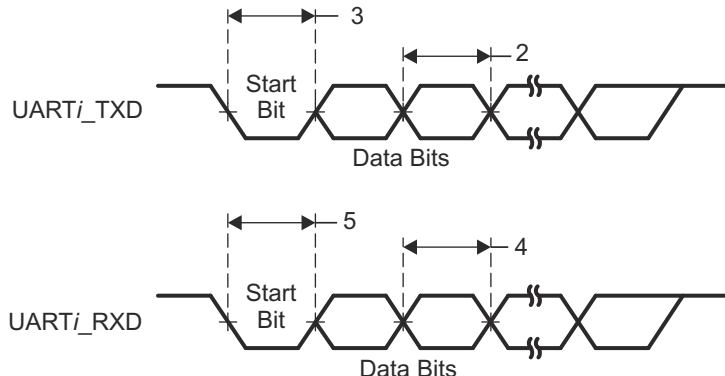
(1)  $U$  = UART baud time =  $1/\text{Programmed baud rate}$

(2)  $P$  = Clock period of the reference clock (FCLK, usually 48 MHz or 192 MHz)

#### 6.9.5.23.2 Switching Characteristics Over Recommended Operating Conditions for UART

| NO. | PARAMETER         | DESCRIPTION                                           | MODE  | MIN           | MAX           | UNIT |
|-----|-------------------|-------------------------------------------------------|-------|---------------|---------------|------|
|     | $f_{\text{baud}}$ | Maximum programmable baud rate                        | 15 pF |               | 12            | MHz  |
|     |                   |                                                       | 30 pF |               | 0.115         |      |
| 2   | $t_{w(TX)}$       | Pulse width, transmit data bit, 15/30 pF high or low  |       | $U - 2^{(1)}$ | $U + 2^{(1)}$ | ns   |
| 3   | $t_{w(RTS)}$      | Pulse width, transmit start bit, 15/30 pF high or low |       | $U - 2^{(1)}$ | $U + 2^{(1)}$ | ns   |

(1)  $U$  = UART baud time =  $1/\text{Programmed baud rate}$



**Figure 6-123. UART Timing**

For more information, see section *Universal Asynchronous Receiver/Transmitter (UART)* in the device TRM.

### 6.9.5.24 USB

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

The USB 3.1 GEN1 Dual-Role Device Subsystem is compliant with the Universal Serial Bus (USB) 3.1 Specification, revision 1.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

For more information, see the *Universal Serial Bus (USB) Subsystem* section in the device TRM.

### 6.9.5.25 Emulation and Debug

#### 6.9.5.25.1 Debug Trace

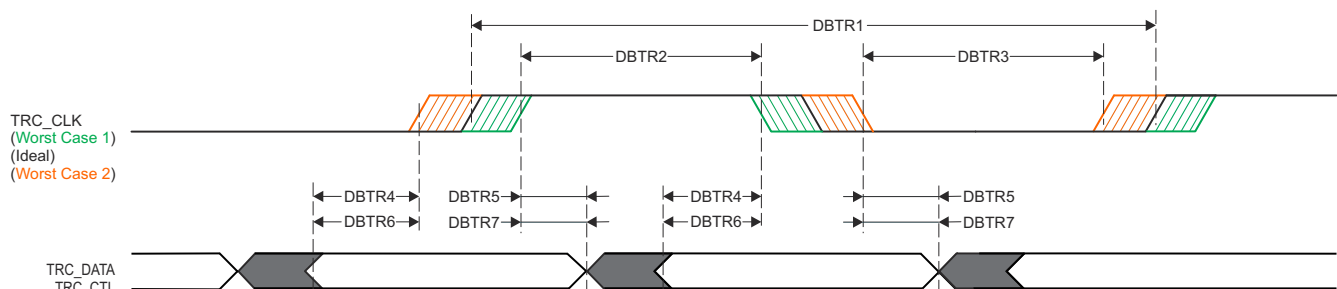
Table 6-79 and Figure 6-124 assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-78. Debug Trace Timing Conditions**

| PARAMETER                            |                                              | MIN | MAX | UNIT |
|--------------------------------------|----------------------------------------------|-----|-----|------|
| <b>OUTPUT CONDITIONS</b>             |                                              |     |     |      |
| $C_L$                                | Output load capacitance                      | 2   | 5   | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b> |                                              |     |     |      |
| $t_d(\text{Trace Mismatch})$         | Propagation delay mismatch across all traces |     | 200 | ps   |

**Table 6-79. Debug Trace Switching Characteristics**

| NO.   | PARAMETER                                          | DESCRIPTION                                        | MIN   | MAX | UNIT |
|-------|----------------------------------------------------|----------------------------------------------------|-------|-----|------|
| DBTR1 | $t_c(\text{TRC\_CLK})$                             | Cycle time, TRC_CLK                                | 10.16 |     | ns   |
| DBTR2 | $t_w(\text{TRC\_CLKH})$                            | Pulse width, TRC_CLK high                          | 4.33  |     | ns   |
| DBTR3 | $t_w(\text{TRC\_CLKL})$                            | Pulse width, TRC_CLK low                           | 4.33  |     | ns   |
| DBTR4 | $t_{\text{osu}}(\text{TRC\_DATA}-\text{TRC\_CLK})$ | Output setup time, TRC_DATA valid to TRC_CLK edge  | 1.27  |     | ns   |
| DBTR5 | $t_{\text{oh}}(\text{TRC\_CLK}-\text{TRC\_DATA})$  | Output hold time, TRC_CLK edge to TRC_DATA invalid | 1.27  |     | ns   |
| DBTR6 | $t_{\text{osu}}(\text{TRC\_CTLV}-\text{TRC\_CLK})$ | Output setup time, TRC_CTL valid to TRC_CLK edge   | 1.27  |     | ns   |
| DBTR7 | $t_{\text{oh}}(\text{TRC\_CLK}-\text{TRC\_CTL})$   | Output hold time, TRC_CLK edge to TRC_CTL invalid  | 1.27  |     | ns   |



SPRSP08\_Dbgug\_01

**Figure 6-124. Debug Trace Switching Characteristics**

#### 6.9.5.25.2 JTAG

For more details about features and additional description information on the device IEEE 1149.1 Standard-Test-Access Port, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

Table 6-80 presents the timing conditions for JTAG.

**Table 6-80. JTAG Timing Conditions**

| PARAMETER         |                         | SIGNAL   | MIN  | MAX  | UNIT |
|-------------------|-------------------------|----------|------|------|------|
| INPUT CONDITIONS  |                         |          |      |      |      |
| SR <sub>I</sub>   | Input slew rate         | TCK      | 0.5  | 2.00 | V/ns |
|                   |                         | TDI, TMS | 0.25 | 2.00 | V/ns |
| OUTPUT CONDITIONS |                         |          |      |      |      |
| C <sub>L</sub>    | Output load capacitance | TDO      | 5    | 15   | pF   |

#### 6.9.5.25.2.1 JTAG Electrical Data and Timing

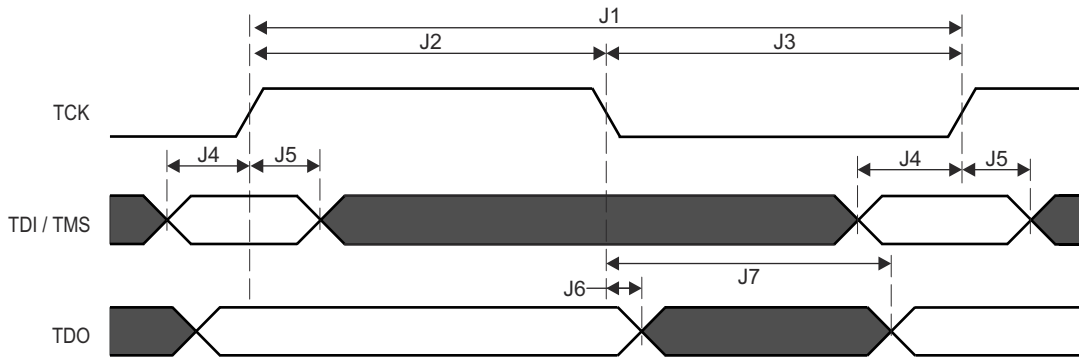
Section 6.9.5.25.2.1.1, Section 6.9.5.25.2.1.2, and Figure 6-125 assume testing over the recommended operating conditions and electrical characteristic conditions.

##### 6.9.5.25.2.1.1 JTAG Timing Requirements

| NO. | PARAMETER         | DESCRIPTION                                      | MIN | MAX | UNIT |
|-----|-------------------|--------------------------------------------------|-----|-----|------|
| J1  | $t_{c(TCK)}$      | Cycle time minimum, TCK                          | 60  |     | ns   |
| J2  | $t_{w(TCKH)}$     | Pulse width minimum, TCK high                    | 24  |     | ns   |
| J3  | $t_{w(TCKL)}$     | Pulse width minimum, TCK low                     | 24  |     | ns   |
| J4  | $t_{su(TDI-TCK)}$ | Input setup time minimum, TDI valid to TCK high  | 7   |     | ns   |
|     | $t_{su(TMS-TCK)}$ | Input setup time minimum, TMS valid to TCK high  | 7   |     | ns   |
| J5  | $t_{h(TCK-TDI)}$  | Input hold time minimum, TDI valid from TCK high | 4   |     | ns   |
|     | $t_{h(TCK-TMS)}$  | Input hold time minimum, TMS valid from TCK high | 4   |     | ns   |

##### 6.9.5.25.2.1.2 JTAG Switching Characteristics

| NO. | PARAMETER          | DESCRIPTION                                | MIN | MAX | UNIT |
|-----|--------------------|--------------------------------------------|-----|-----|------|
| J6  | $t_{d(TCKL-TDOl)}$ | Delay time minimum, TCK low to TDO invalid | 0   |     | ns   |
| J7  | $t_{d(TCKL-TDOv)}$ | Delay time maximum, TCK low to TDO valid   |     | 24  | ns   |



**Figure 6-125. JTAG Test-Port Timing**

## 7 Detailed Description

### 7.1 Overview

AM654x and AM652x Sitara™ processors are Arm applications processors built to meet the complex processing needs of modern industry 4.0 embedded products.

The AM654x and AM652x devices combine four or two Arm Cortex-A53 cores with a dual Cortex-R5F MCU subsystem which includes features intended to help customers achieve their functional safety goals for their end products and three Gigabit industrial communications subsystems (PRU\_ICSSG) to create a SoC capable of high-performance industrial controls with industrial connectivity and processing for functional safety applications. AM65xx is currently undergoing assessment to be certified by TÜV SÜD according to IEC 61508.

The four A53 cores are arranged in two dual-core clusters with shared L2 memory to create two processing channels. Extensive ECC is included on on-chip memory, peripherals, and interconnect for reliability. The SoC as a whole includes features intended to help customers design systems that can achieve their functional safety goals (assessment pending with TÜV SÜD). Cryptographic acceleration and secure boot are available on AM654x and AM652x devices in addition to granular firewalls managed by the DMSC.

Programmability is provided by the quad-core Arm Cortex-A53 RISC CPUs with Neon extension, and the dual Cortex-R5F MCU subsystem is available for general purpose use as two cores or it can be used in lockstep to help meet the needs of functional safety applications. The PRU\_ICSSG subsystems can be used to provide up to six ports of industrial Ethernet such as Profinet IRT, TSN, or EtherCAT® (among many others), or they can be used for standard Gigabit Ethernet connectivity.

TI provides a complete set of software and development tools for the Arm cores including Processor SDK Linux, Linux-RT, RTOS, and Android as well as C compilers and a debugging interface for visibility into source code execution. Applicable safety documentation will be made available to assist customers in developing their functional safety related systems.

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#### Note

For more information on features, subsystems, and architecture of superset device System on Chip (SoC), see the device TRM.

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## 7.2 Processor Subsystems

### 7.2.1 Arm Cortex-A53

The SoC implements two Dual-Core Arm Cortex-A53 Subsystems (CC\_ARMSS0 and CC\_ARMSS1), which are both integrated inside the Compute Cluster (along with the MSMC module). The Cortex-A53 cores are general-purpose processors that can be used for running customer applications.

The CC\_ARMSS is built around the Cortex-A53 MPCore (Arm A53 Cluster), which is provided by Arm and configured by TI. It is based on the symmetric multiprocessor (SMP) architecture, and thus it delivers high performance and optimal power management, debug and emulation capabilities.

The A53 processor is a multi-issue out-of-order superscalar execution engine with integrated L1 Instruction and Data Caches, compatible with Arm®v8-A architecture. It delivers significantly more performance than its predecessors at a higher level of power efficiency.

For more information, see *Compute Cluster Arm Cortex-A53 Subsystem* section in the device TRM.

### 7.2.2 Arm Cortex-R5F

The MCU\_ARMSS is a dual-core implementation of the Arm Cortex-R5F processor configured for split/lock operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight® debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various other modules for protocol conversion and address translation for easy integration into the SoC.

For more information, see *MCU Arm Cortex-R5F Subsystem* section in the device TRM.



## 7.3 Accelerators and Coprocessors

### 7.3.1 PRU\_ICSSG

The Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU\_ICSSG) consists of:

- Two 32-bit load/store RISC CPU cores — Programmable Real-Time Units (PRU0 and PRU1)
- Two auxiliary 32-bit load/store RISC CPU cores — Auxiliary Programmable Real-Time Units (RTU\_PRU0 and RTU\_PRU1)
- Data RAMs per PRU core
- Instruction RAMs per PRU and per RTU\_PRU cores
- Shared RAM
- Peripheral modules: UART0, ECAP0, PWM, IEP0 and IEP1
- Interrupt controller (INTC)

The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

The PRU cores are programmed with a small, deterministic instruction set. Each PRU can operate independently or in coordination with each other and can also work in coordination with the device-level host CPU. This interaction between processors is determined by the nature of the firmware loaded into the PRU's instruction memory.

#### 7.3.1.1 PRU\_ICSSG PRU and RTU\_PRU Cores

The PRU is a processor optimized for performing embedded tasks that require manipulation of packed memory mapped data structures, handling of system events that have tight real-time constraints and interfacing with systems external to the SoC. The PRU is both very small and very efficient at handling such tasks.

#### 7.3.1.2 PRU\_ICSSG Broadside Accelerators Overview

The PRU\_ICSSG supports a broadside interface, which uses the XFR (XIN, XOUT, or XCHG) instruction to transfer the contents of PRUn or RTU\_PRUn (where n = 0 or 1) registers to or from accelerators with the PRU\_ICSSG. This interface enables up to 31 registers (R0-R30, or 124 bytes) to be transferred in a single instruction. The PRU\_ICSSG broadside accelerators are divided into two categories – data processing accelerators and data movement accelerators.

#### 7.3.1.3 PRU\_ICSSG UART Module

The PRU\_ICSSG UART0 peripheral is based on the industry standard TL16C550 asynchronous communications element, which in turn is a functional upgrade of the TL16C450.

The PRU\_ICSSG UART0 performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. The CPU can read the PRU\_ICSSG UART0 status at any time. The PRU\_ICSSG UART0 includes control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

#### 7.3.1.4 PRU\_ICSSG ECAP Module

A single instance of an Enhanced Capture event module (ECAP0) is integrated in each device PRU\_ICSSG0, PRU\_ICSSG1 and PRU\_ICSSG2 subsystem.

This module provides accurate timing of events. When not being used for event capture, its resources can be used to generate a single channel of asymmetrical PWM waveforms (configurable as either one capture input, or as one auxiliary PWM output).

#### 7.3.1.5 PRU\_ICSSG PWM Module

Each of the PRU\_ICSSG modules integrates one Pulse Width Modulation module (PWM). The PWM module uses the PRU\_ICSSG IEP0 and IEP1 compare events to produce the PWM outputs.

### **7.3.1.6 PRU\_ICSSG MII\_G\_RT Module**

The Real-time Media Independent Interface (MII\_G\_RT) provides a programmable I/O interface for the PRUs to access and control up to two MII ports. The MII\_G\_RT module can also be configured to push and pull data independent of the PRU cores.

### **7.3.1.7 PRU\_ICSSG MII MDIO Module**

The PRU\_ICSSG MII MDIO management I/F module implements the 802.3 serial management interface to interrogate and control two Ethernet PHYs simultaneously using a shared two-wire bus.

### **7.3.1.8 PRU\_ICSSG IEP**

The Industrial Ethernet Peripheral (IEP) performs hardware work required for Industrial Ethernet functions. The IEP module features an industrial ethernet timer with 16 compare events, industrial ethernet sync generator and latch capture, industrial ethernet watchdog timer, and a digital I/O port (DIGIO).

For more information, see *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU\_ICSSG)* section in the device TRM.

## **7.3.2 GPU**

The Graphics Processing Unit (GPU) accelerates 2-dimensional (2D) and 3-dimensional (3D) graphics and compute applications.

The GPU module is a scalable architecture which efficiently processes a number of differing multimedia data types concurrently:

- Pixel Data
- Vertex Data
- General Purpose Processing

For more information, see *Graphics Accelerator (GPU)* section in the device TRM.

## 7.4 Other Subsystems

### 7.4.1 DMSC

Integrated in WKUP domain Device Management and Security Controller (WKUP\_DMSC) provides control over the device boot sequencing, device management, power management, and security. With the factory-sealed firmware, DMSC main functions include:

- Device management
- On-chip power management and wake-up control
- Device boot configuration and sequence
- Secure boot setup
- Authentication routines (all modes), including R5F island only boot modes
- Decryption routines
- Firewall control for isolation and Security
- Runtime Security Management and resource allocation
- Arm Cortex-M3 based DMSC acts as system security master and protects critical security assets during run-time. As part of booting on High Security (HS) device, DMSC uses on-chip keys to establish root-of-trust and authenticate images to reinforce trust. DMSC controls the power management of device, hence is responsible to bring device cleanly out of reset and enforce clock and reset rules. DMSC power management functions are critical to bring device to low power modes and sense wakeup events to bring device back to active state. DMSC acts also as main boot processor and as such is the very first subsystem that is brought out of reset after device power-on-reset.

For more information, see *WKUP Device Management and Security Controller (DMSC)* section in the device TRM.

### 7.4.2 MSMC

The Multicore Shared Memory Controller (MSMC) forms the heart of the compute cluster (COMPUTE\_CLUSTER0) providing high-bandwidth resource access both to and from all of the connected processing elements and the rest of the system. MSMC serves as the data-movement backbone of the compute cluster.

For more information, see *Multicore Shared Memory Controller (MSMC)* section in the device TRM.

### 7.4.3 NAVSS

#### 7.4.3.1 NAVSS0

Main SoC Navigator Subsystem (NAVSS0) consists of DMA/Queue Management components – UDMA and Ring Accelerator (UDMASS), Peripherals (Module subsystem [MODSS]), and a North Bridge (NBSS).

**UDMASS** – UDMASS is the essential part of the DMA Architecture. UDMASS consists of:

- Unified DMA Controller
- Ring Accelerator
- Packet Streaming Interface (PSI-L)

**MODSS** – MODSS is a collection of peripherals with different system-level functions, for example, interprocessor communication and time sync, among others. NAVSS0 contains the following modules:

- Mailbox
- Spinlock
- Two Timer Managers (Timer banks)
- Time Stamp Module (CPTS)
- Memory CRC module
- Infrastructure components such as:
  - CBASS
  - Proxies
  - Interrupt aggregators
  - Interrupt router

**NBSS** – This is a north bridge infrastructure

#### 7.4.3.2 MCU\_NAVSS0

MCU Navigator Subsystem (MCU NAVSS) has a subset of the modules of the main NAVSS and is instantiated in the MCU domain.

MCU Navigator Subsystem consists of DMA/Queue Management components – UDMA and Ring Accelerator (UDMASS), and Peripherals (Module subsystem [MODSS]).

**UDMASS** – UDMASS is the essential part of the DMA Architecture. UDMASS consists of:

- Unified DMA Controller
- Ring Accelerator
- Packet Streaming Interface (PSILSS)

**MODSS** – MODSS is a collection of peripherals with different system-level functions. NAVSS0 contains the following modules:

- Memory CRC module
- Infrastructure components such as CBASS, proxies, interrupt aggregators, and an interrupt router

**ECC aggregators** – for SEC/DED memory protection.

For more information, see *Navigator Subsystem (NAVSS)* section in the device TRM.

#### 7.4.4 PDMA Controller

The Peripheral DMA is a simple DMA which has been architected to specifically meet the data transfer needs of peripherals, which perform data transfers using memory mapped registers (MMRs) accessed via a standard non-coherent bus fabric. The PDMA module is located close to one or more peripherals which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only statically configured Transfer Request (TR) operations.

The PDMA is only responsible for performing the data movement transactions which interact with the peripherals themselves. Data which is read from a given peripheral is packed by a PDMA source channel into a PSI-L data stream which is then sent to a remote peer UDMA-P destination channel which then performs the movement of the data into memory. Likewise, a remote UDMA-P source channel fetches data from memory and transfers it to a peer PDMA destination channel over PSI-L which then performs the writes to the peripheral.

For more information, see PDMA Controller section in the device TRM.

## 7.4.5 Peripherals

### 7.4.5.1 ADC

The Analog-to-Digital Converter (ADC) module contains a single 12-bit ADC which can be multiplexed to any 1 of 8 analog inputs (channels).

For more information, see *Analog-to-Digital Converter (ADC)* section in the device TRM.

### 7.4.5.2 CAL

The Camera Adapter Layer Subsystem (CALSS) is based on a Camera Adaptation Layer (CAL) module, which enables connection to multiple camera sensors through shared MIPI D-PHY module and LVDS receiver.

CAL Module (CALSS0) is a very flexible subsystem that enables connection to multiple cameras supporting MIPI CSI-2 over D-PHY serial interface, a LVDS serial interface, and a traditional parallel interface. It also includes an internal write DMA engine connected to VBUSM interface.

For more information, see *Camera Adapter Layer (CAL) Subsystem* section in the device TRM.

### 7.4.5.3 CPSW2G

The two-port Gigabit Ethernet MAC (MCU\_CPSW0) subsystem provides Ethernet packet communication for the device and is configured in a similar manner as a two-port Ethernet switch. MCU\_CPSW0 features the Reduced Gigabit Media Independent Interface (RGMII), Reduced Media Independent Interface (RMII), and the Management Data Input/Output (MDIO) interface for physical layer device (PHY) management.

For more information, see *Gigabit Ethernet MAC (MCU\_CPSW0)* section in the device TRM.

### 7.4.5.4 DCC

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programmed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference.

For more information, see *Dual Clock Comparator (DCC)* section in the device TRM.

### 7.4.5.5 DDRSS

The DDR subsystem in this device comprises DDR controller, DDR PHY and wrapper logic to integrate these blocks in the device. The DDR subsystem is referred to as DDRSS0 and is used to provide an interface to external SDRAM devices which can be utilized for storing program or data. DDRSS0 is accessed via MSMC, and not directly through the system interconnect.

For more information, see *DDR Subsystem (DDRSS)* section in the device TRM.

### 7.4.5.6 DSS

The Display Subsystem (DSS) is a flexible, multi-pipeline subsystem that supports high-resolution display outputs. DSS includes input pipelines providing multi-layer blending with transparency to enable on-the-fly composition. Various pixel processing capabilities are supported, such as color space conversion and scaling, among others. DSS includes a DMA engine, which allows direct access to the frame buffer (device system memory). Display outputs can connect seamlessly to an Open LVDS Display Interface transmitter (OLDITX), or can directly drive device pads as a parallel video output interface.

For more information, see *Display Subsystem (DSS)* section in the device TRM.

### 7.4.5.7 ECAP

Integrated in the MAIN domain one Enhanced Capture (ECAP) module provides accurate timing of events. When not being used for event capture, its resources can be used to generate a single channel of asymmetrical PWM waveforms (configurable as either one capture input, or as one auxiliary PWM output).

ECAP module can be used for:

- Sample rate measurements of audio inputs

- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors.

For more information, see *Enhanced Capture (ECAP) Module* section in the device TRM.

#### **7.4.5.8 EPWM**

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The EPWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the EPWM is built up from smaller single channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in the device TRM.

#### **7.4.5.9 ELM**

The ELM is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. A host processor can then correct the data block by flipping the bits to which the ELM error-location outputs point.

When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller. ELM can be also used to support parallel NOR flash or NAND flash.

The General-Purpose Memory Controller (GPMC) probes data read from an external NAND flash and uses this to compute checksum-like information, called syndrome polynomials, on a per-block basis. Each syndrome polynomial gives a status of the read operations for a full block, including 512 bytes of data, parity bits, and an optional spare-area data field, with a maximum block size of 1023 bytes. Computation is based on a Bose-Chaudhuri-Hocquenghem (BCH) algorithm. The ELM extracts error addresses from these syndrome polynomials.

Based on the syndrome polynomial value, the ELM can detect errors, compute the number of errors, and give the location of each error bit. The actual data is not required to complete the error-correction algorithm. Errors can be reported anywhere in the NAND flash block, including in the parity bits.

For more information, see *Error Location Module (ELM)* section in the device TRM.

#### **7.4.5.10 ESM**

The Error Signaling Module (ESM) aggregates safety-related events and errors from throughout the device into one location. It can signal both low and high priority interrupts to a processor to deal with a safety event and/or manipulate an I/O error pin to signal an external hardware that an error has occurred. Therefore an external controller is able to reset the device or keep the system in a safe, known state.

For more information, see *Error Signaling Module (ESM)* section in the device TRM.

#### **7.4.5.11 EQEP**

The Enhanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system.

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in the device TRM.

#### **7.4.5.12 GPIO**

The General-Purpose Input/Output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, the user can write to an internal register to

control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce host CPU interrupts and DMA synchronization events in different interrupt/event generation modes.

The device has three instances of GPIO modules. The GPIO pins are grouped into banks (16 pins per bank and 9 banks per module), which means that each GPIO module provides up to 144 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 432 (3 instances × (9 banks × 16 pins)) pins. Since WKUP\_GPIO0\_[56:143], GPIO0\_[96:143], and GPIO1\_[90:143] are reserved in this device, general purpose interface supports up to 242 pins.

For more information, see *General-Purpose Interface (GPIO)* section in the device TRM.

#### 7.4.5.13 GPMC

The General-Purpose Memory Controller is a unified memory controller dedicated for interfacing with external memory devices like:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in non-multiplexed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

For more information, see *General-Purpose Memory Controller (GPMC)* section in the device TRM.

#### 7.4.5.14 HyperBus

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##### Note

HyperBus is not available on this device.

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The HyperBus module is a part of the device Flash Subsystem (FSS).

The HyperBus module is a low pin count memory interface that provides high read/write performance. The HyperBus module connects to HyperBus memory (HyperFlash or HyperRAM) and uses simple HyperBus protocol for read and write transactions.

There is one HyperBus™ module inside the device. The HyperBus module includes one HyperBus Memory Controller (HBMC).

For more information, see *HyperBus Interface* section in the device TRM.

#### 7.4.5.15 I2C

The device contains six multimaster Inter-Integrated Circuit (I2C) controllers each of which provides an interface between a local host (LH), such as an Arm and any I<sup>2</sup>C-bus-compatible device that connects via the I<sup>2</sup>C serial bus. External components attached to the I<sup>2</sup>C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I<sup>2</sup>C interface.

Each multimaster I2C module can be configured to act like a slave or master I<sup>2</sup>C-compatible device.

The WKUP\_I2C0 and MCU\_I2C0 controllers have dedicated I<sup>2</sup>C compliant open drain buffers, and support fast mode (up to 400 Kbps). The I2C0, I2C1, I2C2, and I2C3 controllers are multiplexed with standard LVCMOS I/O and connected to emulate open drain. The I<sup>2</sup>C emulation is achieved by configuring the LVCMOS buffers to output Hi-Z instead of driving high when transmitting logic 1.

For more information, see *Inter-Integrated Circuit (I2C) Interface* section in the device TRM.

#### 7.4.5.16 MCAN

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control. CAN has high immunity to electrical interference. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.



The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The device supports two MCAN modules - MCU\_MCAN0 and MCU\_MCAN1. They connect to the physical layer of the CAN network through external (for the device) transceivers. Each MCAN module supports flexible bit rates greater than 1 Mbps and is compliant to ISO 11898-1:2015.

For more information, see *Modular Controller Area Network (MCAN)* section in the device TRM.

#### **7.4.5.17 MCASP**

The MCASP functions as a general-purpose audio serial port are optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an intercomponent digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

Although intercomponent digital audio interface reception (DIR) mode (this is, S/PDIF stream receiving) is not natively supported by the MCASP module, a specific TDM mode implementation for the MCASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

For more information, see *Multichannel Audio Serial Port (MCASP)* section in the device TRM.

#### **7.4.5.18 MCRC**

VBUSM CRC controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of a memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a predetermined good signature value. MCRC controller provides four channels to perform CRC calculation on multiple memories in parallel and can be used on any memory system. Channel 1 can also be put into data trace mode, where MCRC controller compresses each data being read through CPU read data bus.

For more information, see *Memory Cyclic Redundancy Check (MCRC) Controller* section in the device TRM.

#### **7.4.5.19 MCSPI**

The MCSPI module is a multichannel transmit/receive, master/slave synchronous serial bus.

There are total of eight MCSPI modules in the device.

MCSPi3 and MCSPi4 include internal connectivity to MCSPI modules in the MCU domain, as follows:

- MCSPi3 is connected as a master to MCU\_MCSPi1 by default at power-up. MCU\_MCSPi1 and MCSPi3 may be optionally mapped to external device pads.
- MCSPi4 is directly connected as a slave to MCU\_MCSPi2 by default at power-up. MCSPi4 and MCU\_MCSPi2 are not pinned out externally.

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in the device TRM.

#### **7.4.5.20 MMCSD**

There are two MMCSD modules inside the device - MMCSD0 and MMCSD1. Each MMCSD module includes one MMCSD Host Controller.

Each controller has the following data bus width:

- MMCSD0 - 8-bit wide data bus
- MMCSD1 - 4-bit wide data bus

The MMCSD Host Controller provides an interface to eMMC 5.1 (embedded MultiMedia Card), SD 4.10 (Secure Digital), and SDIO 4.0 (Secure Digital IO) devices. The MMCSD Host Controller deals with MMCSD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.



For more information, see *Multimedia Card/Secure Digital (MMCSD) Interface* section in the device TRM.

#### 7.4.5.21 OSPI

The Octal Serial Peripheral Interface (OSPI™) module is a kind of Serial Peripheral Interface (SPI) module which allows single, dual, quad or octal read and write access to external flash devices.

The OSPI module is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signaling its completion via interrupts or status registers. For indirect operations, data is transferred between system memory and external flash memory via an internal SRAM which is loaded for writes and unloaded for reads by a device master at low latency system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM should be accessed using user programmable configuration registers.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in the device TRM.

#### 7.4.5.22 PCIE

The Peripheral Component Interconnect Express (PCIe) subsystem is built around a multi-lane dual-mode PCIe controller that provides low pin-count, high reliability, and high-speed data transfers at rates of up to 5.0 Gbps per lane for serial links on backplanes and printed wiring boards.

The device includes two instantiations of PCIe subsystem named PCIE0 and PCIE1.

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in the device TRM.

#### 7.4.5.23 SerDes

The goal of the SerDes is to convert device (SoC) parallel data into serialized data that can be output over a high-speed electrical interface. In the opposite direction, SerDes converts high-speed serial data into parallel data that can be processed by the device. To this end, the SerDes contains a variety of functional blocks to handle both the external analog interface as well as the internal digital logic.

For more information, see *Serializer/Deserializer (SerDes)* section in the device TRM.

#### 7.4.5.24 RTI

This section describes the Real Time Interrupt (RTI) modules with Windowed Watchdog Timer (WWDT) functionality for the device.

The Real Time Interrupt module provides timer functionality for operating systems and for benchmarking code. The module incorporates several counters, which define the timebases needed for scheduling in the operating system.

This module is specifically designed to fulfill the requirements for OSEK (“Offene Systeme und deren Schnittstellen für die Elektronik im Kraftfahrzeug”; “Open Systems and the Corresponding Interfaces for Automotive Electronics”) as well as OSEK/Time compliant operating systems.

The timers also provide the ability to benchmark certain areas of code by reading the counter contents at the beginning and the end of the desired code range and calculating the difference between the values.

For more information, see *Real Time Interrupt (RTI) Module* section in the device TRM.

#### 7.4.5.25 Timers

There are sixteen timer modules in the device.

All timers include specific functions to generate accurate tick interrupts to the operating system.

Each timer can be clocked from several different independent clocks. The selection of clock source is made from registers in the MCU\_CTRL\_MMR0/CTRL\_MMR0.

In the MCU domain the device provides 2 timer pins to be used as MCU Timer Capture inputs or as MCU Timer PWM outputs. In order to provide maximum flexibility, these 2 pins may be used with any of MCU\_TIMER0

through MCU\_TIMER3 instances. System level muxes are used to control the capture source pin for each MCU\_TIMER[3-0] and the MCU\_TIMER[3-0] source for each MCU\_TIMER\_IO[1-0] PWM output

In the MAIN domain the device provides 8 timer pins to be used as Timer Capture inputs or as Timer PWM outputs. For maximum flexibility, these 8 pins may be used with any of TIMER0 through TIMER11 instances. System level muxes are used to control the capture source pin for each TIMER[11-0] and the TIMER[11-0] source for each TIMER\_IO[7-0] PWM output.

For more information, see *Timers* section in the device TRM.

#### **7.4.5.26 UART**

The UART is a slave peripheral that utilizes the DMA for data transfer or interrupt polling via host CPU. There are five UART modules in the device. All UART modules support IrDA and CIR modes when 48 MHz function clock is used. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

The CIR mode uses a variable pulse-width modulation (PWM) technique (based on multiples of a programmable  $t$  period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits data packets based on a user-definable frame structure and packet content.

For more information, see *Universal Synchronous/Asynchronous Receiver/Transmitter (UART)* section in the device TRM.

#### **7.4.5.27 USB**

Similar to earlier versions of USB bus, USB 3.0 is a general-purpose cable bus, supporting data exchange between a host device and a wide range of simultaneously accessible peripherals.

The device supports two USB subsystems, both instantiated in the MAIN system domain:

- USB3SS0 is SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem with integrated SS (USB3.0) PHY and HS/FS/LS (USB2.0) PHY
- USB3SS1 is HighSpeed (HS) USB 2.0 Dual-Role-Device (DRD) subsystem with integrated HS/FS/LS (USB2.0) PHY

For more information, see *Universal Serial Bus (USB) Subsystem* section in the device TRM.

### **7.5 Identification**

#### **7.5.1 Revision Identification**

For more information about Revision Identification, see [Section 9.1, Device Nomenclature](#).

#### **7.5.2 Die Identification**

The device part number identification data can be read in the CTRLMMR\_WKUP\_JTAG\_DEVICE\_ID register.

For more information about Die Identification, see *Device Identification* section in the device TRM.

#### **7.5.3 JTAG Identification**

The manufacturer identity, the boundary scan part number, and the silicon revision of the device can be read in the CTRLMMR\_WKUP\_JTAGID register.

For more information about JTAG Identification, see *Device Identification* section in the device TRM.

#### **7.5.4 ROM Code Identification**

The ROM code uses several global memories in the MSRAM that are useful for debugging.

For more information about ROM Code Identification, see *Global Memory Addresses Used by ROM Code* section in the device TRM.

## 7.6 Boot Modes

This device supports primary boot from the UART, I2C, OSPI, HyperBus, parallel NOR Flash, SD or eMMC™, USB, PCIe, and Ethernet interfaces. If the primary boot fails, the device also supports a secondary backup boot from the UART, I2C, OSPI (legacy SPI mode only), HyperBus, SD, USB, and Ethernet interfaces.

The Boot Mode pins (BOOTMODE[18:00] and MCU\_BOOTMODE[09:00]) provide the means to select the desired boot mode before the device is powered up. It is the user's responsibility to properly set the (MCU\_)BOOTMODE pins (via pullups or pulldowns) depending on the desired boot scenario.

For more detailed information about the primary/secondary Boot Modes, including the Boot Mode pins, usage, and selections, see the *Boot Mode Pins* section in the device TRM.

## 8 Applications, Implementation, and Layout

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test design implementation to confirm system functionality.

### 8.1 Device Connection and Layout Fundamentals

#### 8.1.1 Power Supply Decoupling and Bulk Capacitors

##### 8.1.1.1 Power Distribution Network Implementation Guidance

The [Sitara™ Processor Power Distribution Networks: Implementation and Analysis](#) provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI supports *only* designs that follow the board design guidelines contained in the application report.

#### 8.1.2 External Oscillator

For more information, see [Section 6.9.4.1, Input Clocks / Oscillators](#).

#### 8.1.3 JTAG and EMU

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the [XDS Target Connection Guide](#).

For more recommendations on EMU routing, see [Emulation and Trace Headers Technical Reference Manual](#).

#### 8.1.4 Reset

The device incorporates four external reset pins (MCU\_PORz, MCU\_RESETh, PORz, and RESETh) and four reset status pins (MCU\_PORz\_OUT, MCU\_RESETh\_STATz, PORz\_OUT, and RESETh\_STATz). Additional reset modes are available through internal registers and emulation.

The device integrates an on-chip Power-on-Reset (POR) generator. Additionally, this device supports an external POR generation through a PORz and MCU\_PORz input pin. The MCU\_BYPASS\_POR pin selects the POR source. When the MCU\_BYPASS\_POR pin is set high at power-up, on-chip POR generation will be completely bypassed and the external POR used. When it is low, the POR is generated internally. However, the four external reset inputs must all be pulled high to enable this internal POR generation.

#### 8.1.5 Unused Pins

For more information about Unused Pins, see [Section 5.5, Connections for Unused Pins](#).

#### 8.1.6 Hardware Design Guide for AM65x/DRA80xM Devices

The [Hardware Design Guide for AM65x/DRA80xM Devices](#) document describes hardware system design considerations for the AM65x/DRA80xM family of processors. This design guide is intended to be used as an aid during the development of application hardware.

## 8.2 Peripheral- and Interface-Specific Design Information

### 8.2.1 DDR Board Design and Layout Guidelines

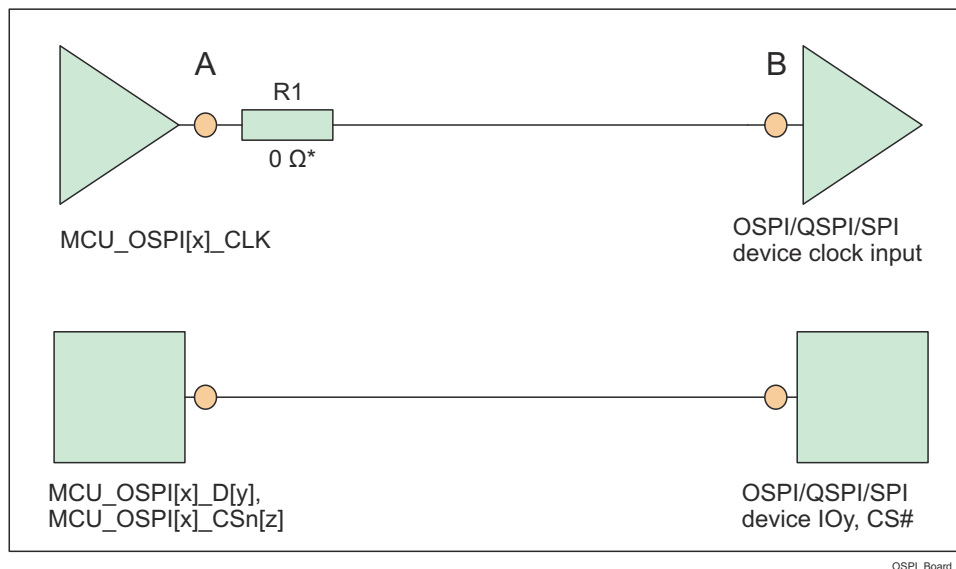
The goal of the [AM65x/DRA80xM DDR Board Design and Layout Guidelines](#) is to make the DDR4 system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using DDR4 memories that follow the guidelines in this document.

### 8.2.2 OSPI Board Design and Layout Guidelines

The following section details the routing guidelines that must be observed when routing the OSPI interfaces.

#### 8.2.2.1 No Loopback and Internal Pad Loopback

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The signal propagation delay from the MCU\_OSPI[x]\_CLK signal to the flash device must be  $< 450\text{pS}$  ( $\sim 7\text{cm}$  as stripline or  $\sim 8\text{cm}$  as microstrip)
- $50\ \Omega$  PCB routing is recommended along with series terminations, as shown in [Figure 8-1](#)
- Propagation delays and matching:
  - A to B  $< 450\text{ps}$
  - Matching skew:  $< 60\text{pS}$



\* $0\ \Omega$  resistor (R1), located as close as possible to the MCU\_OSPI[x]\_CLK pin, is placeholder for fine tuning, if needed

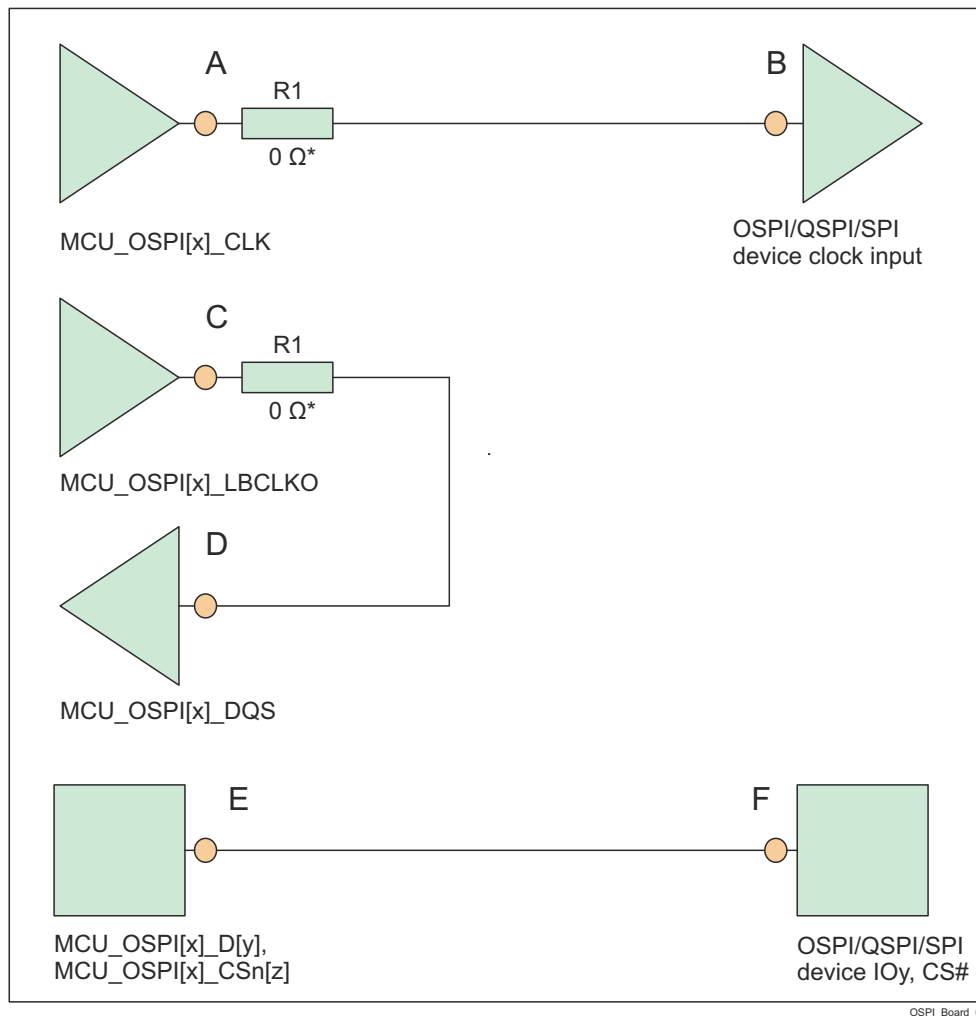
**Figure 8-1. OSPI Interface High Level Schematic**

#### 8.2.2.2 External Board Loopback

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The MCU\_OSPI[x]\_LBCLKO output signal must be looped back into the MCU\_OSPI[x]\_DQS input
- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to half of the signal propagation delay from the MCU\_OSPI[x]\_LBCLKO pin to the MCU\_OSPI[x]\_DQS pin  $((C\text{ to }D)/2)$ . See the note below.
- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) must be approximately equal to the signal propagation delay of the control and data signals between the flash device and the SoC device (E to F, or F to E)
- $50\ \Omega$  PCB routing is recommended along with series terminations, as shown in [Figure 8-2](#)
- Propagation delays and matching:
  - A to B = E to F = (C to D) / 2
  - Matching skew:  $< 60\text{pS}$

### Note

The OSPI Board Loopback Hold time requirement (described in [Section 6.9.5.18, OSPI](#)) is larger than the Hold time provided by a typical flash device. Therefore, the length of MCU\_OSPI[x]\_LBCLKO pin to the MCU\_OSPI[x]\_DQS pin (C to D) may need to be shortened to compensate.

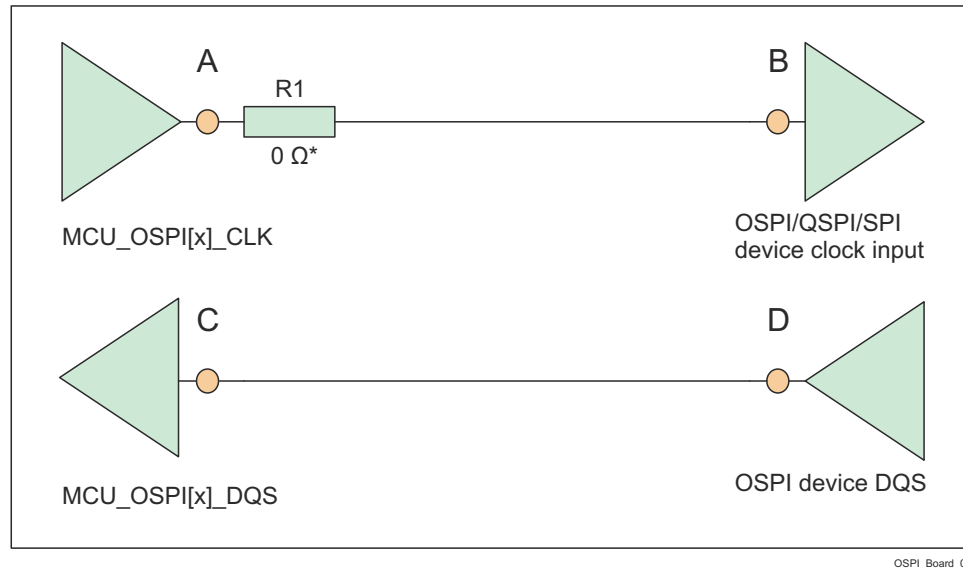


\*0 Ω resistor (R1), located as close as possible to the MCU\_OSPI[x]\_CLK and MCU\_OSPI[x]\_LBCLKO pins, is placeholder for fine tuning, if needed

**Figure 8-2. OSPI Interface High Level Schematic**

#### 8.2.2.3 DQS (Only Available in Octal Flash Devices)

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The DQS pin of the flash devices must be connected to MCU\_OSPI[x]\_DQS signal
- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to the signal propagation delay from the MCU\_OSPI[x]\_DQS pin to the DQS output pin (C to D)
- 50 Ω PCB routing is recommended along with series terminations, as shown in [Figure 8-3](#)
- Propagation delays and matching:
  - A to B = C to D
  - Matching skew: < 60pS



\*0 Ω resistor (R1), located as close as possible to the MCU\_OSPI[x]\_CLK pin, is placeholder for fine tuning, if needed

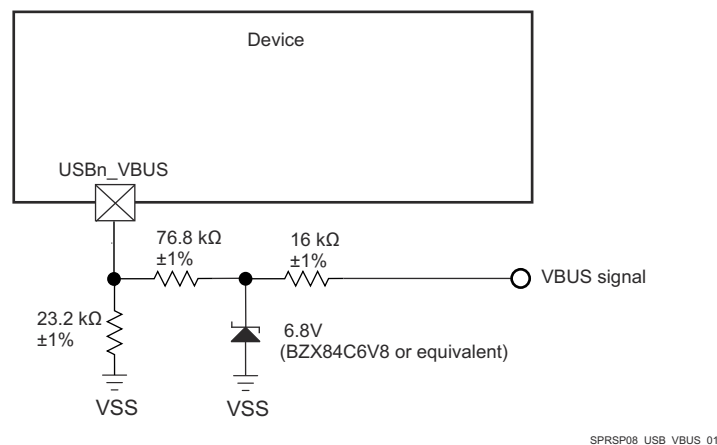
**Figure 8-3. OSPI Interface High Level Schematic**

### 8.2.3 USB Design Guidelines

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5 V for normal operation, and as high as 20 V when the Power Delivery addendum is supported. Some automotive applications require a max voltage to be 30 V.

The AM65xx device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the [Figure 8-4](#)), which limits the voltage applied to the actual device pin (USB0\_VBUS, USB1\_VBUS). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of zener diode at 5 V should be less than 100 nA.

(1)



**Figure 8-4. USB VBUS Detect Voltage Divider / Clamp Circuit**

The USB0\_VBUS and USB1\_VBUS pins may be considered to be fail-safe because the external circuit in [Figure 8-4](#) limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

## 8.2.4 High Speed Differential Signal Routing Guidance

The [High-Speed Interface Layout Guidelines](#) provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application report.

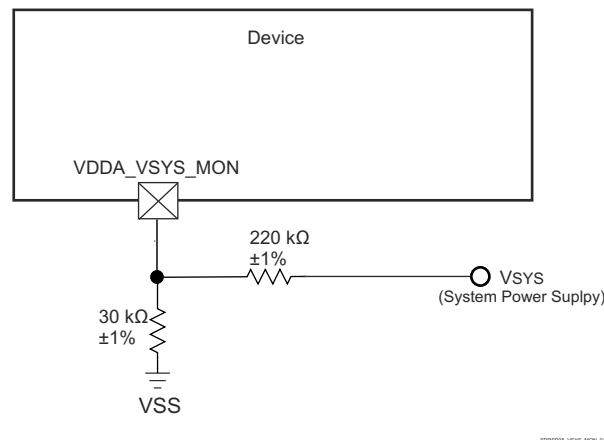
## 8.2.5 System Power Supply Monitor Design Guidelines

The VDDA\_VSYS\_MON pin provides a way to monitor the system power supply and is not fail-safe, unless implemented with the appropriate resistor voltage divider source. This pin should be sourced with a resistor voltage divider that receives its power from the system power supply.

The output of the resistor voltage divider is connected to the VDDA\_VSYS\_MON pin which has a trigger voltage of  $0.5\text{ V} \pm 5\%$ . The resistor voltage divider should be implemented such that it has a reference current in the range of  $1\text{ }\mu\text{A}$  to  $50\text{ }\mu\text{A}$ , output voltage that never exceeds the maximum value defined in [Section 6.1, Absolute Maximums Ratings](#), and output voltage of  $0.54\text{ V}$  when the system supply drops to its lowest desired operating voltage.

The recommended output voltage of  $0.54\text{ V}$  provides  $40\text{ mV}$  of margin that includes  $5\%$  for tolerance of the voltage monitor,  $1\%$  for tolerance of each resistor, plus  $5\text{ mV}$  of potential error introduced by input leakage current. This value ensures the voltage monitor will never trigger before reaching the expected trigger voltage.

[Figure 8-5](#) presents an example, when the system power supply voltage is nominally  $5\text{ V}$  and the desired trigger threshold is  $-10\%$  or  $4.5\text{ V}$ .



**Figure 8-5. System Supply Monitor Voltage Divider Circuit**

In this example the voltage divider ratio should be  $(4.5\text{ V} / 0.54\text{ V}) = 8.33$ . This ratio produces a  $0.54\text{ V}$  potential on the VDDA\_VSYS\_MON pin when the system power supply is  $4.5\text{ V}$ . In this case, the voltage monitor will trigger in the range of  $3.88\text{ V}$  to  $4.5\text{ V}$ . Precision  $1\%$  resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider.

## 8.2.6 MMC Design Guidelines

The MMC peripheral on this device contains an integrated SDIO LDO for handling automatic voltage transitions for SD Interfaces. For details about how to connect the device pins associated with the SDIO LDO, refer to [Figure 8-10](#) through [Figure 8-12](#).

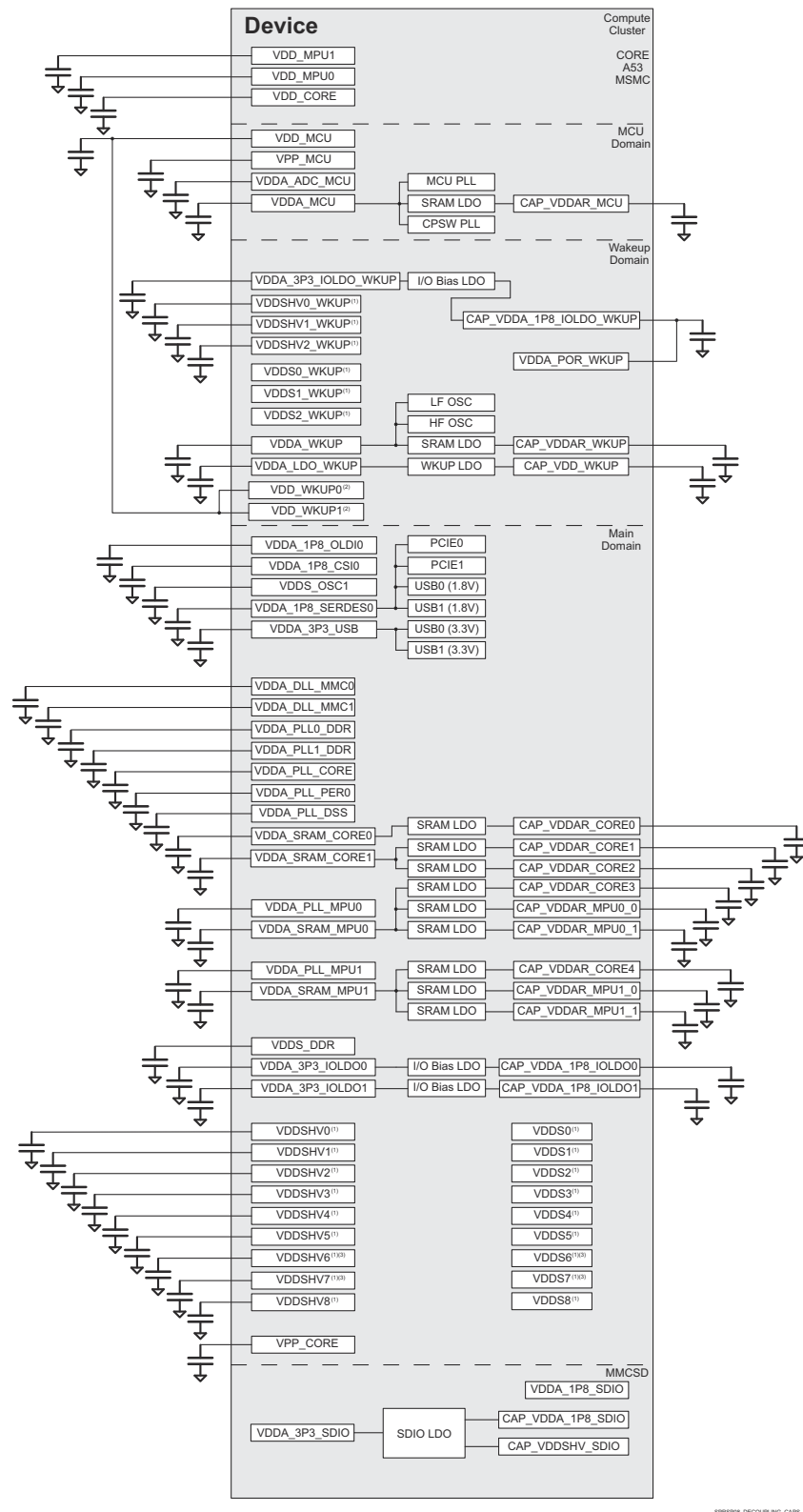
## 8.2.7 Integrated Power Management Features

The device offers integrated power management features that simplify design and cost/BOM of the system level power solution. Simplicity of the system design enables modular and scalable solutions suitable for platform design and re-use. The [AM65x Power Management Features](#) User Guide introduces the integrated power management features and advantages for system level power solution.



## 8.2.8 External Capacitors

Figure 8-6 shows an example of the external decoupling capacitor connections.



**Figure 8-6. External Decoupling Capacitor Connections**

### 8.2.8.1 LVCMOS External Capacitor Connections

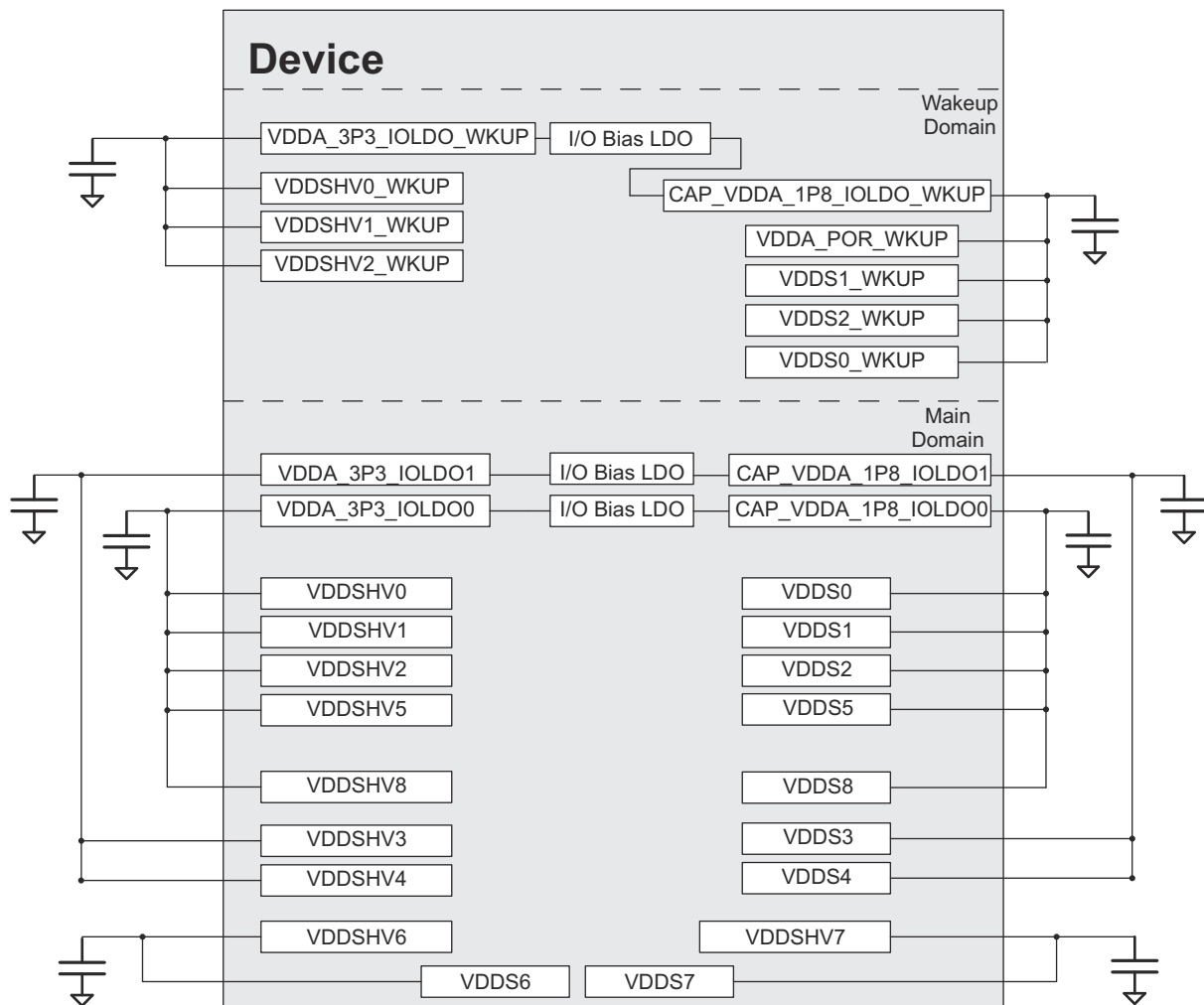
Each VDDSHV[8:0], and VDDSHV[2:0]\_WKUP can be configured as 1.8 V or 3.3 V. Figure 8-7 through Figure 8-10 illustrate different system configurations for the dual-voltage I/O supplies.

VDDSHV[8:0], and VDDSHV[2:0]\_WKUP are the dual-voltage LVCMOS I/O supplies, while VDDS[8:0] are the dual-voltage LVCMOS I/O bias supplies. If any of the VDDSHV[8:0] or VDDSHV[2:0]\_WKUP are configured for 3.3 V operation, the corresponding VDDS[8:0] or VDDS[2:0]\_WKUP should be sourced from the internal I/O Bias LDO. When any of the VDDSHV[8:0] or VDDSHV[2:0]\_WKUP are configured for 1.8 V operation, both VDDS[8:0] and VDDSHV[8:0] or VDDS[2:0]\_WKUP and VDDSHV[2:0]\_WKUP should be supplied from the same source.

Two I/O Bias LDOs are integrated on this device to share load current. The recommended load sharing is as follows:

- IOLDO0 : VDDS0, VDDS1, VDDS2, VDDS5, VDDS7, VDDS8
- IOLDO1 : VDDS3, VDDS4, VDDS6

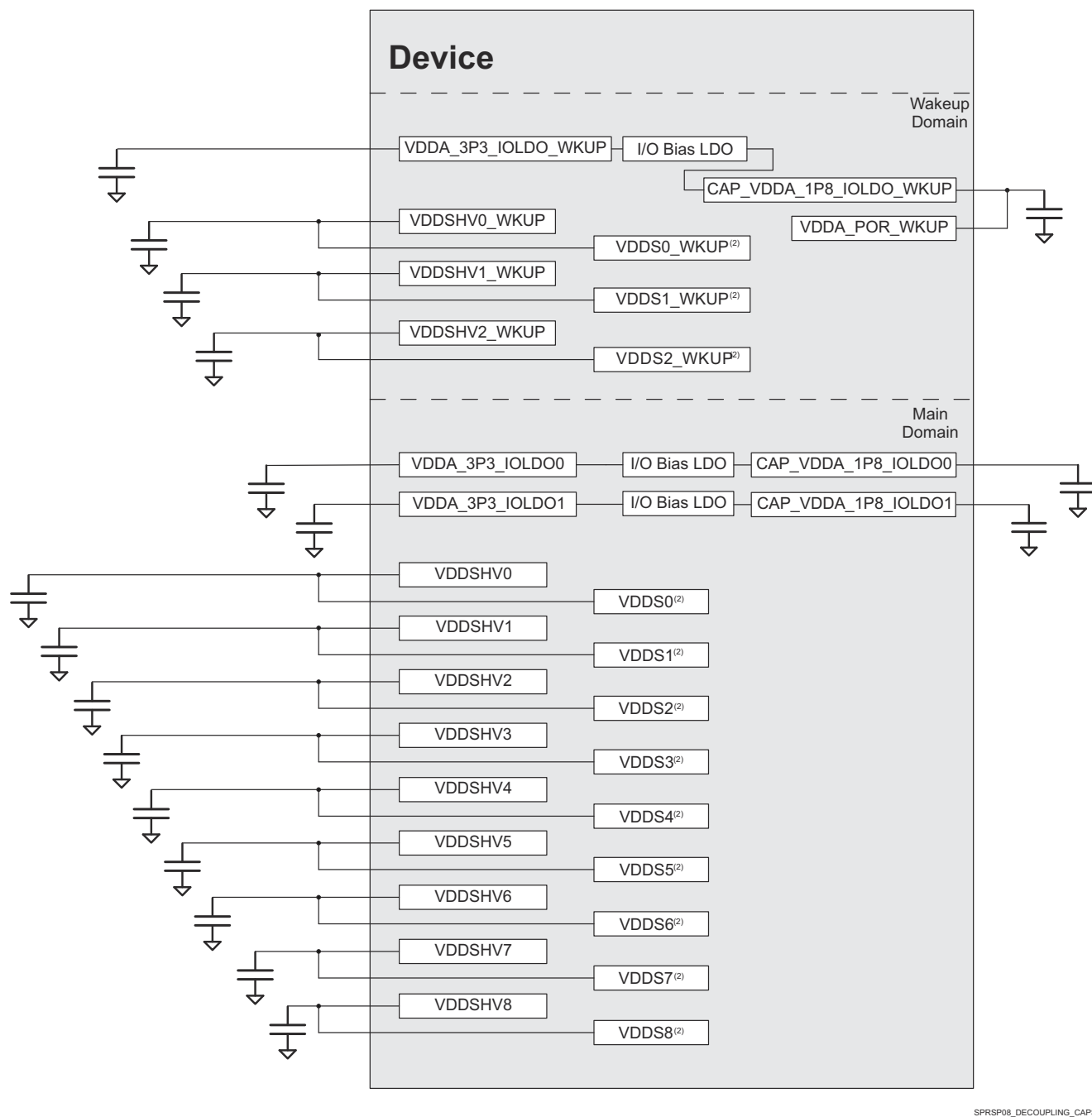
Figure 8-7 shows all VDDSHV[8:0], and VDDSHV[2:0]\_WKUP supplies configured for 3.3V operation.



SPRSP08\_DECOUPLING\_CAPS\_01

**Figure 8-7. All VDDSHV[8:0], and VDDSHV[2:0]\_WKUP Supplies Configured for 3.3 V Operation**

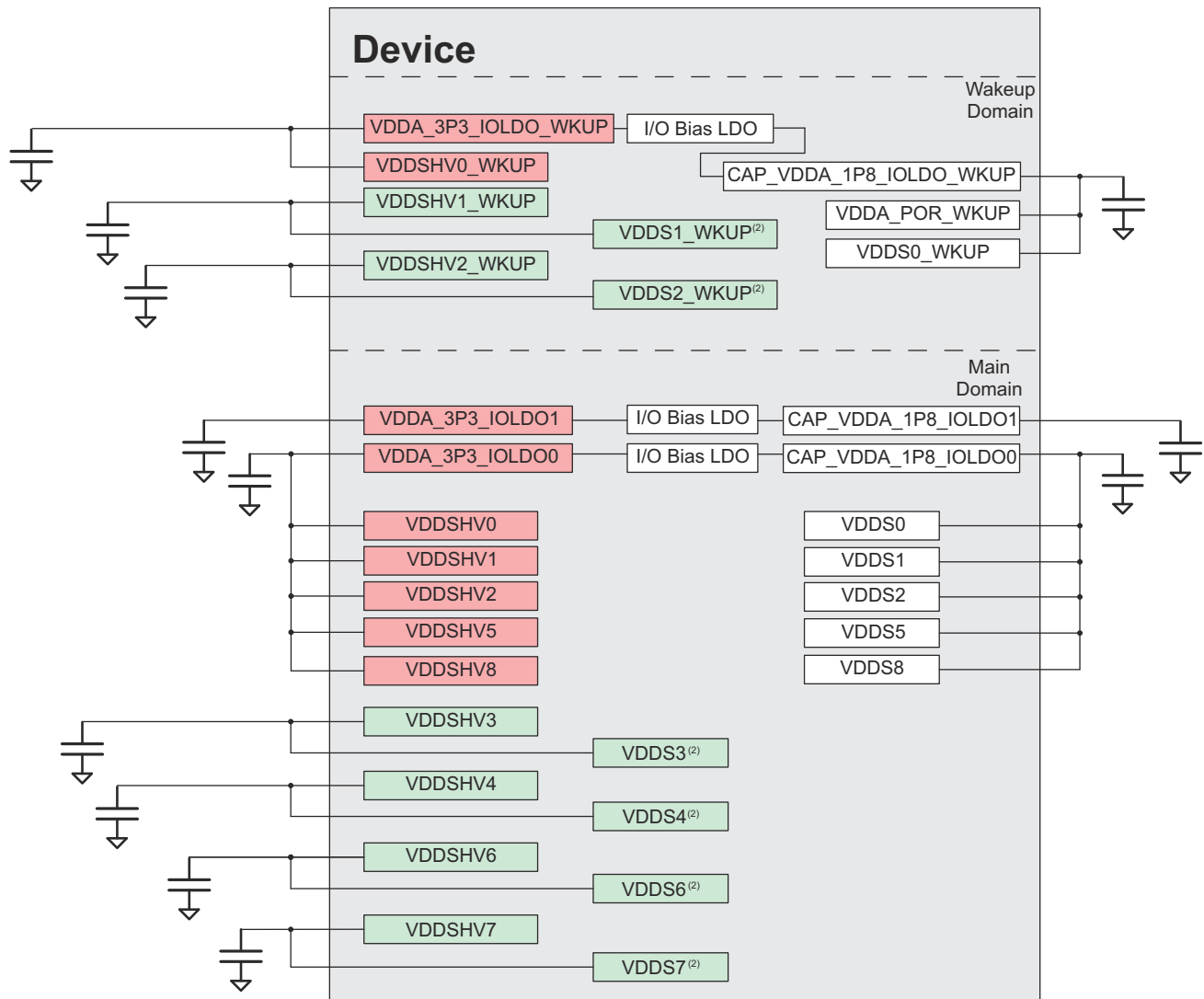
Figure 8-8 shows all VDDSHV[8:0] and VDDSHV[2:0]\_WKUP supplies configured for 1.8 V operation.



SPRSP08\_DECOUPLING\_CAPS\_03

**Figure 8-8. All VDDSHV[8:0] and VDDSHV[2:0]\_WKUP Supplies Configured for 1.8V Operation**

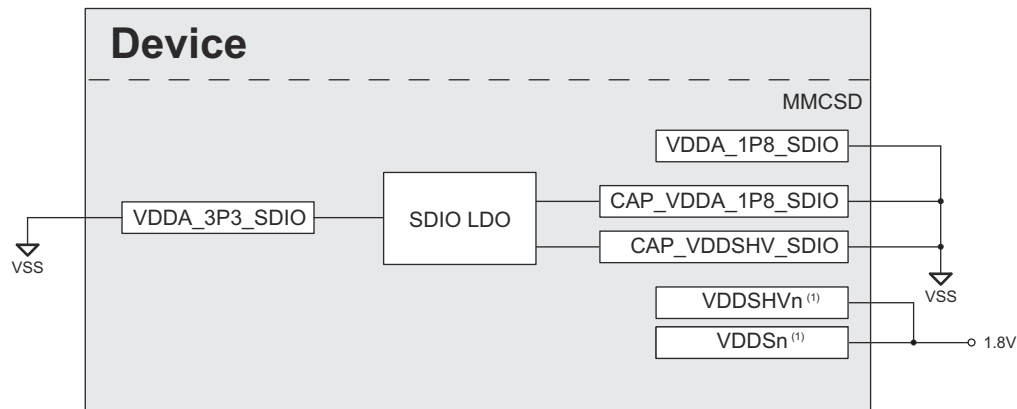
Figure 8-9 shows a split configuration where VDDSHV[0, 1, 2, 5, 8] and VDDSHV0\_WKUP are configured for 3.3 V operation, while VDDSHV[3, 4, 6, 7] and VDDSHV[2:1]\_WKUP are configured for 1.8 V operation. Note the colors indicate rails that are tied to the same source.



SPRSP08\_DECOUPLING\_CAPS\_04

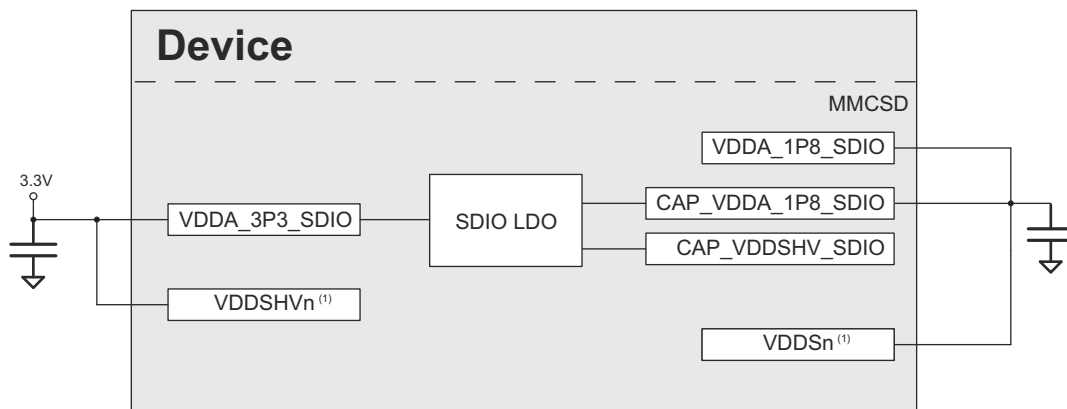
**Figure 8-9. VDDSHV[8:0] and VDDSHV[2:0]\_WKUP Supplies Configured for Combination of 1.8 V or 3.3 V Operation**

Figure 8-10 through Figure 8-12 illustrates the system configuration when VDDSHV6 or VDDSHV7 is used as the MMCSD supply.



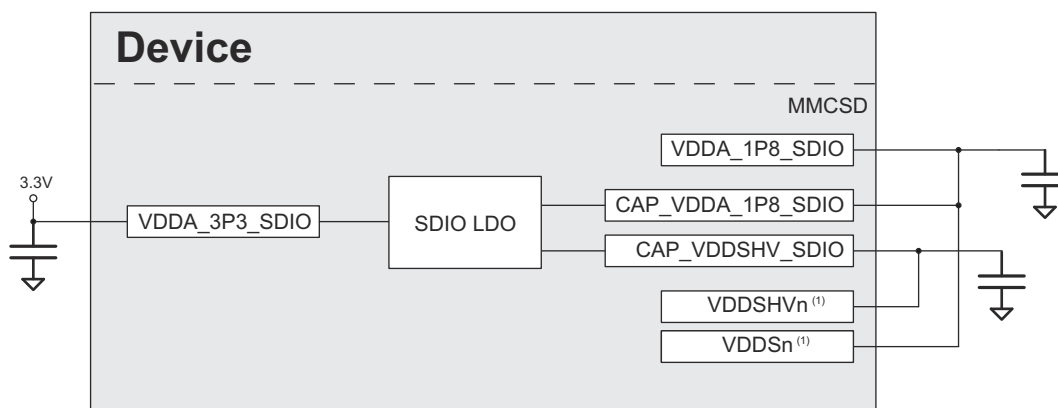
SPRSP08\_DECOUPLING\_CAPS\_06

Figure 8-10. VDDSHV6 or VDDSHV7 Used as the MMCSD Supply for Fixed 1.8V IO



SPRSP08\_DECOUPLING\_CAPS\_07

Figure 8-11. VDDSHV6 or VDDSHV7 Used as the MMCSD Supply for Fixed 3.3V IO



SPRSP08\_DECOUPLING\_CAPS\_05

Figure 8-12. VDDSHV6 or VDDSHV7 Used as the MMCSD Supply for Dynamic 3.3V/1.8V IO

### 8.2.9 Thermal Solution Guidance

The [Thermal Design Guide for DSP and Arm Application Processors](#) Application Note provides guidance for successful implementation of a thermal solution for system designs containing this device. This document

provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application report.

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, AM654x). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

**TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.

**TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

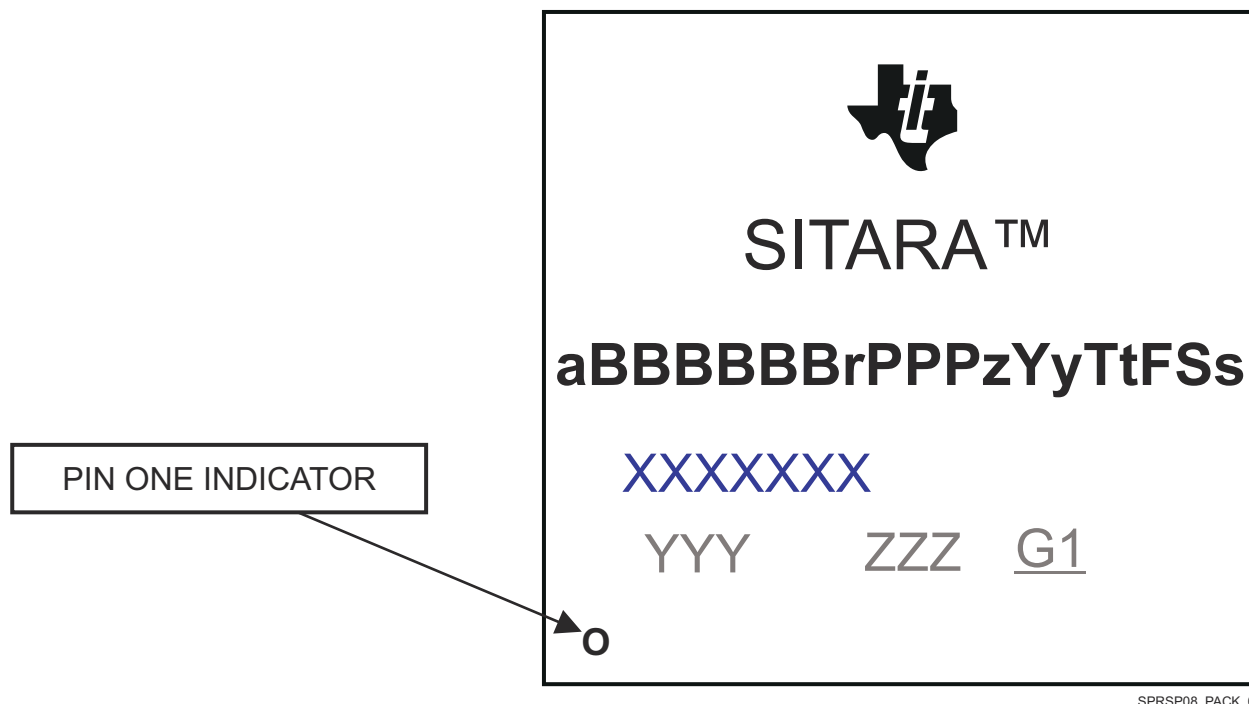
"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM65xx devices in the ACD package type, see the Package Option Addendum of this document, the TI website ([ti.com](http://ti.com)), or contact your TI sales representative.

### 9.1.1 Standard Package Symbolization



SPRSP08\_PACK\_01

**Figure 9-1. Printed Device Reference**

### 9.1.2 Device Naming Convention

**Table 9-1. Nomenclature Description**

| FIELD PARAMETER | FIELD DESCRIPTION           | VALUE  | DESCRIPTION                                                                                |
|-----------------|-----------------------------|--------|--------------------------------------------------------------------------------------------|
| a               | Device evolution stage      | X      | Prototype                                                                                  |
|                 |                             | P      | Preproduction (production test flow, no reliability data)                                  |
|                 |                             | BLANK  | Production                                                                                 |
| BBBBBB          | Base production part number | AM6548 | Quad Core High Tier (See <a href="#">Table 4-1, Device Comparison</a> )                    |
|                 |                             | AM6528 | Dual Core High Tier (See <a href="#">Table 4-1, Device Comparison</a> )                    |
|                 |                             | AM6546 | Quad Core Low Tier (See <a href="#">Table 4-1, Device Comparison</a> )                     |
|                 |                             | AM6526 | Dual Core Low Tier (See <a href="#">Table 4-1, Device Comparison</a> )                     |
| r               | Device revision             | BLANK  | SR 1.0                                                                                     |
|                 |                             | A      | SR 2.0                                                                                     |
|                 |                             | B      | SR 2.1                                                                                     |
| PPP             | Package Designator          | ACD    | ACD FCBGA-N784 (23mm × 23mm) Package                                                       |
| z               | Device Speed                | X      | High speed grade (see <a href="#">Table 6-1, Speed Grade Maximum Frequency</a> )           |
|                 |                             | OTHER  | Alternate speed grade                                                                      |
| Yy              | Device type                 | E      | All industrial protocols enabled (basic protocols plus EtherCAT slave and POWERLINK slave) |
|                 |                             | BLANK  | Basic Industrial protocols enabled                                                         |
| Tt              | Temperature <sup>(1)</sup>  | A      | Extended (see <a href="#">Section 6.4, Recommended Operating Conditions</a> )              |
|                 |                             | BLANK  | Commercial (see <a href="#">Section 6.4, Recommended Operating Conditions</a> )            |
| F               | Functional Safety           | BLANK  | No safety features                                                                         |
|                 |                             | F      | Safety features enabled including lock-step MCU                                            |



**Table 9-1. Nomenclature Description (continued)**

| FIELD PARAMETER | FIELD DESCRIPTION                | VALUE | DESCRIPTION                                           |
|-----------------|----------------------------------|-------|-------------------------------------------------------|
| Ss              | Security Identifier              | S1    | High-Security device, Secure Boot Supported           |
|                 |                                  | SB    | Dummy key High-Security device, Secure Boot Supported |
|                 |                                  | BLANK | General purpose device                                |
| XXXXXXX         | Lot Trace Code (LTC)             |       |                                                       |
| YYY             | Production Code; For TI use only |       |                                                       |
| ZZZ             | Production Code; For TI use only |       |                                                       |
| O               | Pin one designator               |       |                                                       |
| G1              | ECAT—Green package designator    |       |                                                       |

(1) Applies to device max junction temperature.

---

#### Note

X6580ACD is a prototype part that is functionally equivalent to XAM6548ACDXEAF.

---

#### Note

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

---

## 9.2 Tools and Software

The following products support development for AM65xx platforms:

### Design kits and evaluation modules

**AM65x evaluation module** The AM65x Evaluation Module provides a platform to quickly start evaluation of Sitara™ Arm® Cortex®-A53 AM65x Processors (AM6548, AM6546, AM6528, AM6526) and accelerate development for HMI, networking, patient monitoring, and other industrial applications. It is a development platform based on the quad core Cortex-A53, dual Cortex-R5F processor that is integrated with ample connectivity such as PCIe, USB 3.0/2.0, Gigabit Ethernet, and more.

### Development tools

**Clock Tree Tool for Sitara, Automotive, Vision Analytics, & Digital Signal Processors** The Clock Tree Tool (CTT) for Sitara™ Arm®, Automotive, and Digital Signal Processors is an interactive clock tree configuration software that provides information about the clocks and modules in these TI devices. It allows the user to:

- Visualize the device clock tree
- Interact with clock tree elements and view the effect on PRCM registers
- Interact with the PRCM registers and view the effect on the device clock tree
- View a trace of all the device registers affected by the user interaction with clock tree

**Code Composer Studio™ (CCS) Integrated Development Environment (IDE) for Sitara Arm Processors** Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

**Pin mux tool** The Pin MUX Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs. Results are output as C header/code files that can be imported into software development kits (SDKs) or used to configure

customer's custom software. Version 4 of the Pin Mux utility adds the capability of automatically selecting a mux configuration that satisfies the entered requirements.

## Models

[AM654x/DRA80xM BSDL Model](#) BSDL Model

[AM654x/DRA80xM IBIS File](#) IBIS Model

[AM654x/DRA80xM Thermal Models](#) Thermal Model

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at [ti.com](#). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

## 9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the AM65xx devices.

### Technical Reference Manual

[AM65x/DRA80xM Processors Technical Reference Manual](#) Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM65xx family of devices.

### Errata

[AM65x/DRA80xM Processors Silicon Revision 2.1/2.0/1.0 Silicon Errata](#) Describes the known exceptions to the functional specifications for the device.

## 9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 9.5 Trademarks

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## 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.7 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

### Changes from June 30, 2021 to September 15, 2023 (from Revision B (June 2021) to Revision C (September 2023))

Page

|                                                                                                                                                 |   |
|-------------------------------------------------------------------------------------------------------------------------------------------------|---|
| • <b>Global:</b> Moved the Revision History section to the back of the document.....                                                            | 1 |
| • (Features): Updated/Changed the "Functional Safety-Compliant" feature bullets and added the ulink to the "Safety-related certification" ..... | 1 |
| • (Package Information): Updated table title and the table to match the new content standard.....                                               | 4 |

## 11 Mechanical, Packaging, and Orderable Information

### 11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)              |
|--------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------------|
| <a href="#">AM6526BACDXA</a>   | Active        | Production           | FCCSP (ACD)   784 | 60   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6526BACDXA<br>900<br>900 ACD   |
| AM6526BACDXA.B                 | Active        | Production           | FCCSP (ACD)   784 | 60   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6526BACDXA<br>900<br>900 ACD   |
| <a href="#">AM6526BACDXEAF</a> | Active        | Production           | FCCSP (ACD)   784 | 60   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6526BACDXEAF<br>900<br>900 ACD |
| AM6526BACDXEAF.B               | Active        | Production           | FCCSP (ACD)   784 | 60   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6526BACDXEAF<br>900<br>900 ACD |
| <a href="#">AM6528BACDXEA</a>  | Active        | Production           | FCCSP (ACD)   784 | 60   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6528BACDXEA<br>900<br>900 ACD  |
| AM6528BACDXEA.B                | Active        | Production           | FCCSP (ACD)   784 | 60   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6528BACDXEA<br>900<br>900 ACD  |
| <a href="#">AM6546BACDXA</a>   | Active        | Production           | FCCSP (ACD)   784 | 60   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6546BACDXA<br>900<br>900 ACD   |
| AM6546BACDXA.B                 | Active        | Production           | FCCSP (ACD)   784 | 60   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6546BACDXA<br>900<br>900 ACD   |
| <a href="#">AM6548BACDXEAF</a> | Active        | Production           | FCCSP (ACD)   784 | 60   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6548BACDXEAF<br>900<br>900 ACD |
| AM6548BACDXEAF.B               | Active        | Production           | FCCSP (ACD)   784 | 60   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 105   | AM6548BACDXEAF<br>900<br>900 ACD |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

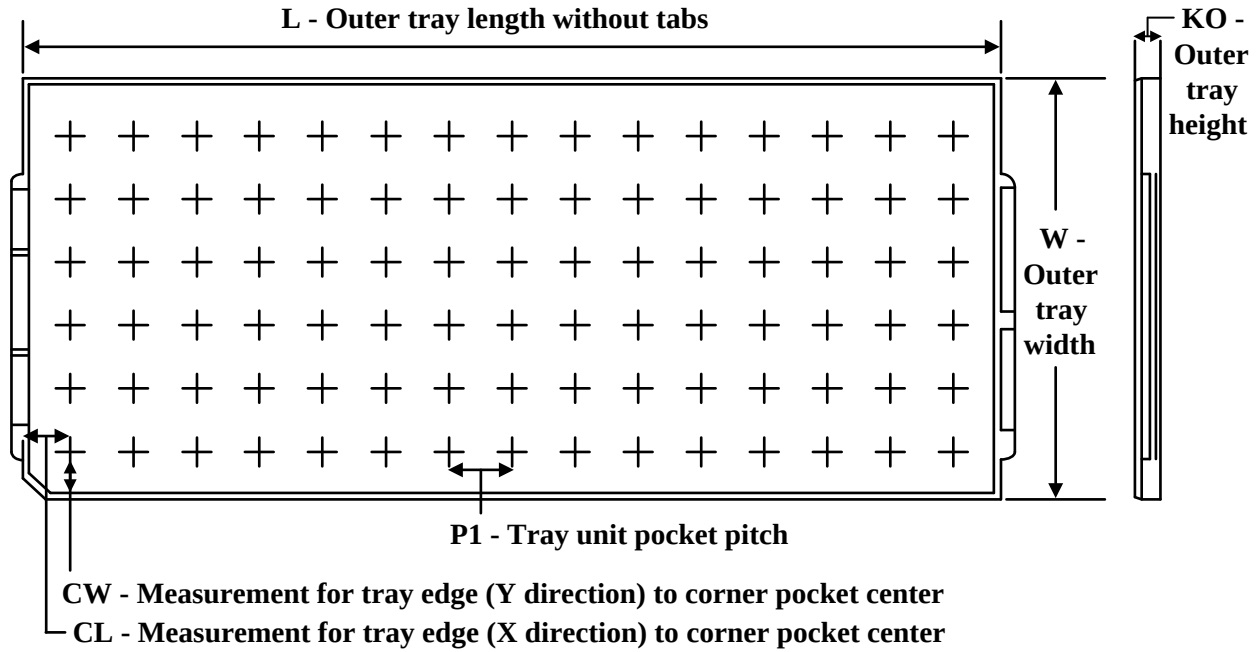
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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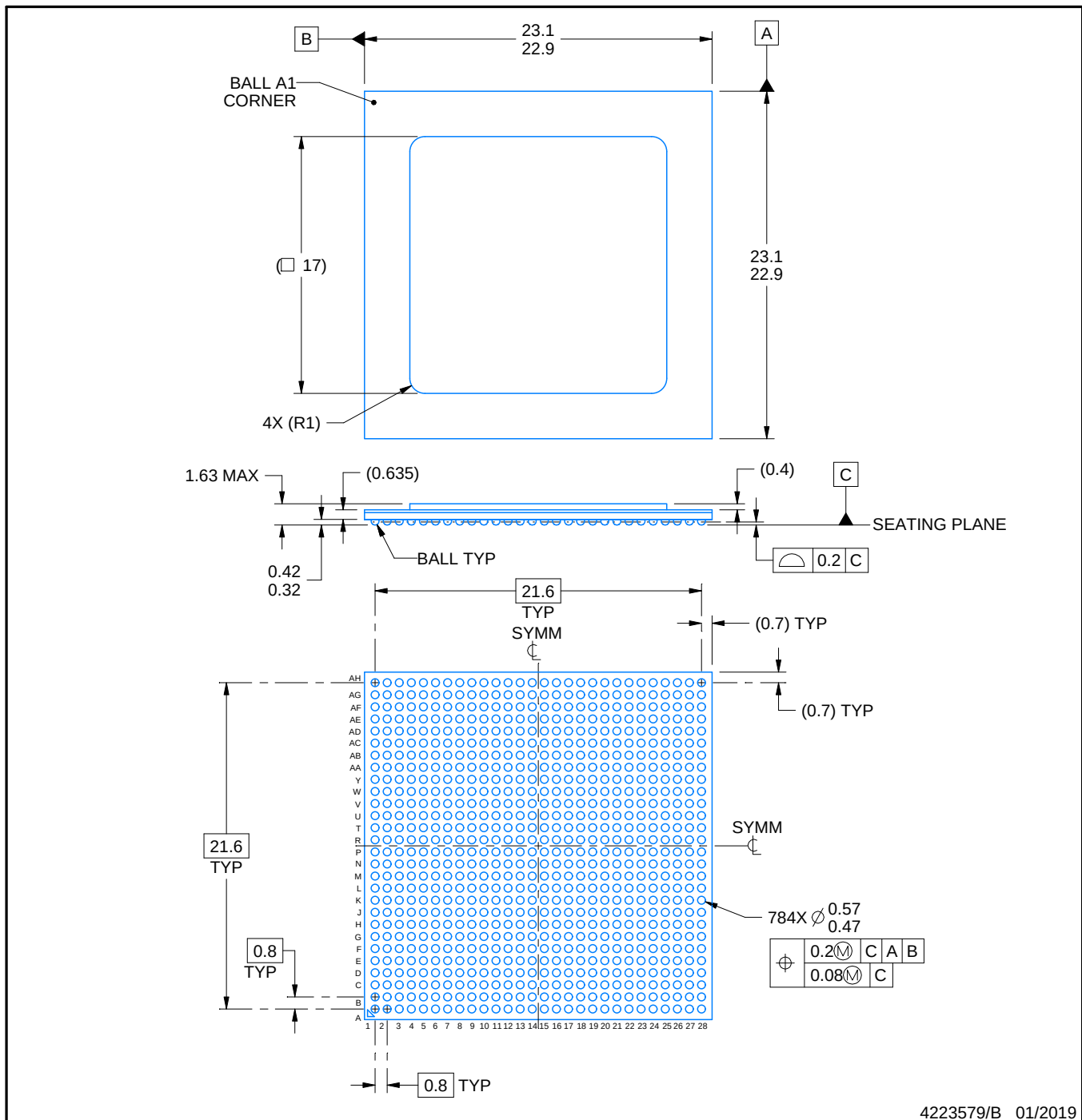
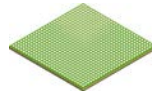
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TRAY**


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device           | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|------------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| AM6526BACDXA     | ACD          | FCCSP        | 784  | 60  | 5 x 12            | 150                  | 322.6  | 135.9  | 7620    | 25.5    | 17.25   | 16.95   |
| AM6526BACDXA.B   | ACD          | FCCSP        | 784  | 60  | 5 x 12            | 150                  | 322.6  | 135.9  | 7620    | 25.5    | 17.25   | 16.95   |
| AM6526BACDXEAF   | ACD          | FCCSP        | 784  | 60  | 5 x 12            | 150                  | 322.6  | 135.9  | 7620    | 25.5    | 17.25   | 16.95   |
| AM6526BACDXEAF.B | ACD          | FCCSP        | 784  | 60  | 5 x 12            | 150                  | 322.6  | 135.9  | 7620    | 25.5    | 17.25   | 16.95   |
| AM6528BACDXEA    | ACD          | FCCSP        | 784  | 60  | 5 x 12            | 150                  | 322.6  | 135.9  | 7620    | 25.5    | 17.25   | 16.95   |
| AM6528BACDXEA.B  | ACD          | FCCSP        | 784  | 60  | 5 x 12            | 150                  | 322.6  | 135.9  | 7620    | 25.5    | 17.25   | 16.95   |
| AM6546BACDXA     | ACD          | FCCSP        | 784  | 60  | 5 x 12            | 150                  | 322.6  | 135.9  | 7620    | 25.5    | 17.25   | 16.95   |
| AM6546BACDXA.B   | ACD          | FCCSP        | 784  | 60  | 5 x 12            | 150                  | 322.6  | 135.9  | 7620    | 25.5    | 17.25   | 16.95   |
| AM6548BACDXEAF   | ACD          | FCCSP        | 784  | 60  | 5 x 12            | 150                  | 322.6  | 135.9  | 7620    | 25.5    | 17.25   | 16.95   |
| AM6548BACDXEAF.B | ACD          | FCCSP        | 784  | 60  | 5 x 12            | 150                  | 322.6  | 135.9  | 7620    | 25.5    | 17.25   | 16.95   |



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## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

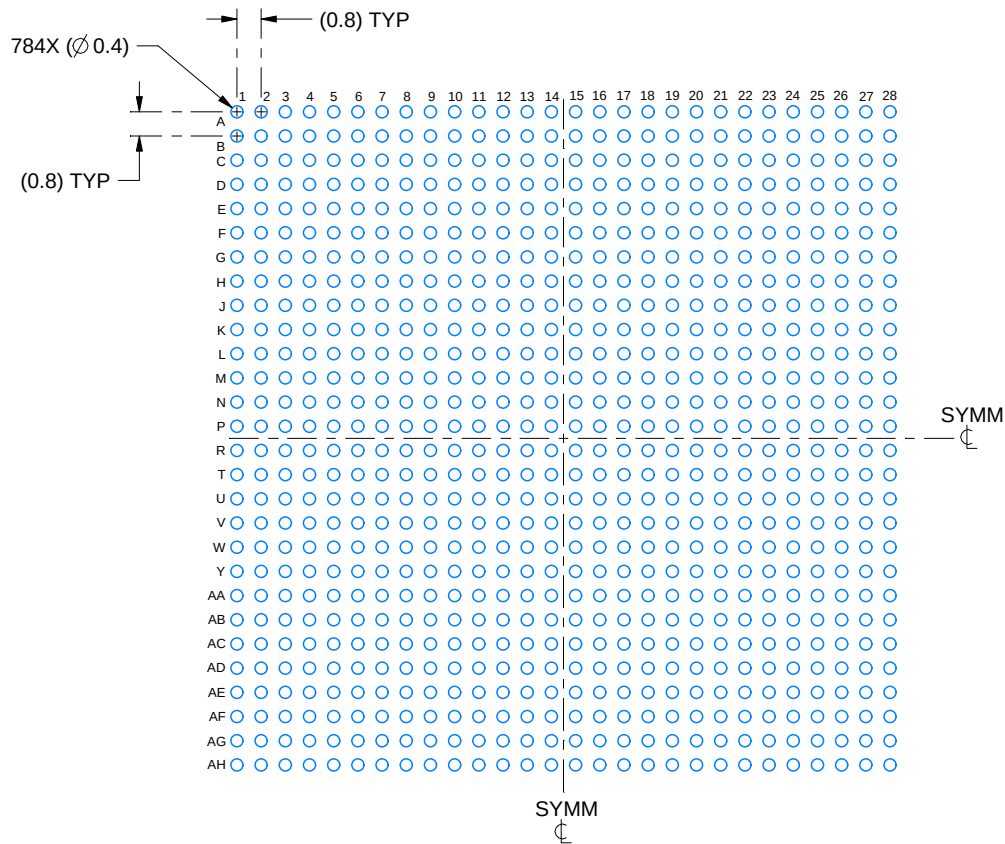


# EXAMPLE BOARD LAYOUT

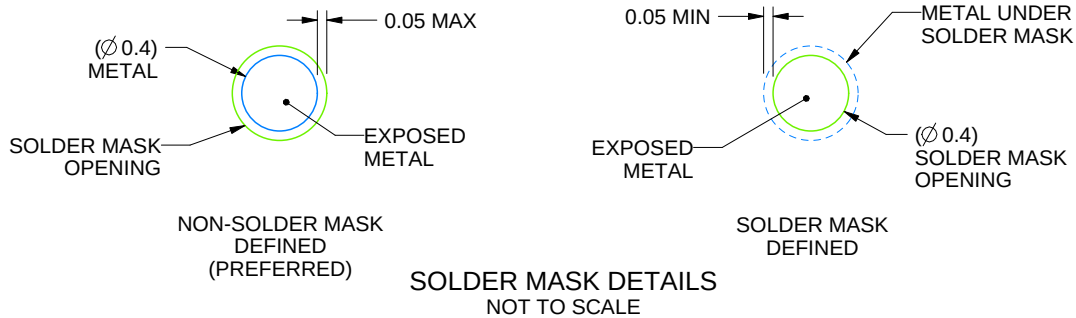
ACD0784A

FCBGA - 1.63 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 4X



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NOTES: (continued)

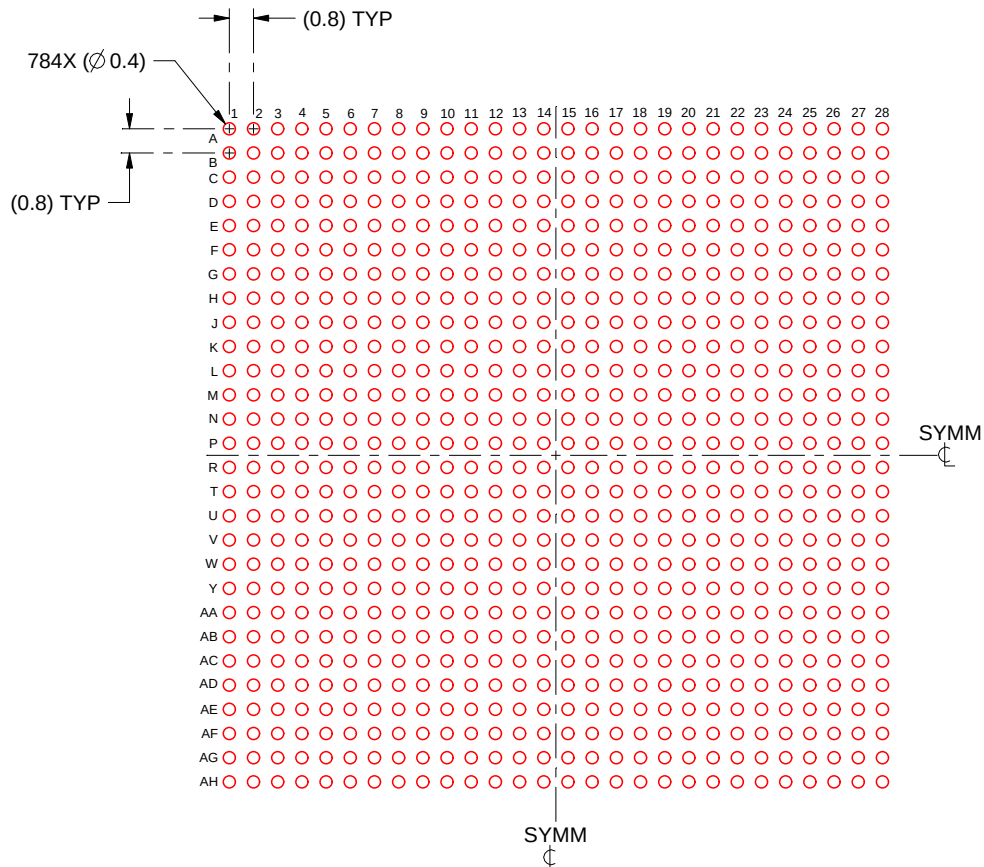
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

ACD0784A

FCBGA - 1.63 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
 BASED ON 0.15 mm THICK STENCIL  
 SCALE: 4X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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