AM13E232x Microcontrollers

1 Features

- **Device Cores**
  - Arm®Cortex®-M33 32-bit CPU up to 250MHz
    - Floating Point Unit (FPU), Custom Datapath Extension (CDE), Memory Protection Unit (MPU) and Micro Trace Buffer (MTB)
    - DSP Extension and 32-bit Trigonometric Math Unit (TMU) accelerates trigonometric calculations
    - DMIPS=*310* and Coremark=*800*
  - 1x TinyEngine™ Neural-Network Processing Unit (NPU) optimized for time-series Edge AI enablement
- **Memories**
  - Up to 512kB (2 banks of up to 256kB, 1kB sectors) of non-volatile flash memory
    - 144-bit word with Error Correction Code
    - Bank swap for dual-image firmware
  - Up to 192kB of 0-wait state SRAM
    - Hardware parity and 1kB instruction cache
- **High-Performance Analog Peripherals**
  - 3x SAR Analog-to-digital Converters (ADCs)
    - 7.81MSPS with 12-bit resolution
    - Each ADC supports up to 32 channels
    - Configurable 1.65V or 2.5V internal shared voltage reference (VREF)
    - Support for external voltage reference (VREF)
    - Hardware oversampling and undersampling modes, with accumulation, averaging and outlier rejection
  - 4x Analog Comparator Sub-systems (CMPSS)
    - Each CMPSS contains 2x Comparators with Window Functionality
    - 2x 10-bit effective DAC and 2x digital filters
    - CMPSS[2:3] support buffered DACL_OUT to pin
  - 3x Programmable Gain Amplifiers (PGA)
    - Unity Gain Support
    - Inverting and non-inverting gain mode support
    - Gain options: 1, 2/-1, 4/-3, 8/-7, 16/-15, 32/-31, 64/-63
    - 4:1 input mux supporting up to 12 channels
    - Programmable output filtering
  - Programmable analog connections between ADC, PGAs, CMPSS and DAC
- **Optimized Low-Power Modes**
  - RUN: 225µA/MHz (CoreMark)
  - STANDBY: 196uA with CPU execution resume and 32kB SRAM retention
  - SHUTDOWN: <5µA with IO wake-up capability
- **Flexible System Peripherals**
  - 12-channel Direct Memory Access (DMA) controller
  - Nested Vectored Interrupt Controller (NVIC)
  - Up to 107 GPIO with Input/Output XBAR connectivity
  - 8 GPIOs with Shutdown Wakeup Capability
  - 1x Windowed Watchdog Timer (WWDT)
    - Independent 32kHz clock with programmable divider
    - 25-bit counter with configurable timer periods
  - 2x general-purpose timers
    - TIMG4 (16-bit), TIMG12 (32-bit)
    - Pre-scaler, Compare/Capture, Shadow
    - Up to 2x channels each
- **Real-time Control Peripherals**
  - 12x Pulse Width Modulator (PWM) channels, all with 75ps high-resolution capability (HRPWM)
    - Minimum Dead-Band Logic (MINDB), Illegal Combo Logic (ICL), and other special features (that is, Diode Emulation [DE]) support
    - Enable Matrix Converters, Multilevel Converters, and Resonant Converters support without additional external logic
  - 3x Motor Control Pulse Width Modulation (MCPWM) modules
    - 6 PWM channels per module with 16-bit time base
    - 4 Start Of Conversion (SOCs) per module enable precise ADC sampling for single shunt or three shunt current sensing mode
    - Support dead-band, trip event and time base synchronization
  - 3x Enhanced Capture (eCAP) modules
    - 32-bit timer for speed, elapsed time, period and duty cycle measurements
    - 1x alternative PWM channel per module
  - 2x Enhanced Quadrature Encoder Pulse (eQEP)
    - Supports linear or rotary incremental encoder interface
    - Edge capture unit for optimized speed measurement at low speed
  - 4x Sigma-Delta Filter Module (SDFM) input channels, 2x independent filters per channel

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  - Device Crossbars (INPUTXBAR, OUTPUTXBAR, PWMXBAR)
    - Flexibility to route signals from GPIO to other modules
    - For example, the INPUTXBAR is used to route signals from a GPIO to other modules such as ADC, CMPSS, MCPWM, eCAP, eQEP, and external interrupts
- **Communication Peripherals**
  - EtherCAT® SubordinateDevice (or SubDevice) Controller (ESC)
  - Fast Serial Interface (FSI) enabling up to 200Mbps data exchange across isolation
  - Two configurable serial interfaces supporting UART (LIN) or I^2C (SMBus/PMBus)
  - Four configurable serial interfaces supporting UART, I^2C, or SPI
  - Two CAN FD/MCAN Controller Area Networks with Flexible Data Rate
- **Clock System**
  - Internal 4MHz/32MHz oscillator (SYSOSC)
  - Internal 32kHz oscillator (LFOSC)
  - System Phase-locked loop (SYSPLL) up to 250MHz
  - External 10MHz to 20MHz crystal oscillator (XTAL)
  - External 4MHz to 48MHz clock input (HFCLK)
- **OS Support**
  - FreeRTOS, Zephyr, Baremetal
- **Safety**
  - Enabling IEC61508 SIL-2 and SIL-3 systems
- **Security and Encryption**
  - Secure Boot/FWU/Debug/JTAG Lock
  - Secure Key Storage and Management
  - Privileged/Non-Privileged resource partitioning
  - Flash Write/Erase/Hide Protections
  - Device Life cycle Management
  - AES Encryption with 128- or 256-bit Key
  - Unique Identification Number (UID)
- **Internal Diagnostic Modules**
  - Cyclic Redundancy Checker (CRC-16, CRC-32)
  - Integrated Temperature Sensor
  - Integrated BOR/POR Supply Monitors
- **Development Support**
  - JTAG (4-pin) and Serial Wire Debug (SWD) (2-pin)
  - Micro Trace Buffer (MTB)
  - Embedded Trace Macrocell (ETM) (TRACE_DATA[0:3])
    - Supports Serial Trace and Parallel Trace
- **Package Options**
  - 144-ball ZGA New Fine Pitch Ball Grid Array (NFBGA) (0.65mm pitch)
  - 128-pin PDT Thin Quad Flat Package (TQFP) (0.4mm pitch)
  - 100-pin PZ Low-profile Quad Flat Pack (LQFP) (0.5mm pitch)
  - 99-ball ZBP Die-Size Ball Grid Array (DSBGA) (0.5mm pitch)
  - 64-pin PM Low-profile Quad Flat Pack (LQFP) (0.5mm pitch)
  - 48-ball YAF Die-Size Ball Grid Array (WCSP) (0.5mm pitch)
- **Operating Characteristics**
  - Supply voltage: 3.3V
  - Ambient Temperature Range(T_A): –40°C up to 125°C

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2 Applications

- Humanoid robot
- Mobile robot
- Industrial and collaborative robot
- Single and multiaxis servo drives

3 Description

AM13E232x microcontrollers (MCUs) are part of the AM13E2x highly integrated, low-cost 32-bit MCU family based on the enhanced Arm®Cortex®-M33 32-bit core platform operating at up to 250MHz frequency. These cost-optimized MCUs offer high-performance analog, control, and digital peripheral integration, support ambient temperature ranges from -40°C to 125°C, and operate with a 3.3V supply voltage.

The AM13E232x MCUs provide up to 512KB of embedded flash program memory (2 banks of 256KB) with built-in error correction code (ECC) and up to 192 KB SRAM with hardware parity.

The core of the MCUs incorporate Custom Datapath Extension (CDE) support, a Memory Protection Unit (MPU), Micro Trace Buffer (MTB), a 32-bit Trigonometric Math Unit (TMU), and a Neural-network Processing Unit (NPU).

AM13E232x MCUs are enabled with robust, high-performance analog peripherals. Three 12-bit ADCs with a maximum sampling rate of 7.81MSPS at 250MHz, eight high speed comparators with built-in 12-bit reference DACs, and three programmable gain amplifiers provide optimal real-time signal chain performance.

These MCUs also offer intelligent digital peripherals such as two advanced control timers (one 16-bit, one 32-bit), one Windowed Watchdog Timer (WWDT), one Watchdog Timer (WDT), and a 12-channel Direct Memory Access (DMA) controller.

Complex real-time control applications are enabled with the MCUs' three MCPWM modules with 6 channels per module, 12 channels of ePWM with high resolution, three Enhanced Capture (ECAP) modules, and two Enganced Quadrature Encoder Pulse (EQEP) modules.

Data integrity and encryption features (AES, secure boot) provide security across the AM13E232x domains. A Cyclic Redundancy Checker (CRC) module provides internal diagnostics to the AM13E232x MCU.

Enhanced communication interfaces are supported through the two MCAN interface and two advanced UNICOMM peripherals. The four UNICOMM block offers configurations for up to four UART, four I^2C, or two SPI interfaces.

An EtherCAT SubDevice Controller is available on this device. The Fast Serial Interface (FSI) enables up to 200Mbps of robust communications across an isolation boundary.

The TI AM13E2x family of MCUs consists of devices with varying degrees of analog and digital integration that allow customers to find the MCU that meets project needs, with 3 device package options to choose from. The AM13E2x MCU platform combines the Arm®Cortex®-M33 platform with a holistic low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

Package Information

PART NUMBER[1]	PACKAGE[2]	PACKAGE SIZE[3]	BODY SIZE (NOM)	PITCH
AM13E232N91	BGA (NFBGA, 144)	TBD	TBD	0.65mm
	PDT (TQFP, 128)	16mm × 16mm	14mm × 14mm	0.4mm

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Package Information (continued)

PART NUMBER[1]	PACKAGE[2]	PACKAGE SIZE[3]	BODY SIZE (NOM)	PITCH
AM13E232191	BGA (NFBGA, 144)	TBD	TBD	0.65mm
	PDT (TQFP, 128)	16mm × 16mm	14mm × 14mm	0.4mm
	PZ (LQFP, 100)	16mm × 16mm	14mm × 14mm	0.5mm
	ZBP (NFBGA, 99)	5.2mm × 5.2mm	5.2mm × 5.2mm	0.5mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm	0.5mm
	YAF (DSBGA, 48)	3.65mm × 3.75mm	3.65mm × 3.75mm	0.5mm
AM13E232181	BGA (NFBGA, 144)	TBD	TBD	0.65mm
	PDT (TQFP, 128)	16mm × 16mm	14mm × 14mm	0.4mm
	PZ (LQFP, 100)	16mm × 16mm	14mm × 14mm	0.5mm
	ZBP (NFBGA, 99)	5.2mm × 5.2mm	5.2mm × 5.2mm	0.5mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm	0.5mm
	YAF (DSBGA, 48)	3.65mm × 3.75mm	3.65mm × 3.75mm	0.5mm
AM13E232192	BGA (NFBGA, 144)	TBD	TBD	0.65mm
	PDT (TQFP, 128)	16mm × 16mm	14mm × 14mm	0.4mm
	PZ (LQFP, 100)	16mm × 16mm	14mm × 14mm	0.5mm
	ZBP (NFBGA, 99)	5.2mm × 5.2mm	5.2mm × 5.2mm	0.5mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm	0.5mm
	YAF (DSBGA, 48)	3.65mm × 3.75mm	3.65mm × 3.75mm	0.5mm
AM13E232182	BGA (NFBGA, 144)	TBD	TBD	0.65mm
	PDT (TQFP, 128)	16mm × 16mm	14mm × 14mm	0.4mm
	PZ (LQFP, 100)	16mm × 16mm	14mm × 14mm	0.5mm
	ZBP (NFBGA, 99)	5.2mm × 5.2mm	5.2mm × 5.2mm	0.5mm
	PM (LQFP, 64)	12mm × 12mm	10mm × 10mm	0.5mm
	YAF (DSBGA, 48)	3.65mm × 3.75mm	3.65mm × 3.75mm	0.5mm

1. For orderable part number see the Mechanical, Packaging, and Orderable Information section.
2. For more information, see the Mechanical, Packaging, and Orderable Information section.
3. The package size (length × width) is a nominal value and includes pins, where applicable.

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3.1 Functional Block Diagram

Figure 3-1 shows the AM13E2x functional block diagram.

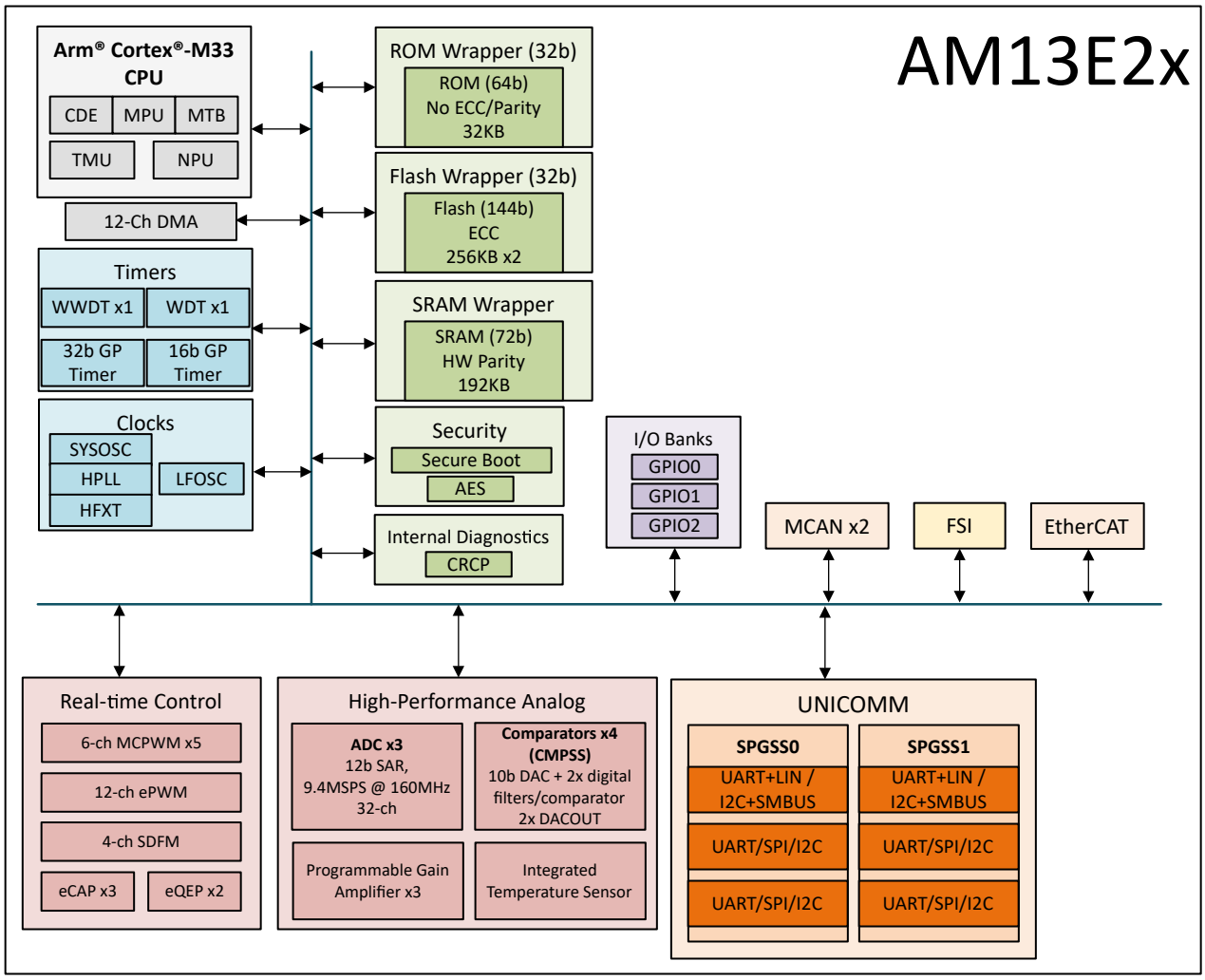


Figure 3-1. AM13E2x Functional Block Diagram

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4 Device Comparison

Table 4-1 lists the features of the AM13E232x microcontrollers.

Table 4-1. Device Comparison

Feature[1]		AM13E232N91	AM13E232191	AM13E232192	AM13E232181	AM13E232182
PROCESSOR AND ACCELERATORS						
Arm®Cortex®-M33	Frequency (MHz)[2]	250 MHz				
	Custom Datapath Extension (CDE)	Yes				
	Memory Protection Unit (MPU)	Yes				
	Micro Trace Buffer (MTB)	Yes				
	Trigonometric Math Unit (TMU)	Yes				
Neural-network Processing Unit (NPU)		Yes	Yes	No	Yes	No
MEMORY						
Flash (with Error Correction Code)		512KB			256KB	
SRAM (with HW Parity)		192KB				
Security: JTAGLOCK, Secure Boot		Yes				
Cyclic Redundancy Checker (CRC-16, CRC-32)		Yes				
SYSTEM						
12-Channel Data Movement Architecture (DMA) Controller		1				
16-bit General-Purpose Timer		1				
32-bit General-Purpose Timer		1				
Windowed Watchdog Timer (WWDT)		1				
Watchdog Timer (WDT)		1				
Internal 4MHz / 32MHz Oscillator (SYSOSC)		1				
Phase-Locked Loop up to 200MHz		1				
Internal 32KHz Oscillator (LFOSC)		1				
Crystal Oscillator (HFXT) / External Clock (HFCLK) input		1				
Internal 3.3V to 1.35V LDO (MLDO)		Yes				
GPIO		Up to 116 (package-dependent)				
ANALOG PERIPHERALS						
Analog to Digital Converter (ADC)	Number of ADCs	3				
	Bits	12-bit ADC				
	ADC channels	Up to 32 channels				
Temperature sensor		1				
Programmable Gain Amplifier (PGA) with Analog Input Mux		3				
Comparator Subsystem	CMPSS_LITE (each includes 8-bit DAC + 2 digital filters)	4				
	DAC Output	2				
CONTROL PERIPHERALS						
MCPWM		3 (6-ch)				
ePWM/HRPWM - Type 4		12-ch	12-ch	N/A	12-ch	N/A
ECAP		2				
EQEP		3				

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Table 4-1. Device Comparison (continued)

Feature[1]			AM13E232N91	AM13E232191	AM13E232192	AM13E232181	AM13E232182
SDFM			1 (4-ch)	1 (4-ch)	N/A	1 (4-ch)	N/A
COMMUNICATION PERIPHERALS							
UNICOMM	SPGS S0	UART	Up to 3 (2 UART, 1 UART+LIN)				
		I2C	Up to 3 (2 I2C, 1 I2C+SMBUS)				
		SPI	Up to 2				
	SPGS S1	UART	Up to 3 (2 UART, 1 UART+LIN)				
		I2C	Up to 3 (2 I2C, 1 I2C+SMBUS)				
		SPI	Up to 2				
MCAN (CAN-FD)			2				
FSI			1 TX, 1RX				
EtherCAT[3]			1	N/A			
PACKAGE, TEMPERATURE, AND QUALIFICATION OPTIONS							
Junction temperature (T_J)			–40°C to 140°C				
Ambient Temperature (T_A)			–40°C to 125°C				

1. A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. For more information, see the *AM13E232x Microcontrollers Technical Reference Manual.*.
2. The maximum CPU clock frequency can be up to 250MHz.
3. The EtherCAT module only supports 200MHz, not 250MHz CPU clock frequency.

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5 Terminal Configuration and Functions

5.1 Pin Diagram

Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

The diagrams in this section are used in conjunction with the other Terminal Configuration and Functions tables to locate signal names and ball grid numbers. The HTML version of this document provides additional information when hovering your cursor over a ball. For full pin configuration and functions for each package option, refer to *Pin Attributes* and *Signal Descriptions* sections.

5.1.1 AM13E232x Pin Diagrams

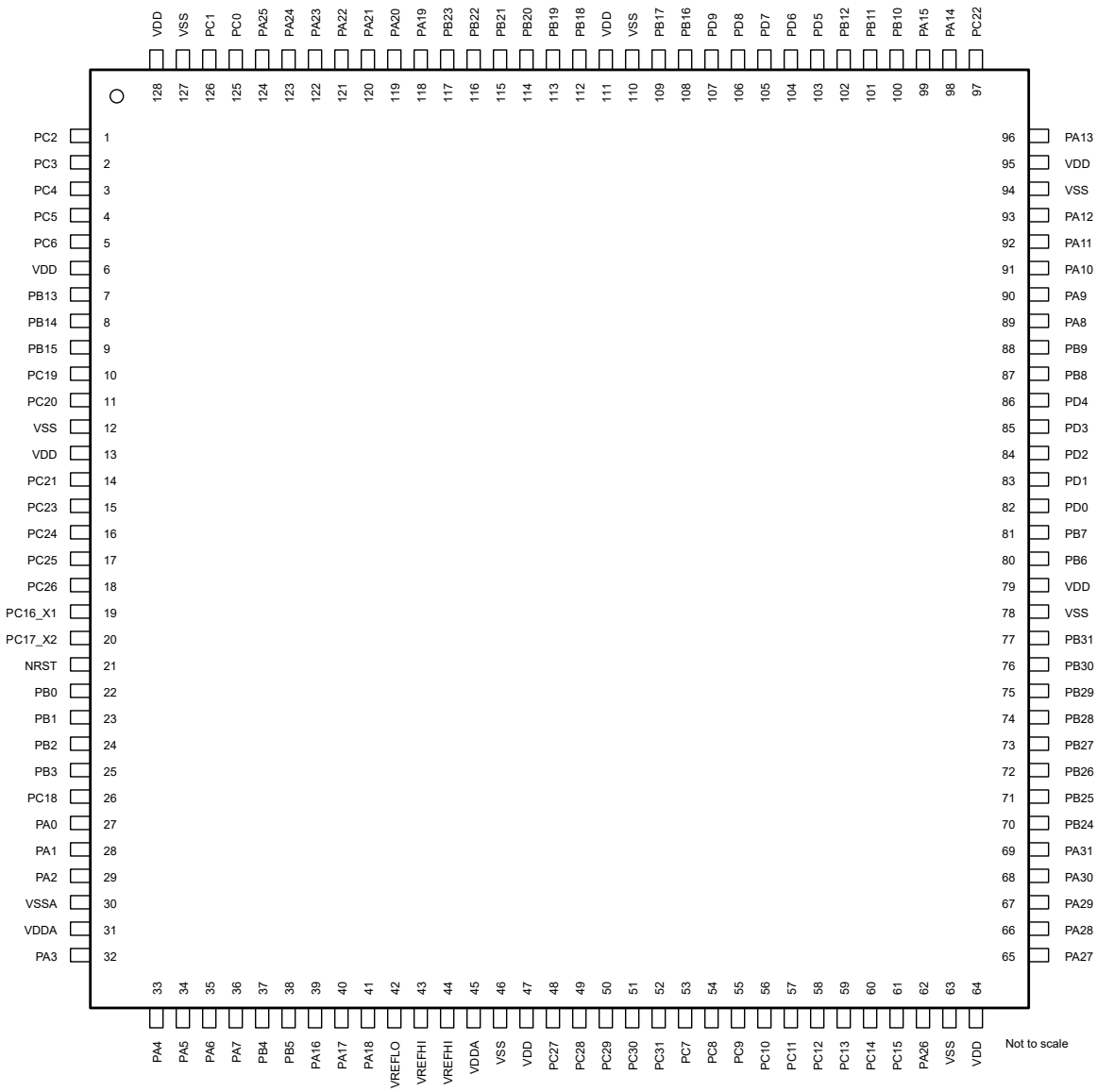


Figure 5-1. LQFP128 (PDT) Package

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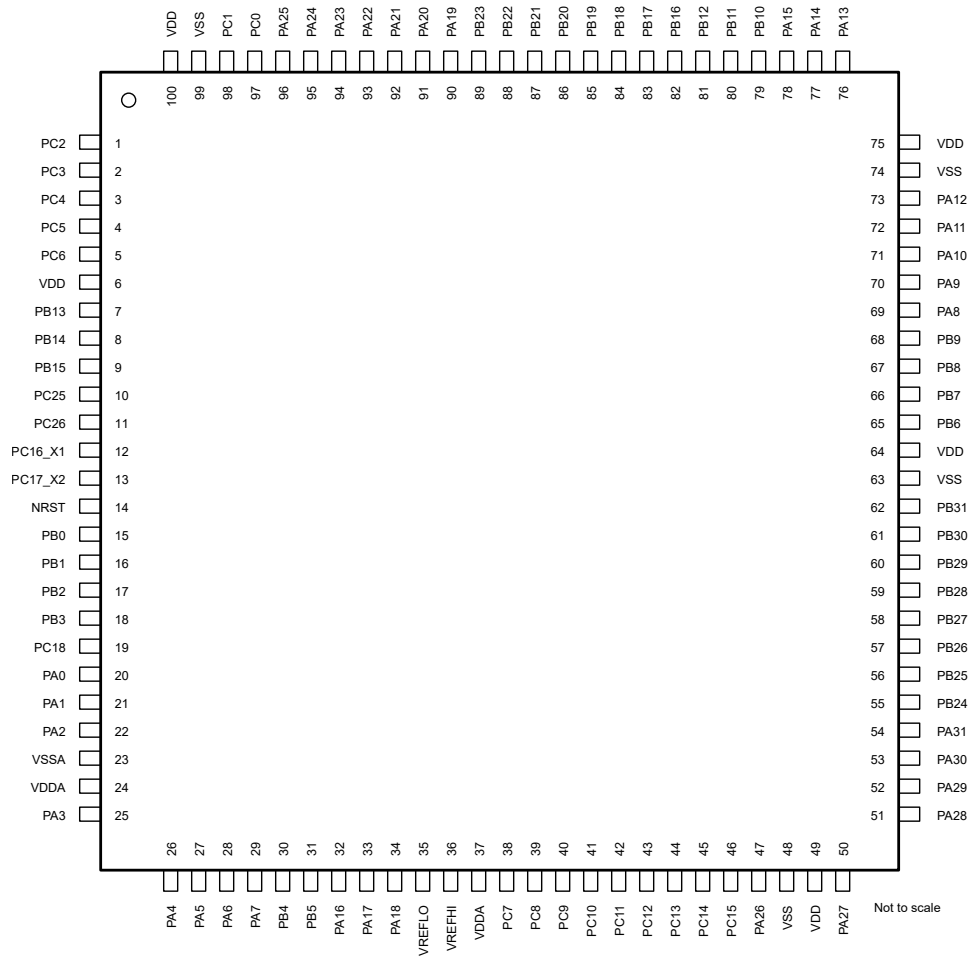


Figure 5-2. LQFP100_G (PZ) Package

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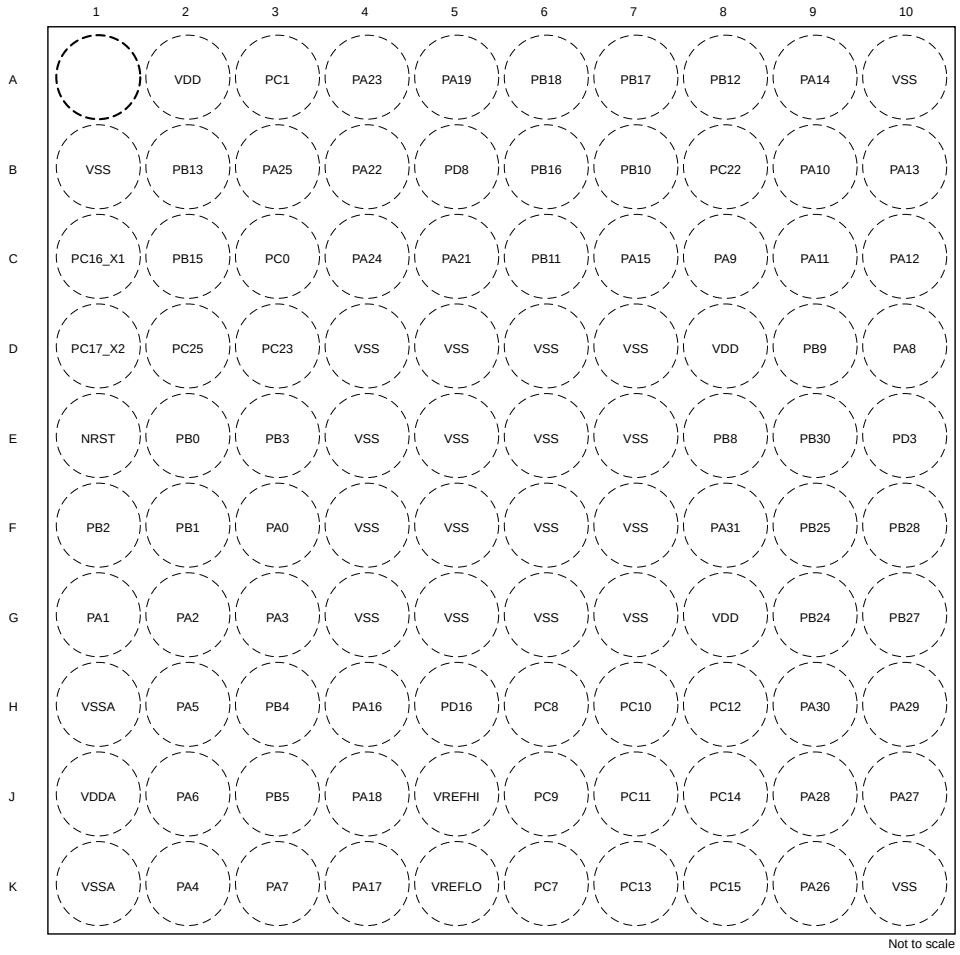


Figure 5-3. BGA99 Package

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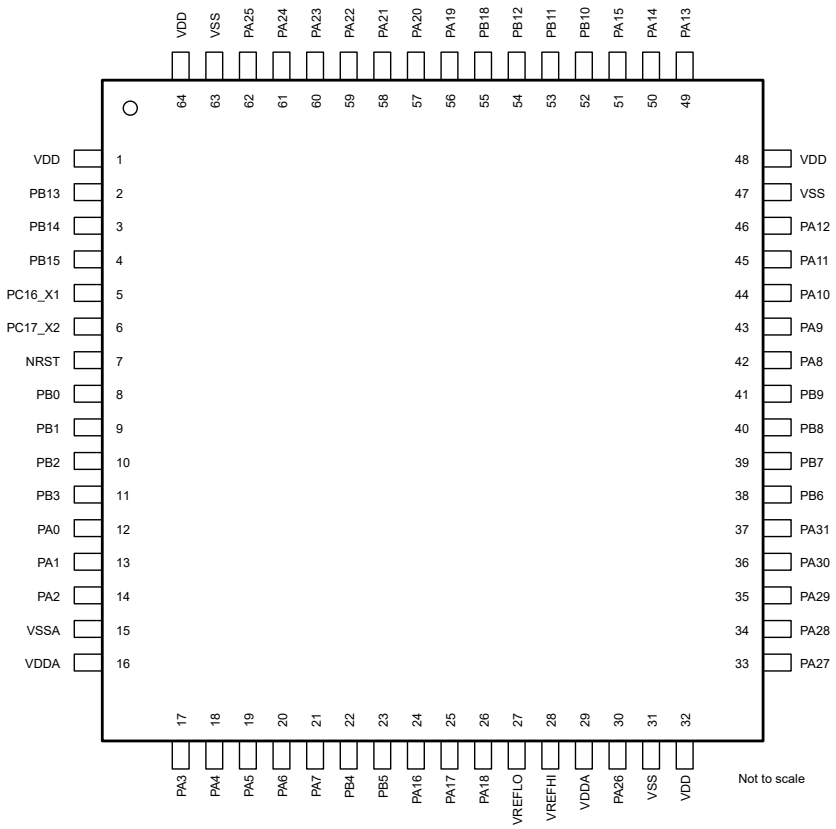


Figure 5-4. LQFP64_G (PM) Package

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5.2 Pin Attributes

5.2.1 Pin Attributes Header List

The following list describes the contents of each column in the *Pin Attributes* table:

1. **Ball Number:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **Ball Name:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **Signal Name:** Signal name of all dedicated and pin multiplexed signal functions associated with a ball.

Note

The *Pin Attributes* table, defines the SoC pin multiplexed signal function implemented at the pin and **does not** define secondary multiplexing of signal functions implemented in device subsystems. Secondary multiplexing of signal functions are not described in this table. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

4. **Mux Mode:** The MUXMODE value associated with each pin multiplexed signal function:
   - MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.
   - MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only defined valid values of MUXMODE can be used.
   - An empty box or "-" means Not Applicable.

Note

- The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when PORz is deasserted.
- Configuring two pins to the same pin multiplexed signal function can yield unexpected results and is not supported. This can be prevented with proper software configuration.
- Configuring a pad to an undefined multiplexing mode results in undefined behavior and must be avoided.

5. **Pad Configuration Register Name:** This is the name of the device pad/pin configuration register.
6. **Pad Configuration Register Address:** This is the memory address of the device pad/pin configuration register.
7. **Pad Configuration Register Default Value**: This is the default value of the register device pad/pin configuration register after PORz is deasserted.

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
21	E1	14	7	B2	NRST IOMUX_NRST 0x400C_C2A8	NRST	NRST	0	RST
							SYSCTL	1	IO
27	F3	20	12	C2	PA0 IOMUX_PA0 0x400C_C100	SDL	ANALOG_AIN6	A	A
							A0_1	AMUX0	A
							Disconnected	0	NA
							GPIO00	1	IO
							A1_1	AMUX1	A
							EPWM3_1A	2	O
							CMP0_HN0	AMUX2	A
							CMP2_HP0_LP0	AMUX3	A
							EPWM0_1A	3	O
							TIMG12_0_CCP0	4	IO
							TIMG4_0_CCP0	5	IO
							UC5_RX_SCL	6	IO
							UC4_TX_SDA_PICO	7	O
							UC1_CTS_CS0	8	IO
							UC1_TX_SDA_PICO	9	O
							EPWM4_1A	10	O
							UC2_RX_SCL	11	IO
							UC0_CTS_CS0	13	IO
							ESC_LED_LINK1_ACTIVE	14	IO
							MCAN1_RX	15	IO
							OUTPUTXBAR8	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
28	G1	21	13	D2	PA1 IOMUX_PA1 0x400C_C104	SDW	ANALOG_AIN7	A	A
							A0_2	AMUX0	A
							Disconnected	0	NA
							GPIO01	1	IO
							A1_2	AMUX1	A
							EPWM3_1B	2	O
							CMP0_HP1_LP1	AMUX2	A
							PGA0_P1	AMUX3	A
							EPWM1_1A	3	O
							PGA1_M0	AMUX4	A
							TIMG12_0_CCP1	4	IO
							PGA2_P2	AMUX5	A
							TIMG4_0_CCP1	5	IO
							UC5_TX_SDA	6	O
							UC4_RX_SCL_SCLK	7	IO
							UC1_RTS_POCI	8	O
							UC1_RX_SCL_SCLK	9	IO
							EPWM0_1B	10	O
							UC2_TX_SDA	11	O
							EPWM4_1B	12	O
							UC0_RTS_POCI	13	O
							ESC_RX0_CLK	14	I
							MCAN1_TX	15	IO
							OUTPUTXBAR4	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
29	G2	22	14	D3	PA2 IOMUX_PA2 0x400C_C108	LB	A0_3	AMUX0	A
							Disconnected	0	NA
							ANALOG_AIN8	A	A
							A2_25	AMUX1	A
							GPIO02	1	IO
							EPWM4_1A	2	O
							CMP1_HN0	AMUX2	A
							EPWM0_1B	3	O
							PGA0_OUT	AMUX3	A
							EPWM2_1A	4	O
							EPWM5_1A	5	O
							EPWM4_1B	6	O
							UC1_TX_SDA_PICO	8	O
							EPWM0_1A	10	O
							UC0_TX_SDA_PICO	13	O
							ESC_RX0_DV	14	I
							OUTPUTXBAR5	16	O
32	G3	25	17	E1	PA3 IOMUX_PA3 0x400C_C10C	NRST	Disconnected	0	NA
							A0_4	AMUX0	A
							ANALOG_AIN9	A	A
							A2_21	AMUX1	A
							GPIO03	1	IO
							CMP1_HP0_LP0	AMUX2	A
							SYSCTL_HFCLKIN	2	A
							EPWM1_1B	3	O
							PGA0_M0	AMUX3	A
							PGA0_P2	AMUX4	A
							TIMG4_0_CCP0	4	IO
							TIMG12_0_CCP0	5	IO
							PGA2_M0	AMUX5	A
							EPWM2_1B	6	O
							EPWM4_1B	7	O
							UC1_RX_SCL_SCLK	8	IO
							EPWM1_1A	10	O
							UC0_RX_SCL_SCLK	13	IO
							ESC_RX0_ERR	14	I
							OUTPUTXBAR6	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
33	K2	26	18	E3	PA4 IOMUX_PA4 0x400C_C110	PWR	Disconnected	0	NA
							A1_17	AMUX0	A
							ANALOG_AIN10	A	A
							A2_18	AMUX1	A
							GPIO04	1	IO
							CMP2_DACL	AMUX2	A
							SYSCTL_XCLKOUT	2	O
							EPWM5_1B	3	O
							CMP0_HN1	AMUX3	A
							INTERNAL_TESTANA0	AMUX4	Internal/A
							TIMG4_0_CCP1	4	IO
							TIMG12_0_CCP1	5	IO
							UC0_RTS_POCI	6	O
							UC2_RTS	7	O
							FSIRX0_D0	8	I
							UC3_RTS_POCI	9	O
							SD0_C2	10	IO
							UC5_RTS	11	O
							ESC_RX0_DATA0	14	I
							OUTPUTXBAR6	16	O
34	H2	27	19	E5	PA5 IOMUX_PA5 0x400C_C114	FLT	Disconnected	0	NA
							A1_13	AMUX0	A
							ANALOG_AIN11	A	A
							A2_19	AMUX1	A
							GPIO05	1	IO
							CMP1_HN1	AMUX2	A
							EPWM3_1A	2	O
							MCPWM2_1B	3	O
							PGA1_M1	AMUX3	A
							INTERNAL_TESTANA1	AMUX4	Internal/A
							EPWM0_1B	4	O
							UC0_RX_SCL_SCLK	6	IO
							FSIRX0_D1	8	I
							UC3_RX_SCL_SCLK	9	IO
							SD0_D2	10	IO
							MCAN0_RX	11	IO
							ESC_RX0_DATA1	14	I
							OUTPUTXBAR7	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
35	J2	28	20	F2	PA6 IOMUX_PA6 0x400C_C118	VREF/FLT	ANALOG_AIN12	A	A
							Disconnected	0	NA
							A0_17	AMUX0	A
							GPIO06	1	IO
							A1_3	AMUX1	A
							A2_26	AMUX2	A
							EPWM0_1A	2	O
							CMP3_DACL	AMUX3	A
							EPWM2_1A	3	O
							EPWM4_1A	4	O
							PGA1_OUT	AMUX4	A
							ADCCAL_ADCINCAL0	AMUX5	A
							UC0_CTS_CS0	6	IO
							FSIRX0_CLK	8	I
							UC3_CTS_CS0	9	IO
							UC3_RTS_POCI	11	O
							UC0_RTS_POCI	13	O
							ESC_RX0_DATA2	14	I
							OUTPUTXBAR8	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
36	K3	29	21	E4	PA7 IOMUX_PA7 0x400C_C11C	GND	ANALOG_AIN13	A	A
							Disconnected	0	NA
							A1_4	AMUX0	A
							GPIO07	1	IO
							A2_22	AMUX1	A
							CMP1_HP1_LP1	AMUX2	A
							EPWM2_1A	2	O
							PGA0_P3	AMUX3	A
							EPWM2_1B	3	O
							EPWM3_1A	4	O
							PGA1_P1	AMUX4	A
							MCPWM1_1B	5	O
							UC0_TX_SDA_PICO	6	O
							MCPWM0_1B	7	O
							EPWM3_1B	8	O
							UC3_TX_SDA_PICO	9	O
							EPWM5_1A	10	O
							EPWM4_1B	11	O
							ESC_RX0_DATA3	14	I
							OUTPUTXBAR1	16	O
89	D10	69	42	D7	PA8 IOMUX_PA8 0x400C_C120	NA	ANALOG_AIN42	A	A
							Disconnected	0	NA
							A1_18	AMUX0	A
							GPIO08	1	IO
							SD0_C2	2	IO
							UC0_RX_SCL_SCLK	3	IO
							SD0_D4	4	IO
							UC1_TX_SDA_PICO	5	O
							EPWM3_1A	6	O
							MCPWM0_1A	7	O
							UC3_RX_SCL_SCLK	9	IO
							UC4_TX_SDA_PICO	10	O
							MCAN0_TX	12	O
							ESC_I2C_SDA	13	IO
							EPWM0_1A	14	O
							EPWM4_1A	15	O
							OUTPUTXBAR3	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
90	C8	70	43	C7	PA9 IOMUX_PA9 0x400C_C124	SDL	ANALOG_AIN43	A	A
							Disconnected	0	NA
							A1_19	AMUX0	A
							GPIO09	1	IO
							SD0_D2	2	IO
							SD0_C1	3	IO
							SD0_C4	4	IO
							UC1_RX_SCL_SCLK	5	IO
							UC4_RX_SCL_SCLK	6	IO
							MCPWM0_2A	7	O
							UC0_TX_SDA_PICO	8	O
							UC5_RTS	9	O
							UC4_TX_SDA_PICO	10	O
							EPWM4_1A	11	O
							UC2_RTS	12	O
							EPWM2_1A	13	O
							EPWM0_1B	14	O
							EPWM4_1B	15	O
							OUTPUTXBAR4	16	O
91	B9	71	44	D6	PA10 IOMUX_PA10 0x400C_C128	HS	Disconnected	0	NA
							GPIO10	1	IO
							FSIRX0_D1	2	I
							SD0_D1	3	IO
							EPWM5_1A	4	O
							UC4_TX_SDA_PICO	5	O
							UC1_TX_SDA_PICO	6	O
							MCPWM0_3A	7	O
							UC0_RX_SCL_SCLK	8	IO
							UC5_RX_SCL	9	IO
							UC4_RX_SCL_SCLK	10	IO
							EPWM4_1B	11	O
							UC2_RX_SCL	12	IO
							EPWM2_1B	13	O
							EPWM1_1A	14	O
							ESC_PHY_RESETn	15	IO
							OUTPUTXBAR8	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
92	C9	72	45	C6	PA11 IOMUX_PA11 0x400C_C12C	SDL	Disconnected	0	NA
							GPIO11	1	IO
							EPWM4_1A	2	O
							UC3_CTS_CS0	3	IO
							UC2_TX_SDA	4	O
							UC4_CTS_CS0	5	IO
							UC1_CTS_CS0	6	IO
							MCPWM0_1B	7	O
							UC0_CTS_CS0	8	IO
							UC5_TX_SDA	9	O
							MCAN0_RX	10	I
							MCPWM2_2A	11	O
							MCPWM0_1A	12	O
							EPWM3_1B	13	O
							EPWM1_1B	14	O
							EPWM3_1A	15	O
							OUTPUTXBAR5	16	O
93	C10	73	46	B7	PA12 IOMUX_PA12 0x400C_C130	PWR	Disconnected	0	NA
							GPIO12	1	IO
							EPWM0_1A	2	O
							EPWM4_1A	3	O
							EPWM1_1B	6	O
							MCPWM0_2B	7	O
							UC0_RTS_POCI	8	O
							UC3_RTS_POCI	9	O
							MCAN0_TX	10	O
							MCPWM2_2B	11	O
							MCPWM0_1B	12	O
							EPWM4_1B	13	O
							EPWM2_1B	14	O
							EPWM3_1B	15	O
							OUTPUTXBAR6	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
96	B10	76	49	B6	PA13 IOMUX_PA13 0x400C_C134	PWR	Disconnected	0	NA
							GPIO13	1	IO
							DEBUG_TMS_SWDIO	2	IO
							EPWM0_1B	3	O
							EPWM4_1B	4	O
							UC0_RX_SCL_SCLK	5	IO
							UC3_RX_SCL_SCLK	6	IO
							UC0_CTS_CS0	8	IO
							SYSCTL_FCC_IN	9	I
							UC3_CTS_CS0	10	IO
							MCPWM2_3A	11	O
							EPWM2_1A	12	O
							EPWM5_1A	13	O
							OUTPUTXBAR7	16	O
98	A9	77	50	B5	PA14 IOMUX_PA14 0x400C_C138	GND	Disconnected	0	NA
							GPIO14	1	IO
							DEBUG_JTCK_SWCLK	2	IO
							UC0_TX_SDA_PICO	5	O
							MCPWM1_2A	6	O
							EPWM2_1A	7	O
							UC1_TX_SDA_PICO	8	O
							UC2_CTS	9	O
							UC5_CTS	10	O
							ESC_TX0_DATA3	14	O
							OUTPUTXBAR8	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
99	C7	78	51	A5	PA15 IOMUX_PA15 0x400C_C13C	LB	Disconnected	0	NA
							GPIO15	1	IO
							DEBUG_JTDI	2	I
							EPWM0_1A	3	O
							MCPWM1_1A	4	O
							UC0_RX_SCL_SCLK	5	IO
							UC0_RTS_POCI	6	O
							UC3_RTS_POCI	7	O
							UC1_RX_SCL_SCLK	8	IO
							UC2_RTS	9	O
							UC5_RTS	10	O
							EPWM4_1A	11	O
							MCAN0_RX	12	I
							ESC_TX1_ENA	14	O
							ESC_RX1_DATA1	15	I
							OUTPUTXBAR1	16	O
39	H4	32	24	G2	PA16 IOMUX_PA16 0x400C_C140	PWR	A0_15	AMUX0	A
							Disconnected	0	NA
							ANALOG_AIN16	A	A
							A2_12	AMUX1	A
							GPIO16	1	IO
							UC1_CTS_CS0	2	IO
							CMP3_HP1_LP1	AMUX2	A
							EPWM3_1A	3	O
							PGA1_P2	AMUX3	A
							PGA2_P3	AMUX4	A
							EPWM5_1B	4	O
							MCPWM1_2B	5	O
							EPWM4_1B	6	O
							MCPWM0_2B	7	O
							EPWM2_1B	8	O
							SYSCTL_FCC_IN	9	I
							ESC_TX0_DATA0	14	O
							OUTPUTXBAR1	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
40	K4	33	25	F3	PA17 IOMUX_PA17 0x400C_C144	PWR	ANALOG_AIN17	A	A
							Disconnected	0	NA
							A0_12	AMUX0	A
							GPIO17	1	IO
							A2_1	AMUX1	A
							CMP0_HP0_LP0	AMUX2	A
							UC1_RTS_POCI	2	IO
							PGA1_M3	AMUX3	A
							EPWM3_1B	3	O
							MCPWM2_1B	4	O
							PGA2_OUT	AMUX4	A
							MCPWM1_3B	5	O
							EPWM5_1B	6	O
							MCPWM0_3B	7	O
							EPWM0_1B	8	O
							UC3_RTS_POCI	11	O
							UC0_RTS_POCI	13	O
							ESC_TX0_DATA1	14	O
							OUTPUTXBAR2	16	O
41	J4	34	26	F4	PA18 IOMUX_PA18 0x400C_C148	SDL	A1_12	AMUX0	A
							ANALOG_AIN18	A	A
							Disconnected	0	NA
							GPIO18	1	IO
							CMP3_HN0_LN0	AMUX1	A
							PGA2_M1	AMUX2	A
							EPWM0_1A	3	O
							MCPWM2_1A	4	O
							EPWM4_1A	5	O
							ESC_LED_STATE_RUN	14	IO
							OUTPUTXBAR3	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
118	A5	90	56	C5	PA19 IOMUX_PA19 0x400C_C14C	SDL	Disconnected	0	NA
							GPIO19	1	IO
							DEBUG_JTDO_SWO	2	O
							EPWM3_1B	3	O
							EPWM4_1B	4	O
							MCPWM1_1B	5	O
							UC0_RX_SCL_SCLK	6	IO
							UC3_RX_SCL_SCLK	7	IO
							UC1_TX_SDA_PICO	8	O
							UC3_TX_SDA_PICO	9	O
							MCAN0_RX	12	I
							SD0_C4	14	IO
							MCAN1_RX	15	IO
							OUTPUTXBAR2	16	O
119		91	57	A4	PA20 IOMUX_PA20 0x400C_C150	SDL	Disconnected	0	NA
							GPIO20	1	IO
							EPWM4_1A	2	O
							EPWM0_1A	3	O
							EPWM5_1A	4	O
							MCPWM1_2B	5	O
							UC0_CTS_CS0	6	IO
							UC3_CTS_CS0	7	IO
							UC1_RX_SCL_SCLK	8	IO
							UC3_RTS_POCI	9	O
							UC4_RX_SCL_SCLK	10	IO
							UC0_RTS_POCI	11	O
							MCAN0_TX	12	O
							EPWM5_1B	13	O
							SD0_D4	14	IO
							MCAN1_TX	15	IO
							OUTPUTXBAR3	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
120	C5	92	58	D5	PA21 IOMUX_PA21 0x400C_C154	SDL	Disconnected	0	NA
							GPIO21	1	IO
							FSIRX0_D0	2	I
							EPWM5_1B	3	O
							MCPWM1_3B	4	O
							EPWM3_1B	5	O
							UC0_TX_SDA_PICO	6	O
							UC3_TX_SDA_PICO	7	O
							UC0_RX_SCL_SCLK	8	IO
							UC3_RX_SCL_SCLK	9	IO
							MCAN0_RX	10	I
							EPWM2_1A	11	O
							EPWM5_1A	12	O
							MCAN1_RX	13	IO
							UC0_CTS_CS0	14	IO
							UC3_CTS_CS0	15	IO
							OUTPUTXBAR4	16	O
121	B4	93	59	B4	PA22 IOMUX_PA22 0x400C_C158	SDL	Disconnected	0	NA
							GPIO22	1	IO
							EPWM0_1B	2	O
							MCPWM2_2A	3	O
							UC2_TX_SDA	4	O
							EPWM4_1B	5	O
							MCPWM1_1A	6	O
							UC5_TX_SDA	7	O
							UC0_TX_SDA_PICO	8	O
							UC3_TX_SDA_PICO	9	O
							MCAN0_TX	10	O
							EPWM2_1B	11	O
							EPWM5_1B	12	O
							MCAN1_TX	13	IO
							EPWM4_1A	14	O
							EPWM1_1A	15	O
							OUTPUTXBAR5	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
122	A4	94	60	D4	PA23 IOMUX_PA23 0x400C_C15C	SDL	Disconnected	0	NA
							GPIO23	1	IO
							EPWM2_1B	2	O
							MCPWM2_2B	3	O
							UC2_RX_SCL	4	IO
							UC0_TX_SDA_PICO	5	O
							EPWM5_1B	6	O
							UC5_RX_SCL	7	IO
							UC0_RX_SCL_SCLK	8	IO
							UC3_RX_SCL_SCLK	9	IO
							UC3_TX_SDA_PICO	10	O
							EPWM3_1B	11	O
							EPWM1_1B	12	O
							EPWM4_1B	13	O
							UC4_CTS_CS0	14	IO
							UC1_CTS_CS0	15	IO
							OUTPUTXBAR6	16	O
123	C4	95	61	A3	PA24 IOMUX_PA24 0x400C_C160	SDL	Disconnected	0	NA
							GPIO24	1	IO
							EPWM0_1A	2	O
							MCPWM2_3A	3	O
							EPWM4_1A	4	O
							UC0_RX_SCL_SCLK	5	IO
							UC3_RX_SCL_SCLK	6	IO
							EPWM2_1A	7	O
							UC0_TX_SDA_PICO	8	O
							UC3_TX_SDA_PICO	9	O
							MCAN0_RX	10	I
							MCPWM1_2A	11	O
							EPWM5_1A	12	O
							ESC_I2C_SCL	13	IO
							SD0_C3	15	IO
							OUTPUTXBAR7	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
124	B3	96	62	C4	PA25 IOMUX_PA25 0x400C_C164	SDL	Disconnected	0	NA
							GPIO25	1	IO
							EPWM2_1A	2	O
							MCPWM2_3B	3	O
							EPWM5_1A	4	O
							UC0_TX_SDA_PICO	5	O
							UC3_TX_SDA_PICO	6	O
							EPWM2_1B	7	O
							UC0_RX_SCL_SCLK	8	IO
							UC3_RX_SCL_SCLK	9	IO
							MCAN0_TX	10	O
							MCPWM1_3A	11	O
							EPWM5_1B	12	O
							MCPWM0_3B	13	O
							EPWM3_1A	14	O
							SD0_D3	15	IO
							OUTPUTXBAR7	16	O
62	K9	47	30	G5	PA26 IOMUX_PA26 0x400C_C168	PWR	ANALOG_AIN28	A	A
							A2_17	AMUX0	A
							Disconnected	0	NA
							GPIO26	1	IO
							CMP0_LN1	AMUX1	A
							EPWM4_1A	2	O
							PGA2_M2	AMUX2	A
							PGA0_M2	AMUX3	A
							TIMG4_0_CCP0	3	IO
							TIMG12_0_CCP0	4	IO
							EPWM2_1A	5	O
							EPWM5_1A	6	O
							UC0_RX_SCL_SCLK	8	IO
							UC0_TX_SDA_PICO	9	O
							UC3_TX_SDA_PICO	10	O
							UC3_RX_SCL_SCLK	11	IO
							ESC_GPI2	14	IO
							OUTPUTXBAR2	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
65	J10	50	33	F5	PA27 IOMUX_PA27 0x400C_C16C	PWR	ANALOG_AIN29	A	A
							A0_14	AMUX0	A
							Disconnected	0	NA
							GPIO27	1	IO
							A1_14	AMUX1	A
							EPWM4_1B	2	O
							CMP1_HP2_LP2	AMUX2	A
							PGA0_P4	AMUX3	A
							TIMG4_0_CCP1	3	IO
							TIMG12_0_CCP1	4	IO
							PGA2_P0	AMUX4	A
							EPWM2_1B	5	O
							SYSCTL_XCLKOUT	7	O
							UC0_RX_SCL_SCLK	8	IO
							UC0_TX_SDA_PICO	9	O
							UC3_TX_SDA_PICO	10	O
							UC3_RX_SCL_SCLK	11	IO
							UC2_RX_SCL	12	IO
							FSITX0_D0	13	IO
							OUTPUTXBAR3	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
66	J9	51	34	F6	PA28 IOMUX_PA28 0x400C_C170	VSS	Disconnected	0	NA
							A0_11	AMUX0	A
							ANALOG_AIN30	A	A
							A2_30	AMUX1	A
							GPIO28	1	IO
							CMP2_LN1	AMUX2	A
							TIMG12_0_CCP0	2	IO
							TIMG4_0_CCP0	3	IO
							PGA1_P3	AMUX3	A
							PGA0_P7	AMUX4	A
							MCAN0_RX	4	I
							UC1_RTS_POCI	6	O
							UC0_CTS_CS0	8	IO
							UC0_RTS_POCI	9	O
							UC4_RTS_POCI	10	O
							UC3_CTS_CS0	11	IO
							FSITX0_D1	13	IO
							EPWM2_1A	14	O
							EPWM3_1A	15	O
							OUTPUTXBAR4	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
67	H10	52	35	F7	PA29 IOMUX_PA29 0x400C_C174	GND	A2_5	AMUX0	A
							Disconnected	0	NA
							ANALOG_AIN31	A	A
							CMP0_HP2_LP2	AMUX1	A
							GPIO29	1	IO
							TIMG12_0_CCP1	2	IO
							PGA0_P5	AMUX2	A
							TIMG4_0_CCP1	3	IO
							PGA1_P4	AMUX3	A
							PGA2_P4	AMUX4	A
							MCAN0_TX	4	O
							EPWM3_1B	6	O
							MCPWM0_1B	7	O
							SYSCTL_FCC_IN	8	I
							UC0_CTS_CS0	9	IO
							UC3_CTS_CS0	11	IO
							FSITX0_CLK	13	IO
							EPWM2_1B	14	O
							EPWM5_1B	15	O
							OUTPUTXBAR5	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
68	H9	53	36	E6	PA30 IOMUX_PA30 0x400C_C178	SDL	Disconnected	0	NA
							A0_5	AMUX0	A
							ANALOG_AIN32	A	A
							A2_27	AMUX1	A
							GPIO30	1	IO
							CMP2_HP3_LP3	AMUX2	A
							EPWM0_1A	2	O
							EPWM4_1A	3	O
							PGA1_P5	AMUX3	A
							PGA2_P5	AMUX4	A
							EPWM2_1B	4	O
							EPWM4_1B	5	O
							UC1_TX_SDA_PICO	6	O
							MCPWM0_2B	7	O
							UC0_RTS_POCI	8	O
							UC4_RTS_POCI	10	O
							UC4_TX_SDA_PICO	11	O
							ESC_TX0_DATA2	13	O
							EPWM3_1A	14	O
							SD0_D3	15	IO
							OUTPUTXBAR6	16	O
69	F8	54	37	E7	PA31 IOMUX_PA31 0x400C_C17C	SDL	ANALOG_AIN33	A	A
							A1_15	AMUX0	A
							Disconnected	0	NA
							GPIO31	1	IO
							A2_28	AMUX1	A
							EPWM1_1A	2	O
							CMP1_LN1	AMUX2	A
							PGA2_M3	AMUX3	A
							EPWM0_1B	3	O
							EPWM5_1B	4	O
							MCPWM0_3B	5	O
							UC1_CTS_CS0	6	IO
							EPWM4_1B	7	O
							UC4_CTS_CS0	11	IO
							EPWM3_1B	14	O
							SD0_C3	15	IO
							OUTPUTXBAR2	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
22	E2	15	8		PB0 IOMUX_PB0 0x400C_C180	SDL	ANALOG_AIN2	A	A
							A0_6	AMUX0	A
							Disconnected	0	NA
							A1_6	AMUX1	A
							GPIO32	1	IO
							CMP2_HN1	AMUX2	A
							MCPWM0_1A	3	O
							EPWM3_1A	4	O
							UC0_RX_SCL_SCLK	9	IO
							UC3_RX_SCL_SCLK	11	IO
							ESC_I2C_SCL	12	IO
							ESC_RX1_DATA3	14	I
							OUTPUTXBAR5	16	O
23	F2	16	9		PB1 IOMUX_PB1 0x400C_C184	SDL	A0_7	AMUX0	A
							ANALOG_AIN3	A	A
							Disconnected	0	NA
							A1_7	AMUX1	A
							GPIO33	1	IO
							CMP2_HP1_LP1	AMUX2	A
							MCPWM0_2A	3	O
							EPWM4_1A	4	O
							EPWM2_1A	5	O
							UC0_TX_SDA_PICO	9	O
							UC3_TX_SDA_PICO	11	O
							ESC_I2C_SDA	12	IO
							ESC_PHY_RESETn	14	IO
							OUTPUTXBAR6	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
24	F1	17	10		PB2 IOMUX_PB2 0x400C_C188	SDL	A0_8	AMUX0	A
							ANALOG_AIN4	A	A
							Disconnected	0	NA
							GPIO34	1	IO
							A1_8	AMUX1	A
							MCPWM0_3A	3	O
							EPWM5_1A	4	O
							EPWM4_1A	6	O
							MCPWM2_2A	7	O
							EPWM1_1A	8	O
							MCAN1_RX	11	IO
							ESC_PHY_CLK	13	IO
							ESC_LED_RUN	14	IO
							OUTPUTXBAR7	16	O
25	E3	18	11		PB3 IOMUX_PB3 0x400C_C18C	SDL	A0_9	AMUX0	A
							ANALOG_AIN5	A	A
							Disconnected	0	NA
							GPIO35	1	IO
							A1_9	AMUX1	A
							PGA2_P1	AMUX2	A
							MCPWM0_1A	3	O
							PGA0_P0	AMUX3	A
							PGA1_P0	AMUX4	A
							EPWM3_1A	4	O
							MCAN1_TX	11	IO
							ESC_LED_ERR	14	IO
							OUTPUTXBAR8	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
37	H3	30	22		PB4 IOMUX_PB4 0x400C_C190	SDL	ANALOG_AIN14	A	A
							A1_5	AMUX0	A
							Disconnected	0	NA
							GPIO36	1	IO
							A2_23	AMUX1	A
							UC1_RX_SCL_SCLK	5	IO
							UC0_TX_SDA_PICO	8	O
							UC3_TX_SDA_PICO	9	O
							MCAN0_RX	10	I
							UC4_RX_SCL_SCLK	11	IO
							ESC_TX0_ENA	14	O
							OUTPUTXBAR2	16	O
38	J3	31	23		PB5 IOMUX_PB5 0x400C_C194	SDL	Disconnected	0	NA
							ANALOG_AIN15	A	A
							A1_11	AMUX0	A
							A2_24	AMUX1	A
							GPIO37	1	IO
							PGA0_M1	AMUX2	A
							PGA1_M2	AMUX3	A
							EPWM3_1B	6	O
							MCPWM0_1B	7	O
							UC0_RX_SCL_SCLK	8	IO
							UC3_RX_SCL_SCLK	9	IO
							MCAN0_TX	10	O
							ESC_TX0_CLK	14	O
							OUTPUTXBAR3	16	O
80		65	38		PB6 IOMUX_PB6 0x400C_C198	SDL	Disconnected	0	NA
							GPIO38	1	IO
							EPWM2_1A	3	O
							MCPWM1_1A	5	O
							EPWM4_1A	6	O
							UC5_RX_SCL	8	IO
							UC2_RX_SCL	9	IO
							EPWM5_1A	14	O
							ESC_I2C_SDA	15	IO
							OUTPUTXBAR3	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
81		66	39		PB7 IOMUX_PB7 0x400C_C19C	SDL	Disconnected	0	NA
							GPIO39	1	IO
							EPWM2_1B	3	O
							EPWM5_1A	4	O
							MCPWM1_2A	5	O
							UC5_TX_SDA	8	O
							UC2_TX_SDA	9	O
							EPWM5_1B	14	O
							ESC_I2C_SCL	15	IO
							OUTPUTXBAR4	16	O
87	E8	67	40		PB8 IOMUX_PB8 0x400C_C1A0	SDL	Disconnected	0	NA
							GPIO40	1	IO
							TRACE_DATA1	2	O
							EPWM0_1A	3	O
							EPWM4_1A	4	O
							MCPWM1_3A	5	O
							UC2_CTS	6	O
							MCPWM2_3A	7	O
							EPWM2_1A	8	O
							UC0_RX_SCL_SCLK	9	IO
							UC3_RX_SCL_SCLK	10	IO
							UC5_RTS	11	O
							FSIRX0_D1	12	I
							EPWM5_1A	13	O
							EPWM5_1B	14	O
							EPWM2_1B	15	O
							OUTPUTXBAR2	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
88	D9	68	41		PB9 IOMUX_PB9 0x400C_C1A4	SDL	Disconnected	0	NA
							GPIO41	1	IO
							EPWM0_1B	3	O
							EPWM4_1B	4	O
							MCPWM1_1A	5	O
							UC2_RTS	6	O
							EPWM4_1A	7	O
							EPWM2_1B	8	O
							UC0_TX_SDA_PICO	9	O
							UC3_TX_SDA_PICO	10	O
							UC5_CTS	11	O
							FSIRX0_CLK	12	I
							ESC_LATCH0	14	IO
							OUTPUTXBAR3	16	O
100	B7	79	52		PB10 IOMUX_PB10 0x400C_C1A8	SDL	Disconnected	0	NA
							GPIO42	1	IO
							UC5_TX_SDA	4	O
							MCPWM1_1B	5	O
							UC2_TX_SDA	6	O
							UC3_RX_SCL_SCLK	7	IO
							UC0_TX_SDA_PICO	8	O
							UC0_RX_SCL_SCLK	9	IO
							UC3_TX_SDA_PICO	10	O
							EPWM1_1B	11	O
							ESC_LED_LINK0_ACTIVE	12	IO
							ESC_TX0_DATA3	13	O
							ESC_TX1_CLK	14	O
							ESC_RX1_DATA2	15	I
							OUTPUTXBAR2	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
101	C6	80	53		PB11 IOMUX_PB11 0x400C_C1AC	SDL	Disconnected	0	NA
							GPIO43	1	IO
							TRACE_CLK	2	IO
							UC5_RX_SCL	4	IO
							MCPWM1_2B	5	O
							UC2_RX_SCL	6	IO
							UC3_CTS_CS0	7	IO
							UC0_RX_SCL_SCLK	8	IO
							UC0_TX_SDA_PICO	9	O
							UC0_CTS_CS0	10	IO
							UC3_RX_SCL_SCLK	11	IO
							SD0_C1	12	IO
							UC3_TX_SDA_PICO	13	O
							ESC_LATCH0	14	IO
							ESC_MDIO_DATA	15	IO
							OUTPUTXBAR3	16	O
102	A8	81	54		PB12 IOMUX_PB12 0x400C_C1B0	SDL	Disconnected	0	NA
							GPIO44	1	IO
							TRACE_DATA3	2	O
							EPWM0_1B	3	O
							EPWM4_1B	4	O
							MCPWM1_3B	5	O
							UC3_TX_SDA_PICO	6	O
							UC3_RX_SCL_SCLK	7	IO
							UC0_RX_SCL_SCLK	8	IO
							EPWM3_1B	9	O
							ESC_TX0_DATA2	10	O
							UC0_TX_SDA_PICO	11	O
							SD0_D1	12	IO
							ESC_TX0_DATA3	13	O
							ESC_RX1_DATA1	15	I
							OUTPUTXBAR4	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
7	B2	7	2	B3	PB13 IOMUX_PB13 0x400C_C1B4	SDL	Disconnected	0	NA
							GPIO45	1	IO
							SYSCTL_XCLKOUT	2	O
							UC1_RTS_POCI	3	IO
							MCPWM0_1B	5	O
							EPWM0_1B	6	O
							MCPWM1_1B	7	O
							SYSCTL_FCC_IN	8	I
							EPWM4_1B	9	O
							ESC_TX1_ENA	12	O
							ESC_TX1_DATA0	14	O
							FSITX0_D0	15	IO
							OUTPUTXBAR6	16	O
8		8	3	C3	PB14 IOMUX_PB14 0x400C_C1B8	SDL	Disconnected	0	NA
							GPIO46	1	IO
							SYSCTL_XCLKOUT	2	O
							UC0_TX_SDA_PICO	8	O
							MCAN0_RX	10	I
							UC3_TX_SDA_PICO	11	O
							ESC_RX1_ERR	12	I
							ESC_SYNC0	14	IO
							FSITX0_D1	15	IO
							OUTPUTXBAR1	16	O
9	C2	9	4	B1	PB15 IOMUX_PB15 0x400C_C1BC	SDL	Disconnected	0	NA
							GPIO47	1	IO
							UC0_RX_SCL_SCLK	8	IO
							MCAN0_TX	10	O
							UC3_RX_SCL_SCLK	11	IO
							ESC_RX1_CLK	12	I
							FSITX0_D1	13	IO
							ESC_SYNC1	14	IO
							FSITX0_CLK	15	IO
							OUTPUTXBAR2	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
108	B6	82			PB16 IOMUX_PB16 0x400C_C1C0	SDL	Disconnected	0	NA
							GPIO48	1	IO
							TRACE_DATA0	2	O
							UC5_TX_SDA	4	O
							MCPWM1_1B	7	O
							EPWM1_1B	8	O
							MCAN0_TX	10	O
							UC2_TX_SDA	11	O
							ESC_MDIO_CLK	12	IO
							MCAN1_RX	13	IO
							OUTPUTXBAR2	16	O
109	A7	83			PB17 IOMUX_PB17 0x400C_C1C4	SDL	Disconnected	0	NA
							GPIO49	1	IO
							UC5_RX_SCL	4	IO
							MCPWM1_1A	5	O
							EPWM1_1A	6	O
							MCAN0_RX	10	I
							UC2_RX_SCL	11	IO
							UC1_TX_SDA_PICO	12	IO
							MCAN1_TX	13	IO
							ESC_RX0_ERR	14	I
							ESC_TX0_ENA	15	O
							OUTPUTXBAR3	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
112	A6	84	55		PB18 IOMUX_PB18 0x400C_C1C8	SDL	Disconnected	0	NA
							GPIO50	1	IO
							TRACE_DATA2	2	O
							TRACE_DATA3	3	O
							UC5_CTS	4	O
							MCPWM1_3A	5	O
							UC3_RX_SCL_SCLK	6	IO
							UC3_TX_SDA_PICO	7	O
							UC0_RX_SCL_SCLK	8	IO
							UC0_TX_SDA_PICO	9	O
							ESC_RX0_CLK	10	I
							UC2_CTS	11	O
							UC1_RX_SCL_SCLK	12	IO
							ESC_TX0_CLK	13	I
							ESC_MDIO_CLK	14	IO
							SD0_C4	15	IO
							OUTPUTXBAR4	16	O
113		85			PB19 IOMUX_PB19 0x400C_C1CC	SDL	Disconnected	0	NA
							GPIO51	1	IO
							EPWM3_1A	3	O
							UC5_RTS	4	O
							UC1_CTS_CS0	8	IO
							UC4_CTS_CS0	10	IO
							UC2_RTS	11	O
							ESC_PDI_UC_IRQ	12	IO
							ESC_RX0_DV	13	I
							ESC_MDIO_DATA	14	IO
							SD0_D4	15	IO
							OUTPUTXBAR5	16	O
114		86			PB20 IOMUX_PB20 0x400C_C1D0	SDL	Disconnected	0	NA
							GPIO52	1	IO
							EPWM3_1B	3	O
							UC1_RTS_POCI	8	O
							UC4_RTS_POCI	10	O
							ESC_RX0_ERR	12	I
							ESC_RX0_DATA0	13	I
							ESC_PHY_CLK	14	IO
							OUTPUTXBAR6	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
115		87			PB21 IOMUX_PB21 0x400C_C1D4	SDL	Disconnected	0	NA
							GPIO53	1	IO
							UC1_TX_SDA_PICO	8	O
							UC4_TX_SDA_PICO	10	O
							ESC_RX0_CLK	12	I
							ESC_RX0_DATA1	13	I
							ESC_RX1_CLK	14	I
							OUTPUTXBAR7	16	O
116		88			PB22 IOMUX_PB22 0x400C_C1D8	SDL	Disconnected	0	NA
							GPIO54	1	IO
							SD0_C1	2	IO
							EPWM4_1B	3	O
							EPWM2_1B	4	O
							EPWM5_1B	5	O
							UC1_RX_SCL_SCLK	8	IO
							UC4_RX_SCL_SCLK	10	IO
							ESC_RX0_DV	12	I
							ESC_RX0_DATA2	13	I
							ESC_RX1_DV	14	I
							OUTPUTXBAR8	16	O
117		89			PB23 IOMUX_PB23 0x400C_C1DC	SDL	Disconnected	0	NA
							GPIO55	1	IO
							SD0_D1	2	IO
							EPWM4_1A	3	O
							EPWM2_1A	4	O
							EPWM5_1A	5	O
							ESC_RX0_DATA0	12	I
							ESC_RX0_DATA3	13	I
							OUTPUTXBAR1	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
70	G9	55			PB24 IOMUX_PB24 0x400C_C1E0	SDL	Disconnected	0	NA
							A0_21	AMUX0	A
							ANALOG_AIN34	A	A
							GPIO56	1	IO
							A1_21	AMUX1	A
							PGA0_M3	AMUX2	A
							UC5_RX_SCL	9	IO
							UC2_RX_SCL	11	IO
							ESC_TX1_DATA3	13	O
							ESC_GPO1	14	IO
							SD0_D1	15	IO
							OUTPUTXBAR3	16	O
71	F9	56			PB25 IOMUX_PB25 0x400C_C1E4	SDL	Disconnected	0	NA
							A0_22	AMUX0	A
							ANALOG_AIN35	A	A
							GPIO57	1	IO
							A1_22	AMUX1	A
							PGA1_P6	AMUX2	A
							PGA2_P7	AMUX3	A
							UC5_TX_SDA	9	O
							UC2_TX_SDA	11	O
							ESC_TX1_DATA2	13	O
							ESC_GPO2	14	IO
							SD0_C1	15	IO
							OUTPUTXBAR4	16	O
72		57			PB26 IOMUX_PB26 0x400C_C1E8	SDL	A0_26	AMUX0	A
							ANALOG_AIN36	A	A
							Disconnected	0	NA
							GPIO58	1	IO
							A1_26	AMUX1	A
							TIMG4_0_CCP0	2	IO
							A2_7	AMUX2	A
							CMP1_LN0	AMUX3	A
							ESC_TX1_DATA1	13	O
							ESC_GPO3	14	IO
							SD0_C3	15	IO
							OUTPUTXBAR5	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
73	G10	58			PB27 IOMUX_PB27 0x400C_C1EC	SDL	A0_27	AMUX0	A
							Disconnected	0	NA
							ANALOG_AIN37	A	A
							A1_27	AMUX1	A
							GPIO59	1	IO
							TIMG4_0_CCP1	2	IO
							A2_8	AMUX2	A
							CMP1_HP3_LP3	AMUX3	A
							PGA0_P6	AMUX4	A
							PGA1_P8	AMUX5	A
							PGA2_P8	AMUX6	A
							UC0_CTS_CS0	8	IO
							UC5_CTS	9	O
							UC2_CTS	10	O
							UC3_CTS_CS0	11	IO
							SD0_D1	13	I
							ESC_GPO0	14	IO
							SD0_D3	15	IO
							OUTPUTXBAR6	16	O
74	F10	59			PB28 IOMUX_PB28 0x400C_C1F0	SDL	ANALOG_AIN38	A	A
							A0_28	AMUX0	A
							Disconnected	0	NA
							GPIO60	1	IO
							A1_28	AMUX1	A
							TIMG4_0_CCP0	2	IO
							A2_9	AMUX2	A
							CMP0_HP3_LP3	AMUX3	A
							MCPWM2_2A	3	O
							PGA2_P6	AMUX4	A
							EPWM1_1A	4	O
							PGA0_P8	AMUX5	A
							EPWM4_1A	5	O
							UC0_RTS_POCI	8	O
							UC5_RTS	9	O
							UC2_RTS	10	O
							UC3_RTS_POCI	11	O
							ESC_PDI_UC_IRQ	14	IO
							OUTPUTXBAR7	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
75		60			PB29 IOMUX_PB29 0x400C_C1F4	SDL	ANALOG_AIN39	A	A
							A0_29	AMUX0	A
							Disconnected	0	NA
							GPIO61	1	IO
							A1_29	AMUX1	A
							TIMG4_0_CCP1	2	IO
							A2_10	AMUX2	A
							CMP0_LN0	AMUX3	A
							MCPWM2_2B	3	O
							EPWM1_1B	4	O
							EPWM4_1B	5	O
							UC5_RX_SCL	6	IO
							UC5_TX_SDA	8	O
							UC2_RX_SCL	10	IO
							UC2_TX_SDA	11	O
							ESC_TX1_DATA3	15	O
							OUTPUTXBAR8	16	O
76	E9	61			PB30 IOMUX_PB30 0x400C_C1F8	SDL	ANALOG_AIN40	A	A
							A0_30	AMUX0	A
							Disconnected	0	NA
							GPIO62	1	IO
							A1_30	AMUX1	A
							TIMG4_0_CCP0	2	IO
							A2_11	AMUX2	A
							CMP2_HP2_LP2	AMUX3	A
							MCPWM2_3A	3	O
							EPWM2_1A	4	O
							PGA1_P7	AMUX4	A
							EPWM5_1A	5	O
							UC5_TX_SDA	6	O
							UC5_RX_SCL	8	IO
							UC2_TX_SDA	10	O
							UC2_RX_SCL	11	IO
							ESC_TX1_DATA2	15	O
							OUTPUTXBAR1	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
77		62			PB31 IOMUX_PB31 0x400C_C1FC	SDL	Disconnected	0	NA
							A2_29	AMUX0	A
							ANALOG_AIN41	A	A
							GPIO63	1	IO
							CMP2_LN0	AMUX1	A
							TIMG4_0_CCP1	2	IO
							MCPWM2_3B	3	O
							EPWM2_1B	4	O
							EPWM5_1B	5	O
							UC1_RTS_POCI	7	O
							UC4_RTS_POCI	11	O
							ESC_TX1_DATA1	15	O
							OUTPUTXBAR2	16	O
125	C3	97			PC0 IOMUX_PC0 0x400C_C200	SDL	Disconnected	0	NA
							GPIO64	1	IO
							EPWM0_1B	3	O
							MCPWM2_1B	4	O
							EPWM0_1A	5	O
							EPWM4_1A	6	O
							UC0_TX_SDA_PICO	8	O
							UC3_TX_SDA_PICO	9	O
							ESC_PHY_CLK	14	IO
							OUTPUTXBAR1	16	O
126	A3	98			PC1 IOMUX_PC1 0x400C_C204	SDL	Disconnected	0	NA
							GPIO65	1	IO
							TRACE_DATA0	2	O
							SD0_C2	3	IO
							EPWM3_1A	4	O
							EPWM2_1A	5	O
							EPWM0_1A	6	O
							MCPWM2_1A	7	O
							UC0_RX_SCL_SCLK	8	IO
							UC3_RX_SCL_SCLK	9	IO
							ESC_LED_LINK1_ACTIVE	12	IO
							FSITX0_D0	13	IO
							ESC_RX1_CLK	14	I
							ESC_PHY1_LINKSTATUS	15	IO
							OUTPUTXBAR2	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
1		1			PC2 IOMUX_PC2 0x400C_C208	SDL	Disconnected	0	NA
							GPIO66	1	IO
							TRACE_CLK	2	IO
							EPWM5_1A	3	O
							UC5_RX_SCL	5	IO
							UC3_RX_SCL_SCLK	6	IO
							MCPWM2_1A	7	O
							SYSCTL_FCC_IN	8	I
							EPWM0_1A	9	O
							UC2_RX_SCL	10	IO
							UC0_RX_SCL_SCLK	11	IO
							ESC_TX1_DATA3	12	O
							ESC_I2C_SDA	14	IO
							SD0_C3	15	IO
							OUTPUTXBAR1	16	O
2		2			PC3 IOMUX_PC3 0x400C_C20C	SDL	Disconnected	0	NA
							GPIO67	1	IO
							TRACE_DATA0	2	O
							EPWM5_1B	3	O
							EPWM4_1A	4	O
							UC5_TX_SDA	5	O
							UC3_RTS_POCI	6	O
							MCPWM2_2A	7	O
							EPWM1_1A	8	O
							UC2_TX_SDA	10	O
							UC0_RTS_POCI	11	O
							ESC_TX1_DATA2	12	O
							ESC_I2C_SCL	14	IO
							SD0_D3	15	IO
							OUTPUTXBAR2	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
3		3			PC4 IOMUX_PC4 0x400C_C210	SDL	Disconnected	0	NA
							GPIO68	1	IO
							TRACE_DATA1	2	O
							EPWM3_1A	3	O
							UC3_RTS_POCI	6	O
							MCPWM2_1B	7	O
							EPWM0_1B	8	O
							UC0_RTS_POCI	11	O
							ESC_TX1_DATA1	12	O
							ESC_TX1_DATA3	14	O
							OUTPUTXBAR3	16	O
4		4			PC5 IOMUX_PC5 0x400C_C214	SDL	Disconnected	0	NA
							GPIO69	1	IO
							TRACE_DATA2	2	O
							EPWM3_1B	3	O
							EPWM4_1B	4	O
							UC3_CTS_CS0	6	IO
							MCPWM2_2B	7	O
							EPWM1_1B	8	O
							UC0_CTS_CS0	11	IO
							ESC_TX1_DATA0	12	O
							ESC_TX1_DATA2	14	O
							OUTPUTXBAR4	16	O
5		5			PC6 IOMUX_PC6 0x400C_C218	SDL	Disconnected	0	NA
							GPIO70	1	IO
							TRACE_DATA3	2	O
							EPWM2_1B	4	O
							UC3_TX_SDA_PICO	6	O
							MCPWM2_3B	7	O
							UC0_TX_SDA_PICO	11	O
							ESC_TX1_CLK	12	O
							ESC_TX1_DATA1	14	O
							OUTPUTXBAR5	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
53	K6	38			PC7 IOMUX_PC7 0x400C_C21C	SDL	Disconnected	0	NA
							ANALOG_AIN19	A	A
							A2_4	AMUX0	A
							GPIO71	1	IO
							CMP3_HP0_LP0	AMUX1	A
							UC0_RTS_POCI	7	O
							UC5_RX_SCL	8	IO
							UC2_RX_SCL	11	IO
							ESC_LATCH1	14	IO
							OUTPUTXBAR1	16	O
54	H6	39			PC8 IOMUX_PC8 0x400C_C220	SDL	Disconnected	0	NA
							A0_23	AMUX0	A
							ANALOG_AIN20	A	A
							GPIO72	1	IO
							A1_23	AMUX1	A
							A2_6	AMUX2	A
							EPWM1_1A	2	O
							CMP3_HN1_LN1	AMUX3	A
							MCPWM0_1B	3	O
							EPWM3_1B	4	O
							MCPWM0_2B	7	O
							UC5_TX_SDA	8	O
							UC2_TX_SDA	11	O
							ESC_PHY0_LINKSTATUS	14	IO
							OUTPUTXBAR2	16	O
55	J6	40			PC9 IOMUX_PC9 0x400C_C224	SDL	Disconnected	0	NA
							A2_2	AMUX0	A
							ANALOG_AIN21	A	A
							CMP3_HP2_LP2	AMUX1	A
							GPIO73	1	IO
							EPWM1_1B	2	O
							MCPWM0_1A	3	O
							EPWM3_1A	4	O
							MCPWM0_3B	7	O
							ESC_PHY1_LINKSTATUS	14	IO
							OUTPUTXBAR3	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
56	H7	41			PC10 IOMUX_PC10 0x400C_C228	SDL	Disconnected	0	NA
							ANALOG_AIN22	A	A
							A0_16	AMUX0	A
							GPIO74	1	IO
							A1_16	AMUX1	A
							A2_14	AMUX2	A
							MCPWM0_2B	3	O
							EPWM4_1B	4	O
							EPWM2_1B	5	O
							MCPWM0_1B	7	O
							ESC_GPI0	14	IO
							OUTPUTXBAR4	16	O
57	J7	42			PC11 IOMUX_PC11 0x400C_C22C	SDL	A0_24	AMUX0	A
							ANALOG_AIN23	A	A
							Disconnected	0	NA
							A1_24	AMUX1	A
							GPIO75	1	IO
							A2_15	AMUX2	A
							MCPWM0_2A	3	O
							EPWM4_1A	4	O
							EPWM2_1A	5	O
							UC3_RTS_POCI	6	O
							UC0_RTS_POCI	11	O
							ESC_GPI1	14	IO
							OUTPUTXBAR5	16	O
58	H8	43			PC12 IOMUX_PC12 0x400C_C230	SDL	Disconnected	0	NA
							A0_25	AMUX0	A
							ANALOG_AIN24	A	A
							A1_25	AMUX1	A
							GPIO76	1	IO
							A2_16	AMUX2	A
							MCPWM0_3B	3	O
							EPWM5_1B	4	O
							UC3_RX_SCL_SCLK	6	IO
							UC0_RX_SCL_SCLK	11	IO
							ESC_GPI2	14	IO
							OUTPUTXBAR6	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
59	K7	44			PC13 IOMUX_PC13 0x400C_C234	SDL	ANALOG_AIN25	A	A
							A2_3	AMUX0	A
							Disconnected	0	NA
							GPIO77	1	IO
							MCPWM0_3A	3	O
							EPWM5_1A	4	O
							UC3_CTS_CS0	6	IO
							UC0_CTS_CS0	11	IO
							ESC_GPI3	14	IO
							OUTPUTXBAR7	16	O
60	J8	45			PC14 IOMUX_PC14 0x400C_C238	SDL	Disconnected	0	NA
							A0_18	AMUX0	A
							ANALOG_AIN26	A	A
							GPIO78	1	IO
							MCPWM0_1A	3	O
							EPWM3_1A	4	O
							EPWM3_1B	5	O
							UC3_TX_SDA_PICO	6	O
							MCPWM0_1B	7	O
							UC0_TX_SDA_PICO	11	O
							ESC_TX0_DATA2	13	O
							OUTPUTXBAR8	16	O
61	K8	46			PC15 IOMUX_PC15 0x400C_C23C	SDL	Disconnected	0	NA
							ANALOG_AIN27	A	A
							A0_19	AMUX0	A
							GPIO79	1	IO
							CMP3_HP3_LP3	AMUX1	A
							EPWM3_1A	5	O
							MCPWM0_1A	7	O
							UC0_TX_SDA_PICO	8	O
							UC0_RX_SCL_SCLK	9	IO
							UC3_RX_SCL_SCLK	10	IO
							UC3_TX_SDA_PICO	11	O
							ESC_GPO0	14	IO
							OUTPUTXBAR1	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
26		19			PC18 IOMUX_PC18 0x400C_C248	SDL	Disconnected	0	NA
							GPIO82	1	IO
							MCPWM2_3A	3	O
							EPWM2_1A	4	O
							EPWM5_1A	5	O
							ESC_LED_LINK0_ACTIVE	14	IO
							OUTPUTXBAR7	16	O
10					PC19 IOMUX_PC19 0x400C_C24C	SDL	Disconnected	0	NA
							GPIO83	1	IO
							MCPWM2_1A	3	O
							EPWM0_1A	4	O
							UC0_RX_SCL_SCLK	5	IO
							UC5_RX_SCL	6	IO
							UC4_TX_SDA_PICO	7	O
							UC5_CTS	8	O
							SYSCTL_FCC_IN	9	I
							UC1_TX_SDA_PICO	11	O
							ESC_RX1_DV	12	I
							ESC_MDIO_CLK	14	IO
							OUTPUTXBAR3	16	O
19	C1	12	5	C1	PC16_X1 IOMUX_PC16_X1 0x400C_C240	SDL	Disconnected	0	NA
							A0_10	AMUX0	A
							ANALOG_AIN0	A	A
							SYSCTL_HFCLKIN	AMUX1	A
							GPIO80	1	IO
							SYSCTL_X1	AMUX2	A
							UC2_TX_SDA	2	O
							EPWM1_1B	4	O
							UC1_TX_SDA_PICO	5	O
							UC1_RTS_POCI	6	O
							MCPWM0_3B	7	O
							UC4_RTS_POCI	8	O
							EPWM5_1B	9	O
							SD0_C1	10	IO
							ESC_RX1_DATA1	14	I
							OUTPUTXBAR2	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
20	D1	13	6	D1	PC17_X2 IOMUX_PC17_X2 0x400C_C244	SDL	A1_10	AMUX0	A
							ANALOG_AIN1	A	A
							Disconnected	0	NA
							GPIO81	1	IO
							CMP2_HN0	AMUX1	A
							UC2_RX_SCL	2	IO
							SYSCTL_X2	AMUX2	A
							UC1_RX_SCL_SCLK	6	IO
							SD0_D1	10	IO
							ESC_RX1_DATA2	14	I
							OUTPUTXBAR3	16	O
11					PC20 IOMUX_PC20 0x400C_C250	SDL	Disconnected	0	NA
							GPIO84	1	IO
							EPWM0_1B	3	O
							MCPWM2_1B	4	O
							UC0_TX_SDA_PICO	5	O
							UC5_TX_SDA	6	O
							UC4_RX_SCL_SCLK	7	IO
							UC5_RTS	8	O
							UC1_RX_SCL_SCLK	11	IO
							ESC_RX1_DATA0	12	I
							ESC_RX1_DATA1	13	I
							ESC_MDIO_DATA	14	IO
							OUTPUTXBAR4	16	O
14					PC21 IOMUX_PC21 0x400C_C254	SDL	Disconnected	0	NA
							GPIO85	1	IO
							MCPWM2_2B	3	O
							EPWM1_1B	4	O
							EPWM4_1B	6	O
							ESC_RX1_DATA1	12	I
							ESC_RX1_DATA0	13	I
							ESC_PHY_CLK	14	IO
							OUTPUTXBAR5	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
97	B8				PC22 IOMUX_PC22 0x400C_C258	SDL	Disconnected	0	NA
							GPIO86	1	IO
							EPWM2_1B	3	O
							MCPWM2_3B	4	O
							UC1_RX_SCL_SCLK	5	IO
							UC4_RX_SCL_SCLK	6	IO
							EPWM0_1A	7	O
							UC0_RTS_POCI	8	O
							EPWM4_1A	9	O
							UC3_RTS_POCI	10	O
							EPWM5_1B	11	O
							ESC_TX0_DATA2	12	O
							ESC_TX0_DATA1	14	O
							ESC_PHY0_LINKSTATUS	15	IO
							OUTPUTXBAR2	16	O
15	D3				PC23 IOMUX_PC23 0x400C_C25C	SDL	Disconnected	0	NA
							GPIO87	1	IO
							UC5_RX_SCL	2	IO
							MCPWM2_2A	3	O
							EPWM1_1A	4	O
							UC4_RTS_POCI	5	O
							EPWM4_1A	6	O
							EPWM0_1B	7	O
							UC1_RTS_POCI	10	O
							UC2_RX_SCL	11	IO
							ESC_RX1_DATA2	12	I
							ESC_RX1_CLK	14	I
							OUTPUTXBAR6	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
16					PC24 IOMUX_PC24 0x400C_C260	SDL	Disconnected	0	NA
							GPIO88	1	IO
							UC5_TX_SDA	2	O
							EPWM0_1B	4	O
							UC4_CTS_CS0	5	IO
							EPWM1_1A	7	O
							UC1_CTS_CS0	10	IO
							UC2_TX_SDA	11	O
							ESC_RX1_DATA3	12	I
							ESC_RX1_DV	14	I
							OUTPUTXBAR7	16	O
17	D2	10			PC25 IOMUX_PC25 0x400C_C264	SDL	Disconnected	0	NA
							GPIO89	1	IO
							UC5_CTS	2	O
							UC2_TX_SDA	3	O
							EPWM0_1A	4	O
							UC4_TX_SDA_PICO	5	O
							UC1_RX_SCL_SCLK	6	IO
							EPWM1_1B	7	O
							UC5_RX_SCL	8	IO
							EPWM4_1A	9	O
							UC1_TX_SDA_PICO	10	IO
							UC2_CTS	11	O
							ESC_RX1_ERR	14	I
							OUTPUTXBAR8	16	O
18		11			PC26 IOMUX_PC26 0x400C_C268	SDL	Disconnected	0	NA
							GPIO90	1	IO
							UC5_RTS	2	O
							UC2_RX_SCL	3	IO
							EPWM1_1A	4	O
							UC4_RX_SCL_SCLK	5	IO
							UC1_RX_SCL_SCLK	6	IO
							SYSCTL_XCLKOUT	7	O
							UC5_TX_SDA	8	O
							UC2_RTS	11	O
							ESC_RX1_DATA0	14	I
							OUTPUTXBAR1	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
48					PC27 IOMUX_PC27 0x400C_C26C	SDL	Disconnected	0	NA
							GPIO91	1	IO
							ESC_TX0_DATA2	14	O
							OUTPUTXBAR4	16	O
49					PC28 IOMUX_PC28 0x400C_C270	SDL	Disconnected	0	NA
							GPIO92	1	IO
							MCPWM2_1A	3	O
							EPWM0_1A	4	O
							MCAN1_TX	11	IO
							ESC_TX0_DATA3	14	O
							OUTPUTXBAR5	16	O
50					PC29 IOMUX_PC29 0x400C_C274	SDL	Disconnected	0	NA
							GPIO93	1	IO
							MCPWM2_2A	3	O
							EPWM1_1A	4	O
							EPWM4_1A	5	O
							UC0_CTS_CS0	7	IO
							ESC_TX1_ENA	14	O
							OUTPUTXBAR6	16	O
51					PC30 IOMUX_PC30 0x400C_C278	SDL	Disconnected	0	NA
							GPIO94	1	IO
							MCPWM2_3A	3	O
							EPWM2_1A	4	O
							UC2_RX_SCL	5	IO
							EPWM5_1A	6	O
							UC0_RX_SCL_SCLK	7	IO
							UC5_RX_SCL	8	IO
							ESC_TX1_CLK	14	O
							OUTPUTXBAR7	16	O
52					PC31 IOMUX_PC31 0x400C_C27C	SDL	Disconnected	0	NA
							GPIO95	1	IO
							MCPWM2_1A	3	O
							EPWM0_1A	4	O
							UC2_TX_SDA	5	O
							UC0_TX_SDA_PICO	7	O
							UC5_TX_SDA	8	O
							ESC_LATCH0	14	IO
							OUTPUTXBAR8	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
82					PD0 IOMUX_PD0 0x400C_C280	SDL	Disconnected	0	NA
							GPIO96	1	IO
							MCPWM2_1B	3	O
							EPWM0_1B	4	O
							UC2_RTS	5	O
							UC5_RTS	8	O
							EPWM4_1A	14	O
							EPWM0_1A	15	O
							OUTPUTXBAR5	16	O
83					PD1 IOMUX_PD1 0x400C_C284	SDL	Disconnected	0	NA
							GPIO97	1	IO
							MCPWM2_2B	3	O
							EPWM1_1B	4	O
							UC2_CTS	5	O
							UC5_CTS	8	O
							EPWM4_1B	14	O
							EPWM0_1B	15	O
							OUTPUTXBAR6	16	O
84					PD2 IOMUX_PD2 0x400C_C288	SDL	Disconnected	0	NA
							GPIO98	1	IO
							MCPWM2_3B	3	O
							EPWM2_1B	4	O
							EPWM5_1B	5	O
							UC0_RX_SCL_SCLK	6	IO
							UC3_RX_SCL_SCLK	11	IO
							ESC_GPO1	14	IO
							EPWM1_1A	15	O
							OUTPUTXBAR7	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
85	E10				PD3 IOMUX_PD3 0x400C_C28C	SDL	Disconnected	0	NA
							GPIO99	1	IO
							UC2_RX_SCL	5	IO
							UC0_CTS_CS0	6	IO
							MCPWM2_1B	7	O
							EPWM0_1B	8	O
							UC3_CTS_CS0	10	IO
							UC5_RX_SCL	11	IO
							ESC_TX1_DATA1	13	O
							ESC_GPO2	14	IO
							EPWM1_1B	15	O
							OUTPUTXBAR8	16	O
86					PD4 IOMUX_PD4 0x400C_C290	SDL	Disconnected	0	NA
							GPIO100	1	IO
							UC2_TX_SDA	5	O
							UC0_TX_SDA_PICO	6	O
							UC3_TX_SDA_PICO	10	O
							UC5_TX_SDA	11	O
							FSIRX0_D0	12	I
							EPWM3_1A	13	O
							EPWM5_1A	14	O
							EPWM2_1A	15	O
							OUTPUTXBAR1	16	O
103					PD5 IOMUX_PD5 0x400C_C294	SDL	Disconnected	0	NA
							GPIO101	1	IO
							UC0_RTS_POCI	6	O
							UC1_CTS_CS0	8	IO
							UC0_CTS_CS0	9	IO
							ESC_TX0_DATA1	12	O
							ESC_SYNC1	14	IO
							OUTPUTXBAR5	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
104					PD6 IOMUX_PD6 0x400C_C298	SDL	Disconnected	0	NA
							GPIO102	1	IO
							FSIRX0_D0	7	I
							UC1_RTS_POCI	8	O
							UC0_RTS_POCI	9	O
							ESC_RX0_DATA1	12	I
							ESC_TX0_ENA	13	O
							ESC_MDIO_CLK	14	IO
							OUTPUTXBAR6	16	O
105					PD7 IOMUX_PD7 0x400C_C29C	SDL	Disconnected	0	NA
							GPIO103	1	IO
							UC0_RX_SCL_SCLK	5	IO
							FSIRX0_D1	7	I
							UC1_TX_SDA_PICO	8	O
							UC0_TX_SDA_PICO	9	O
							UC3_RX_SCL_SCLK	11	IO
							ESC_RX0_DATA2	12	I
							ESC_TX0_CLK	13	I
							ESC_MDIO_DATA	14	IO
							ESC_RX1_DATA2	15	I
							OUTPUTXBAR7	16	O
106	B5				PD8 IOMUX_PD8 0x400C_C2A0	SDL	Disconnected	0	NA
							GPIO104	1	IO
							UC0_TX_SDA_PICO	5	O
							FSIRX0_CLK	7	I
							UC1_RX_SCL_SCLK	8	IO
							UC0_RX_SCL_SCLK	9	IO
							UC3_TX_SDA_PICO	11	O
							ESC_RX0_DATA3	12	I
							ESC_PDI_UC_IRQ	13	O
							EPWM4_1A	14	O
							EPWM0_1A	15	O
							OUTPUTXBAR8	16	O

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Table 5-1. Pin Attributes (LQFP128, BGA99, LQFP100_G, LQFP64_G, WCSP48 Packages) (continued)

LQFP128 PIN	BGA99 PIN	LQFP100_G PIN	LQFP64_G PIN	WCSP48 PIN	BALL NAME/ IOMUX Register/ IOMUX Address	IO TYPE	SIGNAL NAME	MODE	TYPE
107					PD9 IOMUX_PD9 0x400C_C2A4	SDL	Disconnected	0	NA
							GPIO105	1	IO
							UC2_RX_SCL	7	IO
							UC0_TX_SDA_PICO	8	O
							UC5_RX_SCL	9	IO
							UC3_TX_SDA_PICO	10	O
							ESC_TX0_DATA0	12	O
							EPWM4_1B	14	O
							EPWM0_1B	15	O
							OUTPUTXBAR1	16	O
	H5				PD16 IOMUX_PD16 0x400C_C2C0	SDL	Disconnected	0	NA
							GPIO112	1	IO
							EPWM3_1A	2	O
							EPWM4_1A	3	O
							MCPWM1_1A	4	O
							MCPWM1_3A	5	O
							MCPWM2_2A	6	O
							UC2_RX_SCL	7	O
							UC4_RX_SCL_SCLK	8	IO
							UC1_CTS_CS0	9	IO
							ESC_RX1_DATA3	14	I
							OUTPUTXBAR7	16	O
111, 128, 13, 47, 6, 64, 79, 95	A2, D8, G8	100, 49, 6, 64, 75	1, 32, 48, 64	A1, A7, G7	VDD	PWR	VDD		PWR
31, 45	J1	24, 37	16, 29	G1	VDDA	APWR	VDDA		APWR
43, 44	J5	36	28	G4	VREFHI	AREF	VREFHI		AREF
42	K5	35	27	G3	VREFLO	AREF	VREFLO		AREF
110, 12, 127, 46, 63, 78, 94	A10, B1, D4, D5, D6, D7, E4, E5, E6, E7, F4, F5, F6, F7, G4, G5, G6, G7, K10	48, 63, 74, 99	31, 47, 63	A2, A6, G6	VSS	GND	VSS		GND
30	H1, K1	23	15	F1	VSSA	AGND	VSSA		AGND

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5.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

Note

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via IOMUX pad configuration registers. Some device subsystems provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **PIN TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - IO = Input, Output, or simultaneously Input and Output
   - ID = Input with open-drain output function
   - OD = Output, with open-drain output function
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - CAP = LDO capacitor
   - PWR = Power
   - GND = Ground
3. **DESCRIPTION:** Description of the signal
4. **BALL:** Associated ball number

For more information on the I/O cell configurations, see the *Pad Configuration Registers* section within the *Device Configuration* chapter of the device TRM.

Table 5-2. ADC0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
A0_1	A	ADC0 Input 1	27	F3	20	12	C2
A0_2	A	ADC0 Input 2	28	G1	21	13	D2
A0_3	A	ADC0 Input 3	29	G2	22	14	D3
A0_4	A	ADC0 Input 4	32	G3	25	17	E1
A0_5	A	ADC0 Input 5	68	H9	53	36	E6
A0_6	A	ADC0 Input 6	22	E2	15	8	
A0_7	A	ADC0 Input 7	23	F2	16	9	
A0_8	A	ADC0 Input 8	24	F1	17	10	
A0_9	A	ADC0 Input 9	25	E3	18	11	
A0_10	A	ADC0 Input 10	19	C1	12	5	C1
A0_11	A	ADC0 Input 11	66	J9	51	34	F6
A0_12	A	ADC0 Input 12	40	K4	33	25	F3
A0_14	A	ADC0 Input 14	65	J10	50	33	F5

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Table 5-2. ADC0 Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
A0_15	A	ADC0 Input 15	39	H4	32	24	G2
A0_16	A	ADC0 Input 16	56	H7	41		
A0_17	A	ADC0 Input 17	35	J2	28	20	F2
A0_18	A	ADC0 Input 18	60	J8	45		
A0_19	A	ADC0 Input 19	61	K8	46		
A0_21	A	ADC0 Input 21	70	G9	55		
A0_22	A	ADC0 Input 22	71	F9	56		
A0_23	A	ADC0 Input 23	54	H6	39		
A0_24	A	ADC0 Input 24	57	J7	42		
A0_25	A	ADC0 Input 25	58	H8	43		
A0_26	A	ADC0 Input 26	72		57		
A0_27	A	ADC0 Input 27	73	G10	58		
A0_28	A	ADC0 Input 28	74	F10	59		
A0_29	A	ADC0 Input 29	75		60		
A0_30	A	ADC0 Input 30	76	E9	61		

Table 5-3. ADC1 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
A1_1	A	ADC1 Input 1	27	F3	20	12	C2
A1_2	A	ADC1 Input 2	28	G1	21	13	D2
A1_3	A	ADC1 Input 3	35	J2	28	20	F2
A1_4	A	ADC1 Input 4	36	K3	29	21	E4
A1_5	A	ADC1 Input 5	37	H3	30	22	
A1_6	A	ADC1 Input 6	22	E2	15	8	
A1_7	A	ADC1 Input 7	23	F2	16	9	
A1_8	A	ADC1 Input 8	24	F1	17	10	
A1_9	A	ADC1 Input 9	25	E3	18	11	
A1_10	A	ADC1 Input 10	20	D1	13	6	D1
A1_11	A	ADC1 Input 11	38	J3	31	23	
A1_12	A	ADC1 Input 12	41	J4	34	26	F4
A1_13	A	ADC1 Input 13	34	H2	27	19	E5
A1_14	A	ADC1 Input 14	65	J10	50	33	F5
A1_15	A	ADC1 Input 15	69	F8	54	37	E7
A1_16	A	ADC1 Input 16	56	H7	41		
A1_17	A	ADC1 Input 17	33	K2	26	18	E3
A1_18	A	ADC1 Input 18	89	D10	69	42	D7
A1_19	A	ADC1 Input 19	90	C8	70	43	C7
A1_21	A	ADC1 Input 21	70	G9	55		
A1_22	A	ADC1 Input 22	71	F9	56		
A1_23	A	ADC1 Input 23	54	H6	39		
A1_24	A	ADC1 Input 24	57	J7	42		
A1_25	A	ADC1 Input 25	58	H8	43		

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Table 5-3. ADC1 Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
A1_26	A	ADC1 Input 26	72		57		
A1_27	A	ADC1 Input 27	73	G10	58		
A1_28	A	ADC1 Input 28	74	F10	59		
A1_29	A	ADC1 Input 29	75		60		
A1_30	A	ADC1 Input 30	76	E9	61		

Table 5-4. ADC2 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
A2_1	A	ADC2 Input 1	40	K4	33	25	F3
A2_2	A	ADC2 Input 2	55	J6	40		
A2_3	A	ADC2 Input 3	59	K7	44		
A2_4	A	ADC2 Input 4	53	K6	38		
A2_5	A	ADC2 Input 5	67	H10	52	35	F7
A2_6	A	ADC2 Input 6	54	H6	39		
A2_7	A	ADC2 Input 7	72		57		
A2_8	A	ADC2 Input 8	73	G10	58		
A2_9	A	ADC2 Input 9	74	F10	59		
A2_10	A	ADC2 Input 10	75		60		
A2_11	A	ADC2 Input 11	76	E9	61		
A2_12	A	ADC2 Input 12	39	H4	32	24	G2
A2_14	A	ADC2 Input 14	56	H7	41		
A2_15	A	ADC2 Input 15	57	J7	42		
A2_16	A	ADC2 Input 16	58	H8	43		
A2_17	A	ADC2 Input 17	62	K9	47	30	G5
A2_18	A	ADC2 Input 18	33	K2	26	18	E3
A2_19	A	ADC2 Input 19	34	H2	27	19	E5
A2_21	A	ADC2 Input 21	32	G3	25	17	E1
A2_22	A	ADC2 Input 22	36	K3	29	21	E4
A2_23	A	ADC2 Input 23	37	H3	30	22	
A2_24	A	ADC2 Input 24	38	J3	31	23	
A2_25	A	ADC2 Input 25	29	G2	22	14	D3
A2_26	A	ADC2 Input 26	35	J2	28	20	F2
A2_27	A	ADC2 Input 27	68	H9	53	36	E6
A2_28	A	ADC2 Input 28	69	F8	54	37	E7
A2_29	A	ADC2 Input 29	77		62		
A2_30	A	ADC2 Input 30	66	J9	51	34	F6

Table 5-5. ADCCAL Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
ADCCAL_ADCINCAL0	A	ADC Calibration Input 0	35	J2	28	20	F2

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Table 5-6. ANALOG Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
ANALOG_AIN0	A	A0_10 HFCLKIN X1	19	C1	12	5	C1
ANALOG_AIN1	A	A1_10 CMP2_HN0 X2	20	D1	13	6	D1
ANALOG_AIN2	A	A0_6 A1_6 CMP2_HN1	22	E2	15	8	
ANALOG_AIN3	A	A0_7 A1_7 CMP2_HP1_LP1	23	F2	16	9	
ANALOG_AIN4	A	A0_8 A1_8	24	F1	17	10	
ANALOG_AIN5	A	A0_9 A1_9 PGA2_P1 PGA0_P0 PGA1_P0	25	E3	18	11	
ANALOG_AIN6	A	A0_1 A1_1 CMP0_HN0 CMP2_HP0_LP0	27	F3	20	12	C2
ANALOG_AIN7	A	A0_2 A1_2 CMP0_HP1_LP1 PGA0_P1 PGA1_M0 PGA2_P2	28	G1	21	13	D2
ANALOG_AIN8	A	A0_3 A2_25 CMP1_HN0 PGA0_OUT	29	G2	22	14	D3
ANALOG_AIN9	A	A0_4 A2_21 CMP1_HP0_LP0 PGA0_M0 PGA0_P2 PGA2_M0	32	G3	25	17	E1
ANALOG_AIN10	A	A1_17 A2_18 CMP2_DACL CMP0_HN1 TESTANA0	33	K2	26	18	E3
ANALOG_AIN11	A	A1_13 A2_19 CMP1_HN1 PGA1_M1 TESTANA1	34	H2	27	19	E5
ANALOG_AIN12	A	A0_17 A1_3 A2_26 CMP3_DACL PGA1_OUT ADCINCAL0	35	J2	28	20	F2

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Table 5-6. ANALOG Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
ANALOG_AIN13	A	A1_4 A2_22 CMP1_HP1_LP1 PGA0_P3 PGA1_P1	36	K3	29	21	E4
ANALOG_AIN14	A	A1_5 A2_23	37	H3	30	22	
ANALOG_AIN15	A	A1_11 A2_24 PGA0_M1 PGA1_M2	38	J3	31	23	
ANALOG_AIN16	A	A0_15 A2_12 CMP3_HP1_LP1 PGA1_P2 PGA2_P3	39	H4	32	24	G2
ANALOG_AIN17	A	A0_12 A2_1 CMP0_HP0_LP0 PGA1_M3 PGA2_OUT	40	K4	33	25	F3
ANALOG_AIN18	A	A1_12 CMP3_HN0_LN0 PGA2_M1	41	J4	34	26	F4
ANALOG_AIN19	A	A2_4 CMP3_HP0_LP0	53	K6	38		
ANALOG_AIN20	A	A0_23 A1_23 A2_6 CMP3_HN1_LN1	54	H6	39		
ANALOG_AIN21	A	A2_2 CMP3_HP2_LP2	55	J6	40		
ANALOG_AIN22	A	A0_16 A1_16 A2_14	56	H7	41		
ANALOG_AIN23	A	A0_24 A1_24 A2_15	57	J7	42		
ANALOG_AIN24	A	A0_25 A1_25 A2_16	58	H8	43		
ANALOG_AIN25	A	A2_3	59	K7	44		
ANALOG_AIN26	A	A0_18	60	J8	45		
ANALOG_AIN27	A	A0_19 CMP3_HP3_LP3	61	K8	46		
ANALOG_AIN28	A	A2_17 CMP0_LN1 PGA2_M2 PGA0_M2	62	K9	47	30	G5
ANALOG_AIN29	A	A0_14 A1_14 CMP1_HP2_LP2 PGA0_P4 PGA2_P0	65	J10	50	33	F5

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Table 5-6. ANALOG Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
ANALOG_AIN30	A	A0_11 A2_30 CMP2_LN1 PGA1_P3 PGA0_P7	66	J9	51	34	F6
ANALOG_AIN31	A	A2_5 CMP0_HP2_LP2 PGA0_P5 PGA1_P4 PGA2_P4	67	H10	52	35	F7
ANALOG_AIN32	A	A0_5 A2_27 CMP2_HP3_LP3 PGA1_P5 PGA2_P5	68	H9	53	36	E6
ANALOG_AIN33	A	A1_15 A2_28 CMP1_LN1 PGA2_M3	69	F8	54	37	E7
ANALOG_AIN34	A	A0_21 A1_21 PGA0_M3	70	G9	55		
ANALOG_AIN35	A	A0_22 A1_22 PGA1_P6 PGA2_P7	71	F9	56		
ANALOG_AIN36	A	A0_26 A1_26 A2_7 CMP1_LN0	72		57		
ANALOG_AIN37	A	A0_27 A1_27 A2_8 CMP1_HP3_LP3 PGA0_P6 PGA1_P8 PGA2_P8	73	G10	58		
ANALOG_AIN38	A	A0_28 A1_28 A2_9 CMP0_HP3_LP3 PGA2_P6 PGA0_P8	74	F10	59		
ANALOG_AIN39	A	A0_29 A1_29 A2_10 CMP0_LN0	75		60		
ANALOG_AIN40	A	A0_30 A1_30 A2_11 CMP2_HP2_LP2 PGA1_P7	76	E9	61		
ANALOG_AIN41	A	A2_29 CMP2_LN0	77		62		
ANALOG_AIN42	A	A1_18	89	D10	69	42	D7
ANALOG_AIN43	A	A1_19	90	C8	70	43	C7

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Table 5-7. ANALOGTEST Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
INTERNAL_TESTANA0	Internal/A	Internal Analog Test Signal 0	33	K2	26	18	E3
INTERNAL_TESTANA1	Internal/A	Internal Analog Test Signal 1	34	H2	27	19	E5

Table 5-8. CMP0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
CMP0_HN0	A	CMPSS0 High Comparator Negative Input 0	27	F3	20	12	C2
CMP0_HN1	A	CMPSS0 High Comparator Negative Input 1	33	K2	26	18	E3
CMP0_HP0_LP0	A	CMPSS0 High/Low Comparator Positive Input 0	40	K4	33	25	F3
CMP0_HP1_LP1	A	CMPSS0 High/Low Comparator Positive Input 1	28	G1	21	13	D2
CMP0_HP2_LP2	A	CMPSS0 High/Low Comparator Positive Input 2	67	H10	52	35	F7
CMP0_HP3_LP3	A	CMPSS0 High/Low Comparator Positive Input 3	74	F10	59		
CMP0_LN0	A	CMPSS0 Low Comparator Negative Input 0	75		60		
CMP0_LN1	A	CMPSS0 Low Comparator Negative Input 1	62	K9	47	30	G5

Table 5-9. CMP1 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
CMP1_HN0	A	CMPSS1 High Comparator Negative Input 0	29	G2	22	14	D3
CMP1_HN1	A	CMPSS1 High Comparator Negative Input 1	34	H2	27	19	E5
CMP1_HP0_LP0	A	CMPSS1 High/Low Comparator Positive Input 0	32	G3	25	17	E1
CMP1_HP1_LP1	A	CMPSS1 High/Low Comparator Positive Input 1	36	K3	29	21	E4
CMP1_HP2_LP2	A	CMPSS1 High/Low Comparator Positive Input 2	65	J10	50	33	F5
CMP1_HP3_LP3	A	CMPSS1 High/Low Comparator Positive Input 3	73	G10	58		
CMP1_LN0	A	CMPSS1 Low Comparator Negative Input 0	72		57		
CMP1_LN1	A	CMPSS1 Low Comparator Negative Input 1	69	F8	54	37	E7

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Table 5-10. CMP2 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
CMP2_DACL	A	CMPSS2 Buffered DACL Out	33	K2	26	18	E3
CMP2_HN0	A	CMPSS2 High Comparator Negative Input 0	20	D1	13	6	D1
CMP2_HN1	A	CMPSS2 High Comparator Negative Input 1	22	E2	15	8	
CMP2_HP0_LP0	A	CMPSS2 High/Low Comparator Positive Input 0	27	F3	20	12	C2
CMP2_HP1_LP1	A	CMPSS2 High/Low Comparator Positive Input 1	23	F2	16	9	
CMP2_HP2_LP2	A	CMPSS2 High/Low Comparator Positive Input 2	76	E9	61		
CMP2_HP3_LP3	A	CMPSS2 High/Low Comparator Positive Input 3	68	H9	53	36	E6
CMP2_LN0	A	CMPSS2 Low Comparator Negative Input 0	77		62		
CMP2_LN1	A	CMPSS2 Low Comparator Negative Input 1	66	J9	51	34	F6

Table 5-11. CMP3 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
CMP3_DACL	A	CMPSS3 Buffered DACL Out	35	J2	28	20	F2
CMP3_HN0_LN0	A	CMPSS3 High/Low Comparator Negative Input 0	41	J4	34	26	F4
CMP3_HN1_LN1	A	CMPSS3 High/Low Comparator Negative Input 1	54	H6	39		
CMP3_HP0_LP0	A	CMPSS3 High/Low Comparator Positive Input 0	53	K6	38		
CMP3_HP1_LP1	A	CMPSS3 High/Low Comparator Positive Input 1	39	H4	32	24	G2
CMP3_HP2_LP2	A	CMPSS3 High/Low Comparator Positive Input 2	55	J6	40		
CMP3_HP3_LP3	A	CMPSS3 High/Low Comparator Positive Input 3	61	K8	46		

Table 5-12. DEBUG Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
DEBUG_JTCK_SWCLK	IO	JTAG Test Clock/Serial Wire Debug Clock	98	A9	77	50	B5
DEBUG_JTDI	I	JTAG Test Data In	99	C7	78	51	A5
DEBUG_JTDO_SWO	O	JTAG Test Data Out/Serial Wire Debug Out	118	A5	90	56	C5
DEBUG_TMS_SWDIO	IO	JTAG Test Mode Select/Serial Wire Debug In-Out	96	B10	76	49	B6

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Table 5-13. Disconnected0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
Disconnected	NA	No Peripheral Connection	1, 10, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 11, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 14, 15, 16, 17, 18, 19, 2, 20, 22, 23, 24, 25, 26, 27, 28, 29, 3, 32, 33, 34, 35, 36, 37, 38, 39, 4, 40, 41, 48, 49, 5, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 65, 66, 67, 68, 69, 7, 70, 71, 72, 73, 74, 75, 76, 77, 8, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 9, 90, 91, 92, 93, 96, 97, 98, 99	A3, A4, A5, A6, A7, A8, A9, B10, B2, B3, B4, B5, B6, B7, B8, B9, C1, C10, C2, C3, C4, C5, C6, C7, C8, C9, D1, D10, D2, D3, D9, E10, E2, E3, E8, E9, F1, F10, F2, F3, F8, F9, G1, G10, G2, G3, G9, H10, H2, H3, H4, H5, H6, H7, H8, H9, J10, J2, J3, J4, J6, J7, J8, J9, K2, K3, K4, K6, K7, K8, K9	1, 10, 11, 12, 13, 15, 16, 17, 18, 19, 2, 20, 21, 22, 25, 26, 27, 28, 29, 3, 30, 31, 32, 33, 34, 38, 39, 4, 40, 41, 42, 43, 44, 45, 46, 47, 5, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 65, 66, 67, 68, 69, 7, 70, 71, 72, 73, 76, 77, 78, 79, 8, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 9, 90, 91, 92, 93, 94, 95, 96, 97, 98	10, 11, 12, 13, 14, 17, 18, 19, 2, 20, 21, 22, 23, 24, 25, 26, 3, 30, 33, 34, 35, 36, 37, 38, 39, 4, 40, 41, 42, 43, 44, 45, 46, 49, 5, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 6, 60, 61, 62, 8, 9	A3, A4, A5, B1, B3, B4, B5, B6, B7, C1, C2, C3, C4, C5, C6, C7, D1, D2, D3, D4, D5, D6, D7, E1, E3, E4, E5, E6, E7, F2, F3, F4, F5, F6, F7, G2, G5

Table 5-14. EPWM Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
EPWM5_1B	O	EPWM5_1B	81		66	39	

Table 5-15. EPWM0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
EPWM0_1A	O	EPWM0 Output 1A	1, 10, 106, 119, 123, 125, 126, 17, 27, 29, 35, 41, 49, 52, 68, 82, 87, 89, 93, 97, 99	A3, B5, B8, C10, C3, C4, C7, D10, D2, E8, F3, G2, H9, J2, J4	1, 10, 20, 22, 28, 34, 53, 67, 69, 73, 78, 91, 95, 97, 98	12, 14, 20, 26, 36, 40, 42, 46, 51, 57, 61	A3, A4, A5, B7, C2, D3, D7, E6, F2, F4

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Table 5-15. EPWM0 Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
EPWM0_1B	O	EPWM0 Output 1B	102, 107, 11, 121, 125, 15, 16, 28, 29, 3, 34, 40, 69, 7, 82, 83, 85, 88, 90, 96	A8, B10, B2, B4, C3, C8, D3, D9, E10, F8, G1, G2, H2, K4	21, 22, 27, 3, 33, 54, 68, 7, 70, 76, 81, 93, 97	13, 14, 19, 2, 25, 37, 41, 43, 49, 54, 59	B3, B4, B6, C7, D2, D3, E5, E7, F3

Table 5-16. EPWM1 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
EPWM1_1A	O	EPWM1 Output 1A	109, 121, 15, 16, 18, 2, 24, 28, 32, 50, 54, 69, 74, 84, 91	A7, B4, B9, D3, F1, F10, F8, G1, G3, H6	11, 17, 2, 21, 25, 39, 54, 59, 71, 83, 93	10, 13, 17, 37, 44, 59	B4, D2, D6, E1, E7
EPWM1_1B	O	EPWM1 Output 1B	100, 108, 122, 14, 17, 19, 32, 4, 55, 75, 83, 85, 92, 93	A4, B6, B7, C1, C10, C9, D2, E10, G3, J6	10, 12, 25, 4, 40, 60, 72, 73, 79, 82, 94	17, 45, 46, 5, 52, 60	B7, C1, C6, D4, E1

Table 5-17. EPWM2 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
EPWM2_1A	O	EPWM2 Output 1A	117, 120, 123, 124, 126, 23, 26, 29, 35, 36, 51, 57, 62, 66, 76, 80, 86, 87, 90, 96, 98	A3, A9, B10, B3, C4, C5, C8, E8, E9, F2, G2, J2, J7, J9, K3, K9	16, 19, 22, 28, 29, 42, 47, 51, 61, 65, 67, 70, 76, 77, 89, 92, 95, 96, 98	14, 20, 21, 30, 34, 38, 40, 43, 49, 50, 58, 61, 62, 9	A3, B5, B6, C4, C7, D3, D5, E4, F2, F6, G5
EPWM2_1B	O	EPWM2 Output 1B	116, 121, 122, 124, 32, 36, 39, 5, 56, 65, 67, 68, 77, 81, 84, 87, 88, 91, 93, 97	A4, B3, B4, B8, B9, C10, D9, E8, G3, H10, H4, H7, H9, J10, K3	25, 29, 32, 41, 5, 50, 52, 53, 62, 66, 67, 68, 71, 73, 88, 93, 94, 96	17, 21, 24, 33, 35, 36, 39, 40, 41, 44, 46, 59, 60, 62	B4, B7, C4, D4, D6, E1, E4, E6, F5, F7, G2

Table 5-18. EPWM3 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
EPWM3_1A	O	EPWM3 Output 1A	113, 124, 126, 22, 25, 27, 3, 34, 36, 39, 55, 60, 61, 66, 68, 86, 89, 92	A3, B3, C9, D10, E2, E3, F3, H2, H4, H5, H9, J6, J8, J9, K3, K8	15, 18, 20, 27, 29, 3, 32, 40, 45, 46, 51, 53, 69, 72, 85, 96, 98	11, 12, 19, 21, 24, 34, 36, 42, 45, 62, 8	C2, C4, C6, D7, E4, E5, E6, F6, G2

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Table 5-18. EPWM3 Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
EPWM3_1B	O	EPWM3 Output 1B	102, 114, 118, 120, 122, 28, 36, 38, 4, 40, 54, 60, 67, 69, 92, 93	A4, A5, A8, C10, C5, C9, F8, G1, H10, H6, J3, J8, K3, K4	21, 29, 31, 33, 39, 4, 45, 52, 54, 72, 73, 81, 86, 90, 92, 94	13, 21, 23, 25, 35, 37, 45, 46, 54, 56, 58, 60	B7, C5, C6, D2, D4, D5, E4, E7, F3, F7

Table 5-19. EPWM4 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
EPWM4_1A	O	EPWM4 Output 1A	106, 117, 119, 121, 123, 125, 15, 17, 2, 23, 24, 27, 29, 35, 41, 50, 57, 62, 68, 74, 80, 82, 87, 88, 89, 90, 92, 93, 97, 99	B4, B5, B8, C10, C3, C4, C7, C8, C9, D10, D2, D3, D9, E8, F1, F10, F2, F3, G2, H5, H9, J2, J4, J7, K9	10, 16, 17, 2, 20, 22, 28, 34, 42, 47, 53, 59, 65, 67, 68, 69, 70, 72, 73, 78, 89, 91, 93, 95, 97	10, 12, 14, 20, 26, 30, 36, 38, 40, 41, 42, 43, 45, 46, 51, 57, 59, 61, 9	A3, A4, A5, B4, B7, C2, C6, C7, D3, D7, E6, F2, F4, G5
EPWM4_1B	O	EPWM4 Output 1B	102, 107, 116, 118, 121, 122, 14, 28, 29, 32, 36, 39, 4, 56, 65, 68, 69, 7, 75, 83, 88, 90, 91, 93, 96	A4, A5, A8, B10, B2, B4, B9, C10, C8, D9, F8, G1, G2, G3, H4, H7, H9, J10, K3	21, 22, 25, 29, 32, 4, 41, 50, 53, 54, 60, 68, 7, 70, 71, 73, 76, 81, 88, 90, 93, 94	13, 14, 17, 2, 21, 24, 33, 36, 37, 41, 43, 44, 46, 49, 54, 56, 59, 60	B3, B4, B6, B7, C5, C7, D2, D3, D4, D6, E1, E4, E6, E7, F5, G2

Table 5-20. EPWM5 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
EPWM5_1A	O	EPWM5 Output 1A	1, 117, 119, 120, 123, 124, 24, 26, 29, 36, 51, 59, 62, 76, 80, 81, 86, 87, 91, 96	B10, B3, B9, C4, C5, E8, E9, F1, G2, K3, K7, K9	1, 17, 19, 22, 29, 44, 47, 61, 65, 66, 67, 71, 76, 89, 91, 92, 95, 96	10, 14, 21, 30, 38, 39, 40, 44, 49, 57, 58, 61, 62	A3, A4, B6, C4, D3, D5, D6, E4, G5
EPWM5_1B	O	EPWM5 Output 1B	116, 119, 120, 121, 122, 124, 19, 2, 33, 39, 40, 58, 67, 69, 77, 84, 87, 97	A4, B3, B4, B8, C1, C5, E8, F8, H10, H4, H8, K2, K4	12, 2, 26, 32, 33, 43, 52, 54, 62, 67, 88, 91, 92, 93, 94, 96	18, 24, 25, 35, 37, 40, 5, 57, 58, 59, 60, 62	A4, B4, C1, C4, D4, D5, E3, E7, F3, F7, G2

Table 5-21. ESC Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
ESC_GPI0	IO	ESC_GPI0	56	H7	41		

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Table 5-21. ESC Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
ESC_GPI1	IO	ESC_GPI1	57	J7	42		
ESC_GPI2	IO	ESC_GPI2	58, 62	H8, K9	43, 47	30	G5
ESC_GPI3	IO	ESC_GPI3	59	K7	44		
ESC_GPO0	IO	ESC_GPO0	61, 73	G10, K8	46, 58		
ESC_GPO1	IO	ESC_GPO1	70, 84	G9	55		
ESC_GPO2	IO	ESC_GPO2	71, 85	E10, F9	56		
ESC_GPO3	IO	ESC_GPO3	72		57		
ESC_I2C_SCL	IO	ESC_I2C_SCL	123, 2, 22, 81	C4, E2	15, 2, 66, 95	39, 61, 8	A3
ESC_I2C_SDA	IO	ESC_I2C_SDA	1, 23, 80, 89	D10, F2	1, 16, 65, 69	38, 42, 9	D7
ESC_LATCH0	IO	ESC_LATCH0	101, 52, 88	C6, D9	68, 80	41, 53	
ESC_LATCH1	IO	ESC_LATCH1	53	K6	38		
ESC_LED_ERR	IO	ESC_LED_ERR	25	E3	18	11	
ESC_LED_LINK0_ACTIVE	IO	ESC_LED_LINK0_ACTIVE	100, 26	B7	19, 79	52	
ESC_LED_LINK1_ACTIVE	IO	ESC_LED_LINK1_ACTIVE	126, 27	A3, F3	20, 98	12	C2
ESC_LED_RUN	IO	ESC_LED_RUN	24	F1	17	10	
ESC_LED_STATE_RUN	IO	ESC_LED_STATE_RUN	41	J4	34	26	F4
ESC_MDIO_CLK	IO	ESC_MDIO_CLK	10, 104, 108, 112	A6, B6	82, 84	55	
ESC_MDIO_DATA	IO	ESC_MDIO_DATA	101, 105, 11, 113	C6	80, 85	53	
ESC_PDI_UC_IRQ	IO	ESC_PDI_UC_IRQ	106, 113, 74	B5, F10	59, 85		
ESC_PHY0_LINKSTATUS	IO	ESC_PHY0_LINKSTATUS	54, 97	B8, H6	39		
ESC_PHY1_LINKSTATUS	IO	ESC_PHY1_LINKSTATUS	126, 55	A3, J6	40, 98		
ESC_PHY_CLK	IO	ESC_PHY_CLK	114, 125, 14, 24	C3, F1	17, 86, 97	10	
ESC_PHY_RESETn	IO	ESC_PHY_RESETn	23, 91	B9, F2	16, 71	44, 9	D6
ESC_RX0_CLK	I	ESC_RX0_CLK	112, 115, 28	A6, G1	21, 84, 87	13, 55	D2
ESC_RX0_DV	I	ESC_RX0_DV	113, 116, 29	G2	22, 85, 88	14	D3
ESC_RX0_ERR	I	ESC_RX0_ERR	109, 114, 32	A7, G3	25, 83, 86	17	E1
ESC_RX1_CLK	I	ESC_RX1_CLK	115, 126, 15, 9	A3, C2, D3	87, 9, 98	4	B1
ESC_RX1_DV	I	ESC_RX1_DV	10, 116, 16		88		
ESC_RX1_ERR	I	ESC_RX1_ERR	17, 8	D2	10, 8	3	C3
ESC_RX0_DATA0	I	ESC_RX0_DATA0	114, 117, 33	K2	26, 86, 89	18	E3
ESC_RX0_DATA1	I	ESC_RX0_DATA1	104, 115, 34	H2	27, 87	19	E5
ESC_RX0_DATA2	I	ESC_RX0_DATA2	105, 116, 35	J2	28, 88	20	F2
ESC_RX0_DATA3	I	ESC_RX0_DATA3	106, 117, 36	B5, K3	29, 89	21	E4
ESC_RX1_DATA0	I	ESC_RX1_DATA0	11, 14, 18		11		
ESC_RX1_DATA1	I	ESC_RX1_DATA1	102, 11, 14, 19, 99	A8, C1, C7	12, 78, 81	5, 51, 54	A5, C1
ESC_RX1_DATA2	I	ESC_RX1_DATA2	100, 105, 15, 20	B7, D1, D3	13, 79	52, 6	D1
ESC_RX1_DATA3	I	ESC_RX1_DATA3	16, 22	E2, H5	15	8	
ESC_SYNC0	IO	ESC_SYNC0	8		8	3	C3

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Table 5-21. ESC Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
ESC_SYNC1	IO	ESC_SYNC1	103, 9	C2	9	4	B1
ESC_TX0_CLK	I	EtherCAT MII Transmit-0 Clock	105, 112, 38	A6, J3	31, 84	23, 55	
ESC_TX0_ENA	O	ESC_TX0_ENA	104, 109, 37	A7, H3	30, 83	22	
ESC_TX1_CLK	O	ESC_TX1_CLK	100, 5, 51	B7	5, 79	52	
ESC_TX1_ENA	O	ESC_TX1_ENA	50, 7, 99	B2, C7	7, 78	2, 51	A5, B3
ESC_TX0_DATA0	O	ESC_TX0_DATA0	107, 39	H4	32	24	G2
ESC_TX0_DATA1	O	ESC_TX0_DATA1	103, 40, 97	B8, K4	33	25	F3
ESC_TX0_DATA2	O	ESC_TX0_DATA2	102, 48, 60, 68, 97	A8, B8, H9, J8	45, 53, 81	36, 54	E6
ESC_TX0_DATA3	O	EtherCAT MII Transmit-0 Data-3	100, 102, 49, 98	A8, A9, B7	77, 79, 81	50, 52, 54	B5
ESC_TX1_DATA0	O	ESC_TX1_DATA0	4, 7	B2	4, 7	2	B3
ESC_TX1_DATA1	O	ESC_TX1_DATA1	3, 5, 72, 77, 85	E10	3, 5, 57, 62		
ESC_TX1_DATA2	O	ESC_TX1_DATA2	2, 4, 71, 76	E9, F9	2, 4, 56, 61		
ESC_TX1_DATA3	O	ESC_TX1_DATA3	1, 3, 70, 75	G9	1, 3, 55, 60		

Table 5-22. FSI Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
FSIRX0_CLK	I	FSIRX0_CLK	106, 35, 88	B5, D9, J2	28, 68	20, 41	F2
FSIRX0_D0	I	FSIRX0_D0	104, 120, 33, 86	C5, K2	26, 92	18, 58	D5, E3
FSIRX0_D1	I	FSIRX0_D1	105, 34, 87, 91	B9, E8, H2	27, 67, 71	19, 40, 44	D6, E5
FSITX0_CLK	IO	FSITX0_CLK	9	C2	9	4	B1
FSITX0_D0	IO	FSITX0_D0	65, 7	B2, J10	50, 7	2, 33	B3, F5
FSITX0_D1	IO	FSITX0_D1	8, 9	C2	8, 9	3, 4	B1, C3

Table 5-23. FSITX0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
FSITX0_CLK	IO	FSITX0_CLK	67	H10	52	35	F7
FSITX0_D0	IO	FSITX0_D0	126	A3	98		
FSITX0_D1	IO	FSITX0_D1	66	J9	51	34	F6

Table 5-24. GPIO Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
GPIO00	IO	General Purpose Input/Output 0 (Wakeup0)	27	F3	20	12	C2
GPIO01	IO	General Purpose Input/Output 1	28	G1	21	13	D2
GPIO02	IO	General Purpose Input/Output 2 (Wakeup3)	29	G2	22	14	D3
GPIO03	IO	General Purpose Input/Output 3	32	G3	25	17	E1

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Table 5-24. GPIO Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
GPIO04	IO	General Purpose Input/Output 4	33	K2	26	18	E3
GPIO05	IO	General Purpose Input/Output 5	34	H2	27	19	E5
GPIO06	IO	General Purpose Input/Output 6	35	J2	28	20	F2
GPIO07	IO	General Purpose Input/Output 7	36	K3	29	21	E4
GPIO08	IO	General Purpose Input/Output 8	89	D10	69	42	D7
GPIO09	IO	General Purpose Input/Output 9	90	C8	70	43	C7
GPIO10	IO	General Purpose Input/Output 10	91	B9	71	44	D6
GPIO11	IO	General Purpose Input/Output 11	92	C9	72	45	C6
GPIO12	IO	General Purpose Input/Output 12	93	C10	73	46	B7
GPIO13	IO	General Purpose Input/Output 13	96	B10	76	49	B6
GPIO14	IO	General Purpose Input/Output 14	98	A9	77	50	B5
GPIO15	IO	General Purpose Input/Output 15	99	C7	78	51	A5
GPIO16	IO	General Purpose Input/Output 16	39	H4	32	24	G2
GPIO17	IO	General Purpose Input/Output 17	40	K4	33	25	F3
GPIO18	IO	General Purpose Input/Output 18	41	J4	34	26	F4
GPIO19	IO	General Purpose Input/Output 19	118	A5	90	56	C5
GPIO100	IO	General Purpose Input/Output 100	86				
GPIO101	IO	General Purpose Input/Output 101	103				
GPIO102	IO	General Purpose Input/Output 102	104				
GPIO103	IO	General Purpose Input/Output 103	105				
GPIO104	IO	General Purpose Input/Output 104	106	B5			
GPIO105	IO	General Purpose Input/Output 105	107				
GPIO112	IO	General Purpose Input/Output 112		H5			
GPIO20	IO	General Purpose Input/Output 20	119		91	57	A4
GPIO21	IO	General Purpose Input/Output 21	120	C5	92	58	D5
GPIO22	IO	General Purpose Input/Output 22	121	B4	93	59	B4
GPIO23	IO	General Purpose Input/Output 23	122	A4	94	60	D4
GPIO24	IO	General Purpose Input/Output 24	123	C4	95	61	A3
GPIO25	IO	General Purpose Input/Output 25	124	B3	96	62	C4
GPIO26	IO	General Purpose Input/Output 26	62	K9	47	30	G5
GPIO27	IO	General Purpose Input/Output 27	65	J10	50	33	F5
GPIO28	IO	General Purpose Input/Output 28	66	J9	51	34	F6
GPIO29	IO	General Purpose Input/Output 29	67	H10	52	35	F7
GPIO30	IO	General Purpose Input/Output 30	68	H9	53	36	E6
GPIO31	IO	General Purpose Input/Output 31	69	F8	54	37	E7
GPIO32	IO	General Purpose Input/Output 32	22	E2	15	8	
GPIO33	IO	General Purpose Input/Output 33 (Wakeup5)	23	F2	16	9	
GPIO34	IO	General Purpose Input/Output 34	24	F1	17	10	

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Table 5-24. GPIO Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
GPIO35	IO	General Purpose Input/Output 35	25	E3	18	11	
GPIO36	IO	General Purpose Input/Output 36	37	H3	30	22	
GPIO37	IO	General Purpose Input/Output 37 (Wakeup4)	38	J3	31	23	
GPIO38	IO	General Purpose Input/Output 38	80		65	38	
GPIO39	IO	General Purpose Input/Output 39	81		66	39	
GPIO40	IO	General Purpose Input/Output 40	87	E8	67	40	
GPIO41	IO	General Purpose Input/Output 41	88	D9	68	41	
GPIO42	IO	General Purpose Input/Output 42	100	B7	79	52	
GPIO43	IO	General Purpose Input/Output 43	101	C6	80	53	
GPIO44	IO	General Purpose Input/Output 44	102	A8	81	54	
GPIO45	IO	General Purpose Input/Output 45 (Wakeup1)	7	B2	7	2	B3
GPIO46	IO	General Purpose Input/Output 46	8		8	3	C3
GPIO47	IO	General Purpose Input/Output 47	9	C2	9	4	B1
GPIO48	IO	General Purpose Input/Output 48	108	B6	82		
GPIO49	IO	General Purpose Input/Output 49	109	A7	83		
GPIO50	IO	General Purpose Input/Output 50 (Wakeup6)	112	A6	84	55	
GPIO51	IO	General Purpose Input/Output 51 (Wakeup7)	113		85		
GPIO52	IO	General Purpose Input/Output 52	114		86		
GPIO53	IO	General Purpose Input/Output 53	115		87		
GPIO54	IO	General Purpose Input/Output 54	116		88		
GPIO55	IO	General Purpose Input/Output 55	117		89		
GPIO56	IO	General Purpose Input/Output 56	70	G9	55		
GPIO57	IO	General Purpose Input/Output 57	71	F9	56		
GPIO58	IO	General Purpose Input/Output 58	72		57		
GPIO59	IO	General Purpose Input/Output 59	73	G10	58		
GPIO60	IO	General Purpose Input/Output 60	74	F10	59		
GPIO61	IO	General Purpose Input/Output 61	75		60		
GPIO62	IO	General Purpose Input/Output 62	76	E9	61		
GPIO63	IO	General Purpose Input/Output 63	77		62		
GPIO64	IO	General Purpose Input/Output 64	125	C3	97		
GPIO65	IO	General Purpose Input/Output 65	126	A3	98		
GPIO66	IO	General Purpose Input/Output 66	1		1		
GPIO67	IO	General Purpose Input/Output 67	2		2		
GPIO68	IO	General Purpose Input/Output 68	3		3		
GPIO69	IO	General Purpose Input/Output 69	4		4		
GPIO70	IO	General Purpose Input/Output 70 (Wakeup2)	5		5		
GPIO71	IO	General Purpose Input/Output 71	53	K6	38		
GPIO72	IO	General Purpose Input/Output 72	54	H6	39		
GPIO73	IO	General Purpose Input/Output 73	55	J6	40		
GPIO74	IO	General Purpose Input/Output 74	56	H7	41		

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Table 5-24. GPIO Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
GPIO75	IO	General Purpose Input/Output 75	57	J7	42		
GPIO76	IO	General Purpose Input/Output 76	58	H8	43		
GPIO77	IO	General Purpose Input/Output 77	59	K7	44		
GPIO78	IO	General Purpose Input/Output 78	60	J8	45		
GPIO79	IO	General Purpose Input/Output 79	61	K8	46		
GPIO80	IO	General Purpose Input/Output 80	19	C1	12	5	C1
GPIO81	IO	General Purpose Input/Output 81	20	D1	13	6	D1
GPIO82	IO	General Purpose Input/Output 82	26		19		
GPIO83	IO	General Purpose Input/Output 83	10				
GPIO84	IO	General Purpose Input/Output 84	11				
GPIO85	IO	General Purpose Input/Output 85	14				
GPIO86	IO	General Purpose Input/Output 86	97	B8			
GPIO87	IO	General Purpose Input/Output 87	15	D3			
GPIO88	IO	General Purpose Input/Output 88	16				
GPIO89	IO	General Purpose Input/Output 89	17	D2	10		
GPIO90	IO	General Purpose Input/Output 90	18		11		
GPIO91	IO	General Purpose Input/Output 91	48				
GPIO92	IO	General Purpose Input/Output 92	49				
GPIO93	IO	General Purpose Input/Output 93	50				
GPIO94	IO	General Purpose Input/Output 94	51				
GPIO95	IO	General Purpose Input/Output 95	52				
GPIO96	IO	General Purpose Input/Output 96	82				
GPIO97	IO	General Purpose Input/Output 97	83				
GPIO98	IO	General Purpose Input/Output 98	84				
GPIO99	IO	General Purpose Input/Output 99	85	E10			

Table 5-25. GROUND Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
VSS	GND	Digital Ground	110, 12, 127, 46, 63, 78, 94	A10, B1, D4, D5, D6, D7, E4, E5, E6, E7, F4, F5, F6, F7, G4, G5, G6, G7, K10	48, 63, 74, 99	31, 47, 63	A2, A6, G6
VSSA	AGND	Analog Ground	30	H1, K1	23	15	F1

Table 5-26. MCAN Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
MCAN0_RX	IO	MCAN0_RX	34	H2	27	19	E5
MCAN1_RX	IO	MCAN1_RX	118, 120, 24, 27	A5, C5, F1, F3	17, 20, 90, 92	10, 12, 56, 58	C2, C5, D5

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Table 5-26. MCAN Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
MCAN1_TX	IO	MCAN1_TX	119, 25, 28, 49	E3, G1	18, 21, 91	11, 13, 57	A4, D2

Table 5-27. MCAN0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
MCAN0_RX	I	CAN Receive (RX) Signal	109, 118, 120, 123, 37, 66, 8, 92, 99	A5, A7, C4, C5, C7, C9, H3, J9	30, 51, 72, 78, 8, 83, 90, 92, 95	22, 3, 34, 45, 51, 56, 58, 61	A3, A5, C3, C5, C6, D5, F6
MCAN0_TX	O	CAN Transmit (TX) Signal	108, 119, 121, 124, 38, 67, 89, 9, 93	B3, B4, B6, C10, C2, D10, H10, J3	31, 52, 69, 73, 82, 9, 91, 93, 96	23, 35, 4, 42, 46, 57, 59, 62	A4, B1, B4, B7, C4, D7, F7

Table 5-28. MCAN1 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
MCAN1_RX	IO	MCAN1_RX	108	B6	82		
MCAN1_TX	IO	MCAN1_TX	109, 121	A7, B4	83, 93	59	B4

Table 5-29. MCPWM Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
MCPWM1_1A	O	MCPWM1 Output 1A		H5			
MCPWM1_3A	O	MCPWM1_3A	112	A6, H5	84	55	
MCPWM2_2A	O	EPWM2 Output 2A		H5			

Table 5-30. MCPWM0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
MCPWM0_1A	O	MCPWM0 Output 1A	22, 25, 55, 60, 61, 89, 92	C9, D10, E2, E3, J6, J8, K8	15, 18, 40, 45, 46, 69, 72	11, 42, 45, 8	C6, D7
MCPWM0_1B	O	MCPWM0 Output 1B	36, 38, 54, 56, 60, 67, 7, 92, 93	B2, C10, C9, H10, H6, H7, J3, J8, K3	29, 31, 39, 41, 45, 52, 7, 72, 73	2, 21, 23, 35, 45, 46	B3, B7, C6, E4, F7
MCPWM0_2A	O	MCPWM0 Output 2A	23, 57, 90	C8, F2, J7	16, 42, 70	43, 9	C7
MCPWM0_2B	O	MCPWM0 Output 2B	39, 54, 56, 68, 93	C10, H4, H6, H7, H9	32, 39, 41, 53, 73	24, 36, 46	B7, E6, G2
MCPWM0_3A	O	MCPWM0 Output 3A	24, 59, 91	B9, F1, K7	17, 44, 71	10, 44	D6
MCPWM0_3B	O	MCPWM0 Output 3B	124, 19, 40, 55, 58, 69	B3, C1, F8, H8, J6, K4	12, 33, 40, 43, 54, 96	25, 37, 5, 62	C1, C4, E7, F3

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Table 5-31. MCPWM1 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
MCPWM1_1A	O	MCPWM1 Output 1A	109, 121, 80, 88, 99	A7, B4, C7, D9	65, 68, 78, 83, 93	38, 41, 51, 59	A5, B4
MCPWM1_1B	O	MCPWM1 Output 1B	100, 108, 118, 36, 7	A5, B2, B6, B7, K3	29, 7, 79, 82, 90	2, 21, 52, 56	B3, C5, E4
MCPWM1_2A	O	MCPWM1 Output 2A	123, 81, 98	A9, C4	66, 77, 95	39, 50, 61	A3, B5
MCPWM1_2B	O	MCPWM1 Output 2B	101, 119, 39	C6, H4	32, 80, 91	24, 53, 57	A4, G2
MCPWM1_3A	O	MCPWM1 Output 3A	124, 87	B3, E8	67, 96	40, 62	C4
MCPWM1_3B	O	MCPWM1 Output 3B	102, 120, 40	A8, C5, K4	33, 81, 92	25, 54, 58	D5, F3

Table 5-32. MCPWM2 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
MCPWM2_1A	O	MCPWM2 Output 1A	1, 10, 126, 41, 49, 52	A3, J4	1, 34, 98	26	F4
MCPWM2_1B	O	MCPWM2 Output 1B	11, 125, 3, 34, 40, 82, 85	C3, E10, H2, K4	27, 3, 33, 97	19, 25	E5, F3
MCPWM2_2A	O	MCPWM2 Output 2A	121, 15, 2, 24, 50, 74, 92	B4, C9, D3, F1, F10	17, 2, 59, 72, 93	10, 45, 59	B4, C6
MCPWM2_2B	O	MCPWM2 Output 2B	122, 14, 4, 75, 83, 93	A4, C10	4, 60, 73, 94	46, 60	B7, D4
MCPWM2_3A	O	MCPWM2 Output 3A	123, 26, 51, 76, 87, 96	B10, C4, E8, E9	19, 61, 67, 76, 95	40, 49, 61	A3, B6
MCPWM2_3B	O	MCPWM2 Output 3B	124, 5, 77, 84, 97	B3, B8	5, 62, 96	62	C4

Table 5-33. OUTPUTXBAR Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
OUTPUTXBAR1	O	Output X-BAR Output (Group 1)	1, 107, 117, 125, 18, 36, 39, 53, 61, 76, 8, 86, 99	C3, C7, E9, H4, K3, K6, K8	1, 11, 29, 32, 38, 46, 61, 78, 8, 89, 97	21, 24, 3, 51	A5, C3, E4, G2
OUTPUTXBAR2	O	Output X-BAR Output (Group 2)	100, 108, 118, 126, 19, 2, 37, 40, 54, 62, 69, 77, 87, 9, 97	A3, A5, B6, B7, B8, C1, C2, E8, F8, H3, H6, K4, K9	12, 2, 30, 33, 39, 47, 54, 62, 67, 79, 82, 9, 90, 98	22, 25, 30, 37, 4, 40, 5, 52, 56	B1, C1, C5, E7, F3, G5
OUTPUTXBAR3	O	Output X-BAR Output (Group 3)	10, 101, 109, 119, 20, 3, 38, 41, 55, 65, 70, 80, 88, 89	A7, C6, D1, D10, D9, G9, J10, J3, J4, J6	13, 3, 31, 34, 40, 50, 55, 65, 68, 69, 80, 83, 91	23, 26, 33, 38, 41, 42, 53, 57, 6	A4, D1, D7, F4, F5
OUTPUTXBAR4	O	Output X-BAR Output (Group 4)	102, 11, 112, 120, 28, 4, 48, 56, 66, 71, 81, 90	A6, A8, C5, C8, F9, G1, H7, J9	21, 4, 41, 51, 56, 66, 70, 81, 84, 92	13, 34, 39, 43, 54, 55, 58	C7, D2, D5, F6

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Table 5-33. OUTPUTXBAR Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
OUTPUTXBAR5	O	Output X-BAR Output (Group 5)	103, 113, 121, 14, 22, 29, 49, 5, 57, 67, 72, 82, 92	B4, C9, E2, G2, H10, J7	15, 22, 42, 5, 52, 57, 72, 85, 93	14, 35, 45, 59, 8	B4, C6, D3, F7
OUTPUTXBAR6	O	Output X-BAR Output (Group 6)	104, 114, 122, 15, 23, 32, 33, 50, 58, 68, 7, 73, 83, 93	A4, B2, C10, D3, F2, G10, G3, H8, H9, K2	16, 25, 26, 43, 53, 58, 7, 73, 86, 94	17, 18, 2, 36, 46, 60, 9	B3, B7, D4, E1, E3, E6
OUTPUTXBAR7	O	Output X-BAR Output (Group 7)	105, 115, 123, 124, 16, 24, 26, 34, 51, 59, 74, 84, 96	B10, B3, C4, F1, F10, H2, H5, K7	17, 19, 27, 44, 59, 76, 87, 95, 96	10, 19, 49, 61, 62	A3, B6, C4, E5
OUTPUTXBAR8	O	Output X-BAR Output (Group 8)	106, 116, 17, 25, 27, 35, 52, 60, 75, 85, 91, 98	A9, B5, B9, D2, E10, E3, F3, J2, J8	10, 18, 20, 28, 45, 60, 71, 77, 88	11, 12, 20, 44, 50	B5, C2, D6, F2

Table 5-34. PGA0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
PGA0_OUT	A	PGA0 Output	29	G2	22	14	D3
PGA0_M0	A	PGA0 Negative (-) Input 0	32	G3	25	17	E1
PGA0_M1	A	PGA0 Negative (-) Input 1	38	J3	31	23	
PGA0_M2	A	PGA0 Negative (-) Input 2	62	K9	47	30	G5
PGA0_M3	A	PGA0 Negative (-) Input 3	70	G9	55		
PGA0_P0	A	PGA0 Positive (+) Input 0	25	E3	18	11	
PGA0_P1	A	PGA0 Positive (+) Input 1	28	G1	21	13	D2
PGA0_P2	A	PGA0 Positive (+) Input 2	32	G3	25	17	E1
PGA0_P3	A	PGA0 Positive (+) Input 3	36	K3	29	21	E4
PGA0_P4	A	PGA0 Positive (+) Input 4	65	J10	50	33	F5
PGA0_P5	A	PGA0 Positive (+) Input 5	67	H10	52	35	F7
PGA0_P6	A	PGA0 Positive (+) Input 6	73	G10	58		
PGA0_P7	A	PGA0 Positive (+) Input 7	66	J9	51	34	F6
PGA0_P8	A	PGA0 Positive (+) Input 8	74	F10	59		

Table 5-35. PGA1 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
PGA1_OUT	A	PGA1 Output	35	J2	28	20	F2
PGA1_M0	A	PGA1 Negative (-) Input 0	28	G1	21	13	D2
PGA1_M1	A	PGA1 Negative (-) Input 1	34	H2	27	19	E5
PGA1_M2	A	PGA1 Negative (-) Input 2	38	J3	31	23	
PGA1_M3	A	PGA1 Negative (-) Input 3	40	K4	33	25	F3
PGA1_P0	A	PGA1 Positive (+) Input 0	25	E3	18	11	

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Table 5-35. PGA1 Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
PGA1_P1	A	PGA1 Positive (+) Input 1	36	K3	29	21	E4
PGA1_P2	A	PGA1 Positive (+) Input 2	39	H4	32	24	G2
PGA1_P3	A	PGA1 Positive (+) Input 3	66	J9	51	34	F6
PGA1_P4	A	PGA1 Positive (+) Input 4	67	H10	52	35	F7
PGA1_P5	A	PGA1 Positive (+) Input 5	68	H9	53	36	E6
PGA1_P6	A	PGA1 Positive (+) Input 6	71	F9	56		
PGA1_P7	A	PGA1 Positive (+) Input 7	76	E9	61		
PGA1_P8	A	PGA1 Positive (+) Input 8	73	G10	58		

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Table 5-36. PGA2 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
PGA2_OUT	A	PGA2 Output	40	K4	33	25	F3
PGA2_M0	A	PGA2 Negative (-) Input 0	32	G3	25	17	E1
PGA2_M1	A	PGA2 Negative (-) Input 1	41	J4	34	26	F4
PGA2_M2	A	PGA2 Negative (-) Input 2	62	K9	47	30	G5
PGA2_M3	A	PGA2 Negative (-) Input 3	69	F8	54	37	E7
PGA2_P0	A	PGA2 Positive (+) Input 0	65	J10	50	33	F5
PGA2_P1	A	PGA2 Positive (+) Input 1	25	E3	18	11	
PGA2_P2	A	PGA2 Positive (+) Input 2	28	G1	21	13	D2
PGA2_P3	A	PGA2 Positive (+) Input 3	39	H4	32	24	G2
PGA2_P4	A	PGA2 Positive (+) Input 4	67	H10	52	35	F7
PGA2_P5	A	PGA2 Positive (+) Input 5	68	H9	53	36	E6
PGA2_P6	A	PGA2 Positive (+) Input 6	74	F10	59		
PGA2_P7	A	PGA2 Positive (+) Input 7	71	F9	56		
PGA2_P8	A	PGA2 Positive (+) Input 8	73	G10	58		

Table 5-37. POWER Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
VDD	PWR	VDD	111, 128, 13, 47, 6, 64, 79, 95	A2, D8, G8	100, 49, 6, 64, 75	1, 32, 48, 64	A1, A7, G7
VDDA	APWR	3.3V Analog Power Pin	31, 45	J1	24, 37	16, 29	G1

Table 5-38. SD Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
SD0_C1	IO	SD0_C1	101, 116, 19, 71, 90	C1, C6, C8, F9	12, 56, 70, 80, 88	43, 5, 53	C1, C7
SD0_C2	IO	SD0_C2	126, 33, 89	A3, D10, K2	26, 69, 98	18, 42	D7, E3
SD0_C3	IO	SD0_C3	1, 123, 69, 72	C4, F8	1, 54, 57, 95	37, 61	A3, E7

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Table 5-38. SD Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
SD0_C4	IO	SD0_C4	112, 118, 90	A5, A6, C8	70, 84, 90	43, 55, 56	C5, C7
SD0_D1	IO	SD0_D1	102, 117, 20, 70, 91	A8, B9, D1, G9	13, 55, 71, 81, 89	44, 54, 6	D1, D6
SD0_D2	IO	SD0_D2	34, 90	C8, H2	27, 70	19, 43	C7, E5
SD0_D3	IO	SD0_D3	124, 2, 68, 73	B3, G10, H9	2, 53, 58, 96	36, 62	C4, E6
SD0_D4	IO	SD0_D4	113, 119, 89	D10	69, 85, 91	42, 57	A4, D7

Table 5-39. SD0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
SD0_D1	I	SDFM-0 Channel 1 Data Input	73	G10	58		

Table 5-40. SYSCTL Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
NRST	RST	Device Reset (NRST)	21	E1	14	7	B2
SYSCTL	IO	SYSCTL	21	E1	14	7	B2
SYSCTL_FCC_IN	I	Frequency Clock Counter (FCC) Input Signal	1, 10, 39, 67, 7, 96	B10, B2, H10, H4	1, 32, 52, 7, 76	2, 24, 35, 49	B3, B6, F7, G2
SYSCTL_HFCLKIN	A	External Clock Input	19, 32	C1, G3	12, 25	17, 5	C1, E1
SYSCTL_X1	A	Crystal (XTAL) Input (X1) or Single-ended Clock Input	19	C1	12	5	C1
SYSCTL_X2	A	Crystal (XTAL) Output (X2)	20	D1	13	6	D1
SYSCTL_XCLKOUT	O	External Clock Output. This pin outputs an (optionally) divided-down version of a chosen clock signal from within the device.	18, 33, 65, 7, 8	B2, J10, K2	11, 26, 50, 7, 8	18, 2, 3, 33	B3, C3, E3, F5

Table 5-41. TIMER Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
TIMG12_0_CCP0	IO	TIMG12_0 Capture/Compare0 Signal	27, 32, 62, 66	F3, G3, J9, K9	20, 25, 47, 51	12, 17, 30, 34	C2, E1, F6, G5
TIMG12_0_CCP1	IO	TIMG12_0 Capture/Compare1 Signal	28, 33, 65, 67	G1, H10, J10, K2	21, 26, 50, 52	13, 18, 33, 35	D2, E3, F5, F7
TIMG4_0_CCP0	IO	TIMG4_0 Capture/Compare0 Signal	27, 32, 62, 66, 72, 74, 76	E9, F10, F3, G3, J9, K9	20, 25, 47, 51, 57, 59, 61	12, 17, 30, 34	C2, E1, F6, G5
TIMG4_0_CCP1	IO	TIMG4_0 Capture/Compare1 Signal	28, 33, 65, 67, 73, 75, 77	G1, G10, H10, J10, K2	21, 26, 50, 52, 58, 60, 62	13, 18, 33, 35	D2, E3, F5, F7

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Table 5-42. TRACE Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
TRACE_CLK	IO	Trace Clock	1, 101	C6	1, 80	53	
TRACE_DATA0	O	TRACE_DATA0	108, 126, 2	A3, B6	2, 82, 98		
TRACE_DATA1	O	Trace Data 1	3, 87	E8	3, 67	40	
TRACE_DATA2	O	Trace Data 2	112, 4	A6	4, 84	55	
TRACE_DATA3	O	Trace Data 3	102, 112, 5	A6, A8	5, 81, 84	54, 55	

Table 5-43. UC Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
UC1_RTS_POCI	IO	UC1_RTS_POCI	40, 7	B2, K4	33, 7	2, 25	B3, F3
UC1_RX_SCL_SCLK	IO	UC1_RX_SCL_SCLK	112	A6	84	55	
UC1_TX_SDA_PICO	IO	UC1_TX_SDA_PICO	109, 17	A7, D2	10, 83		
UC2_RX_SCL	IO	UC2_RX_SCL	65	J10	50	33	F5
UC1_CTS_CS0	IO	UC1_CTS_CS0	39	H4	32	24	G2

Table 5-44. UC0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
UC0_RTS_POCI	O	UNICOMM0 RTS: UART Release To Send POCI: SPI Peripheral Out - Controller In	103, 104, 119, 2, 28, 3, 33, 35, 40, 53, 57, 66, 68, 74, 93, 97, 99	B8, C10, C7, F10, G1, H9, J2, J7, J9, K2, K4, K6	2, 21, 26, 28, 3, 33, 38, 42, 51, 53, 59, 73, 78, 91	13, 18, 20, 25, 34, 36, 46, 51, 57	A4, A5, B7, D2, E3, E6, F2, F3, F6
UC0_RX_SCL_SCLK	IO	UNICOMM0 RX: UART Receive SCL: I2C Clock SCLK: SPI Clock	1, 10, 100, 101, 102, 105, 106, 112, 118, 120, 122, 123, 124, 126, 22, 32, 34, 38, 51, 58, 61, 62, 65, 84, 87, 89, 9, 91, 96, 99	A3, A4, A5, A6, A8, B10, B3, B5, B7, B9, C2, C4, C5, C6, C7, D10, E2, E8, G3, H2, H8, J10, J3, K8, K9	1, 15, 25, 27, 31, 43, 46, 47, 50, 67, 69, 71, 76, 78, 79, 80, 81, 84, 9, 90, 92, 94, 95, 96, 98	17, 19, 23, 30, 33, 4, 40, 42, 44, 49, 51, 52, 53, 54, 55, 56, 58, 60, 61, 62, 8	A3, A5, B1, B6, C4, C5, D4, D5, D6, D7, E1, E5, F5, G5
UC0_TX_SDA_PICO	O	UNICOMM0 TX: UART Transmit SDA: I2C Data PICO: SPI Peripheral In - Controller Out	100, 101, 102, 105, 106, 107, 11, 112, 120, 121, 122, 123, 124, 125, 23, 29, 36, 37, 5, 52, 60, 61, 62, 65, 8, 86, 88, 90, 98	A4, A6, A8, A9, B3, B4, B5, B7, C3, C4, C5, C6, C8, D9, F2, G2, H3, J10, J8, K3, K8, K9	16, 22, 29, 30, 45, 46, 47, 5, 50, 68, 70, 77, 79, 8, 80, 81, 84, 92, 93, 94, 95, 96, 97	14, 21, 22, 3, 30, 33, 41, 43, 50, 52, 53, 54, 55, 58, 59, 60, 61, 62, 9	A3, B4, B5, C3, C4, C7, D3, D4, D5, E4, F5, G5

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Table 5-44. UC0 Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
UC0_CTS_CS0	IO	UNICOMM0 CTS: UART Clear To Send CS0: SPI Chip Select 0	101, 103, 119, 120, 27, 35, 4, 50, 59, 66, 67, 73, 85, 92, 96	B10, C5, C6, C9, E10, F3, G10, H10, J2, J9, K7	20, 28, 4, 44, 51, 52, 58, 72, 76, 80, 91, 92	12, 20, 34, 35, 45, 49, 53, 57, 58	A4, B6, C2, C6, D5, F2, F6, F7

Table 5-45. UC1 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
UC1_RTS_POCI	O	UNICOMM1 RTS: UART Release To Send POCI: SPI Peripheral Out - Controller In	104, 114, 15, 19, 28, 66, 77	C1, D3, G1, J9	12, 21, 51, 62, 86	13, 34, 5	C1, D2, F6
UC1_RX_SCL_SCLK	IO	UNICOMM1 RX: UART Receive SCL: I2C Clock SCLK: SPI Clock	106, 11, 116, 119, 17, 18, 20, 28, 32, 37, 90, 97, 99	B5, B8, C7, C8, D1, D2, G1, G3, H3	10, 11, 13, 21, 25, 30, 70, 78, 88, 91	13, 17, 22, 43, 51, 57, 6	A4, A5, C7, D1, D2, E1
UC1_TX_SDA_PICO	O	UNICOMM1 TX: UART Transmit SDA: I2C Data PICO: SPI Peripheral In - Controller Out	10, 105, 115, 118, 19, 27, 29, 68, 89, 91, 98	A5, A9, B9, C1, D10, F3, G2, H9	12, 20, 22, 53, 69, 71, 77, 87, 90	12, 14, 36, 42, 44, 5, 50, 56	B5, C1, C2, C5, D3, D6, D7, E6
UC1_CTS_CS0	IO	UNICOMM1 CTS: UART Clear To Send CS0: SPI Chip Select 0	103, 113, 122, 16, 27, 69, 92	A4, C9, F3, F8, H5	20, 54, 72, 85, 94	12, 37, 45, 60	C2, C6, D4, E7

Table 5-46. UC2 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
UC2_CTS	O	UNICOMM2 CTS: UART Clear To Send	112, 17, 73, 83, 87, 98	A6, A9, D2, E8, G10	10, 58, 67, 77, 84	40, 50, 55	B5
UC2_RTS	O	UNICOMM2 RTS: UART Release To Send	113, 18, 33, 74, 82, 88, 90, 99	C7, C8, D9, F10, K2	11, 26, 59, 68, 70, 78, 85	18, 41, 43, 51	A5, C7, E3
UC2_RX_SCL	IO	UNICOMM2 RX: UART Receive SCL: I2C Clock	1, 101, 107, 109, 122, 15, 18, 20, 27, 51, 53, 70, 75, 76, 80, 85, 91	A4, A7, B9, C6, D1, D3, E10, E9, F3, G9, H5, K6	1, 11, 13, 20, 38, 55, 60, 61, 65, 71, 80, 83, 94	12, 38, 44, 53, 6, 60	C2, D1, D4, D6
UC2_TX_SDA	O	UNICOMM2 TX: UART Transmit SDA: I2C Data	100, 108, 121, 16, 17, 19, 2, 28, 52, 54, 71, 75, 76, 81, 86, 92	B4, B6, B7, C1, C9, D2, E9, F9, G1, H6	10, 12, 2, 21, 39, 56, 60, 61, 66, 72, 79, 82, 93	13, 39, 45, 5, 52, 59	B4, C1, C6, D2

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Table 5-47. UC3 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
UC3_RTS_POCI	O	UNICOMM3 RTS: UART Release To Send POCI: SPI Peripheral Out - Controller In	119, 2, 3, 33, 35, 40, 57, 74, 93, 97, 99	B8, C10, C7, F10, J2, J7, K2, K4	2, 26, 28, 3, 33, 42, 59, 73, 78, 91	18, 20, 25, 46, 51, 57	A4, A5, B7, E3, F2, F3
UC3_RX_SCL_SCLK	IO	UNICOMM3 RX: UART Receive SCL: I2C Clock SCLK: SPI Clock	1, 100, 101, 102, 105, 112, 118, 120, 122, 123, 124, 126, 22, 34, 38, 58, 61, 62, 65, 84, 87, 89, 9, 96	A3, A4, A5, A6, A8, B10, B3, B7, C2, C4, C5, C6, D10, E2, E8, H2, H8, J10, J3, K8, K9	1, 15, 27, 31, 43, 46, 47, 50, 67, 69, 76, 79, 80, 81, 84, 9, 90, 92, 94, 95, 96, 98	19, 23, 30, 33, 4, 40, 42, 49, 52, 53, 54, 55, 56, 58, 60, 61, 62, 8	A3, B1, B6, C4, C5, D4, D5, D7, E5, F5, G5
UC3_TX_SDA_PICO	O	UNICOMM3 TX: UART Transmit SDA: I2C Data PICO: SPI Peripheral In - Controller Out	100, 101, 102, 106, 107, 112, 118, 120, 121, 122, 123, 124, 125, 23, 36, 37, 5, 60, 61, 62, 65, 8, 86, 88	A4, A5, A6, A8, B3, B4, B5, B7, C3, C4, C5, C6, D9, F2, H3, J10, J8, K3, K8, K9	16, 29, 30, 45, 46, 47, 5, 50, 68, 79, 8, 80, 81, 84, 90, 92, 93, 94, 95, 96, 97	21, 22, 3, 30, 33, 41, 52, 53, 54, 55, 56, 58, 59, 60, 61, 62, 9	A3, B4, C3, C4, C5, D4, D5, E4, F5, G5
UC3_CTS_CS0	IO	UNICOMM3 CTS: UART Clear To Send CS0: SPI Chip Select 0	101, 119, 120, 35, 4, 59, 66, 67, 73, 85, 92, 96	B10, C5, C6, C9, E10, G10, H10, J2, J9, K7	28, 4, 44, 51, 52, 58, 72, 76, 80, 91, 92	20, 34, 35, 45, 49, 53, 57, 58	A4, B6, C6, D5, F2, F6, F7

Table 5-48. UC4 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
UC4_RTS_POCI	O	UNICOMM4 RTS: UART Release To Send POCI: SPI Peripheral Out - Controller In	114, 15, 19, 66, 68, 77	C1, D3, H9, J9	12, 51, 53, 62, 86	34, 36, 5	C1, E6, F6
UC4_RX_SCL_SCLK	IO	UNICOMM4 RX: UART Receive SCL: I2C Clock SCLK: SPI Clock	11, 116, 119, 18, 28, 37, 90, 91, 97	B8, B9, C8, G1, H3, H5	11, 21, 30, 70, 71, 88, 91	13, 22, 43, 44, 57	A4, C7, D2, D6
UC4_TX_SDA_PICO	O	UNICOMM4 TX: UART Transmit SDA: I2C Data PICO: SPI Peripheral In - Controller Out	10, 115, 17, 27, 68, 89, 90, 91	B9, C8, D10, D2, F3, H9	10, 20, 53, 69, 70, 71, 87	12, 36, 42, 43, 44	C2, C7, D6, D7, E6
UC4_CTS_CS0	IO	UNICOMM4 CTS: UART Clear To Send CS0: SPI Chip Select 0	113, 122, 16, 69, 92	A4, C9, F8	54, 72, 85, 94	37, 45, 60	C6, D4, E7

Table 5-49. UC5 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
UC5_CTS	O	UNICOMM5 CTS: UART Clear To Send	10, 112, 17, 73, 83, 88, 98	A6, A9, D2, D9, G10	10, 58, 68, 77, 84	41, 50, 55	B5

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Table 5-49. UC5 Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
UC5_RTS	O	UNICOMM5 RTS: UART Release To Send	11, 113, 18, 33, 74, 82, 87, 90, 99	C7, C8, E8, F10, K2	11, 26, 59, 67, 70, 78, 85	18, 40, 43, 51	A5, C7, E3
UC5_RX_SCL	IO	UNICOMM5 RX: UART Receive SCL: I2C Clock	1, 10, 101, 107, 109, 122, 15, 17, 27, 51, 53, 70, 75, 76, 80, 85, 91	A4, A7, B9, C6, D2, D3, E10, E9, F3, G9, K6	1, 10, 20, 38, 55, 60, 61, 65, 71, 80, 83, 94	12, 38, 44, 53, 60	C2, D4, D6
UC5_TX_SDA	O	UNICOMM5 TX: UART Transmit SDA: I2C Data	100, 108, 11, 121, 16, 18, 2, 28, 52, 54, 71, 75, 76, 81, 86, 92	B4, B6, B7, C9, E9, F9, G1, H6	11, 2, 21, 39, 56, 60, 61, 66, 72, 79, 82, 93	13, 39, 45, 52, 59	B4, C6, D2

Table 5-50. VREF Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	LQFP128 PIN	BGA99 PIN	LQFP100 G PIN	LQFP64 G PIN	WCSP48 PIN
VREFHI	AREF	Positive ADC Voltage Reference	43, 44	J5	36	28	G4
VREFLO	AREF	Negative ADC Voltage Reference	42	K5	35	27	G3

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

Parameters		MIN	MAX	UNIT
Supply voltage	VDD with respect to VSS	–0.3	4.6	V
	VDDA with respect to VSSA	–0.3	4.6	
Input voltage (3)	V_{IN} (3.3V)	–0.3	4.6	V
Output voltage	V_O	–0.3	4.6	V
Input clamp current - per pin (4) (5)	I_{IK} - V_{IN} < VSS/VSSA - V_{IN} > VDD/VDDA)	–20	20	mA
Input clamp current - total for all inputs (4) (5)	$I_{IKTOTAL}$ - V_{IN} < VSS/VSSA - V_{IN} > VDD/VDDA)	–20	20	mA
Current of SDIO pin(6)	I_{IO_SD}		4	mA
Current of HSIO pin(6)	I_{IO_HS}		6	mA
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Ambient temperature	T_A	–40	125	°C
Operating junction temperature	T_J	–40	150	°C
Storage temperature(7)	T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) Input clamp current must also be observed.
(4) Continuous clamp current per pin is ±2mA. Do not operate in this condition continuously as V_{DD}/V_{DDA} voltage may internally rise and impact other electrical specifications.
(5) Applying a V_{IN} greater than VDD/VDDA or less than VSS/VSSA will turn on the ESD current clamping diode causing additional current to flow to the respective supply rail. If this occurs, the current must be kept within the MIN/MAX listed to prevent permanent damage to the device.
(6) Refer to Digital IO Features by IO Type table in Pin Attributes section, SDIO includes SD, SDL and SDW IOs, HSIO includes HS IO.
(7) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

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6.2 Supply Current Characteristics

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations.

6.2.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled (unless otherwise noted).

PARAMETER		TEST CONDITIONS			25°C		55°C		85°C		105°C		125°C		UNIT
		V_{DD}	V_{DDC}	MCLK	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
RUN Mode															
I_{DD} (Run) (1)(4)	MCLK=SYSPLL, CoreMark, execute from RAM (SRAM3) (2)	3.3V	1.35V	250MHz											mA
				200MHz											
				170MHz											
				135MHz											
			1.30V	180MHz											
			1.25V	170MHz											
			1.20V	160MHz											
				150MHz											
				130MHz											
				120MHz											
				100MHz											
				80MHz											
				50MHz											mA
	MCLK=SYSOSC, CoreMark, execute from RAM (SRAM3) (2)	3.3V	1.20V	32MHz											mA
I_{DD} (Run) (1)(4)	MCLK=SYSPLL, CoreMark, execute from flash (2)	3.3V	1.35V	250MHz											mA
				200MHz											
				170MHz											
				135MHz											
			1.30V	180MHz											
			1.25V	170MHz											
			1.20V	160MHz											
				150MHz											
				130MHz	28.6										
				120MHz											
				80MHz											
				50MHz											
	MCLK=SYSOSC, CoreMark, execute from flash	3.3V	1.20V	32MHz											

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VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled (unless otherwise noted).

PARAMETER		TEST CONDITIONS			25°C		55°C		85°C		105°C		125°C		UNIT
		V_{DD}	V_{DDC}	MCLK	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{DD} (Run) with motor control (3) (4)	MCLK=SYSPLL, motor control app, execute from flash (2)	3.3V	1.35V	250MHz											mA
				200MHz											
				170MHz											
				135MHz											
			1.30V	180MHz											
			1.25V	170MHz											
			1.20V	160MHz											
				150MHz											
				130MHz	33.29										
				120MHz											
				100MHz	27.03										
I_{DD} (Run) with motor control (3) (4)	MCLK=SYSPLL, motor control app, execute SRAM3	3.3V	1.35V	250MHz											mA
				200MHz											
				170MHz											
				135MHz											
			1.30V	180MHz											
			1.25V	170MHz											
			1.20V	160MHz											
				150MHz											
				130MHz	33.6										
				120MHz											
				100MHz	27.3										
SLEEP Mode															
I_{DD} (Sleep)	MCLK=SYSPLL, SYSPLLREF=SYSOSC CPU is halted	3.3V	1.35V	250MHz											µA
				200MHz											
				170MHz											
				135MHz											
			1.30V	180MHz											
			1.25V	170MHz											
			1.20V	135MHz											
				100MHz											
				32MHz											µA
I_{DD} (Sleep)	MCLK=SYSOSC, PLL is disabled CPU is halted	3.3V	1.20V	32MHz											µA
I_{DD} (Run) with motor control (3) (4)	MCLK=SYSPLL, motor control app, execute from flash (2)	3.3V	1.35V	250MHz											mA

(1) Current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency.
(2) V_{DDC} (Core Voltage) can be set to the right value to reduce the current consumption based on the required running frequency (MCLK), CPU is executing continuously CoreMark or App code from Flash with Cache enabled and 3 wait states access.
(3) Motor Control App - 3 PWMs running at 10KHz(All PWM out's are mapped to GPIOs), ADC conversion happening with PWM triggers, DMA initialized, 3 SPI instances initialized with waiting for data over GPIOs.
(4) Guaranteed by characterization results, unless otherwise specified.

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6.2.2 STOP/STANDBY Modes

VDD=3.3V. All inputs in VDD domain tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
STOP Mode													
I_{DD} (Stop)	SYSOSC=32MHz, USE4MHZSTOP=1, DISABLESTOP=0	4MHz			240								uA
STANDBY0 Mode													
I_{DD} (Standby 0)	GPIOA enabled, RAM retention, PD0 all clocked	32kHz			196								uA
STANDBY1 Mode													
I_{DD} (Standby 1)	GPIOA enabled, RAM retention, PD0 all clock gated	OFF			196								uA

6.2.3 SHUTDOWN Mode

All inputs in VDD domain tied to 0V or VDD. Core regulator is powered down.

PARAMETER		VDD	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{DD} (Shutdown)	Supply current in SHUTDOWN mode	3.3V			2.5								uA

6.3 Recommended Operating Conditions

Parameters		MIN	NOM	MAX	UNIT
Device supply voltage, VDD and VDDA	Internal BOR enabled(1)	3.1	3.3	3.63	V
	Internal BOR disabled	2.8	3.3	3.63	
Device ground, VSS			0		V
Analog ground, VSSA			0		V
V_{IN}	Digital input voltage (2)	VSS – 0.3		VDD + 0.3	V
	Analog input voltage (2)	VSSA – 0.3		VDDA + 0.3	V
Capacitor connected between VDD and VSS, C_{VDD}	Filter capacitor(3)		10		µF
Junction temperature, T_J	T Series	–40		140	°C
Free-Air temperature, T_A	T Series	–40		125	°C

(1) Internal BOR is enabled by default.
(2) Applying a VIN greater than VDD/VDDA or less than VSS/VSSA voltage will internally rise and could impact other electrical characteristics.
(3) Connect C_{VDD} between VDD and VSS as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD}

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6.4 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital and Analog IO							
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MIN	VDD * 0.8			V
			I_{OH} = –100µA	VDD – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX			0.4	V
			I_{OL} = 100µA			0.2	
I_{OH}	High-level output source current for all output pins			–4			mA
I_{OL}	Low-level output sink current for all output pins					4	mA
R_{OH}	High-level output impedance for all output pins		VOH=VDDS-0.4V		66		Ω
R_{OL}	Low-level output impedance for all output pins		VOL=0.4V		60		Ω
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
$V_{HYSTERESIS}$	Input hysteresis (AIO)			125			mV
	Input hysteresis (GPIO)			125			
$I_{PULLDOWN}$	Input current	Pins with pulldown	VDD = 3.3V V_{IN} = VDD		120		µA
I_{PULLUP}	Input current	Digital inputs with pullup enabled(1)	VDD = 3.3V V_{IN} = 0 V		160		µA
$R_{PULLDOWN}$	Weak pulldown resistance				40		kΩ
R_{PULLUP}	Weak pullup resistance				40		kΩ
I_{LEAK}	Pin leakage	Digital inputs	Pullups and outputs disabled 0 V ≤ V_{IN} ≤ VDD			0.1	µA
I_{LEAK}	Pin leakage	Analog pins	Analog drivers disabled 0 V ≤ V_{IN} ≤ VDDA			0.1	µA
C_I	Input capacitance	Digital inputs			2		pF
		Analog pins(2)					
POR and BOR							
POR, BOR(3)							

(1) See Pins With Internal Pullup and Pulldown table for a list of pins with a pullup or pulldown.
(2) The analog pins are specified separately; see the Per-Channel Parasitic Capacitance tables that are in the ADC Input Model section.
(3) See the *Power Management Module (PMM)* section.

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6.5 Digital IO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Electrical Characteristics							
V_{IH}	High level input voltage	All I/O except Reset	2.8 ≤ VDD ≤ 3.6	0.7*VDD		VDD+0.3	V
		Reset pin	2.8 ≤ VDD ≤ 3.6	0.85*VDD		VDD+0.3	
V_{IL}	Low level input voltage	All I/O except Reset	2.8 ≤ VDD ≤ 3.6	-0.3		0.3*VDD	
		Reset pin	2.8 ≤ VDD ≤ 3.6	-0.3		0.15*VDD	V
V_{HYS}	Hysteresis	All I/O except Reset	2.8 ≤ VDD ≤ 3.6	0.1*VDD			
		Reset pin	2.8 ≤ VDD ≤ 3.6	0.3*VDD			
I_{lkg}	High-Z leakage current(1)(2)	SDIO	2.8 ≤ VDD ≤ 3.6			50	nA
		HSIO	2.8 ≤ VDD ≤ 3.6			200	nA
R_{PU}	Pull up resistance		VIN = VSS		40		kΩ
R_{PD}	Pull down resistance		VIN = VDD		40		kΩ
C_I	Input capacitance		VDD = 3.3V		5		pF
V_{OH}	High level output voltage	SDIO	VDD≥2.7V, I_{IO}=–4mA	VDD-0.4			V
		HSIO	VDD≥2.7V, DRV=1, I_{IO}=–6mA	VDD-0.4			
			VDD≥2.7V, DRV=0, I_{IO}=–4mA	VDD-0.4			
V_{OL}	Low level output voltage	SDIO	VDD≥2.7V, I_{IO}=4mA			0.4	V
		HSIO	VDD≥2.7V, DRV=1, I_{IO}=6mA			0.4	
			VDD≥2.7V, DRV=0, I_{IO}=4mA			0.4	
Switching Characteristics							
f_{max}	Port output frequency	SDIO (3)	VDD ≥ 2.7V, C_L= 20pF			32	MHz
		HSIO	VDD ≥ 2.7V, DRV = 1, C_L= 20pF			50	
			VDD ≥ 2.7V, DRV = 0, C_L= 20pF			32	
t_r,t_f	Output rise/fall time	SDIO	VDD ≥ 2.7V, C_L = 20pF			3.5	ns
		HSIO	VDD ≥ 2.7V, DRV = 1, C_L = 20pF			1.8	
			VDD ≥ 2.7V, DRV = 0, C_L = 20pF			5.9	

(1) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
(3) The sum of the $|I_{IO}|$ current sourced or sunk by the device must always respect the absolute maximum rating

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6.6 Thermal Information

This section provides the thermal resistance characteristics used on this device. For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the T_J value identified in *Recommended Operating Conditions*.

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6.7 System

6.7.1 Power Supply Sequencing

6.7.1.1 Power Supply Ramp

Figure 6-1 shows the relationships of POR-, POR+, BOR0-, and BOR0+ during powerup and powerdown.

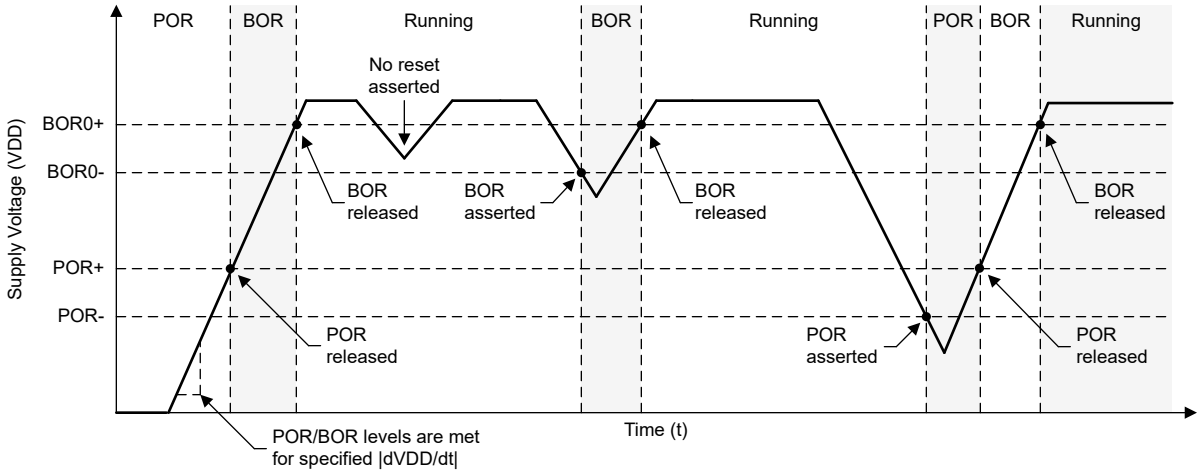


Figure 6-1. Power Cycle POR and BOR Conditions

6.7.1.2 POR and BOR

The two voltage monitors (POR and BOR) have to release their respective outputs before the device begins operation (that is, NRST goes high). However, if either of the voltage monitors trips, NRST is driven low. The I/Os are held in high impedance when any of the voltage monitors trip.

The POR monitor supervises the VDD rail. During power up, this is the first monitor to release (that is, first to untrip) on VDD.

The BOR monitor also supervises the VDD rail. During power up, this is the second monitor to release (that is, second to untrip) on VDD. This monitor has a tighter tolerance compared to the POR.

Any drop in voltage below the recommended operating voltages will trip the BOR and reset the device but this can be disabled by setting VMONCTL.bit.BORLVMONDIS to 1. The BOR can only be disabled after the device has fully booted up. If the BOR is disabled, the POR will reset the device for voltage drops.

6.7.1.2.1 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD	Power supply range		3.1	3.3	3.6	V
VDD	Power supply range	BOR bypass	2.8	3.3	3.6	V
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
dVDD/dt	VDD (supply voltage) slew rate	Falling (1)			0.01	V/us
dVDD/dt	VDD (supply voltage) slew rate	Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level	Rising	0.95	1.30	1.59	V
V_{POR-}	Power-on reset voltage level	Falling	0.9	1.25	1.54	V
$V_{HYS, POR}$	POR hysteresis			50		mV
$V_{BOR+, COLD}$	Brown-out reset voltage (default level)	Cold start, rising	2.45	2.7	2.97	V
V_{BOR+}	Brown-out reset voltage (default level)	Rising (1)	2.8	2.885	2.97	V
V_{BOR-}	Brown-out reset voltage (default level)	Falling (1)	2.8	2.85	2.97	V
$V_{BOR, STBY}$	Brown-out reset voltage (default level)	STANDBY mode	2.73	2.84	2.97	V

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HYS,BOR}$	Brown-out reset hysteresis			35		mV
$t_{PD:BOR}$	BOR propagation delay	RUN/SLEEP/STOP mode			10	us
$t_{PD:BOR}$	BOR propagation delay	STANDBY mode			100	us
C_{VDD} (2)(3)	VDD Capacitance Per Pin		0.1			uF
C_{VDDA} (2)(3)	VDDA Capacitance Per Pin		2.2			uF
$V_{BOR-VDD-GB}$ (4)	VDD Brown Out Reset Voltage Guardband			0.1		V
$I_{VREG(Run)-LOAD}$	Run Voltage Regulator Load Current				175	mA
$I_{VREG(Stop)-LOAD}$	Stop Voltage Regulator Load Current				5	mA

(1) Device operating in RUN, SLEEP, or STOP mode.
(2) The exact value of the decoupling capacitance depends on the system voltage regulation solution that is supplying these pins.
(3) It is recommended to tie the 3.3V rails (VDD, VDDA) together and supply them from a single source.
(4) TI recommends $V_{BOR-VDDIO-GB}$ to avoid BOR-VDD resets due to normal supply noise or load-transient events on the 3.3-V VDD system regulator. Good system regulator design and decoupling capacitance (following the system regulator specifications) are important to prevent activation of the BOR-VDD during normal device operation. The value of $V_{BOR-VDD-GB}$ is a system-level design consideration; the voltage listed here is typical for many applications.

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6.7.1.3 Timing Characteristics

6.7.1.3.1 Timing Characteristics

over recommended operating conditions, VDD=3.3V, T_a=25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wakeup Timing						
$t_{WAKE:SLEEP}$	Wakeup time from SLEEP to RUN (1)					µs
$t_{WAKE:STOP}$	Wakeup time from STOP to RUN (SYSOSC enabled) (1)			68		µs
$t_{WAKE:STBY}$	Wakeup time from STANDBY0 to RUN (1)			120		µs
	Wakeup time from STANDBY1 to RUN (1)			121		µs
$t_{WAKEUP:SHDN}$	Wakeup time from SHUTDOWN to RUN			1040		µs
Asynchronous Fast Clock Request Timing						
t_{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STOP				µs
	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY0				
	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is STANDBY1				
Startup Timing						
$t_{START:RESET}$	Device cold startup time from reset/ power-up (2)					µs
NRST Timing						
$t_{RST:BOOTRST}$	Pulse length on NRST pin to generate BOOTRST	ULPCLK≥4MHz				µs
		ULPCLK=32kHz				
$t_{RST:POR}$	Pulse length on NRST pin to generate POR					s

(1) The wake-up time is measured from the edge of an external wake-up signal (IOMUX wake-up event) to the time that first instruction of the user program is executed.
(2) The start-up time is measured from the time that VDD crosses VBOR0- (cold start-up) to the time that the first instruction of the user program is executed.

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6.7.2 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32 kHz)
- **SYSOSC**: Internal high-frequency oscillator (4 MHz or 32 MHz with factory trim)
- **LFXT/LFCKIN** : Low-frequency external crystal oscillator or digital clock input (32 kHz)
- **HFXT/HFCKIN**: High-frequency external crystal oscillator or digital clock input (4 to 48 MHz)
- **SYSPLL**: System phase locked loop with 3 outputs (32 to 250 MHz)

6.7.2.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=0 (BASE)		32		MHz
		SYSOSCCFG.FREQ=1		4		
f_{SYSOSC}	SYSOSC frequency accuracy with FCL enabled(1) (2)	-40℃ ≤ Ta ≤ 70℃	-1.0		1.0	%
		-40℃ ≤ Ta ≤ 90℃ (3)(4)	-1.0		1.0	%
		-40℃ ≤ Ta ≤ 105℃ (3)(4)	-1.4		1	%
		-40℃ ≤ Ta ≤ 125 ℃ (3)(4)	-2.0		1	%
		-20℃ ≤ Ta ≤ 90℃ over 10 years(4)				%
		-40℃ ≤ Ta ≤ 105℃ over 10 years(4)				%
	SYSOSC raw frequency accuracy with FCL disabled, 32MHz(5)	SYSOSCCFG.FREQ=0, -40℃ ≤ T_a ≤ 105℃				%
	SYSOSC frequency accuracy with FCL disabled, 4MHz	SYSOSCCFG.FREQ=1, -40℃ ≤ T_a ≤ 105℃				%
$t_{settle, SYSOSC}$	Settling time to target accuracy(6)	SETUSEFCL=1				us
$f_{settle, SYSOSC}$	f_{SYSOSC} accuracy during t_{settle}(6)	SETUSEFCL=1	-11			%

(1) f_{SYSOSC} may shift due to the thermal and mechanical stress of solder reflow. A post-reflow bake can restore the unit to its original data sheet performance.
(2) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an internal reference resistor when using the FCL. See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy.
(3) Data is preliminary, derived from characterization and design, not verified through production testing.
(4) Power consumption is assumed to be 0.25W.
(5) SYSOSC accuracy is measured in the default power-up state, with MCLK = SYSOSC, the CPU executing a continuous while(1) loop, and the SYSPLL disabled.
(6) When SYSOSC is waking up (for example, when exiting a low power mode) and FCL is enabled, the SYSOSC will initially undershoot the target frequency f_{SYSOSC} by an additional error of up to $f_{settle,SYSOSC}$ for the time $t_{settle,SYSOSC}$, after which the target accuracy is achieved.

6.7.2.2 High Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High Frequency External Crystal Oscillator (XTAL)						
f_{XTAL}	XTAL frequency	USEHSCLK=1, USEEXTHFCLK=0	10		20	MHz
DC_{XTAL}	XTAL duty cycle	USEHSCLK=1, USEEXTHFCLK=0		50		%
OA_{XTAL}	XTAL crystal oscillation allowance	4 to 48MHz range		2		kΩ
$C_{L, eff}$	Integrated effective load capacitance(1)	USEHSCLK=1, USEEXTHFCLK=0		1		pF
$t_{start, XTAL}$	XTAL start-up time (2)	32MHz crystal		0.5		ms
I_{HFXT}	XTAL current consumption	f_{HFXT}=4MHz, R_m=300Ω, C_L=12pF		75		uA
		f_{HFXT}=32MHz, R_m=30Ω, C_L=12pF, C_m=6.26fF, L_m=1.76mH		600		
High Frequency Digital Clock Input (HFCLK_IN)						

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{HFIN}	HFCLK_IN frequency (3)	USEHSCLK=1, USEEXTHFCLK=1	4		48	MHz
DC_{HFIN}	HFCLK_IN duty cycle (3)	USEEXTHFCLK=1	40		60	%

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{X1}×C_{X2}/(C_{X1}+C_{X2})$, where C_{X1} and C_{X2} are the total capacitance at SYSCTL_X1 and SYSCTL_X2, respectively.
(2) The High Frequency External Crystal Oscillator (XTAL) startup time ($t_{start, XTAL}$) is measured from the time the XTAL is enabled until stable oscillation for a typical crystal. Start-up time is dependent upon crystal frequency and crystal specifications. Refer to the External Crystal Oscillator (XTAL) section of the AM13E232x Microcontrollers Technical Reference Manual
(3) The digital clock input (SYSCTL_HFCLKIN) accepts a logic level square wave clock.

6.7.2.3 System Phase Lock Loop (SYSPLL)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SYSPLLREF}$	SYSPLL reference frequency range		20		25	MHz
f_{VCO}	VCO output frequency	BIASRANGEFIX should be HIGH and by default this is recommended mode of operation.	160		800	MHz
f_{SYSPLL}	SYSPLL output frequency range (1)	SYSPLLCLK0, SYSPLLCLK1	5		400	MHz
DC_{PLL}	SYSPLL output duty cycle	$f_{SYSPLLREF}$=32MHz, f_{VCO}=400MHz, SYSPLLCLK0/1	45		55	%
$Jitter_{SYSPLL}$	SYSPLL RMS cycle-to-cycle jitter	$f_{SYSPLLREF}$=32MHz, fINTCLK = 8MHz		TBD		%
	SYSPLL RMS period jitter		-2.5		2.5	
I_{SYSPLL}	SYSPLL current consumption	$f_{SYSPLLREF}$=32MHz, f_{VCO}=400MHz, PDIV=2; SYSPLL =400 MHz			1.35	mA
$t_{start,\ SYSPLL}$	SYSPLL start-up time	$f_{SYSPLLREF}$=32MHz, f_{VCO}=400MHz, PDIV=2; SYSPLL =200 MHz, ±1% accuracy			24.5	us

(1) The SYSPLL may support higher output frequencies than the device clock system supports. Ensure that the device maximum frequency specifications are not violated when configuring the SYSPLL output frequencies.

6.7.2.4 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFOSC}	LFOSC frequency			32768		Hz
	LFOSC accuracy	-40 °C ≤ T_a ≤ 125 °C	–5		5	%
		-40 °C ≤ T_a ≤ 85 °C	–3		3	%
I_{LFOSC}	LFOSC current consumption			300		nA
$t_{start,\ LFOSC}$	LFOSC start-up time			1.7		ms

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6.7.3 Flash Memory Characteristics

The on-chip flash memory is tightly integrated to the CPU, allowing code execution directly from flash through 256-bit-wide prefetch reads, a pipeline buffer and code block cache. Flash performance for sequential code is equal to execution from RAM. Factoring in discontinuities, most applications will run with an efficiency of approximately 80% relative to code executing from RAM.

This device also has SECCFG sectors which are used for security configuration and flash management.

Minimum Required AM13E232 Flash Wait States with Different Clock Frequencies lists the minimum required wait states for AM13E232 flash at different frequencies.

Table 6-1. Minimum Required AM13E232 Flash Wait States with Different Clock Frequencies

CPUCLK (MHz)	Wait States (FRDCNTL[RWAIT](1))
200 < CPUCLK ≤ 250	4
150 < CPUCLK ≤ 200	3
100 < CPUCLK ≤ 150	2
0 < CPUCLK ≤ 100	1

(1) Minimum required FRDCNTL[RWAIT] is 1, RWAIT=0 is not supported.

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6.7.3.1 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
$VDD_{PGM/ERASE}$	Program and erase supply voltage		3.1		3.6	V
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta			10	mA
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta			10	mA
Endurance						
N_{WEC}	Write/Erase cycle endurance		20			k cycles
N_{WEC}	Write/Erase Cycles for entire device (limited by flash pump endurance)		20			k cycles
Retention						
t_{RET_85}	Flash memory data retention	-40°C <= Tj <= 85°C	20			years
Program and Erase Timing						
$t_{PROG\ (WORD,\ 128)}$	Program time for flash word (1) (3)			40		µs
$t_{PROG\ (SEC,\ 128)}$	Program time for 2kB sector (2) (3)			5.1		ms
t_{ERASE} (4) (5)	2KB (sector) erase time	at < 25 erase/program cycles		15	55	ms
	64KB erase time			17	61	ms
	128KB erase time			18	66	ms
	256KB erase time			21	78	ms
t_{ERASE}	2KB (sector) erase time	at 1000 erase/program cycles		25	130	ms
	64KB erase time			28	143	ms
	128KB erase time			30	157	ms
	256KB erase time			35	183	ms
t_{ERASE}	2KB (sector) erase time	at 2000 erase/program cycles		30	221	ms
	64KB erase time			33	243	ms
	128KB erase time			36	265	ms
	256KB erase time			42	310	ms
t_{ERASE}	2KB (sector) erase time	at 20K erase/program cycles		120	1003	ms
	64KB erase time			132	1102	ms
	128KB erase time			145	1205	ms
	256KB erase time			169	1410	ms
F_{CLK}	Flash clock frequency				50	MHz

(1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
- Code that uses flash API to program the flash
- Flash API itself
- Flash data to be programmed

In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the JTAG debug probe used.
Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does.
Erase time includes Erase verify by the CPU and does not involve any data transfer.

(2) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.

(3) Flash word size is 128 data bits (16 bytes). On devices with ECC, the total flash word size is 144 bits (128 data bits plus 16 ECC bits).

(4) Erase time includes Erase verify by the CPU.

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(5) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.

6.7.4 RAM Specifications

The device includes a 192kB of SRAM across four banks fully protected by hardware parity. SRAM memory can be used for storing volatile information such as the call stack, heap, global data, and code.

- SRAM0 (32kB) memory fully retained in low power modes of STOP and STANDBY operating mode.

The Table 6-2 describes the operational conditions for the multiple SRAM banks on the device.

Table 6-2. SRAM Bank Property

	SRAM0	SRAM1/2/3
0-Wait State Frequency	200MHz / 250MHz	200MHz / 250MHz
Safety	Parity	Parity
Security	GSC based	GSC based
RUN Mode State	ACTIVE	ACTIVE
SLEEP Mode State	ACTIVE	ACTIVE
STOP Mode State	RETAINED	OFF
STANDBY 0 Mode State	RETAINED	OFF
STANDBY 1 Mode State	RETAINED	OFF
SHUTDOWN Mode State	OFF	OFF

For more details, see the SRAM chapter of the *AM13E232x Microcontrollers Technical Reference Manual*.

6.7.5 ROM Specifications

Table 6-3. ROM Parameters

ROM Block	SIZE EACH	ECC/Parity	Secured	WAIT STATES	HOST ACCESS LIST
CPU Boot ROM	48KB	No	No	1 @ 200MHz / 250MHz	CPU1

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6.8 Analog Peripherals

The analog subsystem module is described in this section.

The analog modules on this device includes 3 Analog-to-Digital Converters(ADC), 1 Temperature Sensor, 3 Programmable Gain Amplifiers (PGA), and 4 Comparator Subsystems (CMPSS).

The analog subsystem has the following features:

- Flexible voltage references
  - The ADC is referenced to VREFHI and VREFLO pins.
    - VREFHI pin voltage can be driven in externally or can be generated by an internal bandgap voltage reference
    - The internal voltage reference range can be selected to be 0V to 2.5V
  - The comparator DACs are referenced to VDDA and VSSA
- Flexible pin usage
  - Low comparator DAC (COMPDACOUT) can optionally be brought out to a multiplexed ADC pin for external use (mutually exclusive with use of CMPSS compare functions and only available on some CMPSS instances)
  - Internal connection to VREFLO on ADC for offset self-calibration

6.8.1 Analog-to-Digital Converter (ADC)

The ADC module described here is a successive approximation (SAR) style ADC with resolution of 12 bits. This section refers to the analog circuits of the converter as the “core,” and includes the channel-select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The digital circuits of the converter are referred to as the “wrapper” and include logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

Each ADC module consists of a single sample-and-hold (S/H) circuit. The ADC module is designed to be duplicated multiple times on the same chip, allowing simultaneous sampling or independent operation of multiple ADCs. The ADC wrapper is start-of-conversion (SOC)-based.

Each ADC has the following features:

- Resolution of 12 bits
- Ratiometric external reference set by VREFHI/VREFLO
- Selectable internal reference of 2.5 V or 3.3 V
- Single-ended signal mode
- Input multiplexer with up to 32 channels
- 16 configurable SOCs controlled by sequencers (SEQ[0:3])
- 16 individually addressable result registers
- Sample cap reset feature for memory crosstalk mitigation
- Multiple trigger sources
  - Software immediate start
  - All MCPWMs: ADCSOC A or B
  - GPIO (external SOC)
  - GP Timers 0/1
  - ADCINT1/2
  - eCAP events in capture mode (CEVT1, CEVT2, CEVT3, and CEVT4) and APWM mode (period match, compare match, or both).
  - Global software trigger for multiple ADCs
- Four flexible interrupts
- Burst-mode triggering option
- Hardware oversampling mode up to 128x, with configurable trigger spread delay
- Hardware undersampling mode
- Trigger phase delay function

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- Four post-processing blocks, each with:
  - Saturating offset calibration
  - Error from setpoint calculation
  - High, low, and zero-crossing compare, with interrupt and MCPWM trip capability
  - Configurable digital filter for high/low/zero-crossing compare
  - Trigger-to-sample delay capture
  - Absolute value calculation
  - 24-bit accumulation register for oversampling, with configurable binary shift
  - Minimum/maximum calculation for outlier rejection

6.8.1.1 ADC Electrical Data and Timing

Note

The ADC inputs should be kept below VDDA + 0.3 V. If an ADC input goes above this level, ADC disturbances to other channels may occur by two mechanisms:

- ADC input overvoltage will overdrive the CMPSS mux, disturbing all other channels which share a common CMPSS mux. This disturbance will be continuous regardless of if the overvoltage input is sampled by the ADC
- When the ADC samples the overvoltage ADC input, VREFHI will be pulled up to a higher level. This will disturb subsequent ADC conversions on any channel until the V_{REF} stabilizes

The VREFHI pin must be kept below VDDA + 0.3 V to ensure proper functional operation. If the VREFHI pin exceeds this level, a blocking circuit may activate, and the internal value of VREFHI may float to 0 V internally, giving improper ADC conversion.

6.8.1.1.1 ADC Operating Conditions

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from MCLK)	200MHz MCLK	5		100	MHz
	250MHz MCLK	5		125	MHz
Sample rate[4] [5]	100MHz ADCCLK, SAMPCAPRESETSEL = 0			6.25	MSPS
	100MHz ADCCLK, SAMPCAPRESETSEL = 1			6.67	MSPS
	125MHz ADCCLK, SAMPCAPRESETSEL = 0			7.35	MSPS
	125MHz ADCCLK, SAMPCAPRESETSEL = 1			7.81	MSPS
Sample window duration (set by ACQPS and MCLK)[1]	With 50Ω or less R_s	40			ns
	Internal VREFLO Connection	40			
VREFHI	External Reference	2.4	2.5 or 3.0	VDDA	V
VREFHI[2]	Internal Reference = 3.3V Range		1.65		V
	Internal Reference = 2.5V Range		2.5		V
VREFLO		VSSA		VSSA	V
VREFHI - VREFLO		2.4		VDDA	V
Conversion range	Internal Reference = 3.3V Range	0		3.3	V
	Internal Reference = 2.5V Range	0		2.5	
	External Reference	VREFLO		VREFHI	
Conversion range	Package = QFN48	0		VDDA[3]	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.

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(3) On QFN48 package, VREFHI is internally tied to VDDA and VREFLO is internally tied to VSSA. Internal reference mode is not supported on QFN48 package.
(4) Non-integer ADC clock dividers are not supported: ADCCTL2.PRESCALE should only use even values
(5) Sample and hold cap reset feature must be enabled; SAMPCAPRESETSEL = 0

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6.8.1.1.2 ADC Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles(1)				11	ADCCLKs
Power Up Time	External Reference mode			500	µs
	Internal Reference mode			5000	µs
	Internal Reference mode, when switching between 2.5V range and 3.3V range.			5000	µs
VREFHI input current(2)			200		µA
Internal Reference Capacitor Value(3)		2.2			µF
External Reference Capacitor Value(3)		2.2			µF
DC Characteristics					
Gain Error	Internal reference		±45		LSB
	External reference		±5		
Offset Error			±2		LSB
Channel-to-Channel Gain Error(5)			2		LSB
Channel-to-Channel Offset Error(5)			2		LSB
ADC-to-ADC Gain Error(6)	Identical VREFHI and VREFLO for all ADCs		4		LSB
ADC-to-ADC Offset Error(6)	Identical VREFHI and VREFLO for all ADCs		2		LSB
DNL Error			±1.0		LSB
INL Error			±2.0		LSB
ADC-to-ADC Isolation	VREFHI = 2.5V, synchronous ADCs	–1		1	LSBs
AC Characteristics					
SNR(4)	VREFHI = 2.5V, fin = 100kHz, MCLK from X1		67.08		dB
	VREFHI = 2.5V, fin = 100kHz, MCLK from SYSOSC		TBD		
THD(4)	VREFHI = 2.5V, fin = 100kHz		–77		dB
SFDR(4)	VREFHI = 2.5V, fin = 100kHz		82		dB
SINAD(4)	VREFHI = 2.5V, fin = 100kHz, MCLK from X1		67.08		dB
	VREFHI = 2.5V, fin = 100kHz, MCLK from SYSOSC		62.3		
ENOB(4)	VREFHI = 2.5V, fin = 100kHz, MCLK from X1, Single ADC		10.8		bits
PSRR	VDDA = 3.3V DC + 200mV DC up to Sine at 1kHz		60		dB
	VDDA = 3.3V DC + 200mV Sine at 900kHz		57		

(1) Using SAMPCAPRESET feature; SAMPCAPRESETSEL = 1 and SAMPCAPRESETDISABLE = 0 inside the corresponding ADCSOCxCTL register.
(2) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(3) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(4) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(5) Variation across all channels belonging to the same ADC module.
(6) Worst case variation compared to other ADC modules.

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6.8.1.1.3 ADC Input Model

The ADC input characteristics are given by Figure 6-2 .

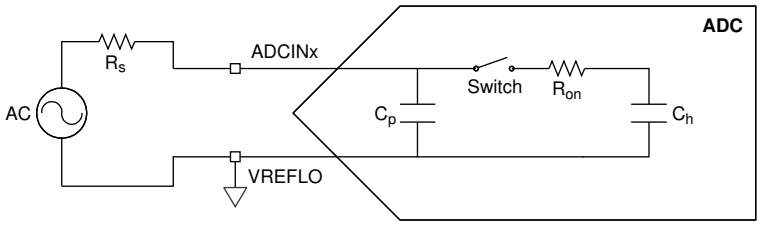


Figure 6-2. ADC Input Model

This input model should be used with actual signal source impedance to determine the acquisition window duration. For more information, see the *Choosing an Acquisition Window Duration* section of the Analog-to-Digital Converter (ADC) chapter in the *AM13E232x Microcontrollers Technical Reference Manual*. For recommendations on improving ADC input circuits, see the *ADC Input Circuit Evaluation for C2000 MCUs* Application Note.

ADC Input Model

over operating free-air temperature range (unless otherwise noted)

PARAMETER	Description	Reference Mode	TYP	UNIT
C_p	Parasitic input capacitance	All Modes		
R_{on}	Sampling switch resistance	External Reference, 2.5V Internal Reference	400	Ω
		3.3V Internal Reference	500	Ω
C_h	Sampling capacitance	External Reference, 2.5V Internal Reference	10	pF
		3.3V Internal Reference	8	pF
R_s	Nominal source impedance	All Modes	50	Ω

6.8.1.1.4 ADC Timing Requirements

		MIN	MAX	UNIT
$t_{su(ADCCHSEL-SOC)}$	ADCCHSEL valid before ADCSOC high	0.5		ns
$t_{su(ADCSOC)}$	ADCSOC low before ADCCLK high	1		ns
$t_{w(ADCCLK)}$	Width of ADCCLK	0.8		ns
$t_{w(ADCSOC)}$	Width of ADCSOC	0.6		ns

6.8.1.1.5 External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, $\overline{ADCSOCxO}$ low	$32t_{c(SYSCLK)}$		cycles

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6.8.2 Comparator Subsystem (CMPSS)

The Comparator Subsystem (CMPSS) consists of analog comparators and supporting circuits that are useful for power applications such as peak current mode control, switched-mode power supply, power factor correction, voltage trip monitoring, and so forth.

The comparator subsystem is built around a number of modules. Each subsystem contains two comparators, two reference 8-bit DACs, and two digital filters. Comparators are denoted "H" or "L" within each module where “H” and “L” represent high and low, respectively. Each comparator generates a digital output which indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator is driven from an external pin. The negative input can be driven by an external pin or by the programmable reference 10-bit DAC. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. An unfiltered output is also available if filtering is not required.

Each CMPSS includes:

- Two analog comparators
- Two (10-bit effective DACs on CMPSS_LITE instances)
- Two digital filters, 65536 max filter clock prescale
- Ability to synchronize submodules with EPWMSYNCPER
- Ability to synchronize output with MCLK
- Ability to latch output
- Ability to invert output
- Option to use hysteresis on the input
- Option for negative input of comparator to be driven by an external signal or by the reference DAC
- Option for positive input of comparator to be driven by an external signal or by the PGA
- Option to use the low comparator DAC output, CMPx_DACL, on an external pin (select instances only, mutually exclusive with use of compare functionality)

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6.8.2.1 CMPSS Electrical Data and Timing

6.8.2.1.1 CMPSS_LITE Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPU	Power-up time	Bandgap Not Enabled			500	µs
Comparator input (CMPINxx) range			0		VDDA	V
Input referred offset error		Via AIO/AGPIO, Input common mode = 5% to 95% of VDDA	–20		20	mV
Hysteresis[1]	Hysteresis[1]	0x	-6	0	6	mV
Hysteresis[1]		1x	1	10	19	mV
		2x	7	20	34	
		3x	14	30	51	
		4x	19	41	70	
		5x	25	52	88	
		6x	31	64	109	
		7x	37	77	131	
Response time (delay from CMPINx input change to output on MCPWM X-BAR or Output X-BAR)		Step response		21	40	ns
		Ramp response (1.65V/µs)		26		
		Ramp response (8.25mV/µs)		30		
VDDA	Analog Supply		2.8	3.3	3.63	V
VDD	Core Supply		1.08	1.2	1.32	V
Tj	Temperature		–40	27	155	°C
Resolution				12		bits
Input Clock (SYSCLK) Frequency			1		100	MHz
Input Clock (SYSCLK) Pulse Width				TSYSCLK/2		
Conversion Range		VDAC	0		VDAC	V
Conversion Range		VDDA	0		VDDA	V
VDAC	VDAC Range		2.4	3.3	VDDA	V
DNL	Differential Non Linearity		–1		4	LSB
INL	Static Integral Non Linearity		–16		16	LSB
Ramp Linearity	Dynamic Ramp Error	20 DAC Input Steps per 60 MHz SYSCLK. Response Must be Monotonic.	–64		64	LSB
Full Scale Step Response Settling Time					1	µs
Comparator Trip Disturbance			–512	+/-120	512	LSB
Comparator Trip Disturbance Settling Time					200	ns
Gain	Gain Error		–2		2	% of FSR
Reference Input Impedence	Reference Input Impedance			8		kΩ
PSRR	Power Supply Rejection Ratio	Up to 250 kHz		46		dB
Ramp Response Time				26		ns
Slow Ramp Response Time				30		ns
Step Response Time		AIO			50	ns
Input Offsett Error	Input Offset Error	w/ Jitter Aggressor	–20	5	20	mV
Input Hysteresis from Ideal			–5	0	5	mV
CMRR	Common Mode Rejection Ratio		40			dB
IVDDA	Active Current (Analog Supply)	CMPSS			120	µA
IVDD	Active Current (Core Supply)	CMPSS			6	µA
IVDDA(leak)	Leakage Current (Analog Supply)	CMPSS				µA
IVDD(leak)	Leakage Current (Core Supply)	CMPSS				µA
IVDDA	Active Current (Analog Supply)	DAC		400		µA
IVDD	Active Current (Core Supply)	DAC		0		µA

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over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IVDDA(leak)	Leakage Current (Analog Supply)	DAC				µA
IVDD(leak)	Leakage Current (Core Supply)	DAC				µA
dvt	Transient vt shift			5		mV

(1) Hysteresis is available for all comparator input source configurations.

6.8.2.1.2 CMPSS_LITE DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMPSS_LITE DAC output range		0		VDDA	V
Static offset error(1)		–25		25	mV
Static gain error(1)		–0.5		0.5	% of FSR
Static DNL	Endpoint corrected	–5		5	LSB (12-bit)
Static INL	Endpoint corrected	–5		5	LSB (12-bit)
Static TUE (Total Unadjusted Error)				35	mV
Settling time	Settling to 1LSB after full-scale output change		1		µs
Resolution(2)			12		bits

(1) Includes comparator input referred errors.
(2) 9.5-bit effective resolution for monotonic response

6.8.3 Programmable Gain Amplifier (PGA)

The Programmable Gain Amplifier (PGA) is used to amplify an input voltage for the purpose of increasing the effective resolution of the downstream ADC and CMPSS modules.

The integrated PGA helps to reduce cost and design effort for many control applications that traditionally require external, stand-alone amplifiers. On-chip integration ensures that the PGA is compatible with the downstream ADC and CMPSS modules. Software-selectable gain and filter settings make the PGA adaptable to various performance needs.

The PGA has the following features:

- Rail to rail input and output voltage within VDDA and VSSA range
- Programmable gain modes including unity gain and other values from 2X - 64X
- Standalone gain mode using off-chip passive components
- Post-gain filtering using on-chip resistors
- Differential input support
- Hardware assisted chopping for offset reduction
- Support for Kelvin ground connections using PGA_INM pins

The active component in the PGA is an embedded operational amplifier (op amp) that is configured as a non-inverting or inverting amplifier with internal feedback resistors. These internal feedback resistor values are paired to produce software selectable voltage gains.

Three PGA signals are available at the device pins:

- PGA_INP is the positive input to the PGA op-amp.
- PGA_INM is the negative input to the PGA op-amp. See the device data manual for more information.
- PGA_OUT supports op-amp output filtering with RC components. The filtered signal is available for sampling and monitoring by on-chip ADC and CMPSS modules.

6.8.3.1 PGA Electrical Data and Timing

6.8.3.1.1 PGA Operating Conditions

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDA		2.8	3.3	3.6	V

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over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD		1.08	1.2	1.32	V
TEMP	T_J	–40	27	155	C
Clock Frequency		SYSCLK		150	MHz
Clock Duty Cycle		40	50	60	%
PGA Output Range(1)		VSSA+0.025		VDDA–0.025	V
PGA Input Range		–0.05		VDDA	V
Min ADC S+H	With Filter	75			ns
Min ADC S+H (No Filter, Level Shifting)		220			ns
Capacitive Load on PGA Out			40		pF

(1) This is the linear output range of the PGA. The PGA can output voltages outside this range, but the voltages will not be linear.

6.8.3.1.2 PGA Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
Min ADC S+H Settling within ±1 ADC LSB Accuracy (No Filter; All Gain Settings; Single ADC Driven) (5)	Gain = 1	125			ns
	Gain = 2/-1	146			
	Gain = 4/-3	125			
	Gain = 8/-7	154			
	Gain = 16/-15	227			
	Gain = 32/-31	322			
	Gain = 64/-63	420			
Gain Settings			1		
			2, 4, 8, 16, 32, 64		
			–1, –3, –7, –15, –31, –63		
Short Circuit Current (6)			41		mA
Full Scale Step Response (No Filter) Settling within 0.05% Accuracy(5)	G<64			420	ns
	G = 64/-63			500	ns
Settling Time: Gain Switching				10	µs
Slew Rate	Naked OPA Mode		12		V/µs
Slew Rate	Gain = 1		12		V/µs
	Gain = 2/-1		24		V/µs
	Gain = 4/-3		43		V/µs
	Gain = 8/-7		67		V/µs
	Gain = 16/-15		35		V/µs
	Gain = 32/-31		29		V/µs
	Gain = 64/-63		26		V/µs
Overload Recovery Time	Settling to 0.1%		.400		µs

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over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ia}	Gain = 1		256		kΩ
	Gain = 2/-1		14		kΩ
	Gain = 4/-3		7		kΩ
	Gain = 8/-7		8		kΩ
	Gain = 16/-15		8		kΩ
	Gain = 32/-31		8		kΩ
	Gain = 64/-63		4		kΩ
R_{ib}	Gain = 1		0		kΩ
	Gain = 2/-1		14		kΩ
	Gain = 4/-3		21		kΩ
	Gain = 8/-7		56		kΩ
	Gain = 16/-15		120		kΩ
	Gain = 32/-31		248		kΩ
	Gain = 64/-63		252		kΩ
Filter Resistor Targets	R_{FILT} = 800Ω		800		Ω
	R_{FILT} = 400Ω		400		Ω
	R_{FILT} = 200Ω		200		Ω
	R_{FILT} = 100Ω		100		Ω
	R_{FILT} = 50Ω		50	62	Ω
Active Current	VDDA Without Filter		1.3	1.7	mA
	VDDA With Filter		1.3	1.9	mA
	VDD Without Filter		10	200	uA
	VDD With Filter		10	200	uA
Leakage Current	VDDA		.02		µA
	VDD		.03		µA
Gain Bandwidth Product (Naked Op-Amp Mode)	Gain=1		7		MHz
Closed Loop -3bd BW	Gain=1		15		MHz
	Gain=2/-1		14		MHz
	Gain=4/-3		13.5		MHz
	Gain=8/-7		12		MHz
	Gain=16/-15		11		MHz
	Gain=32/-31		5.5		MHz
	Gain=64/-63		5.0		MHz
DC Characteristics					
Gain Error(1)	Gain = 1	–0.18		0.18	%
	Gain = 2, -1	–0.37		0.37	%
	Gain = 4, -3	–0.6		0.6	%
	Gain = 8, -7	–0.73		0.73	%
	Gain = 16, -15	–0.81		0.81	%
	Gain = 32, -31	–1.0		1.0	%
	Gain = 64, -63	–1.82		1.82	%
Offset Error (Untrimmed)	Input Referred	–8		8	mV
Offset Error(2)	Input Referred	–3.0	+/–1.0	3.0	mV
Offset Temp Coefficient	Input Referred	–7.0		7.0	µV/C

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over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset Error - Chopped		–0.8		0.8	mV
Offset Temp Coefficient - Chopped			0.3		µV/C
Offset Trim Range	Min			–8	mV
	8			mV	
Long Term Offset Drift	Input Referred		3		mV
INL	With ADC	–3		3	12b LSB
DC Code Spread	G<64		2.5		12b LSB
	G = 64/-63		4		12b LSB
AC Characteristics					
Phase Margin Naked OPA	C_{load} = 40pF G=1		45		Deg
Aol (Open loop voltage gain) Naked OPA	R_L=7.5kΩ to GND 0.3V<V_O<VDDA-0.3V		94		dB
THD + Noise (THD+N) Naked OPA	f_{in}=1kHz G=1		82		dB
Bandwidth(3)	All Gain Modes		7		MHz
SNR 10kHz (With ADC)	Gain = 1		68		dB
	Gain = 2, -1		68		
	Gain = 4, -3		66		
	Gain = 8, -7		62		
	Gain = 16, -15		58		
	Gain = 32, -31		55		
	Gain = 64, -63		51		
THD(4)	DC		–78		dB
THD(Up to 100kHz) (4)	Gain = 1		–58		dB
	Gain = 2, -1		–70		
	Gain = 4, -3		–70		
	Gain = 8, -7		–70		
	Gain = 16, -15		–70		
	Gain = 32, -31		–58		
	Gain = 64, -63		–58		
CMRR	DC: V_{IN} <=1.5V		–86		dB
	DC: Full Input Range		–77		dB
	Up to 100kHz		–50		dB
PSRR(4)	DC		–75		dB
	Up to 10kHz		–60		dB
	Up to 100kHz		–40		dB
Noise PSD(4)	1kHz		200		nV/sqrt(Hz)
	10kHz		100		nV/sqrt(Hz)
Integrated Noise (Input Referred)(4)	3Hz to 30MHz		100		µV

(1) Includes ADC gain error.
(2) Includes ADC offset error.
(3) 3dB bandwidth.
(4) Performance of PGA alone.
(5) Step response time w filter = tS+H + 7.6*R_{filt}* C_{filt}

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(6) Assumes no filter circuit

6.8.4 Internal Analog Connections

over operating free-air temperature range (unless otherwise noted)

Internal Signal	Connections
TEMPSENSOR	A0_13/A2_13
PGA0_OUT (Internal)	A0_31
PGA1_OUT (Internal)	A1_31
PGA2_OUT (Internal)	A2_31

6.9 Control Peripherals

6.9.1 Enhanced Capture (eCAP)

The features of the eCAP module include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed by way of Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module features described in this section include:

- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single-shot capture of up to four event time-stamps
- Continuous mode capture of time stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output

The capture functionality of the Type 1 eCAP is enhanced from the Type 0 eCAP with the following added features:

- Event filter reset bit
  - Writing a 1 to ECCTL2[CTRFILTRESET] clears the event filter, the modulo counter, and any pending interrupts flags. Resetting the bit is useful for initialization and debug.
- Modulo counter status bits
  - The modulo counter (ECCTL2 [MODCNTRSTS]) indicates which capture register is loaded next. In the Type 0 eCAP, to know the current state of the modulo counter was not possible
- DMA trigger source
  - eCAPxDMA was added as a DMA trigger. CEVT[1-4] can be configured as the source for eCAPxDMA.
- Input multiplexer
  - ECCTL0 [INPUTSEL] selects one of 128 input signals, which are detailed in the Configuring Device Pins for the *eCAP* section of the Enhanced Capture (eCAP) chapter in the TRM.
- EALLOW protection
  - EALLOW protection was added to critical registers. To maintain software compatibility with Type-0, configure DEV_CFG_REGS.ECAPTYPE to make these registers unprotected.

The capture functionality of the Type 2 eCAP is enhanced from the Type 1 eCAP with the following added features:

- Added ECAPxSYNCINSEL register
  - ECAPxSYNCINSEL register is added for each eCAP to select an external SYNCIN. Every eCAP can have a separate SYNCIN signal.

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6.9.1.1 eCAP Block Diagram

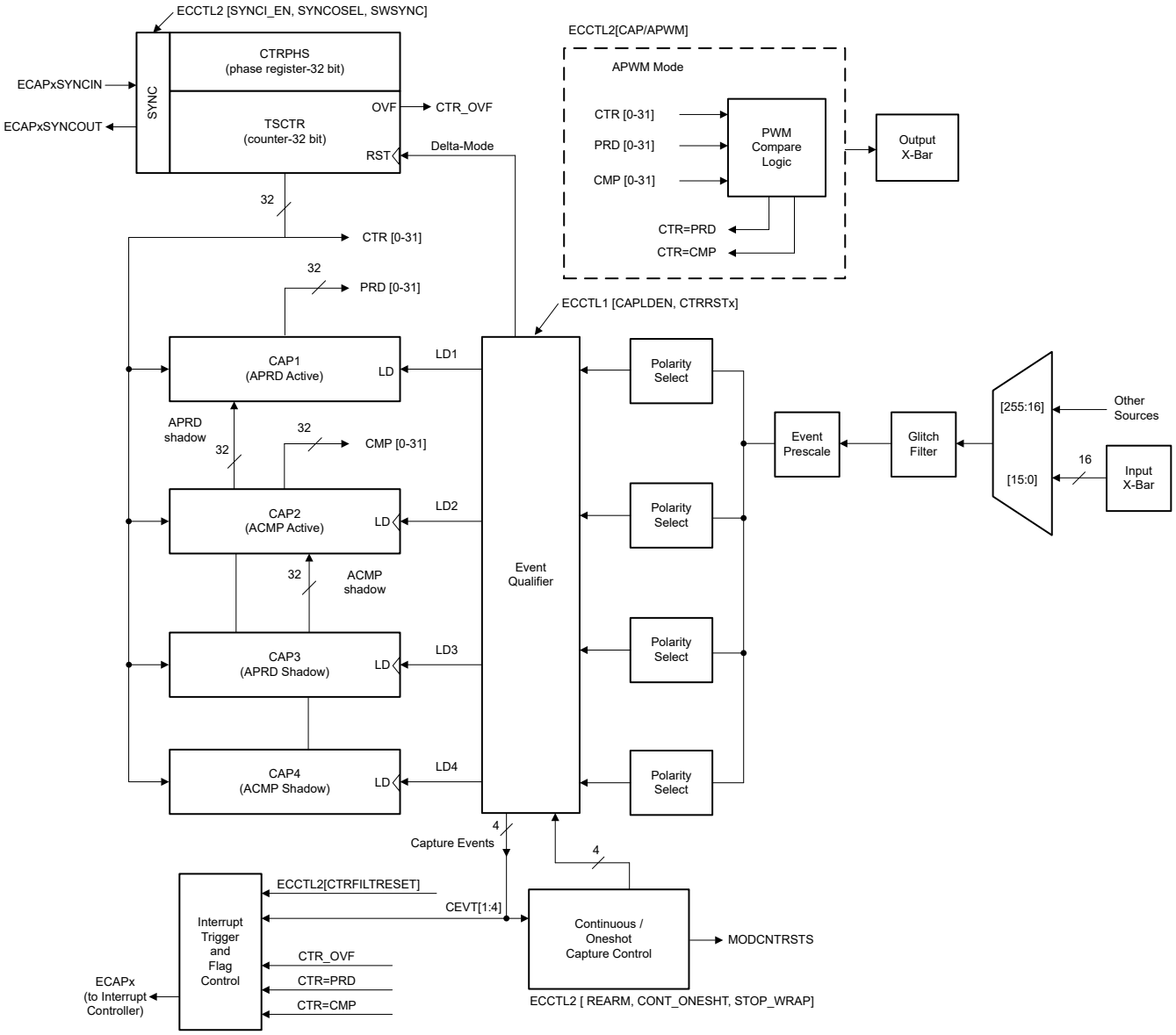


Figure 6-3. eCAP Block Diagram

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6.9.1.2 eCAP Synchronization

The eCAP modules can be synchronized with each other by selecting a common SYNCIN source. SYNCIN source for eCAP can be either software sync-in or external sync-in. The external sync-in signal can come from PWM, eCAP, or X-Bar. The SYNC signal is defined by the selection in the ECAPxSYNCINSEL[SEL] bit for ECAPx as shown in the diagram below.

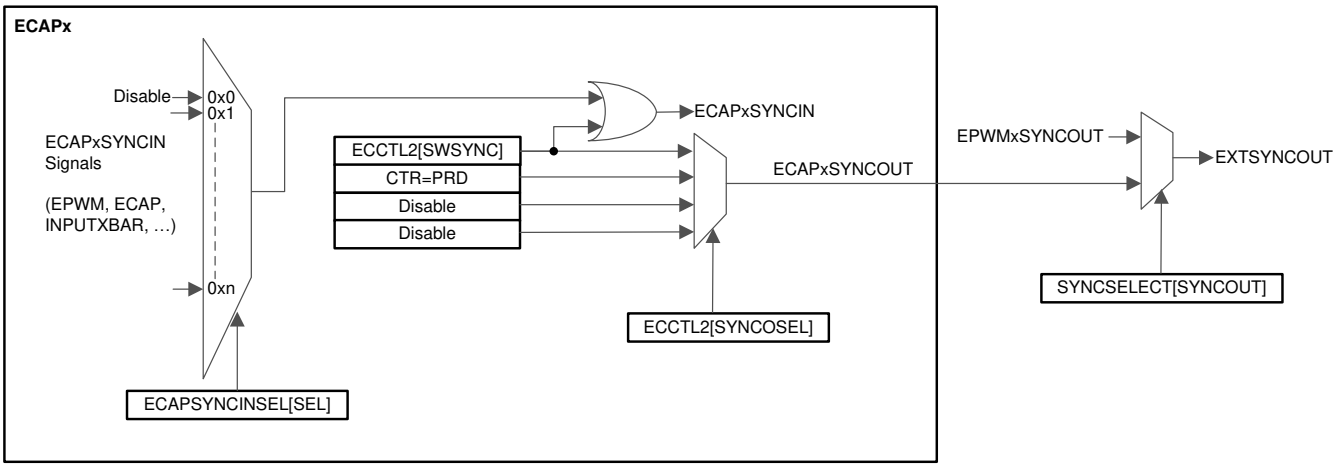


Figure 6-4. eCAP Synchronization Scheme

6.9.1.3 eCAP Electrical Data and Timing

6.9.1.3.1 eCAP Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SYSCLK)}$			ns
		Synchronous	$2t_{c(SYSCLK)}$			
		With input qualifier	$1t_{c(SYSCLK)} + t_{w_(IQSW)}$			

6.9.1.3.2 eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20			ns

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6.9.2 Enhanced Quadrature Encoder Pulse (eQEP)

The eQEP module on this device is Type-2. The eQEP interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position control systems.

The eQEP peripheral contains the following major functional units:

- Programmable input qualification for each pin (part of the GPIO MUX)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)
- Quadrature Mode Adapter (QMA)

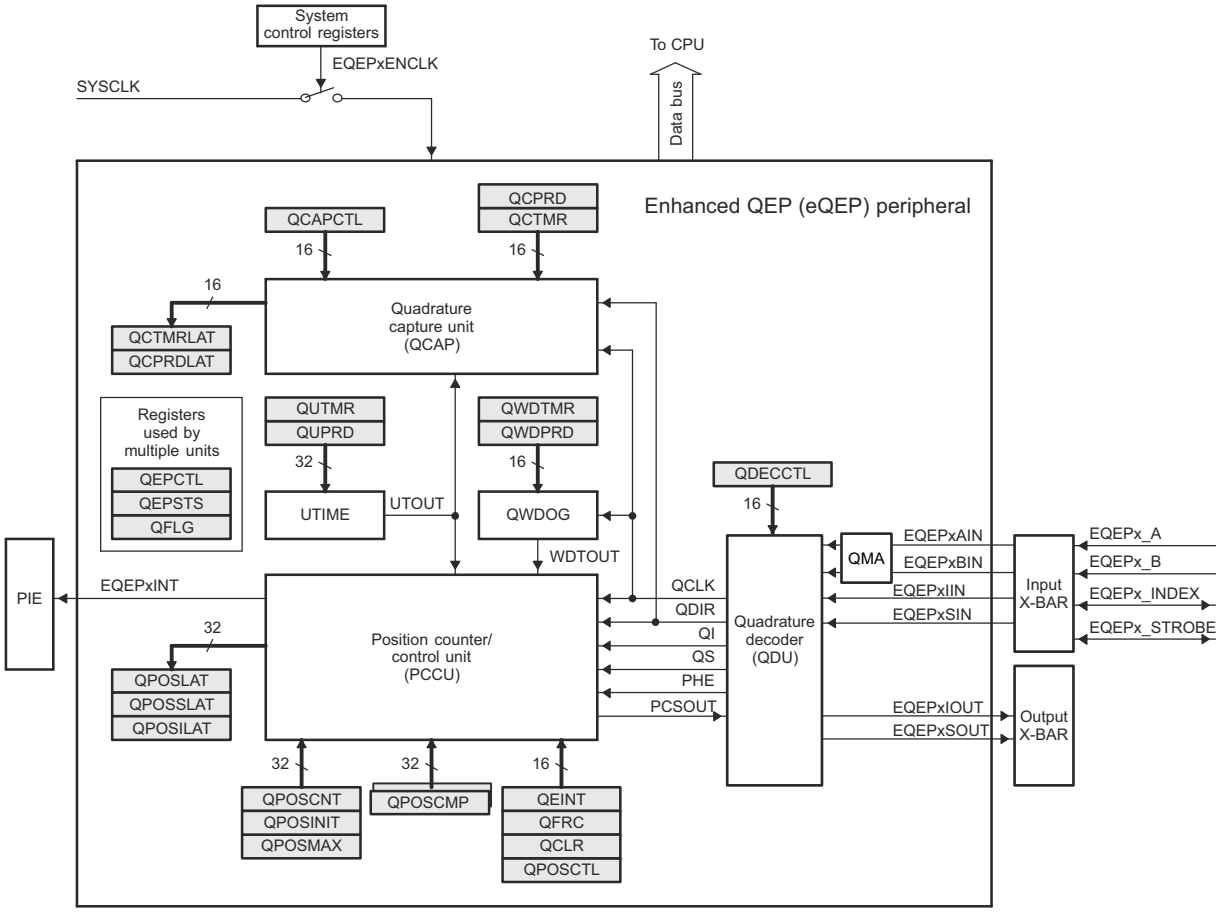


Figure 6-5. eQEP Block Diagram

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6.9.2.1 eQEP Electrical Data and Timing

6.9.2.1.1 eQEP Timing Requirements

			MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(QEPP)}$	QEP input period	Synchronous with input qualifier	$2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles

(1) The GPIO GPxQSELn Asynchronous mode should not be used for eQEP module input pins.

6.9.2.1.2 eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		$5t_{c(SYSCLK)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		$7t_{c(SYSCLK)}$	cycles

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6.9.3 Sigma-Delta Filter Module (SDFM)

SDFM features include:

- Eight external pins per SDFM module
  - Four sigma-delta data input pins per SDFM module (SD-Dx, where x = 1 to 4)
  - Four sigma-delta clock input pins per SDFM module (SD-Cx, where x = 1 to 4)
- Different configurable modulator clock modes supported:
  - Mode 0: Modulator clock rate equals the modulator data rate.
- Four independent, configurable secondary filter (comparator) units per SDFM module:
  - Four different filter type selection (Sinc1/Sinc2/SincFast/Sinc3) options available
  - Ability to detect over-value condition, under-value condition, and Threshold-crossing conditions
    1. Two independent Higher Threshold comparators (used to detect over-value condition)
    2. Two independent Lower Threshold comparators (used to detect under-value condition)
    3. One independent Threshold-Crossing comparator (used to measure duty cycle/frequency with eCAP)
  - OSR value for comparator filter unit (COSR) programmable from 1 to 32
- Four independent configurable primary filter (data filter) units per SDFM module:
  - Four different filter type selection (Sinc1/Sinc2/SincFast/Sinc3) options available
  - OSR value for data filter unit (DOSR) programmable from 1 to 256
  - Ability to enable or disable (or both) individual filter module
  - Ability to synchronize all four independent filters of an SDFM module by using the Main Filter Enable (MFE) bit or by using PWM signals
- Data filter output can be represented in either 16 bits or 32 bits.
- Data filter unit has a programmable mode FIFO to reduce interrupt overhead. The FIFO has the following features:
  - The primary filter (data filter) has a 16-deep x 32-bit FIFO.
  - The FIFO can interrupt the CPU after programmable number of data-ready events.
  - FIFO Wait-for-Sync feature: Ability to ignore data-ready events until the PWM synchronization signal (SDSYNC) is received. Once the SDSYNC event is received, the FIFO is populated on every data-ready event.
  - Data filter output can be represented in either 16 bits or 32 bits.
- PWMx.SOCA/SOCB can be configured to serve as SDSYNC source on a per-data-filter-channel basis.
- PWMs can be used to generate a modulator clock for sigma-delta modulators.
- Configurable Input Qualification available for both SD-Cx and SD-Dx
- Ability to use one filter channel clock (SD-C1) to provide clock to other filter clock channels.
- Configurable digital filter available on comparator filter events to blank out comparator events caused by spurious noise

Figure 6-6 shows the SDFM module block diagram.

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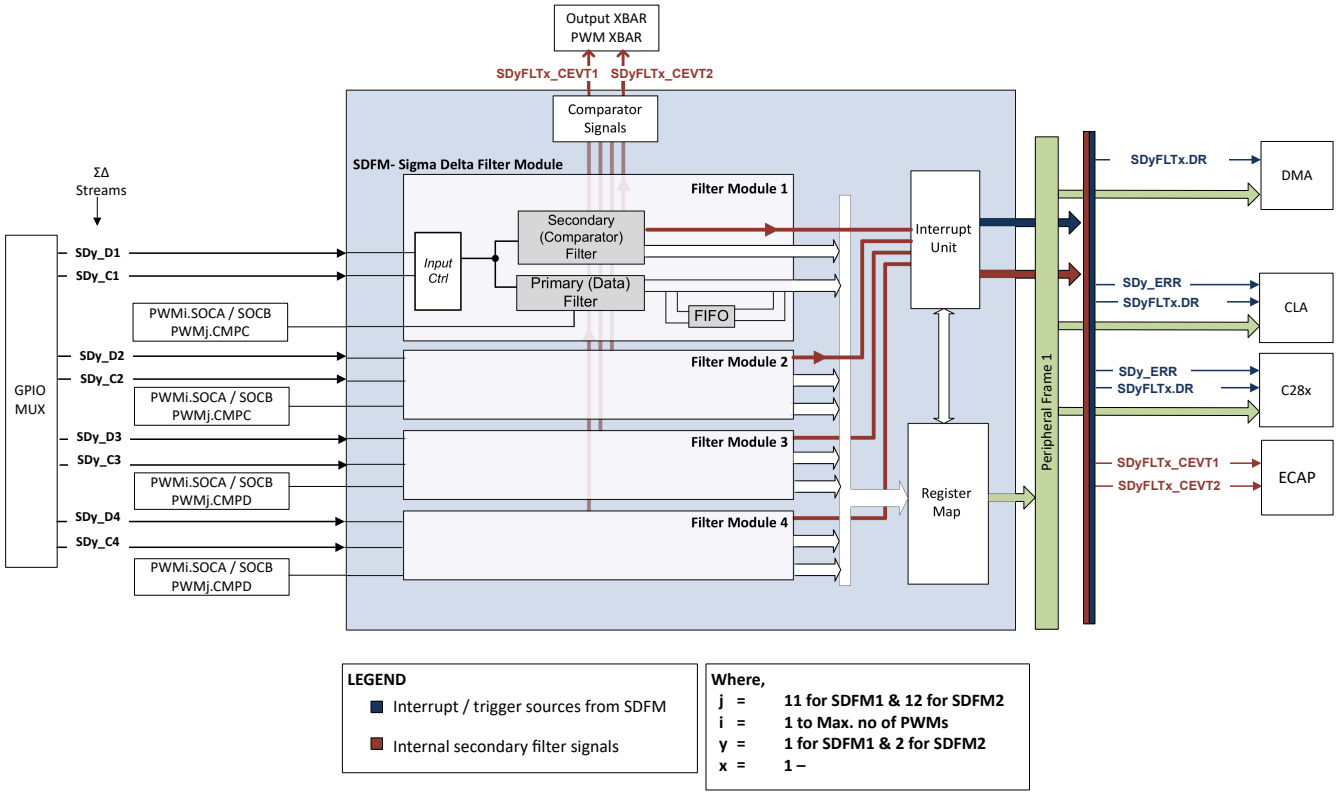


Figure 6-6. Sigma Delta Filter Module (SDFM) Block Diagram

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6.9.3.1 SDFM Electrical Data and Timing

6.9.3.1.1 SDFM Electrical Data and Timing (Synchronized GPIO)

When using this synchronized GPIO mode, the timing requirement for $t_{w(GPI)}$ pulse duration of $2t_{c(SYSCLK)}$ must be met. It is important for both SD-Cx and SD-Dx pairs to be configured with the SYNC option. This section lists the SDFM timing requirements when using the synchronized GPIO (SYNC) option. Figure 6-7 shows the SDFM timing diagram.

The *SDFM Timing Requirements When Using Synchronized GPIO - SYNC Option* table lists the SDFM timing requirements. The following configurations should be made:

- SDFM GPIO pins should be configured in SYNC mode only (using GPYQSELn = 00b).
- Both SDx-Cy and SDx-Dy signals should NOT be synchronized to PLLRAWCLK (using SDCTLPARMx.SDDATASYNC / SDCLKSYNC = 0b).

Note

The SDFM Synchronized GPIO (SYNC) option provides protection against SDFM module corruption due to occasional random noise glitches on the SDx_Cy pin that may result in a false comparator trip and filter output.

The SDFM Synchronized GPIO (SYNC) mode does not provide protection against persistent violations of the above timing requirements. Timing violations will result in data corruption proportional to the number of bits which violate the requirements.

6.9.3.1.1.1 SDFM Timing Requirements When Using Synchronized GPIO - SYNC Option

		MIN	MAX	UNIT
Mode 0				
$t_{c(SDC)M0}$	Cycle time, SDx_Cy	5 * SYSCLK period	256 * SYSCLK period	ns
$t_{w(SDCHL)M0}$	Pulse duration, SDx_Dy high / Low	2 * SYSCLK period	3 * SYSCLK period	ns
$t_{su(SDDV-SDCH)M0}$	Setup time, SDx_Dy valid before SDx_Cy goes high	2 * SYSCLK period		ns
$t_{h(SDCH-SDD)M0}$	Hold time, SDx_Dy wait after SDx_Cy goes high	2 * SYSCLK period		ns

6.9.3.1.2 SDFM Electrical Data and Timing (Using ASYNC)

The *SDFM Timing Requirements When Using Asynchronous GPIO ASYNC Option* table lists the SDFM timing requirements. The following configurations should be made:

- SDFM GPIO pins should be configured in ASYNC mode only (using GPYQSELn = 0b11).
- Both SDx-Cy and SDx-Dy signals need to be synchronized to PLLRAWCLK (using SDCTLPARMx registers).

Figure 6-7 shows the SDFM timing diagram.

6.9.3.1.2.1 SDFM Timing Requirements When Using Async GPIO and SDFM Sync to PLL

		MIN	MAX	UNIT
Mode 0				
$t_{c(SDC)M0}$	Cycle time, SDx_Cy	4 * $t_{c(PLLRAWCLK)}$	256 * SYSCLK period	ns
$t_{w(SDDHL)M0}$	Pulse duration, SDx_Dy (high / Low)	2 * $t_{c(PLLRAWCLK)}$		ns
$t_{su(SDDV-SDCH)M0}$	Setup time, SDx_Dy valid before SDx_Cy goes high	1 * $t_{c(PLLRAWCLK)}$ + 3		ns
$t_{h(SDCH-SDD)M0}$	Hold time, SDx_Dy wait after SDx_Cy goes high	1 * $t_{c(PLLRAWCLK)}$ + 3		ns

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6.9.3.1.3 SDFM Timing Diagram

WARNING

Special precautions should be taken on both SD-Cx and SD-Dx signals to ensure a clean and noise-free signal that meets SDFM timing requirements. Precautions such as series termination resistors for ringing noise due to any impedance mismatch of clock driver and spacing of traces from other noisy signals are recommended.

Note

The SDFM SD-Cx and SD-Dx signals, when synchronized to PLLRAWCLK, provide protection against SDFM module corruption due to occasional random noise glitches that may result in a false comparator trip and filter output. However, the signals do not provide protection against persistent violations of the above timing requirements. Timing violations will result in data corruption proportional to the number of bits which violate the requirements.

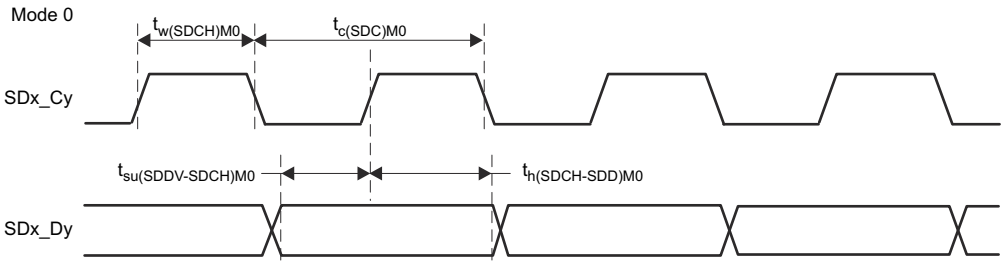


Figure 6-7. SDFM Timing Diagram – Mode 0

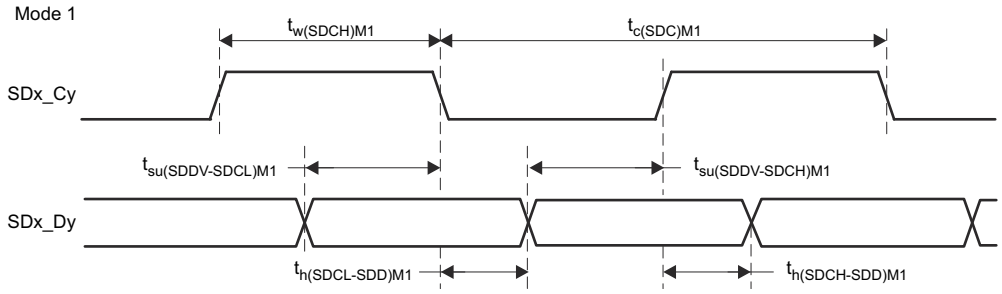


Figure 6-8. SDFM Timing Diagram – Mode 1

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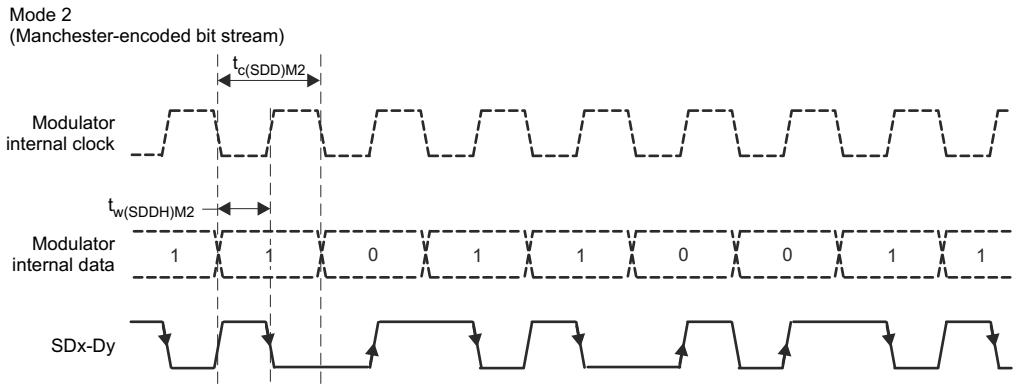


Figure 6-9. SDFM Timing Diagram – Mode 2

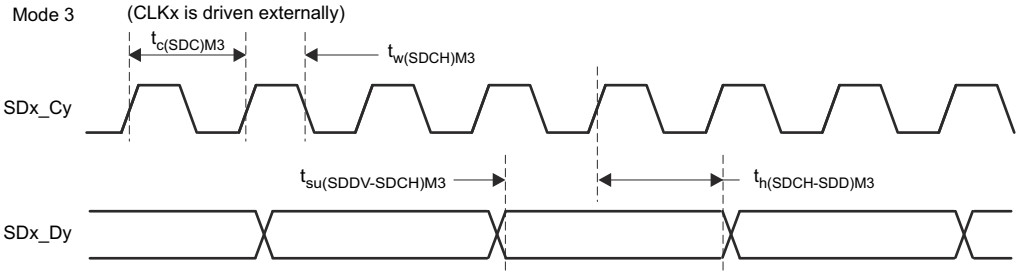


Figure 6-10. SDFM Timing Diagram – Mode 3

6.9.4 Multichannel Pulse Width Modulator (MCPWM)

The MCPWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The MCPWM module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the MCPWM module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

The MCPWM and eCAP synchronization scheme on the device provides flexibility in partitioning the MCPWM and eCAP modules and allows localized synchronization within the modules.

Figure 6-11 shows the MCPWM module.

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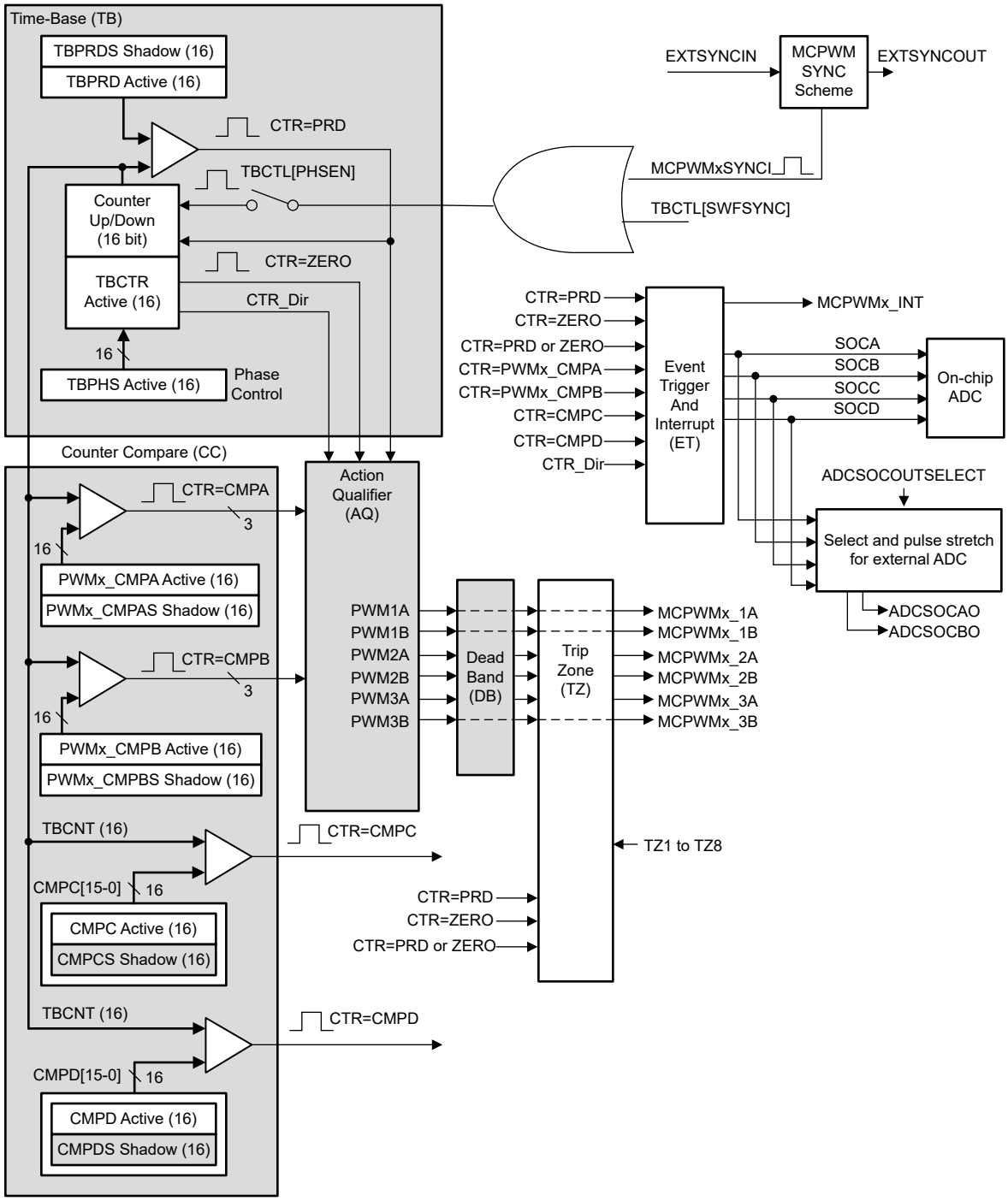


Figure 6-11. MCPWM Submodules and Critical Internal Signal Interconnects

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6.9.4.1 Control Peripherals Synchronization

The MCPWM and eCAP synchronization scheme on the device provides flexibility in partitioning the MCPWM and eCAP modules and allows localized synchronization within the modules. Figure 6-12 shows the synchronization scheme.

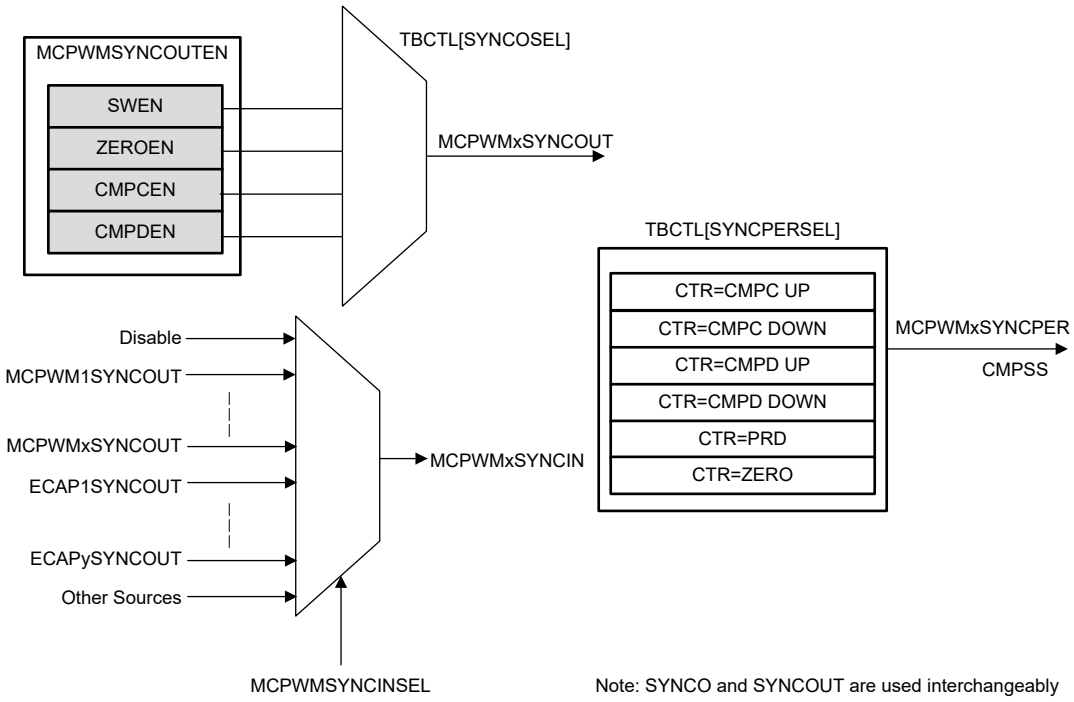


Figure 6-12. Synchronization Chain Architecture

6.9.4.2 MCPWM Electrical Data and Timing

6.9.4.2.1 MCPWM Timing Requirements

PARAMETER			MIN	MAX	UNIT
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		

6.9.4.2.2 MCPWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low	20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width	$8t_{c(SYSCLK)}$		cycles
$t_{d(TZ-PWM)}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM Hi-Z		30	ns
tskew	Skew of all MCPWM outputs (Shortest Path)(1)		5.1	ns
tskew	Skew of all MCPWM outputs (Longest Path)(1)		8.9	ns

(1) The MCPWMs have a similar configuration.

6.9.5 Enhanced Pulse Width Modulator (ePWM)

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type 4 module is able to generate complex pulse width

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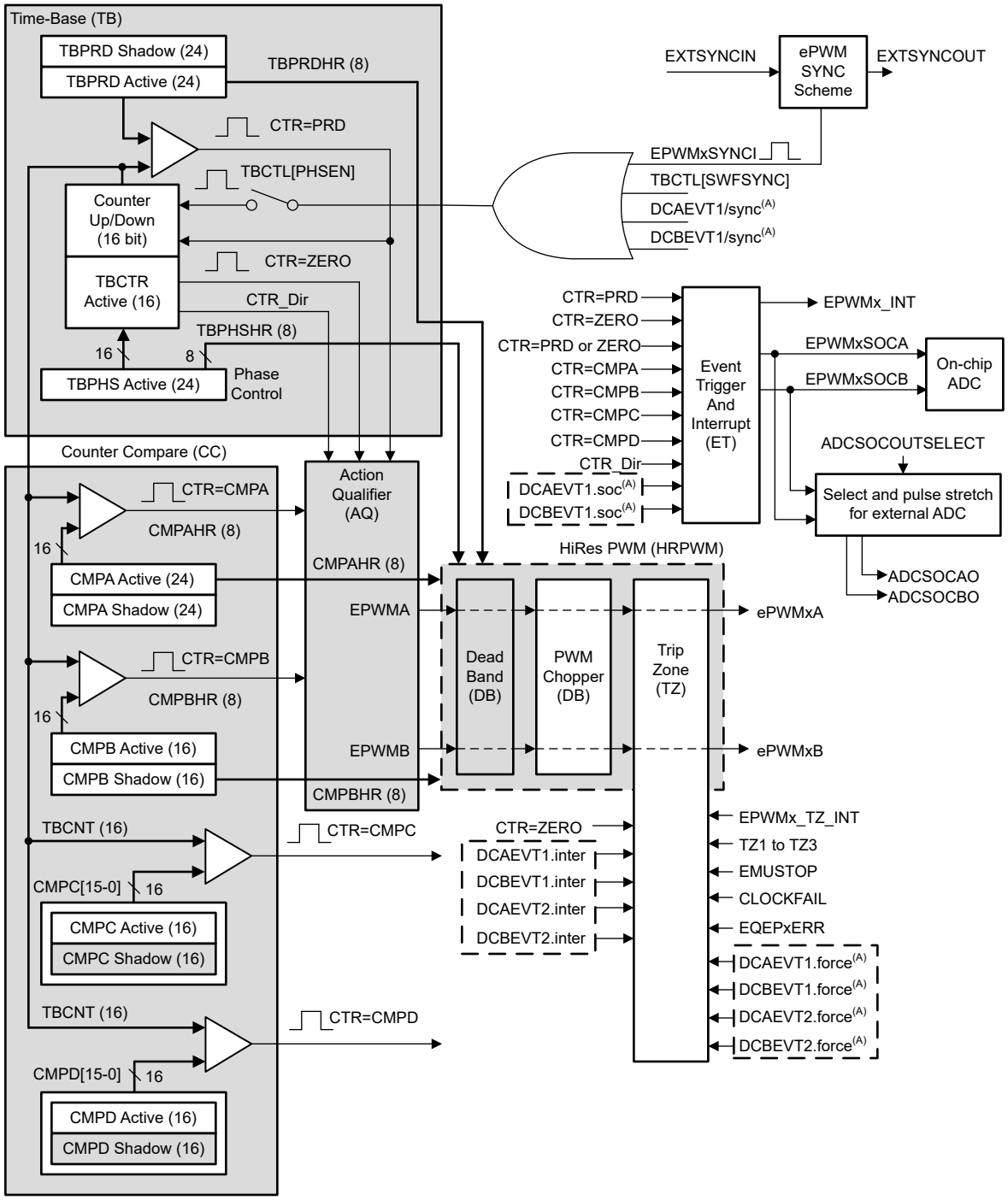
waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type 4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules.

Figure 6-11 shows the ePWM module.

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A. These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs.

Figure 6-13. ePWM Submodules and Critical Internal Signal Interconnects

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6.9.5.1 Control Peripherals Synchronization

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules. Figure 6-12 shows the synchronization scheme.

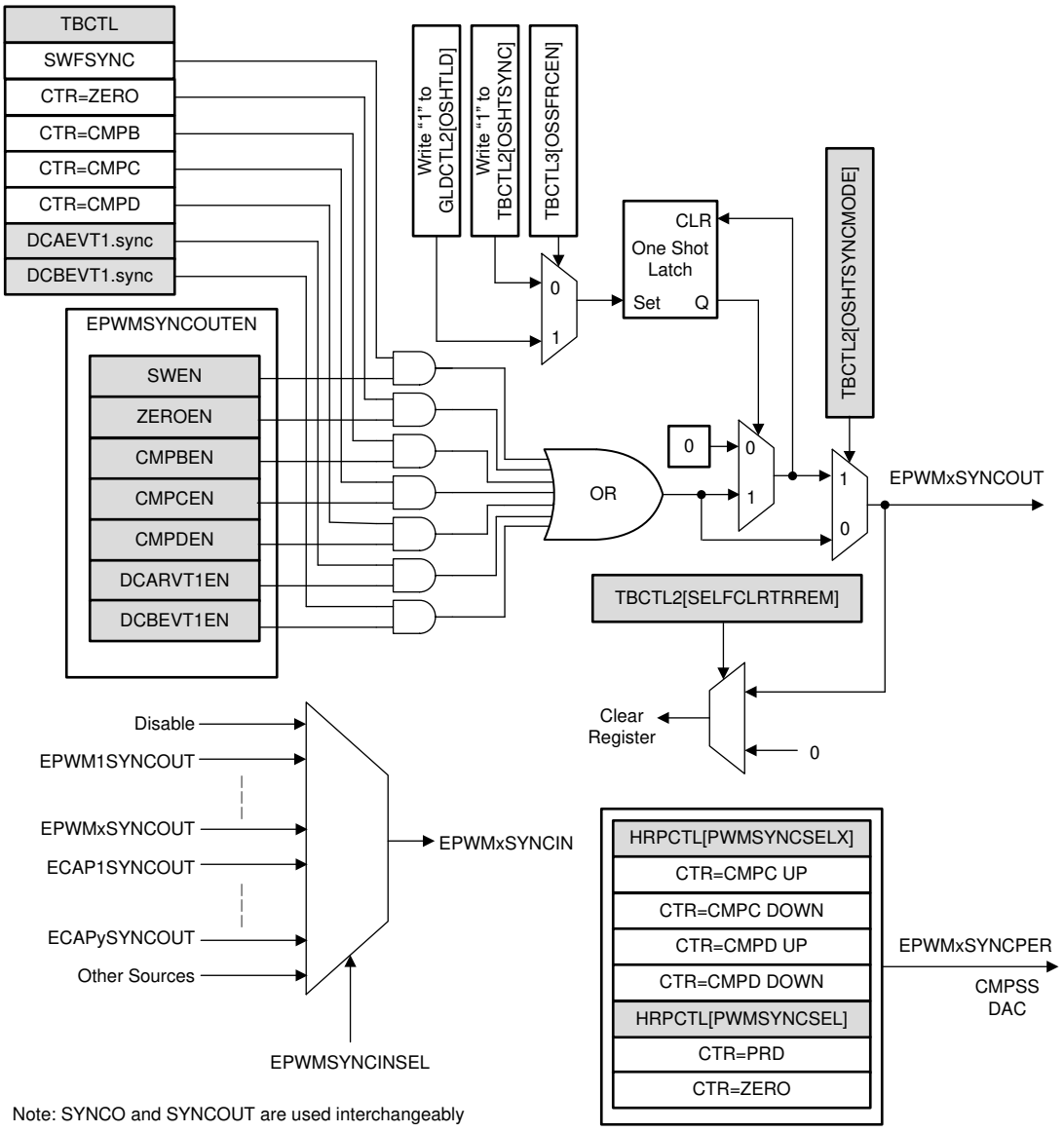


Figure 6-14. Synchronization Chain Architecture

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6.9.5.2 ePWM Electrical Data and Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.9.5.2.1 ePWM Timing Requirements

			MIN	MAX	UNIT
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		

6.9.5.2.2 ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER[1]		MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low	20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width	$8t_{c(SYSCLK)}$		cycles
$t_{d(TZ-PWM)}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM Hi-Z		25	ns

(1) 20-pF load on pin.

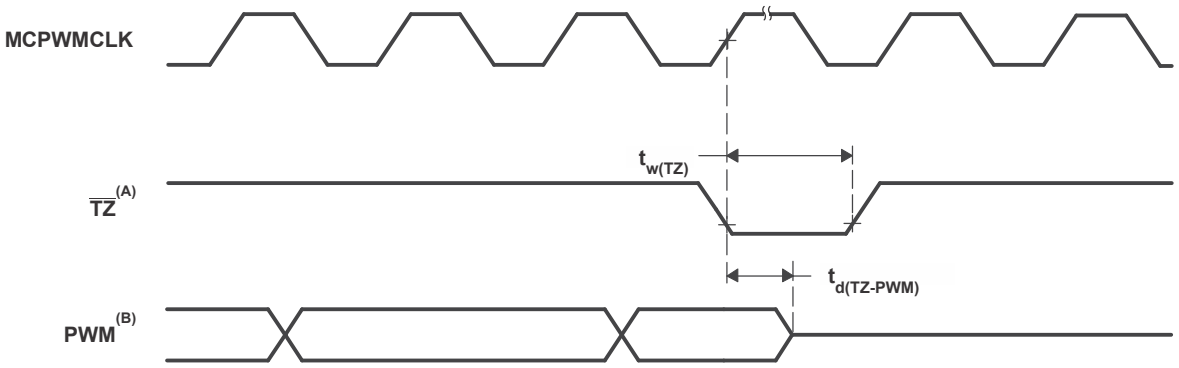
6.9.5.2.3 Trip-Zone Input Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.9.5.2.3.1 Trip-Zone Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZx}$ input low	Asynchronous	$1t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		cycles
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		cycles

6.9.5.2.3.2 PWM Hi-Z Characteristics Timing Diagram



A. $\overline{TZ}$: $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, TRIP1–TRIP12

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 6-15. PWM Hi-Z Characteristics

6.9.6 High-Resolution Pulse Width Modulator (HRPWM)

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module, there are two HR outputs:

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- HR Duty and Deadband control on Channel A
- HR Duty and Deadband control on Channel B

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A, B, phase, period and deadband registers of the ePWM module.

6.9.6.1 HRPWM Electrical Data and Timing

6.9.6.1.1 High-Resolution PWM Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1)	Micro Edge Positioning (MEP) step size(1)		75	152	ps

(1) The MEP step size will be largest at high temperature and minimum voltage on V_{DD}. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

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6.10 Communication Peripherals

6.10.1 UNICOMM (UART/I²C/SPI)

UNICOMM is a highly flexible peripheral which can be configured to operate with a UART, SPI, I²C Controller or a I²C Target protocol at runtime. A UNICOMM instance can only be configured for one protocol mode at a time. The user can select one of the serial interfaces during initialization. The peripheral uses shared 16-deep FIFOs in each UCx instance to maximize the device capability. A scalable peripheral group (SPG) combines one or more UNICOMM instances for special functions like inter-module internal loopback and I2C pairing. *UNICOMM (UCx) Serial Interface* describes the peripheral serial interfaces available on each UNICOMM instance and how these are grouped into SPG groupings on the device.

Table 6-4. UNICOMM (UCx) Serial Interface

SPG Instance	UNICOMM Instance	Supported Serial Protocols	Available Peripheral Types
SPG0 (PD1)	UC0	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC1	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC2	UART, LIN, I2C, SMBUS	Basic+ UART, Advanced I2C Controller/Target
SPG1 (PD1)	UC3	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC4	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC5	UART, LIN, I2C, SMBUS	Basic+ UART, Advanced I2C Controller/Target

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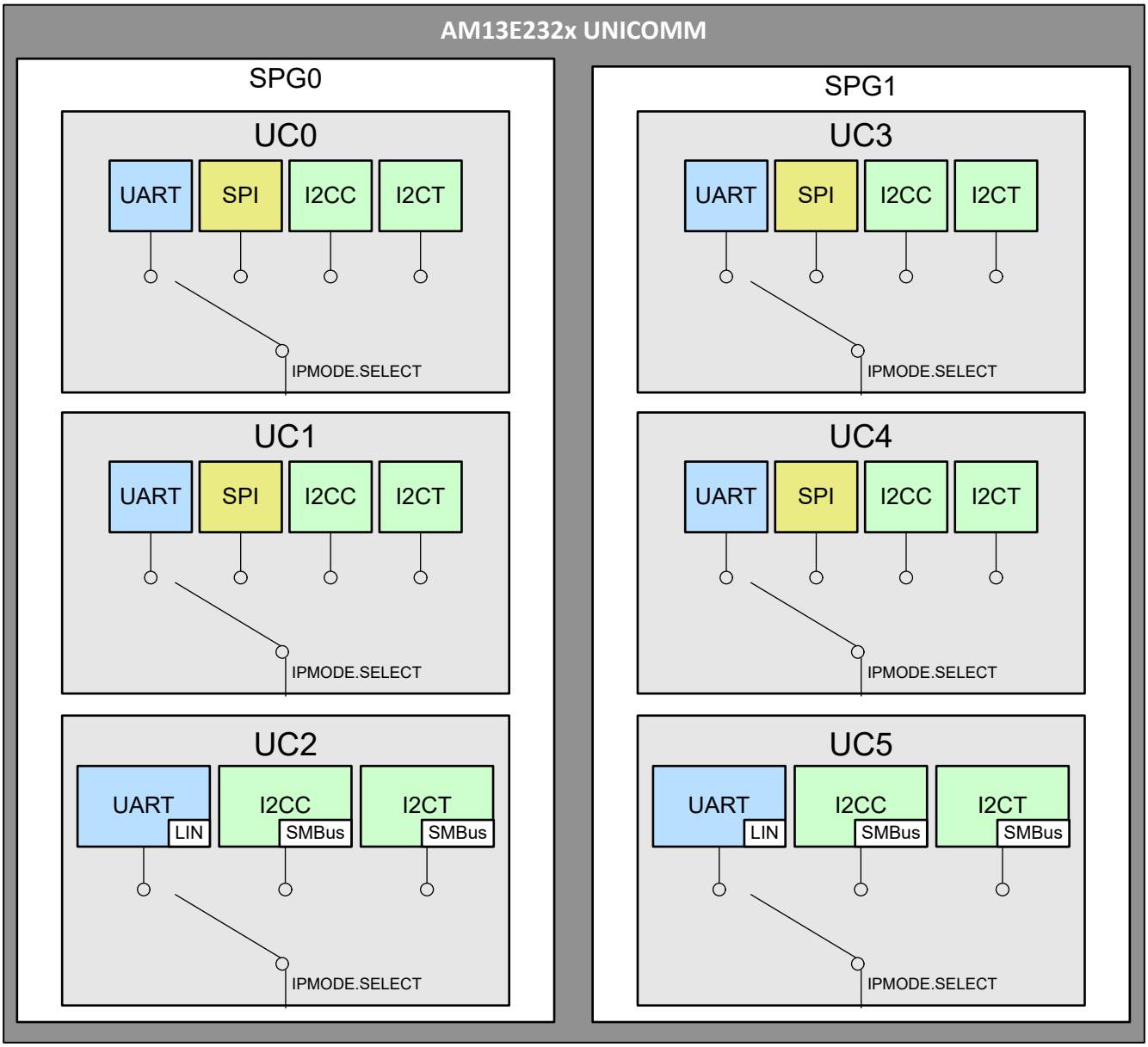


Figure 6-16. Unicomm Block Diagram

6.10.1.1 Universal Asychronous Receiver/Transmitter (UART)

The universal asychronous receiver/transmitter (UART) UNICOMM peripheral mode supports the following key features:

- Fully programmable serial interface:
  - 5, 6, 7 or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - LSB-first or MSB-first data transmit and receive
  - Line-break detection
  - Programmable baud-rate generation with oversampling by 16, 8 or 3
- Separate 16-deep transmit (TX) and receive (RX) FIFOs
- Direct Memory Access (DMA) Support

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- Local Interconnect Network (LIN) hardware support (Basic+ instances)
- Transmit to receive internal loopback mode operation
- Hardware Flow Control (CTS/RTS)
- RS485 Flow Control support
- Idle-line Multiprocessor Mode
- 9-Bit UART Mode
- ISO7816 Smartcard support (Basic instances)

See *UART (UNICOMM) Features* for more detailed information on supported features for individual UCx instances.

Table 6-5. UART (UNICOMM) Features

Supported Features	Basic Instances: UC0.UART, UC1.UART, UC3.UART,UC4.UART	Basic+ Instances: UC2.UART, UC5.UART
Active in Stop and Standby Mode	Yes	Yes
Hardware Flow Control (CTS/RTS)	Yes	Yes
9-bit Mode	Yes	Yes
LIN Mode	No	Yes
ISO7816 Smart Card	Yes	No
DMA Access / Support	Yes	Yes
Internal Loopback Support	Yes	Yes
Idle-line Multiprocessor Mode	Yes	Yes
RS485 Flow Control Mode	Yes	Yes

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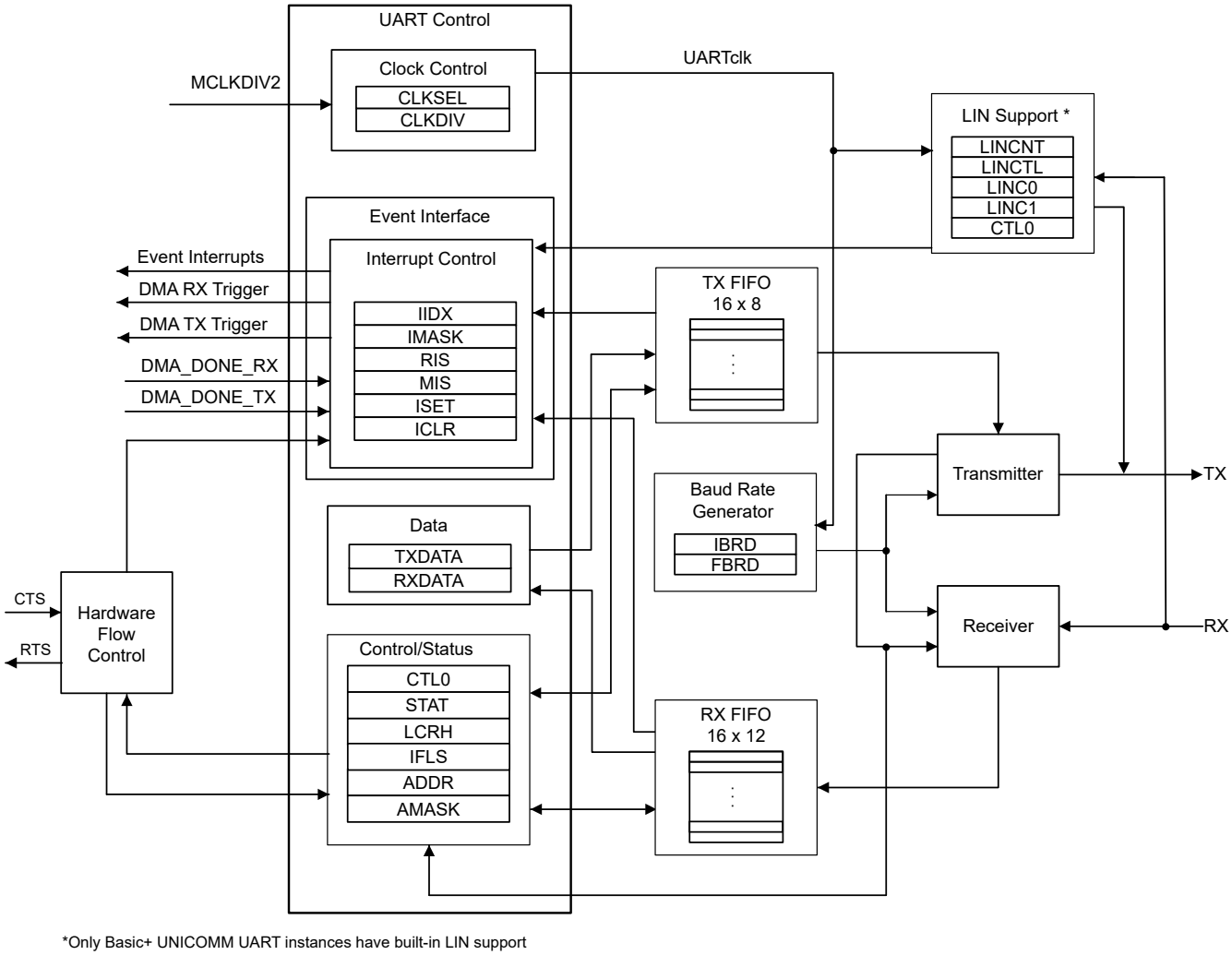


Figure 6-17. UART Functional Block Diagram

For more details, see the UART (UNICOMM) chapter of the *AM13E232x Microcontrollers Technical Reference Manual*.

6.10.1.1.1 UART Timings and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency	UART in Power Domain1			100	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)	UART in Power Domain1			12.5	Mbps
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

6.10.1.2 Inter-Integrated Circuit (I2C)

The inter-intergrated circuit (I2C) UNICOMM peripheral modes (I2C Controller and I2C Target) support the following key features:

- 7-bit and 10-bit addressing modes

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- Dual Addressing Support
- Standard-mode (Sm) Support, with a bit rate up to 100 kbit/s
- Fast-mode (Fm) Support, with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) Support, with a bit rate up to 1 Mbit/s
  - Supported on open drain IOs (ODIO) and high-drive (HDIO) IOs only
- Separate 16-deep transmit (TX) and receive (RX) FIFOs
- Direct Memory Access (DMA) Support
- SMBus 3.0 Support
  - Packet Error Checking (PEC)
  - Timeout Detection
  - Enhanced Frame Acknowledgement: Manual or Automatic
  - Default Device/Host/Alert Response Address
  - Target Arbitration
- Analog and Digital Glitch Suppresion

See *I2C Controller and Target (UNICOMM) Features* for more detailed information on supported features for individual UCx instances and I2C operating modes (I2C Controller and I2C Target).

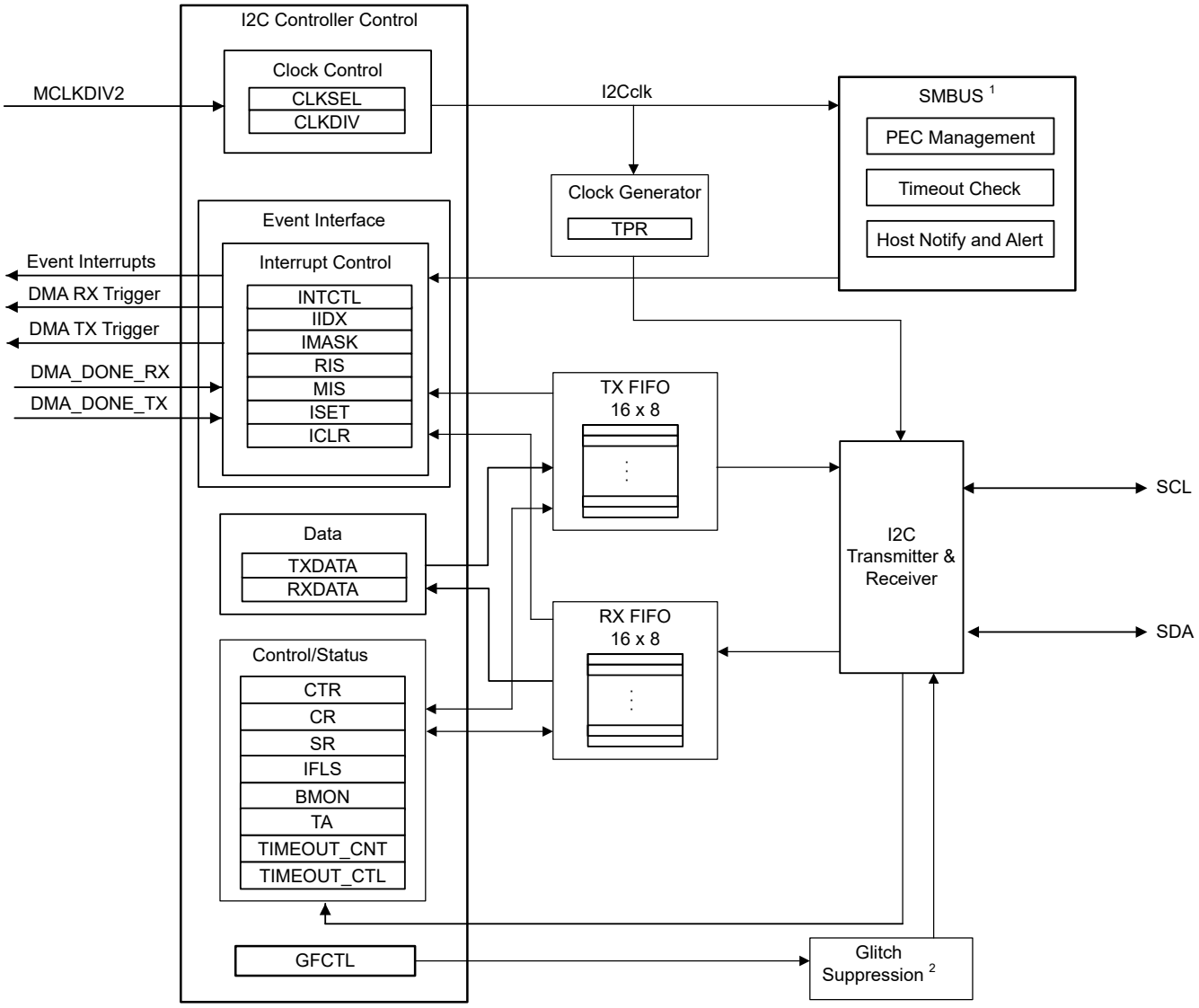
Table 6-6. I2C Controller and Target (UNICOMM) Features

Supported Features	I2C Controllers		I2C Targets	
	Basic Instances: UC0.I2CC, UC1.I2CC, UC3.I2CC, UC4.I2CC	Advanced Instances: UC2.I2CC, UC5.I2CC	Basic Instances: UC0.I2CT, UC1.I2CT, UC3.I2CT, UC4.I2CT	Advanced Instances: UC2.I2CT, UC5.I2CT
Standard-mode (Sm) Support	Yes	Yes	Yes	Yes
Fast-mode (Fm) Support	Yes	Yes	Yes	Yes
Fast-mode Plus (Fm+) Support	Yes	Yes	Yes	Yes
Analog Glitch Filtering	No	Yes	No	Yes
Digital Glitch Filtering	Yes	No	Yes	No
Burst Mode	No	Yes	-	-
SMBus v3.0 Support	No	Yes		
Dual Addressing	-	-	No	Yes

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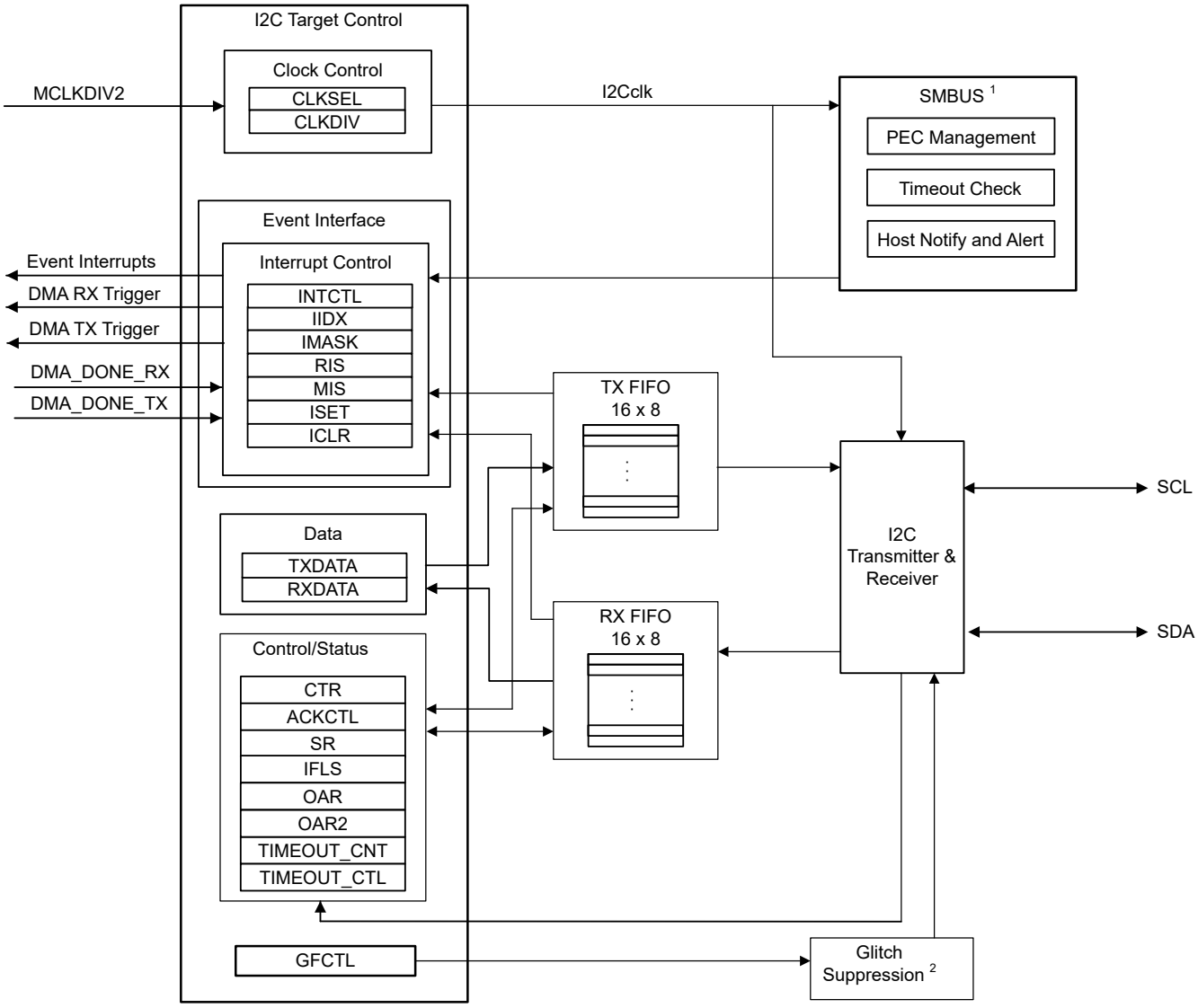
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[1] Only Advanced I2CC instances have built-in SMBUS support
[2] Basic I2CC instances have only digital glitch support and Advanced I2CC instances have only analog glitch support

Figure 6-18. I2C Controller (I2CC) Functional Block Diagram

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[1] Only Advanced I2CT instances have built-in SMBUS support
[2] Basic I2CT instances have only digital glitch support and Advanced I2CT instances have only analog glitch support

For more details, see the I2C (UNICOMM) chapter of the *AM13E232x Microcontrollers Technical Reference Manual*.

Figure 6-19. I2C Target (I2CT) Functional Block Diagram

6.10.1.2.1 I2C Timings and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency	I2C in Power Domain1, , MCLK = 200MHz		100		100		100	MHz
		I2C in Power Domain1, , MCLK = 250MHz		125		125		125	MHz
f_{SCL}	SCL clock frequency			0.1		0.4		1	MHz

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over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	LOW period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us
$t_{HD,DAT}$	Data hold time		0		0		0		ns
$t_{SU,DAT}$	Data setup time		250		100		50		ns
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	data valid acknowledge time			3.45		0.9		0.45	us

6.10.1.2.2 I2C Filter Timings

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

6.10.1.2.3 I²C Timing Diagram

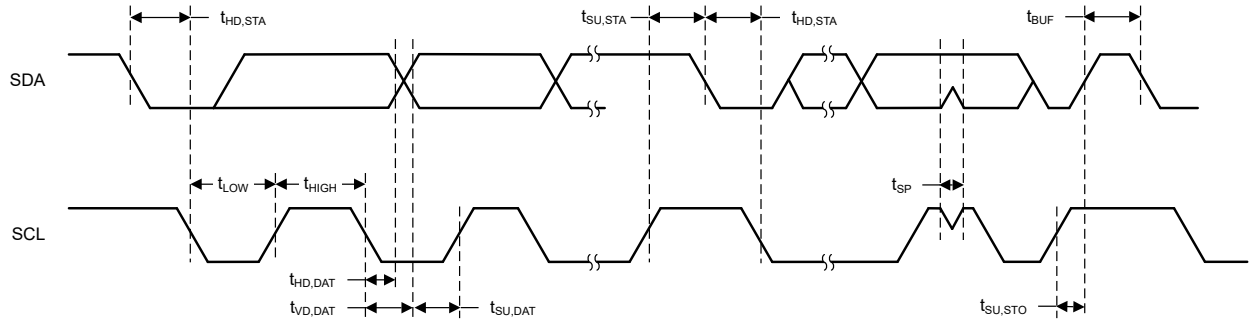


Figure 6-20. I2C Timing Diagram

6.10.1.3 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) UNICOMM peripheral mode supports the following key features:

- Supports up to 40 Mbits/s in both controller and peripheral mode [1]
- Controller or Peripheral Modes
- Separate 16-deep transmit (TX) and receive (RX) FIFOs
- Direct Memory Access (DMA) Support
- Single Parity for Transmit and Receive
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4-16 bits (controller mode) and 7-16 bits (peripheral mode)
- Texas Instruments Synchronous Serial and Motorola SPI Frame Format Support

[1] Only SPI signals on HSIO pins support data rates up to 40 Mbits/s; see the *Pin Diagrams* section for HSIO pins.

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All UCx instances with SPI peripheral mode available on this device (UC0.SPI, UC1.SPI, UC3.SPI, and UC4.SPI) support all of the above features.

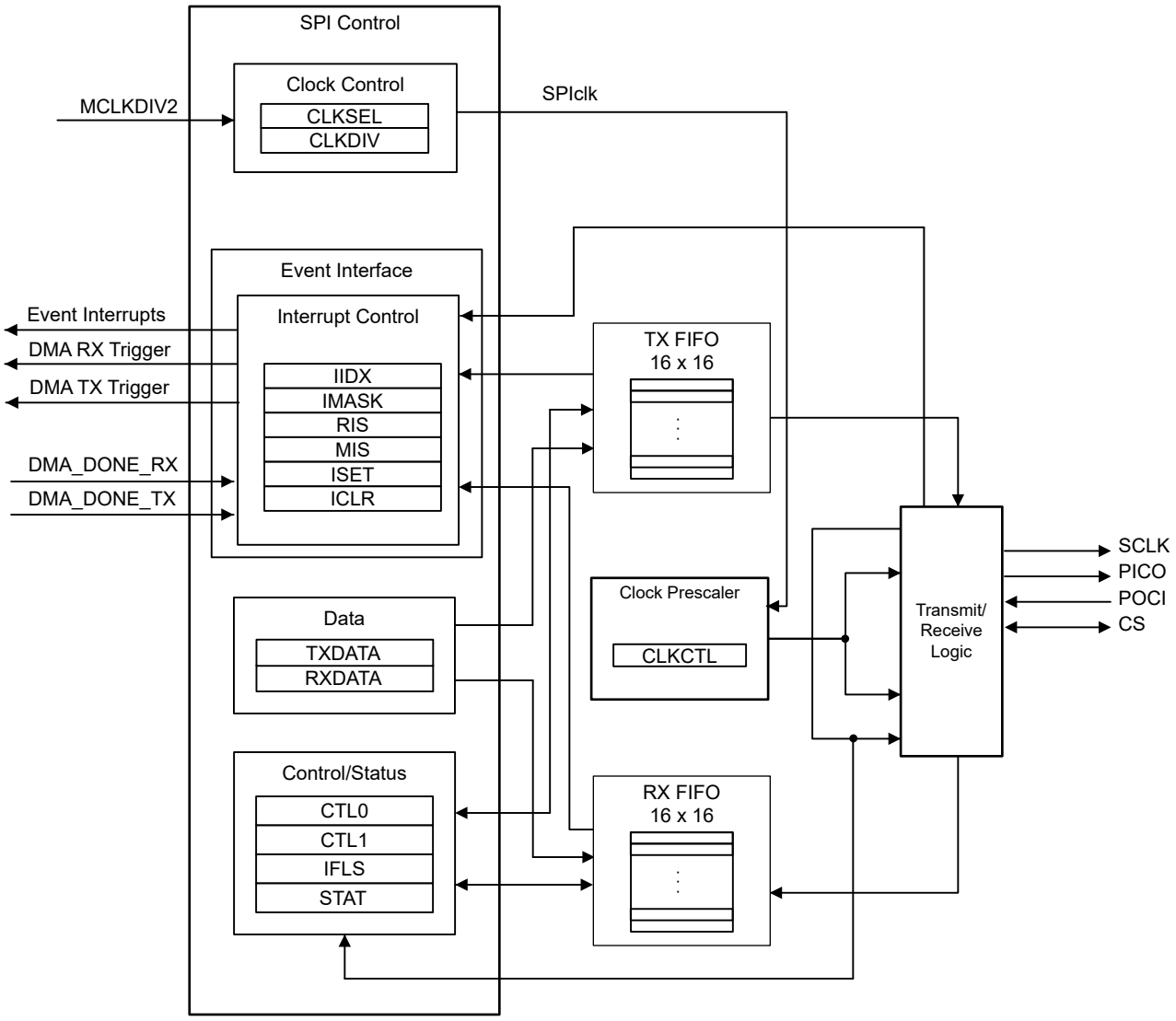


Figure 6-21. SPI Functional Block Diagram

For more details, see the SPI (UNICOMM) chapter of the *AM13E232x Microcontrollers Technical Reference Manual*.

6.10.1.3.1 SPI Timings and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		MIN	TYP	MAX	UNIT
SPI					
f_{SPI}	SPI clock frequency, MCLK = 200MHz			25	MHz
	SPI clock frequency, MCLK = 250MHz			31.25	MHz
DC_{SCK}	SCK Duty Cycle	40	50	60	%
Controller					
$t_{SCLK_H/L}$	SCLK High or Low time	(tSPI/2) - 1	tSPI / 2	(tSPI/2) + 1	ns

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over operating free-air temperature range (unless otherwise noted)

PARAMETERS		MIN	TYP	MAX	UNIT
$t_{CS.LEAD}$	CS lead-time, CS active to clock	1 SPI Clock - 3	1 SPI Clock		ns
		1/2 SPI Clock - 3	1/2 SPI Clock		ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	1 SPI Clock - 3	1 SPI Clock		ns
$t_{CS.ACC}$	CS access time, CS active to PICO data out		1/2 SPI Clock	1/2 SPI Clock + 3	ns
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high inpedance		1 SPI Clock	1 SPI Clock + 3	ns
$t_{SU.CI}$	POCI input data setup time (1)	1			ns
$t_{HD.CI}$	POCI input data hold time	20			ns
$t_{SU.CI}$	POCI input data setup time (1)	18			ns
$t_{HD.CI}$	POCI input data hold time	0			ns
$t_{VALID.CO}$	PICO output data valid time (2)			3	ns
$t_{HD.CO}$	PICO output data hold time (3)	-3			ns
Peripheral					
$t_{CS.LEAD}$	CS lead-time, CS active to clock	19			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	1			ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out			25	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high impedance			39	ns
$t_{SU.PI}$	PICO input data setup time	7			ns
$t_{HD.PI}$	PICO input data hold time	0			ns
$t_{VALID.PO}$	POCI output data valid time(2)			19	ns
$t_{HD.PO}$	POCI output data hold time(3)	3			ns

(1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge

6.10.1.3.2 SPI Timing Diagram

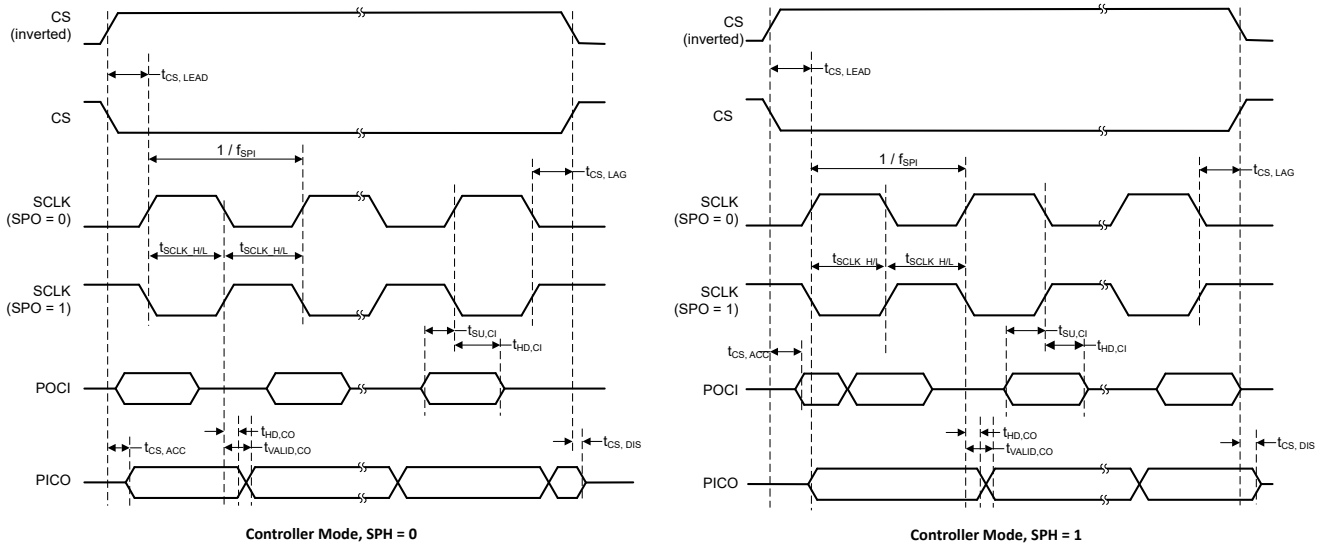


Figure 6-22. SPI Timing Diagram - Controller Mode

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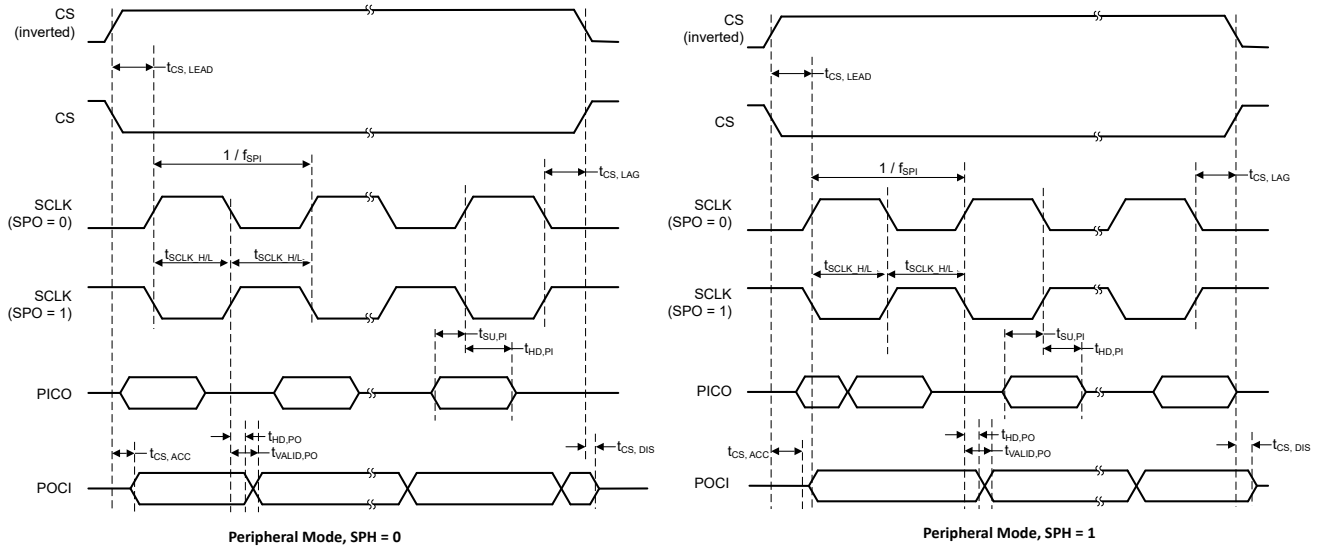


Figure 6-23. SPI Timing Diagram - Peripheral Mode

6.10.2 Modular Controller Area Network (MCAN)

The Modular Controller Area Network (MCAN) controller enables communication with a CAN2.0A, CAN2.0B, or CAN-FD bus and is compliant to ISO 11898-1:2015 standard supporting up to 1-Mbps nominal bit rate, up to 8-Mbps data bit rate. Key features of the CAN-FD peripheral include:

- Full support for 64-byte CAN-FD frames
- Dedicated 1KB message SRAM with ECC
- Configurable transmit FIFO, transmit queue and event FIFO (up to 32 elements)
- Up to 32 dedicated transmit buffers and 64 dedicated receive buffers
- Two configurable receive FIFOs (up to 64 elements each)
- Up to 128 filter elements
- Two interrupt lines
- Power-down and wake-up support
- Timestamp counter

For more details, see the Modular Controller Area Network (MCAN) chapter of the *AM13E232x Microcontrollers Technical Reference Manual*.

6.10.2.1 CAN Timings and Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CANCLK}	CAN input clock frequency	MCLK=250MHz			125	MHZ
		MCLK=200MHz			100	
f_{BAUD}	CAN Baud rate				8	Mbps

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6.10.3 Fast Serial Interface (FSI)

The Fast Serial Interface (FSI) module is a serial communication peripheral capable of reliable and robust high-speed communications. The FSI is designed to ensure data robustness across many system conditions such as chip-to-chip as well as board-to-board across an isolation barrier. Payload integrity checks such as CRC, start- and end-of-frame patterns, and user-defined tags, are encoded before transmit and then verified after receipt without additional CPU interaction. Line breaks can be detected using periodic transmissions, all managed and monitored by hardware. The FSI is also tightly integrated with other control peripherals on the device. To ensure that the latest sensor data or control parameters are available, frames can be transmitted on every control loop period. An integrated skew-compensation block has been added on the receiver to handle skew that may occur between the clock and data signals due to a variety of factors, including trace-length mismatch and skews induced by an isolation chip. With embedded data robustness checks, data-link integrity checks, skew compensation, and integration with control peripherals, the FSI can enable high-speed, robust communication in any system. These and many other features of the FSI follow.

The FSI module includes the following features:

- Independent transmitter and receiver cores
- Source-synchronous transmission
- Dual data rate (DDR)
- One or two data lines
- Programmable data length
- Skew adjustment block to compensate for board and system delay mismatches
- Frame error detection
- Programmable frame tagging for message filtering
- Hardware ping to detect line breaks during communication (ping watchdog)
- Two interrupts per FSI core
- Externally triggered frame generation
- Hardware- or software-calculated CRC
- Embedded ECC computation module
- Register write protection
- DMA support
- SPI compatibility mode (limited features available)

Operating the FSI at maximum speed (60 MHz) at dual data rate (120Mbps) may require the integrated skew compensation block to be configured according to the specific operating conditions on a case-by-case basis. The *Fast Serial Interface (FSI) Skew Compensation* Application Note provides example software on how to configure and set up the integrated skew compensation block on the Fast Serial Interface.

The FSI consists of independent transmitter (FSITX) and receiver (FSIRX) cores. The FSITX and FSIRX cores are configured and operated independently. The features available on the FSITX and FSIRX are described in the *FSI Transmitter* section and the *FSI Receiver* section of the *AM13E232x Microcontrollers Technical Reference Manual*, respectively.

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6.10.3.1 FSI Transmitter

The FSI transmitter module handles the framing of data, CRC generation, signal generation of TXCLK, TXD0, and TXD1, as well as interrupt generation. The operation of the transmitter core is controlled and configured through programmable control registers. The transmitter control registers let the CPU program, control, and monitor the operation of the FSI transmitter. The transmit data buffer is accessible by the CPU and the DMA.

The transmitter has the following features:

- Automated ping frame generation
- Externally triggered ping frames
- Software-configurable frame lengths
- 16-word data buffer
- Data buffer underrun and overrun detection
- Hardware-generated CRC on data bits
- Software ECC calculation on select data
- DMA support

Figure 6-24 shows the FSITX CPU interface. Figure 6-25 shows the high-level block diagram of the FSITX. Not all data paths and internal connections are shown. This diagram provides a high-level overview of the internal modules present in the FSITX.

Figure 6-24. FSITX CPU Interface

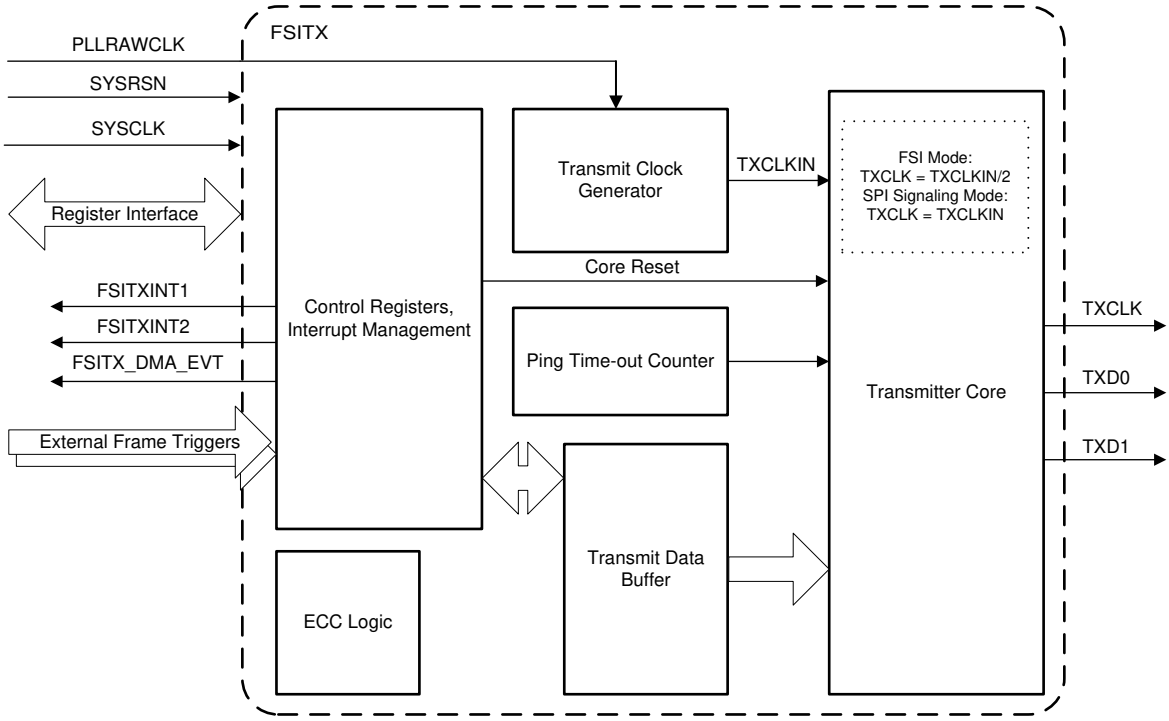


Figure 6-25. FSITX Block Diagram

6.10.3.1.1 FSITX Electrical Data and Timing

6.10.3.1.1.1 FSITX Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER[1]		MIN	MAX	UNIT
1	$t_{c(TXCLK)}$	Cycle time, TXCLK		19.4	ns
2	$t_{w(TXCLK)}$	Pulse width, TXCLK low or TXCLK high	$(0.5t_{c(TXCLK)}) – 1$	$(0.5t_{c(TXCLK)}) + 1$	ns
3	$t_{d(TXCLK–TXD)}$	Delay time, TXCLK rising or falling toTXD valid	$(0.25t_{c(TXCLK)}) – 2$	$(0.25t_{c(TXCLK)}) + 2$	ns

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over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER(1)		MIN	MAX	UNIT
4	$t_{d(TXCLK)}$	TXCLK delay compensation at TX_DLYLINE_CTRL[TXCLK_DLY]=31	9.4	35	ns
5	$t_{d(TXD0)}$	TXD0 delay compensation at TX_DLYLINE_CTRL[TXD0_DLY]=31	9.4	35	ns
6	$t_{d(TXD1)}$	TXD1 delay compensation at TX_DLYLINE_CTRL[TXD1_DLY]=31	9.4	35	ns
7	$t_{d(DELAY_ELEMENT)}$	Incremental delay of each delay line element for TXCLK, TXD0, and TXD1	0.27	1.1	ns

(1) 10-pF load on pin.

6.10.3.1.2 FSITX Timings

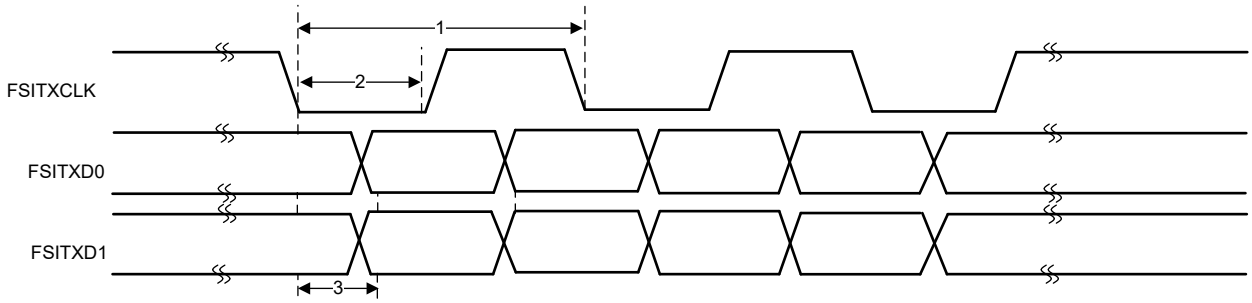


Figure 6-26. FSITX Timings

6.10.3.2 FSI Receiver

The receiver module interfaces to the FSI clock (RXCLK), and data lines (RXD0 and RXD1) after they pass through an optional programmable delay line. The receiver core handles the data framing, CRC computation, and frame-related error checking. The receiver bit clock and state machine are run by the RXCLK input, which is asynchronous to the device system clock.

The receiver control registers let the CPU program, control, and monitor the operation of the FSIRX. The receive data buffer is accessible by the CPU, and the DMA.

The receiver core has the following features:

- 16-word data buffer
- Multiple supported frame types
- Ping frame watchdog
- Frame watchdog
- CRC calculation and comparison in hardware
- ECC detection
- Programmable delay line control on incoming signals
- DMA support
- SPI compatibility mode

Figure 6-27 shows the FSIRX CPU interface. Figure 6-28 provides a high-level overview of the internal modules present in the FSIRX. Not all data paths and internal connections are shown.

Figure 6-27. FSIRX CPU Interface

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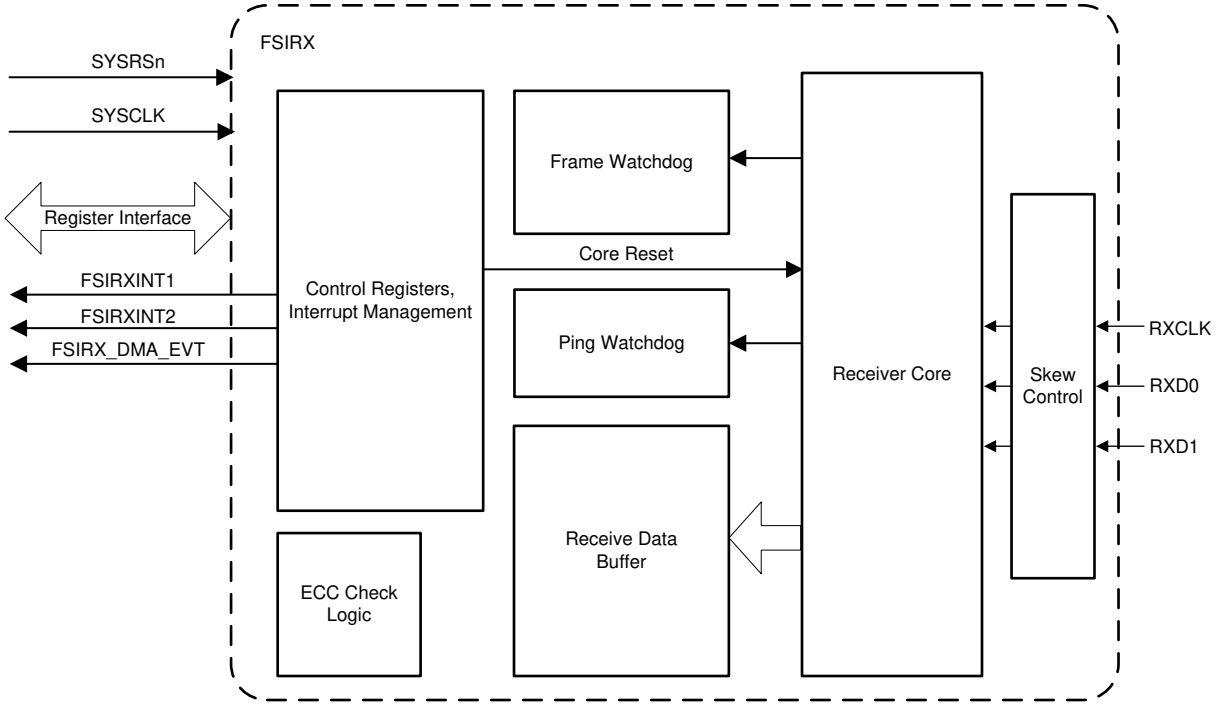


Figure 6-28. FSIRX Block Diagram

6.10.3.2.1 FSIRX Electrical Data and Timing

6.10.3.2.1.1 FSIRX Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(RXCLK)}$	Cycle time, RXCLK		16.67	ns
2	$t_{w(RXCLK)}$	Pulse width, RXCLK low or RXCLK high.	$0.35t_{c(RXCLK)}$	$0.65t_{c(RXCLK)}$	ns
3	$t_{su(RXCLK–RXD)}$	Setup time with respect to RXCLK, applies to both edges of the clock	1.7		ns
4	$t_{h(RXCLK–RXD)}$	Hold time with respect to RXCLK, applies to both edges of the clock	2		ns

6.10.3.2.1.2 FSIRX Switching Characteristics

NO.	PARAMETER[1]		MIN	MAX	UNIT
1	$t_{d(RXCLK)}$	RXCLK delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31	9.7	35	ns
2	$t_{d(RXD0)}$	RXD0 delay compensation at RX_DLYLINE_CTRL[RXD0_DLY]=31	9.7	35	ns
3	$t_{d(RXD1)}$	RXD1 delay compensation at RX_DLYLINE_CTRL[RXD1_DLY]=31	9.7	35	ns
4	$t_{d(DELAY_ELEMENT)}$	Incremental delay of each delay line element for RXCLK, RXD0, and RXD1	0.27	1.1	ns
TDM1	$t_{skew(TDM_CLK-TDM_Dx)}$	Delay skew introduced between RXCLK-TDM_CLK delay and RXDx-TDM_Dx delays	-3	3	ns
TDM1	$t_{d(RXCLK-TDM_CLK)}$	Delay time, RXCLK input to TDM_CLK output	2	14.5	ns
TDM2	$t_{d(RXD0-TXD0)}$	Delay time, RXD0 input to TXD0 output	2	14.5	ns
TDM3	$t_{d(RXD1-TXD1)}$	Delay time, RXD1 input to TXD1 output	2	14.5	ns

(1) 10-pF load on pin.

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6.10.3.2.2 FSIRX Timings

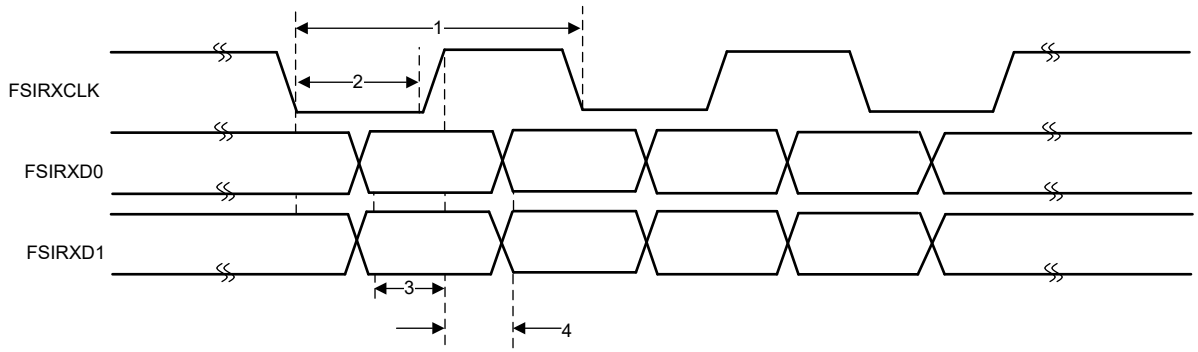


Figure 6-29. FSIRX Timings

6.10.3.3 FSI SPI Compatibility Mode

The FSI supports a SPI compatibility mode to enable communication with programmable SPI devices. In this mode, the FSI transmits its data in the same manner as a SPI in a single clock configuration mode. While the FSI is able to physically interface with a SPI in this mode, the external device must be able to encode and decode an FSI frame to communicate successfully. This is because the FSI transmits all SPI frame phases with the exception of the preamble and postamble. The FSI provides the same data validation and frame checking as if it was in standard FSI mode, allowing for more robust communication without consuming CPU cycles. The external SPI is required to send all relevant information and can access standard FSI features such as the ping frame watchdog on the FSIRX, frame tagging, or custom CRC values. The list of features of SPI compatibility mode follows:

- Data will transmit on rising edge and receive on falling edge of the clock.
- Only 16-bit word size is supported.
- TXD1 will be driven like an active-low chip-select signal. The signal will be low for the duration of the full frame transmission.
- No receiver chip-select input is required. RXD1 is not used. Data is shifted into the receiver on every active clock edge.
- No preamble or postamble clocks will be transmitted. All signals return to the idle state after the frame phase is finished.
- It is not possible to transmit in the SPI peripheral configuration because the FSI TXCLK cannot take an external clock source.

6.10.3.3.1 FSITX SPI Signaling Mode Electrical Data and Timing

Special timings are not required for the FSIRX in SPI signaling mode. FSIRX timings listed in the *FSIRX Timing Requirements* table are applicable in SPI compatibility mode. Setup and Hold times are only valid on the falling edge of FSIRXCLK because this is the active edge in SPI signaling mode.

6.10.3.3.1.1 FSITX SPI Signaling Mode Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER[1]		MIN	MAX	UNIT
1	$t_{c(TXCLK)}$	Cycle time, TXCLK		19.4	ns
2	$t_{w(TXCLK)}$	Pulse width, TXCLK low or TXCLK high	$(0.5t_{c(TXCLK)}) - 1$	$(0.5t_{c(TXCLK)}) + 1$	ns
3	$t_{d(TXCLKH–TXD0)}$	Delay time, TXD0 valid after TXCLK high		3	ns
4	$t_{d(TXD1-TXCLK)}$	Delay time, TXCLK high after TXD1 low	$t_{w(TXCLK)} - 3$		ns
5	$t_{d(TXCLK-TXD1)}$	Delay time, TXD1 high after TXCLK low	$t_{w(TXCLK)}$		ns

(1) 10-pF load on pin

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6.10.3.3.1.2 FSITX SPI Signaling Mode Timings

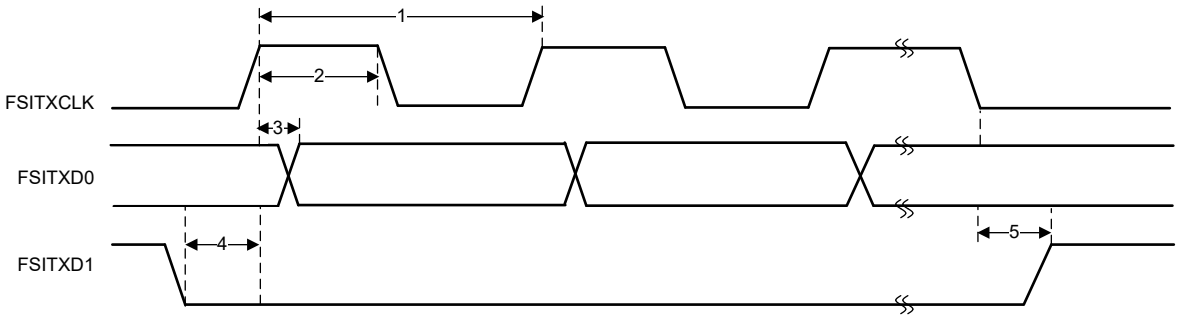


Figure 6-30. FSITX SPI Signaling Mode Timings

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6.10.4 EtherCAT SubordinateDevice Controller (ESC)

Ethernet for Control Automation Technology (EtherCAT®) is an Ethernet-based fieldbus system, invented by Beckhoff Automation and is standardized in IEC 61158. All the SubordinateDevice (or SubDevice) nodes connected to the bus interpret, process, and modify the data addressed to them quickly, without having to buffer the frame inside the node. This real-time behavior, frame processing, and forwarding requirements are implemented by the EtherCAT SubDevice controller (ESC) hardware. EtherCAT does not require software interaction for data transmission inside the SubDevices. EtherCAT only defines the MAC layer while the higher-layer protocols and stack are implemented in software on the microcontrollers connected to the ESC.

The EtherCAT:

- Involves MainDevice (or MDevice) and SubDevices setup where SubDevice nodes are physically connected daisy-chain style but logically operate on a loop
- Specializes in precise, low-jitter synchronization across SubDevice nodes
- Uses IEEE 802.3 Ethernet physical layer and standard Ethernet frames

6.10.4.1 ESC Features

The ESC on this MCU provides the following functionality:

- Up to 2 MII ports to connect to EtherCAT PHYs
- Process data interface through 16-bit asynchronous interface
- 64-bit distributed clocking
  - Sync output signals to synchronize device events and latch input signals supporting time-stamping for events
  - Distributed clock features of SYNC0/1 (o/ps) and LATCH0/1 able to synchronize GPIOs and allow inputs from any GPIOs as well as other muxing options for internal device events
- 8 Field bus Memory Management Units (FMMUs)
  - Support all native types of RD/, WR/, RDWR, and built-in features of bit- and byte-addressing
- 8 Sync Managers
- I2C EEPROM interface
- Up-to 32 general-purpose inputs (GPIs) and 32 general-purpose outputs (GPOs)
- 2 SYNC and 2 LATCH signals connected to GPIO pads
- 16KB RAM with parity

6.10.4.2 ESC Subsystem Integrated Features

In addition to the ESC features, the following are the device-specific features provided by the integration of the ESC and the MCU:

- ESC access allocation to CPU during initialization
- EtherCAT reset request from MDevice can be routed to NMI or general interrupt controller on MCU
- RAM Parity error routed to NMI on MCU
- DMA access to EtherCAT RAM
- Up to 32 GPIs and up to 32 GPOs feature integrated to 16-bit ASYNC PDI interface
- Interface to CLB
- CM-I2C internal loopback feature for EEPROM
- PDI emulation feature
- Distributed clock feature of SYNC0/1 able to synchronize PWMs, generate interrupt/DMA requests, or trigger eCAP capture to allow external component action through GPIO access.
- Distributed clock feature of LATCH0/1 allows inputs from any GPIO or PWM crossbar triggers

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6.10.4.3 EtherCAT IP Block Diagram

Figure 6-31 shows the general functionality of EtherCAT IP.

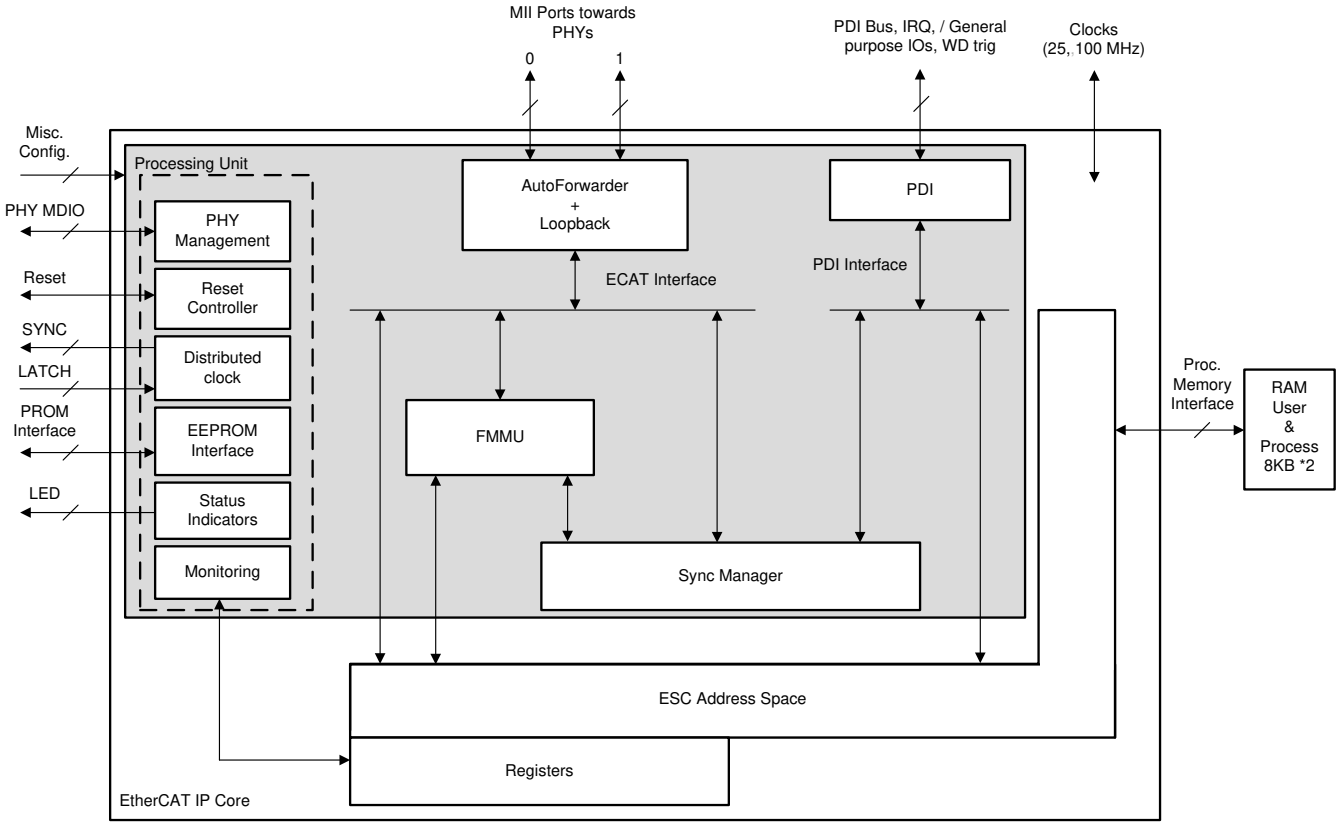


Figure 6-31. EtherCAT IP Block Diagram

6.10.4.4 EtherCAT Electrical Data and Timing

6.10.4.4.1 EtherCAT Timing Requirements

NO.			MIN	NOM	MAX	UNIT
EtherCAT						
	$t_{c(ECATCLK)}$	Cycle time, ECATCLK		10		ns
MII1	$t_{c(TXCLK)}$	Cycle time, ESC_TXy_CLK		40		ns
MII2/MII3	$t_{w(TXCK)}$	Pulse duration, ESC_TXy_CLK high or low	16		24	ns
MII4	$t_{c(RXCK)}$	Cycle time, ESC_RXy_CLK		40		ns
MII5/MII6	$t_{w(RXCK)}$	Pulse duration, ESC_RXy_CLK high or low	16		24	ns
MII8	$t_{su(RXDV-RXCKH)}$	Setup time, receive signals valid before ESC_RXy_CLK high	10			ns
MII9	$t_{h(RXCKH-RXDV)}$	Hold time, receive signals valid after ESC_RXy_CLK high	2			ns
MDIO						
MDIO4	$t_{su(MDV-MCKH)}$	Setup time, ESC_MDIO_DATA valid before ESC_MDIO_CLK high	20			ns
MDIO5	$t_{h(MCKH-MDV)}$	Hold time, ESC_MDIO_DATA valid after ESC_MDIO_CLK high	–1			ns

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6.10.4.4.2 EtherCAT Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
Auto Shift Compensation						
MII7	$t_{d(TXCLK-TXDV)}$	Delay time, ESC_TXy_CLK to ESC_TXy_DATA[3:0] and ESC_TXy_ENA	0 + input_dly + output_dly + TX_SHIFT*$t_{c(CLK_100)}$		10 + input_dly + output_dly + TX_SHIFT*$t_{c(CLK_100)}$	ns
MDIO						
MDIO1	$t_{c(MCK)}$	Cycle time, ESC_MDIO_CLK		400		ns
MDIO2/MDIO3	$t_{w(MCK)}$	Pulse duration, ESC_MDIO_CLK high or low	160		240	ns
MDIO7	$t_{d(MCKH-MDV)}$	Delay time, ESC_MDIO_CLK high to ESC_MDIO_DATA valid			$0.5t_{c(MCK)}$ + 30	ns
	$t_{v(MCKH-MDV)}$	Valid time, ESC_MDIO_DATA valid after ESC_MDIO_CLK high	$0.5t_{c(MCK)}$ – 3.0			ns

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6.10.4.4.3 EtherCAT Timing Diagrams

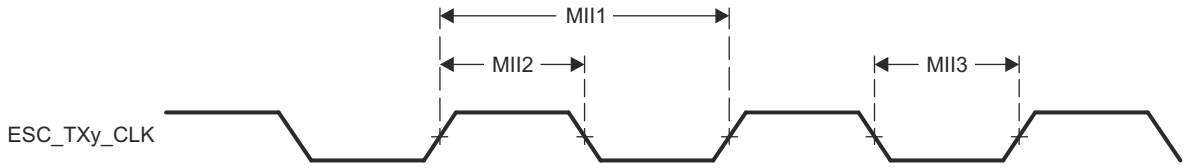


Figure 6-32. EtherCAT Transmit Clock Timing (MII Operation)

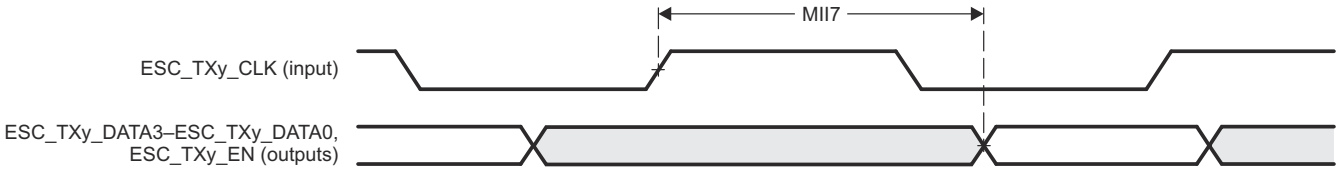


Figure 6-33. EtherCAT Transmit Interface Timing (MII Operation)

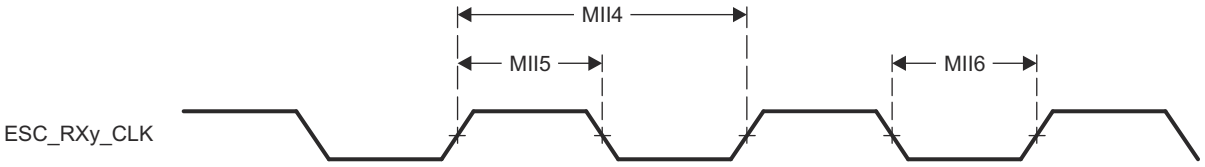


Figure 6-34. EtherCAT Receive Clock Timing (MII Operation)

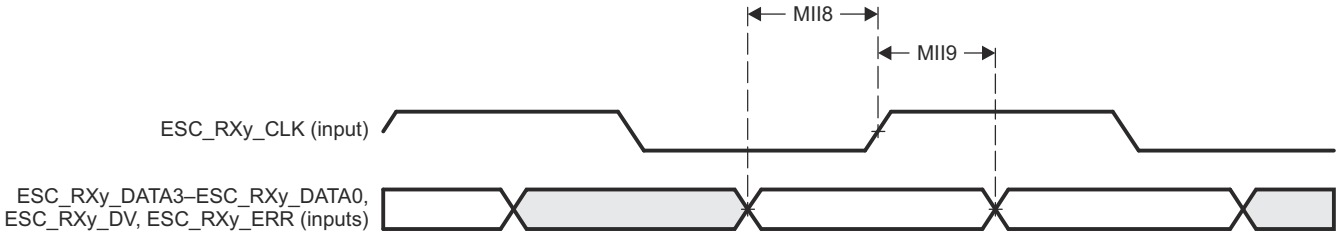


Figure 6-35. EtherCAT Receive Interface Timing (MII Operation)

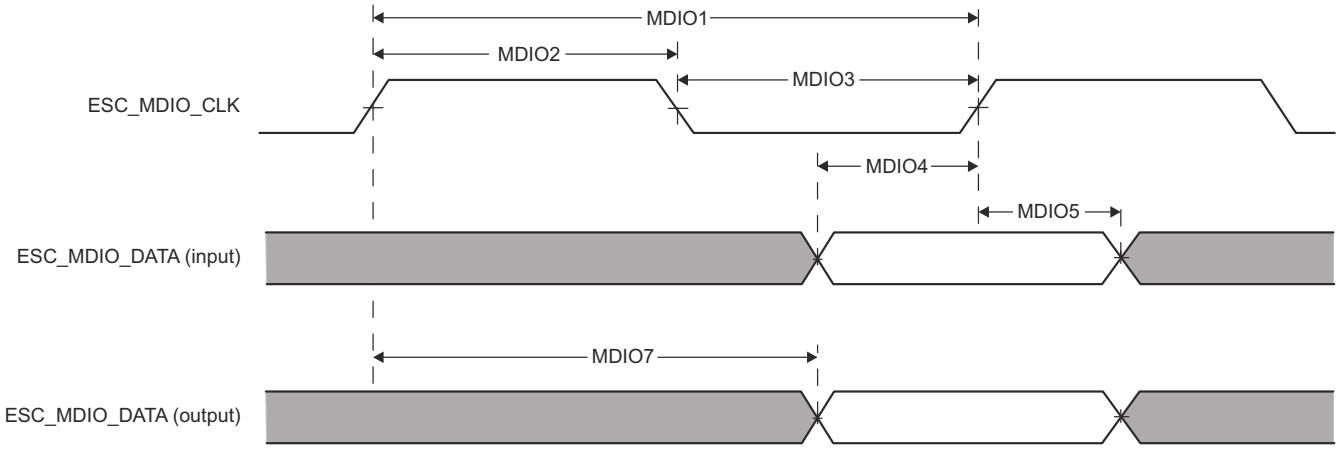


Figure 6-36. EtherCAT MDIO Timing Diagrams

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7 Detailed Description

7.1 Overview

The AM13E232x series of microcontrollers (MCUs) are cost-optimized 32-bit devices built for complex real-time control applications such as motor control. AM13E232x MCUs include a high-performance Arm® Cortex®-M33 core operating at up to 200MHz or 250MHz with a proprietary math accelerator for trigonometric operations (TMU) through a Custom Datapath Extension (CDE) and a TinyEngineTM Neural-network Processing Unit (NPU) Artificial Intelligence (AI) Engine to enable simultaneous motor control and AI model execution. Its rich analog integration offers industry-leading speed, precision, and reduced system cost. The digital peripherals offered on AM13E232x MCUs are specifically designed for motor control applications, and include tailored communications interfaces for appliance and industrial motor drive end equipment.

The AM13E232x series of microcontrollers (MCUs) provides up to 512KB of embedded flash program memory (2 banks of 256KB) with built-in error correction code (ECC) and up to 128KB SRAM (4 banks of 32KB) with hardware parity.

The AM13E232x series of microcontrollers (MCUs) offers a range of options in various memory, peripheral, and package configurations, enabling customers to find the most fitting solution that meets their specific project needs. The AM13E232x MCU platform combines the Arm® Cortex®-M33 platform with a holistic low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

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7.2 Memory

7.2.1 Memory Map

Table 7-1. Memory Map

MEMORY	SIZE	START ADDRESS	END ADDRESS	ECC/ PARITY	ACCESS PROTECTION	SECURITY
Flash Bank 0	256K x 16	0x0000 0000	0x0003 FFFF	ECC	Yes	Yes(2)
Flash Bank 1	256K x 16	0x0004 0000	0x0007 FFFF	ECC	Yes	Yes(2)
ROM(1)	48K x 16	0x0100 0000	0x0100 BFFF	Parity	No	No
SRAM0	32K x 16	0x2000 0000	0x2000 7FFF	Parity	Yes	Yes(2)
SRAM1	32K x 16	0x2000 8000	0x2000 FFFF	Parity	Yes	Yes(2)
SRAM2	32K x 16	0x2001 0000	0x2001 7FFF	Parity	Yes	Yes(2)
SRAM3	32K x 16	0x2001 8000	0x2001 FFFF	Parity	Yes	Yes(2)
SRAM4	32K x 16	0x2002 0000	0x2002 7FFF	Parity	Yes	Yes(2)
SRAM5	32K x 16	0x2002 8000	0x2002 FFFF	Parity	Yes	Yes(2)

(1) ROM is for TI internal use only.
(2) Global Security Controller (GSC) based secure.

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7.2.2 Peripheral Registers Memory Map

Table 7-2. Peripheral Registers Memory Map

Structure	DriverLib Name	Base Address
pd1 by2 clock		
PGA_REGS	PGA0	0x400F_C000
PGA_REGS	PGA1	0x400F_D000
PGA_REGS	PGA2	0x400F_E000
MCAN_REGS	MCAN0	0x4011_0000
MCAN_REGS	MCAN1	0x4011_8000
TIMG4_REGS	TIMG4	0x4018_0000
TIMG12_REGS	TIMG12	0x4018_8000
AES_REGS	AES	0x401B_0000
CRCP_REGS	CRC	0x401B_2000
KEYSTORE_REGS	KEYSTORE	0x401B_6000
UNICOMMUART_REGS	UC0_UART	0x4060_0000
UNICOMMUART_REGS	UC1_UART	0x4060_1000
UNICOMMUART_REGS	UC2_UART	0x4060_2000
UNICOMMI2CC_REGS	UC0_I2CC	0x4060_8000
UNICOMMI2CC_REGS	UC1_I2CC	0x4060_9000
UNICOMMI2CC_REGS	UC2_I2CC	0x4060_A000
UNICOMMI2CT_REGS	UC0_I2CT	0x4061_0000
UNICOMMI2CT_REGS	UC1_I2CT	0x4061_1000
UNICOMMI2CT_REGS	UC2_I2CT	0x4061_2000
UNICOMMSPI_REGS	UC0_SPI	0x4061_8000
UNICOMMSPI_REGS	UC1_SPI	0x4061_9000
UNICOMM_REGS	UNICOMM0	0x4063_0000
UNICOMM_REGS	UNICOMM1	0x4063_2000
UNICOMM_REGS	UNICOMM2	0x4063_4000
SPG_REGS	SPG0	0x4063_F000
UNICOMMUART_REGS	UC3_UART	0x4064_0000
UNICOMMUART_REGS	UC4_UART	0x4064_1000
UNICOMMUART_REGS	UC5_UART	0x4064_2000
UNICOMMI2CC_REGS	UC3_I2CC	0x4064_8000
UNICOMMI2CC_REGS	UC4_I2CC	0x4064_9000
UNICOMMI2CC_REGS	UC5_I2CC	0x4064_A000
UNICOMMI2CT_REGS	UC3_I2CT	0x4065_0000
UNICOMMI2CT_REGS	UC4_I2CT	0x4065_1000

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Table 7-2. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address
UNICOMMI2CT_REGS	UC5_I2CT	0x4065_2000
UNICOMMSPI_REGS	UC3_SPI	0x4065_8000
UNICOMMSPI_REGS	UC4_SPI	0x4065_9000
UNICOMM_REGS	UNICOMM3	0x4067_0000
UNICOMM_REGS	UNICOMM4	0x4067_2000
UNICOMM_REGS	UNICOMM5	0x4067_4000
SPG_REGS	SPG1	0x4067_F000
pd1 by1 clock		
ADC_LITE_REGS	ADC0	0x4000_0000
ADC_LITE_REGS	ADC1	0x4000_2000
ADC_LITE_REGS	ADC2	0x4000_4000
ADC_LITE_RESULT_REGS	ADC0RESULT	0x4000_A000
ADC_LITE_RESULT_REGS	ADC1RESULT	0x4000_B000
ADC_LITE_RESULT_REGS	ADC2RESULT	0x4000_C000
MCPWM_6CH_REGS	MCPWM0	0x4001_0000
MCPWM_6CH_REGS	MCPWM1	0x4001_1000
MCPWM_6CH_REGS	MCPWM2	0x4001_2000
DMA_REGS	DMA0	0x4002_0000
FLASH_CTRL_REGS	FLASH	0x4002_8000
MEM_CFG_REGS	MEMCFG	0x4002_A000
EAM_REGS	EAM	0x4002_C000
EPWM_REGS	EPWM0	0x400B_4000
EPWM_REGS	EPWM1	0x400B_5000
EPWM_REGS	EPWM2	0x400B_6000
EPWM_REGS	EPWM3	0x400B_7000
EPWM_REGS	EPWM4	0x400B_8000
EPWM_REGS	EPWM5	0x400B_9000
ECAP_REGS	ECAP0	0x4044_0000
ECAP_REGS	ECAP1	0x4044_1000
ECAP_REGS	ECAP2	0x4044_2000
HRCAP_REGS	HRCAP2	0x4044_2040
EQEP_REGS	EQEP0	0x4044_8000
EQEP_REGS	EQEP1	0x4044_9000
CMPSS_LITE_REGS	CMPSS0	0x4046_0000
CMPSS_LITE_REGS	CMPSS1	0x4046_1000

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Table 7-2. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address
CMPSS_LITE_REGS	CMPSS2	0x4046_2000
CMPSS_LITE_REGS	CMPSS3	0x4046_3000
INPUT_XBAR_REGS	INPUTXBAR	0x4046_8000
PWM_XBAR_REGS	PWMXBAR	0x4046_9000
OUTPUTXBAR_REGS	OUTPUTXBAR	0x4046_A000
SYNC_SOC_REGS	SYNC	0x4046_B000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR0_FLAGS	0x4047_0000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR1_FLAGS	0x4047_1000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR2_FLAGS	0x4047_2000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR3_FLAGS	0x4047_3000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR4_FLAGS	0x4047_4000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR5_FLAGS	0x4047_5000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR6_FLAGS	0x4047_6000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR7_FLAGS	0x4047_7000
INPUT_FLAG_XBAR_REGS	INPUTXBAR_FLAGS	0x4049_0000
SDFM_REGS	SDFM	0x4049_1000
ESCSS_REGS	ESCSS	0x404A_8000
ESCSS_CONFIG_REGS	ESCSS_CONFIG	0x404A_8200
FSI_TX_REGS	FSI_TX	0x4050_0000
FSI_RX_REGS	FSI_RX	0x4050_1000
pd1 by4 clock		
NVMNW_REGS	NVMNW	0x4004_2000
GSC_REGS	GSC	0x4004_6000
cbpdd0		
SYSCTL_REGS	SYSCTL	0x400A_F000
DEBUGSS_REGS	DEBUGSS	0x400C_7000
IOMUX_REGS	IOMUX	0x400C_C000
WWDT_REGS	WWDT	0x400D_0000
GPIO_REGS	GPIO0	0x400F_0000
GPIO_REGS	GPIO1	0x400F_2000
GPIO_REGS	GPIO2	0x400F_4000
GPIO_REGS	GPIO3	0x400F_6000

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7.2.3 Static RAM

The CPU subsystem has a dedicated static RAM block with hardware parity, with up to 192KB of SRAM.

7.2.4 Flash Memory

On the AM13E232x microcontrollers, two flash banks of up to 256KB each are available. Each Flash bank is made up of 2KB physical sectors. Code to program the flash should be executed out of RAM, there should not be any kind of access to the flash bank when an erase or program operation is in progress.

7.3 Arm® Cortex®-M33 CPU

The Arm® Cortex®-M33 CPU is a 32-bit processor ideal for embedded applications that require efficient security or digital signal control. This CPU core includes features to enable such embedded applications, including memory protection units, a floating point unit, custom datapath instructions, and a micro trace buffer for instruction trace capabilities.

7.3.1 Trigonometric Math Unit (TMU)

The Trigonometric Math Unit (TMU) extends the capabilities of the Arm® Cortex®-M33 CPU by leveraging instructions to speed up common trigonometric and arithmetic operations listed in Table 7-3.

Table 7-3. TMU Supported Instructions

Instructions	Description
SINPUF32	Returns the SINE of input value
COSPUF32	Returns the COSINE of input value
ATANPUF32	Returns the ATAN of input value
DIVF32	Returns DIV value of two input values
QUADF32	Returns the quadrant value and the ratio of X and Y inputs which are provided as per unit values
SQRTF32	Returns the square root of input value
IEXP2F32	Returns inverse exponent of input value
LOG2F32	Returns base-2 logarithm of input value
ISQRTF32	Returns the inverse square root of input value
RSCTFLG	Read/Set/Clear the LUF and LVF flags that are maintained inside the TMU CDE

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7.3.2 Debug Subsystem

The AM13E232x Debug Subsystem integrates the JTAG interface and accesses the Cortex®-M33 CPU debug registers through the Debug Access Port (DAP). The Cortex®-M33 DAP can be configured as a JTAG Debug Port (JTAG-DP), Serial Wire Debug Port (SW-DP), or Serial Wire/JTAG Debug Port (SWJ-DP).

Note

MCLK (CPUCLK) must be at 100MHz to use ETM tracing.

Micro Trace Buffer

The Micro Trace Buffer (MTB) on AM13E232x MCUs provides basic execution trace capability to the CPU core. When enabled, the MTB records changes in program flow, reported by the Cortex®-M33 processor over the execution trace interface. This information is stored as trace packets in the MTB memory. An external debugger can extract the trace information using the DAP. The debugger can then reconstruct the program flow from this information.

7.4 TinyEngine™ Neural-network Processing Unit (NPU)

The TinyEngine™ Neural-network Processing Unit (NPU) supports intelligent inferencing running pre-trained models. Capable of 800-3200MOPS (Mega Operations Per Second), the TinyEngine™ NPU provides up to 10x Neural Network (NN) inferencing cycle improvement compared to a software-only implementation. Load and train models with tools from TI for an advanced set of capabilities.

7.5 DMA

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

- DMA0: 12 independent DMA transfer channels
  - 6 full-feature channel supporting repeated transfer modes
  - 6 basic channels supporting single transfer modes and scatter mode
- Configurable DMA channel priorities
- Byte (8-bit), short word (16-bit), word (32-bit) and long word (64-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- Early interrupt generation for ping-pong buffer architecture
- Cascading channels upon completion of activity on another channel
- Stride mode to support data re-organization, such as 3-phase metering applications

For more details, see the DMA chapter of the *AM13E232x Microcontrollers Technical Reference Manual*.

7.6 Error Aggregator Module (EAM)

The Error Aggregator Module (EAM) aggregates errors that include but are not limited to single error correction (SEC) and double error detection (DED) for the system memory and security errors. EAM latches the error into corresponding register that is forwarded to SYSCTL to generate an NMI or interrupt the CPU based on the priority of the error. The EAM module can be protected by a security firewall based on the GSC setting to allow customer critical code in secure mode of the application to handle the error in a context safe method.

The EAM supports the following features:

- ECC error logging for SEC and DED from flash and SRAM
- Security error logging for non-secure access to a firewall region for memory and peripherals
- Security error logging for hide protected region in the flash

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- First error logged with initiator and type of access error logged

7.7 Power Management and Clock Unit (PMCU)

7.7.1 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the band-gap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brownout reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY operating modes to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted

For more details, see the PMU chapter of the *AM13E232x Microcontrollers Technical Reference Manual*.

7.7.2 Operating Modes

AM13E232x MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code when in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST, SWD/JTAG interface, a logic level match on certain IOs, or an interrupt from the low frequency sub system (LFSS).

To further balance performance and power consumption, AM13E232x devices implement two power domains: PD1, PD0. PD1 contains the CPU, memories, and high performance peripherals. PD1 contains is always powered in RUN and SLEEP modes, but is disabled in all other modes. PD0 contains low speed, low power peripherals which are always powered in RUN, SLEEP, STOP, and STANDBY modes. PD1 and PD0 are both disabled in SHUTDOWN mode.

7.7.2.1 Functionality by Operating Mode

Supported functionality in each operating mode is given in *Supported Functionality by Operating Modes*.

Functional key:

- **EN**: The function is enabled in the specified mode.
- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **RET**: The function's memory and configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode, but its use is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained. When waking up from an OFF state, all module registers must be re-configured to the desired settings by application software.

Table 7-4. Supported Functionality by Operating Modes

OPERATING MODE		RUN	SLEEP	STOP	STANDBY0	STANDBY1	SHUTDOWN
Supply State	VDD	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V
	VDDC	1.35V	1.35V	1.0V	1.0V	1.0V	0V

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Table 7-4. Supported Functionality by Operating Modes (continued)

OPERATING MODE		RUN	SLEEP	STOP	STANDBY0	STANDBY1	SHUTDOWN
PMU	POR monitor	EN					OFF
	BOR monitor	EN					OFF
	Main LDO	EN		OFF			
	STOP LDO	EN					OFF
	VOSC LDO	EN					OFF
Oscillators	SYSOSC	EN, 32MHz		EN, 4MHz	OFF		
	LFOSC	EN					
	XTAL	OPT		DIS			OFF
	HPLL	OPT		DIS			OFF
Clocks	MCLK	200MHz / 250MHz		DIS			OFF
	MCLK/2	100MHz / 125MHz		DIS			OFF
	MCLK/4	50MHz / 62.5MHz		DIS			OFF
	CPUCLK	200MHz / 250MHz	DIS				OFF
	LFCLK	32kHz					OFF
	ULPCLK	50MHz / 62.5MHz		4MHz	32kHz	OFF	OFF
	HFCLK	OPT		DIS			OFF
	CANCLK	OPT		DIS			OFF
	ADCCLK	100MHz / 125MHz		DIS			OFF
	LFCLK Monitor	OPT					OPT
	MCLK Monitor	OPT			DIS		OFF
Core Functions	CPU	EN	DIS				OFF
	Flash	EN		DIS			OFF
	SRAM0	EN		DIS + RET			OFF
	SRAM1/2/3	EN		DIS			OFF
PD1 Peripherals	ADC[0:2]	OPT		DIS + RET			OFF
	PGA[0:2]	OPT		DIS + RET			OFF
	CMPSS[0:3]	OPT		DIS + RET			OFF
	ECAP[0:1]	OPT		DIS + RET			OFF
	EQEP[0:2]	OPT		DIS + RET			OFF
	MCPWM[0:4]	OPT		DIS + RET			OFF
	UC[0:5]	OPT		DIS + RET			OFF
	MCAN0	OPT		DIS			OFF
	NPU	OPT		DIS			OFF
	EPI	OPT		DIS			OFF
	TIMG12_0	OPT		DIS + RET			OFF
	TIMG4_0	OPT		DIS + RET			OFF
	AES	OPT		DIS			OFF
	DMA0	OPT		DIS + RET			OFF
	XBAR	OPT		DIS			OFF
	EAM	OPT		DIS			OFF
	GSC	OPT		DIS + RET			OFF
	KEYSTORE	OPT		DIS + RET			OFF
	CRC	OPT		DIS + RET			OFF
	VREF	EN		EN (Sampled)			OFF

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Table 7-4. Supported Functionality by Operating Modes (continued)

OPERATING MODE		RUN	SLEEP	STOP	STANDBY0	STANDBY1	SHUTDOWN
PD0 Peripherals	GPIO[0:3]	**OPT**					**OFF**
	SYSCTL	**EN**					**OFF**
	WWDT	**OPT**					**OFF**
IOMUX		**EN**		**EN (Sampled)**			**OFF**
IO Wakeup		**EN**		**EN + RET**			**OFF**
Wake Sources		**N/A**	• IRQ • IO • DMA Req • Debug Req • WWDT	• IO • Debug Req • WWD		• IO • Debug Req	• IO (subset)1 • Debug Req

1. Select WAKEUP GPIOs. Refer to the device-specific data sheet.

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7.7.3 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32 kHz)
- **SYSOSC**: Internal high-frequency oscillator (4 MHz or 32 MHz with factory trim, 16 MHz or 24 MHz with user trim)
- **HFXT/HFCKIN**: High-frequency external crystal oscillator or digital clock input (4 to 48 MHz)
- **SYSPLL**: System phase locked loop with 3 outputs (32 to 200 MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals in MCLK domain, derived from SYSOSC, LFCLK, or HSCLK, active in RUN and SLEEP modes
- **MCLK/2**: Main system clock for PD1 peripherals in MCLK/2 domain, derived MCLK and divided by 2
- **MCLK/4**: Main system clock for PD1 peripherals in MCLK/4 domain, derived MCLK and divided by 4
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **LFCLK**: 32-kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **XCLKOUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes
- **HFCLK**: High-frequency clock derived from HFXT or HFCLK_IN, available in RUN and SLEEP mode
- **HSCLK**: High-speed clock derived from HFCLK or the SYSPLL, available in RUN and SLEEP mode
- **CANCLK**: CAN functional clock, derived from HFCLK or SYSPLL

For more details, see the CKM chapter of the *AM13E232x Microcontrollers Technical Reference Manual*.

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7.8 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO Pad configuration registers allow for programmable drive strength, speed, pullup-down, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register
- GPIO pins with Standard-drive with wake functionality can wake-up the device from SHUTDOWN mode

For more details, see the IOMUX chapter of the *AM13E232x Microcontrollers Technical Reference Manual*

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7.8.1 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO. It also provides the controls for the output driver, input path, and the wake-up logic for wakeup from SHUTDOWN mode. For more information, refer to the IOMUX section of the *AM13E232x Microcontrollers Technical Reference Manual*

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in *Superset Input/Output Diagram*. Not all pins will have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available. See the device-specific data sheet for detailed information on what features are supported for a specific pin.

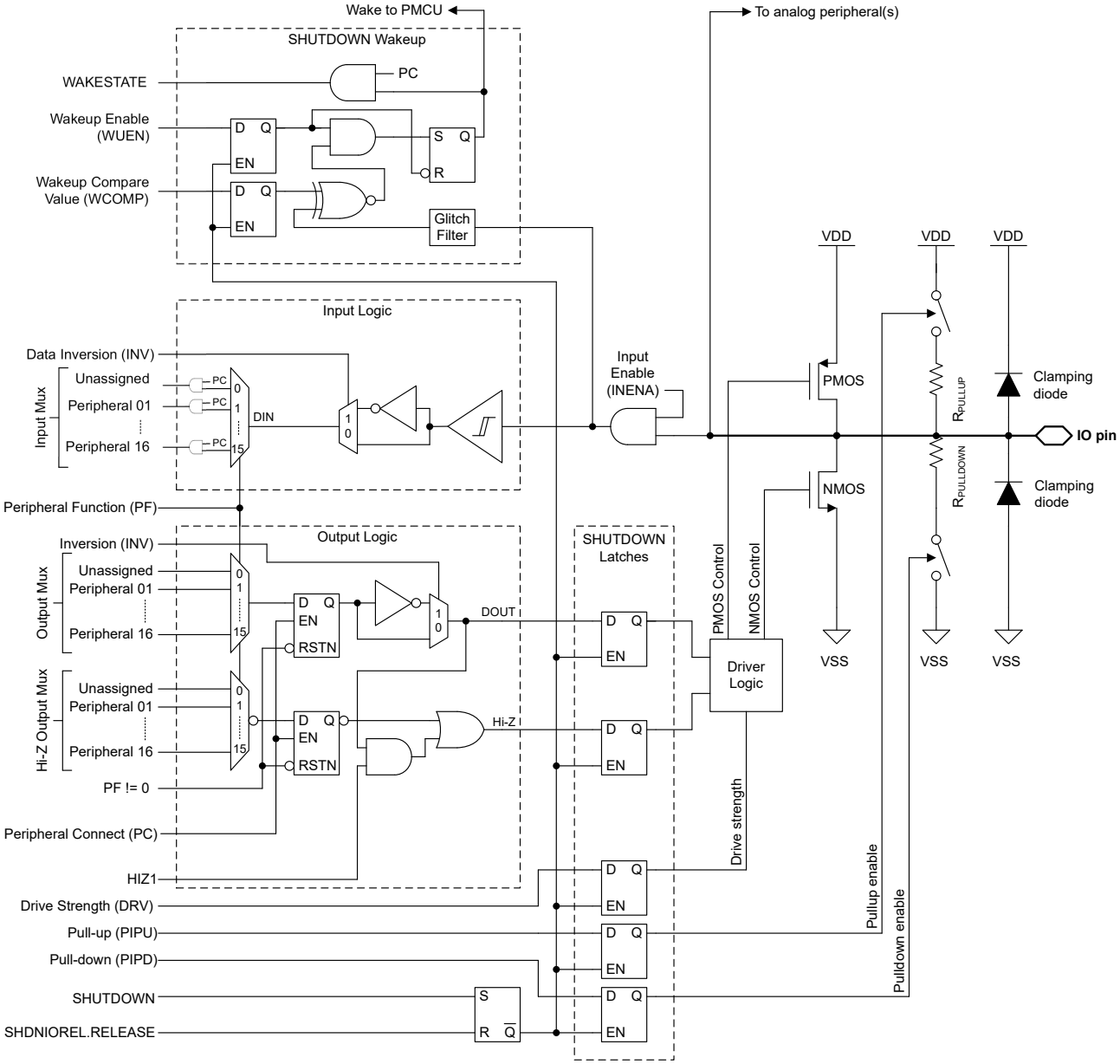


Figure 7-1. Superset Input/Output Diagram

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7.9 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device. For a complete description of the debug functionality, see the debug chapter of the *AM13E232x Microcontrollers Technical Reference Manual*

Table 7-5. Serial Wire Debug Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

7.10 Bootstrap Loader (BSL)

The bootstrap loader (BSL) enables configuration of the device as well as programming of the device memory through a UART, I2C, or MCAN serial interface. Access to the device memory and configuration through the BSL is protected by a 256-bit user-defined HASH password. The BSL can be completely disabled in the device configuration, if desired. The BSL is enabled by default from TI to support use of the BSL for production programming.

A minimum of two pins are required to use the BSL: the BSL_UART_RX and BSL_UART_TX signals (for UART), or the BSL_I^{2}C_SCL and BSL_I^{2}C_SDA signals (for I^{2}C) or the BSL_CAN_RX and BSL_CAN_TX signals (for MCAN). Additionally, one or two additional pins (BSL_INVOKE and NRST) can be used for controlled invocation of the bootloader by an external host.

If enabled, the BSL can be invoked (started) in the following ways:

- The BSL is invoked during the boot process if the BSL_invoke pin state matches the defined BSL_invoke logic level. If the device fast boot mode is enabled, this invocation check is skipped. An external host can force the device into the BSL by asserting the invoke condition and applying a reset pulse to the NRST pin to trigger a BOOTRST, after which the device verifies the invoke condition during the reboot process and start the BSL if the invoke condition matches the expected logic level.
- The BSL is automatically invoked during the boot process if the reset vector and stack pointer are left unprogrammed. As a result, a blank device from TI invokes the BSL during the boot process without any need to provide a hardware invoke condition on the BSL_invoke pin. This enables production programming using just the serial interface signals.
- The BSL can be invoked at runtime from application software by issuing a SYSRST with BSL entry command.

Table 7-6. BSL Pin Requirements and Functions

DEVICE SIGNAL	CONNECTION	BSL FUNCTION
BSL_UART_RX	Required for UART	UART receive signal (RX), an input
BSL_UART_TX	Required for UART	UART transmit signal (TX) an output
BSL_I2C_SCL	Required for I2C	I^{2}C BSL clock signal (SCL)
BSL_I2C_SDA	Required for I2C	I^{2}C BSL data signal (SDA)
BSL_CAN_RX	Required for CAN	MCAN receive signal (RX), an input
BSL_CAN_TX	Required for CAN	MCAN receive signal (TX), an output
BSL_INVOKE	Optional	Active-high digital input used to start the BSL during boot
NRST	Optional	Active-low reset pin used to trigger a reset and subsequent check of the invoke signal (BSL_invoke)

For a complete description of the BSL functionality and command set, see the AM13E232x Bootloader User's Guide.

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7.11 Security

Security features are enforced by the Global Security Controller (GSC). The AM13E232x microcontroller supports the following security features using a combination of hardware blocks, BootROM software, and Customer Secure Code (CSC) programmable into the flash sectors:

- Secure boot
- Secure debug
- Secure firmware update
- Secure key storage
- Secure key management
- Privileged/Non-Privileged partitioning of on chip resources (flash sectors, RAM chunks, peripherals)

In addition to the GSC, AM13E232x has two other security hardware IPs present on the MCU: AESADV and the Keystore Controller.

7.11.1 Global Security Controller (GSC)

The Global Security Controller (GSC) is implemented on the AM13E232x microcontroller to support the following features:

- Provides privileged and non-privileged context information to access on-chip memory and peripherals
- Monitors the bus transactions from multiple initiators to ensure context of access to targets is maintained
- Logs errors for incorrect transactions on the bus
- Performs interrupt or reset generation when context is violated
- Provides mechanism to handle static and dynamic configuration of the security block
- Provides mechanism for managing the life cycle of the device.

The GSC is comprised of the following blocks:

- SRAM Protection Controller (SPC): Controls the context for SRAM
- Flash Protection Controller (FPC): Controls the context for on-chip flash
- Peripheral Protection Controller (PPC): Controls the context for peripherals
- Secure Exception Controller (SEC): Logs and provides action on a security exception

For more details, see the Global Security Controller (GSC) chapter of the *AM13E232x Microcontrollers Technical Reference Manual*

7.11.2 AESADV

The AES advanced (AESADV) accelerator module performs encryption and decryption of 128-bit data blocks with a 128-bit or 256-bit key in hardware according to the advanced encryption standard (AES). AES is a symmetric-key block cipher algorithm specified in FIPS PUB 197.

The AESADV accelerator features include:

- AES operation with 128-bit and 256-bit keys
- Key scheduling in hardware
- Enc/decrypt only modes: CBC, CFB-1, CFB-8, CFB-128, OFB-128, CTR/ICM
- Authentication only modes: CBC-MAC, CMAC
- Support for AES-CCM and AES-GCM modes
- AES-CCM and AES-GCM modes support continuation with hold/resume of payload data
- 32-bit word access to provide key data, input data, and output data
- AESADV ready interrupt
- DMA triggers for input/output data
- Supported in RUN and SLEEP (see the Operating Modes section of the *AM13E232x Microcontrollers Technical Reference Manual*)

For more details, see the AESADV chapter of the *AM13E232x Microcontrollers Technical Reference Manual*

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7.11.3 Keystore Controller

The Keystore Controller on the AM13E232x MCU provides secure management of the Advanced Encryption Engine (AES) keys. During the execution of secure customer code, keys are securerly desposited into the Keystore Controller. The AES engine can then access keys in a secure manner without leaking any key data to observers.

Both 128- and 256-bit keys can be stored in the Keystore key slots.

For more details, see the KEYSTORE chapter of the *AM13E232x Microcontrollers Technical Reference Manual*

7.11.4 CRC Accelerator

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for 32-bit CRC based on CRC32-ISO3309
- Support for bit reversal
- Support for custom polynomials

For more details, see the CRC chapter of the *AM13E232x Microcontrollers Technical Reference Manual*

7.12 Timers (TIMx)

The timer peripherals in these devices support the following key features, for specific configuration see Table 7-7:

Specific features for the general-purpose timer (TIMGx) include:

- 16-bit and 32-bit timers with up, down or up-down counting modes, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Two independent CC channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Shadow CC/load register available
- Support interrupt/DMA trigger generation and cross peripherals (such as ADC) trigger capability

Table 7-7. TIMx Configurations

TIMER NAME	POWER DOMAIN	RESOLUTION	PRESCALER	REPEAT COUNTER	CAPTURE / COMPARE CHANNELS	PHASE LOAD	SHADOW LOAD	SHADOW CC	DEADBAND	FAULT	QEI
TIMG4_0	PD1	16-bit	8-bit	–	2	–	Yes	Yes	–	–	–
TIMG12_0	PD1	32-bit	–	–	2	–	–	Yes	–	–	–

7.13 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

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8 Applications, Implementation, and Layout

8.1 JTAG and TRACE

Texas Instruments supports a variety of eXtended Development System (XDS™) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the XDS Target Connection Guide.

For recommendations on JTAG, and TRACE routing, see the Emulation and Trace Headers Technical Reference Manual

8.2 Schematic

TI recommends connecting a combination of a bulk decoupling capacitor (C_{VDD}) and a small-value low-ESR ceramic decoupling capacitor (C_{DEC}) across the VDD and VSS pins, the VDDA and VSSA pins, as well as placing these capacitors as close as possible to the supply pins that they decouple (within a few millimeters) to achieve a minimal loop area. The C_{VDD} bulk decoupling capacitor has a standard value referenced in the specifications section of the datasheet, but may be adjusted if needed based upon the PCB design and application requirements. For example, larger bulk capacitors can be used, but this can affect the supply rail ramp-up time.

The $\overline{\text{NRST}}$ reset pin must be pulled up to VDD (supply level) for the device to release from RESET state and start the boot process. TI recommends connecting an external pullup resistor (Rpu_{NRST}) with a pulldown capacitor (C_{NRST}) for most applications to ensure that the default $\overline{\text{NRST}}$ state is logic-high (not triggering MCU reset), while also enabling the $\overline{\text{NRST}}$ pin to be controlled by another device or a debug probe.

Note

Refer to the *AM13E232x Hardware Design Guidelines* for detailed application design guidance, such as recommended hardware connections and selection of external passive components.

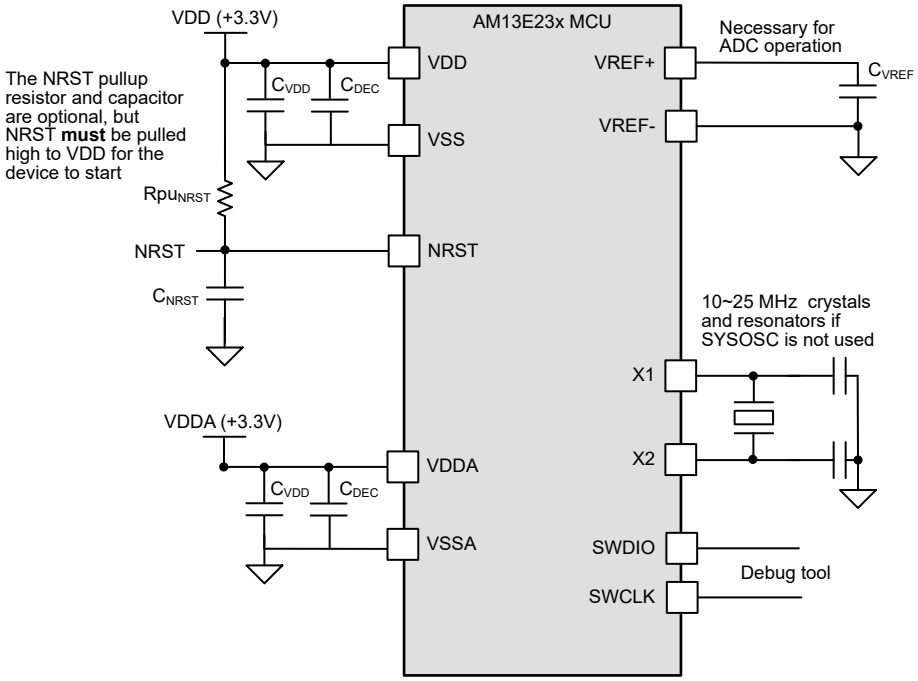


Figure 8-1. Basic Application Schematic

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8.3 Typical Applications

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

The Typical Applications section details some applications of this device. For a more extensive list of applications, see the Section 2 of this data sheet.

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Third-Party Products Disclaimer

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9.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all ASM MCU devices and support tools. . Each ASM MCU commercial family member has one of two prefixes: ASM or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (ASM).

X – Experimental device that is not necessarily representative of the final device's electrical specifications

ASM – Fully qualified production device

X devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." ASM devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Device Nomenclature provides a legend for reading the complete device name.

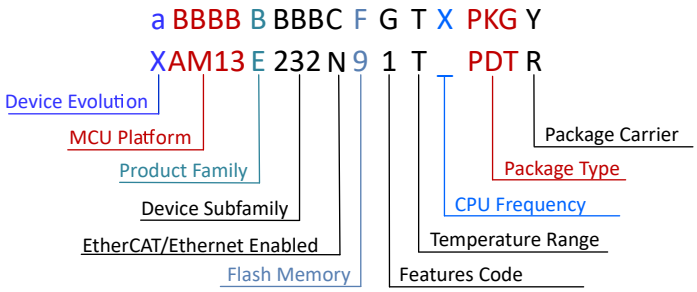


Figure 9-1. Device Nomenclature

Nomenclature Section	Device/Platform Subfamily	Descriptor	Device Options
Device Evolution		a	X = Prototype P = Preproduction (no reliability data) BLANK = Production
MCU Platform	Platform	B	AM1 = AM1x Family of MCU's
	CPU Type		3 = Cortex M33 CPU
Product/Family/Type		B	E = Entry Level Motor Control Device
Device Subfamily	Frequency Class	B	2 = 200/250 MHz Class Device
	Voltage	B	3 = 3.3V Design
	Variant	B	2 = Variant 2 in this family series

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Nomenclature Section	Device/Platform Subfamily	Descriptor	Device Options
EtherCAT/Ethernet Enabled		C	1 = Single CPU, No EtherCAT or Ethernet N = EtherCAT or Ethernet enabled
Flash Memory		F	8 = 256KB Flash 9 = 512KB Flash
Features Code		G	1 = With TINIE + Advanced Control 2 = Without TINIE + Advanced Control
Temperature Range		T	T = -40°C to 125°C (Ambient)
CPU Frequency		X	BLANK = 250MHz
Package Type		PKG	ZGA = BGA144PDT = LQFP128 PZ = LQFP100_G ZBP = BGA99 PM = LQFP64_G YAF = WCSP48
Package Carrier		Y	R = Tape & Reel Carrier

For orderable part numbers of ASM devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

9.3 Tools and Software

Design Kits and Evaluation Modules

AM13E232LaunchPad (LP) Boards: LP-AM13E232 ***Update link***	Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose ASM MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming/debugging. The LP ecosystem includes dozens of BoosterPack stackable plug-in modules to extend functionality.

Embedded Software

AM13 Software Development Kit (SDK)	Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all AM13 devices.

Software Development Tools

TI Developer Zone	Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.
TI Resource Explorer	Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.
SysConfig	Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE ,in TI Cloud Tools or a standalone version. (offline version)
ASM Academy ***Update link***	Great starting point for all developers to learn about the ASM MCU Platform with training modules that span a wide range of topics. Part of TIRex.
GUI Composer	GUIs that simplify evaluation of certain ASM MCU features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.

IDE & compiler toolchains

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Code Composer Studio™ (CCS)	Code Composer Studio is an integrated development environment (IDE) for TI's microcontrollers and processors. It comprises a suite of tools used to develop and debug embedded applications. CCS is completely free to use and is available on Eclipse and Theia frameworks.
IAR Embedded Workbench® IDE	IAR Embedded Workbench for Arm delivers a complete development toolchain for building and debugging embedded applications for ASM AM13.The included IAR C/C++ Compiler generates highly optimized code for your application, and the C-SPY Debugger is a fully integrated debugger for source and disassembly level debugging with support for complex code and data breakpoint.
Keil® MDK IDE	Arm Keil MDK is a complete debugger and C/C++ compiler toolchain for building and debugging embedded applications for ASM AM13.Keil MDK includes a fully integrated debugger for source and disassembly level debugging. MDK provides full CMSIS compliance.
TI Arm-Clang	TI Arm Clang is included in the Code Composer Studio IDE.
GNU Arm Embedded Toolchain	The ASM AM13 SDK supports development using the open-source Arm GNU Toolchain. Arm GCC is supported by Code Composer Studio IDE (CCS).

9.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the AM13E232x MCUs. Copies of these documents are available on the Internet at www.ti.com.

Technical Reference Manual

AM13E232x Microcontrollers Technical Reference Manual	This manual describes the modules and peripherals of the AM13E232x family of devices. Each description presents the module or peripheral in a general sense. Not all features and functions of all modules or peripherals are present on all devices. In addition, modules or peripherals can differ in the exact implementation on different devices. Pin functions, internal signal connections, and operational parameters differ from device to device.

9.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2026	*	Initial Release

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XAM13E232N91TPDT	Active	Preproduction	TQFP (PDT) | 128	90 | JEDEC TRAY (10+1)	-	Call TI	Call TI	-40 to 125	

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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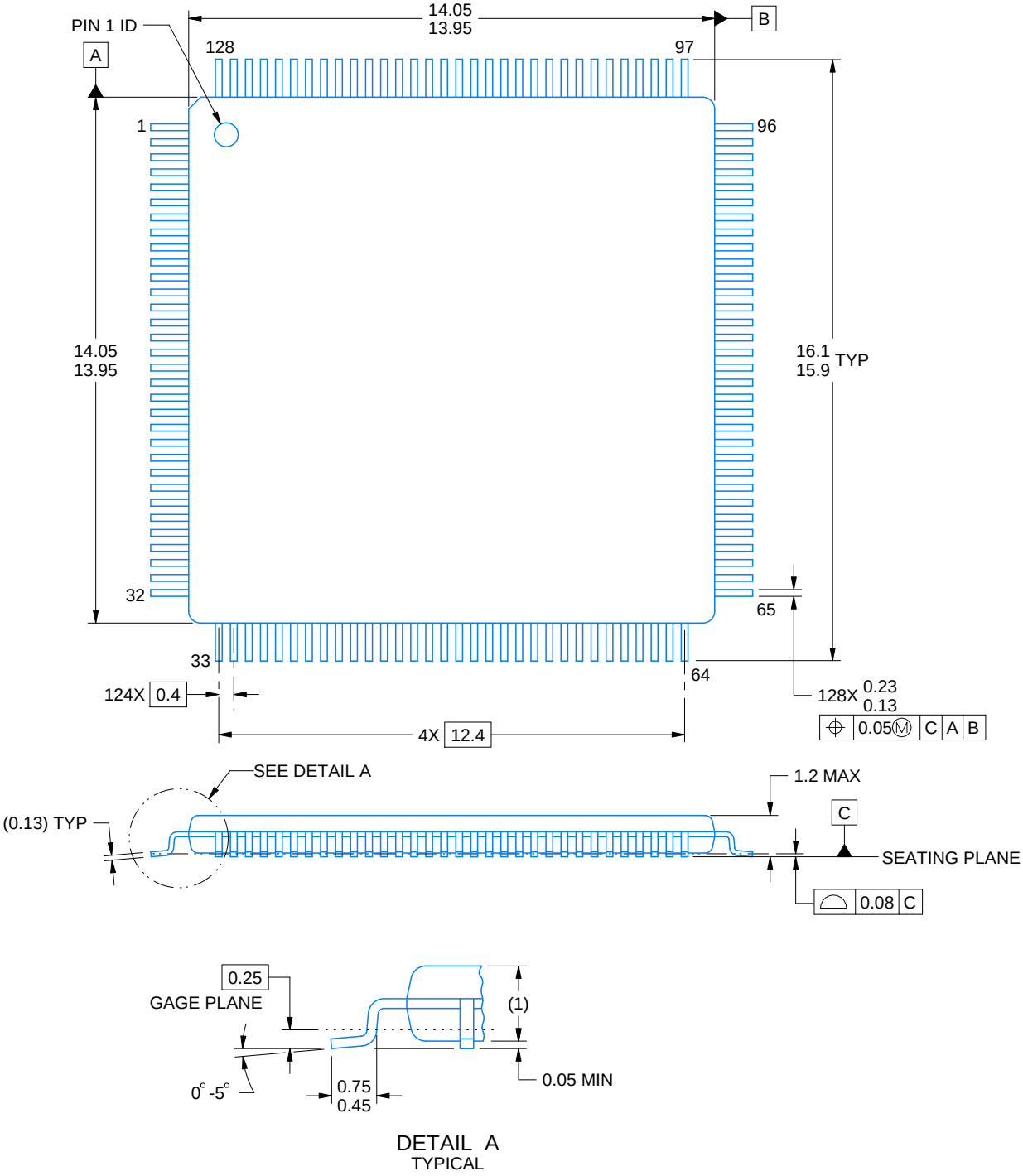
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

PDT0128A

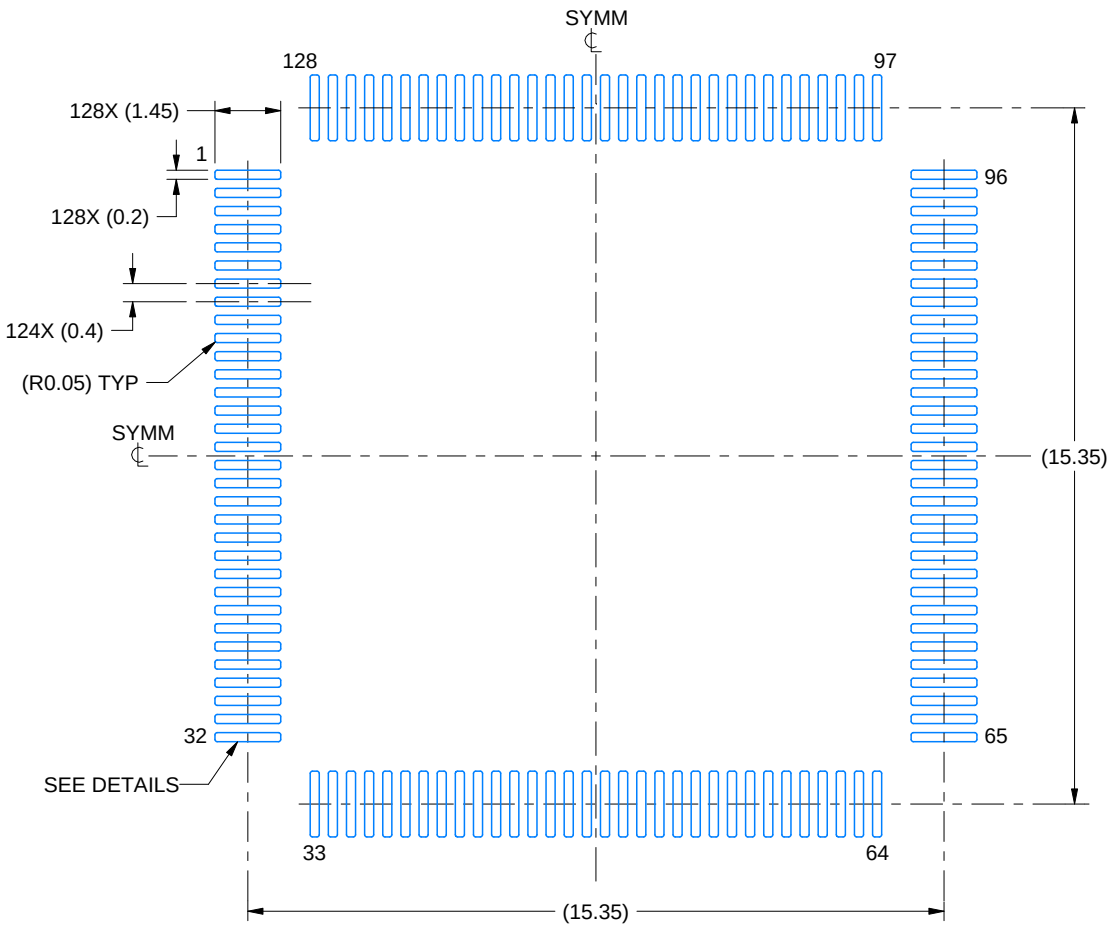
TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK

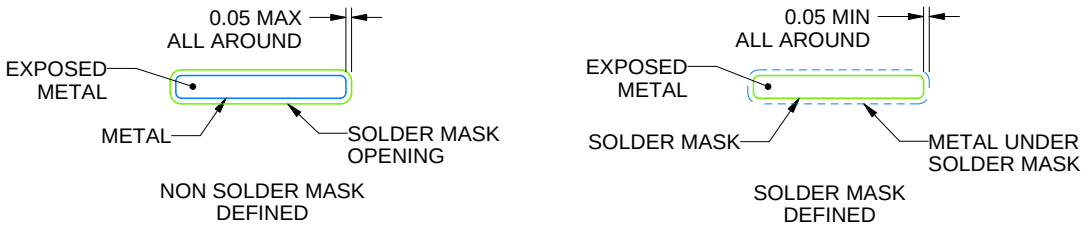


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

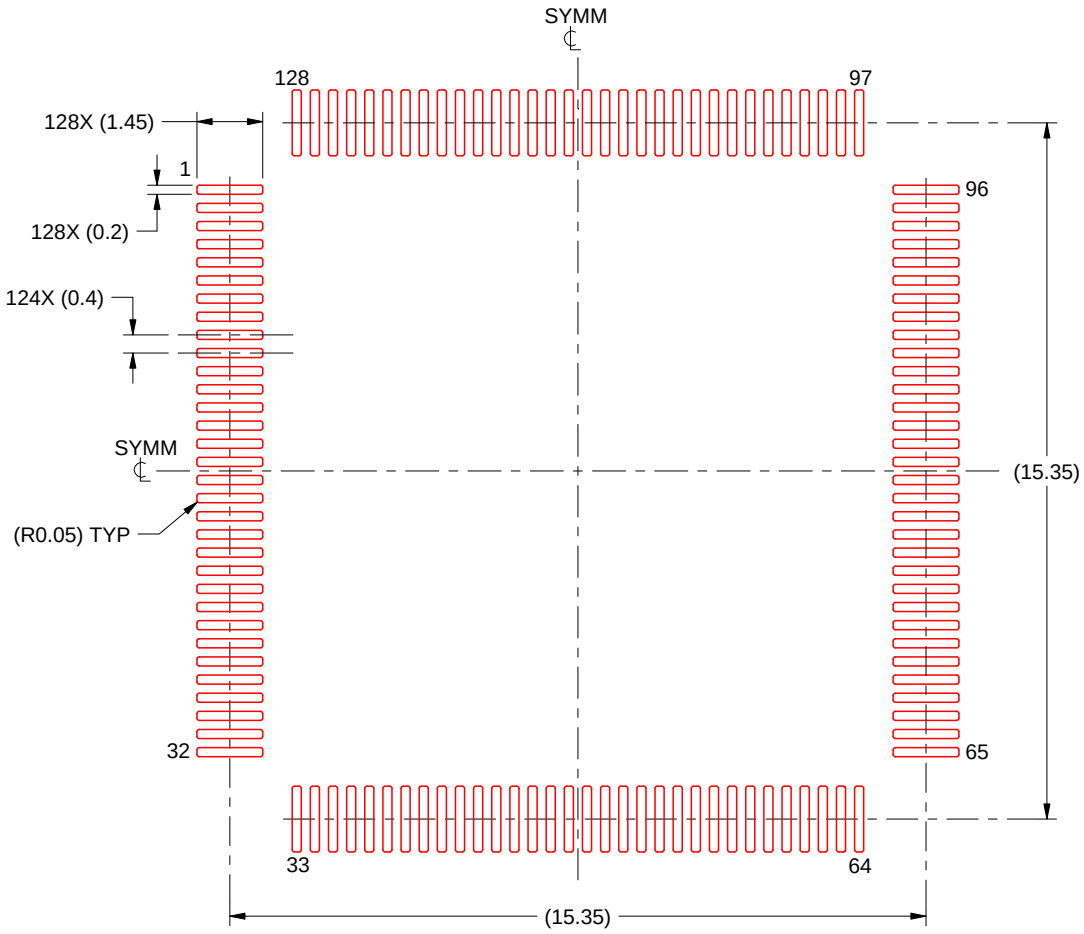


SOLDER MASK DETAILS

4215171/A 10/2023

NOTES: (continued)

3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
5. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215171/A 10/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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