

AFE7700 Quad-Channel General Purpose RF Transceiver

1 Features

- Quad transmitters based on direct up-conversion architecture:
 - Up to 600 MHz of RF transmitted bandwidth per chain
- Quad receivers based on 0-IF down-conversion architecture:
 - Up to 200 MHz of RF received bandwidth per chain
- Feedback chain based on RF sampling ADC:
 - Up to 600 MHz of RF received bandwidth
- RF frequency range: 600 MHz to 6 GHz
- Four wideband fractional-N PLL, VCO for TX and RX LO
- Dedicated integer-N PLL, VCO for data converters clock generation
- JESD204B and JESD204C SerDes interface support:
 - 8 SerDes transceivers up to 29.5 Gbps
 - 8b/10b and 64b/66b encoding
 - 16-bit, 12-bit, 24-bit and 32-bit formatting
 - Subclass 1 multi-device synchronization
- Package: 17-mm × 17-mm FCBGA, 0.8-mm pitch

2 Applications

- Phased Array Radar
- Defense Radio
- Wireless Communications Test
- Vector Signal Transceiver (VST)
- Electronic Warfare

3 Description

The AFE7700 device is a high-performance, multichannel transceiver, integrating four direct up-conversion transmitter chains, four direct down-conversion receiver chains, and two wideband RF sampling digitizing auxiliary chains (feedback paths). The high dynamic range of the transmitter and receiver chains enables high performance wireless transceiver systems.

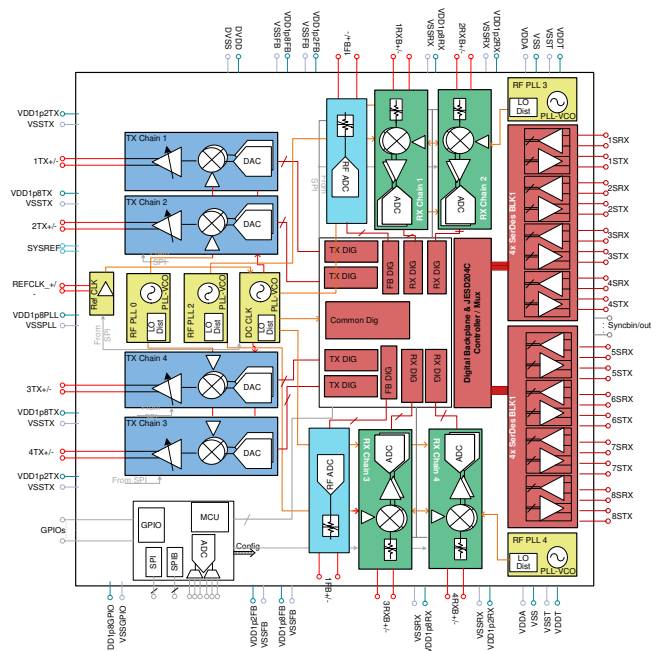
The low power dissipation and large channel integration of the AFE7700 allows the device to address the power and size constraints of multi-antenna and phased array systems. The wideband and high dynamic range feedback path can assist the Digital Pre-Distortion (DPD) of power amplifiers and IQ correction in the transmitter chain. The fast SerDes speed can reduce the number of lanes required to transfer the data in and out.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AFE7700	FCBGA (400)	17.00 mm × 17.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

AFE7700 Block Diagram



4 Description (continued)

Each receiver chain of the AFE7700 includes a 28-dB range digital step attenuator (DSA), followed by a wideband passive IQ demodulator, and a baseband amplifier with integrated programmable antialiasing low pass filters, driving a continuous-time sigma-delta ADC. The RX chain can receive an instantaneous bandwidth (IBW) up to 200 MHz. Each receiver channel has two analog peak power detectors and various digital power detectors to assist an external or internal autonomous AGC control for receiver channels, and a RF overload detector for device reliability protection. The integrated QMC (quadrature mismatch compensation) algorithm is capable to continuously monitor and correct for the RX chain I and Q imbalance mismatch without the need to inject any specific signals or perform offline calibration.

Each transmitter chain includes two 14-bit, 3-Gsps IQ DACs, followed by a programmable reconstruction and DAC image rejection filter, an IQ modulator driving a wideband RF amplifier with 39-dB range gain control. The TX chain integrated QMC and LO leakage cancellation algorithms, leveraging the FB path can constantly track and correct for the TX chain IQ mismatch and LO leakage.

Each FB path is based on RF sampling architecture, and includes an input RF DSA driving a 14-bit, 3-Gsps RF ADC. The direct sampling architecture provides an inherently wideband receiver chain and simplifies the calibration of the TX chains impairments. The FB path integrates two independent NCO that allows a fast switching between two observed RF input bands.

The synthesizer section integrates four fractional-N RF PLL that can generate four different RF LO, allowing the device to support up to two different bands, each one configured as two transmitters, two receivers and one feedback paths.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2019) to Revision A	Page
• Changed the device status From: <i>Advanced Information</i> To: <i>Production Data</i>	1

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.3 Trademarks

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6.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE7700IABJ	Active	Production	FCBGA (ABJ) 400	90 JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7700
AFE7700IABJ.B	Active	Production	FCBGA (ABJ) 400	90 JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7700
AFE7700IALK	Active	Production	FCBGA (ALK) 400	90 JEDEC TRAY (10+1)	No	SNPB	Level-3-220C-168 HR	-40 to 85	AFE7700 SNPB
AFE7700IALK.B	Active	Production	FCBGA (ALK) 400	90 JEDEC TRAY (10+1)	No	SNPB	Level-3-220C-168 HR	-40 to 85	AFE7700 SNPB

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

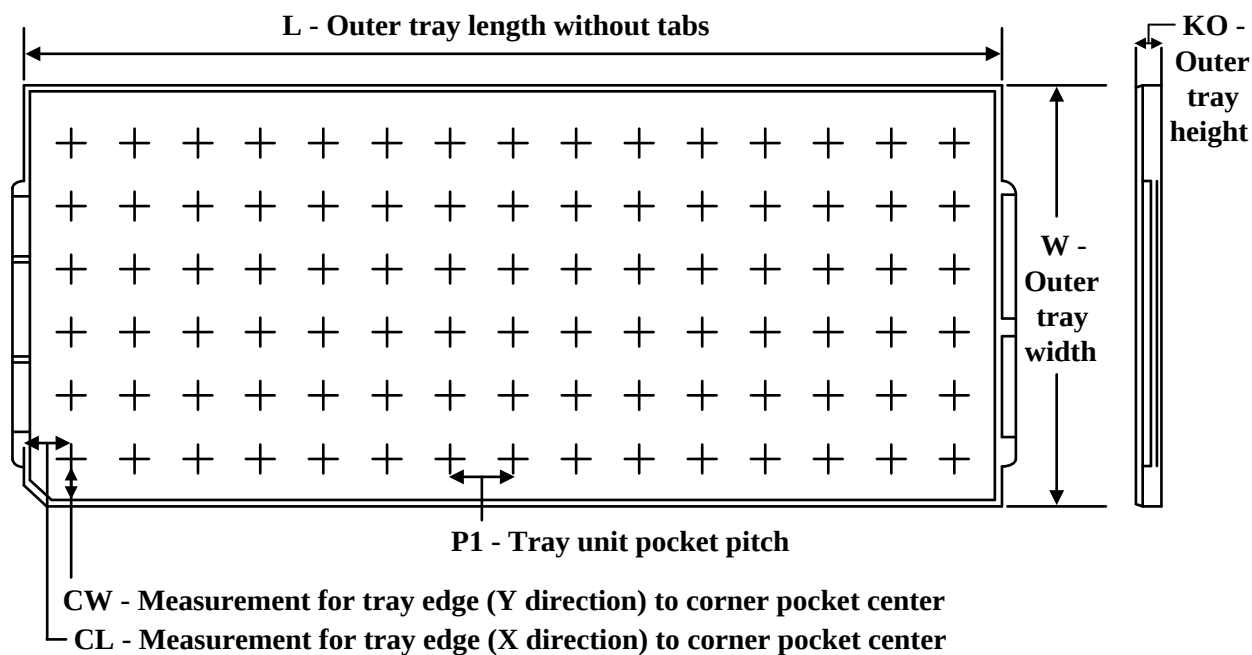
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
AFE7700IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7700IABJ.B	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7700IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7700IALK.B	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2

FCBGA - 2.65 mm max height

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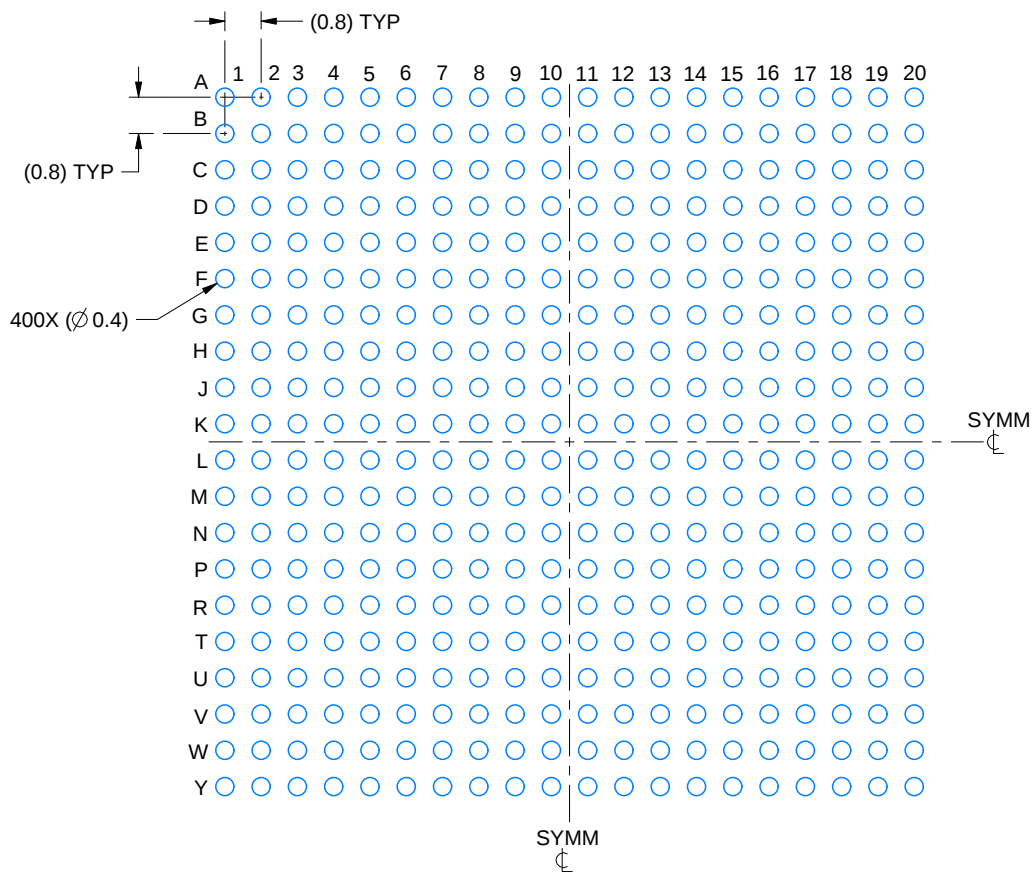
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).

EXAMPLE BOARD LAYOUT

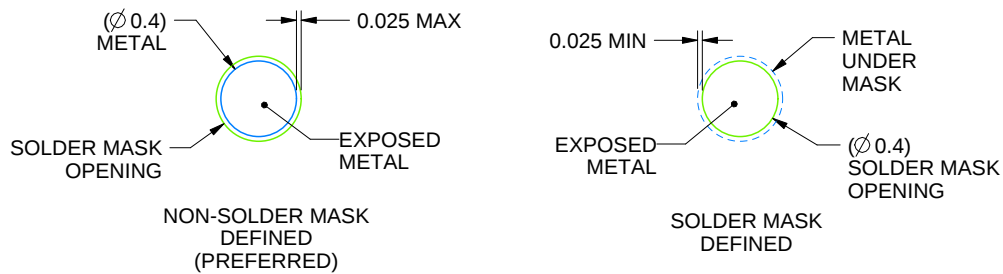
ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

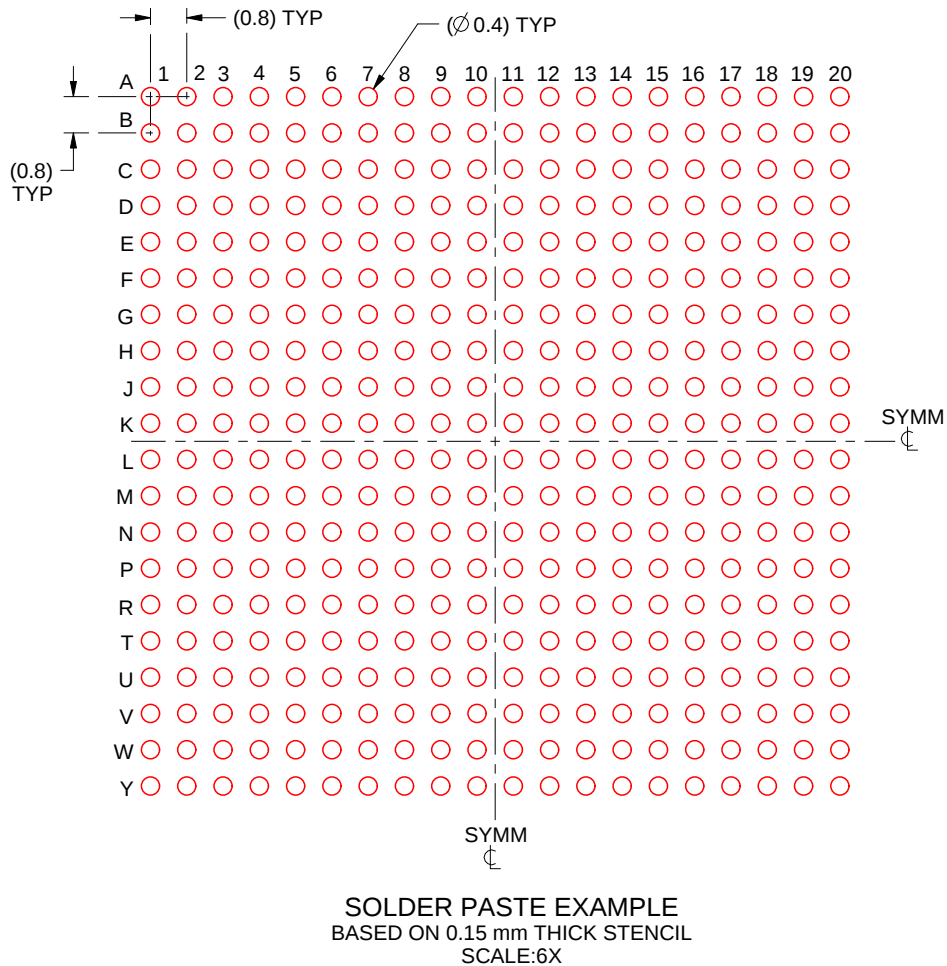
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).

EXAMPLE STENCIL DESIGN

ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

FCBGA - 2.65 mm max height

[illegible]

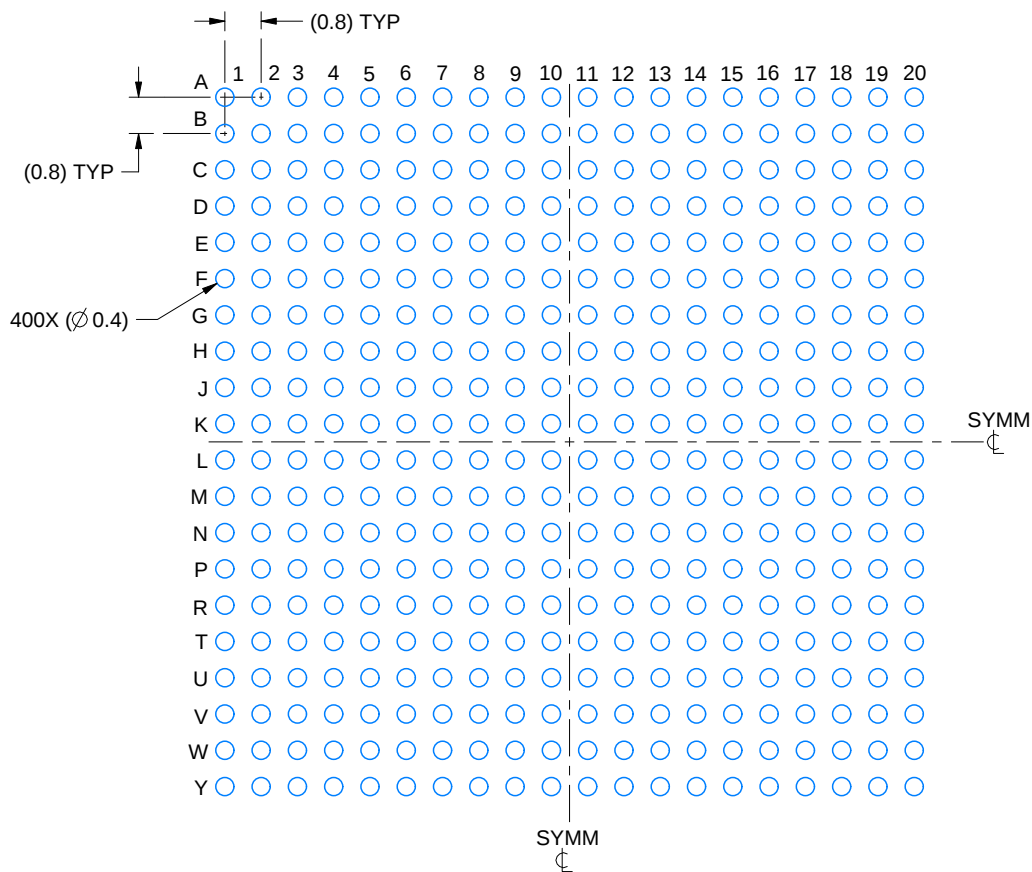
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).

EXAMPLE BOARD LAYOUT

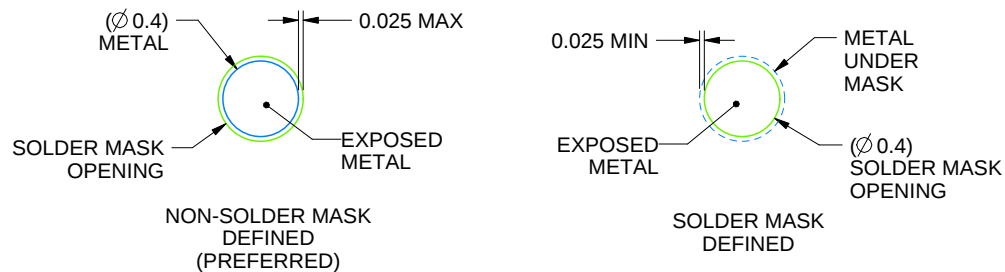
ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

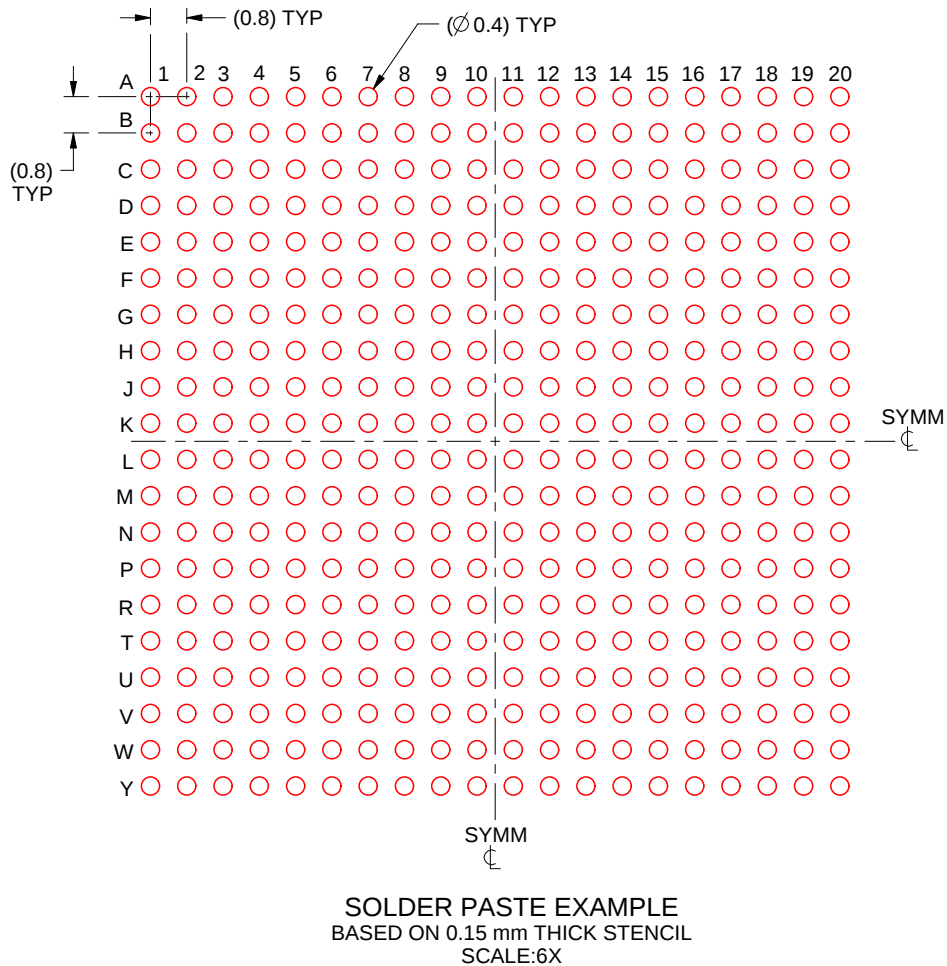
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).

EXAMPLE STENCIL DESIGN

ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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