16-Bit, 1.25MSPS Analog-to-Digital Converter

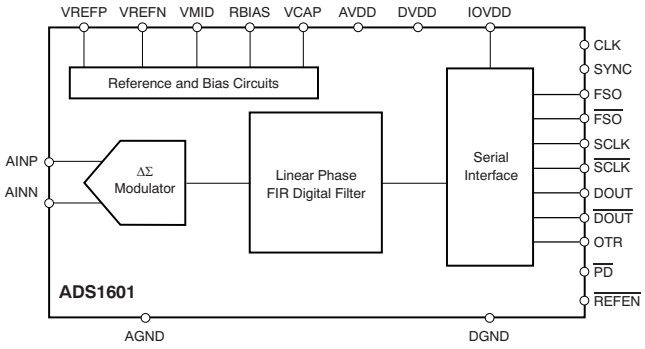
Check for Samples: ADS1601

FEATURES

- **High Speed:**
  - **Data Rate: 1.25MSPS**
  - **Bandwidth: 615kHz**
- **Outstanding Performance:**
  - **SNR: 92dB at f_{IN} = 100kHz, –1dBFS**
  - **THD: –103dB at f_{IN} = 100kHz, –6dBFS**
  - **SFDR: 105dB at f_{IN} = 100kHz, –6dBFS**
- **Ease-of-Use:**
  - **High-Speed 3-Wire Serial Interface**
  - **Directly Connects to TMS320 DSPs**
  - **On-Chip Digital Filter Simplifies Anti-Alias Requirements**
  - **Simple Pin-Driven Control—No On-Chip Registers to Program**
  - **Selectable On-Chip Voltage Reference**
  - **Simultaneous Sampling with Multiple ADS1601s**
- **Low Power:**
  - **330mW at 1.25MSPS**
  - **145mW at 625kSPS**
  - **Power-Down Mode**

APPLICATIONS

- **Sonar**
- **Vibration Analysis**
- **Data Acquisition**



DESCRIPTION

The ADS1601 is a high-speed, high-precision, delta-sigma analog-to-digital converter (ADC) manufactured on an advanced CMOS process. The ADS1601 oversampling topology reduces clock jitter sensitivity during the sampling of high-frequency, large amplitude signals by a factor of four over that achieved by Nyquist-rate ADCs. Consequently, signal-to-noise ratio (SNR) is particularly improved. Total harmonic distortion (THD) is –103dB, and the spurious-free dynamic range (SFDR) is 105dB

Optimized for power and performance, the ADS1601 dissipates only 330mW while providing a full-scale differential input range of ±0.94V_{REF}. Having such a wide input range makes out-of-range signals uncommon. The OTR pin indicates if an analog input out-of-range condition does occur. The differential input signal is measured against the differential reference, which can be generated internally on the ADS1601 or supplied externally.

The ADS1601 uses an inherently stable advanced modulator with an on-chip decimation filter. The filter stop band extends to 19.3MHz, which greatly simplifies the anti-aliasing circuitry. The modulator samples the input signal up to 20MSPS, depending on f_{CLK}, while the 16x decimation filter uses a series of four half-band FIR filter stages to provide 75dB of stop band attenuation and 0.001dB of passband ripple.

Output data is provided over a simple 3-wire serial interface at rates up to 1.25MSPS, with a –3dB bandwidth of 615kHz. The output data or its complementary format directly connects to DSPs such as TI's TMS320 family, FPGAs, or ASICs. A dedicated synchronization pin enables simultaneous sampling with multiple ADS1601s in multi-channel systems. Power dissipation is set by an external resistor that allows a reduction in dissipation when operating at slower speeds. All of the ADS1601 features are controlled by dedicated I/O pins, which simplify operation by eliminating the need for on-chip registers.

The high performing, easy-to-use ADS1601 is especially suitable for demanding measurement applications in sonar, vibration analysis, and data acquisition. The ADS1601 is offered in a small, 7mm × 7mm TQFP-48 package and is specified from –40°C to +85°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	ADS1601	UNIT
AVDD to AGND	–0.3 to +6	V
DVDD to DGND	–0.3 to +3.6	V
IOVDD to DGND	–0.3 to +6	V
AGND to DGND	–0.3 to +0.3	V
Input current	100, momentary	mA
Input current	10, continuous	mA
Analog I/O to AGND	–0.3 to AVDD + 0.3	V
Digital I/O to DGND	–0.3 to IOVDD + 0.3	V
Maximum junction temperature	+150	°C
Operating temperature range	–40 to +105	°C
Storage temperature range	–60 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = –40°C to +85°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, V_{CM} = +2.7V, and R_{BIAS} = 60kΩ, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1601 MIN	ADS1601 TYP	ADS1601 MAX	UNIT
Analog Input					
Differential input voltage (V_{IN}) (AINP – AINN)	0dBFS		±0.94V_{REF}		V
Common-mode input voltage (V_{CM}) (AINP + AINN) / 2			2.7		V
Differential input voltage (V_{IN}) (AINP or AINN with respect to AGND)	0dBFS	–0.1		4.6	V
Dynamic Specifications					
Data rate			$1.25\left(\frac{f_{CLK}}{20MHZ}\right)$		MSPS
Signal-to-noise ratio (SNR)	f_{IN} = 10kHz, –1dBFS		92		dB
	f_{IN} = 10kHz, –3dBFS	87	90		dB
	f_{IN} = 10kHz, –6dBFS	84	87		dB
	f_{IN} = 100kHz, –1dBFS		92		dB
	f_{IN} = 100kHz, –3dBFS	87	90		dB
	f_{IN} = 100kHz, –6dBFS	84	87		dB
	f_{IN} = 500kHz, –1dBFS		91		dB
	f_{IN} = 500kHz, –3dBFS		89		dB
	f_{IN} = 500kHz, –6dBFS		87		dB
Total harmonic distortion (THD)	f_{IN} = 10kHz, –1dBFS		–91		dB
	f_{IN} = 10kHz, –3dBFS		–100	–90	dB
	f_{IN} = 10kHz, –6dBFS		–104	–97	dB
	f_{IN} = 100kHz, –1dBFS		–88		dB
	f_{IN} = 100kHz, –3dBFS		–96	–90	dB
	f_{IN} = 100kHz, –6dBFS		–103	–96	dB
	f_{IN} = 500kHz, –1dBFS		–115		dB
	f_{IN} = 500kHz, –3dBFS		–112		dB
	f_{IN} = 500kHz, –6dBFS		–110		dB
Signal-to-noise + distortion (SINAD)	f_{IN} = 10kHz, –1dBFS		88		dB
	f_{IN} = 10kHz, –3dBFS	85	89		dB
	f_{IN} = 10kHz, –6dBFS	84	87		dB
	f_{IN} = 100kHz, –1dBFS		87		dB
	f_{IN} = 100kHz, –3dBFS	85	88		dB
	f_{IN} = 100kHz, –6dBFS	84	86		dB
	f_{IN} = 500kHz, –1dBFS		91		dB
	f_{IN} = 500kHz, –3dBFS		89		dB
	f_{IN} = 500kHz, –6dBFS		87		dB
Spurious-free dynamic range (SFDR)	f_{IN} = 10kHz, –1dBFS		92		dB
	f_{IN} = 10kHz, –3dBFS	91	100		dB
	f_{IN} = 10kHz, –6dBFS	98	109		dB
	f_{IN} = 100kHz, –1dBFS		88		dB
	f_{IN} = 100kHz, –3dBFS	90	97		dB
	f_{IN} = 100kHz, –6dBFS	97	105		dB
	f_{IN} = 500kHz, –1dBFS		120		dB
	f_{IN} = 500kHz, –3dBFS		118		dB
	f_{IN} = 500kHz, –6dBFS		115		dB
Intermodulation distortion (IMD)	f_1 = 499kHz, –6dBFS f_2 = 501kHz, –6dBFS		94		dB
Aperture delay			4		ns

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = –40°C to +85°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, V_{CM} = +2.7V, and R_{BIAS} = 60kΩ, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1601 MIN	ADS1601 TYP	ADS1601 MAX	UNIT
Digital Filter Characteristics					
Passband		0	$550\left(\frac{f_{CLK}}{20MHZ}\right)$		kHz
Passband ripple				±0.001	dB
Passband transition	–0.1dB attenuation		$575\left(\frac{f_{CLK}}{20MHZ}\right)$		kHz
	–3.0dB attentuation		$615\left(\frac{f_{CLK}}{20MHZ}\right)$		kHz
Stop band		$0.7\left(\frac{f_{CLK}}{20MHZ}\right)$		$19.3\left(\frac{f_{CLK}}{20MHZ}\right)$	MHz
Stop band attenuation		75			dB
Group delay			$20.8\left(\frac{20MHz}{f_{CLK}}\right)$		µs
Settling time	Complete settling		$40.8\left(\frac{20MHz}{f_{CLK}}\right)$		µs
Static Specifications					
Resolution		16			Bits
No missing codes			16		Bits
Input-referred noise			0.5	0.75	LSB, rms
Integral nonlinearity	–0.5dBFS signal		0.75		LSB
Differential nonlinearity			0.25		LSB
Offset error			–0.05		%FSR
Offset error drift			0.5		ppmFSR/°C
Gain error			0.25(1)		%
Gain error drift	Excluding reference drift		10		ppm/°C
Common-mode rejection	At DC		75		dB
Power-supply rejection	At DC		65		dB
Internal Voltage Reference	$\overline{REFEN}$ = low				
V_{REF} = (VREFP – VREFN)		2.75	3	3.25	V
VREFP		3.5	3.8	4.1	V
VREFN		0.5	0.8	1.1	V
VMID		2.3	2.4	2.6	V
V_{REF} drift			50		ppm/°C
Startup time			15		ms
External Voltage Reference	$\overline{REFEN}$ = high				
V_{REF} = (VREFP – VREFN)		2.0	3	3.25	V
VREFP		3.5	4	4.25	V
VREFN		0.5	1	1.5	V
VMID		2.3	2.5	2.6	V

(1) There is a constant gain error of 2.5% in addition to the variable gain error of ±0.25%. Therefore, the gain error is 2.5 ± 0.25%.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = –40°C to +85°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, V_{CM} = +2.7V, and R_{BIAS} = 60kΩ, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1601			UNIT
		MIN	TYP	MAX	
Clock Input					
Frequency (f_{CLK})				20	MHz
Duty cycle	f_{CLK} = 20MHz	45		55	%
Digital Input/Output					
V_{IH}		0.7 × IOVDD		IOVDD	V
V_{IL}		DGND		0.3 × IOVDD	V
V_{OH}	I_{OH} = 50µA	IOVDD – 0.5			V
V_{OL}	I_{OL} = 50µA			DGND + 0.5	V
Input leakage	DGND < V_{DIGIN} < IOVDD			±10	µA
Power-Supply Requirements					
AVDD		4.75		5.25	V
DVDD		2.7		3.3	V
IOVDD	I_{OH} = 50µA	2.7		5.25	V
AVDD current (I_{AVDD})	$\overline{REFEN}$ = low		65	77	mA
	$\overline{REFEN}$ = high		55	65	mA
DVDD current (I_{DVDD})	IOVDD = 3V		15	18	mA
IOVDD current (I_{IOVDD})	IOVDD = 3V		3	8	mA
Power dissipation	AVDD = 5V, DVDD = 3V, IOVDD = 3V, $\overline{REFEN}$ = high		330	380	mW
	$\overline{PD}$ = low, CLK disabled		10		mW
Temperature Range					
Specified		–40		+85	°C
Operating		–40		+105	°C
Storage		–60		+150	°C

DEFINITIONS

Absolute Input Voltage

Absolute input voltage, given in volts, is the voltage of each analog input (AINN or AINP) with respect to AGND.

Aperture Delay

Aperture delay is the delay between the rising edge of CLK and the sampling of the input signal.

Common-Mode Input Voltage

Common-mode input voltage (V_{CM}) is the average voltage of the analog inputs:

$$\frac{(AINP + AINN)}{2}$$

Differential Input Voltage

Differential input voltage (V_{IN}) is the voltage difference between the analog inputs (AINP−AINN).

Differential Nonlinearity (DNL)

DNL, given in least-significant bits of the output code (LSB), is the maximum deviation of the output code step sizes from the ideal value of 1LSB.

Full-Scale Range (FSR)

FSR is the difference between the maximum and minimum measurable input signals (FSR = $1.88V_{REF}$).

Gain Error

Gain error, given in %, is the error of the full-scale input signal with respect to the ideal value.

Gain Error Drift

Gain error drift, given in ppm/°C, is the drift over temperature of the gain error. The gain error is specified as the larger of the drift from ambient (T = 25°C) to the minimum or maximum operating temperatures.

Integral Nonlinearity (INL)

INL, given in least-significant bits of the output code (LSB), is the maximum deviation of the output codes from a best fit line.

Intermodulation Distortion (IMD)

IMD, given in dB, is measured while applying two input signals of the same magnitude, but with slightly different frequencies. It is calculated as the difference between the rms amplitude of the input signal to the rms amplitude of the peak spurious signal.

Offset Error

Offset Error, given in % of FSR, is the output reading when the differential input is zero.

Offset Error Drift

Offset error drift, given in ppm of FSR/°C, is the drift over temperature of the offset error. The offset error is specified as the larger of the drift from ambient (T = +25°C) to the minimum or maximum operating temperatures.

Signal-to-Noise Ratio (SNR)

SNR, given in dB, is the ratio of the rms value of the input signal to the sum of all the frequency components below $f_{CLK}/2$ (the Nyquist frequency) excluding the first six harmonics of the input signal and the dc component.

Signal-to-Noise and Distortion (SINAD)

SINAD, given in dB, is the ratio of the rms value of the input signal to the sum of all the frequency components below fCLK/2 (the Nyquist frequency) including the harmonics of the input signal but excluding the dc component.

Spurious-Free Dynamic Range (SFDR)

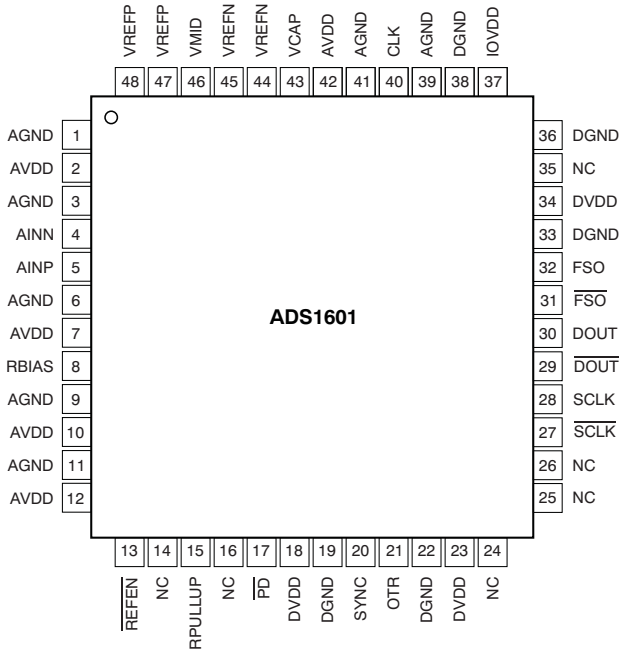
SFDR, given in dB, is the difference between the rms amplitude of the input signal to the rms amplitude of the peak spurious signal.

Total Harmonic Distortion (THD)

THD, given in dB, is the ratio of the sum of the rms value of the first six harmonics of the input signal to the rms value of the input signal.

PIN ASSIGNMENTS

TQFP PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	1, 3, 6, 9, 11, 39, 41	Analog	Analog ground
AVDD	2, 7, 10, 12, 42	Analog	Analog supply
AINN	4	Analog input	Negative analog input
AINP	5	Analog input	Positive analog input
RBIAS	8	Analog	Terminal for external analog bias setting resistor.
$\overline{\text{REFEN}}$	13	Digital input: active low	Internal reference enable. Internal pull-down resistor of 170kΩ to DGND.
NC	14, 16, 24–26, 35	Do not connect	These terminals must be left unconnected.
RPULLUP	15	Digital Input	Pull-up to DVDD with 10kΩ resistor (see Figure 50).
$\overline{\text{PD}}$	17	Digital input: active low	Power-down all circuitry. Internal pull-up resistor of 170kΩ to DGND.
DVDD	18, 23, 34	Digital	Digital supply
DGND	19, 22, 33, 36, 38	Digital	Digital ground
SYNC	20	Digital input	Synchronization control input
OTR	21	Digital output	Indicates analog input signal is out of range.
SCLK	28	Digital output	Serial clock output
$\overline{\text{SCLK}}$	27	Digital output	Serial clock output, complementary signal.
DOUT	30	Digital output	Data output
$\overline{\text{DOUT}}$	29	Digital output	Data output, complementary signal.
FSO	32	Digital output	Frame synchronization output
$\overline{\text{FSO}}$	31	Digital output	Frame synchronization output, complementary signal.
IOVDD	37	Digital	Digital I/O supply
CLK	40	Digital output	Clock input supply
VCAP	43	Analog	Terminal for external bypass capacitor connection to internal bias voltage.
VREFN	44, 45	Analog	Negative reference voltage
VMID	46	Analog	Midpoint voltage
VREFP	47, 48	Analog	Positive reference voltage

TIMING DIAGRAMS

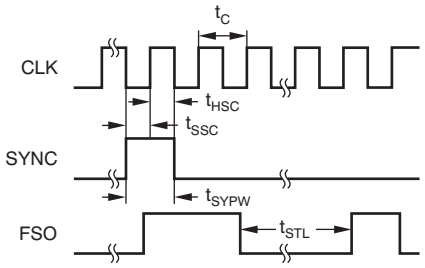


Figure 1. Initialization Timing

TIMING REQUIREMENTS

For T_A = –40°C to +85°C, DVDD = 2.7V to 3.6V, and IOVDD = 2.7V to 5.25V.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{SYPW}	SYNC positive pulse width	1			CLK period
t_C	Clock period (CLK)	50			ns
t_{SSC}	Setup time; SYNC rising edge to CLK rising edge	0.5			CLK period
t_{HSC}	Hold time; CLK rising edge to SYNC falling edge	0.5			CLK period
t_{STL}	Settling time of the ADS1601; FSO falling edge to next FSO rising edge			833	CLK periods

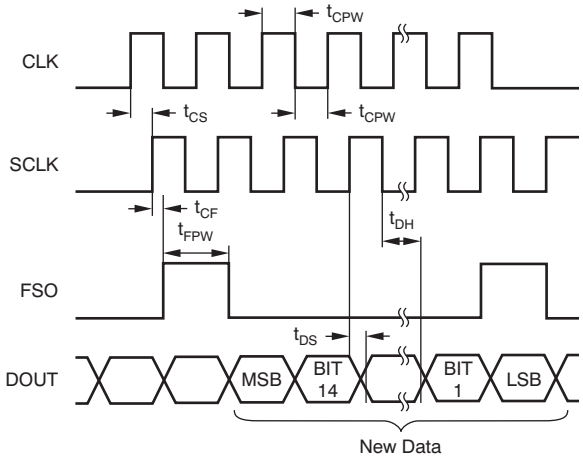


Figure 2. Data Retrieval Timing

TIMING REQUIREMENTS

For T_A = –40°C to +85°C, DVDD = 2.7V to 3.6V, and IOVDD = 2.7V to 5.25V.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{CS}	Rising edge of CLK to rising edge of SCLK			15	ns
t_{CF}	Rising edge of SCLK to rising edge of FSO			5	ns
t_{CPW}	CLK positive or negative pulse width	25			ns
t_{FPW}	Frame sync output high pulse width		1		CLK period
t_{DS}	SCLK rising edge to new DOUT valid			5	ns
t_{DH}	SCLK falling edge to DOUT invalid	20			ns

TYPICAL CHARACTERISTICS

All specifications at T_A = +25°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, V_{CM} = +2.7V, and R_{BIAS} = 60kΩ, unless otherwise noted.

SPECTRAL RESPONSE

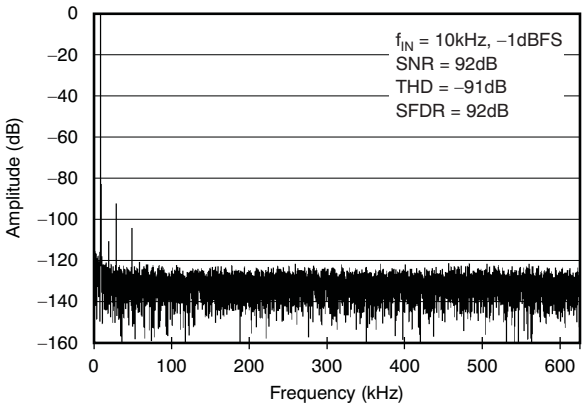


Figure 3.

SPECTRAL RESPONSE

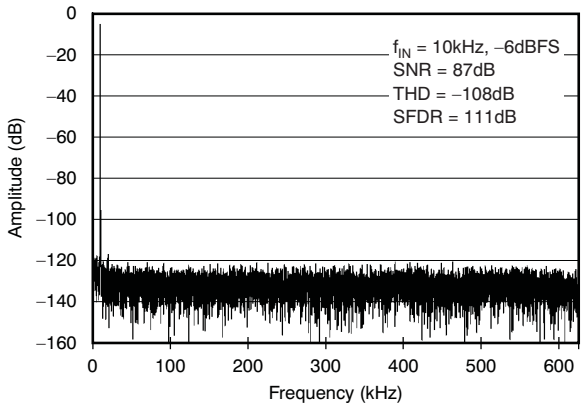


Figure 4.

SPECTRAL RESPONSE

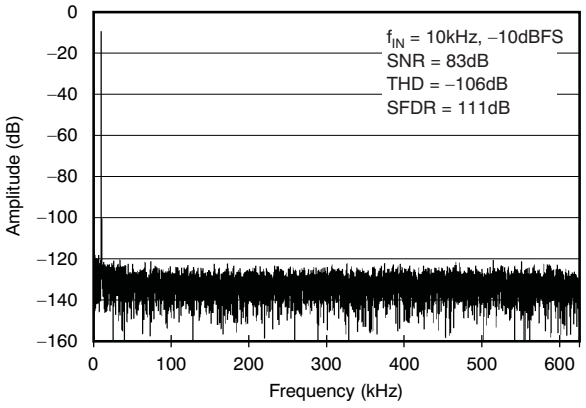


Figure 5.

SPECTRAL RESPONSE

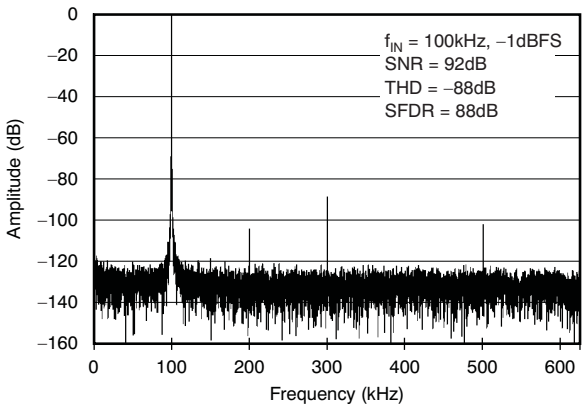


Figure 6.

SPECTRAL RESPONSE

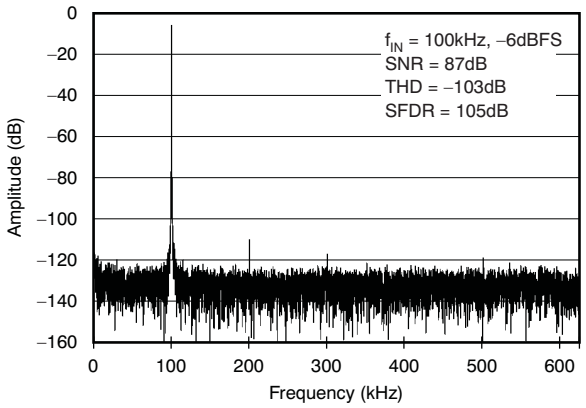


Figure 7.

SPECTRAL RESPONSE

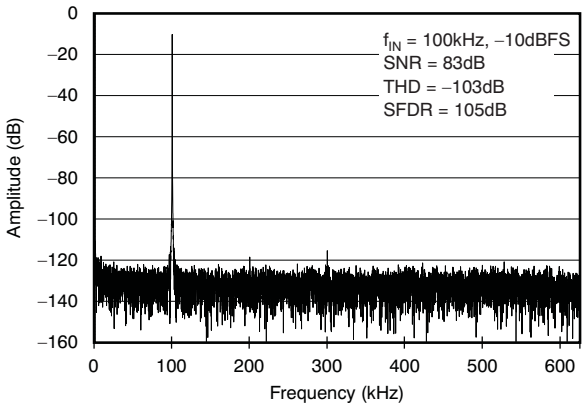


Figure 8.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, V_{CM} = +2.7V, and R_{BIAS} = 60kΩ, unless otherwise noted.

SPECTRAL RESPONSE

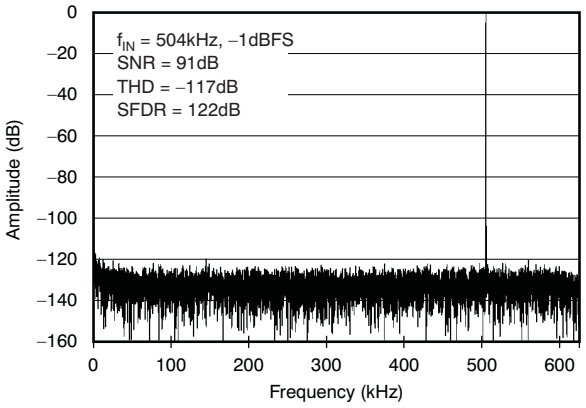


Figure 9.

SPECTRAL RESPONSE

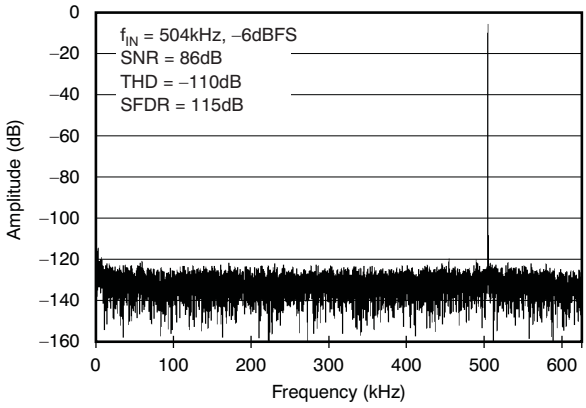


Figure 10.

SPECTRAL RESPONSE

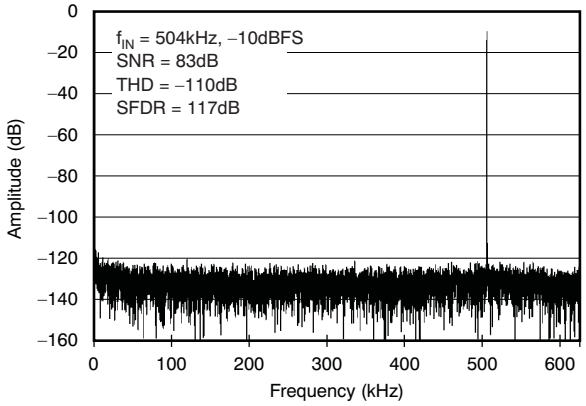


Figure 11.

SNR, THD, AND SFDR vs INPUT SIGNAL AMPLITUDE

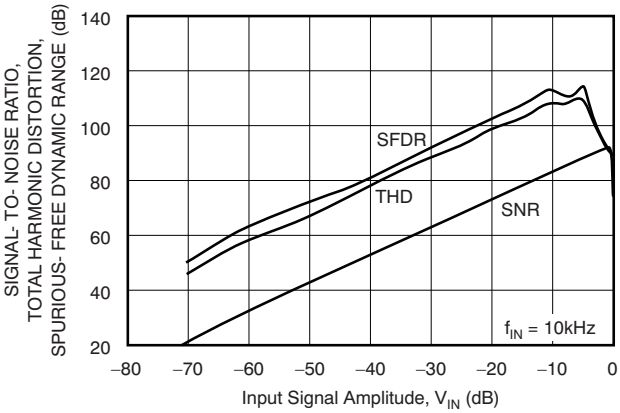


Figure 12.

SNR, THD, AND SFDR vs INPUT SIGNAL AMPLITUDE

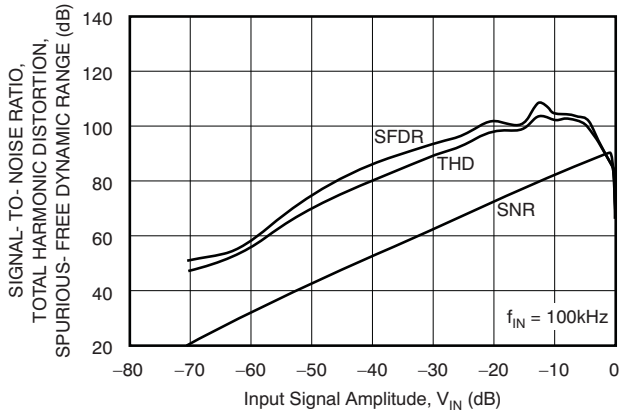


Figure 13.

SNR, THD, AND SFDR vs INPUT SIGNAL AMPLITUDE

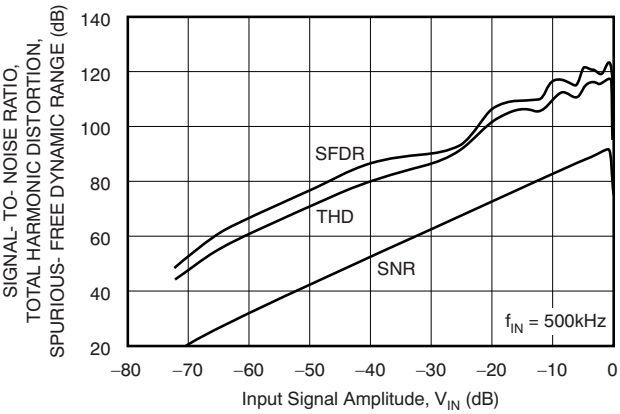


Figure 14.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, V_{CM} = +2.7V, and R_{BIAS} = 60kΩ, unless otherwise noted.

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

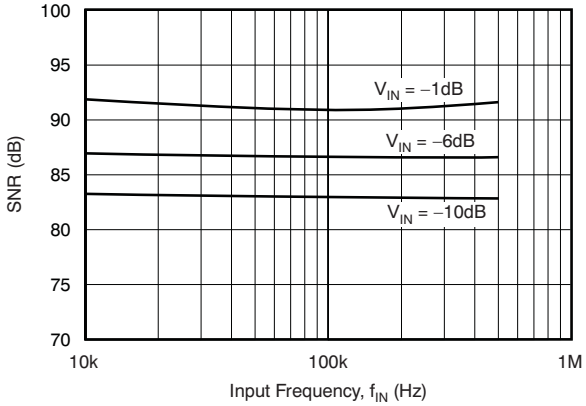


Figure 15.

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

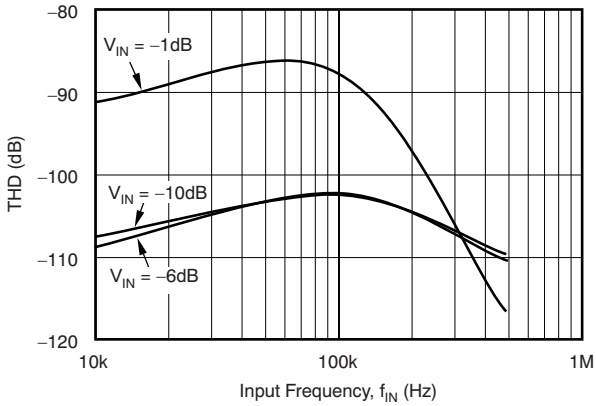


Figure 16.

SPURIOUS-FREE DYNAMIC RANGE vs INPUT FREQUENCY

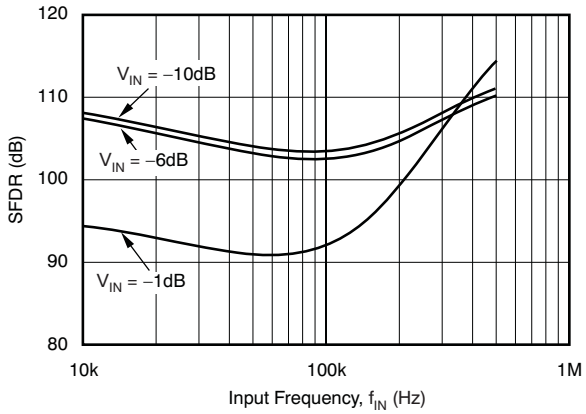


Figure 17.

SIGNAL-TO-NOISE RATIO vs INPUT COMMON-MODE VOLTAGE

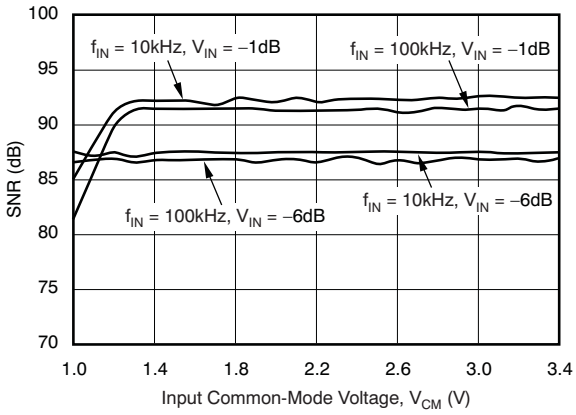


Figure 18.

TOTAL HARMONIC DISTORTION vs INPUT COMMON-MODE VOLTAGE

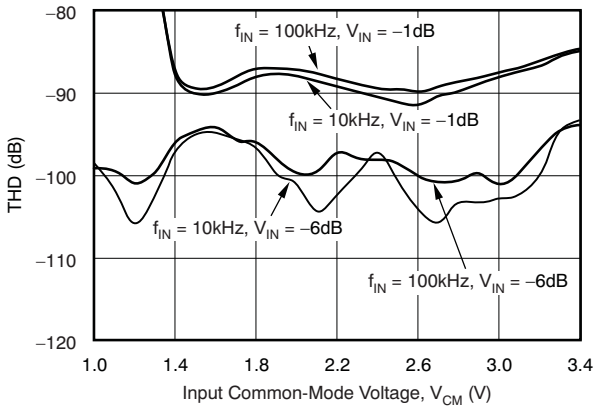


Figure 19.

SPURIOUS-FREE DYNAMIC RANGE vs INPUT COMMON-MODE VOLTAGE

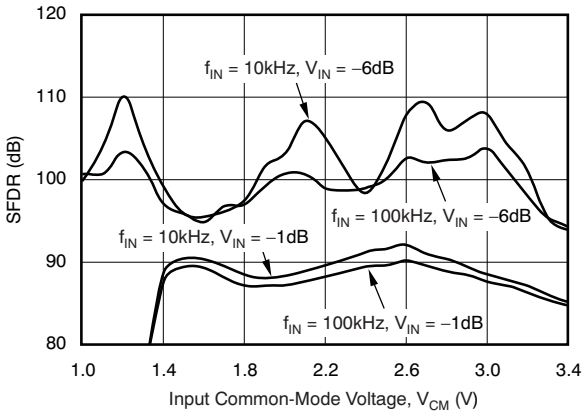


Figure 20.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, V_{CM} = +2.7V, and R_{BIAS} = 60kΩ, unless otherwise noted.

SIGNAL-TO-NOISE RATIO vs CLOCK FREQUENCY

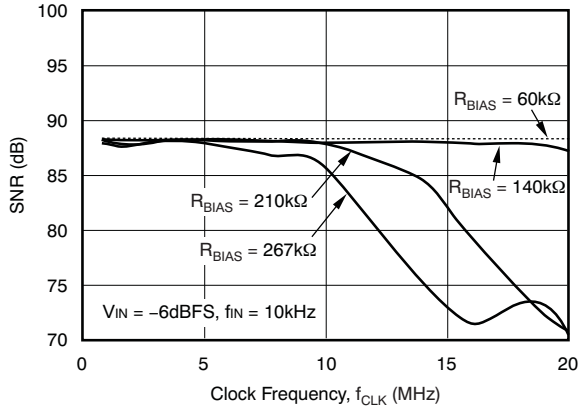


Figure 21.

TOTAL HARMONIC DISTORTION vs CLOCK FREQUENCY

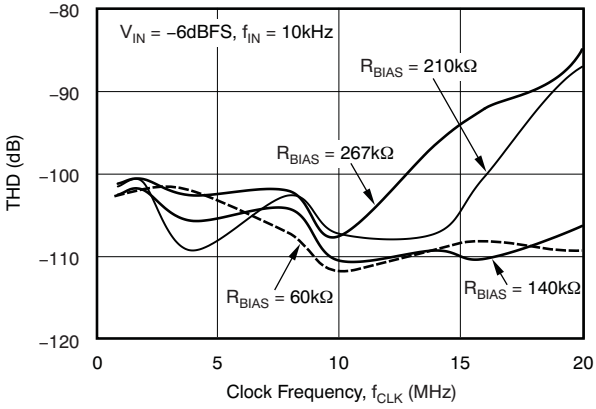


Figure 22.

SPURIOUS-FREE DYNAMIC RANGE vs CLOCK FREQUENCY

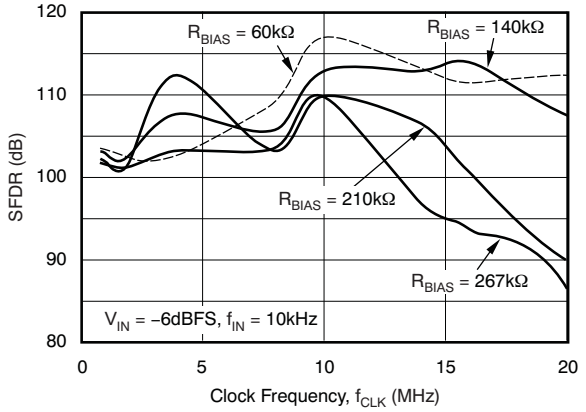


Figure 23.

NOISE vs DC INPUT VOLTAGE

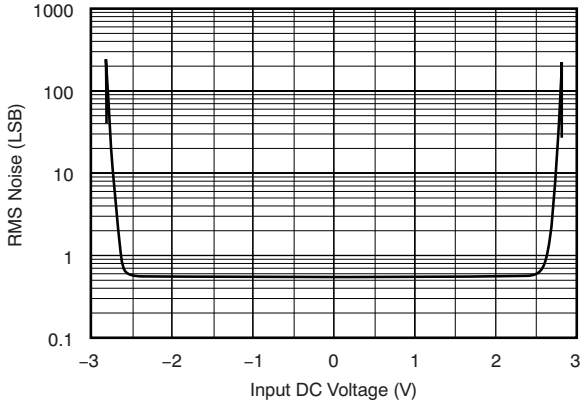


Figure 24.

NOISE HISTOGRAM

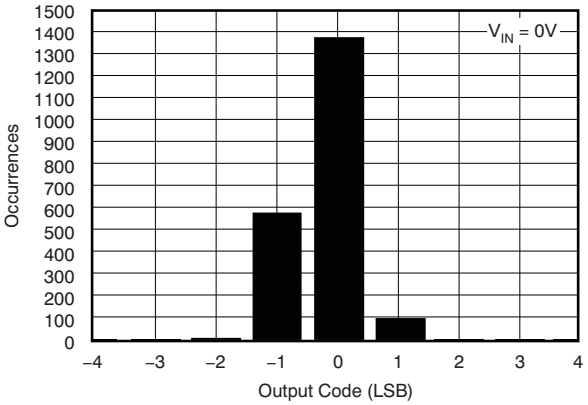


Figure 25.

OFFSET DRIFT OVER TIME

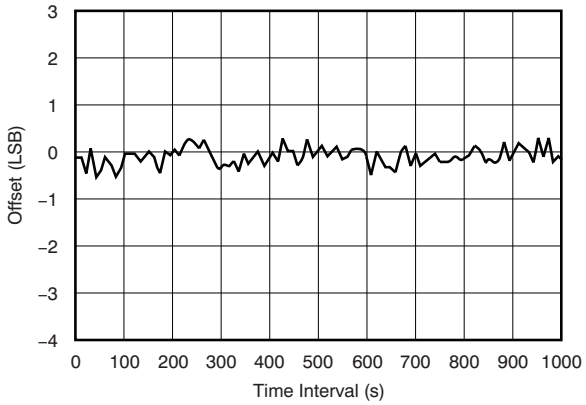


Figure 26.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, V_{CM} = +2.7V, and R_{BIAS} = 60kΩ, unless otherwise noted.

POWER-SUPPLY CURRENT vs TEMPERATURE

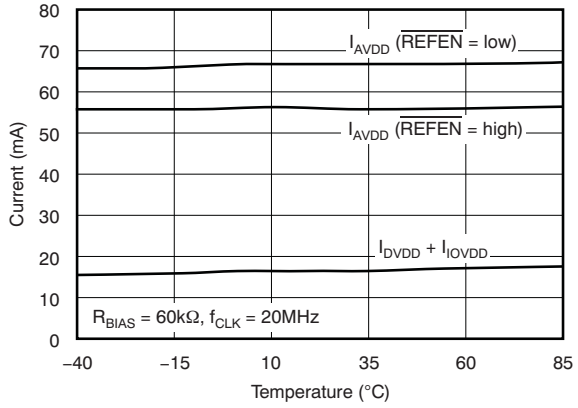


Figure 27.

SUPPLY CURRENT vs CLOCK FREQUENCY

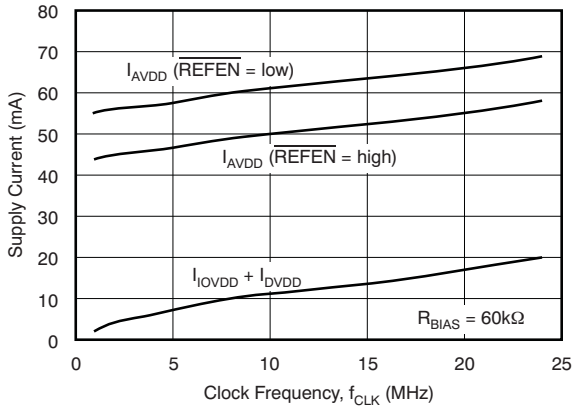


Figure 28.

ANALOG SUPPLY CURRENT vs R_{BIAS}

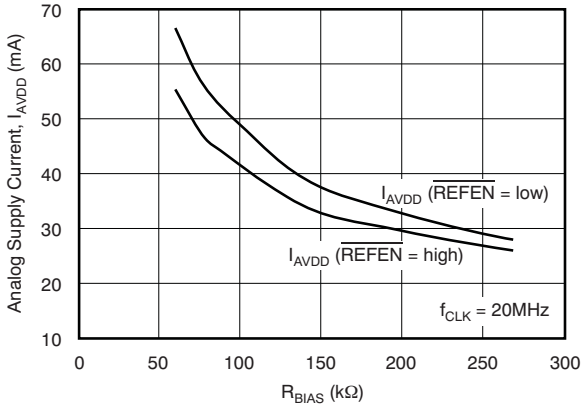


Figure 29.

SIGNAL-TO-NOISE RATIO vs TEMPERATURE

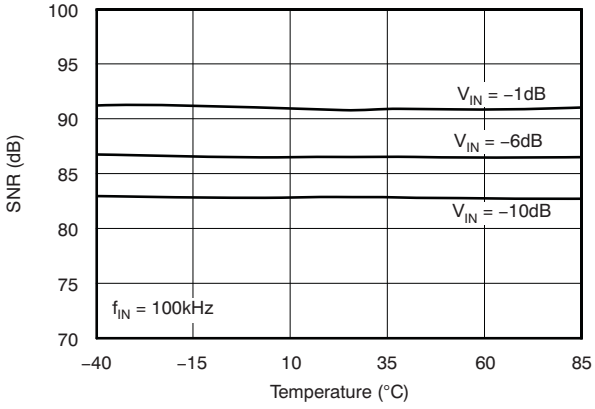


Figure 30.

TOTAL HARMONIC DISTORTION vs TEMPERATURE

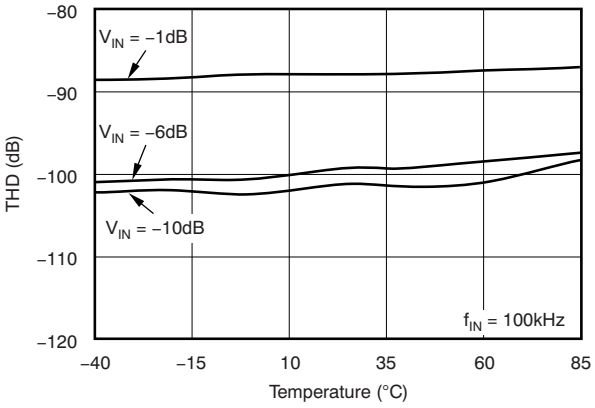


Figure 31.

SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE

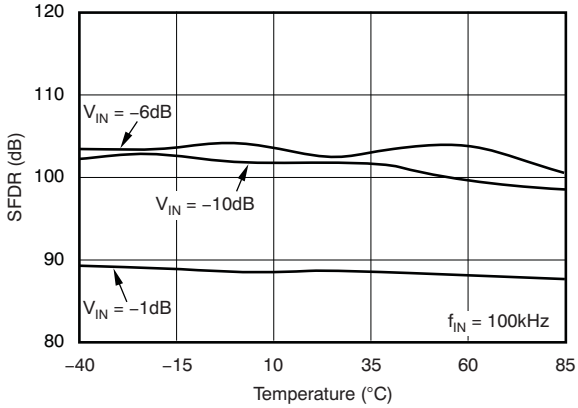


Figure 32.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, V_{CM} = +2.7V, and R_{BIAS} = 60kΩ, unless otherwise noted.

V_{REF} vs TEMPERATURE

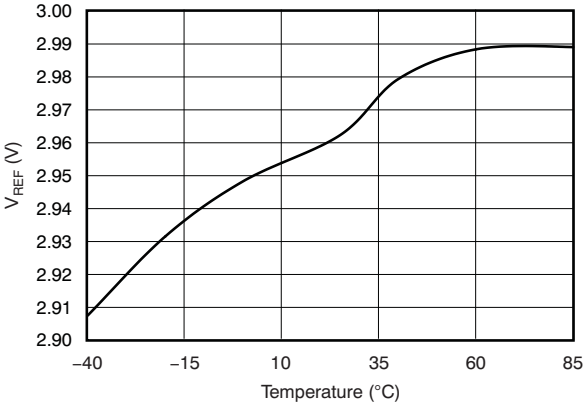


Figure 33.

INTERMODULATION RESPONSE

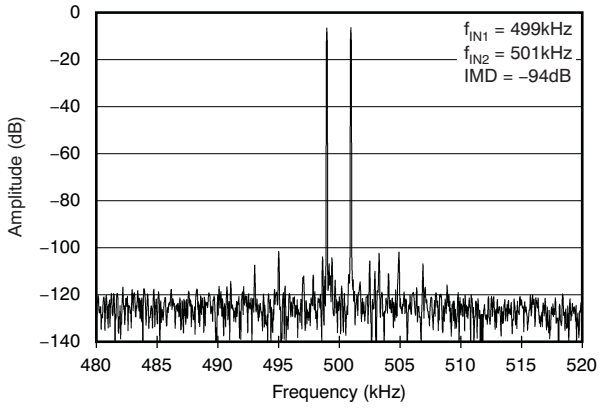


Figure 34.

OVERVIEW

The ADS1601 is a high-performance delta-sigma ADC. The modulator uses an inherently stable 2-1-1 multi-stage architecture incorporating proprietary circuitry that allows for very linear high-speed operation. The modulator samples the input signal at 20MSPS (when f_{CLK} = 20MHz). A low-ripple linear phase digital filter decimates the modulator output by 16 to provide high resolution 16-bit output data.

Conceptually, the modulator and digital filter measure the differential input signal, V_{IN} = (AINP – AINN), against the scaled differential reference, V_{REF} = (VREFP – VREFN), as shown in Figure 35. The voltage reference can either be generated internally or supplied externally. A three-wire serial interface, designed for direct connection to DSPs, outputs the data. A separate power supply for the I/O allows flexibility for interfacing to different logic families. Out-of-range conditions are indicated with a dedicated digital output pin. Analog power dissipation is controlled using an external resistor. This control allows reduced dissipation when operating at slower speeds. When not in use, power consumption can be dramatically reduced by setting the $\overline{PD}$ pin low to enter Power-Down mode.

ANALOG INPUTS (AINP, AINN)

The ADS1601 measures the differential signal, V_{IN} = (AINP – AINN), against the differential reference, V_{REF} = (VREFP – VREFN). The most positive measurable differential input is $0.94V_{REF}$, which produces the most positive digital output code of 7FFFh. Likewise, the most negative measurable differential input is $–0.94V_{REF}$, which produces the most negative digital output code of 8000h.

The ADS1601 supports a very wide range of input signals. For V_{REF} = 3V, the full-scale input voltage is ±2.82V. Having such a wide input range makes out-of-range signals unlikely. However, if an out-of-range signal occurs, the digital output OTR goes high.

The analog inputs must be driven with a differential signal to achieve optimum performance. For the input signal:

$$V_{CM} = \frac{AINP + AINN}{2}$$

the recommended common-mode voltage is 2.7V. In addition to the differential and common-mode input voltages, the absolute input voltage is also important. This is the voltage on either input (AINP or AINN) with respect to AGND. The range for this voltage is:

–0.1V < (AINN or AINP) < 4.6V

If either input is taken below –0.1V, ESD protection diodes on the inputs will turn on. Exceeding 4.6V on either input results in degradation in the linearity performance. ESD protection diodes will also turn on if the inputs are taken above AVDD (+5V).

The recommended absolute input voltage is:

–0.1V < (AINN or AINP) < 4.2V

Keeping the inputs within this range provides for optimum performance.

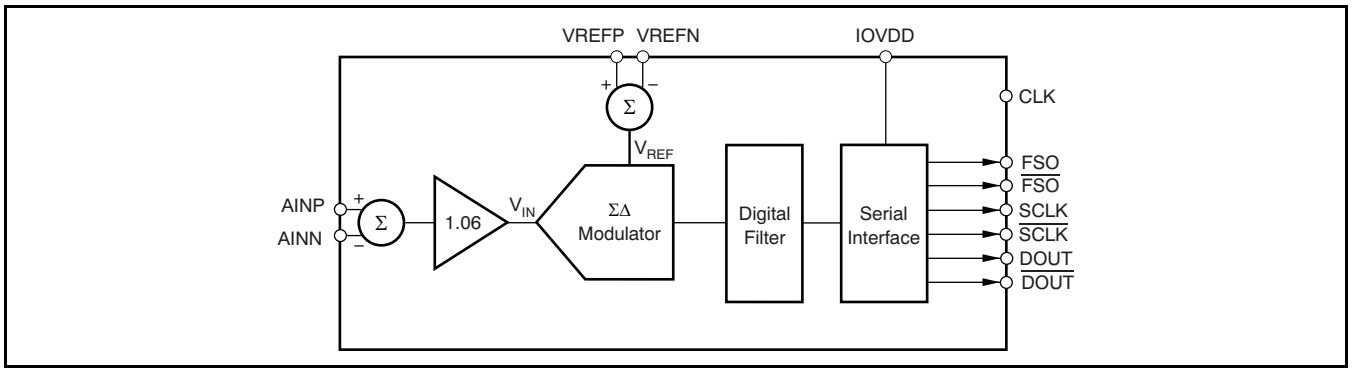


Figure 35. Conceptual Block Diagram

INPUT CIRCUITRY

The ADS1601 uses switched-capacitor circuitry to measure the input voltage. Internal capacitors are charged by the inputs and then discharged internally with this cycle repeating at the frequency of CLK. Figure 36 shows a conceptual diagram of these circuits. Switches S_2 represent the net effect of the modulator circuitry in discharging the sampling capacitors; the actual implementation is different. The timing for switches S_1 and S_2 is shown in Figure 37.

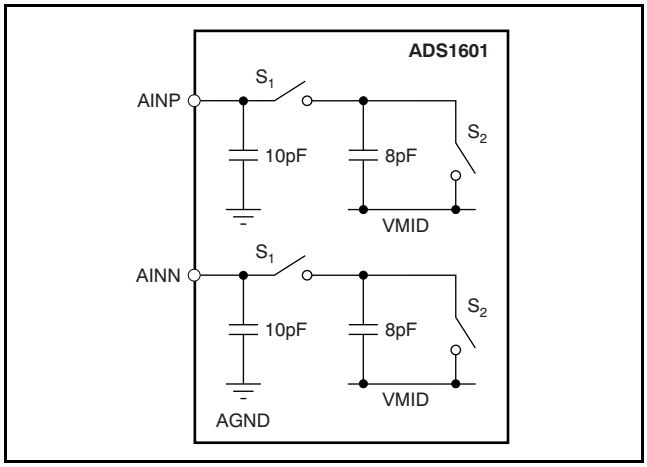


Figure 36. Conceptual Diagram of Internal Circuitry Connected to the Analog Inputs

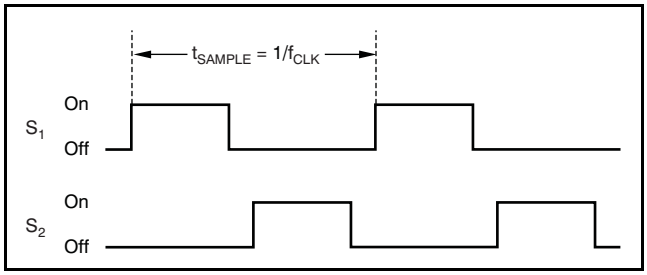
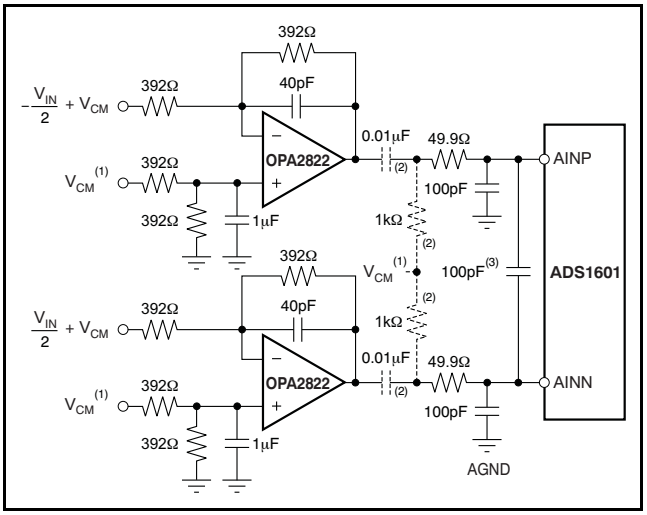


Figure 37. Timing for the Switches in Figure 36

DRIVING THE INPUTS

The external circuits driving the ADS1601 inputs must be able to handle the load presented by the switching capacitors within the ADS1601. The input switches S_1 in Figure 36 are closed for approximately one-half of the sampling period, t_{SAMPLE}, allowing only ≠ 24ns for the internal capacitors to be charged by the inputs when f_{CLK} = 20MHz.

Figure 38 and Figure 39 show the recommended circuits when using single-ended or differential op amps, respectively. *The analog inputs must be driven differentially to achieve optimum performance.* The external capacitors, between the inputs and from each input to AGND, improve linearity and should be placed as close to the pins as possible. Place the drivers close to the inputs and use good capacitor bypass techniques on their supplies, such as a smaller high-quality ceramic capacitor in parallel with a larger capacitor. Keep the resistances used in the driver circuits low—thermal noise in the driver circuits degrades the overall noise performance. When the signal can be ac-coupled to the ADS1601 inputs, a simple RC filter can set the input common-mode voltage. The ADS1601 is a high-speed, high-performance ADC. Special care must be taken when selecting the test equipment and setup used with this device. Pay particular attention to the signal sources to ensure they do not limit performance when measuring the ADS1601.



(1) Recommended V_{CM} = 2.7V.

(2) Optional ac-coupling circuit provides common-mode input voltage.

(3) Increase to 390pF when f_{IN} ≤ 100kHz for improved SNR and THD.

Figure 38. Recommended Driver Circuit Using the OPA2822

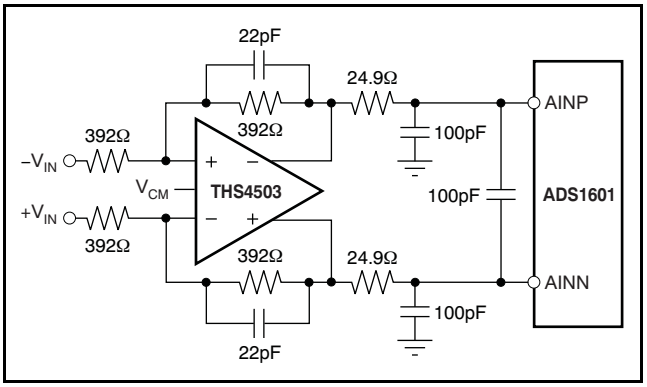


Figure 39. Recommended Driver Circuit Using the THS4503 Differential Amplifier

REFERENCE INPUTS (VREFN, VREFP, VMID)

The ADS1601 can operate from an internal or external voltage reference. In either case, the reference voltage V_{REF} is set by the differential voltage between VREFN and VREFP: V_{REF} = (VREFP – VREFN). VREFP and VREFN each use two pins, which should be shorted together. VMID equals approximately 2.5V and is used by the modulator. VCAP connects to an internal node and must also be bypassed with an external capacitor.

INTERNAL REFERENCE ($\overline{\text{REFEN}}$ = LOW)

To use the internal reference, set the $\overline{\text{REFEN}}$ pin low. This activates the internal circuitry that generates the reference voltages. The internal reference voltages are applied to the pins. Good bypassing of the reference pins is critical to achieve optimum performance and is done by placing the bypass capacitors as close to the pins as possible. Figure 40 shows the recommended bypass capacitor values. Use high-quality ceramic capacitors for the smaller values. Avoid loading the internal reference with external circuitry. If the ADS1601 internal reference is to be used by other circuitry, buffer the reference voltages to prevent directly loading the reference pins.

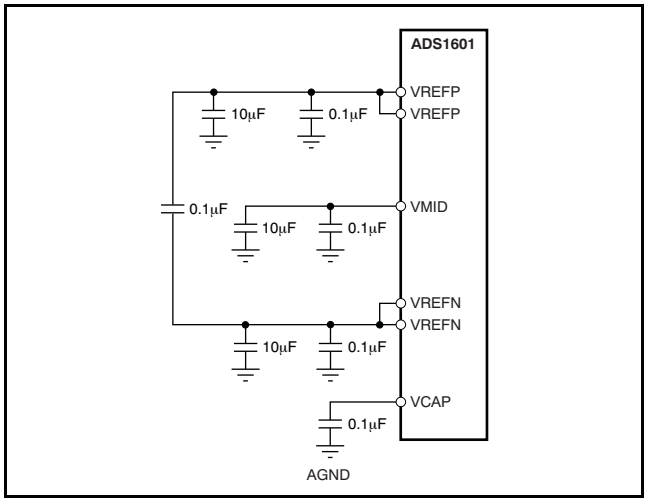


Figure 40. Reference Bypassing When Using the Internal Reference

EXTERNAL REFERENCE ($\overline{\text{REFEN}}$ = HIGH)

To use an external reference, set the $\overline{\text{REFEN}}$ pin high. This deactivates the internal generators for VREFP, VREFN, and VMID, and saves approximately 25mA of current on the analog supply (AVDD). The voltages applied to these pins must be within the values specified in the Electrical Characteristics table. Typically, VREFP = 4V, VMID = 2.5V, and VREFN = 1V. The external circuitry must be capable of providing both a dc and a transient current. Figure 41 shows a simplified diagram of the internal circuitry of the reference when the internal reference is disabled. As with the input circuitry, switches S_1 and S_2 open and close as shown by the timing in Figure 37.

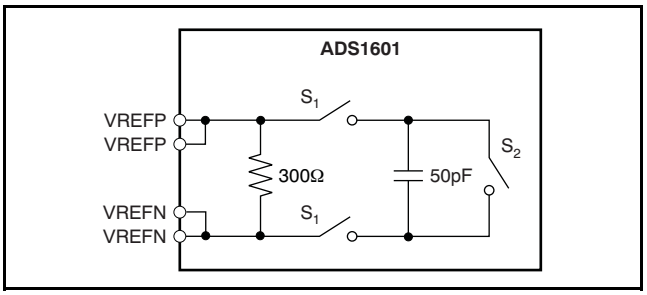


Figure 41. Conceptual Internal Circuitry for the Reference When $\overline{\text{REFEN}}$ = High

Figure 42 shows the recommended circuitry for driving these reference inputs. Keep the resistances used in the buffer circuits low to prevent excessive thermal noise from degrading performance. Layout of these circuits is critical; be sure to follow good high-speed layout practices. Place the buffers, and especially the bypass capacitors, as close to the pins as possible. VCAP is unaffected by the setting on $\overline{\text{REFEN}}$ and must be bypassed when using the internal or an external reference.

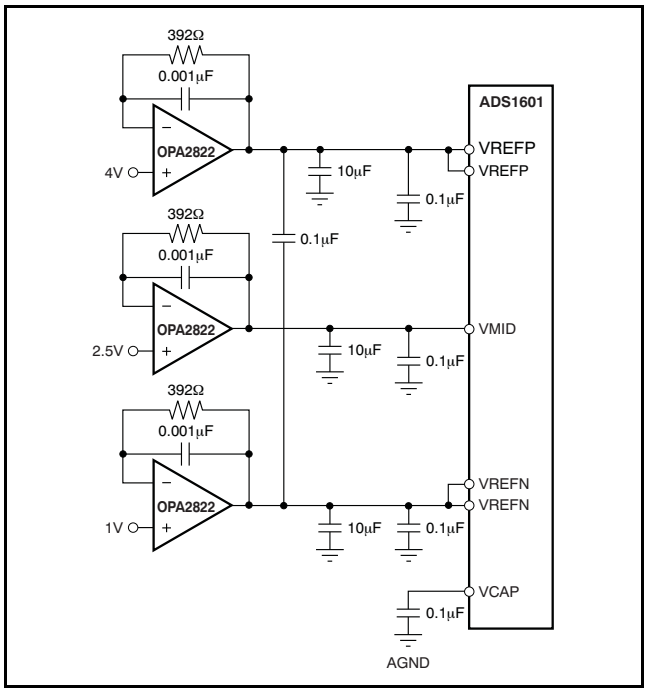


Figure 42. Recommended Buffer Circuit When Using an External Reference

CLOCK INPUT (CLK)

The ADS1601 requires an external clock signal to be applied to the CLK input pin. The sampling of the modulator is controlled by this clock signal. As with any high-speed data converter, a high quality clock is essential for optimum performance. Crystal clock oscillators are the recommended CLK source; other sources, such as frequency synthesizers, are usually inadequate. Make sure to avoid excess ringing on the CLK input; keeping the trace as short as possible helps.

Measuring high-frequency, large amplitude signals requires tight control of clock jitter. The uncertainty during sampling of the input from clock jitter limits the maximum achievable SNR. This effect becomes more pronounced with higher frequency and larger magnitude inputs. Fortunately, the ADS1601 oversampling topology reduces clock jitter sensitivity over that of Nyquist rate converters such as pipeline and successive approximation converters by a factor of $\sqrt{16}$.

In order to not limit the ADS1601 SNR performance, keep the jitter on the clock source below the values shown in Table 1. When measuring lower frequency and lower amplitude inputs, more CLK jitter can be tolerated. In determining the allowable clock source jitter, select the worst-case input (highest frequency, largest amplitude) that will be seen in the application.

Table 1. Maximum Allowable Clock Source Jitter for Different Input Signal Frequencies and Amplitude

INPUT SIGNAL		MAXIMUM ALLOWABLE CLOCK SOURCE JITTER
MAXIMUM FREQUENCY	MAXIMUM AMPLITUDE	
500kHz	–0.5dB	6ps
500kHz	–20dB	60ps
100kHz	–0.5dB	30ps
100kHz	–20dB	300ps

DATA FORMAT

The 16-bit output data are in binary two's complement format as shown in Table 2. When the input is positive out-of-range, exceeding the positive full-scale value of $+0.94V_{REF}$, the output clips to all 7FFFh and the OTR output goes high.

Likewise, when the input is negative out-of-range by going below the negative full-scale value of $–0.94V_{REF}$, the output clips to 8000h and the OTR output goes high. The OTR remains high while the input signal is out-of-range.

Table 2. Output Code versus Input Signal

INPUT SIGNAL (INP – INN)	IDEAL OUTPUT CODE(1)	OTR
≥ $+0.94V_{REF}$ (> 0dB)	7FFFh	1
$–0.94V_{REF}$ (0dB)	7FFFh	0
$\frac{+0.94V_{REF}}{2^{15}-1}$	001h	0
0	0000h	0
$\frac{-0.94V_{REF}}{2^{15}-1}$	FFFFh	0
$-0.94V_{REF}\left(\frac{2^{15}}{2^{15}-1}\right)$	8000h	0
$-0.94V_{REF}\left(\frac{2^{15}}{2^{15}-1}\right)$	8000h	1

(1) Excludes effects of noise, INL, offset and gain errors.

OUT-OF-RANGE INDICATION (OTR)

If the output code exceeds the positive or negative full-scale, the out-of-range digital output OTR will go high on the falling edge of SCLK. When the output code returns within the full-scale range, OTR returns low on the falling edge of SCLK.

DATA RETRIEVAL

Data retrieval is controlled through a simple serial interface. The interface operates in a master fashion by outputting both a frame sync indicator (FSO) and a serial clock (SCLK). Complementary outputs are provided for the frame sync output (FSO), serial clock (SCLK), and data output (DOUT). When not needed, leave the complementary outputs unconnected.

INITIALIZING THE ADS1601

After the power supplies have stabilized, you must initialize the ADS1601 by issuing a SYNC pulse as shown in Figure 1. This operation needs only to be done once after power-up and does not need to be performed when exiting the Power-Down mode. Note that the ADS1601 silicon was revised in June 2006. The digital interface timing specifications were modified slightly from the previous revision. This data sheet reflects behavior of the latest revision. Contact the factory for more information on the previous revision.

SYNCHRONIZING MULTIPLE ADS1601s

The SYNC input can be used to synchronize multiple ADS1601s to provide simultaneous sampling. All devices to be synchronized must use a common CLK input. With the CLK inputs running, pulse SYNC on the falling edge of CLK, as shown in Figure 43. Afterwards, the converters will be converting synchronously with the FSO outputs updating simultaneously. After synchronization, FSO is held low until the digital filter has fully settled.

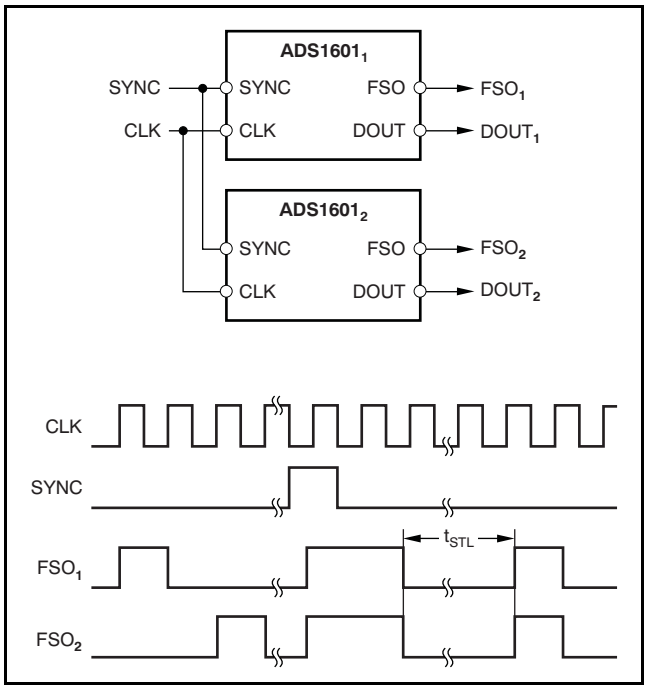


Figure 43. Synchronizing Multiple Converters

STEP RESPONSE

Figure 44 plots the normalized step response for an input applied at t = 0. The x-axis units of time are conversions cycles. It takes 51 cycles to fully settle; for f_{CLK} = 20MHz, this corresponds to 40.8µs.

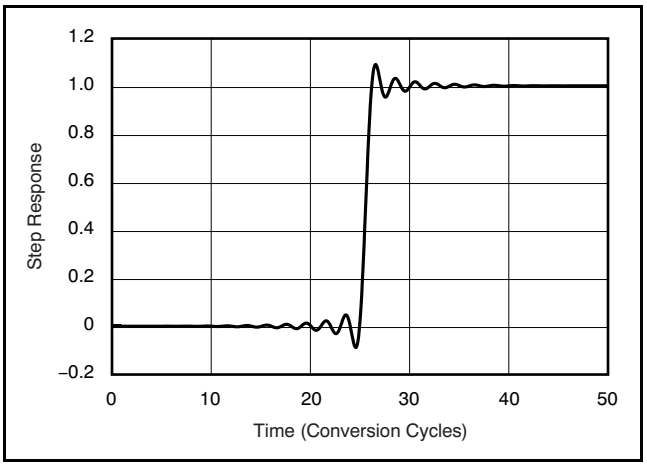


Figure 44. Step Response

FREQUENCY RESPONSE

The linear phase FIR digital filter sets the overall frequency response. Figure 45 shows the frequency response from dc to 10MHz for f_{CLK} = 20MHz. The frequency response of the ADS1601 filter scales directly with CLK frequency. For example, if the CLK frequency is decreased by half (to 10MHz), the values on the X-axis in Figure 45 would need to be scaled by half, with the span becoming dc to 5MHz. Figure 46 shows the passband ripple from dc to 600kHz (f_{CLK} = 20MHz). Figure 47 shows a closer view of the passband transition by plotting the response from 400kHz to 650kHz (f_{CLK} = 20MHz).

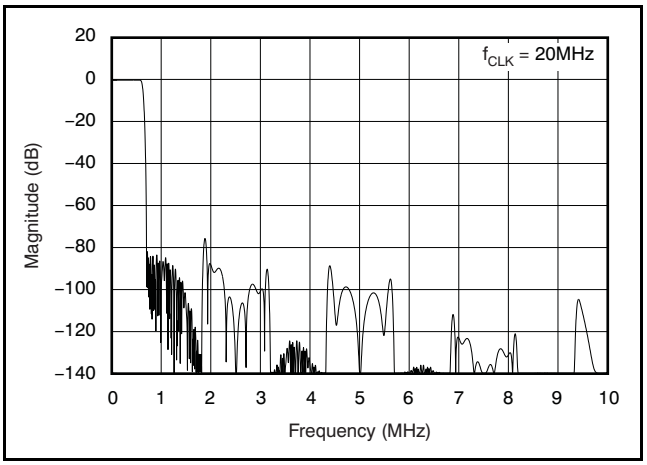


Figure 45. Frequency Response

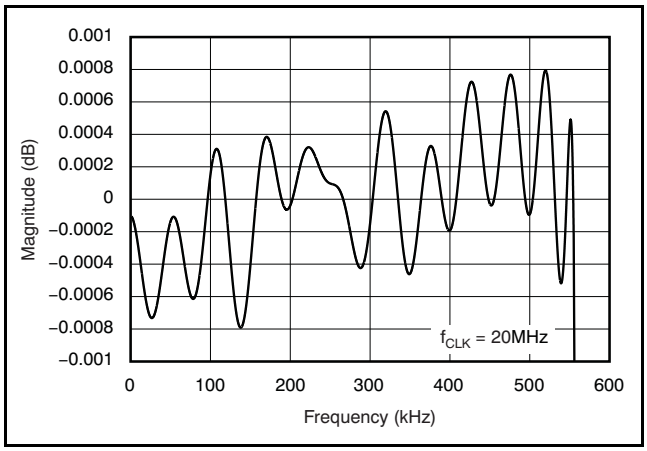


Figure 46. Passband Ripple

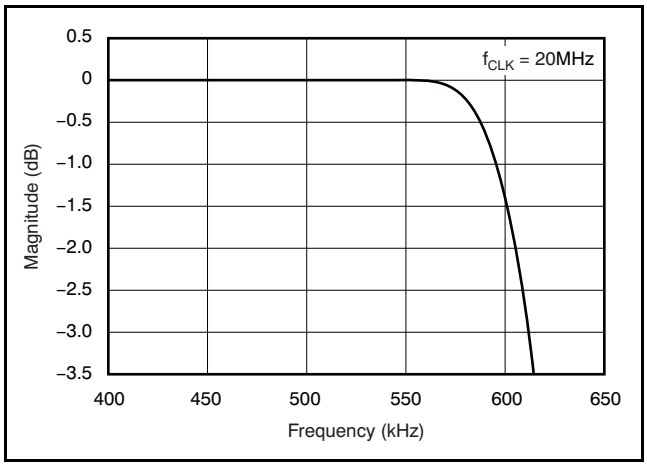


Figure 47. Passband Transition

ANTI-ALIAS REQUIREMENTS

Higher frequency, out-of-band signals must be eliminated to prevent aliasing with ADCs. Fortunately, the ADS1601 on-chip digital filter greatly simplifies this filtering requirement. Figure 48 shows the ADS1601 response out to 60MHz (f_{CLK} = 20MHz). Since the stop band extends out to 19.3MHz, the anti-alias filter in front of the ADS1601 only needs to be designed to remove higher frequency signals than this, which can usually be accomplished with a simple RC circuit on the input driver.

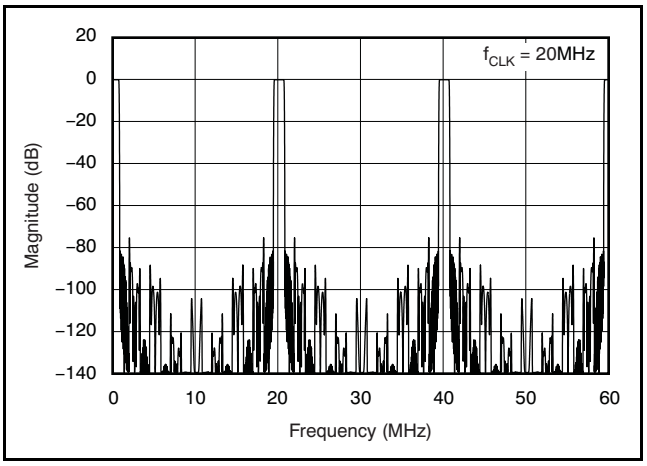


Figure 48. Frequency Response Out to 120MHz

ANALOG POWER DISSIPATION

An external resistor connected between the RBIAS pin and the analog ground sets the analog current level, as shown in Figure 49. The current is inversely proportional to the resistor value. Table 3 shows the recommended values of R_{BIAS} for different CLK frequencies. Notice that the analog current can be reduced when using a slower frequency CLK input because the modulator has more time to settle. Avoid adding any capacitance in parallel to R_{BIAS} because this interferes with the internal circuitry used to set the biasing. Please note that changing R_{BIAS} changes internally-generated voltages, including the internal reference; therefore, it should be understood that the recommendations of Table 3 are for external reference only.

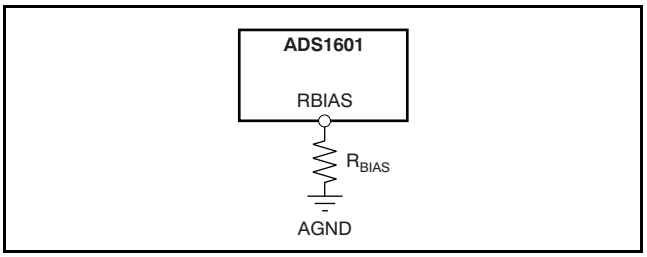


Figure 49. External Resistor Used to Set Analog Power Dissipation

Table 3. Recommended R_{BIAS} Resistor Values for Different CLK Frequencies

f_{CLK}	DATA RATE	R_{BIAS}	TYPICAL POWER DISSIPATION WITH $\overline{REFEN}$ HIGH
5MHz	315kSPS	267k	100mW
10MHz	625kSPS	210k	145mW
15MHz	940kSPS	140k	200mW
20MHz	1.25MSPS	60k	325mW

POWER DOWN ($\overline{PD}$)

When not in use, the ADS1601 can be powered down by taking the $\overline{PD}$ pin low. All circuitry is shut down, including the voltage reference. To minimize the digital current during power down, stop the clock signal supplied to the CLK input. There is an internal pull-up resistor of 170kΩ on the $\overline{PD}$ pin, but it is recommended that this pin be connected to IOVDD if not used. Make sure to allow time for the reference to start up after exiting power-down mode. The internal reference typically requires 15ms. After the reference has stabilized, allow at least 100 conversions for the modulator and digital filter to settle before retrieving data.

POWER SUPPLIES

Three supplies are used on the ADS1601: analog (AVDD), digital (DVDD) and digital I/O (IOVDD). Each supply must be suitably bypassed to achieve the best performance. It is recommended that a 1µF and 0.1µF ceramic capacitor be placed as close to each supply pin as possible. Connect each supply-pin bypass capacitor to the associated ground, as shown in Figure 50. Each main supply bus should also be bypassed with a bank of capacitors from 47µF to 0.1µF, as shown. The I/O and digital supplies (IOVDD and DVDD) can be connected together when using the same voltage. In this case, only one bank of 47µF to 0.1µF capacitors is needed on the main supply bus, though each supply pin must still be bypassed with a 1µF and 0.1µF ceramic capacitor.

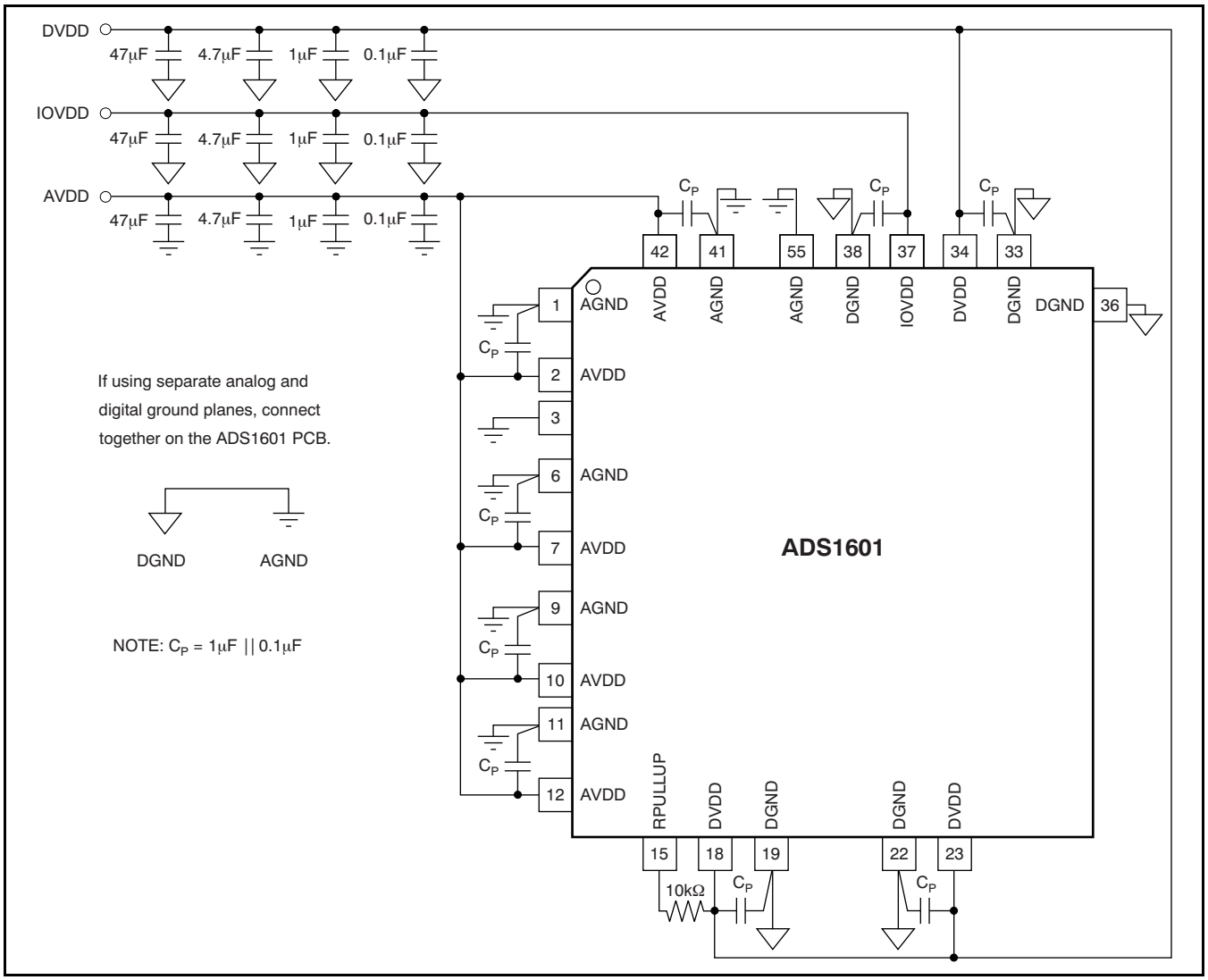


Figure 50. Recommended Power-Supply Bypassing

LAYOUT ISSUES AND COMPONENT SELECTION

The ADS1601 is a very high-speed, high-resolution data converter. In order to achieve maximum performance, the user must give very careful consideration to both the layout of the printed circuit board (PCB) in addition to the routing of the traces. Capacitors that are critical to achieve the best performance from the device should be placed as close to the pins of the device as possible. These include capacitors related to the analog inputs, the reference, and the power supplies.

For critical capacitors, it is recommended that Class II dielectrics such as Z5U be avoided. These dielectrics have a narrow operating temperature, a large tolerance on the capacitance, and lose up to 20% of the rated capacitance over 10,000 hours. Rather, select capacitors with a Class I dielectric. C0G (also known as NP0), for example, has a tight tolerance less than ±30ppm/°C and is very stable over time. Should Class II capacitors be chosen because of the size constraints, select an X7R or X5R dielectric to minimize the variations of the capacitor's critical characteristics.

The resistors used in the circuits to drive the input and reference should be kept as low as possible to prevent excess thermal noise from degrading the system performance.

The digital outputs from the device should always be buffered. This will have a number of benefits: it reduces the loading of the internal digital buffers, which decreases noise generated within the device, and it also reduces device power consumption.

APPLICATIONS INFORMATION

Interfacing the ADS1601 to the TMS320 DSP family.

Since the ADS1601 communicates with the host via a serial interface, the most suitable method to connect to any of the TMS320 DSPs is via the multi-channel buffered serial port (McBSP). A typical connection to the TMS320 DSP is shown in Figure 51.

The McBSP provides a host of functions including:

- Full-duplex communication
- Double-buffered data registers
- Independent framing and clocking for reception and transmission of data

The sequence begins with a one-time synchronization of the serial port by the microprocessor. The ADS1601 recognizes the SYNC signal if it is high for at least one CLK period. Transfers are initiated by the ADS1601 after the SYNC signal is de-asserted by the microprocessor.

The FSO signal from the ADS1601 indicates that data is available to be read, and is connected to the frame sync receive (FSR) pin of the DSP. The clock receiver (CLKR) is derived directly from the ADS1601 serial clock output to ensure continued synchronization of data with the clock.

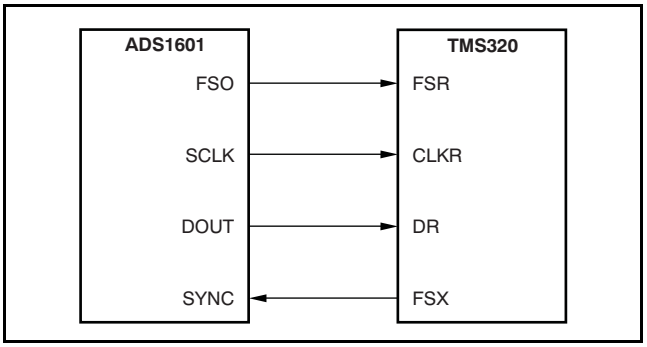


Figure 51. ADS1601—TMS320 Interface Connection

An evaluation module (EVM) is available from Texas Instruments. The module consists of the ADS1601 and supporting circuits, allowing users to quickly assess the performance and characteristics of the ADS1601. The EVM easily connects to various microcontrollers and DSP systems. For more details, or to download a copy of the ADS1601EVM User's Guide, visit the Texas Instruments web site at www.ti.com.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2010) to Revision D **Page**

- Added footnote 1 to Electrical Characteristics table 4

Changes from Revision B (September 2008) to Revision C **Page**

- Changed the *Timing Diagrams* section 8
- Added note to *Initializing the ADS1601* section 19
- Updated Figure 43 19

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS1601IPFBR	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1601I
ADS1601IPFBR.B	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1601I
ADS1601IPFBRG4	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1601I
ADS1601IPFBRG4.B	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1601I
ADS1601IPFBT	Active	Production	TQFP (PFB) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1601I
ADS1601IPFBT.B	Active	Production	TQFP (PFB) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1601I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

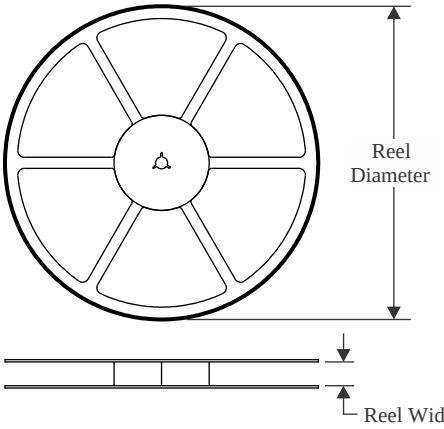
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

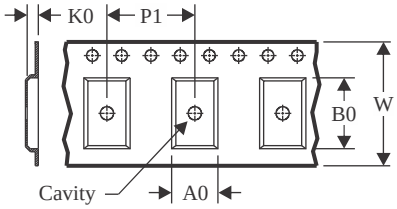
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

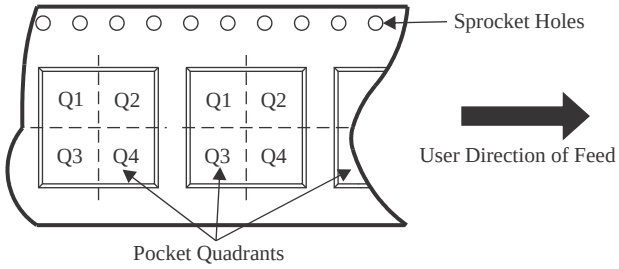


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

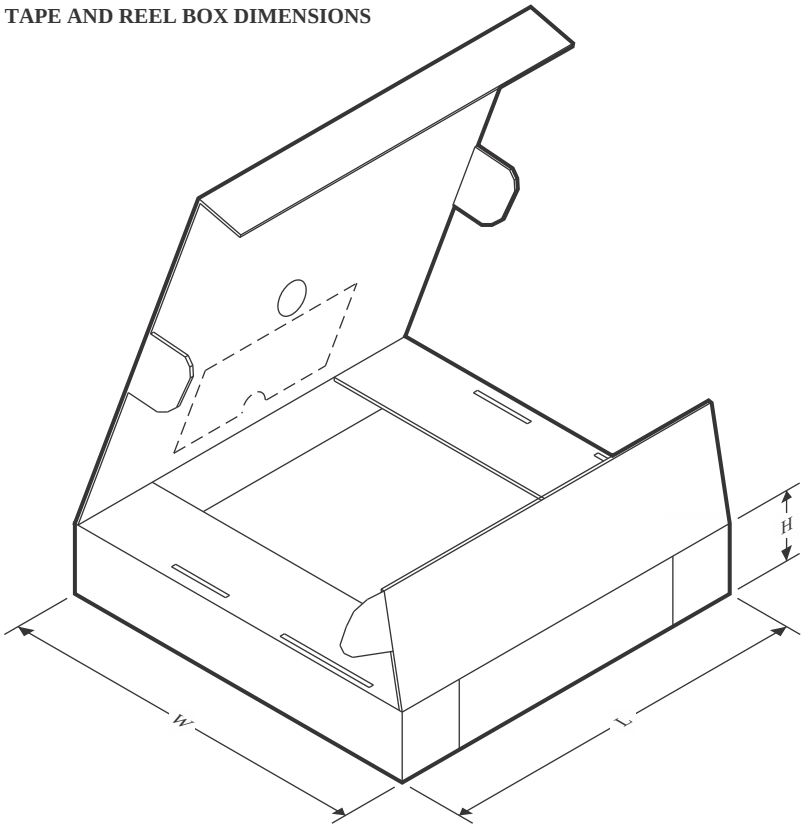
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1601IPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
ADS1601IPFBRG4	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

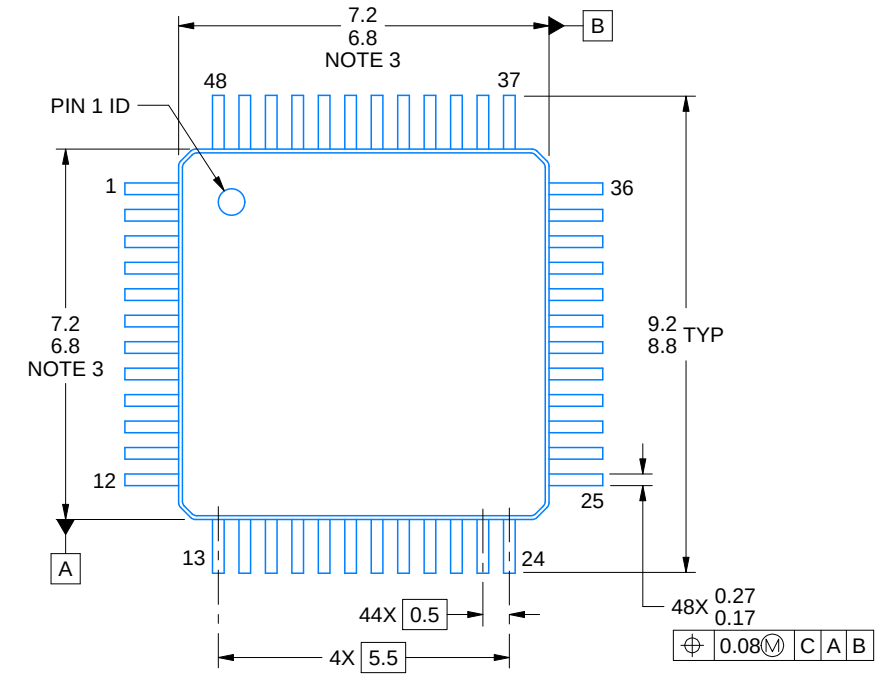
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1601IPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
ADS1601IPFBRG4	TQFP	PFB	48	1000	350.0	350.0	43.0

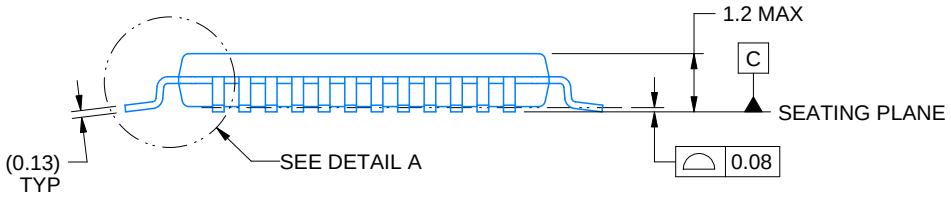
PACKAGE OUTLINE

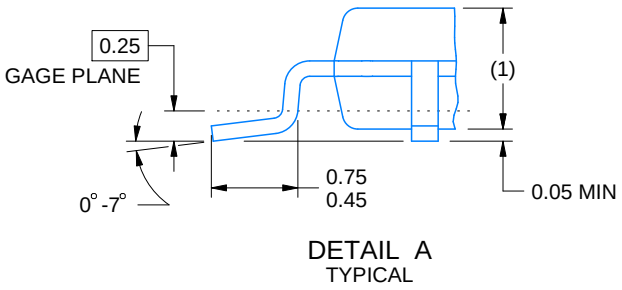
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK





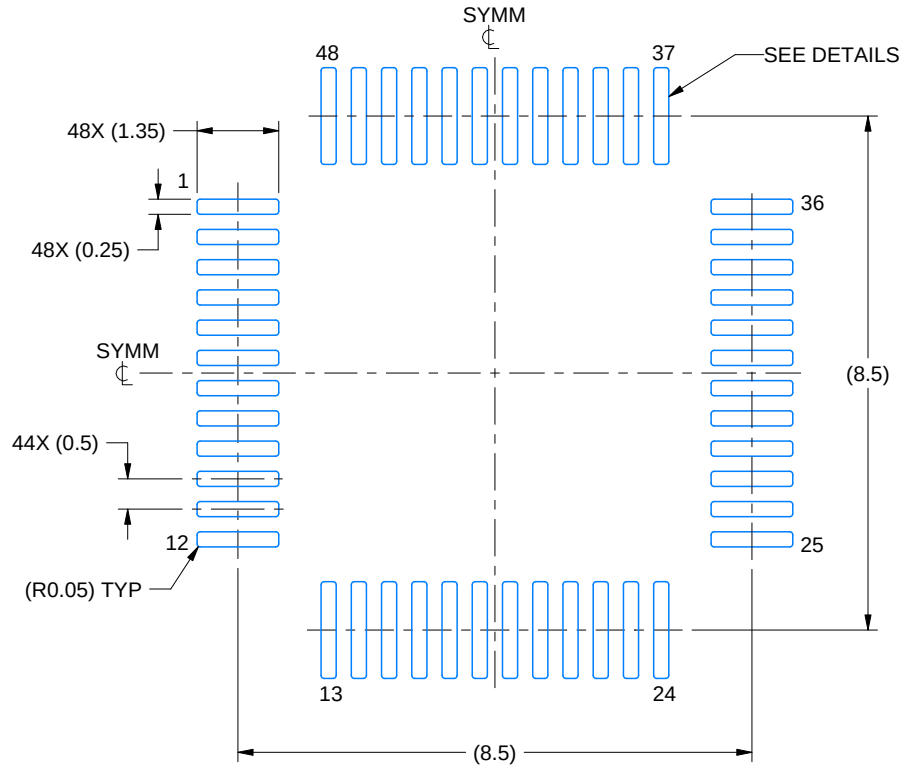


DETAIL A
TYPICAL

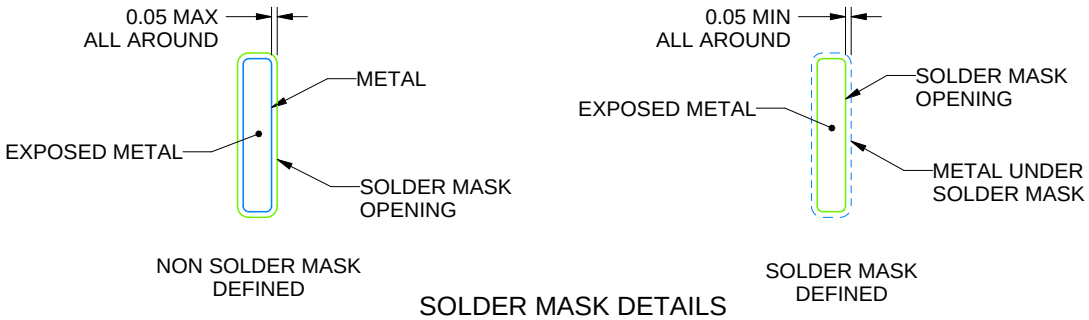
4215157/A 03/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

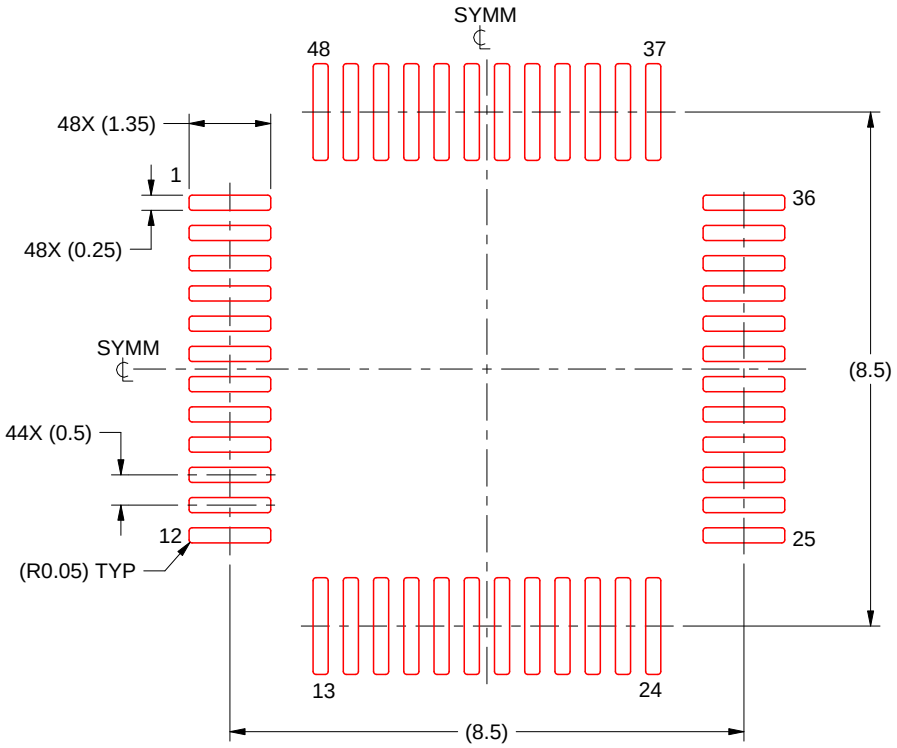


SOLDER MASK DETAILS

4215157/A 03/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

4215157/A 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025