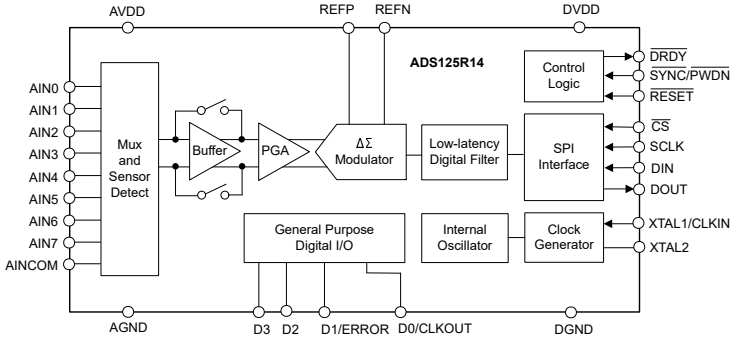
ADS125R1x 3, 6 and 9-Channel, 320kSPS, 24-Bit, ΔΣ ADCs With Input Buffer and PGA

1 Features

- Up to 26.0 bits of effective resolution
- Low noise PGA with gain 1 to 128
- Programmable data rate 2.5SPS to 320kSPS
- Input buffer range includes ground
- High Performance
  - Nonlinearity: 0.5ppm FSR (typical)
  - Offset drift: 10nV/°C (gain = 128, typical)
  - Gain drift: 0.5ppm/°C FSR (typical)
  - Noise: 11nV$_{RMS}$ (5SPS, gain = 128, typical)
- 320kSPS, 160kSPS, 80kSPS speed modes
- Autozero mode reduces offset error
- Available in 2mm x 2mm QFN package
- Input multiplexer with open-sensor detection
- One-shot conversions with single-cycle settling
- 35µs conversion time for fast channel scanning
- Internal, external or crystal clock options
- General purpose input/output pins
- Offset and gain calibration
- Analog power supply range: 2.85V to 5.5V
- Digital power supply range: 1.65V to 5.5V
- Fully specified from –40°C to +125°C

2 Applications

- Factory automation and control
  - Analog input module
- Test and measurement
  - Weigh scale
  - Battery formation and test
  - Analytical lab instrumentation
- Medical
  - Bio-chemistry analyzer



ADS125R14 Simplified Block Diagram

3 Description

The ADS125R11, ADS125R13 and ADS125R14 are high resolution, 24-bit, delta-sigma (ΔΣ), analog-to-digital converters with data rates up to 320kSPS with three, six and nine channels. The ADS125R11 and ADS125R14 are pin-to-pin performance upgrades to the ADS1255 and ADS1256 ADCs.

The ADS125R1x devices provide low offset and gain drift with low INL error. Autozero operation tracks offset error over time and temperature. Three speed modes optimize power consumption, sample rate, bandwidth and resolution for the application.

The ADCs are comprised of an input buffer, PGA, a delta-sigma modulator and a low latency digital filter. The flexible input multiplexer accepts single-ended and differential signals with integrated current sources for open-sensor detection. The input buffer reduces measurement error caused by signal loading of the sensor. The PGA provides gains up to x128 to increase measurement resolution.

The digital filter provides sample rates from 2.5SPS (for high resolution) to 320kSPS (for high throughput and high bandwidth applications). In the 320kSPS mode, eight channels of data are measured in less than 300µs with 16.9 bits effective resolution. The sinc3 filter provides greater than 100dB rejection of 50Hz and 60Hz interference signals.

The SPI-compatible interface supports 2-, 3- or 4-wire communication modes. The SPI CRC helps to verify error-free transmission of data. The register map CRC verifies register settings against unexpected changes. The general-purpose, input-input digital pins offer an output signal for error detection, and a clock output to synchronize other ADCs in multiple channel systems.

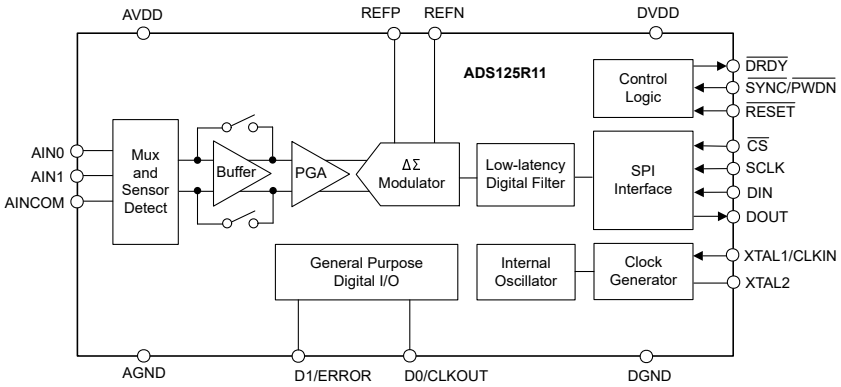
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS125R11	RUK (WQFN, 20)	3mm × 3mm
	DB (SSOP, 20)	7.2mm × 7.8mm
ADS125R13	RUC (X2QFN, 14)	2mm × 2mm
ADS125R14	RUY (WQFN, 28)	4mm × 4mm
	DB (SSOP, 28)	10.2mm × 7.8mm

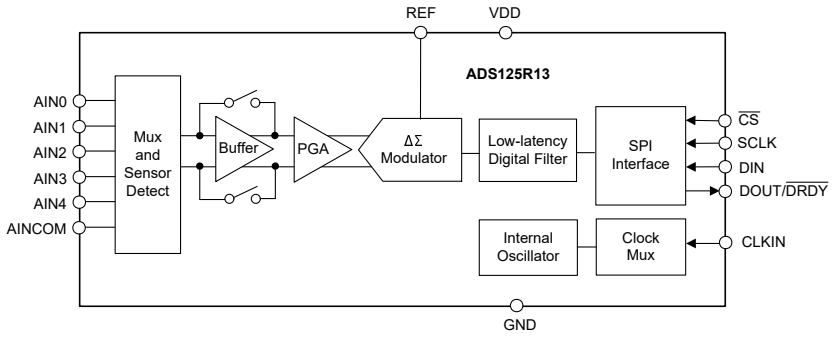
(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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ADS125R11 Simplified Block Diagram



ADS125R13 Simplified Block Diagram

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4 Device Comparison Table

DEVICE	ANALOG INPUTS	CLOCK SOURCES	GPIO PINS	SYNCHRONIZATION
ADS125R11	3	Internal, External, Crystal	2	Hardware, Software
ADS125R13	6	Internal, External	0	Software
ADS125R14	9	Internal, External, Crystal	4	Hardware, Software

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5 Pin Configuration and Functions

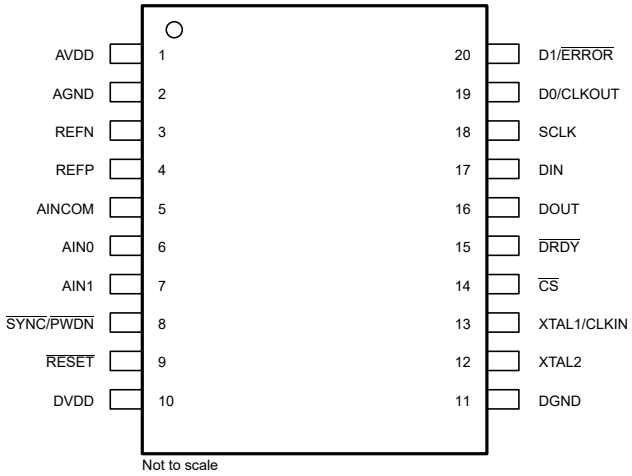


Figure 5-1. ADS125R11 DB Package, SSOP-20, Top View

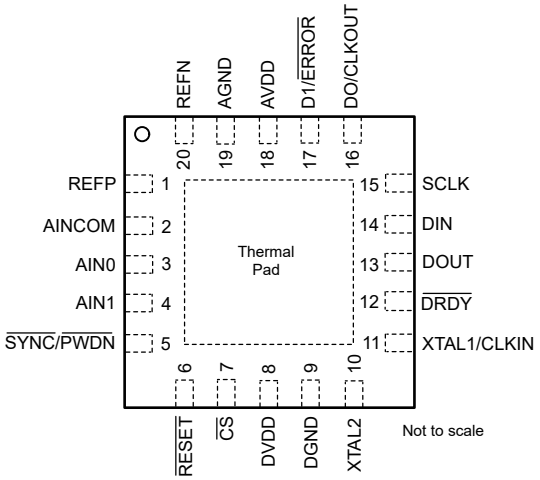


Figure 5-2. ADS125R11 RUK Package, WQFN-20, Top View

Table 5-1. ADS125R11 Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	SSOP	WQFN		
AGND	2	19	GND	Analog ground
AIN0	6	3	I	Analog input 0
AIN1	7	4	I	Analog input 1
AINCOM	5	2	I	Analog input common
AVDD	1	18	P	Analog power supply
$\overline{CS}$	14	7	I	Serial chip select, active low
D0/CLKOUT	19	16	I/O	Digital 0I/O / Clock signal output
D1/$\overline{ERROR}$	20	17	I/O	Digital 1I/O / Error output, active low
DGND	11	9	GND	Digital ground
DIN	17	14	I	Serial data input
DOUT	16	13	O	Serial data output
$\overline{DRDY}$	15	12	O	Data ready output, active low
DVDD	10	8	P	Digital power supply
REFN	3	20	I	Negative reference input
REFP	4	1	I	Positive reference input
$\overline{RESET}$	9	6	I	Reset input, active low
SCLK	18	15	I	Serial data clock input
$\overline{SYNC}$/PWDN	8	5	I	Synchronization / Power-down input, active low
XTAL1/CLKIN	13	11	I	Crystal oscillator connection / clock signal input
XTAL2	12	10	O	Crystal oscillator connection
Thermal Pad	—	Pad	GND	Thermal power pad; connect to AGND

1. I = input, O = output, P = power, GND = ground, N/A = not applicable

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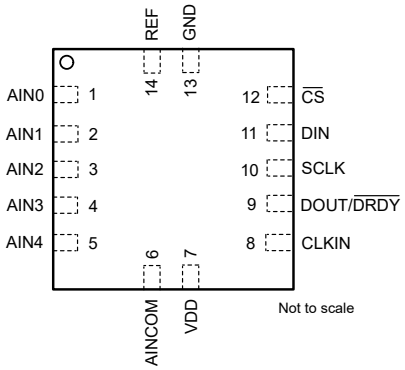


Figure 5-3. ADS125R13 RUC Package, X2QFN-14(Top View)

Table 5-2. ADS125R13 Pin Functions

PIN		TYPE [1]	DESCRIPTION
NAME	X2QFN		
AIN0	1	I	Analog input 0
AIN1	2	I	Analog input 1
AIN2	3	I	Analog input 2
AIN3	4	I	Analog input 3
AIN4	5	I	Analog input 4
AINCOM	6	I	Analog input common
CLKIN	8	I	Clock signal input
$\overline{CS}$	12	I	Serial chip select, active low
GND	13	GND	ADC ground
DIN	11	I	Serial data input
DOUT/$\overline{DRDY}$	9	O	Serial data output / Data ready output, active low
REF	14	I	Reference input
SCLK	10	I	Serial data clock input
VDD	7	P	Analog and digital power supply

1. I = input, O = output, P = power, GND = ground, N/A = not applicable

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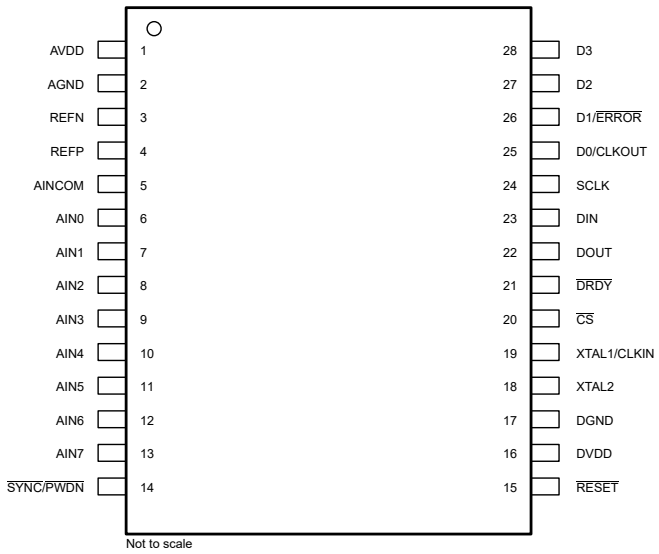


Figure 5-4. ADS125R14 DB Package, SSOP-28 (Top View)

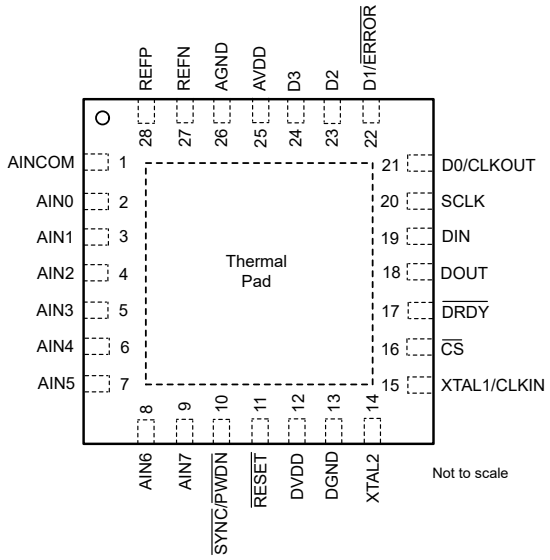


Figure 5-5. ADS125R14 RUY Package,WQFN-28(Top View)

Table 5-3. ADS125R14 Pin Functions

PIN			TYPE (1)	DESCRIPTION
NAME	SSOP	WQFN		
AGND	2	26	GND	Analog ground
AIN0	6	2	I	Analog input 0
AIN1	7	3	I	Analog input 1
AIN2	8	4	I	Analog input 2
AIN3	9	5	I	Analog input 3
AIN4	10	6	I	Analog input 4
AIN5	11	7	I	Analog input 5
AIN6	12	8	I	Analog input 6
AIN7	13	9	I	Analog input 7
AINCOM	5	1	I	Analog input common
AVDD	1	25	P	Analog power supply
$\overline{CS}$	20	16	I	Serial chip select, active low
D0/CLKOUT	25	21	I/O	Digital 0I/O / Clock signal output
D1/$\overline{ERROR}$	26	22	I/O	Digital 1I/O / Error output, active low
D2	27	23	I/O	Digital 2I/O
D3	28	24	I/O	Digital 3I/O
DGND	17	13	GND	Digital ground
DIN	23	19	I	Serial data input
DOUT	22	18	O	Serial data output
$\overline{DRDY}$	21	17	O	Data ready output, active low
DVDD	16	12	P	Digital power supply
REFN	3	27	I	Negative reference input
REFP	4	28	I	Positive reference input
$\overline{RESET}$	15	11	I	Reset input, active low
SCLK	24	20	I	Serial data clock input
$\overline{SYNC}$/PWDN	14	10	I	Synchronization / Power-down input, active low

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Table 5-3. ADS125R14 Pin Functions (continued)

PIN			TYPE [1]	DESCRIPTION
NAME	SSOP	WQFN		
XTAL1/CLKIN	19	15	I	Crystal oscillator connection / clock signal input
XTAL2	18	14	O	Crystal oscillator connection
Thermal Pad	—	Pad	GND	Thermal power pad; connect to AGND

1. I = input, O = output, P = power, GND = ground, N/A = not applicable

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AGND	–0.3	6.5	V
	DVDD to DGND	–0.3	6.5	
	(ADS125R13 VDD to GND))	–0.3	6.5	
	AGND to DGND	–0.3	0.3	
Analog input voltage	AIN(x), AINCOM, REFP, REFN	AGND – 0.3	AVDD + 0.3	V
	(ADS125R13 AIN(x), AINCOM, REF)	GND – 0.3	VDD + 0.3	V
Digital input/output voltage	XTAL2, $\overline{\text{DRDY}}$, DOUT, D0/CLKOUT, D1/$\overline{\text{ERROR}}$, D2, D3	DGND – 0.3	DVDD + 0.3	V
	(ADS125R13 DOUT/$\overline{\text{DRDY}}$)	GND – 0.3	VDD + 0.3	V
	$\overline{\text{SYNC}}$/$\overline{\text{PWDN}}$, $\overline{\text{CS}}$, XTAL1/CLKIN, DIN, SCLK, $\overline{\text{RESET}}$	DGND – 0.3	6.5	
	(ADS125R13 $\overline{\text{CS}}$, CLKIN, DIN, SCLK)	GND – 0.3	6.5	
Input current	Continuous, any pin except power-supply pins(2)	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional – this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Analog input pins AIN(x), AINCOM, REFP, and REFN are diode-clamped to analog supply and ground. Limit the input current to 10mA in the event the input voltage exceeds AVDD (VDD for ADS125R13) by more than 0.3V or AGND (GND for ADS125R13) by less than –0.3V. Digital pins XTAL2, $\overline{\text{DRDY}}$, DOUT, D0/CLKOUT, D1/$\overline{\text{ERROR}}$, D2, D3 and DOUT/$\overline{\text{DRDY}}$ are diode-clamped to DVDD and DGND (VDD and GND for ADS125R13). Digital pins $\overline{\text{SYNC}}$/$\overline{\text{PWDN}}$, $\overline{\text{CS}}$, XTAL1/CLKIN, DIN, SCLK and $\overline{\text{RESET}}$ are diode-clamped to DGND only (GND for ADS125R13). Limit the input current to 10mA in the event the input voltage exceeds the digital power supply by more 0.3V (for effected pins) or exceeds digital ground by less than –0.3V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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6.3 ADS125R11 and ADS125R14 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted).

				MIN	NOM	MAX	UNIT
POWER SUPPLY							
	AVDD analog power supply	AVDD to AGND	Low-speed and mid-speed modes	2.85		5.5	V
			High-speed mode	3		5.5	
			High-speed mode, Buffer off, Gain ≥ 16	4.5		5.5	
	DVDD digital power supply	DVDD to DGND		1.65		5.5	V
ANALOG INPUTS							
V_{IN}	Differential input voltage $V_{IN} = V_{AIN(x)} – V_{AIN(y)}$			$–2V_{REF}$/Gain		$2V_{REF}$/Gain	V
$V_{AIN(x)}$, V_{AINCOM}	Absolute input voltage	Buffer off		AGND – 0.1		AVDD + 0.1	V
		Buffer on		AGND – 0.05		AVDD – 1.45	
VOLTAGE REFERENCE INPUTS							
V_{REF}	Reference voltage ($V_{REF} = V_{REFP} – V_{REFN}$)			0.5	2.5	AVDD	V
V_{REFN}	Negative reference voltage	Buffer off		AGND – 0.1		V_{REFP} – 0.5	V
		Buffer on		AGND		V_{REFP} – 0.5	
V_{REFP}	Positive reference voltage	Buffer off		V_{REFN} + 0.5		AVDD + 0.1	V
		Buffer on		V_{REFN} + 0.5		AVDD + 0.1	
		Buffer on with self-calibration or gain self-calibration		V_{REFN} + 0.5		AVDD – 1.45	
CLOCK FREQUENCY							
f_{CLKIN}	External clock signal applied to CLKIN			0.1	7.68	8.4	MHz
	CLKIN duty cycle			45%		55%	
f_{XTAL}	External crystal between XTAL1 and XTAL2			2	7.68	8.4	MHz
f_{MOD}	Modulator clock frequency	High-speed mode		0.1	3.84	4.2	MHz
		Mid-speed mode		0.05	1.92	2.1	
		Low-speed mode		0.025	0.96	1.05	
DIGITAL INPUTS							
	Input voltage			DGND		DVDD	V
TEMPERATURE RANGE							
T_A	Ambient temperature	Operational		–45		125	°C
		Specification		–40		125	

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6.4 ADS125R13 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted).

				MIN	NOM	MAX	UNIT
POWER SUPPLY							
	VDD power supply	VDD to GND	Low-speed and mid-speed modes	2.85		5.5	V
			High-speed mode	3		5.5	
			High-speed mode, buffer off, gain ≥ 16	4.5		5.5	
ANALOG INPUTS							
V_{IN}	Differential input voltage $V_{IN} = V_{AIN(x)} – V_{AIN(y)}$			$–2V_{REF}$/Gain		$2V_{REF}$/Gain	V
$V_{AIN(x)}$, V_{AINCOM}	Absolute input voltage	Buffer off		GND – 0.1		VDD + 0.1	V
		Buffer on		GND – 0.05		VDD – 1.45	
VOLTAGE REFERENCE INPUTS							
V_{REF}	Reference voltage (V_{REF} – GND)	Buffer off		0.5		VDD	V
		Buffer on		0.5		VDD	
		Buffer on with self-calibration or gain self-calibration		0.5		VDD – 1.45	
CLOCK FREQUENCY							
f_{CLKIN}	External clock signal applied to CLKIN			0.1	7.68	8.4	MHz
f_{MOD}	Modulator clock frequency	High-speed mode		0.1	3.84	4.2	MHz
		Mid-speed mode		0.05	1.92	2.1	
		Low-speed mode		0.025	0.96	1.05	
DIGITAL INPUTS							
	Input voltage			GND		VDD	V
TEMPERATURE RANGE							
T_A	Ambient temperature	Operational		–45		125	°C
		Specification		–40		125	

6.5 Thermal Information

THERMAL METRIC[1]		ADS125R11		ADS125R13	ADS125R14		UNIT
		WQFN (RUK)	SSOP (DB)	X2QFN (RUC)	WQFN (RUY)	SSOP (DB)	
		20 PINS	20 PINS	14 PINS	28 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	81.5	TBD	TBD	70.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	47.1	TBD	TBD	39.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	46.5	TBD	TBD	41.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	11.6	TBD	TBD	9.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	46.4	TBD	TBD	41.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	NA	TBD	TBD	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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6.6 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications at T_A = 25°C; all specifications at AVDD = 5V, DVDD = 1.8V, VDD = 5V (ADS125R13), f_{CLKIN} = 7.68MHz,OSR = 64, Gain = 1, Buffer on, Autozero off, V_{IN} = 0V, V_{CM} = 2.5V, V_{REF} = 2.5V, all speed modes (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL CHARACTERISTICS						
	No missing code resolution	OSR ≥ 64	24			Bits
	PGA gain	V_{IN} = ±2V_{REF}/Gain		1, 2, 4, 8, 16, 32, 64, 128		V/V
e_n	Noise			See the Noise Performance section for details		
	Crystal oscillator start-up time			2		ms
f_{OSC}	Internal oscillator frequency		TBD	7.68	TBD	MHz
I_{SDCS}	Sensor detect current sources			Off, 0.5, 2, 10		µA
NMRR	Normal-mode rejection ratio	f_{IN} = 50Hz (±1Hz), f_{DATA} = 50SPS, sinc3 filter	101			dB
		f_{IN} = 60Hz (±1Hz), f_{DATA} = 60SPS, sinc3 filter	106			
		f_{IN} = 400Hz (±8Hz), f_{DATA} = 400SPS, sinc3 filter	101			
HIGH-SPEED MODE CHARACTERISTICS						
f_{DATA}	Data rate	f_{MOD} = 3.84MHz	5		320,000	SPS
Z_{IN}	Differential input impedance	Buffer off, gain = 1, 2, 4, 8, 16		80/gain		kΩ
		Buffer off, gain = 32, 64, 128		1.5		
		Buffer on, f_{DATA} ≤ 7.5kSPS		375		MΩ
I_b	Input bias current	Buffer on		0.1		nA
Z_{REF}	Voltage reference impedance			25		kΩ
INL	Integral nonlinearity(1)	All gains		0.5	TBD	ppm FSR
Vos	Offset error(2)	T_A = 25°C	–TBD	±250/gain + 10	TBD	µV
		Autozero mode, all gains	–TBD	±2	TBD	
dVos/dT	Offset drift			120/gain + 10	TBD	nV/°C
		Autozero mode, all gains		18	TBD	
GE	Gain error(2)	T_A = 25°C, all gains	–TBD	±400	TBD	ppm FSR
dGE/dT	Gain error drift	All gains		0.5	TBD	ppm/°C
THD	Total harmonic distortion(1)	All gains, f_{IN} = 1kHz, f_{DATA} = 30kSPS		-115	TBD	dB
CMRR	Common-mode rejection ratio	Buffer on, 50Hz or 60Hz	TBD	129		dB
		Buffer on, up to 10kHz		123		
		Buffer off, 50Hz or 60Hz	TBD	128		
PSRR	Power-supply rejection ratio	AVDD 10% Δdc	TBD	115		dB
		DVDD, 8% Δdc	TBD	105		
		VDD, 10% Δdc (ADS125R13)	TBD	100		
MID-SPEED MODE CHARACTERISTICS						
f_{DATA}	Data rate	f_{MOD} = 1.92MHz	2.5		160,000	SPS
Z_{IN}	Differential input impedance	Buffer off, gain = 1, 2, 4, 8, 16		160/gain		kΩ
		Buffer off, gain = 32, 64, 128		3.2		
		Buffer on, f_{DATA} ≤ 7.5kSPS		375		MΩ
I_b	Input bias current	Buffer on		0.1		nA
Z_{REF}	Voltage reference impedance			42		kΩ
INL	Integral nonlinearity(1)	All gains		0.5	TBD	ppm FSR
Vos	Offset error(2)	T_A = 25°C	–TBD	±250/gain + 10	TBD	µV
		Autozero mode, all gains	–TBD	±0.5	TBD	
dVos/dT	Offset drift			120/gain + 10	TBD	nV/°C
		Autozero mode, all gains		10	TBD	
GE	Gain error(2)	T_A = 25°C, all gains	–TBD	±400	TBD	ppm FSR
dGE/dT	Gain error drift	All gains		0.5	TBD	ppm/°C
THD	Total harmonic distortion(1)	All gains, f_{IN} = 1kHz, f_{DATA} = 30kSPS		-115	TBD	dB

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minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications at T_A = 25°C; all specifications at AVDD = 5V, DVDD = 1.8V, VDD = 5V (ADS125R13), f_{CLKIN} = 7.68MHz,OSR = 64, Gain = 1, Buffer on, Autozero off, V_{IN} = 0V, V_{CM} = 2.5V, V_{REF} = 2.5V, all speed modes (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	Buffer on, 50Hz or 60Hz	TBD	128		dB
		Buffer on, up to 10kHz		127		
		Buffer off, 50Hz or 60Hz	TBD	126		
PSRR	Power-supply rejection ratio	AVDD, 10% Δdc	TBD	110		dB
		DVDD, 8% Δdc	TBD	105		
		VDD, 10% Δdc (ADS125R13)	TBD	100		
LOW-SPEED MODE CHARACTERISTICS						
f_{DATA}	Data rate	f_{MOD} = 0.96MHz	1.25		80,000	SPS
Z_{IN}	Differential input impedance	Buffer off, gain = 1, 2, 4, 8, 16		320/gain		kΩ
		Buffer off, gain = 32, 64, 128		6.5		
		Buffer on, f_{DATA} ≤ 7.5kSPS		375		MΩ
I_b	Input bias current	Buffer on		0.1		nA
Z_{REF}	Voltage reference impedance			66		kΩ
INL	Integral nonlinearity(1)	All gains		0.5	TBD	ppm FSR
V_{OS}	Offset error(2)	T_A = 25°C	–TBD	±250/gain + 10	TBD	µV
		Autozero mode, all gains	–TBD	±0.5	TBD	
dVos/dT	Offset error drift			120/gain + 10	TBD	nV/°C
		Autozero mode, all gains		5	TBD	
GE	Gain error(2)	T_A = 25°C, all gains	–TBD	±400	TBD	ppm FSR
dGE/dT	Gain error drift	All gains		0.5	TBD	ppm/°C
THD	Total harmonic distortion(1)	All gains, f_{IN} = 1kHz, f_{DATA} = 30kSPS		-115	TBD	dB
CMRR	Common-mode rejection ratio	Buffer on, 50Hz or 60Hz	TBD	126		dB
		Buffer on, up to 10kHz		110		
		Buffer off, 50Hz or 60Hz	TBD	124		
PSRR	Power-supply rejection ratio	AVDD, 10% Δdc	TBD	105		dB
		DVDD, 8% Δdc	TBD	105		
		VDD, 10% Δdc (ADS125R13)	TBD	100		
DIGITAL INPUTS/OUTPUTS						
V_{IL}	Logic-low input threshold(3)				0.3 · DVDD	V
V_{IH}	Logic-high input threshold		0.7 · DVDD			V
	Input hysteresis			150		mV
	Input current		–1		1	µA
V_{OL}	Logic-low output voltage	I_{OL} = 1mA			0.2 · DVDD	V
		I_{OL} = 5mA, DVDD = 3.3V			0.2 · DVDD	
V_{OH}	Logic-high output voltage	I_{OH} = –1mA	0.8 · DVDD			V
		I_{OH} = –5mA, DVDD = 3.3V	0.8 · DVDD			

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minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications at T_A = 25°C; all specifications at AVDD = 5V, DVDD = 1.8V, VDD = 5V (ADS125R13), f_{CLKIN} = 7.68MHz,OSR = 64, Gain = 1, Buffer on, Autozero off, V_{IN} = 0V, V_{CM} = 2.5V, V_{REF} = 2.5V, all speed modes (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SUPPLY CURRENT							
I_{AVDD}	AVDD Current(3)	High-speed mode	Buffer off, gain = 1		1.5	TBD	mA
			Buffer off, gain = 128		3.2	TBD	
			Buffer on, gain = 1		7.8	TBD	
			Buffer on, gain = 128		17	TBD	
		Mid-speed mode	Buffer off, gain = 1		0.72	TBD	mA
			Buffer off, gain = 128		1.5	TBD	
			Buffer on, gain = 1		3.5	TBD	
			Buffer on, gain = 128		7.4	TBD	
		Low-speed mode	Buffer off, gain = 1		0.45	TBD	mA
			Buffer off, gain = 128		0.78	TBD	
			Buffer on, gain = 1		2.2	TBD	
			Buffer on, gain = 128		3.7	TBD	
		Standby mode			10		µA
		Power-down mode			5		µA
DIGITAL SUPPLY CURRENT							
I_{DVDD}	DVDD current(3)	High-speed mode	CLKOUT off, OSR = 64, DVDD = 3.3V		0.23	TBD	mA
		Mid-speed mode			0.16	TBD	
		Low-speed mode			0.13	TBD	
		Standby mode	External clock, DVDD = 3.3V		35		µA
			Internal oscillator, DVDD = 3.3V		45		
		Power-down mode	DVDD = 3.3V		1		µA
POWER DISSIPATION							
P_D	Power dissipation	High-speed mode, DVDD = 3.3V	Buffer off, gain = 1		8.3	TBD	mW
			Buffer off, gain = 128		17	TBD	
			Buffer on, gain = 1		40	TBD	
			Buffer on, gain = 128		86	TBD	
		Mid-speed mode, DVDD = 3.3V	Buffer off, gain = 1		4.1	TBD	mW
			Buffer off, gain = 128		8.0	TBD	
			Buffer on, gain = 1		18	TBD	
			Buffer on, gain = 128		38	TBD	
		Low-speed mode, DVDD = 3.3V	Buffer off, gain = 1		2.7	TBD	mW
			Buffer off, gain = 128		4.3	TBD	
			Buffer on, gain = 1		12	TBD	
			Buffer on, gain = 128		19	TBD	
		Standby mode	External clock, DVDD = 3.3V		0.17	TBD	mW
		Power-down mode	DVDD = 3.3V		0.03	TBD	mW

(1) INL and THD tested with 95% full-scale differential signal. Buffer on, gain = 1 test condition: V_{CM} = 1.25V and V_{REF} = 1.25V. Buffer on, gain = 2 test condition: V_{CM} = 1.25V and V_{REF} = 2.5V. INL tested by the best-fit method.
(2) Offset and gain calibration reduces these errors to the level of noise.
(3) ADS125R13 uses a single pin (VDD) for analog and digital power supplies. VDD power supply current is the sum of AVDD and DVDD power supply currents. DVDD current measured with SPI transfer present.

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6.7 Timing Requirements

Over operating ambient temperature range. DVDD = 1.65V to 5.5V (ADS125R13 = 2.85V to 5.5V). Input signals rise and fall time = 5ns and timed from a voltage level = DVDD / 2, unless otherwise noted.

		MIN	MAX	UNIT
SERIAL INTERFACE				
$t_{c(SC)}$	SCLK period	40		ns
			10	t_{DATA}
$t_{w(SCH)}$	Pulse duration, SCLK high	15		ns
			9	t_{DATA}
$t_{w(SCL)}$	Pulse duration, SCLK low	15		ns
$t_{d(CSSC)}$	Delay time, $\overline{CS}$ low to first SCLK	5		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge	5		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	10		ns
$t_{d(SC)}$	Delay time, last SCLK for DIN to first SCLK for DOUT (RDATA, RDATAC, RREG response)	15		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ high after final SCLK falling edge	15		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	20		ns
$t_{d(COM)}$	Delay time, final SCLK falling edge of command to first SCLK rising edge of next command			
	RREG, WREG, RDATA, RDATAC, $\overline{SYNC}$	15		ns
	RDATAC, $\overline{RESET}$, STANDBY, SELFOCAL, SYSOCAL, SELFGCAL, SYSGCAL, SELFCAL	Wait for $\overline{DRDY}$ to go low		
$\overline{RESET}$				
$t_{w(RSL)}$	Pulse duration, $\overline{RESET}$ low	4		t_{CLKIN} or t_{OSC}
$\overline{SYNC}$/$\overline{PWDN}$				
$t_{w(SPL)}$	Pulse duration, $\overline{SYNC}$/$\overline{PWDN}$ low for synchronization	4		t_{CLKIN} or t_{OSC}
	Pulse duration, $\overline{SYNC}$/$\overline{PWDN}$ low for power-down mode	20		t_{DATA}
$t_{su(SPCLK)}$	Setup time, $\overline{SYNC}$/$\overline{PWDN}$ rising edge before CLKIN falling edge(1)	5		ns
$t_{h(SPCLK)}$	Hold time, $\overline{SYNC}$/$\overline{PWDN}$ rising edge after CLKIN falling edge(1)	15		ns

(1) Apply $\overline{SYNC}$/$\overline{PWDN}$ rising edge outside of the window defined by the setup and hold times to avoid one CLKIN cycle of uncertainty.

6.8 Switching Characteristics

Over operating ambient temperature range and C_{LOAD} = 20pF. DVDD = 1.65V to 5.5V (ADS125R13 = 2.85V to 5.5V). Input signals rise and fall time = 5ns and timed from a voltage level = DVDD / 2, unless otherwise noted.

PARAMETER		MODEL	MIN	TYP	MAX	UNIT
SERIAL INTERFACE						
$t_{p(DO)}$	Propagation delay time, SCLK rising edge to valid data output	All			16	ns
$t_{h(DO)}$	Hold time, SCLK rising edge to invalid data output	All	3			ns
$t_{p(DOZ)}$	Propagation delay time, last SCLK falling edge to DOUT Hi-Z	ADS125R11, ADS125R14	6		10	t_{CLKIN} or t_{OSC}
$t_{p(CSDR)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT/$\overline{DRDY}$ driven	ADS125R13 only			15	ns
$t_{p(SCDR)}$	Propagation delay time, last SCLK falling edge to change DOUT/$\overline{DRDY}$ pin function from DOUT to $\overline{DRDY}$ mode	ADS125R13 only	20		40	ns
$t_{p(DOZ)}$	Propagation delay time, $\overline{CS}$ high to DOUT/$\overline{DRDY}$ Hi-Z	ADS125R13 only			15	ns
$\overline{DRDY}$ and DOUT/$\overline{DRDY}$						
$t_{p(RSDRH)}$	Propagation delay time, $\overline{DRDY}$ or DOUT/$\overline{DRDY}$ high after reset	All, external clock		212		µs
		All, internal clock		178		µs
$t_{p(DRL)}$	Propagation delay time, $\overline{DRDY}$ or DOUT/$\overline{DRDY}$ low (first conversion)	All			212	µs
$t_{w(DRH)}$	Pulse Duration, $\overline{DRDY}$ or DOUT/$\overline{DRDY}$ high with no data retrieval	All	5			$1/f_{MOD}$

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7 Timing Diagrams

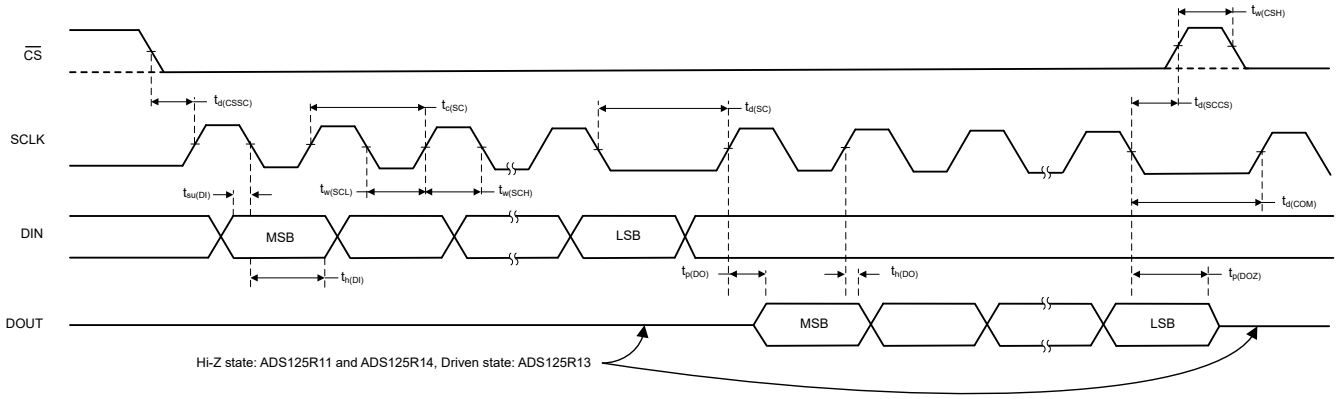


Figure 7-1. Serial Interface Read/Write Timing

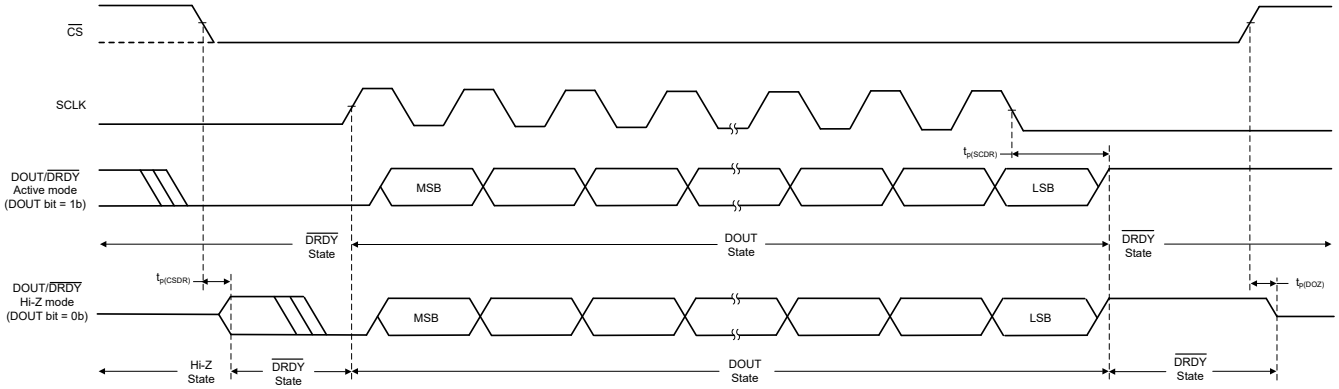


Figure 7-2. ADS125R13 Conversion Data Read Timing

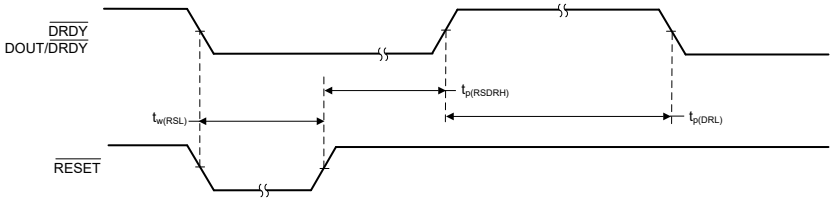


Figure 7-3. RESET Pin to DRDY Timing

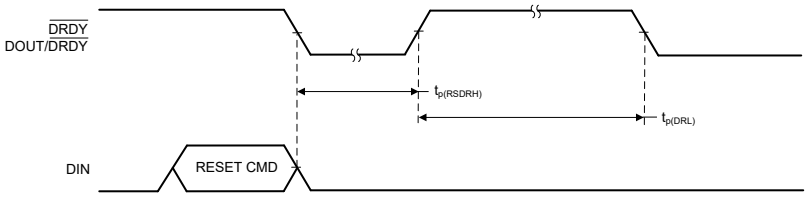


Figure 7-4. Reset Command to DRDY Timing

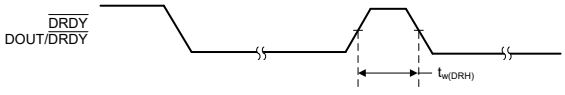


Figure 7-5. DRDY Timing (no data retrieval)

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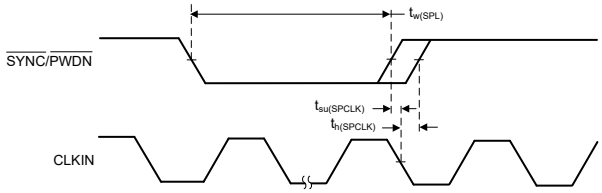


Figure 7-6. SYNC/PWDN Timing

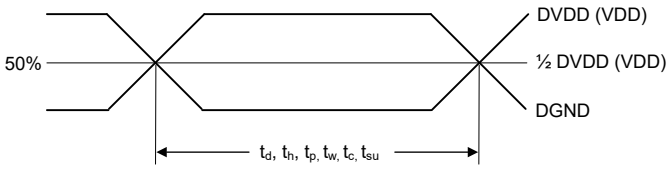


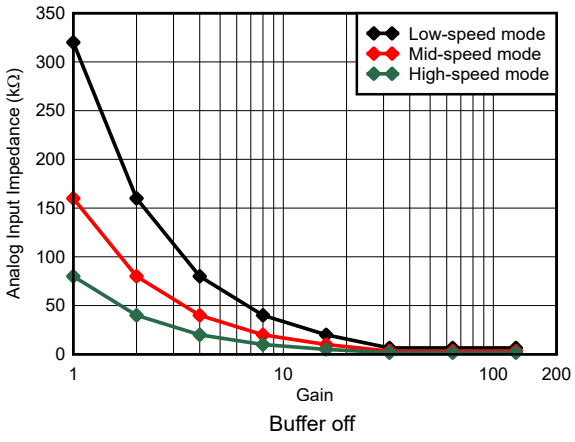
Figure 7-7. Timing Reference

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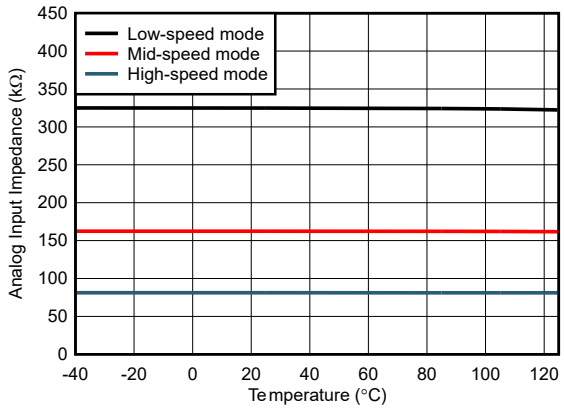
8 Typical Characteristics

AVDD = 5V, DVDD = 1.8V, VDD = 5V (ADS125R13), V_{REF} = 2.5V, Gain = 1, Buffer on, V_{IN} = 0V, V_{CM} = 2.5V, f_{DATA} = 30kSPS, and T_A = 25°C (unless otherwise noted)



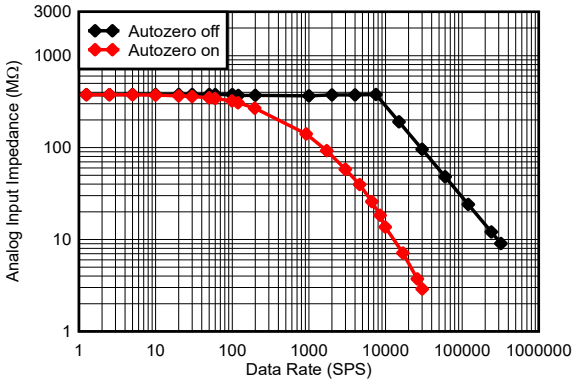
Buffer off

Figure 8-1. Analog Input Impedance vs Gain



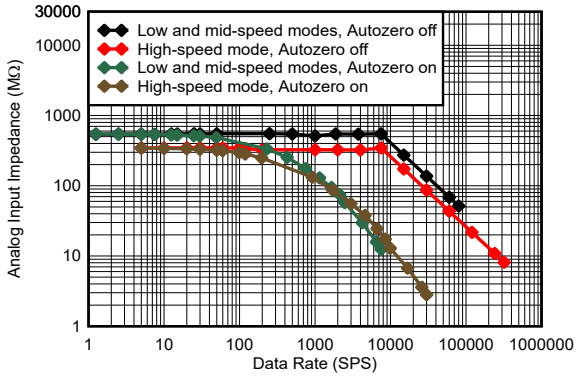
Buffer off, Gain = 1

Figure 8-2. Analog Input Impedance vs Temperature



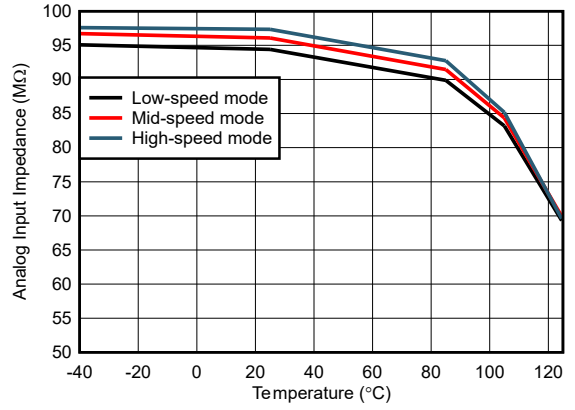
All speed modes, Buffer on, Gain ≤ 8

Figure 8-3. Analog Input Impedance vs Data Rate



Buffer on, Gain ≥ 16

Figure 8-4. Analog Input Impedance vs Data Rate



Buffer on, Gain = 1, 30kSPS

Figure 8-5. Analog Input Impedance vs Temperature

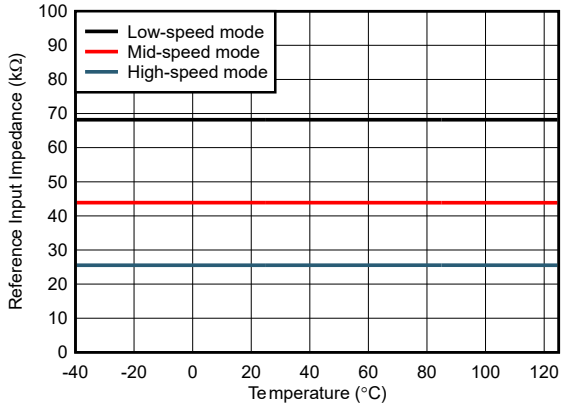


Figure 8-6. Reference Input Impedance vs Temperature

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8 Typical Characteristics (continued)

AVDD = 5V, DVDD = 1.8V, VDD = 5V (ADS125R13), V_{REF} = 2.5V, Gain = 1, Buffer on, V_{IN} = 0V, V_{CM} = 2.5V, f_{DATA} = 30kSPS, and T_A = 25°C (unless otherwise noted)

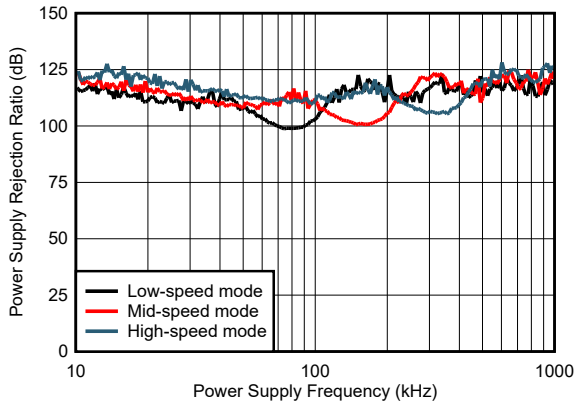


Figure 8-7. DVDD PSRR vs Power Supply Frequency

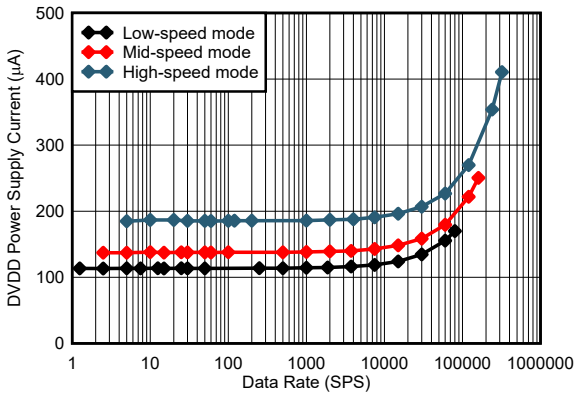


Figure 8-8. DVDD Current vs Data Rate

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9 Parameter Measurement Information

9.1 Detailed Measurements

The following sections detail the measurement of device parameters.

9.1.1 Offset and Gain Error

Offset error is measured with an external short between two analog input pins. The shorted input connection is tied to AGND. Gain error of the ADC is the difference between the actual and the ideal ADC transfer functions. Any error present in the reference voltage is not included in the gain error measurement. Equation 1 shows the calculation of gain error.

$$\text{Gain Error (ppm FSR)} = 10^6 \cdot (\Delta V_{OUT} – (\Delta V_{IN} \cdot \text{Gain})) / (\Delta V_{IN} \cdot \text{Gain}) \quad (1)$$

where:

- ΔV_{OUT} = Difference of two ADC output voltages
- ΔV_{IN} = Difference of two input voltages: $0.95 \cdot 2V_{REF}/\text{Gain}$ and $–0.95 \cdot 2V_{REF}/\text{Gain}$. V_{REF} = 2.5V.

9.1.2 Offset and Gain Drift Measurement

Offset and gain drift is defined as the change of error measured at multiple points over the specified temperature range. The box method is used in which a box is formed over the maximum and minimum errors over the specified temperature range. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. Equation 2 describes drift using the box method.

$$\text{Offset or Gain Drift } (d\alpha/dT) = (\alpha_{MAX} – \alpha_{MIN}) / (T_{MAX} – T_{MIN}) \quad (2)$$

where:

- α_{MAX} and α_{MIN} = Maximum and minimum offset or gain errors over the specified temperature range
- T_{MAX} and T_{MIN} = Maximum and minimum temperatures

9.1.3 NMRR

Normal-mode rejection ratio (NMRR) specifies the rejection of normal-mode input signals at 50Hz, 60Hz and 400Hz.

9.1.4 CMRR

Common-mode rejection ratio (CMRR) specifies the rejection of common-mode input signals. For DC CMRR, two common-mode voltages are applied at AGND + 50mV and AVDD – 50mV (buffer off) or AVDD – 1.5V (buffer on). For the ADS125R13, the test voltages are referenced to GND and VDD. As shown in Equation 3, the change in offset voltage versus the change in common-mode voltage determines DC CMRR.

$$\text{DC CMRR (dB)} = 20 \cdot \log(\Delta V_{CM} / \Delta V_{OS}) \quad (3)$$

where:

- ΔV_{CM} = Change of common-mode test voltage
- ΔV_{OS} = Change of offset voltage

For AC CMRR, an ac common-mode voltage is applied over the specified frequency range with V_{CM} = mid power supply (buffer off) or V_{CM} = 1.75V (buffer on). As shown in Equation 4, the nine largest amplitude in the FFT spectrum are summed as powers and scaled to the amplitude of the test signal.

$$\text{AC CMRR (dB)} = 20 \cdot \log(V_{CM} / V_O) \quad (4)$$

where:

- V_{CM} (RMS) = AC common-mode input signal amplitude
- V_O (RMS) = Root-sum-square amplitude at spurious frequencies = $\sqrt{(V_0^2 + V_1^2 + ...V_8^2)}$

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9.1.5 PSRR

Power-supply rejection ratio (PSRR) specifies the rejection of power supply disturbances. For DC PSRR, the power-supply voltage is changed with the analog inputs shorted together. The change of offset voltage is recorded over the change in power supply voltage. DC PSRR is computed as shown in Equation 5.

$$\text{PSRR (dB)} = 20 \cdot \log(\Delta V_{PS} / \Delta V_{OS}) \quad (5)$$

where:

- ΔV_{PS} = Change of power supply voltage
- ΔV_{OS} = Change of offset voltage

For AC PSRR, the power supply voltage is modulated with a 100mV signal at various test frequencies. An FFT of the ADC data under modulation is performed. As shown in Equation 6, the nine largest spurious frequencies in the frequency spectrum are summed as powers to determine AC PSRR.

$$\text{AC PSRR (dB)} = 20 \cdot \log(V_{PS} / V_O) \quad (6)$$

where:

- V_{PS} = 100mV power-supply modulation
- V_O = Root-sum-square amplitude of highest amplitude spurious frequencies = $\sqrt{(V_0^2 + V_1^2 + ...V_8^2)}$

9.1.6 INL

Integral nonlinearity (INL) error specifies the (dc) linearity of the ADC. INL is measured by applying a series of dc test voltages with amplitudes corresponding to the ADC gain. A straight line is computed from the slope and offset transfer function of the ADC. INL is the difference between the set of test voltages [$V_{IN(N)}$] and the corresponding set of output codes scaled to voltage [$V_{OUT(N)}$]. Equation 7 shows the *end-point* method of calculating INL error.

$$\text{INL (ppm FSR)} = \text{maximum absolute value of the set: } [10^6 \cdot (V_{IN(N)} – V_{OUT(N)}) / \text{FSR}] \quad (7)$$

where:

- N = Index of dc test voltage
- [$V_{IN(N)}$] = Set of test voltages over the range –95% FSR to 95% FSR
- [$V_{OUT(N)}$] = Set of corresponding ADC output voltages
- FSR (full-scale range) = $\pm 2V_{REF}$ / Gain

The INL *best-fit* method uses the least-squared error (LSE) to determine a new straight line to equalize the root-sum-square of the INL error above and below the new line.

9.1.7 THD

Total harmonic distortion (THD) specifies the dynamic (ac) linearity of the ADC. The test signal is –0.2dBFS, 1kHz with a common-mode voltage to meet the headroom requirements of the input buffer. As shown in Equation 8, THD is calculation of the ratio of the root-sum-square amplitude of harmonics to the input signal amplitude.

$$\text{THD (dB)} = 20 \cdot \log(V_H / V_{IN}) \quad (8)$$

where:

- V_H = Root-sum-square of harmonics: $\sqrt{(V_2^2+V_3^2+ ...V_n^2)}$, where V_n = Ninth harmonic voltage
- V_{IN} = Input signal fundamental

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9.2 Noise Performance

The ADS125R1x are a family of 24-bit delta-sigma ADCs providing very high resolution. The ADC resolution depends on the device configuration: speed mode, PGA gain, data rate and on use of the input buffer. The configurations allow trades-off between power consumption, resolution, conversion time and input impedance.

For a given data rate, the high-speed mode provides the lowest noise due to increased amount of averaging in the filter. Similarly, decreasing the data rate increases the amount of averaging in the filter which decreases noise. Because noise is an input-referred quantity, increasing the gain of the PGA decreases noise. The input buffer greatly increases the analog input impedance but affects noise performance over most data rates and gain settings.

Table 9-1 through Table 9-9 summarize noise performance for the high, mid and low speed modes and the sinc3, sinc4, and sinc5 digital filters. Noise data are the result of the standard deviation (rms) of the conversion data with inputs shorted to ground. Noise data are representative of typical performance using 32-bit output data format at T_A = 25°C with 64 consecutive conversions for data rates <100SPS or 1 second of consecutive conversions for data rates ≥ 100SPS. Because of the statistical nature of noise, repeated noise measurements can yield higher or lower noise results.

Effective resolution is the performance level in bits based on noise performance. Equation 9 converts input-referred noise (e_n) to effective resolution (bits). Noise-free resolution (the resolution in which no code flicker occurs) is typically 2.7 bits less than effective resolution. Because noise performance does not significantly change with reference voltage for OSR ≥ 64, increasing the reference voltage increases effective resolution. Effective resolution typically decreases with increased gain because the input range decreases at a faster rate than noise performance reduces.

$$\text{Effective Resolution (bits)} = \log_2 (4 \cdot V_{REF} / (\text{Gain} \cdot e_n)) \quad (9)$$

Table 9-1. Input-Referred Noise (e_N - μV_{RMS}) and Effective Resolution (Bits), High-Speed Mode, Sinc3 Filter, V_{REF} = 2.5V

DR[7:0]	DATA RATE (SPS)	INPUT BUFFER	GAIN							
			1	2	4	8	16	32	64	128
00000000b	10	On Off	0.159 (25.9) 0.163 (25.9)	0.104 (25.5) 0.085 (25.8)	0.072 (25.0) 0.051 (25.6)	0.056 (24.4) 0.032 (25.2)	0.042 (23.8) 0.022 (24.8)	0.028 (23.4) 0.012 (24.7)	0.028 (22.4) 0.013 (23.5)	0.028 (21.4) 0.013 (22.5)
00010000b	20	On Off	0.236 (25.3) 0.227 (25.4)	0.146 (25.0) 0.117 (25.4)	0.102 (24.5) 0.067 (25.2)	0.080 (23.9) 0.045 (24.7)	0.063 (23.3) 0.031 (24.3)	0.041 (22.9) 0.017 (24.1)	0.041 (21.9) 0.015 (23.3)	0.041 (20.9) 0.016 (22.2)
00100000b	40	On Off	0.323 (24.9) 0.296 (25.0)	0.200 (24.6) 0.167 (24.8)	0.147 (24.0) 0.098 (24.6)	0.110 (23.4) 0.063 (24.2)	0.086 (22.8) 0.043 (23.8)	0.056 (22.4) 0.022 (23.7)	0.056 (21.4) 0.022 (22.8)	0.056 (20.4) 0.022 (21.8)
00110000b	50	On Off	0.371 (24.7) 0.343 (24.8)	0.234 (24.3) 0.184 (24.7)	0.164 (23.9) 0.108 (24.5)	0.124 (23.3) 0.070 (24.1)	0.097 (22.6) 0.047 (23.7)	0.064 (22.2) 0.024 (23.6)	0.064 (21.2) 0.024 (22.6)	0.064 (20.2) 0.024 (21.6)
01000000b	60	On Off	0.400 (24.6) 0.375 (24.7)	0.253 (24.2) 0.204 (24.5)	0.177 (23.7) 0.120 (24.3)	0.135 (23.1) 0.078 (23.9)	0.104 (22.5) 0.051 (23.5)	0.069 (22.1) 0.025 (23.6)	0.069 (21.1) 0.025 (22.6)	0.069 (20.1) 0.025 (21.6)
01010000b	100	On Off	0.519 (24.2) 0.494 (24.3)	0.320 (23.9) 0.263 (24.2)	0.227 (23.4) 0.154 (23.9)	0.172 (22.8) 0.096 (23.6)	0.137 (22.1) 0.067 (23.2)	0.091 (21.7) 0.033 (23.1)	0.091 (20.7) 0.033 (22.2)	0.091 (19.7) 0.033 (21.2)
01100000b	120	On Off	0.541 (24.1) 0.516 (24.2)	0.353 (23.8) 0.290 (24.0)	0.248 (23.3) 0.171 (23.8)	0.190 (22.6) 0.106 (23.5)	0.149 (22.0) 0.073 (23.0)	0.098 (21.6) 0.036 (23.1)	0.098 (20.6) 0.036 (22.1)	0.098 (19.6) 0.036 (21.1)
01110000b	200	On Off	0.718 (23.7) 0.686 (23.8)	0.438 (23.4) 0.360 (23.7)	0.324 (22.9) 0.210 (23.5)	0.242 (22.3) 0.132 (23.2)	0.194 (21.6) 0.090 (22.7)	0.123 (21.3) 0.047 (22.7)	0.122 (20.3) 0.047 (21.7)	0.122 (19.3) 0.047 (20.7)
10000000b	240	On Off	0.809 (23.6) 0.736 (23.7)	0.512 (23.2) 0.420 (23.5)	0.357 (22.7) 0.229 (23.4)	0.263 (22.2) 0.149 (23.0)	0.218 (21.5) 0.100 (22.6)	0.137 (21.1) 0.051 (22.5)	0.137 (20.1) 0.050 (21.6)	0.137 (19.1) 0.050 (20.6)
10010000b	400	On Off	1.02 (23.2) 0.956 (23.3)	0.638 (22.9) 0.527 (23.2)	0.471 (22.3) 0.315 (22.9)	0.346 (21.8) 0.187 (22.7)	0.270 (21.1) 0.130 (22.2)	0.178 (20.7) 0.064 (22.2)	0.177 (19.7) 0.064 (21.2)	0.177 (18.7) 0.064 (20.2)
10100000b	800	On Off	1.41 (22.8) 1.34 (22.8)	0.900 (22.4) 0.734 (22.7)	0.644 (21.9) 0.436 (22.4)	0.483 (21.3) 0.270 (22.1)	0.378 (20.7) 0.180 (21.7)	0.258 (20.2) 0.091 (21.7)	0.253 (19.2) 0.090 (20.7)	0.253 (18.2) 0.090 (19.7)
10110000b	1600	On Off	2.03 (22.2) 1.94 (22.3)	1.25 (21.9) 1.06 (22.2)	0.903 (21.4) 0.617 (21.9)	0.705 (20.8) 0.385 (21.6)	0.537 (20.2) 0.258 (21.2)	0.356 (19.7) 0.128 (21.2)	0.356 (18.7) 0.128 (20.2)	0.356 (17.7) 0.127 (19.2)

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Table 9-2. Input-Referred Noise (e_N - μV_{RMS}) and Effective Resolution (Bits), Mid-Speed Mode, Sinc3 Filter, V_{REF} = 2.5V

DR[7:0]	DATA RATE (SPS)	INPUT BUFFER	GAIN							
			1	2	4	8	16	32	64	128
00000000b	5	On Off	0.164 (25.9) 0.149 (26.0)	0.101 (25.6) 0.078 (26.0)	0.070 (25.1) 0.047 (25.7)	0.056 (24.5) 0.033 (25.2)	0.040 (23.9) 0.023 (24.7)	0.025 (23.6) 0.011 (24.8)	0.025 (22.6) 0.011 (23.8)	0.024 (21.6) 0.011 (22.7)
00010000b	10	On Off	0.223 (25.4) 0.214 (25.5)	0.141 (25.1) 0.116 (25.4)	0.104 (24.5) 0.066 (25.2)	0.073 (24.0) 0.042 (24.8)	0.055 (23.4) 0.029 (24.4)	0.034 (23.1) 0.015 (24.3)	0.035 (22.1) 0.015 (23.3)	0.035 (21.1) 0.015 (22.4)
00100000b	20	On Off	0.329 (24.9) 0.286 (25.1)	0.181 (24.7) 0.162 (24.9)	0.139 (24.1) 0.094 (24.7)	0.099 (23.6) 0.061 (24.3)	0.080 (22.9) 0.040 (23.9)	0.050 (22.6) 0.020 (23.9)	0.050 (21.6) 0.020 (22.9)	0.049 (20.6) 0.020 (21.9)
00110000b	25	On Off	0.348 (24.8) 0.334 (24.8)	0.221 (24.4) 0.183 (24.7)	0.158 (23.9) 0.110 (24.5)	0.116 (23.4) 0.062 (24.3)	0.085 (22.8) 0.041 (23.9)	0.055 (22.4) 0.022 (23.8)	0.055 (21.4) 0.022 (22.8)	0.055 (20.4) 0.022 (21.7)
01000000b	30	On Off	0.377 (24.7) 0.357 (24.7)	0.233 (24.4) 0.194 (24.6)	0.168 (23.8) 0.112 (24.4)	0.129 (23.2) 0.073 (24.0)	0.093 (22.7) 0.046 (23.7)	0.060 (22.3) 0.024 (23.6)	0.059 (21.4) 0.024 (22.7)	0.059 (20.3) 0.024 (21.6)
01010000b	50	On Off	0.488 (24.2) 0.465 (24.4)	0.314 (23.9) 0.250 (24.3)	0.221 (23.4) 0.143 (24.1)	0.165 (22.8) 0.088 (23.8)	0.123 (22.3) 0.060 (23.3)	0.078 (21.7) 0.030 (23.3)	0.078 (20.7) 0.030 (22.2)	0.078 (19.7) 0.030 (21.3)
01100000b	60	On Off	0.531 (24.1) 0.505 (24.2)	0.334 (23.8) 0.273 (24.1)	0.242 (23.3) 0.157 (23.9)	0.183 (22.6) 0.097 (23.6)	0.137 (22.0) 0.068 (23.1)	0.084 (21.6) 0.034 (23.1)	0.084 (20.6) 0.034 (22.2)	0.084 (19.6) 0.034 (21.2)
01110000b	100	On Off	0.725 (23.7) 0.618 (23.9)	0.410 (23.5) 0.344 (23.8)	0.292 (23.0) 0.196 (23.6)	0.247 (22.3) 0.115 (23.4)	0.179 (21.7) 0.084 (22.8)	0.113 (21.5) 0.046 (22.8)	0.113 (20.4) 0.046 (21.7)	0.113 (19.3) 0.046 (20.7)
10000000b	120	On Off	0.770 (23.6) 0.719 (23.7)	0.455 (23.4) 0.375 (23.7)	0.312 (22.9) 0.226 (23.4)	0.245 (22.3) 0.148 (23.0)	0.184 (21.7) 0.091 (22.7)	0.115 (21.4) 0.045 (22.7)	0.115 (20.4) 0.045 (21.6)	0.115 (19.3) 0.045 (20.7)
10010000b	200	On Off	0.936 (23.3) 0.952 (23.3)	0.629 (22.9) 0.508 (23.2)	0.431 (22.5) 0.279 (23.1)	0.330 (21.8) 0.185 (22.7)	0.238 (21.3) 0.119 (22.3)	0.150 (21.0) 0.060 (22.3)	0.150 (19.9) 0.058 (21.4)	0.150 (18.9) 0.058 (20.4)
10100000b	400	On Off	1.34 (22.8) 1.27 (22.9)	0.875 (22.4) 0.724 (22.7)	0.627 (21.9) 0.411 (22.5)	0.470 (21.3) 0.253 (22.2)	0.344 (20.8) 0.173 (21.8)	0.220 (20.5) 0.085 (21.8)	0.220 (19.5) 0.085 (20.8)	0.220 (18.4) 0.085 (19.8)
10110000b	800	On Off	1.98 (22.3) 1.85 (22.4)	1.27 (21.9) 1.00 (22.3)	0.889 (21.4) 0.573 (22.1)	0.641 (20.9) 0.362 (21.7)	0.497 (20.3) 0.241 (21.3)	0.310 (19.9) 0.119 (21.3)	0.311 (18.9) 0.119 (20.3)	0.310 (18.0) 0.119 (19.3)

Table 9-3. Input-Referred Noise (e_N - μV_{RMS}) and Effective Resolution (Bits), Low-Speed Mode, Sinc3 Filter, V_{REF} = 2.5V

DR[7:0]	DATA RATE (SPS)	INPUT BUFFER	GAIN							
			1	2	4	8	16	32	64	128
00000000b	2.5	On Off	0.164 (25.9) 0.142 (26.1)	0.092 (25.7) 0.073 (26.0)	0.064 (25.2) 0.046 (25.7)	0.041 (24.9) 0.031 (25.3)	0.034 (24.1) 0.020 (24.9)	0.023 (23.7) 0.010 (25.0)	0.022 (22.8) 0.010 (23.9)	0.021 (21.8) 0.010 (22.8)
00010000b	5	On Off	0.216 (25.5) 0.210 (25.5)	0.135 (25.1) 0.115 (25.4)	0.097 (24.6) 0.060 (25.3)	0.067 (24.2) 0.039 (24.9)	0.055 (23.4) 0.025 (24.6)	0.031 (23.3) 0.014 (24.4)	0.030 (22.3) 0.013 (23.5)	0.030 (21.3) 0.012 (22.6)
00100000b	10	On Off	0.294 (25.0) 0.310 (24.9)	0.184 (24.7) 0.151 (25.0)	0.128 (24.2) 0.088 (24.8)	0.090 (23.6) 0.054 (24.5)	0.072 (23.1) 0.034 (24.1)	0.041 (22.9) 0.018 (24.1)	0.042 (21.8) 0.018 (23.0)	0.044 (20.7) 0.018 (22.1)
00110000b	12.5	On Off	0.337 (24.8) 0.314 (24.9)	0.219 (24.4) 0.173 (24.8)	0.148 (24.0) 0.094 (24.7)	0.104 (23.5) 0.060 (24.3)	0.084 (22.8) 0.039 (23.9)	0.049 (22.6) 0.021 (23.8)	0.048 (21.6) 0.021 (22.9)	0.047 (20.7) 0.021 (21.9)
01000000b	15	On Off	0.365 (24.7) 0.345 (24.8)	0.242 (24.3) 0.188 (24.7)	0.253 (24.0) 0.112 (24.4)	0.123 (23.3) 0.068 (24.1)	0.085 (22.8) 0.044 (23.8)	0.054 (22.5) 0.022 (23.8)	0.054 (21.5) 0.022 (22.7)	0.054 (20.4) 0.022 (21.8)
01010000b	25	On Off	0.468 (24.3) 0.453 (24.4)	0.296 (24.0) 0.248 (24.3)	0.211 (23.5) 0.142 (24.1)	0.155 (22.9) 0.083 (23.8)	0.111 (22.4) 0.055 (23.4)	0.070 (22.1) 0.028 (23.4)	0.069 (21.1) 0.028 (22.3)	0.069 (20.1) 0.028 (21.3)
01100000b	30	On Off	0.513 (24.2) 0.469 (24.3)	0.325 (23.9) 0.269 (24.1)	0.229 (23.4) 0.153 (24.0)	0.169 (22.8) 0.096 (23.6)	0.124 (22.3) 0.063 (23.2)	0.075 (22.0) 0.031 (23.2)	0.072 (21.0) 0.031 (23.2)	0.072 (20.0) 0.031 (21.2)
01110000b	50	On Off	0.652 (23.9) 0.599 (24.0)	0.371 (23.7) 0.362 (23.7)	0.289 (23.0) 0.194 (23.6)	0.233 (22.4) 0.111 (23.4)	0.150 (22.0) 0.085 (22.8)	0.094 (21.7) 0.042 (22.9)	0.092 (20.7) 0.042 (21.9)	0.092 (19.6) 0.040 (20.9)
10000000b	60	On Off	0.710 (23.7) 0.747 (23.7)	0.436 (23.4) 0.389 (23.6)	0.321 (22.9) 0.204 (23.5)	0.250 (22.3) 0.123 (23.3)	0.167 (21.8) 0.084 (22.8)	0.112 (21.5) 0.040 (23.0)	0.112 (20.4) 0.040 (21.7)	0.112 (19.4) 0.040 (20.9)
10010000b	100	On Off	0.904 (23.4) 0.927 (23.4)	0.564 (23.1) 0.448 (23.4)	0.415 (22.5) 0.284 (23.1)	0.305 (22.0) 0.181 (22.7)	0.225 (21.4) 0.105 (22.5)	0.142 (21.1) 0.057 (22.5)	0.141 (20.1) 0.057 (21.4)	0.140 (19.1) 0.057 (20.4)
10100000b	200	On Off	1.37 (22.8) 1.29 (22.9)	0.813 (22.6) 0.734 (22.7)	0.594 (22.0) 0.408 (22.5)	0.426 (21.5) 0.248 (22.3)	0.322 (20.9) 0.155 (21.9)	0.195 (20.6) 0.080 (21.9)	0.191 (19.6) 0.080 (20.8)	0.190 (18.7) 0.080 (19.9)
10110000b	400	On Off	1.91 (22.3) 1.83 (22.4)	1.20 (22.0) 0.941 (22.3)	0.868 (21.5) 0.547 (22.1)	0.610 (21.0) 0.345 (21.8)	0.459 (20.4) 0.228 (21.4)	0.280 (20.1) 0.112 (21.5)	0.275 (19.1) 0.112 (20.4)	0.275 (18.1) 0.112 (19.4)

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Table 9-4. Input-Referred Noise (e_N - μV_{RMS}) and Effective Resolution (Bits), High-Speed Mode, Sinc4 + Averaging Filter, V_{REF} = 2.5V

DR[7:0]	DATA RATE (SPS)	INPUT BUFFER	GAIN							
			1	2	4	8	16	32	64	128
00000011b	5	On Off	0.151 (26.0) 0.154 (26.0)	0.097 (25.6) 0.076 (26.0)	0.071 (25.1) 0.047 (25.7)	0.057 (24.4) 0.031 (25.3)	0.042 (23.8) 0.021 (24.8)	0.028 (23.4) 0.011 (24.8)	0.028 (22.4) 0.011 (23.7)	0.028 (21.4) 0.011 (22.7)
00010011b	10	On Off	0.217 (25.5) 0.221 (25.4)	0.146 (25.0) 0.114 (25.4)	0.102 (24.5) 0.065 (25.2)	0.074 (24.0) 0.044 (24.8)	0.061 (23.3) 0.030 (24.3)	0.039 (23.0) 0.015 (24.4)	0.038 (21.9) 0.015 (23.3)	0.038 (21.0) 0.015 (22.3)
00100011b	20	On Off	0.314 (24.9) 0.281 (25.1)	0.195 (24.6) 0.165 (24.8)	0.132 (24.2) 0.094 (24.7)	0.108 (23.5) 0.058 (24.3)	0.080 (22.9) 0.040 (23.9)	0.054 (22.5) 0.021 (23.8)	0.054 (21.5) 0.021 (22.8)	0.054 (20.5) 0.021 (21.8)
00110011b	30	On Off	0.373 (24.7) 0.357 (24.7)	0.228 (24.4) 0.188 (24.7)	0.162 (23.9) 0.118 (24.3)	0.129 (23.2) 0.076 (24.0)	0.104 (22.5) 0.048 (23.6)	0.065 (22.2) 0.024 (23.6)	0.065 (21.2) 0.024 (22.7)	0,065 (20.2) 0.024 (21.7)
01000011b	50	On Off	0.489 (24.3) 0.452 (24.4)	0.307 (24.0) 0.243 (24.3)	0.213 (23.5) 0.144 (24.0)	0.171 (22.8) 0.090 (23.7)	0.130 (22.2) 0.059 (23.3)	0.084 (21.8) 0.032 (23.2)	0.084 (20.8) 0.032 (22.2)	0.084 (19.8) 0.032 (21.3)
01010011b	60	On Off	0.533 (24.2) 0.516 (24.2)	0.338 (23.8) 0.280 (24.1)	0.243 (23.3) 0.161 (23.9)	0.186 (22.7) 0.103 (23.5)	0.139 (22.1) 0.070 (23.1)	0.094 (21.7) 0.035 (23.1)	0.094 (20.7) 0.035 (22.1)	0.094 (19.7) 0.035 (21.1)
01100011b	100	On Off	0.682 (23.8) 0.632 (23.9)	0.443 (23.4) 0.365 (23.7)	0.309 (22.9) 0.200 (23.6)	0.238 (22.3) 0.133 (23.2)	0.181 (21.7) 0.089 (22.7)	0.119 (21.3) 0.043 (22.8)	0.119 (20.3) 0.043 (21.8)	0.119 (19.3) 0.043 (20.8)
01110010b	120	On Off	0.743 (23.7) 0.717 (23.7)	0.482 (23.3) 0.396 (23.6)	0.336 (22.8) 0.225 (23.4)	0.262 (22.2) 0.141 (23.1)	0.198 (21.6) 0.096 (22.6)	0.130 (21.2) 0.048 (22.6)	0.130 (20.2) 0.048 (21.7)	0.130 (19.2) 0.048 (20.7)
10000010b	200	On Off	0.980 (23.3) 0.898 (23.4)	0.636 (22.9) 0.508 (23.2)	0.400 (22.6) 0.307 (23.0)	0.316 (21.9) 0.190 (22.6)	0.262 (21.2) 0.120 (22.3)	0.166 (20.8) 0.061 (22.3)	0.166 (19.8) 0.061 (21.3)	0.166 (18.8) 0.061 (20.3)
10010010b	1000	On Off	2.12 (22.2) 2.10 (22.2)	1.35 (21.8) 1.09 (22.1)	0.941 (21.3) 0.656 (21.9)	0.732 (20.7) 0.405 (21.6)	0.583 (20.0) 0.275 (21.1)	0.370 (19.7) 0.136 (21.2)	0.370 (18.7) 0.136 (20.1)	0.370 (17.7) 0.136 (19.1)
10100001b	2000	On Off	3.03 (21.7) 2.92 (21.7)	1.87 (21.3) 1.57 (21.6)	1.39 (20.8) 0.920 (21.4)	1.04 (20.2) 0.574 (21.1)	0.796 (19.6) 0.388 (20.6)	0.528 (19.2) 0.190 (20.7)	0.528 (18.2) 0.190 (19.6)	0.528 (17.2) 0.190 (18.6)
10110000b	4000	On Off	4.27 (21.2) 3.98 (21.3)	2.67 (20.8) 2.21 (21.1)	1.88 (20.3) 1.30 (20.9)	1.46 (19.7) 0.808 (20.6)	1.12 (19.1) 0.550 (20.1)	0.740 (18.7) 0.267 (20.2)	0.740 (17.7) 0.267 (19.2)	0.740 (16.7) 0.267 (18.2)
11000000b	7500	On Off	5.78 (20.7) 5.42 (20.8)	3.62 (20.4) 2.93 (20.7)	2.59 (19.9) 1.74 (20.5)	1.97 (19.3) 1.07 (20.1)	1.53 (18.6) 0.773 (19.7)	1.02 (18.2) 0.359 (19.7)	1.02 (17.2) 0.359 (18.7)	1.02 (16.2) 0.359 (17.7)
11010000b	15,000	On Off	7.76 (20.3) 7.32 (20.4)	4.89 (20.0) 4.00 (20.3)	3.47 (19.5) 2.35 (20.0)	2.63 (18.9) 1.46 (19.7)	2.05 (18.2) 0.993 (19.3)	1.32 (17.9) 0.486 (19.3)	1.32 (16.9) 0.486 (18.3)	1.32 (15.9) 0.486 (17.3)
11100000b	30,000	On Off	10.0 (19.9) 9.50 (20.0)	6.30 (19.6) 5.21 (19.9)	4.45 (19.1) 3.04 (19.6)	3.40 (18.5) 1.88 (19.3)	2.62 (17.9) 1.29 (18.9)	1.66 (17.5) 0.630 (18.9)	1.66 (16.5) 0.630 (17.9)	1.66 (15.5) 0.630 (16.9)
11110000b	60,000	On Off	11.6 (19.7) 10.9 (19.8)	7.29 (19.4) 6.05 (19.7)	5.16 (18.9) 3.52 (19.4)	3.91 (18.3) 2.19 (19.1)	3.00 (17.7) 1.49 (18.7)	1.90 (17.3) 0.732 (18.7)	1.90 (16.3) 0.732 (17.7)	1.90 (15.3) 0.732 (16.7)
11110100b	120,000	On Off	17.0 (19.2) 16.3 (19.2)	10.6 (18.9) 8.83 (19.1)	7.38 (18.4) 5.08 (18.9)	5.54 (17.8) 3.15 (18.6)	4.26 (17.2) 2.12 (18.2)	2.67 (16.8) 1.04 (18.2)	2.67 (15.8) 1.04 (17.2)	2.67 (14.8) 1.04 (16.2)
11111000b	240,000	On Off	36.6 (18.1) 35.7 (18.1)	20.2 (17.9) 18.5 (18.0)	12.5 (17.6) 9.94 (17.9)	8.58 (17.2) 5.65 (17.8)	6.27 (16.6) 3.48 (17.5)	3.88 (16.3) 1.72 (17.5)	3.88 (15.3) 1.72 (16.5)	3.88 (14.3) 1.72 (16.5)
11111100b	320,000	On Off	81.8 (16.9) 82.2 (16.9)	42.7 (16.8) 41.0 (16.9)	22.7 (16.7) 20.9 (16.9)	13.2 (16.5) 11.0 (16.8)	8.46 (16.2) 5.95 (16.7)	5.00 (15.9) 2.98 (16.7)	5.00 (14.9) 2.98 (15.7)	5.00 (13.9) 2.98 (14.7)

Table 9-5. Input-Referred Noise (e_N - μV_{RMS}) and Effective Resolution (Bits), Mid-Speed Mode, Sinc4 + Averaging Filter, V_{REF} = 2.5V

DR[7:0]	DATA RATE (SPS)	INPUT BUFFER	GAIN							
			1	2	4	8	16	32	64	128
00000011b	2.5	On Off	0.144 (26.0) 0.160 (25.9)	0.094 (25.7) 0.070 (26.1)	0.064 (25.2) 0.046 (25.7)	0.049 (24.6) 0.026 (25.5)	0.034 (24.1) 0.020 (24.9)	0.027 (23.5) 0.010 (24.9)	0.027 (22.5) 0.010 (24.0)	0.027 (21.5) 0.011 (22.8)
00010011b	5	On Off	0.213 (25.5) 0.204 (25.5)	0.142 (25.1) 0.109 (25.5)	0.099 (24.6) 0.064 (25.2)	0.074 (24.0) 0.038 (25.0)	0.054 (23.5) 0.028 (24.4)	0.035 (23.2) 0.014 (24.4)	0.035 (22.0) 0.014 (23.4)	0.035 (21.2) 0.014 (22.4)
00100011b	10	On Off	0.289 (25.0) 0.274 (25.1)	0.188 (24.7) 0.152 (25.0)	0.134 (24.1) 0.088 (24.8)	0.095 (23.7) 0.057 (24.4)	0.069 (23.1) 0.038 (24.0)	0.046 (22.7) 0.019 (24.0)	0.045 (21.7) 0.019 (22.9)	0.045 (20.7) 0.019 (21.9)
00110011b	15	On Off	0.330 (24.8) 0.327 (24.9)	0.221 (24.4) 0.174 (24.8)	0.162 (23.9) 0.112 (24.4)	0.114 (23.4) 0.063 (24.3)	0.083 (22.8) 0.047 (23.7)	0.055 (22.4) 0.023 (23.7)	0.055 (21.4) 0.023 (22.7)	0.055 (20.4) 0.023 (21.7)
01000011b	25	On Off	0.470 (24.3) 0.453 (24.4)	0.296 (24.0) 0.243 (24.3)	0.215 (23.5) 0.151 (24.0)	0.153 (23.0) 0.088 (23.8)	0.118 (22.3) 0.058 (23.4)	0.074 (22.0) 0.029 (23.4)	0.074 (21.0) 0.029 (22.3)	0.074 (20.0) 0.029 (21.3)
01010011b	30	On Off	0.493 (24.3) 0.489 (24.3)	0.322 (23.9) 0.268 (24.2)	0.228 (23.4) 0.159 (23.9)	0.176 (22.8) 0.096 (23.6)	0.118 (22.3) 0.063 (23.2)	0.077 (22.0) 0.032 (23.2)	0.077 (20.9) 0.032 (22.2)	0.077 (20.0) 0.032 (21.2)
01100011b	50	On Off	0.671 (23.8) 0.593 (24.0)	0.430 (23.5) 0.331 (23.8)	0.286 (23.1) 0.195 (23.6)	0.222 (22.4) 0.120 (23.3)	0.168 (21.8) 0.081 (22.9)	0.104 (21.5) 0.042 (22.9)	0.104 (20.5) 0.042 (21.9)	0.104 (19.5) 0.042 (20.8)

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Table 9-5. Input-Referred Noise (e_N - μV_{RMS}) and Effective Resolution (Bits), Mid-Speed Mode, Sinc4 + Averaging Filter, V_{REF} = 2.5V (continued)

DR[7:0]	DATA RATE (SPS)	INPUT BUFFER	GAIN							
			1	2	4	8	16	32	64	128
01110010b	60	On Off	0.721 (23.7) 0.682 (23.8)	0.441 (23.4) 0.362 (23.7)	0.319 (22.9) 0.207 (23.5)	0.237 (22.3) 0.133 (23.2)	0.186 (21.7) 0.086 (22.8)	0.113 (21.4) 0.044 (22.8)	0.113 (20.4) 0.044 (21.7)	0.113 (19.4) 0.044 (20.8)
10000010b	100	On Off	0.908 (23.4) 0.864 (23.5)	0.569 (23.1) 0.516 (23.2)	0.451 (22.4) 0.272 (23.1)	0.296 (22.0) 0.167 (22.8)	0.235 (21.3) 0.114 (22.4)	0.150 (21.0) 0.056 (22.4)	0.150 (20.1) 0.056 (21.5)	0.150 (19.0) 0.056 (20.3)
10010010b	500	On Off	2.06 (22.2) 1.90 (22.3)	1.27 (21.9) 1.07 (22.2)	0.932 (21.4) 0.607 (22.0)	0.667 (20.8) 0.374 (21.7)	0.516 (20.2) 0.258 (21.2)	0.330 (19.9) 0.126 (21.2)	0.330 (18.8) 0.126 (20.2)	0.330 (17.8) 0.126 (19.3)
10100001b	1000	On Off	2.81 (21.8) 2.78 (21.8)	1.84 (21.4) 1.49 (21.7)	1.29 (20.9) 0.873 (21.4)	0.986 (20.3) 0.535 (21.2)	0.740 (19.7) 0.352 (20.8)	0.455 (19.4) 0.180 (20.7)	0.455 (18.4) 0.180 (19.7)	0.455 (17.4) 0.180 (18.7)
10110000b	2000	On Off	4.11 (21.2) 3.83 (21.3)	2.57 (20.9) 2.10 (21.2)	1.81 (20.4) 1.21 (21.0)	1.35 (19.8) 0.754 (20.7)	1.01 (19.2) 0.489 (20.3)	0.643 (18.9) 0.250 (20.3)	0.643 (17.9) 0.250 (19.2)	0.643 (16.9) 0.250 (18.3)
11000000b	3750	On Off	5.48 (20.8) 5.12 (20.9)	3.46 (20.5) 2.78 (20.8)	2.47 (19.9) 1.66 (20.5)	1.82 (19.4) 1.01 (20.2)	1.39 (18.8) 0.672 (19.8)	0.864 (18.5) 0.334 (19.8)	0.864 (17.5) 0.334 (18.8)	0.864 (16.5) 0.334 (17.8)
11010000b	7500	On Off	7.43 (20.4) 7.09 (20.4)	4.70 (20.0) 3.83 (20.3)	3.33 (19.5) 2.21 (20.1)	2.45 (19.0) 1.36 (19.8)	1.88 (18.3) 0.913 (19.4)	1.16 (18.0) 0.455 (19.4)	1.16 (17.0) 0.455 (18.4)	1.16 (16.0) 0.455 (17.4)
11100000b	15,000	On Off	9.75 (20.0) 9.13 (20.1)	6.07 (19.7) 4.96 (19.9)	4.33 (19.1) 2.86 (19.7)	3.18 (18.6) 1.76 (19.4)	2.40 (18.0) 1.17 (19.0)	1.49 (17.7) 0.586 (19.0)	1.49 (16.7) 0.586 (18.0)	1.49 (15.7) 0.586 (17.0)
11110000b	30,000	On Off	11.2 (19.8) 10.6 (19.9)	7.06 (19.4) 5.78 (19.7)	4.98 (18.9) 3.32 (19.5)	3.71 (18.4) 2.06 (19.2)	2.76 (17.8) 1.36 (18.8)	1.69 (17.5) 0.681 (18.8)	1.69 (16.5) 0.681 (17.8)	1.69 (15.5) 0.681 (16.8)
11110100b	60,000	On Off	16.4 (19.2) 15.5 (19.3)	10.2 (18.9) 8.41 (19.2)	7.10 (18.4) 4.80 (19.0)	5.21 (17.9) 2.94 (18.7)	3.93 (17.3) 1.94 (18.3)	2.39 (17.0) 0.972 (18.3)	2.39 (16.0) 0.972 (17.3)	2.39 (15.0) 0.972 (16.3)
11111000b	120,000	On Off	35.3 (18.1) 35.1 (18.1)	19.9 (17.9) 18.0 (18.1)	12.2 (17.6) 9.63 (18.0)	8.16 (17.2) 5.41 (17.8)	5.78 (16.7) 3.25 (17.6)	3.47 (16.5) 1.62 (17.6)	3.47 (15.5) 1.62 (16.6)	3.47 (14.5) 1.62 (15.6)
11111100b	160,000	On Off	82.9 (16.9) 82.3 (16.9)	42.3 (16.9) 41.6 (16.9)	22.9 (16.7) 21.1 (16.9)	13.0 (16.6) 10.8 (16.8)	8.03 (16.2) 5.84 (16.7)	4.60 (16.1) 2.91 (16.7)	4.60 (15.1) 2.90 (15.7)	4.60 (14.1) 2.91 (14.7)

Table 9-6. Input-Referred Noise (e_N - μV_{RMS}) and Effective Resolution (Bits), Low-Speed Mode, Sinc4 + Averaging Filter, V_{REF} = 2.5V

DR[7:0]	DATA RATE (SPS)	INPUT BUFFER	GAIN							
			1	2	4	8	16	32	64	128
00000011b	1.25	On Off	0.170 (25.8) 0.130 (26.2)	0.104 (25.5) 0.086 (25.8)	0.060 (25.3) 0.039 (25.9)	0.047 (24.6) 0.032 (25.2)	0.029 (24.4) 0.019 (24.9)	0.022 (23.7) 0.010 (24.9)	0.022 (22.8) 0.010 (23.9)	0.022 (21.8) 0.010 (22.9)
00010011b	2.5	On Off	0.206 (25.5) 0.196 (25.6)	0.125 (25.3) 0.104 (25.5)	0.093 (24.7) 0.058 (25.4)	0.066 (24.2) 0.038 (25.0)	0.047 (23.6) 0.023 (24.7)	0.030 (23.3) 0.014 (24.5)	0.030 (22.3) 0.014 (23.4)	0.030 (21.3) 0.014 (22.4)
00100011b	5	On Off	0.311 (24.9) 0.266 (25.2)	0.172 (24.8) 0.153 (25.0)	0.128 (24.2) 0.081 (24.9)	0.094 (23.7) 0.051 (24.5)	0.068 (23.1) 0.035 (24.1)	0.041 (22.9) 0.017 (23.9)	0.041 (21.9) 0.017 (22.9)	0.041 (20.9) 0.017 (21.8)
00110011b	7.5	On Off	0.343 (24.8) 0.353 (24.8)	0.232 (24.4) 0.183 (24.7)	0.160 (23.9) 0.102 (24.5)	0.120 (23.3) 0.058 (24.4)	0.080 (22.9) 0.043 (23.8)	0.052 (22.5) 0.020 (23.9)	0.051 (21.6) 0.020 (22.9)	0.051 (20.6) 0.020 (21.9)
01000011b	12.5	On Off	0.439 (24.4) 0.435 (24.5)	0.276 (24.1) 0.226 (24.4)	0.200 (23.6) 0.136 (24.1)	0.140 (23.1) 0.086 (23.8)	0.111 (22.4) 0.052 (23.5)	0.064 (22.2) 0.027 (23.5)	0.064 (21.2) 0.027 (22.4)	0.064 (20.2) 0.027 (21.5)
01010011b	15	On Off	0.526 (24.2) 0.469 (24.3)	0.317 (23.9) 0.235 (24.3)	0.215 (23.5) 0.153 (24.0)	0.154 (23.0) 0.093 (23.7)	0.111 (22.4) 0.054 (23.5)	0.071 (22.0) 0.030 (23.4)	0.071 (21.0) 0.030 (22.3)	0.071 (20.1) 0.030 (21.3)
01100011b	25	On Off	0.633 (23.9) 0.626 (23.9)	0.386 (23.6) 0.335 (23.8)	0.285 (23.1) 0.191 (23.6)	0.191 (22.6) 0.121 (23.3)	0.154 (22.0) 0.077 (22.9)	0.094 (21.6) 0.040 (22.9)	0.094 (20.7) 0.040 (22.0)	0.094 (19.7) 0.040 (20.9)
01110010b	30	On Off	0.717 (23.7) 0.696 (23.8)	0.451 (23.4) 0.366 (23.7)	0.311 (22.9) 0.211 (23.5)	0.223 (22.4) 0.123 (23.3)	0.159 (21.9) 0.083 (22.8)	0.100 (21.6) 0.042 (22.8)	0.100 (20.6) 0.042 (21.9)	0.100 (19.6) 0.042 (20.8)
10000010b	50	On Off	0.792 (23.6) 0.954 (23.3)	0.621 (22.9) 0.471 (23.3)	0.424 (22.5) 0.249 (23.3)	0.289 (22.0) 0.177 (22.7)	0.203 (21.6) 0.097 (22.6)	0.132 (21.2) 0.051 (22.5)	0.132 (20.2) 0.051 (21.5)	0.132 (19.2) 0.051 (20.4)
10010010b	250	On Off	2.01 (22.2) 1.88 (22.3)	1.28 (21.9) 1.03 (22.2)	0.881 (21.4) 0.611 (22.0)	0.636 (20.9) 0.334 (21.8)	0.474 (20.3) 0.232 (21.4)	0.298 (20.0) 0.122 (21.3)	0.298 (19.0) 0.122 (20.3)	0.298 (18.0) 0.122 (19.3)
10100001b	500	On Off	2.75 (21.8) 2.60 (21.9)	1.81 (21.4) 1.49 (21.7)	1.23 (20.9) 0.809 (21.6)	0.879 (20.4) 0.505 (21.2)	0.660 (19.9) 0.327 (20.9)	0.410 (19.5) 0.169 (20.8)	0.410 (18.5) 0.169 (19.8)	0.410 (17.5) 0.169 (18.8)
10110000b	1000	On Off	4.01 (21.2) 3.85 (21.3)	2.49 (20.9) 2.06 (21.2)	1.77 (20.4) 1.17 (21.0)	1.25 (19.9) 0.695 (20.8)	0.939 (19.3) 0.476 (20.3)	0.568 (19.1) 0.232 (20.4)	0.568 (18.1) 0.232 (19.3)	0.568 (17.1) 0.232 (18.4)
11000000b	1875	On Off	5.38 (20.8) 5.15 (20.9)	3.43 (20.5) 2.76 (20.8)	2.32 (20.0) 1.55 (20.6)	1.71 (19.5) 0.980 (20.3)	1.25 (18.9) 0.627 (19.9)	0.770 (18.6) 0.318 (19.9)	0.770 (17.6) 0.318 (18.9)	0.770 (16.6) 0.318 (17.9)
11010000b	3750	On Off	7.38 (20.4) 6.94 (20.5)	4.54 (20.1) 3.77 (20.3)	3.21 (19.6) 2.13 (20.2)	2.32 (19.0) 1.29 (19.9)	1.69 (18.5) 0.851 (19.5)	1.03 (18.2) 0.428 (19.5)	1.03 (18.2) 0.428 (18.5)	1.03 (16.2) 0.428 (17.5)

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Table 9-6. Input-Referred Noise (e_N - μV_{RMS}) and Effective Resolution (Bits), Low-Speed Mode, Sinc4 + Averaging Filter, V_{REF} = 2.5V (continued)

DR[7:0]	DATA RATE (SPS)	INPUT BUFFER	GAIN							
			1	2	4	8	16	32	64	128
11100000b	7500	On Off	9.67 (20.0) 8.99 (20.1)	5.82 (19.7) 4.85 (20.0)	4.15 (19.2) 2.78 (19.8)	2.99 (18.7) 1.69 (19.5)	2.21 (18.1) 1.11 (19.1)	1.34 (17.8) 0.558 (19.1)	1.34 (16.8) 0.558 (18.1)	1.34 (15.8) 0.558 (17.1)
11110000b	15,000	On Off	11.1 (19.8) 10.4 (19.9)	6.84 (19.5) 5.63 (19.8)	4.84 (19.0) 3.20 (19.6)	3.49 (18.4) 1.96 (19.3)	2.53 (17.9) 1.29 (18.9)	1.53 (17.6) 0.656 (18.9)	1.53 (16.6) 0.656 (17.9)	1.53 (15.6) 0.656 (17.9)
11110100b	30,000	On Off	16.3 (19.2) 15.4 (19.3)	9.90 (18.9) 8.34 (19.2)	6.87 (18.5) 4.65 (19.0)	4.96 (17.9) 2.83 (18.8)	3.58 (17.4) 1.83 (18.4)	2.15 (17.1) 0.922 (18.4)	2.15 (16.1) 0.922 (17.4)	2.15 (15.1) 0.922 (16.4)
11111000b	60,000	On Off	35.2 (18.1) 34.9 (18.1)	19.5 (18.0) 17.9 (18.1)	11.9 (17.7) 9.46 (18.0)	7.80 (17.3) 5.22 (17.9)	5.36 (16.8) 3.08 (17.6)	3.14 (16.6) 1.55 (17.6)	3.14 (15.6) 1.55 (16.6)	3.14 (14.6) 1.55 (15.6)
11111100b	80,000	On Off	82.1 (16.9) 81.9 (16.9)	42.0 (16.9) 41.1 (16.9)	22.2 (16.8) 20.7 (16.9)	12.6 (16.6) 10.7 (16.8)	7.62 (16.3) 5.66 (16.8)	4.25 (16.2) 2.85 (16.7)	4.25 (15.2) 2.85 (15.7)	4.25 (14.2) 2.85 (14.7)

Table 9-7. Input-Referred Noise (e_n - μV_{RMS}) and Effective Resolution (bits), High-Speed Mode, Sinc5 + Averaging Filter, V_{REF} = 2.5V

DR[7:0]	DATA RATE (SPS)	INPUT BUFFER	GAIN							
			1	2	4	8	16	32	64	128
00000011b	5	On Off	0.162 (25.9) 0.147 (26.0)	0.093 (25.7) 0.079 (25.9)	0.063 (25.2) 0.049 (25.6)	0.056 (24.4) 0.030 (25.3)	0.042 (23.8) 0.024 (24.6)	0.030 (23.3) 0.011 (24.7)	0.026 (22.5) 0.011 (23.7)	0.025 (21.6) 0.011 (22.7)
00010011b	10	On Off	0.217 (25.5) 0.219 (25.4)	0.139 (25.1) 0.113 (25.4)	0.100 (24.6) 0.066 (25.2)	0.078 (24.0) 0.042 (24.8)	0.056 (23.4) 0.030 (24.3)	0.040 (22.9) 0.015 (24.3)	0.032 (22.0) 0.015 (23.3)	0.035 (21.0) 0.015 (22.3)
00100011b	20	On Off	0.306 (25.0) 0.292 (25.0)	0.199 (24.6) 0.158 (24.9)	0.139 (24.1) 0.097 (24.6)	0.108 (23.5) 0.059 (24.3)	0.084 (22.9) 0.042 (23.8)	0.054 (22.5) 0.021 (23.8)	0.055 (21.5) 0.021 (22.8)	0.053 (20.4) 0.020 (21.9)
00110011b	30	On Off	0.383 (24.6) 0.353 (24.8)	0.247 (24.3) 0.206 (24.5)	0.159 (23.9) 0.114 (24.4)	0.122 (23.3) 0.070 (24.1)	0.107 (22.5) 0.051 (23.5)	0.064 (22.3) 0.025 (23.6)	0.065 (21.2) 0.025 (22.6)	0.065 (20.2) 0.024 (21.7)
01000011b	50	On Off	0.492 (24.3) 0.455 (24.4)	0.307 (24.0) 0.255 (24.2)	0.226 (23.4) 0.143 (24.0)	0.162 (22.9) 0.093 (23.7)	0.127 (22.2) 0.062 (23.3)	0.088 (21.8) 0.031 (23.2)	0.086 (20.8) 0.031 (22.3)	0.085 (19.8) 0.031 (21.3)
01010011b	60	On Off	0.545 (24.1) 0.492 (24.3)	0.339 (23.8) 0.276 (24.1)	0.235 (23.3) 0.165 (23.9)	0.177 (22.7) 0.101 (23.6)	0.145 (22.0) 0.068 (23.1)	0.096 (21.7) 0.033 (23.1)	0.092 (20.7) 0.034 (22.2)	0.092 (19.7) 0.033 (21.1)
01100011b	100	On Off	0.690 (23.8) 0.656 (23.9)	0.433 (23.5) 0.349 (23.8)	0.300 (23.0) 0.205 (23.5)	0.238 (22.4) 0.131 (23.2)	0.183 (21.7) 0.085 (22.8)	0.115 (21.3) 0.044 (22.8)	0.112 (20.3) 0.044 (21.8)	0.112 (19.3) 0.044 (20.7)
01110010b	120	On Off	0.752 (23.7) 0.707 (23.8)	0.489 (23.3) 0.393 (23.6)	0.336 (22.8) 0.214 (23.4)	0.258 (22.2) 0.145 (23.0)	0.198 (21.6) 0.094 (22.6)	0.133 (21.1) 0.047 (22.7)	0.134 (20.2) 0.048 (21.6)	0.133 (19.2) 0.047 (20.7)
10000010b	200	On Off	0.965 (23.3) 0.876 (23.4)	0.641 (22.9) 0.472 (23.3)	0.461 (22.4) 0.306 (23.0)	0.350 (21.8) 0.173 (22.8)	0.242 (21.3) 0.119 (22.3)	0.162 (20.9) 0.062 (22.3)	0.165 (19.8) 0.064 (21.2)	0.164 (18.9) 0.063 (20.3)
10010010b	1000	On Off	2.20 (22.1) 2.03 (22.2)	1.36 (21.8) 1.10 (22.1)	0.951 (21.3) 0.655 (21.9)	0.751 (20.7) 0.397 (21.6)	0.599 (20.0) 0.278 (21.1)	0.379 (19.7) 0.137 (21.1)	0.378 (18.7) 0.133 (20.2)	0.381 (17.6) 0.133 (19.2)
10100001b	2000	On Off	3.02 (21.7) 2.84 (21.7)	1.89 (21.3) 1.60 (21.6)	1.34 (20.8) 0.914 (21.4)	1.04 (20.2) 0.573 (21.1)	0.784 (19.6) 0.382 (20.6)	0.530 (19.2) 0.186 (20.7)	0.530 (18.2) 0.189 (19.7)	0.530 (17.1) 0.191 (18.6)
10110000b	4000	On Off	4.26 (21.2) 4.01 (21.2)	2.71 (20.8) 2.18 (21.1)	1.90 (20.3) 1.28 (20.9)	1.45 (19.7) 0.796 (20.6)	1.13 (19.1) 0.535 (20.2)	0.736 (18.7) 0.266 (20.2)	0.735 (17.7) 0.265 (19.2)	0.735 (16.7) 0.267 (18.2)
11000000b	7500	On Off	5.72 (20.7) 5.37 (20.8)	3.56 (20.4) 2.94 (20.7)	2.55 (19.9) 1.69 (20.5)	1.95 (19.3) 1.08 (20.1)	1.54 (18.6) 0.728 (19.7)	1.00 (18.2) 0.354 (19.8)	1.02 (17.2) 0.356 (18.7)	1.04 (16.2) 0.356 (17.7)
11010000b	15,000	On Off	7.65 (20.3) 7.21 (20.4)	4.80 (20.0) 3.96 (20.3)	3.41 (19.5) 2.31 (20.0)	2.60 (18.9) 1.45 (19.7)	2.03 (18.2) 0.979 (19.3)	1.30 (17.9) 0.481 (19.3)	1.30 (16.9) 0.480 (18.3)	1.30 (15.9) 0.482 (17.3)
11100000b	30,000	On Off	9.70 (20.0) 9.25 (20.0)	6.14 (19.6) 5.03 (19.9)	4.35 (19.1) 2.94 (19.7)	3.29 (18.5) 1.84 (19.4)	2.53 (17.9) 1.24 (18.9)	1.62 (17.6) 0.613 (19.0)	1.62 (16.6) 0.607 (18.0)	1.63 (15.6) 0.610 (17.0)
11110000b	60,000	On Off	11.1 (19.8) 10.4 (19.9)	6.95 (19.5) 5.79 (19.7)	4.85 (19.0) 3.38 (19.5)	3.68 (18.4) 2.07 (19.2)	2.87 (17.7) 1.42 (18.7)	1.82 (17.4) 0.694 (18.8)	1.81 (16.4) 0.693 (17.8)	1.81 (15.4) 0.693 (16.8)
11110100b	120,000	On Off	16.1 (19.2) 15.2 (19.3)	10.0 (18.9) 8.35 (19.2)	6.98 (18.4) 4.82 (19.0)	5.25 (17.9) 2.97 (18.7)	4.04 (17.2) 2.01 (18.2)	2.53 (16.9) 0.981 (18.3)	2.53 (15.9) 0.981 (17.3)	2.53 (14.9) 0.981 (16.3)
11111000b	240,000	On Off	28.8 (18.4) 27.7 (18.5)	16.6 (18.2) 14.6 (18.4)	10.8 (17.8) 8.13 (18.2)	7.78 (17.3) 4.81 (18.0)	5.79 (16.7) 3.08 (17.6)	3.62 (16.4) 1.50 (17.7)	3.63 (15.4) 1.51 (16.7)	3.63 (14.4) 1.50 (15.7)
11111100b	320,000	On Off	55.6 (17.5) 55.1 (17.5)	29.5 (17.4) 28.1 (17.4)	16.8 (17.2) 14.6 (17.4)	10.6 (16.9) 7.88 (17.3	7.29 (16.4) 4.54 (17.1)	4.43 (16.1) 2.24 (17.1)	4.44 (15.1) 2.23 (16.1)	4.43 (14.1) 2.24 (16.1)

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Table 9-8. Input-Referred Noise (e_n - μV_{RMS}) and Effective Resolution (bits), Mid-Speed Mode, Sinc5 + Averaging Filter, V_{REF} = 2.5V

DR[7:0]	DATA RATE (SPS)	INPUT BUFFER	GAIN							
			1	2	4	8	16	32	64	128
00000011b	2.5	On Off	0.158 (25.9) 0.136 (26.1)	0.093 (25.7) 0.077 (25.9)	0.073 (25.0) 0.047 (25.7)	0.049 (24.6) 0.028 (25.4)	0.040 (23.9) 0.019 (25.0)	0.022 (23.8) 0.010 (25.0)	0.023 (22.7) 0.010 (23.9)	0.023 (21.7) 0.010 (22.9)
00010011b	5	On Off	0.208 (25.5) 0.204 (25.5)	0.135 (25.1) 0.104 (25.5)	0.098 (24.6) 0.065 (25.2)	0.070 (24.1) 0.036 (25.0)	0.053 (23.5) 0.028 (24.4)	0.033 (23.2) 0.013 (24.4)	0.033 (22.1) 0.013 (23.5)	0.033 (21.1) 0.013 (22.5)
00100011b	10	On Off	0.294 (25.0) 0.287 (25.1)	0.188 (24.7) 0.157 (24.9)	0.127 (24.2) 0.086 (24.8)	0.091 (23.7) 0.058 (24.4)	0.074 (23.0) 0.040 (23.9)	0.047 (22.7) 0.020 (23.9)	0.047 (21.6) 0.020 (23.0)	0.047 (20.6) 0.020 (21.9)
00110011b	15	On Off	0.362 (24.7) 0.351 (24.8)	0.236 (24.3) 0.187 (24.7)	0.163 (23.9) 0.104 (24.5)	0.120 (23.3) 0.065 (24.2)	0.093 (22.7) 0.045 (23.7)	0.056 (22.4) 0.022 (23.7)	0.056 (21.5) 0.022 (22.7)	0.056 (20.4) 0.022 (21.7)
01000011b	25	On Off	0.433 (24.5) 0.454 (24.4)	0.284 (24.1) 0.231 (24.4)	0.205 (23.5) 0.142 (24.1)	0.159 (22.9) 0.084 (23.8)	0.121 (22.3) 0.056 (23.4)	0.074 (22.0) 0.029 (23.4)	0.074 (21.1) 0.029 (22.4)	0.074 (20.0) 0.029 (21.4)
01010011b	30	On Off	0.538 (24.1) 0.468 (24.3)	0.329 (23.9) 0.267 (24.2)	0.234 (23.3) 0.152 (24.0)	0.177 (22.7) 0.089 (23.7)	0.128 (22.2) 0.064 (23.2)	0.082 (21.8) 0.031 (23.3)	0.082 (20.9) 0.031 (22.2)	0.082 (19.9) 0.031 (21.2)
01100011b	50	On Off	0.641 (23.9) 0.633 (23.9)	0.410 (23.5) 0.328 (23.9)	0.291 (23.0) 0.202 (23.6)	0.221 (22.4) 0.117 (23.3)	0.167 (21.8) 0.079 (22.9)	0.103 (21.5) 0.039 (22.9)	0.103 (20.5) 0.039 (21.9)	0.103 (19.5) 0.039 (20.9)
01110010b	60	On Off	0.720 (23.7) 0.646 (23.9)	0.454 (23.4) 0.372 (23.7)	0.320 (22.9) 0.227 (23.4)	0.243 (22.3) 0.128 (23.2)	0.175 (21.8) 0.086 (22.8)	0.114 (21.4) 0.044 (22.7)	0.114 (20.4) 0.044 (21.7)	0.114 (19.4) 0.044 (20.8)
10000010b	100	On Off	0.894 (23.4) 0.857 (23.5)	0.609 (23.0) 0.524 (23.2)	0.392 (22.6) 0.277 (23.1)	0.328 (21.9) 0.155 (22.9)	0.225 (21.4) 0.122 (22.3)	0.152 (21.0) 0.056 (22.4)	0.152 (20.0) 0.056 (21.5)	0.152 (19.1) 0.056 (20.4)
10010010b	500	On Off	2.11 (22.2) 1.93 (22.3)	1.32 (21.8) 1.08 (22.1)	0.878 (21.4) 0.624 (21.9)	0.702 (20.8) 0.370 (21.7)	0.522 (20.2) 0.249 (21.3)	0.320 (19.9) 0.126 (21.2)	0.320 (18.9) 0.126 (20.2)	0.320 (17.9) 0.126 (19.2)
10100001b	1000	On Off	2.89 (21.7) 2.72 (21.8)	1.84 (21.4) 1.51 (21.7)	1.32 (20.8) 0.852 (21.5)	0.969 (20.3) 0.533 (21.2)	0.728 (19.7) 0.359 (20.7)	0.454 (19.4) 0.174 (20.8)	0.454 (18.4) 0.181 (19.7)	0.454 (17.4) 0.177 (18.8)
10110000b	2000	On Off	4.06 (21.2) 3.78 (21.3)	2.59 (20.9) 2.06 (21.2)	1.84 (20.4) 1.21 (21.0)	1.38 (19.8) 0.747 (20.7)	1.00 (19.3) 0.500 (20.3)	0.640 (18.9) 0.248 (20.3)	0.640 (17.9) 0.248 (19.3)	0.640 (16.9) 0.248 (18.3)
11000000b	3750	On Off	5.50 (20.8) 5.18 (20.9)	3.45 (20.5) 2.78 (20.8)	2.44 (20.0) 1.60 (20.6)	1.81 (19.4) 1.00 (20.3)	1.38 (18.8) 0.667 (19.8)	0.850 (18.5) 0.330 (19.9)	0.850 (17.5) 0.330 (18.8)	0.850 (16.5) 0.330 (17.8)
11010000b	7500	On Off	7.44 (20.4) 6.93 (20.5)	4.63 (20.0) 3.75 (20.3)	3.32 (19.5) 2.19 (20.1)	2.45 (19.0) 1.34 (19.8)	1.85 (18.4) 0.893 (19.4)	1.18 (18.0) 0.450 (19.4)	1.18 (17.0) 0.450 (18.4)	1.18 (16.0) 0.450 (17.4)
11100000b	15,000	On Off	9.37 (20.0) 8.80 (20.1)	5.93 (19.7) 4.81 (20.0)	4.17 (19.2) 2.76 (19.8)	3.12 (18.6) 1.70 (19.5)	2.31 (18.0) 1.14 (19.1)	1.44 (17.7) 0.570 (19.1)	1.44 (16.7) 0.570 (18.1)	1.44 (15.7) 0.570 (17.1)
11110000b	30,000	On Off	10.6 (19.8) 9.96 (19.9)	6.72 (19.5) 5.43 (19.8)	4.71 (19.0) 3.15 (19.6)	3.47 (18.5) 1.92 (19.3)	2.61 (17.9) 1.28 (18.9)	1.61 (17.6) 0.645 (18.9)	1.61 (16.6) 0.645 (17.9)	1.61 (15.6) 0.645 (16.9)
11110100b	60,000	On Off	15.5 (19.3) 14.7 (19.4)	9.62 (19.0) 7.92 (19.3)	6.71 (18.5) 4.53 (19.1)	4.95 (17.9) 2.78 (18.8)	3.69 (17.4) 1.83 (18.4)	2.26 (17.1) 0.920 (18.4)	2.26 (16.1) 0.920 (17.4)	2.26 (15.1) 0.920 (16.4)
11111000b	120,000	On Off	28.0 (18.4) 27.1 (18.5)	16.2 (18.2) 14.2 (18.4)	10.5 (17.9) 7.81 (18.3)	7.32 (17.4) 4.51 (18.1)	5.33 (16.8) 2.81 (17.8)	3.24 (16.6) 1.41 (17.8)	3.24 (15.6) 1.41 (16.8)	3.24 (14.6) 1.41 (15.8)
11111100b	160,000	On Off	55.2 (17.5) 54.6 (17.5)	29.1 (17.4) 27.7 (17.5)	16.5 (17.2) 14.4 (17.4)	10.2 (16.9) 7.62 (17.3)	6.77 (16.5) 4.31 (17.1)	3.99 (16.3) 2.15 (17.1)	3.99 (15.3) 2.15 (16.2)	3.99 (14.3) 2.15 (15.2)

Table 9-9. Input-Referred Noise (e_n - μV_{RMS}) and Effective Resolution (bits), Low-Speed Mode, Sinc5 + Averaging Filter, V_{REF} = 2.5V

DR[7:0]	DATA RATE (SPS)	INPUT BUFFER	GAIN							
			1	2	4	8	16	32	64	128
00000011b	1.25	On Off	0.151 (26.0) 0.156 (25.9)	0.091 (25.7) 0.082 (25.9)	0.062 (25.3) 0.039 (25.9)	0.048 (24.6) 0.025 (25.6)	0.030 (24.3) 0.016 (25.2)	0.022 (23.7) 0.009 (25.0)	0.022 (22.8) 0.010 (23.9)	0.022 (21.8) 0.010 (22.9)
00010011b	2.5	On Off	0.211 (25.5) 0.218 (25.5)	0.135 (25.1) 0.109 (25.5)	0.088 (24.7) 0.065 (25.2)	0.073 (24.0) 0.040 (24.9)	0.044 (23.8) 0.028 (24.4)	0.031 (23.2) 0.014 (24.5)	0.030 (22.3) 0.013 (23.6)	0.030 (21.3) 0.013 (22.6)
00100011b	5	On Off	0.310 (24.9) 0.290 (25.0)	0.177 (24.8) 0.156 (24.9)	0.135 (24.1) 0.084 (24.8)	0.096 (23.6) 0.050 (24.6)	0.067 (23.2) 0.035 (24.1)	0.044 (22.8) 0.018 (24.0)	0.044 (21.8) 0.018 (23.0)	0.044 (20.8) 0.018 (22.0)
00110011b	7.5	On Off	0.370 (24.7) 0.313 (24.9)	0.219 (24.4) 0.167 (24.8)	0.152 (24.0) 0.105 (24.5)	0.112 (23.4) 0.060 (24.3)	0.083 (22.8) 0.045 (23.7)	0.049 (22.6) 0.021 (23.8)	0.049 (21.6) 0.021 (22.9)	0.049 (20.6) 0.021 (21.9)
01000011b	12.5	On Off	0.482 (24.3) 0.422 (24.5)	0.249 (24.3) 0.239 (24.3)	0.229 (23.4) 0.134 (24.1)	0.136 (23.1) 0.082 (23.9)	0.111 (22.4) 0.050 (23.5)	0.063 (22.3) 0.026 (23.5)	0.063 (21.2) 0.026 (22.4)	0.063 (20.2) 0.026 (21.4)
01010011b	15	On Off	0.515 (24.2) 0.475 (24.3)	0.326 (23.9) 0.267 (24.2)	0.227 (23.4) 0.138 (24.1)	0.157 (22.9) 0.086 (23.8)	0.114 (22.4) 0.055 (23.4)	0.075 (22.0) 0.030 (23.3)	0.075 (21.1) 0.030 (22.2)	0.075 (20.1) 0.030 (21.3)
01100011b	25	On Off	0.653 (23.9) 0.609 (24.0)	0.390 (23.6) 0.352 (23.8)	0.279 (23.1) 0.189 (23.7)	0.215 (22.5) 0.120 (23.3)	0.151 (22.0) 0.080 (22.9)	0.095 (21.6) 0.039 (22.9)	0.095 (20.7) 0.039 (22.0)	0.095 (19.7) 0.039 (21.0)

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Table 9-9. Input-Referred Noise (e_n - μV_{RMS}) and Effective Resolution (bits), Low-Speed Mode, Sinc5 + Averaging Filter, V_{REF} = 2.5V (continued)

DR[7:0]	DATA RATE (SPS)	INPUT BUFFER	GAIN							
			1	2	4	8	16	32	64	128
01110010b	30	On Off	0.727 (23.7) 0.711 (23.7)	0.431 (23.5) 0.371 (23.7)	0.295 (23.0) 0.210 (23.5)	0.231 (22.4) 0.130 (23.2)	0.158 (21.9) 0.087 (22.8)	0.100 (21.6) 0.042 (22.8)	0.100 (20.6) 0.042 (21.9)	0.100 (19.6) 0.042 (20.8)
10000010b	50	On Off	0.975 (23.3) 0.929 (23.4)	0.535 (23.2) 0.460 (23.4)	0.409 (22.5) 0.253 (23.2)	0.252 (22.2) 0.177 (22.7)	0.221 (21.4) 0.098 (22.6)	0.125 (21.3) 0.054 (22.4)	0.125 (20.3) 0.054 (21.5)	0.125 (19.3) 0.054 (20.5)
10010010b	250	On Off	2.07 (22.2) 2.00 (22.3)	1.23 (22.0) 1.05 (22.2)	0.928 (21.4) 0.619 (21.9)	0.628 (20.9) 0.345 (21.8)	0.481 (20.3) 0.239 (21.3)	0.289 (20.1) 0.123 (21.3)	0.289 (19.0) 0.123 (20.3)	0.289 (18.1) 0.123 (19.3)
10100001b	500	On Off	2.88 (21.7) 2.82 (21.8)	1.79 (21.4) 1.37 (21.8)	1.27 (20.9) 0.841 (21.5)	0.949 (20.3) 0.503 (21.2)	0.675 (19.8) 0.334 (20.8)	0.398 (19.6) 0.171 (20.8)	0.399 (18.6) 0.171 (19.8)	0.399 (17.6) 0.171 (18.8)
10110000b	1000	On Off	3.98 (21.3) 3.80 (21.3)	2.45 (21.0) 2.03 (21.2)	1.73 (20.5) 1.12 (21.1)	1.29 (19.9) 0.704 (20.8)	0.942 (19.3) 0.462 (20.4)	0.565 (19.1) 0.235 (20.4)	0.565 (18.1) 0.235 (19.3)	0.565 (17.1) 0.235 (18.3)
11000000b	1875	On Off	5.43 (20.8) 5.18 (20.9)	3.36 (20.5) 2.72 (20.8)	2.35 (20.0) 1.54 (20.6)	1.68 (19.5) 0.965 (20.3)	1.26 (18.9) 0.635 (19.9)	0.753 (18.7) 0.317 (19.9)	0.753 (17.7) 0.317 (18.9)	0.756 (16.6) 0.317 (17.9)
11010000b	3750	On Off	7.36 (20.4) 6.77 (20.5)	4.53 (20.1) 3.73 (20.4)	3.22 (19.6) 2.11 (20.2)	2.31 (19.0) 1.26 (19.9)	1.67 (18.5) 0.856 (19.5)	1.02 (18.2) 0.430 (19.5)	1.02 (17.2) 0.430 (18.5)	1.02 (16.2) 0.430 (17.5)
11100000b	7500	On Off	9.28 (20.0) 8.69 (20.1)	5.72 (19.7) 4.67 (20.0)	4.02 (19.2) 2.69 (19.8)	2.89 (18.7) 1.63 (19.5)	2.13 (18.2) 1.06 (19.2)	1.29 (17.9) 0.540 (19.1)	1.29 (16.9) 0.540 (18.1)	1.29 (15.9) 0.540 (17.1)
11110000b	15,000	On Off	10.4 (19.9) 9.85 (20.0)	6.43 (19.6) 5.32 (19.8)	4.62 (19.0) 3.01 (19.7)	3.29 (18.5) 1.84 (19.4)	2.41 (18.0) 1.21 (19.0)	1.46 (17.7) 0.610 (19.0)	1.46 (16.7) 0.610 (18.0)	1.46 (15.7) 0.610 (17.0)
11110100b	30,000	On Off	15.3 (19.3) 14.1 (19.4)	9.32 (19.0) 7.86 (19.3)	6.50 (18.6) 4.42 (19.1)	4.73 (18.0) 2.65 (18.8)	3.39 (17.5) 1.72 (18.5)	2.03 (17.2) 0.871 (18.5)	2.03 (16.2) 0.871 (17.5)	2.03 (15.2) 0.871 (16.5)
11111000b	60,000	On Off	27.6 (18.5) 27.0 (18.5)	15.7 (18.3) 14.0 (18.4)	10.2 (17.9) 7.57 (18.3)	6.98 (17.4) 4.32 (18.1)	4.91 (17.0) 2.65 (17.8)	2.92 (16.7) 1.34 (17.8)	2.92 (15.7) 1.34 (16.8)	2.92 (14.7) 1.34 (15.8)
11111100b	80,000	On Off	54.6 (17.5) 54.1 (17.5)	28.8 (17.4) 27.7 (17.5)	16.2 (17.2) 14.2 (17.4)	9.79 (17.0) 7.48 (17.3)	6.32 (16.6) 4.15 (17.2)	3.64 (16.4) 2.08 (17.2)	3.64 (15.4) 2.08 (16.2)	3.64 (14.4) 2.08 (15.2)

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10 Detailed Description

10.1 Overview

The ADS125R1x are a family of high-performance 24-bit, delta-sigma (ΔΣ) analog-to-digital converters. The devices are available in leaded SSOP and leadless QFN packages with data rates up to 320kSPS.

The ADS125R11 supports one differential or two single-ended inputs with two general-purpose digital I/Os and crystal clock oscillator. The ADS125R13 supports three differential or five single-ended inputs and is available in a small 2mm × 2mm X2QFN package. The ADS125R14 supports four differential or eight single-ended inputs with four general-purpose digital I/Os and crystal clock oscillator. The ADS125R11 and ADS125R14 are performance upgrades to the ADS1255 and ADS1256 ADCs.

Figure 10-1 through Figure 10-3 show the functional block diagrams of the devices.

The input multiplexer selects the input channels for measurement in any combination of single-ended or differential-input connections. Current sources within the multiplexer allow detection of open- or short-circuit conditions of the external sensor. The input buffer greatly increases the input impedance to reduce loading of the sensor. With gains of 1, 2, 4, 8, 16, 32, 64 and 128, the low-noise PGA extends the dynamic range of the ADC.

The modulator measures the differential input signal against the external reference voltage with a transfer function given by $V_{IN} = \pm 2V_{REF}/Gain$. The modulator shapes the quantization noise to an out-of-band frequency range where the noise is reduced by the digital filter. For most data rates, noise remaining within the signal band is thermal noise with constant density. Programmable speed modes and data rates provide trade-offs between resolution, bandwidth, and power consumption.

The digital filter decimates and filters the modulator data to produce the high-resolution final output data. Filter options include sinc4 or sinc5 filters followed by a post-averaging filter, or a sinc3 filter to optimize rejection of line-cycle interference signals. A 32-bit data option eliminates the effects of quantization error when programmed for slow data rates with high resolution.

Self and system calibration commands correct initial gain and offset errors, errors after changing ADC configurations and errors over-temperature. The autozero mode tracks offset voltage drift over time and temperature without the need for calibration.

The devices support internal and external clock options. The clock options are 7.68MHz internal oscillator, external clock input or crystal oscillator (not available for ADS125R13). The clock divider pre-scales the modulator clock frequency to match the selected ADC speed range.

The SPI-compatible serial interface is used to program the ADC and read conversion data. The SPI can be configured to operate with as little as two wires or with four wires for full SPI compatibility. Integrated cyclic redundancy check (CRC) for communication and CRC for the SPI registers improve system-level reliability.

The $\overline{\text{DRDY}}$ pin (DOUT/$\overline{\text{DRDY}}$ for ADS125R13) signals when conversion data are ready. The $\overline{\text{SYNC}}$/$\overline{\text{PWDN}}$ pin of the ADS125R11 and ADS125R14 synchronizes conversions. Holding the pin low powers-down the ADC. The active-low $\overline{\text{RESET}}$ pin resets the ADC. Synchronization and reset functionality are also available through the SPI.

The general-purpose digital I/Os of the ADS125R11 and ADS125R14 provide static read/write control of up to four digital pins. The D0/CLKOUT general-purpose pin provides a clock output signal to synchronize conversions of other ADCs. The D1/$\overline{\text{ERROR}}$ pin provides an error output signal when an internal error is detected.

Power supply voltage AVDD powers the analog circuit and supply voltage DVDD powers the digital circuit and also the powers the digital I/O power. The ADS125R13 combines the analog and digital power supplies into one pin (VDD).

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10.2 Functional Block Diagrams

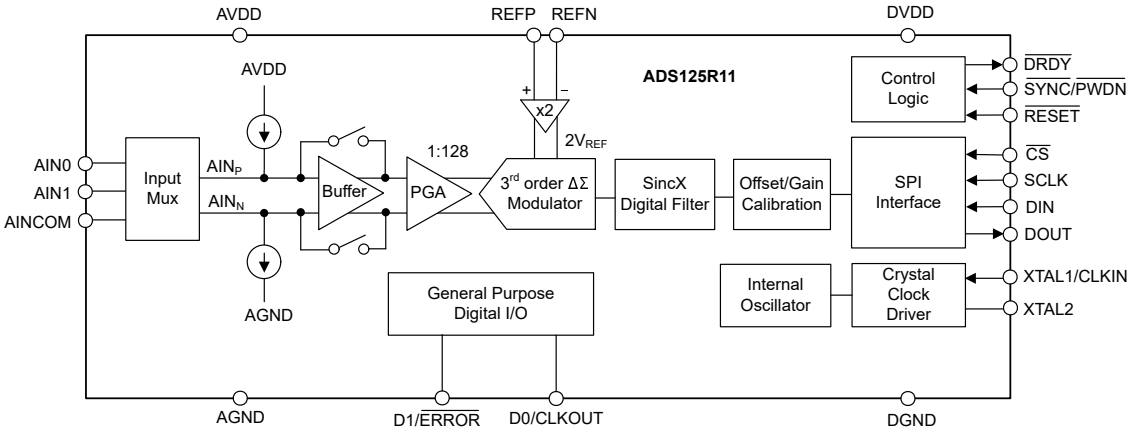


Figure 10-1. ADS125R11

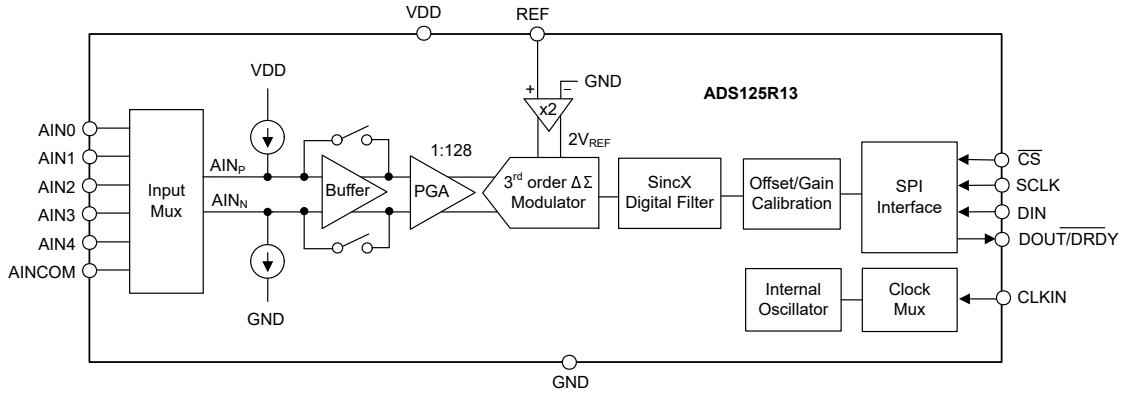


Figure 10-2. ADS125R13

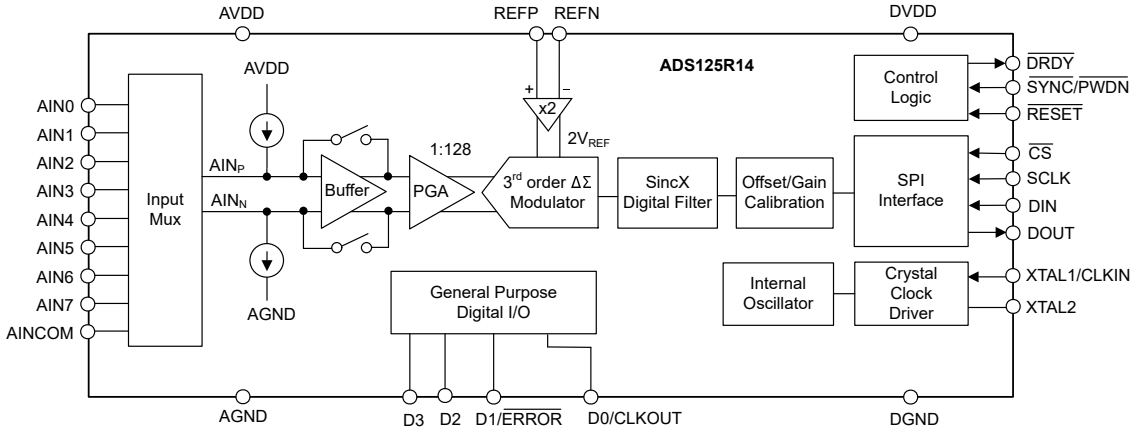


Figure 10-3. ADS125R14

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10.3 Feature Description

10.3.1 Analog Inputs

The ADCs signal range is V_{IN} = ±2V_{REF}/Gain, where V_{IN} is the difference voltage of two analog inputs. See the Recommended Operating Conditions section for details of the allowed signal range with and without buffer operation.

Figure 10-4 shows the simplified diagram of the analog input multiplexer.

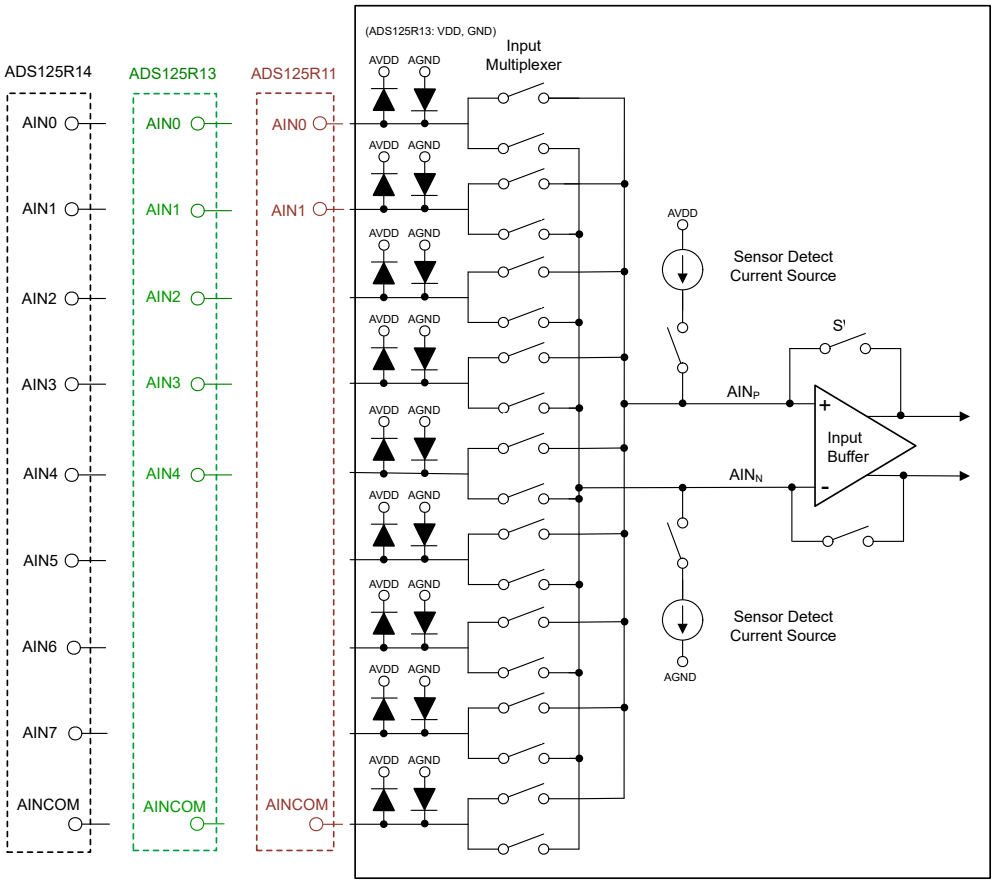


Figure 10-4. Analog Input Circuit

Diodes protect the analog inputs from electrostatic discharge (ESD). The diodes are designed to protect against ESD events that can occur during the manufacturing process and during printed circuit board (PCB) assembly when manufactured in an ESD-controlled environment. If the inputs are driven below AGND – 0.3V, or above AVDD + 0.3V (GND and VDD for ADS125R13), the protection diodes potentially conduct. If these conditions are possible, use external clamp diodes, series resistors, or both to limit the input current to the specified value.

In general, there are no restrictions on the analog input selection. That is, any pin can be selected as the positive ADC input (AIN_P) and any pin can be selected as the negative ADC input (AIN_N). AINCOM is functionally identical to the other analog inputs and can be used as a positive signal input or designated as the common input for signal-ended measurements. Note that AINCOM does not need to be tied to ground. For example, AINCOM (as well as the other analog inputs) can be tied to a midpoint voltage such as +2.5V.

The ADS125R14 provides nine analog channels, supporting four differential inputs, eight single-ended inputs, or a combination of differential and single-ended inputs. The ADS125R13 provides six analog channels, supporting three differential input or five single-ended inputs. The ADS125R11 provides three analog channels supporting one differential input or two single-ended inputs. The PSEL[3:0] bits of the MUX register select the positive input

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and the NSEL[3:0] bits select the negative input. To minimize input current of active channels, tie unused inputs to ground or leave floating. Make sure to only select the valid channels available for each ADC.

10.3.2 Sensor Detect Current Sources

The sensor detect current sources (SDCS) are used to verify the integrity of the external sensor connected to the ADC inputs. When enabled, the SDCS source and sink currents through the input multiplexer to the external sensor. The SDCS[1:0] bits of the ADCON register program the currents. The currents are: off, 0.5µA, 2µA, or 10µA.

Figure 10-5 shows the simplified diagram of ADC input structure with the external sensor modeled as resistance R_{SENS} between two input pins. When the current sources are enabled (arrows indicate enabled switch positions), a positive current is sourced to the input pin connected to AIN_P and a negative current sourced from the input pin connected to AIN_N. The two series resistors, R_{MUX}, model the ADC internal multiplexer resistance that ranges from 15Ω to 100Ω depending on the analog supply voltage and ambient temperature. The signal measured when the current sources are active equals the total IR drop: $I_{SDC} \times (2R_{MUX} + R_{SENS})$. Note that when the sensor is a direct short (that is, $R_{SENS} = 0$), there is still a small signal measured by the ADC: $I_{SDC} \times 2R_{MUX}$. Therefore, when the current sources are active during normal sensor measurements, an offset error occurs. To avoid the offset error, enable the current sources only when performing sensor diagnostics.

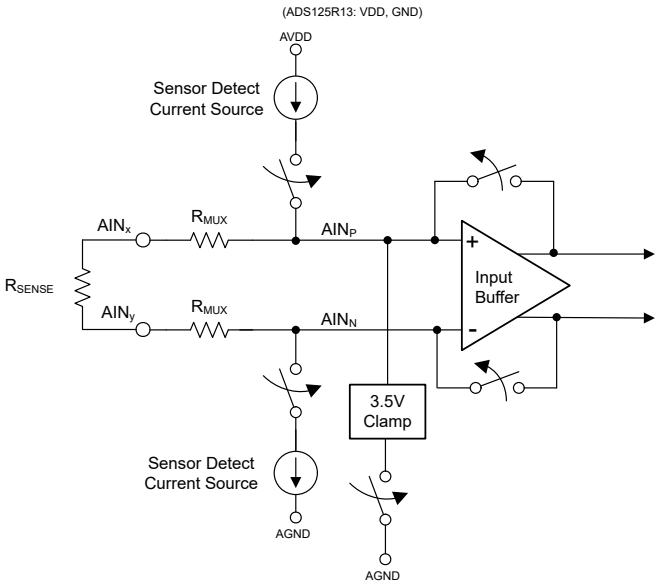


Figure 10-5. Sensor Detect Circuit

When the current sources are enabled, the analog input buffer is automatically active regardless of whether the input buffer is enabled or not. This is done to prevent the modulator input current from loading the current sources. When the current sources are active, the internal AIN_P must stay below 3.5V to be within the absolute input range of the buffer. To verify this condition is met, an internal 3.5V clamp circuit starts sinking current from AIN_P to AGND. Note that this clamp is active only when the current sources are enabled.

10.3.3 Input Buffer

A low-drift, chopper-stabilized input buffer is available to increase the input impedance presented by the ADC. The buffer is enabled by the BUFEN bit of the STATUS register. When the input buffer is enabled, the voltage on the analog inputs with respect to ground must remain between AGND – 0.05V and AVDD − 1.45V (GND – 0.05V and VDD − 1.45V for ADS125R13). Exceeding this range reduces performance, in particular the linearity of the converter. When performing self gain calibration the reference voltage is internally connected to the buffer inputs, therefore this same voltage range limitation applies to the reference inputs.

The input buffer is chopper-stabilized to reduce 1/f noise and offset drift. The switching effects caused by the input buffer chopping places a finite value on the input impedance which is modeled by an effective resistance,

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Z_{IN}, as shown in Figure 10-6. The buffer input impedance is a function of data rate, autozero mode and temperature. Figure 8-3 through Figure 8-5 show the buffer input impedance.

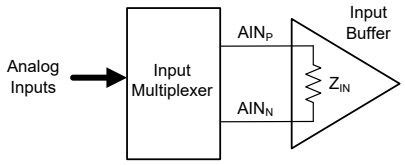


Figure 10-6. Buffer Effective Input Impedance (Z_{IN})

10.3.4 Delta-Sigma Modulator

The delta-sigma modulator is a switched-capacitor, third-order architecture that achieves excellent noise and linearity performance with low power consumption.

The modulator measures the input signal using sample capacitors that are continuously charged and discharged. Figure 10-7 shows a simplified schematic of the ADS125R1x modulator input sampling circuit. Figure 10-8 shows the on/off timings of the switches. Switches S_1 are closed during the input sampling phase. In this phase, C_{A1} charges to V_{AINP}, C_{A2} charges to V_{AINN}, and C_B charges to the difference of V_{AINP} and V_{AINN} by the analog input signal. For the discharge phase, S_1 opens first and then S_2 closes. C_{A1} and C_{A2} discharge to approximately AVDD/2 (ADS125R13 VDD/2) and C_B discharges to 0V. This two-phase sample/discharge cycle repeats at a period of t_{SAMPLE}. As shown in Table 10-1, the sample period and the sample capacitors are functions of the PGA gain.

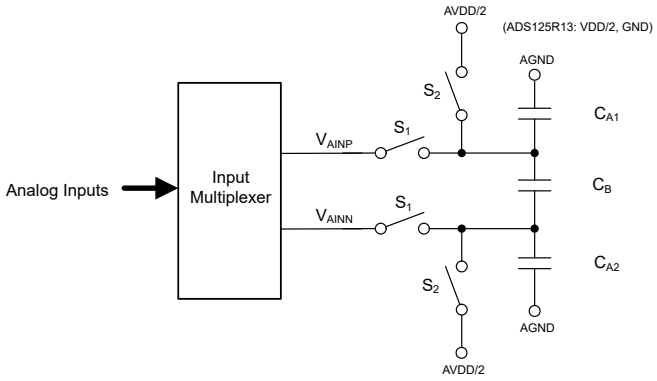


Figure 10-7. Simplified Modulator Input Circuit

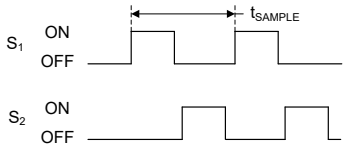


Figure 10-8. Modulator Switch Timing

Table 10-1. Input Sampling Period With C_A, C_BValues

MODULATOR GAIN	t_{SAMPLE}	C_{A1}, C_{A2} (pF)	C_B (pF)
1	1 / f_{MOD}	2.1	2.4
2	1 / f_{MOD}	4.2	4.9
4	1 / f_{MOD}	8.3	9.7
8	1 / f_{MOD}	17	19
16	1 / f_{MOD}	33	39

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Table 10-1. Input Sampling Period With C_A, C_BValues (continued)

MODULATOR GAIN	t_{SAMPLE}	C_{A1}, C_{A2} (pF)	C_B (pF)
32	1 / 2f_{MOD}	52	58
64	1 / 2f_{MOD}	52	58
128	1 / 2f_{MOD}	52	58

Charging of the input capacitors draws a transient current when switch S_1 is closed. This results in a kick-back voltage. For best linearity performance, the external driving circuit charging the sampling capacitor must settle to the final voltage before the end of the sampling phase.

The average value of the transient current is useful to derive an effective input impedance Z_{IN}, where $Z_{IN} = V_{IN} / I_{AVERAGE}$. Figure 10-9 shows the switched capacitors of Figure 10-7 replaced by effective input impedances. The common mode input impedance of the modulator is Z_A. The differential mode input impedance (Z_{IN}) is Z_B || 2Z_A. The impedances scale inversely with the modulator frequency. For example, if f_{MOD} is reduced by a factor of two, the impedances double. Figure 8-1 shows the modulator input impedance as a function of gain at 30kSPS data rate.

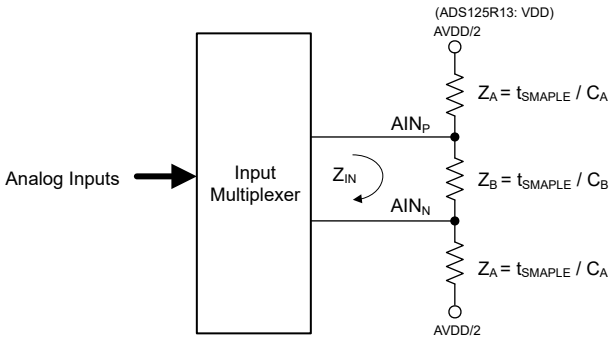


Figure 10-9. Modulator Input Impedance Model

10.3.4.1 PGA Gain

The PGA provides programmable voltage gains that extend the dynamic range of the ADC. The gains are binary 1 to 128, with the input range defined by: ±2V_{REF}/Gain. For optimal resolution, program the gain to the highest possible value based on the expected input signal while avoiding over-ranging the ADC inputs. For example, for V_{REF} = 2.5V, if the largest signal to be measured is 1V, gain = 4 is optimum because resultant input range is ±1.25V. Gains greater than 4 results in incorrect conversion results. Table 10-2 shows the input voltage range versus PGA gain. Note the input ranges shown in the table are with input buffer off. See the Input Buffer section for details of the buffer input range,

Table 10-2. Input Voltage Range

PGA GAIN	INPUT VOLTAGE RANGE (BUFFER OFF)	
	V_{REF} = 2.5V	V_{REF} = 5V
1	±5V	±5V(1)
2	±2.5V	±5V
4	±1.25V	±2.5V
8	±0.625V	±1.25V
16	±312.5mV	±0.625V
32	±156.25mV	±312.5mV
64	±78.125mV	±156.25mV
128	±39.0625mV	±78.125mV

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1. The input range is limited to ±5V for V_{REF} = 5V and PGA gain = 1.

PGA gain is programmed by the PGA[2:0] bits of the ADCON register. Recalibrating the A/D converter after changing the gain is recommended. The self-calibration time depends on the data rate. See the Calibration Time section for details.

10.3.5 Reference Voltage

The ADC requires a reference voltage for operation. The reference voltage is the voltage between the REFP and REFN pins as defined by: $V_{REF} = V_{REFP} - V_{REFN}$. The reference voltage for the ADS125R13 is the voltage between the REF and GND pins. The reference inputs use a structure similar to that of the modulator inputs. Figure 10-10 and Figure 10-11 show simplified models of reference input circuit.

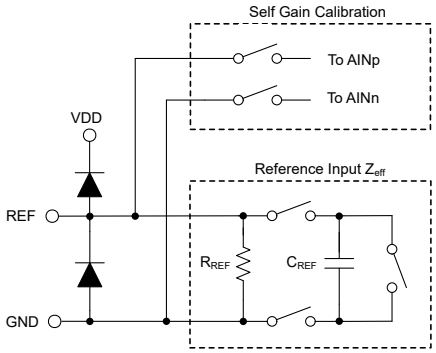


Figure 10-10. Reference Input Sampling Circuit (ADS125R13)

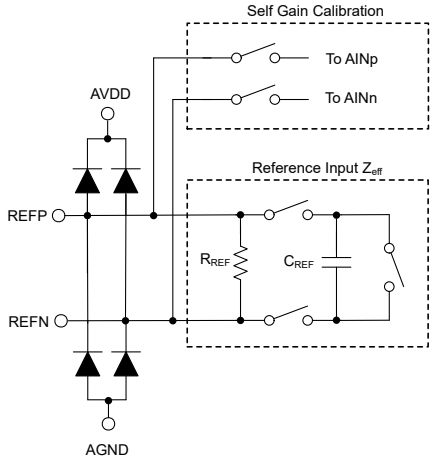


Figure 10-11. Reference Input Sampling Circuit (ADS125R11, ADS125R14)

ESD diodes protect the reference inputs. Make sure the voltages on the reference pins do not go below AGND by more than 0.3V, or above AVDD by 0.3V. For the ADS125R13, make sure the voltage on the REF pin does not go below GND by more than 0.3V, or above VDD by 0.3V. These restrictions keep the ESD diodes from turning on. If out-of-range voltages are possible, use external clamp diodes, series resistors, or both to limit the input current to the specified value.

Because of the current transients caused by the charging of C_{REF} at period = t_{SAMPLE} (1 fMOD), a voltage reference capable of driving the reference sampling circuit is essential to achieve best performance. Many types of voltage references require an external buffer to drive the reference sampling circuit. See the Application Information section for information of a voltage reference with an integrated buffer. The average input current presented by charging the reference capacitor along with the fixed resistance are modeled by an effective impedance (Z_{REF}). Part of Z_{REF} scales inversely with the modulator frequency (f_{MOD}) due to charging of C_{REF} and part of Z_{REF} is due to R_{REF}.

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During self gain calibration, the reference voltage is connected to AINp and AINn. If the input buffer is disabled, the reference pins are driving an additional load from the modulator input. Make sure the voltage reference can drive this additional load. When the buffer is enabled, the reference loading is much less, but the buffer limits the allowable voltage range of the reference input. The reference input voltage must remain within the input range of the buffer to produce a valid self-gain calibration.

10.3.6 Digital Filter

The digital filter averages and decimates the data of the modulator to produce high-resolution final output data. By adjusting the amount of filtering, tradeoffs are available between resolution and data rate: filter more for higher resolution, filter less for higher data rate.

The digital filter topology is a cascaded-integrator-comb (CIC) topology that minimizes the delay (latency) of the data as the data propagates through the filter stages. The CIC filter is also known as a sinc filter because of the characteristic sinx/x (sinc) frequency response.

Figure 10-12 shows the digital filter diagram. Three types of filters are available: sinc5 + averager, sinc4 + averager and a sinc3 filter without averager. The sinc5 + averager and the sinc4 + averager filters have similar frequency response profiles with the difference the sinc5 + averager provides overall lower noise while the sinc4 + averager has shorter settling time and wider signal bandwidth. At equivalent data rates, the sinc3 filter provides the best noise performance and line frequency rejection, but with increased settling time and lower signal bandwidth.

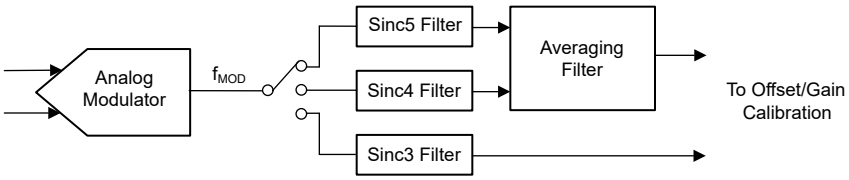


Figure 10-12. Digital Filter Block Diagram

The digital filter type is programmed by bits FILTR[1:0] of register CONFIG0 and the data rate is programmed by bits DR[7:0] of register DRATE. Oversampling ratio (OSR) is the amount of filtering and data rate reduction of modulator data performed by the filter to provide output data. Overall OSR is the product of the first stage OSR (M) and the second stage number of averages. Table 10-3 and Table 10-4 show the OSR and averaging factor of the filter. Be sure to select only the valid DR[7:0] bits of each filter type. When the sinc3 filter is selected use the DR[7:0] values of Table 10-3.

Table 10-3. Data Rates for Sinc3 Filter

DR[7:0]	OSR (M)	DATA RATE (SPS)		
		HIGH-SPEED MODE	MID-SPEED MODE	LOW-SPEED MODE
10110000b	2400	1,600	800	400
10100000b	4800	800	400	200
10010000b	9600	400	200	100
10000000b	16000	240	120	60
01110000b	19200	200	100	50
01100000b	32000	120	60	30
01010000b	38400	100	50	25
01000000b	64000	60	30	15
00110000b	76800	50	25	12.5
00100000b	96000	40	20	10
00010000b	192000	20	10	5
00000000b	384000	10	5	2.5

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Table 10-4. Data Rates for Sinc4 and Sinc5 (+ Averaging Filter)

DR[7:0]	OVERALL OSR	SINC OSR (M)	NUMBER OF AVERAGES (n)	DATA RATE (SPS)		
				HIGH-SPEED MODE	MID-SPEED MODE	LOW-SPEED MODE
11111100b	12	12	1	320,000	160,000	80,000
11111000b	16	16	1	240,000	120,000	60,000
11110100b	32	32	1	120,000	60,000	30,000
11110000b	64	64	1	60,000	30,000	15,000
11100000b	128	64	2	30,000	15,000	7,500
11010000b	256	64	4	15,000	7,500	3,750
11000000b	512	64	8	7,500	3,750	1,875
10110001b	960	64	15	4,000	2,000	1,000
10100010b	1920	64	30	2,000	1,000	500
10010010b	3840	64	60	1,000	500	250
10000010b	19200	64	300	200	100	50
01110010b	32000	64	500	120	60	30
01100011b	38400	64	600	100	50	25
01010011b	64000	64	1000	60	30	15
01000011b	76800	64	1200	50	25	12.5
00110011b	128000	64	2000	30	15	7.5
00100011b	192000	64	3000	20	10	5
00010011b	384000	64	6000	10	5	2.5
00000011b	768000	64	12000	5	2.5	1.25

10.3.6.1 Frequency Response

The digital filter establishes the overall frequency response of the ADC. For the sinc5 and sinc4 (+ averager) filters, the frequency response is the product of the first and second stages, as shown by Equation 10. For the sinc3 filter, the frequency response is from the first stage filter only (averager bypassed).

$$\left|H_{(f)}\right| = \left| \frac{\sin\left[\frac{\pi f M}{f_{MOD}}\right]}{M \cdot \sin\left[\frac{\pi f}{f_{MOD}}\right]} \right|^{x} \cdot \left| \frac{\sin\left[\frac{64 n \pi f}{f_{MOD}}\right]}{n \cdot \sin\left[\frac{64 \pi f}{f_{MOD}}\right]} \right| \quad (10)$$

where:

- f = signal frequency
- f_{MOD} = modulator frequency
- M = first stage decimation (Table 10-4 and Table 10-3)
- x = order of first stage (3, 4, or 5)
- n = number of averages of second stage (Table 10-4)

The digital filter attenuates noise of the modulator, including noise from within the ADC and external noise present on the input signal. Changing the sinc filter decimation and changing the number of averages changes the data rate and the signal bandwidth. Higher values of these parameters reduces signal bandwidth which correspondingly reduces noise.

The digital filter has frequency response notches (or zeros) at the output data rate, and multiples thereof. At these frequencies, the filter has zero gain. This feature can be useful when trying to eliminate a particular interference signal. For example, to eliminate 50Hz interference and harmonics, set the data rate to 50SPS or a sub-multiple of 50SPS, such as 10SPS. Figure 10-13 shows the frequency-normalized response of the sinc3, sinc4 and sinc5 (without averaging filter). Figure 10-14 shows the frequency response of the sinc5 + averaging filter at 2.5SPS. At the lower data rates such as 2.5SPS, the averaging filter determines the frequency response.

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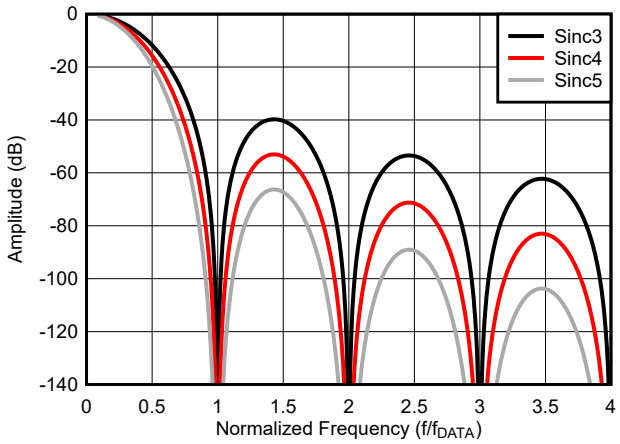


Figure 10-13. Sincx Filter Frequency Responses (Sinc4/5 Without Averaging Filter)

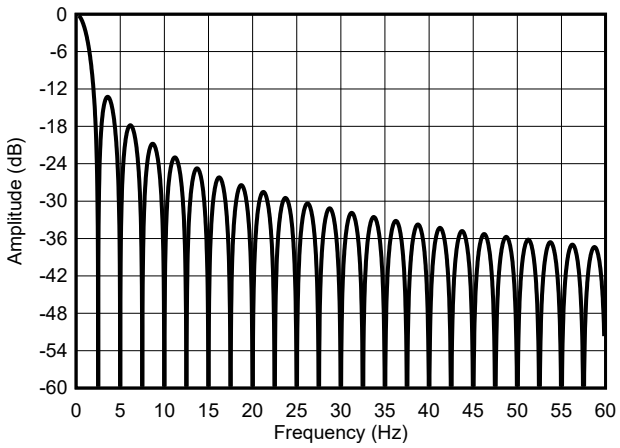


Figure 10-14. Sinc4/5 Filter Frequency Response (2.5SPS)

Figure 10-15 shows the rejection of a 50Hz input signal at 50SPS for the various filter types. The frequency response of 60SPS is similar but with new notches present at 60Hz, 120Hz and so on. The sinc3 filter type provides the widest and deepest notch at 50Hz and 60Hz for best noise rejection.

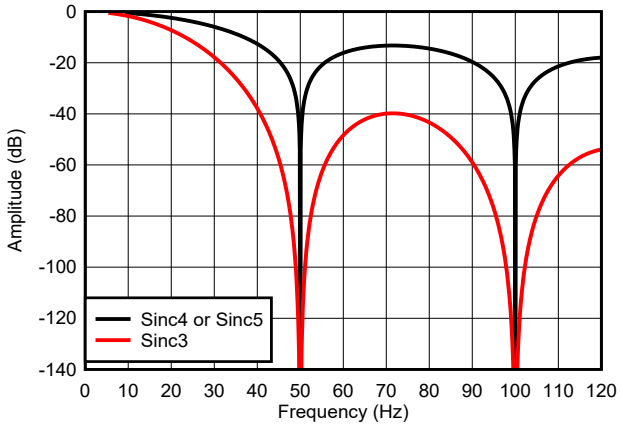


Figure 10-15. 50SPS Frequency Response

Table 10-5 shows the Normal Mode Rejection Ratio (NMRR) with 2% and 6% difference between the signal frequency and the digital filter notch frequency (expressed as Δf). Note for a given data rate, the sinc3 filter provides improves NMRR in comparison to the sinc4 and sinc5 averaging filters.

Table 10-5. Normal Mode Rejection Ratio

DATA RATE (SPS)	50Hz REJECTION				60Hz REJECTION				400Hz REJECTION			
	SINC3 FILTER		SINC4 and SINC5 FILTER		SINC3 FILTER		SINC4 and SINC5 FILTER		SINC3 FILTER		SINC4 and SINC5 FILTER	
	2% Δf	6% Δf	2% Δf	6% Δf	2% Δf	6% Δf	2% Δf	6% Δf	2% Δf	6% Δf	2% Δf	6% Δf
10	102dB	75dB	34dB	25dB	104dB	77dB	34dB	25dB	139dB	125dB	46dB	42dB
50	101dB	71dB	33dB	24dB	50dB	57dB	17dB	19dB	102dB	82dB	34dB	27dB
60	40dB	35dB	13dB	12dB	106dB	71dB	33dB	24dB	78dB	85dB	26dB	28dB
400	<1dB								101dB	71dB	33dB(1)	24dB(1)

(1) For sinc4 and sinc5 averaging filters, the ADC clock frequency scaled to yield 400SPS from the 500SPS setting

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The frequency response of the filter repeats at multiples of the modulator frequency (f_{MOD}). Figure 10-16 shows the response out to 7.68MHz for mid-speed mode. Notice how the responses near DC, 1.92MHz, 3.84MHz, 5.76MHz, 7.68MHz are the same. The digital filter attenuates signals and noise on the ADC inputs up to the frequency where the response repeats. However, signals and noise at multiples of f_{MOD} alias to the original filter pass band. If signals or noise are present, remove these with external filtering. In many cases, a simple RC filter at the inputs is sufficient to remove the noise.

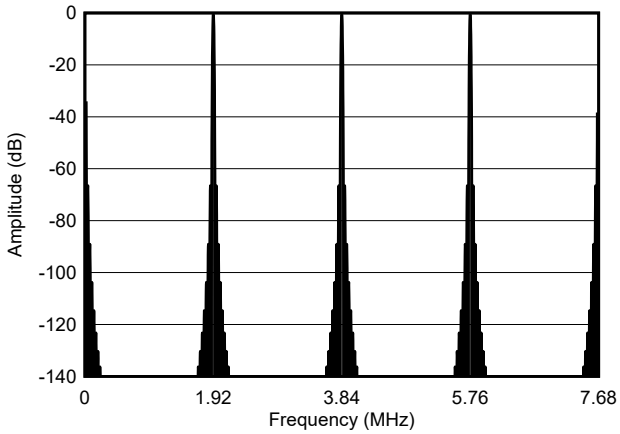


Figure 10-16. 30kSPS Frequency Response out to 7.68MHz (Mid-Speed Mode)

The bandwidth of the ADC depends on the data rate and the filter type. Table 10-6 lists the –3dB bandwidth of the filters. The bandwidth listed in the table exclude analog filters used in the signal path.

Table 10-6. Digital Filter Bandwidth

DATA RATE (SPS)			-3dB BANDWIDTH (Hz)	
HIGH-SPEED MODE	MID-SPEED MODE	LOW-SPEED MODE	SINC5	SINC4
320,000	160,000	80,000	$0.204f_{DATA}$	$0.227f_{DATA}$
240,000	120,000	60,000	$0.204f_{DATA}$	$0.227f_{DATA}$
120,000	60,000	30,000	$0.204f_{DATA}$	$0.227f_{DATA}$
60,000	30,000	15,000	$0.204f_{DATA}$	$0.227f_{DATA}$
30,000	15,000	7,500	$0.321f_{DATA}$	$0.341f_{DATA}$
15,000	7,500	3,750	$0.400f_{DATA}$	$0.411f_{DATA}$
7,500	3,750	1,875	$0.431f_{DATA}$	$0.435f_{DATA}$
4,000	2,000	1,000	$0.439f_{DATA}$	$0.440f_{DATA}$
2,000	1,000	500	$0.442f_{DATA}$	
1,000	500	250		
200	100	50		
120	60	30		
100	50	25		
60	30	15		
50	25	12.5		
30	15	7.5		
20	10	5		
10	5	2.5		
5	2.5	1.25		
All data rates of sinc3 filter			$0.262f_{DATA}$	

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10.3.6.2 Settling Time

Settling time is the time required for a signal to propagate through the digital filter which depends on the filter type and order. Table 10-7 and Table 10-8 show the filter settling times (t_{SET}) after synchronizing the ADC to a step-change input. In multiplexed input systems, the settling time determines total data throughput when scanning through channels. Settling time scales with clock frequency. Note an additional delay 2050/f_{MOD} occurs when exiting the power down mode.

Table 10-7. Settling time for Sinc3 Filter (DELAY[3:0] = 0000b)

HIGH-SPEED MODE		MID-SPEED MODE		LOW-SPEED MODE	
DATA RATE (SPS)	t_{SET} (µs)	DATA RATE (SPS)	t_{SET} (µs)	DATA RATE (SPS)	t_{SET} (µs)
1,600	1898	800	3796	400	7591
800	3773	400	7546	200	15091
400	7523	200	15046	100	30091
240	12523	120	25046	60	50091
200	15023	100	30046	50	60091
120	25023	60	50046	30	100091
100	30023	50	60046	25	120091
60	50023	30	100046	15	200091
50	60023	25	120046	12.5	240091
40	75023	20	150046	10	300091
20	150023	10	300046	5	600091
10	300023	5	600046	2.5	1200091

Table 10-8. Setting Time for Sinc5 and Sinc4 Filters (DELAY[3:0] = 0000b)

HIGH-SPEED MODE		MID-SPEED MODE		LOW-SPEED MODE	
DATA RATE (SPS)	SINC5 / SINC4 t_{SET} (µs)	DATA RATE (SPS)	SINC5 / SINC4 t_{SET} (µs)	DATA RATE (SPS)	SINC5 / SINC4 t_{SET} (µs)
320,000	38 / 35	160,000	77 / 71	80,000	154 / 141
240,000	44 / 39	120,000	87 / 79	60,000	174 / 158
120,000	64 / 56	60,000	129 / 112	30,000	258 / 224
60,000	106 / 89	30,000	212 / 179	15,000	424 / 358
30,000	123 / 106	15,000	246 / 212	7,500	491 / 424
15,000	156 / 139	7,500	312 / 279	3,750	624 / 558
7,500	223 / 206	3,750	446 / 412	1,875	891 / 824
4,000	339 / 323	2,000	679 / 646	1,000	1358 / 1291
2,000	589 / 573	1,000	1179 / 1146	500	2358 / 2291
1,000	1089 / 1073	500	2179 / 2146	250	4358 / 4291
200	5089 / 5073	100	10179 / 10146	50	20358 / 20291
120	8423 / 8406	60	16846 / 16812	30	33691 / 33624
100	10089 / 10073	50	20179 / 20146	25	40358 / 40291
60	16756 / 16739	30	33512 / 33479	15	67024 / 66958
50	20089 / 20073	25	40179 / 40146	12.5	80358 / 80291
30	33423 / 33406	15	66846 / 66812	7.5	133691 / 133624
20	50089 / 50073	10	100179 / 100146	5	200358 / 200291
10	100089 / 100073	5	200179 / 200146	2.5	400358 / 400291
5	200089 / 200073	2.5	400179 / 400146	1.25	800358/ 800291

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10.3.7 GENERAL-PURPOSE I/O (D0D3)

General purpose, digital I/O pins are available for input/output of digital signals. The digital I/O are push-pull outputs relative to DVDD and DGND. The ADS125R14 has four digital I/O pins and the ADS125R11 has two digital I/O pins.

The DIRx bit field (direction) of the GPIO register configures the pins as inputs or outputs. The bits of the DIOx field (values) are the forcing output values (write), or the input values (read) of the pins. Reading the DIOx bits returns the state of the pins, whether the pins are configured as inputs or outputs.

The digital I/O pins default to inputs after power-up or reset, except for D0/CLKOUT, which defaults to the clock output signal. During Standby and Power down modes, pins programmed as outputs remain active. To prevent unused input pins from floating, use external pull-down resistors or configure the pins as outputs.

The D0/CLKOUT pin provides a clock out signal, overriding manual I/O control. See the D0/CLKOUT Pin section for details. The D1/$\overline{\text{ERROR}}$ pin is provides the ADC error output signal, also overriding manual I/O control. See the D1/$\overline{\text{ERROR}}$ Pin section for details.

10.3.8 D0/CLKOUT Pin

The D0/CLKOUT pin provides a clock output signal which is used to synchronize clocks of other ADCs in simultaneous-sampling systems. See Figure 10-18 for the internal clock routing. The CLK_OUT[1:0] bits of the ADCON register programs the output clock frequency. The default configuration is clock output CLK_OUT[1:0] = 01b ($f_{CLKOUT} = f_{CLKIN}$). CLK_OUT[1:0] = 00b disables the clock output, which places the pin under general-purpose I/O control.

10.3.9 D1/$\overline{\text{ERROR}}$ Pin

D1/$\overline{\text{ERROR}}$ is an error output pin that asserts low upon detection of an internal error. The error signal is the logic-OR of the STATUS1 register error flags ($\overline{\text{ADC_ERR}}$, $\overline{\text{REG_ERR}}$ and $\overline{\text{SPI_ERR}}$). The pin is normally high then drives low when one of the error bits are low (active). The pin remains low until all error flags are reset to 1, at which time the pin returns high. The error pin is enabled by the ERR_EN bit of the CONFIG1 register, otherwise the pin is under general purpose I/O control. Because the output is push-pull, do not connect together outputs from multiple devices.

Figure 10-17 shows the error flags of the STATUS1 register.

Figure 10-17. STATUS1 Register

7	6	5	4	3	2	1	0
RESERVED					$\overline{\text{ADC_ERR}}$	$\overline{\text{REG_ERR}}$	$\overline{\text{SPI_ERR}}$

- $\overline{\text{ADC_ERR}}$: Internal ADC error
  Cycle power or reset the device to clear the error. If the error remains, replace the device.
- $\overline{\text{REG_ERR}}$: Register-map CRC error
  Correct the CRC register or other register contents then write 1b to clear the error.
- $\overline{\text{SPI_ERR}}$: SPI CRC error.
  Write 1b to clear the error then check the results of the SPI operation that resulted in the error.

10.4 Device Functional Modes

10.4.1 Speed Modes

The ADC has three speed modes to optimize power consumption, data rate and resolution for the application requirement. The modes are high-speed, mid-speed and low-speed, selected by the MODE[1:0] bits of register CONFIG0. The modulator frequency (f_{MOD}) must be set according to the speed mode. The clock pre-scaler (CLK_DIV[1:0]) can be used to set the modulator frequency. See Table 10-9 for the modulator frequency of the speed modes.

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10.4.2 Clock Operation

The ADC supports internal or external clock operation. Figure 10-18 shows the internal clock tree. The clock multiplexer selects internal or external clock through the CLK_SRC bit of the CONFIG1 register. The output of the clock multiplexer connects to a clock divider which sets the modulator frequency (f_{MOD}). The divider is programmed by the CLKDIV[1:0] bits of the CONFIG1 register. The output of the clock multiplexer also connects to the clock output divider for the D0/CLKOUT pin.

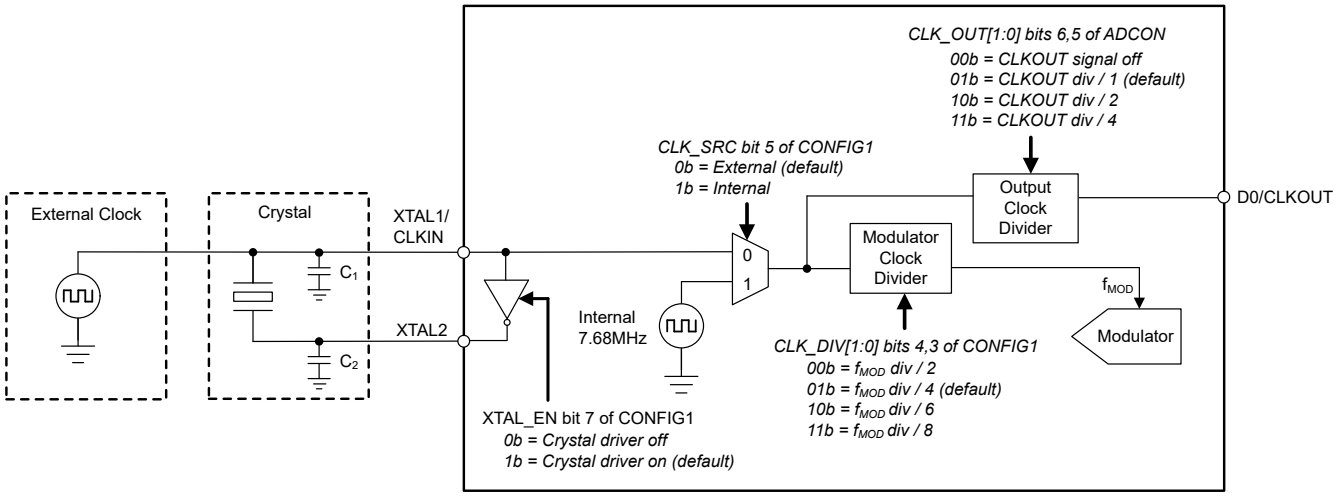


Figure 10-18. Clock Diagram

Table 10-9 shows example clock frequencies and CLK_DIV[1:0] bits to program the f_{MOD} frequency.

Table 10-9. Clock Frequencies

SPEED MODE	MAIN CLOCK FREQUENCY f_{OSC} or f_{CLKIN}	CLK_DIV[1:0]	MODULATOR FREQUENCY f_{MOD}
High	7.68MHz	00b = div 2	3.84MHz
Mid	7.68MHz	01b = div 4	1.92MHz
	3.84MHz	00b = div 2	
Low	7.68MHz	11b = div 8	0.96MHz
	3.84MHz	01b = div 4	
	1.92MHz	00b = div 2	

The modulator clock frequency can be slower to set specific data rates between the standard data rates. The noise performance at the new clock frequency is the same as the original clock frequency.

For external clock, program the CLK_SRC bit to 0b (default) and apply a clock signal to the XTAL1/CLKIN pin (with XTAL2 floating). ADC begins operation when the clock signal is applied. The clock signal must be free from glitches with low jitter. Excessive clock jitter can degrade SNR performance when measuring ac input signals. For example, if the signal input frequency is 20kHz, clock jitter must be no more than 100ps. Avoid ringing on the clock input. A series resistor placed at the clock output buffer driving the CLKIN pin often helps reduce ringing.

For external crystal operation, program the CLK_SRC bit to 0b and enable the crystal by the XTAL_EN bit of the CONFIG1 register (default = enabled). 256 clock cycles occurs before ADC operation starts to allow the crystal to fully stabilize after power-up. Figure 10-18 shows the crystal connection with load capacitors (C_1, C_2). Place the crystal and capacitors close to the ADC pins using short, direct traces. Avoid running other clock signals (microcontroller clock, SCLK signal and so forth) close to the crystal PCB traces. Neither the XTAL1/CLKIN nor XTAL2 pins can be used to drive any other circuit. Use the clock signal output of the D0/CLKOUT pin to synchronize the clock of other ADCs.

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Table 10-10 shows two crystals compatible with the ADS125R1x. Other compatible crystals depend on the electrical parameters of the crystal (frequency, ESR, C_O and C_L). Use the *ADS125R1x Crystal Calculator* to determine the compatibility of other crystals (TBD).

Table 10-10. Compatible Crystals

MANUFACTURER PART #	CRYSTAL FREQUENCY
ECS: ECS-76.8-18-5PX-XES	7.68MHz
CTS: TS-076F3-YID	3.84MHz

The ADC has an oscillator operating at 7.68MHz. Program the CLK_SRC bit = 1b to select the internal oscillator for operation. Divide the oscillator frequency using the internal clock divider to the modulator frequency of the speed modes. When changing clock modes from external to internal, an internal delay of 256 clock cycles allows for internal oscillator stabilization.

10.4.3 Synchronization

The ADC is synchronized on the rising edge of the $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ pin (available on ADS125R11 and ADS125R14) or by the SYNC command of SPI (available on all devices). Synchronization starts a new conversion cycle with output data withheld until the filter is fully settled. $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ can be tied high to free-run conversions. In this case, the ADC can be synchronized through the SYNC command.

As shown in Figure 10-19, $\overline{\text{DRDY}}$ is driven high when $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ is taken low. If held low for 20 $\overline{\text{DRDY}}$ periods, the device enters power down mode. When taken high, synchronization occurs on the next falling edge of CLKIN. $\overline{\text{DRDY}}$ drives low when the filter is fully settled (t_{SET}), which indicates conversion data are available to read. The data are fully settled - there is no need to ignore or discard data. See Table 10-8 and Table 10-7 for settling time data (t_{SET}). Note SPI communication is not possible on the serial interface while the pin $\overline{\text{SYNC}}/\overline{\text{PDWN}}$ pin is low.

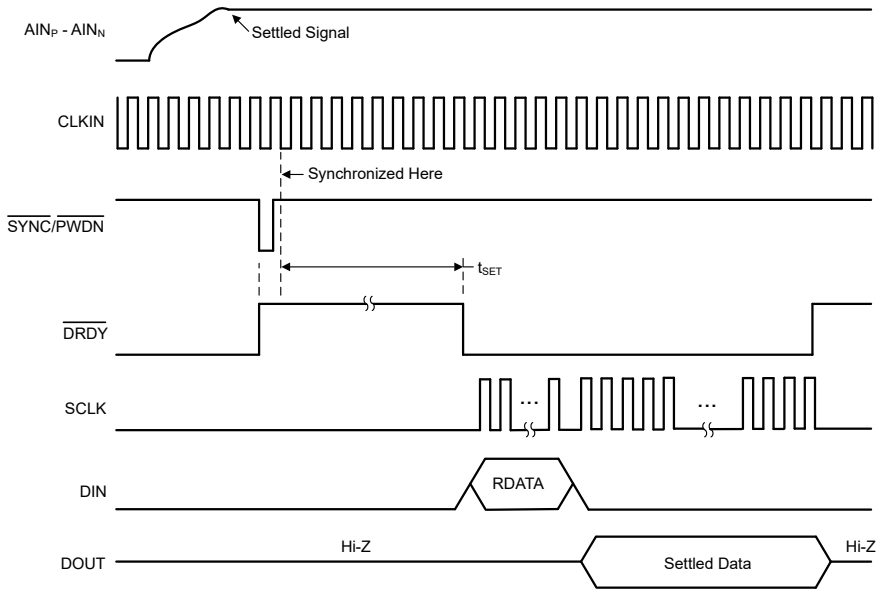


Figure 10-19. $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ Pin Synchronization (ADS125R11 and ADS125R14 Only)

To synchronize with the SYNC command, first shift-in the eight bits of the command. This stops conversions. When ready to synchronize, shift-in the WAKEUP command. Synchronization occurs on the rising edge of CLKIN after the first SCLK rising edge of the WAKEUP command. Fully settled data are available at time t_{SET} when $\overline{\text{DRDY}}$ falls low. Figure 10-20 shows the SYNC command for the ADS125R11 and ADS125R14. The ADS125R13 combines the functions of the DOUT and $\overline{\text{DRDY}}$ pins on the DOUT/$\overline{\text{DRDY}}$ pin. Keep the $\overline{\text{CS}}$ pin must be low to observe the low transition of DOUT/$\overline{\text{DRDY}}$.

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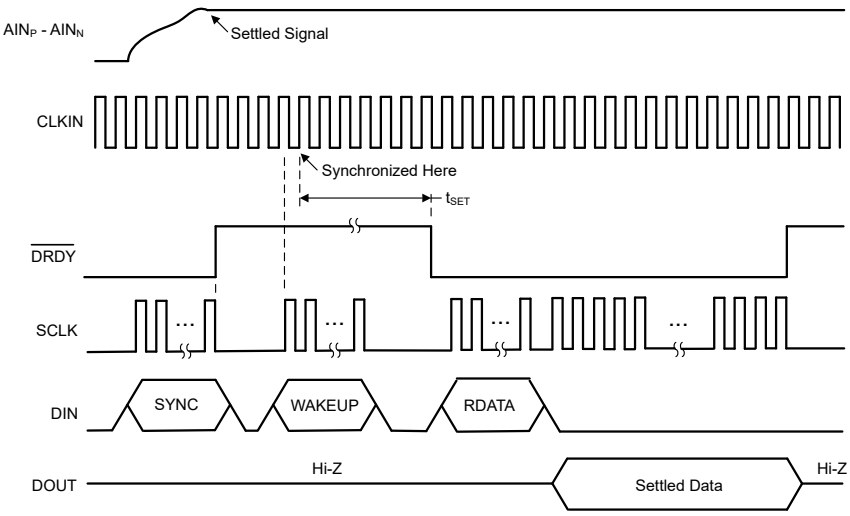


Figure 10-20. ADS125R11 and ADS125R14 SYNC Command Synchronization

10.4.3.1 Cycling Through the Inputs

The most efficient way to cycle through the inputs is to change the multiplexer (write to the MUX register) immediately after $\overline{\text{DRDY}}$ goes low. Then after changing the multiplexer, synchronize the conversion process by issuing the SYNC and WAKEUP commands, then retrieve the previous data with the RDATA command. Changing the multiplexer before reading the data allows the ADC to start measuring the new input channel sooner. Figure 10-21 demonstrates efficient input cycling. There is no need to ignore or discard data while cycling through the inputs because the ADC provides fully settled data when $\overline{\text{DRDY}}$ goes low.

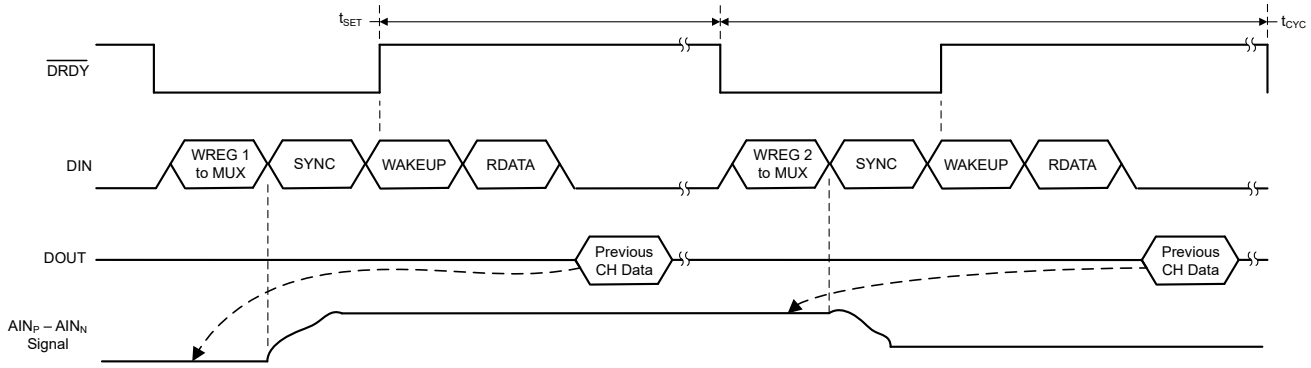


Figure 10-21. Cycling the Input Multiplexer

Table 10-11 and Table 10-12 show the effective cycling speed when stepping through the input multiplexer.

Table 10-11. Multiplexer Cycling Speed (Sinc3 Filter)

HIGH-SPEED MODE		MID-SPEED MODE		LOW-SPEED MODE	
DATA RATE (SPS)	CYCLING THROUGHPUT (Hz)	DATA RATE (SPS)	CYCLING THROUGHPUT (Hz)	DATA RATE (SPS)	CYCLING THROUGHPUT (Hz)
1,600	526	800	263	400	132
800	265	400	132	200	66.2
400	133	200	66.5	100	33.2
240	79.8	120	39.9	60	20.0
200	66.6	100	33.3	50	16.6
120	40.0	60	20.0	30	10.0
100	33.3	50	16.7	25	8.3
60	20.0	30	10.0	15	5.0

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Table 10-11. Multiplexer Cycling Speed (Sinc3 Filter) (continued)

HIGH-SPEED MODE		MID-SPEED MODE		LOW-SPEED MODE	
DATA RATE (SPS)	CYCLING THROUGHPUT (Hz)	DATA RATE (SPS)	CYCLING THROUGHPUT (Hz)	DATA RATE (SPS)	CYCLING THROUGHPUT (Hz)
50	16.7	25	8.3	12.5	4.2
40	13.3	20	6.7	10	3.3
20	6.7	10	3.3	5	1.7
10	3.3	5	1.7	2.5	0.8

Table 10-12. Multiplexer Cycling Speed (Sinc4 and Sinc5 + Averaging Filters)

HIGH-SPEED MODE		MID-SPEED MODE		LOW-SPEED MODE	
DATA RATE (SPS)	CYCLING THROUGHPUT (Hz)	DATA RATE (SPS)	CYCLING THROUGHPUT (Hz)	DATA RATE (SPS)	CYCLING THROUGHPUT (Hz)
320,000	23974 / 25916	160,000	12481 / 13537	80,000	6372 / 6923
240,000	21313 / 23390	120,000	11045 / 12165	60,000	5625 / 6207
120,000	14759 / 16829	60,000	7564 / 8655	30,000	3830 / 4390
60,000	9139 / 10781	30,000	4640 / 5488	15,000	2338 / 2769
30,000	7931 / 9139	15,000	4018 / 4640	7,500	2022 / 2338
15,000	6273 / 7005	7,500	3169 / 3544	3,750	1593 / 1782
7,500	4423 / 4775	3,750	2228 / 2407	1,875	1118 / 1208
4,000	2918 / 3067	2,000	1466 / 1541	1,000	735 / 773
2,000	1687 / 1736	1,000	846 / 870	500	424 / 436
1,000	915 / 929	500	458 / 465	250	229 / 233
200	196 / 197	100	98.2 / 98.5	50	49.1 / 49.3
120	119 /119	60	59.4 / 59.5	30	29.7 / 29.7
100	99.1 / 99.2	50	49.5 / 49.6	25	24.8 / 24.8
60	59.7 / 59.7	30	29.8 / 29.9	15	14.9 / 14.9
50	49.8 / 49.8	25	24.9 / 24.9	12.5	12.4 / 12.4
30	29.9 / 29.9	15	15.0 / 15.0	7.5	7.5 / 7.5
20	20.0 / 20.0	10	10.0 / 10.0	5	5.0 / 5.0
10	10.0/ 10.0	5	5.0 / 5.0	2.5	2.5 / 2.5
5	5.0 / 5.0	2.5	2.5 / 2.5	1.25	1.25 / 1.25

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10.4.3.2 One-Shot Conversions

A reduction of power consumption is achieved from the ADC by duty-cycling conversions using the STANDBY and WAKEUP commands. The procedure for this is shown in Figure 10-22. Issue the STANDBY command to enter standby mode. When ready for a measurement, issue the WAKEUP command to start a conversion. $\overline{DRDY}$ drives low t_{SET} + t_{WAKEUP} later, indicating the conversion is complete at which time data can be read using the RDATA command. Following the data read, issue another STANDBY command to reduce power. When ready for the next measurement, repeat the cycle starting with another WAKEUP command. The settling time values (t_{SET}) are shown in the Settling Time section. The typical wakeup time (t_{WAKEUP}) = 2050 / f_{MOD}.

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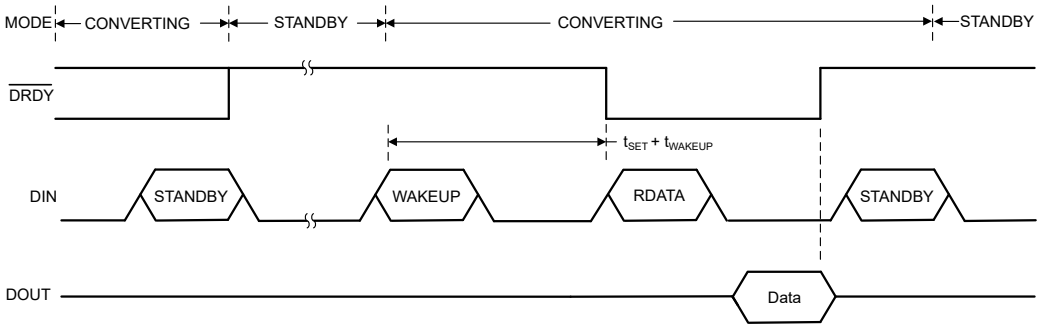


Figure 10-22. One-Shot Conversions

10.4.3.3 Continuous Conversions

If the input signal changes during a conversion, the output data are a mix of old and new data for several conversion periods until the digital filter produces fully settled data. This is shown in Figure 10-23.

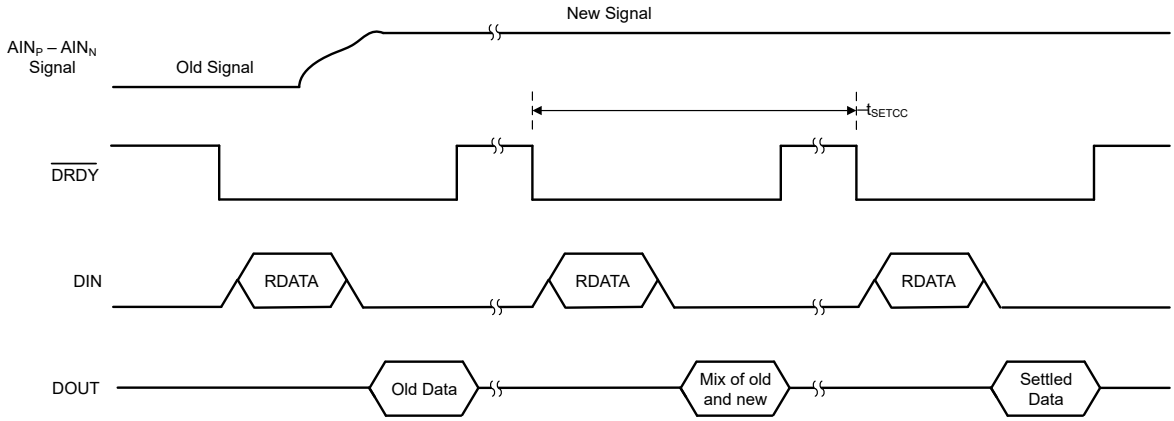


Figure 10-23. Input Step Change While Continuous Converting

Settling time is often considered in terms of data periods for convenience. The number of data periods for settled data assumes a fully-settled input before the first $\overline{\text{DRDY}}$ pulse. If an input step change occurs after the first $\overline{\text{DRDY}}$ pulse, add an additional conversion period to the values of Table 10-13.

Table 10-13. Continuous Conversion Settling Time

DATA RATE (SPS)			SETTLING TIME (t_{SETCC}) $\overline{\text{DRDY}}$ PERIODS		
HIGH-SPEED MODE	MID-SPEED MODE	LOW-SPEED MODE	SINC5	SINC4	SINC3
320,000	160,000	80,000	5	4	—
240,000	120,000	60,000	5	4	—
120,000	60,000	30,000	5	4	—
60,000	30,000	15,000	5	4	—
30,000	15,000	7,500	3	3	—
15,000	7,500	3,750	2	2	—
7,500	3,750	1,875	1	1	—
4,000	2,000	1,000	1	1	—
2,000	1,000	500	1	1	—
1,000	500	250	1	1	—
200	100	50	1	1	—
120	60	30	1	1	—
100	50	25	1	1	—

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Table 10-13. Continuous Conversion Settling Time (continued)

DATA RATE (SPS)			SETTLING TIME (t_{SETCC}) $\overline{DRDY}$ PERIODS		
HIGH-SPEED MODE	MID-SPEED MODE	LOW-SPEED MODE	SINC5	SINC4	SINC3
60	30	15	1	1	—
50	25	12.5	1	1	—
30	15	7.5	1	1	—
20	10	5	1	1	—
10	5	2.5	1	1	—
5	2.5	1.25	1	1	—
All Sinc3 Data Rates			—	—	3

10.4.3.4 Delay Time

A programmable delay time is available to delay the start of the first conversion after device synchronization. The delay time allows settling of external circuitry after an input multiplexer change or for settling of the voltage reference after exiting Standby or Power-down modes. The delay time is in addition to the settling time (t_{SET}) of the digital filter. Because the delay time is only used when the ADC is first synchronized, further conversions are not delayed. See the DELAY[3:0] bits of the CONFIG2 register for details.

10.4.3.5 Conversion Restart after Register Change

The ADC restarts conversions when certain register bits are changed by the SPI register write commands. Table 10-14 shows the register bits that result in conversion restart. If necessary, re-synchronize the ADC as after changing the bits of these registers.

Table 10-14. Register Bits Resulting in Conversion Cycle Restart

REGISTER	REGISTER BITS
STATUS	BUF_EN
MUX	PSEL[3:0], NSEL[3:0]
ADCON	SDCS[1:0], PGA[2:0]
DRATE	DR[7:0]
CONFIG0	AZERO_EN, MODE[1:0], FILTER[1:0]
CONFIG1	XTAL_EN, CLK_SRC, CLKDIV[1:0]
CONFIG2	AZ_DELAY[3:0], DELAY[3:0]

10.4.4 Standby Mode

The standby mode lowers device power consumption by reducing internal biasing. The crystal oscillator continues to operate to avoid start-up time of the crystal when exiting standby mode. The clock output signal of the D0/CLKOUT pin and SPI also continue to operate. To enter Standby mode, issue the STANDBY command. To exit Standby mode, issue the WAKEUP command. $\overline{DRDY}$ (DOUT/$\overline{DRDY}$ for ADS125R13) remains high after exiting Standby mode until valid data are ready. Standby mode can be used to perform power-efficient one-shot conversions; see the One-Shot Conversions section for more details.

10.4.5 Power-Down Mode

Power-down mode powers down the device. To enter power-down, hold the $\overline{SYNC}/\overline{PDWN}$ pin low for 20 $\overline{DRDY}$ cycles or send the PWDN command through SPI. To exit power-down, take the $\overline{SYNC}/\overline{PDWN}$ pin high or send the WAKEUP command. When power-down is exited, allow for the crystal oscillator start-up time (2ms typical). For all external clock sources, 8192 CLKIN cycles are counted before the first conversion is started.

10.4.6 Reset

The ADC automatically resets at power-up (POR). The ADC is manually reset by the $\overline{RESET}$ pin (hardware reset) and the RESET command (software reset). When reset, the ADC is re-initialized with registers reset to

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default settings. The CLK0, CLK1 bits are reset to the default state by hardware reset only, otherwise software reset leaves the bits unchanged.

For hardware reset, take the $\overline{\text{RESET}}$ pin low for a minimum of four t_{CLKIN} of t_{OSC} clock cycles, then take the pin high to release reset. Software reset takes effect at the end of the RESET command. Note that for the ADS125R13, hardware reset is not available.

10.4.6.1 Power-on Reset

The ADC is automatically reset at power-up. At reset, the device initializes operation and registers are reset to default. As shown in Figure 12-8, SPI can begin after the power supplies cross the power supply voltage thresholds. A clock signal is not required to begin SPI operation.

10.4.7 Autozero Mode

The ADC features an autozero mode that tracks offset error over time and temperature. Because autozero operates continuously to remove offset error, digital self-calibration is not required. Autozero performs conversions on the selected input channels with opposite polarities on alternate cycles. The alternate cycle data are subtracted and divided by 2 which effectively reduces the offset error leaving the original signal unchanged. See Equation 11.

$$\text{Autozero operation} = (V_{IN} + \text{Offset} - (-V_{IN} + \text{Offset})) / 2 \quad (11)$$

The data rate in autozero mode is reduced because the digital filter must settle after each conversion. The autozero mode data rates (f_{AZ}) are shown in Table 10-15.

Table 10-15. Autozero Data Rate (AZ_DELAY[3:0] = 0100b)

DR[7:0]	AUTOZERO DATA RATE, f_{AZ} (SPS)					
	SINC4 / SINC5 (+ AVERAGING FILTER)			SINC3 FILTER		
	HIGH-SPEED MODE	MID-SPEED MODE	LOW-SPEED MODE	HIGH-SPEED MODE	MID-SPEED MODE	LOW-SPEED MODE
11111100b	39,385 / 35,068	19,692 / 17,534	9,846 / 8,767	N/A	N/A	N/A
11111000b	33,833 / 29,853	16,916 / 14,826	8.458 / 7,413	N/A	N/A	N/A
11110100b	21,634 / 18,329	10,817 / 9,165	5,408 / 4,582	N/A	N/A	N/A
11110000b	12,570 / 10,392	6,285 / 5,196	3,142 / 2,598	N/A	N/A	N/A
11100000b	10,392 / 8,858	5,196 / 4,429	2,598 / 2,215	N/A	N/A	N/A
11010000b	7,719 / 6,839	3,859 / 3,419	1,930 / 1,710	N/A	N/A	N/A
11000000b	5,096 / 4,697	2,548 / 2,349	1,274 / 1,174	N/A	N/A	N/A
10110001b	3,196 / 3,034	1,598 / 1,517	799.0 / 758.6	N/A	N/A	N/A
10110000b	N/A	N/A	N/A	529.7	264.8	132.4
10100010b	1,777 / 1,725	888.3 / 862.7	444.1 / 431.4	N/A	N/A	N/A
10100000b	N/A	N/A	N/A	265.8	132.9	66.44
10010010b	940.8 / 926.3	470.4 / 463.2	235.2 / 231.6	N/A	N/A	N/A
10010000b	N/A	N/A	N/A	133.1	66.55	33.28
10000010b	197.5 / 196.9	98.76 / 98.43	49.38 / 49.22	N/A	N/A	N/A
10000000b	N/A	N/A	N/A	79.92	39.96	19.98
01110010b	119.1 / 118.9	59.55 / 59.43	29.78 / 29.72	N/A	N/A	N/A
01110000b	N/A	N/A	N/A	66.61	33.31	16.65
01100011b	99.38 / 99.21	49.69 / 49.60	24.84 / 24.80	N/A	N/A	N/A
01100000b	N/A	N/A	N/A	39.98	19.99	9.995
01010011b	59.77 / 59.71	29.89 / 29.86	14.94 / 14.93	N/A	N/A	N/A
01010000b	N/A	N/A	N/A	33.32	16.66	8.330
01000011b	49.84 / 49.80	24.92 / 24.90	12.46 / 12.45	N/A	N/A	N/A
01000000b	N/A	N/A	N/A	19.99	9.997	4.999

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Table 10-15. Autozero Data Rate (AZ_DELAY[3:0] = 0100b) (continued)

DR[7:0]	AUTOZERO DATA RATE, f_{AZ} (SPS)					
	SINC4 / SINC5 (+ AVERAGING FILTER)			SINC3 FILTER		
	HIGH-SPEED MODE	MID-SPEED MODE	LOW-SPEED MODE	HIGH-SPEED MODE	MID-SPEED MODE	LOW-SPEED MODE
00110011b	29.94 / 29.93	14.97 / 14.96	7.486 / 7.482	N/A	N/A	N/A
00110000b	N/A	N/A	N/A	16.66	8.332	4.166
00100011b	19.98 / 19.97	9.987 / 9.984	4.994 / 4.992	N/A	N/A	N/A
00100000b	N/A	N/A	N/A	13.31	6.666	13.331
00010011b	9.994 / 9.992	4.997 / 4.996	2.498 / 2.498	N/A	N/A	N/A
00010000b	N/A	N/A	N/A	6.666	3.333	1.667
00000011b	4.998 / 4.998	2.499 / 2.499	1.250 / 1.250	N/A	N/A	N/A
00000000b	N/A	N/A	N/A	3.333	1.667	0.833

Notches in the frequency response such as those produced by data rates 50SPS and 60SPS, are unchanged in autozero mode. Due to the autozero averaging of two conversions, new frequency notches are produced at n × f_{AZ}, (where n = 1, 2, 3 and so forth). The new notches are in addition to the original notches. The latency time of the first autozero data is approximately 2 / f_{AZ}, while the latency of following data is 1 / f_{AZ}.

The AZ_DELAY[3:0] bits of register CONFIG2 programs a delay time for the autozero process. The delay time is used at the start of each conversion to allow complete settling of the signal. The autozero delay time allows for settling of external R/C components when the input channel is reversed. The default delay time is 32 modulator clock cycles. For best performance at higher sample rates, increase the autozero delay to 64 modulator clock cycles. Increasing the delay time decreases the autozero data rate.

Due to the effective averaging of two conversions, noise performance improves by $\sqrt{2}$ (with exception of filter decimation factors 12 and 16). Autozero mode also changes the input buffer impedance. See Figure 8-3 and Figure 8-4 for input buffer impedance. For proper operation, disable autozero mode when using the calibration commands or when the auto-calibration (ACAL) mode is enabled. Autozero is enabled by the AZERO_EN bit of register CONFIG0.

10.4.8 Calibration

Offset and gain errors are compensated through calibration registers. As shown in Figure 10-24, the 24-bit offset calibration value is subtracted from the conversion data before multiplication by the 24-bit gain calibration value. Output data are rounded to the final resolution (16, 24 or 32 bit widths) and clipped to the +FS and –FS code values.

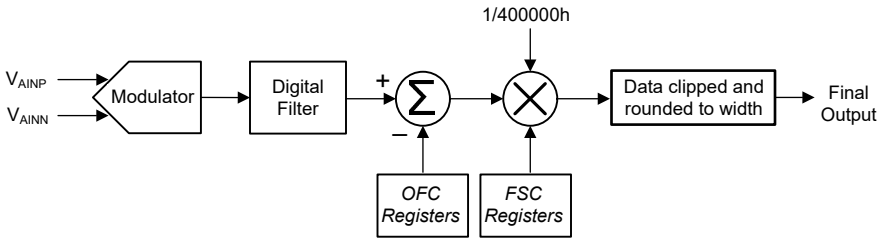


Figure 10-24. Calibration Block Diagram

Equation 12 shows how conversion data are calibrated:

$$\text{Final Output Data} = (\text{Data} - \text{OFC}) \times \text{FSC} / 400000\text{h} \quad (12)$$

OFC is 24-bit value in two's complement form, consisting of three 8-bit registers: OFC0, OFC1, OFC2 stored in little-endian format. The offset value is left-justified to align the MSB of the 16-bit and 32-bit data formats. FSC is a 24-bit value in straight binary format scaled with1/400000h, consisting of three registers: FSC0, FSC1, FSC2

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stored in little-endian format. Calibration is performed manually by writing data to the registers or obtained by the ADC through calibration commands.

10.4.8.1 Calibration Commands

The ADC has two types of calibration commands: Self and System. Self calibration is performed internally and does not require a calibration signal. System calibration requires the application of a calibration signal.

Figure 10-25 shows the calibration command sequence. $\overline{DRDY}$ is driven high when the calibration command is received to indicate calibration has started. $\overline{DRDY}$ drives low when calibration completes (t_{CAL}). At this time, new conversion data are ready using the new OFC and FSC calibration values. Do not send other commands until $\overline{DRDY}$ transitions low. Calibration time t_{CAL} depends on several variables: type of calibration command, data rate, digital filter and speed mode. Note that calibration commands are not available in Autozero mode. Disable the Autozero mode before calibrating.

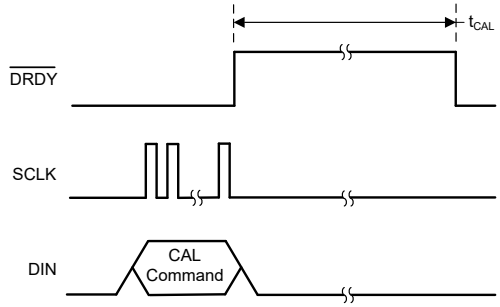


Figure 10-25. Calibration Commands

10.4.8.1.1 Self-Calibration

Self-calibration corrects offset and gain errors internal to the ADC. Calibration can be necessary when the ADC configuration is changed, for example, gain and buffer mode. Calibration signals are not required for self-calibration.

SELFOCAL performs self-offset calibration. The inputs are internally shorted and the OFC registers are updated with the calibration results. When enabled, the buffer is in-circuit for calibration. Perform offset calibration prior to gain calibration. Table 10-16 shows the calibration times.

SELFGCAL performs self-gain calibration. The inputs are connected to a scaled reference voltage to calibrate the full scale range corresponding to the ADC gain. If the input buffer is active, the buffer input range (AVDD – 1.45V) can be exceeded during calibration, resulting in invalid results. If this condition exists, disable the buffer during calibration or use a low voltage reference. The FSC registers are updated with the calibration results. Table 10-17 shows the calibration time.

SELFCAL sequentially performs self-offset calibration followed by self-gain calibration. Self-calibration updates the OFC and FSC registers. Table 10-18 shows the calibration time.

10.4.8.1.2 System-Calibration

System-calibration commands correct offset and gain errors using the SYSOCAL and SYSGCAL commands. Calibration can be necessary when the ADC configuration is changed, for example, gain and buffer mode. Calibration signals are required for system-calibration.

SYSOCAL performs system-offset calibration. The user typically shorts the inputs or applies 0V to the system for calibration. The buffer offset is also calibrated when enabled. The OFC registers are updated with the calibration results. Perform offset calibration prior to gain calibration. Table 10-16 shows the calibration time.

SYSGCAL performs system-gain calibration. The user applies a positive full-scale signal corresponding to the ADC gain to the system inputs. The calibration signal must be settled before issuing the command. Full scale output of the ADC is then scaled according to the calibration signal through the FSC register. The calibration

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signal is not to exceed 105% of the nominal input range to avoid inaccurate conversion data. As in normal operation, observe the input buffer headroom specification. Table 10-16 shows the calibration time.

10.4.8.1.3 Calibration Time

This section shows the calibration times for the calibration commands. Table 10-16 through Table 10-18 apply to the mid-speed mode and sinc5 filter. Calibration time for high-speed mode divide by 2 and for low speed mode the calibration times multiply by 2. Divide the f_{MOD} frequency by OSR to determine the data rate. Calibration times for the sinc3 and sinc4 filter modes are TBD.

Table 10-16. SELFOCAL, SYSOCAL, SYSGCAL Calibration Time

OSR	CALIBRATION TIME		
	SELF OFFSET	SYSTEM OFFSET	SYSTEM GAIN
12x1	TBD	TBD	TBD
16x1	TBD	TBD	TBD
32x1	TBD	TBD	TBD
64x1	0.360ms	0.360ms	0.490ms
64x2	0.427ms	0.427ms	0.456ms
64x4	0.560ms	0.560ms	0.590ms
64x8	0.827ms	0.827ms	0.856ms
64x15	1.3ms	1.3ms	1.3ms
64x30	2.3ms	2.3ms	2.3ms
64x60	4.3ms	4.3ms	4.3ms
64x300	20.3ms	20.3ms	20.3ms
64x500	33.6ms	33.6ms	33.6ms
64x600	40.3ms	40.3ms	40.3ms
64x1000	67.0ms	67.0ms	67.0ms
64x1200	80.3ms	80.3ms	80.3ms
64x2000	134ms	134ms	134ms
64x3000	200ms	200ms	200ms
64x6000	400ms	400ms	400ms
64x12000	800ms	800ms	800ms

Table 10-17. SELFGCAL Calibration Time

OSR	PGA GAIN				
	1	2	4	8	16, 32, 64, 128
12x1	TBD	TBD	TBD	TBD	TBD
16x1	TBD	TBD	TBD	TBD	TBD
32x1	TBD	TBD	TBD	TBD	TBD
64x1	0.390ms	0.390ms	0.424ms	0.490ms	0.623ms
64x2	0.457ms	0.457ms	0.457ms	0.523ms	0.656ms
64x4	0.590ms	0.590ms	0.590ms	0.590ms	0.723ms
64x8	0.856ms				
64x15	1.4ms				
64x30	2.4ms				
64x60	4.5ms				
64x300	21.0ms				
64x500	34.0ms				
64x600	41.6ms				
64x1000	67.8ms				

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Table 10-17. SELFGCAL Calibration Time (continued)

OSR	PGA GAIN				
	1	2	4	8	16, 32, 64, 128
64x1200	83.0ms				
64x2000	135ms				
64x3000	207ms				
64x6000	414ms				
64x12000	827ms				

Table 10-18. SELFCAL Calibration Time

OSR	PGA GAIN				
	1	2	4	8	16, 32, 64, 128
12x1	TBD	TBD	TBD	TBD	TBD
16x1	TBD	TBD	TBD	TBD	TBD
32x1	TBD	TBD	TBD	TBD	TBD
64x1	0.568ms	0.568ms	0.602ms	0.669ms	0.802ms
64x2	0.669ms	0.669ms	0.669ms	0.735ms	0.868ms
64x4	0.869ms	0.869ms	0.869ms	0.869ms	1.00ms
64x8	1.3ms				
64x15	2.0ms				
64x30	3.5ms				
64x60	6.6ms				
64x300	31.1ms				
64x500	50.9ms				
64x600	61.8ms				
64x1000	101ms				
64x1200	123ms				
64x2000	202ms				
64x3000	307ms				
64x6000	613ms				
64x12000	1227ms				

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10.5 Programming

10.5.1 Serial Interface (SPI)

The SPI-compatible serial interface is used to read and write register data, and to output the conversion data. The interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT operating in SPI mode 1 (CPOL = 0 and CPHA = 1). For ADS125R13, the SPI signals are $\overline{CS}$, SCLK, DIN and DOUT/$\overline{DRDY}$. In SPI mode 1, SCLK idles low and data are shifted-out on SCLK rising edges and are shifted-in on SCLK falling edges. SCLK is an input to the ADC and can be operated at a higher frequency than the ADC main clock. An optional 8-bit CRC validates the data integrity of the SPI transactions.

10.5.1.1 Chip Select ($\overline{CS}$)

$\overline{CS}$ is an active-low input that enables the SPI for communication. SPI is enabled by taking $\overline{CS}$ low and is disabled by taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the SPI resets, commands are blocked and DOUT enters a high-impedance state. $\overline{DRDY}$ is active regardless of the state of $\overline{CS}$. For the ADS125R13, the operation of the DOUT/$\overline{DRDY}$ pin when $\overline{CS}$ is high is determined by programming. Tie $\overline{CS}$ low to operate the interface in 3-wire SPI mode.

10.5.1.2 Serial Clock (SCLK)

SCLK is the serial clock input that shifts data into and out of the ADC. Output data are updated on the rising edge of SCLK and input data are latched on the falling edge. SCLK is a Schmitt-triggered input designed to increase noise immunity. Even though SCLK is noise resistant, keep SCLK as noise-free as possible to avoid unintentional transitions. Avoid ringing and overshoot on the SCLK input. A PCB series-termination resistor located at the SCLK driver often reduces ringing. When the serial interface is idle, hold SCLK low.

If SCLK is held low for 32 $\overline{DRDY}$ periods, the SPI serial interface resets and the next SCLK pulse starts a new communication cycle. This timeout feature can be used to recover communication from a SCLK noise pulse, particularly for applications that tie $\overline{CS}$ low. See Figure 10-26.

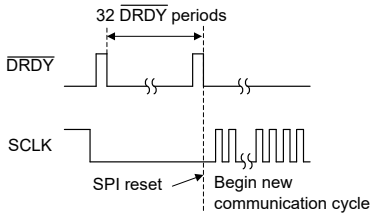


Figure 10-26. SPI Reset

10.5.1.3 Data Input (DIN)

DIN is the serial data input to the device. Input data is latched on the falling edge of SCLK.

10.5.1.4 Data Output (DOUT)

DOUT is the serial data output. Data is shifted-out on the rising edge of SCLK. DOUT is in Hi-Z mode before and after the output data. This allows the option of connecting DIN and DOUT together for 2-wire or 3-wire SPI operation. When used in this mode, data is transmitted/received by a bi-directional line from the host. Be aware that the RDATAC command must not be issued while DIN and DOUT are tied together. See Figure 10-28 for DOUT operation.

10.5.1.5 Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ falling edge indicates conversion data are ready. $\overline{DRDY}$ resets high when all the data bits (and CRC byte) have been read. If data is not read, $\overline{DRDY}$ remains low then pulses high when the next conversion data are ready as shown in Figure 10-27. Do not retrieve during this update period as the data are invalid. Figure 10-28 shows details of $\overline{DRDY}$ behavior when reading data.

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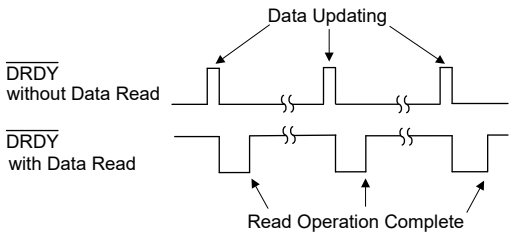


Figure 10-27. DRDY With and Without Data Read

After Reset, Synchronization, Standby mode, Power-Down mode or Calibration, DRDY is initially high then drives low when the first conversion data are ready.

10.5.1.6 Data Output/Data Ready (DOUT/DRDY)

Only for the ADS125R13, the DOUT/DRDY pin combines the data ready (DRDY) and data output (DOUT) functions. The default mode of DOUT/DRDY is data ready, which when driven low indicates conversion data are ready. The first rising of the SCLK input changes the pin to data output from which data are read. The pin changes back to data ready when the read operation is completed.

DOUT/DRDY is programmable to active or Hi-Z modes when CS is high. The active mode allows monitoring the data ready signal while CS is high. Since DOUT/DRDY is active, the output must not be shared with outputs of other devices. The Hi-Z mode tri-states DOUT/DRDY while CS is high. In this mode, the pin is enabled only when CS is low. The DOUT bit of register CONFIG1 programs the mode. See Figure 7-2 for operational details.

10.5.1.7 Conversion Data Format

Conversion data are programmable to 16-bit, 24-bit or 32-bit output data formats. 32-bit data format provides 28 active bits and is useful for slow sample rates where the quantization error of 24-bit data can limit resolution. The 16-bit data format reduces data transfer time for faster sample rates where 24-bit resolution is not always necessary. The output data format is programmed by the FORMAT[1:0] bits (default = 24 bits).

Conversion data are coded in either two's complement, to represent positive and negative differential signals (bipolar input signals), or coded in straight binary to represent only positive differential signals (unipolar input signals). The RANGE bit selects the input range (default = bipolar). Table 10-19 shows the code values for bipolar input range and Table 10-20 shows the code values for unipolar input range. For either bipolar and unipolar input range, conversion data clips to the minimum and maximum values to avoid code overflow when the respective minimum and maximum input ranges are exceeded.

Table 10-19. Code Values (Bipolar Input Range)

INPUT VOLTAGE (V_{IN})(1)	16-bit FORMAT	24-bit FORMAT	32-bit FORMAT
≥$(2V_{REF} / Gain) \cdot (2^n - 1) / 2^n$	7FFFh	7FFFFFh	7FFFFFF0h
$(2V_{REF} / Gain) / (2^n - 1)$	0001h	000001h	00000010h
0	0000h	000000h	00000000h
$(-2V_{REF} / Gain) / 2^n$	FFFFh	FFFFFFh	FFFFFFF0h
≤$-2V_{REF} / Gain$	8000h	800000h	80000000h

(1) n = 15 (16-bit format), n = 23 (24-bit format), n = 27 (32-bit format). Output codes are ideal values and exclude the effects of noise, INL, offset and gain errors.

Table 10-20. Code Values (Unipolar Input Range)

INPUT VOLTAGE (V_{IN})(1)	16-bit FORMAT	24-bit FORMAT	32-bit FORMAT
≥$2V_{REF} / Gain$	FFFFh	FFFFFFh	FFFFFFF0h
$(2V_{REF} / Gain) / 2^n$	0001h	000001h	00000010h
≤0	0000h	000000h	00000000h

(1) n = 16 (16-bit format), n = 24 (24-bit format), n = 28 (32-bit format). Output codes are ideal values and exclude the effects of noise, INL, offset and gain errors.

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10.5.1.8 Reading Conversion Data

There are two modes in which to read conversion data: read data direct without supplying the read data command (in Read Data Continuous mode), or read data by supplying the read data command (in Stop Read Data Continuous mode). Stop Read Data Continuous mode is default.

10.5.1.8.1 Read Data Continuous Mode (RDATAC)

Conversion data are read in the RDATAC mode by simply applying SCLKs – no command is necessary to read data. The RDATAC command engages the RDATAC mode. As shown in Figure 10-28, after $\overline{\text{DRDY}}$ (DOUT/$\overline{\text{DRDY}}$ for ADS125R13) drives low, data are ready to read. After the data are read, $\overline{\text{DRDY}}$ is driven high and DOUT enters the Hi-Z state. For the ADS1253, DOUT/$\overline{\text{DRDY}}$ changes to the data ready mode to indicate the next data ready. Reading back all bits is not necessary, but $\overline{\text{DRDY}}$ stays low until new data are ready. Be aware that only the SDATAC or RESET commands are acknowledged in RDATAC mode. To access register data, send the SDATAC command to stop RDATAC mode, then send the register command. Do not use the RDATAC mode if DIN and DOUT are connected together.

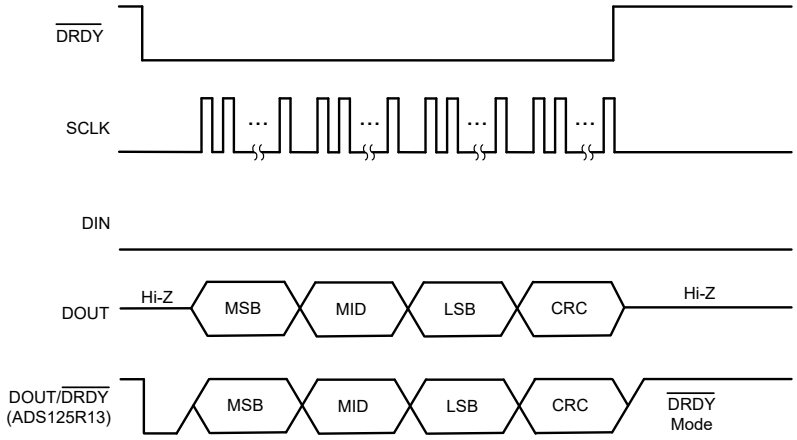


Figure 10-28. Read Data in RDATAC Mode

10.5.1.8.2 Stop Read Data Continuous Mode (SDATAC)

The SDATAC mode requires the read data command (RDATA) to read conversion data. The SDATAC command enables the SDATAC mode. As shown in Figure 10-29, when $\overline{\text{DRDY}}$ (DOUT/$\overline{\text{DRDY}}$ for the ADS125R13) drives low, send the RDATA command to read data. After all data bits have been read, $\overline{\text{DRDY}}$ drives high and DOUT enters the Hi-Z state. For the ADS1253, the DOUT/$\overline{\text{DRDY}}$ pin becomes the data ready signal for the next data ready. Reading back all bits is not necessary, but $\overline{\text{DRDY}}$ does not return high until new data are ready.

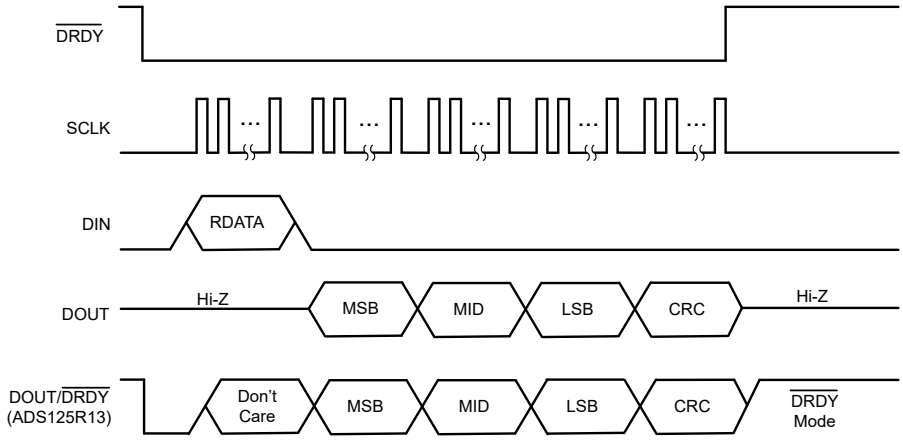


Figure 10-29. Read Data in SDATAC Mode

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10.5.1.9 SPI CRC

An 8-bit CRC validates SPI data transfer between the host and ADC. The CRC is enabled by the S_CRC_EN bit of register CONFIG1. In CRC mode, the user appends the CRC byte at the end of the input command. The ADC appends an output CRC byte after the conversion or register data. The CRC is 8-bits, based on the CRC-8-ATM (HEC) polynomial: $x^8 + x^2 + x^1 + 1$. The nine coefficients of the polynomial are: 100000111. The input argument is XORed with FFh allowing error detection in the event that DIN or DOUT fail low.

The input CRC is calculated over a one, two or three byte argument depending on the command. Figure 10-30 shows an example of a CRC input byte (CRC-IN) following the three bytes of a single-register write operation. If a CRC error is detected, the command is ignored and the $\overline{\text{SPI_ERR}}$ bit of the STATUS1 register latches low (active). The bit is *sticky* until the user resets the bit by writing 1b (1-to-reset). Further register reads and writes and conversion data reads are allowed if a CRC error occurs. If enabled by the ERR_EN bit of register CONFIG1, the D1/$\overline{\text{ERROR}}$ pin also drives low indicating the error. The pin remains low until $\overline{\text{SPI_ERR}}$ and other ADC error sources are reset.

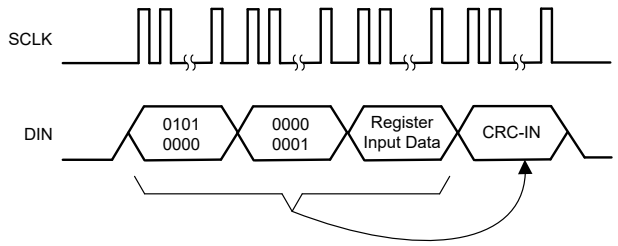


Figure 10-30. CRC WREG Command Example

Note that CRC input data check for a *multiple* register write operation is not supported. Only perform single register write operations in CRC mode. The $\overline{\text{SPI_ERR}}$ flag does not assert if multiple register writes are attempted.

Figure 10-31 shows the CRC output byte (CRC-OUT) that follows the output data. The CRC-OUT calculation includes all bytes of a multiple register read operation and all bytes of the conversion data. If a CRC error is detected externally, the conversion data can be re-read as long as the read operation occurs before the next $\overline{\text{DRDY}}$ pulse.

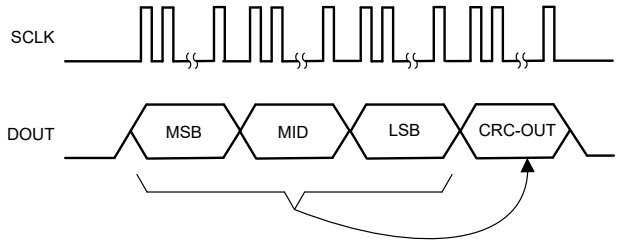


Figure 10-31. CRC Read Conversion Data Example

The ORDER bit reverses the bit order of the output data (within each byte) from MSB first to LSB first. ORDER does not affect input data, input data are always MSB first. Treat CRC-OUT if ORDER = 1 as follows.

- Read the output data
- Calculate the CRC of the received data bytes without reversing the bits
- Reverse the bits of the received CRC byte and compare the data to the calculated CRC

10.5.1.10 Register CRC

The ADC monitors register values by comparing a calculated CRC to the CRC written to the CRC register. The $\overline{\text{REG_ERR}}$ bit of the STATUS1 register asserts low if the CRC values do not match. The CRC is calculated over Page 0 register addresses 0h through Ah and Page1 register addresses 0h through 2h. Because the $\overline{\text{DRDY}}$ bit of the STATUS register and the lower four data bits of the IO register are dynamic, these bits are masked from

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the CRC calculation. CRC verification is enabled by the R_CRC_EN bit of register CONFIG1. The register map CRC polynomial is the same as the SPI CRC polynomial (See the SPI CRC section).

The following is the recommended procedure for the register CRC:

1. Compute the CRC value with the R_CRC_EN bit = 1b (CRC enabled)
2. Write the register values including the above CRC value but with R_CRC_EN bit = 0b (CRC disabled)
3. Write the R_CRC_EN bit = 1b to enable the CRC.
4. Wait 14 clock cycles for the ADC to generate the comparison CRC to determine the CRC error.

To clear the CRC error, correct the CRC value (or the registers in error) then write 1b to the $\overline{\text{REG_ERR}}$ bit (1-to-reset). When enabled by the ERR_EN bit of register CONFIG1, the D1/$\overline{\text{ERROR}}$ pin drives low to indicate a register CRC error. The pin remains low until the $\overline{\text{REG_ERR}}$ bit is reset.

The calibration commands write new values to the OFC and FSC register which require a new CRC value. Read the new calibration values from the OFC and FSC registers to compute a new CRC value.

10.5.2 Device Commands

Device commands are used to read and write register data, ADC calibration, ADC control and so forth. Commands are summarized in Table 10-21. Commands are stand-alone except for register read and write (RREG, WREG) which are multiple byte. The next command can follow immediately after the preceding command.

Table 10-21. Device Commands

COMMAND	DESCRIPTION	1st BYTE	2nd BYTE
WAKEUP	Completes SYNC and exits Standby and Power-down	0000 0000b (00h) 1111 1111b (FFh)	
RDATA	Read Conversion Data	0000 0001b (01h)	
RDATAC	Read-data Continuous Mode	0000 0011b (03h)	
SDATAC	Stop Read-data Continuous Mode	0000 1111b (0Fh)	
RREG	Read Register rrrr(1)	0001 rrrrb (1xh)	000n nnnnb(2)
WREG	Write Register rrrr(1)	0101 rrrrb (5xh)	000n nnnnb(2)
SELFCAL	Offset and Gain Self-calibration	1111 0000b (F0h)	
SELFOCAL	Offset Self-calibration	1111 0001b (F1h)	
SELFGCAL	Gain Self-calibration	1111 0010b (F2h)	
SYSOCAL	Offset System-calibration	1111 0011b (F3h)	
SYSGCAL	Gain System-calibration	1111 0100b (F4h)	
PWDN	Power Down	1111 1010b (FAh)	
SYNC	Synchronize Conversions	1111 1100b (FCh)	
STANDBY	Standby	1111 1101b (FDh)	
RESET	ADC Reset	1111 1110b (FEh)	

(1) rrrr = starting register address for read/write commands. Use a single-register write operation to the page pointer register (address = Fh) to select the register page.
(2) n nnnn = number of registers to be read/written – 1. For example, set n nnnn = 2 to read/write three registers.

10.5.2.1 RDATA: Read Conversion Data

This command reads conversion data while in the SDATAC mode. See the Stop Read Data Continuous Mode (SDATAC) section for details.

10.5.2.2 RDATAC: Set Read Data Continuous Mode

This command enables the Read Data Continuous mode. This mode does not require the RDATA command to read conversion data – simply apply SCLKs to read the data. RDATAC mode is canceled by the SDATAC or

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RESET commands – no other input commands are acknowledged while in this mode. Do not use this mode if DIN and DOUT are connected together.

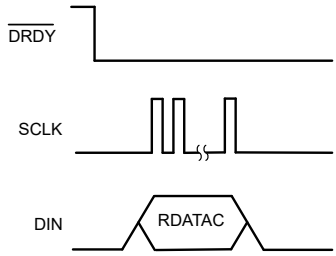


Figure 10-32. RDATAC Command Sequence

10.5.2.3 SDATAC: Stop Read Data Continuous

This command enables the Stop Read Data Continuous mode (SDATAC). This mode requires the read data command (RDATA) to read conversion data. Issue the command after $\overline{\text{DRDY}}$ goes low and complete the command before $\overline{\text{DRDY}}$ returns high (DOUT/$\overline{\text{DRDY}}$ for ADS125R13).

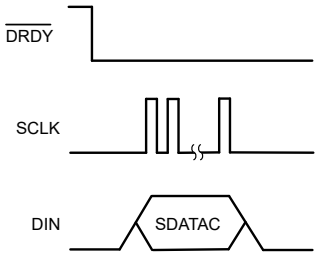


Figure 10-33. SDATAC Command Sequence

10.5.2.4 RREG: Read From Registers

The RREG command is used to read register data with the address of the first register specified as part of the first command byte. The number of registers to read is one plus the number specified in the second command byte. If the register count exceeds the number of registers of a page, the address wraps to the beginning of the other page. The page pointer register, which selects page 0 or page 1, is only accessible by a single-register read operation.

Figure 10-34 shows an example of a two-register read operation starting with register 1h (MUX) of page 0. The PAGE_PTR register is previously set to page 0 (00h) for this example. The 1st command byte is 0001 rrrr, where rrrr is the address of the first register to read from the page. The 2nd command byte is 000n nnnn, where n nnnn is the number of registers to read – 1. In this example, the output data is from registers MUX and ADCON.

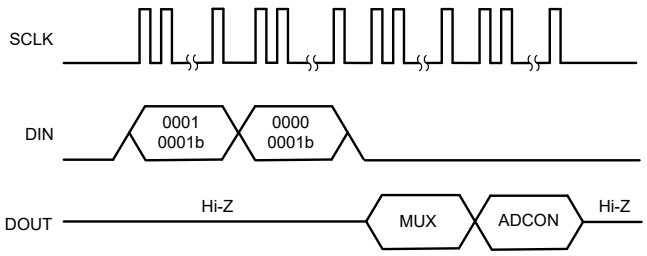


Figure 10-34. RREG Command Sequence

10.5.2.5 WREG: Write to Registers

The WREG command is used to write register data with the first register address specified as part of the first command byte. The number of registers written is one plus the number specified in the second command byte.

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If the count exceeds the number of registers of a page, the addresses wrap to the beginning of the other page. The page pointer register, which selects page 0 or page 1, is only accessible by a single register write operation.

Figure 10-35 shows an example of a two-register write operation starting register 3h (DRATE) of page 0. The PAGE_PTR register is previously set to page 0 (00h) for this example. The 1st command byte is 0101rrrrb, where rrrr is the address of the first register to write within a page. The 2nd command byte is 000n nnnnb, where n nnnn is the number of registers to write – 1. Bytes 3 and 4 following the command bytes are the register data to be written to registers DRATE and IO. The data takes effect on the 8th SCLK of the data bytes.

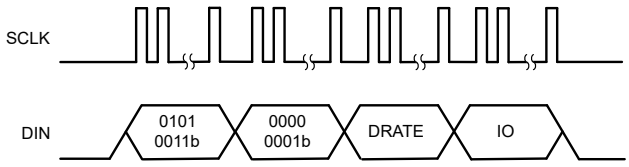


Figure 10-35. WREG Command Sequence

10.5.2.6 SELFCAL, SELFOCAL, SELFGCAL, SYSOCAL, SYSGCAL: Calibration Commands

The ADS125R1x supports self-calibration commands (offset, gain and combined offset/gain) and system-calibration commands (offset and gain). The Offset Calibration Register (OFC) and Full-Scale Calibration Register (FSC) update with new calibration results. For self-calibration, the ADC generates the calibration signals. For system calibration, the appropriate calibration signals must be applied to the inputs. See the Calibration section for more details.

10.5.2.7 SYNC: Synchronize A/D Conversion

The SYNC command synchronizes the A/D conversion. First exit the RDATAC mode, then shift in the SYNC command followed by the WAKEUP command when ready to synchronize. Synchronization occurs on the first CLKIN rising edge after the first SCLK used to shift in the WAKEUP command. See Figure 10-20 for details.

10.5.2.8 STBY: Standby Mode

This command places the device into the standby mode to reduce power consumption. After issuing the STANDBY command, make sure there is no more activity on SCLK while $\overline{CS}$ is low, as this interrupts Standby mode. To exit Standby mode, issue the WAKEUP command. This command can also be used to perform power efficient, single conversions (see the One-Shot Conversions section).

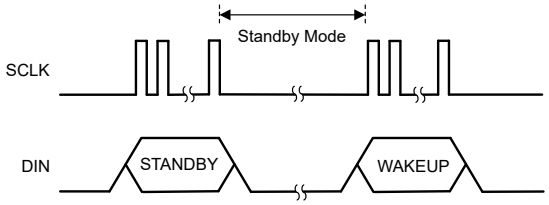


Figure 10-36. STANDBY Command Sequence

10.5.2.9 PWDN: Power-down

This command powers down the device. After issuing the PWDN command, make sure there is no more activity on SCLK while $\overline{CS}$ is low, as this exits power-down. To exit power-down, issue the WAKEUP command.

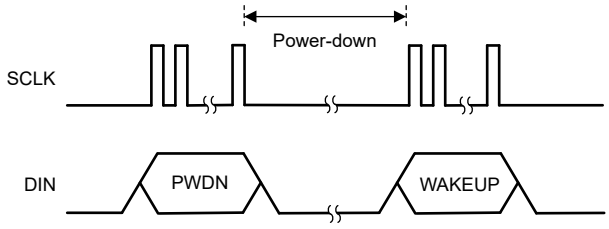


Figure 10-37. Power-Down Command Sequence

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10.5.2.10 RESET: ADC Reset

This command resets the ADC. Reset restarts conversions and returns all registers except the CLK0 and CLK1 bits in the ADCON register to default values. This command also stops the Read Data Continuous mode. Issue the RESET command after $\overline{\text{DRDY}}$ goes low.

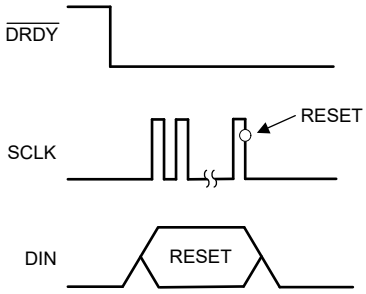


Figure 10-38. RESET Command

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11 Registers

The ADC registers are divided into two pages: page 0 and page 1. Page 0 registers are compatible to the ADS1255 and ADS1256 ADCs. Page 1 registers support additional functions. To access the registers, first select the register page by writing 0h or 1h to the PAGE_PTR register from either page (address Fh). The page number remains in effect until changed by the user. When an address rollover occurs during multiple register read and write operations, the address pointer wraps to the first register of the other page. Table 11-1 shows the register summary.

11.1 Register Summary Table

Table 11-1. Register Summary

Page	Addr.	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0h	0h	STATUS	RESERVED				ORDER	ACAL	BUFEN	$\overline{\text{DRDY}}$
	1h	MUX	PSEL[3:0]				NSEL[3:0]			
	2h	ADCON	RESERVED	CLK_OUT[1:0]		SDCS[1:0]		PGA[2:0]		
	3h	DRATE	DR[7:0]							
	4h	GPIO	DIR3	DIR2	DIR1	DIR0	DIO3	DIO2	DIO1	DIO0
	5h	OFC0	OFC_LSB[7:0]							
	6h	OFC1	OFC_MID[7:0]							
	7h	OFC2	OFC_MSB[7:0]							
	8h	FSC0	FSC_LSB[7:0]							
	9h	FSC1	FSC_MID[7:0]							
	Ah	FSC2	FSC_MSB[7:0]							
	Fh	PAGE_PTR	PAGE_PTR[7:0]							
1h	0h	CONFIG0	AZERO_EN	RANGE	FORMAT[1:0]		MODE[1:0]		FILTER[1:0]	
	1h	CONFIG1	XTAL_EN	DOUT	CLK_SRC	CLK_DIV[1:0]		ERR_EN	R_CRC_EN	S_CRC_EN
	2h	CONFIG2	AZ_DELAY[3:0]				DELAY[3:0]			
	3h	CRC	CRC[7:0]							
	4h	STATUS1	RESERVED					$\overline{\text{ADC_ERR}}$	$\overline{\text{REG_ERR}}$	$\overline{\text{SPI_ERR}}$
	5h	DEV_ID	DEV_ID[7:0]							
	6h	REV_ID	REV_ID[7:0]							
	Fh	PAGE_PTR	PAGE_PTR[7:0]							

The bit access types are encoded to fit into small table cells. Table 11-2 shows the access type codes that are used in the register sections.

Table 11-2. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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11.1.1 STATUS Register (Page = 0h, Address = 0h) [Reset = 01h]

Return to the Summary Table.

Figure 11-1. STATUS Register

7	6	5	4	3	2	1	0
RESERVED				ORDER	ACAL	BUFEN	$\overline{\text{DRDY}}$
R-0b				R/W-0b	R/W-0b	R/W-0b	R-1b

Table 11-3. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0b	Reserved
3	ORDER	R/W	0b	Data output bit order Input data is always shifted in most significant byte and bit first. Output data is always shifted out most significant *byte* first. The ORDER bit only controls the bit order of the output data within the byte. 0b = Most significant bit first 1b = Least significant bit first
2	ACAL	R/W	0b	Auto-calibration enable When enabled, self-calibration begins at the completion of the WREG command that changes the following bits: PGA[2:0] of register ADCON, DR[7:0] of register DRATE, BUFEN of register STATUS, FILTER[1:0] and MODE[1:0] of register CONFIG0 and CLK_SRC and CLK_DIV[1:0] of register CONFIG1. 0b = Auto-calibration disabled 1b = Auto-calibration enabled
1	BUFEN	R/W	0b	Analog input buffer enable 0b = Buffer disabled 1b = Buffer enabled
0	$\overline{\text{DRDY}}$	R	1b	Data ready This read-only bit duplicates the $\overline{\text{DRDY}}$ pin. The bit also applies to the ADS125R13 DOUT/$\overline{\text{DRDY}}$ pin when in data ready mode. 0b = $\overline{\text{DRDY}}$ pin low 1b = $\overline{\text{DRDY}}$ pin high

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11.1.2 MUX Register (Page = 0h, Address = 1h) [Reset = 01h]

Return to the Summary Table.

Figure 11-2. MUX Register

7	6	5	4	3	2	1	0
PSEL[3:0]				NSEL[3:0]			
R/W-0000b				R/W-0001b			

Table 11-4. MUX Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	PSEL[3:0]	R/W	0000b	Positive input channel select Select only the valid input channels of each device. 0000b = AIN0 0001b = AIN1 0010b = AIN2 0011b = AIN3 0100b = AIN4 0101b = AIN5 (AINCOM for ADS125R13) 0110b = AIN6 0111b = AIN7 1000b = AINCOM (ADS125R11 and ADS125R14) ≥1001b = Reserved
3:0	NSEL[3:0]	R/W	0001b	Negative input channel select Select only the valid input channels of each device. 0000b = AIN0 0001b = AIN1 0010b = AIN2 0011b = AIN3 0100b = AIN4 0101b = AIN5 (AINCOM for ADS125R13) 0110b = AIN6 0111b = AIN7 1000b = AINCOM (ADS125R11 and ADS125R14) ≥1001b = Reserved

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11.1.3 ADCON Register (Page = 0h, Address = 2h) [Reset = 20h]

Return to the Summary Table.

Figure 11-3. ADCON Register

7	6	5	4	3	2	1	0
RESERVED	CLK_OUT[1:0]		SDCS[1:0]		PGA[2:0]		
R-0b	R/W-01b		R/W-00b		R/W-000b		

Table 11-5. ADCON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6:5	CLK_OUT[1:0]	R/W	01b	D0/CLKOUT pin clock output frequency Select the D0/CLKOUT pin output clock frequency. The output frequency is a division of the CLKIN input signal or the internal oscillator. When not using CLKOUT, it is recommended that it be turned off. 00b = Clock output off (pin is under GPIO control) 01b = Clock output frequency = div / 1 10b = Clock output frequency = div / 2 11b = Clock output frequency = div / 4
4:3	SDCS[1:0]	R/W	00b	Sensor detect current sources Program the current sources. The current sources can be activated to verify the integrity of an external sensor supplying a signal to the ADC. A shorted sensor produces a very small signal while an open-circuit sensor produces a very large signal. 00b = Sensor detect current off 01b = Sensor detect current = 0.5µA 10b = Sensor detect current = 2µA 11b = Sensor detect current = 10µA
2:0	PGA[2:0]	R/W	000b	Gain setting Select the ADC gain. 000b = 1 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b = 64 111b = 128

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11.1.4 DRATE Register (Page = 0h, Address = 3h) [Reset = F0h]

Return to the Summary Table.

Figure 11-4. DRATE Register

7	6	5	4	3	2	1	0
DR[7:0]							
R/W-11110000b							

Table 11-6. DRATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DR[7:0]	R/W	11110000b	Data rate setting Select the output data rate. The valid data rate settings are shown in the Digital Filter section.

11.1.5 GPIO Register (Page = 0h, Address = 4h) [Reset = E0h]

Return to the Summary Table.

Figure 11-5. GPIO Register

7	6	5	4	3	2	1	0
DIR3	DIR2	DIR1	DIR0	DIO3	DIO2	DIO1	DIO0
R/W-1b	R/W-1b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 11-7. GPIO Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIR3	R/W	1b	GPIO direction for D3 pin 0b = D3 pin is an output 1b = D3 pin is an input
6	DIR2	R/W	1b	GPIO direction for D2 pin 0b = D2 pin is an output 1b = D2 pin is an input
5	DIR1	R/W	1b	GPIO direction for D1/$\overline{\text{ERROR}}$ pin 0b = D1/$\overline{\text{ERROR}}$ pin is an output 1b = D1/$\overline{\text{ERROR}}$ pin is an input
4	DIR0	R/W	0b	GPIO direction for D0/CLKOUT pin 0b = D0/CLKOUT pin is an output 1b = D0/CLKOUT pin is an input
3	DIO3	R/W	0b	GPIO status for D3 pin 0b = D3 pin is logic low 1b = D3 pin is logic high
2	DIO2	R/W	0b	GPIO status for D2 pin 0b = D2 pin is logic low 1b = D2 pin is logic high
1	DIO1	R/W	0b	GPIO status for D1/$\overline{\text{ERROR}}$ pin 0b = D1/$\overline{\text{ERROR}}$ pin is logic low 1b = D1/$\overline{\text{ERROR}}$ is logic high
0	DIO0	R/W	0b	GPIO status for D0/CLKOUT pin 0b = D0/CLKOUT pin is logic low 1b = D0/CLKOUT pin is logic high

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11.1.6 OFC0 Register (Page = 0h, Address = 5h) [Reset = 00h]

Return to the Summary Table.

Figure 11-6. OFC0 Register

7	6	5	4	3	2	1	0
OFC_LSB[7:0]							
R/W-00000000b							

Table 11-8. OFC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OFC_LSB[7:0]	R/W	00000000b	Offset calibration byte 0 (LSB) See the Calibration section for details.

11.1.7 OFC1 Register (Page = 0h, Address = 6h) [Reset = 00h]

Return to the Summary Table.

Figure 11-7. OFC1 Register

7	6	5	4	3	2	1	0
OFC_MID[7:0]							
R/W-00000000b							

Table 11-9. OFC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OFC_MID[7:0]	R/W	00000000b	Offset calibration byte 1 (MID) See the Calibration section for details.

11.1.8 OFC2 Register (Page = 0h, Address = 7h) [Reset = 00h]

Return to the Summary Table.

Figure 11-8. OFC2 Register

7	6	5	4	3	2	1	0
OFC_MSB[7:0]							
R/W-00000000b							

Table 11-10. OFC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OFC_MSB[7:0]	R/W	00000000b	Offset calibration byte 2 (MSB) See the Calibration section for details.

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11.1.9 FSC0 Register (Page = 0h, Address = 8h) [Reset = 00h]

Return to the Summary Table.

Figure 11-9. FSC0 Register

7	6	5	4	3	2	1	0
FSC_LSB[7:0]							
R/W-00000000b							

Table 11-11. FSC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FSC_LSB[7:0]	R/W	00000000b	Full-scale calibration byte 0 (LSB) See the Calibration section for details.

11.1.10 FSC1 Register (Page = 0h, Address = 9h) [Reset = 00h]

Return to the Summary Table.

Figure 11-10. FSC1 Register

7	6	5	4	3	2	1	0
FSC_MID[7:0]							
R/W-00000000b							

Table 11-12. FSC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FSC_MID[7:0]	R/W	00000000b	Full-scale calibration byte 1 (MID) See the Calibration section for details.

11.1.11 FSC2 Register (Page = 0h, Address = Ah) [Reset = 40h]

Return to the Summary Table.

Figure 11-11. FSC2 Register

7	6	5	4	3	2	1	0
FSC_MSB[7:0]							
R/W-01000000b							

Table 11-13. FSC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FSC_MSB[7:0]	R/W	01000000b	Full-scale calibration byte 2 (MSB) See the Calibration section for details.

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11.1.12 PAGE_PTR Register (Page = 0h, Address = Fh) [Reset = 00h]

Return to the Summary Table.

Figure 11-12. PAGE_PTR Register

7	6	5	4	3	2	1	0
PAGE_PTR[7:0]							
R/W-00000000b							

Table 11-14. PAGE_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PAGE_PTR[7:0]	R/W	00000000b	Register page pointer Used to access page 0 or page 1 registers. 00000000b = Page 0 registers 00000001b = Page 1 registers

11.1.13 CONFIG0 Register (Page = 1h, Address = 0h) [Reset = 14h]

Return to the Summary Table.

Figure 11-13. CONFIG0 Register

7	6	5	4	3	2	1	0
AZERO_EN	RANGE	FORMAT[1:0]		MODE[1:0]		FILTER[1:0]	
R/W-0b	R/W-0b	R/W-01b		R/W-01b		R/W-00b	

Table 11-15. CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AZERO_EN	R/W	0b	Autozero Enable autozero mode. See the Autozero Mode section for more details. 0b = Autozero off 1b = Autozero on
6	RANGE	R/W	0b	Bipolar or unipolar input range Select bipolar or unipolar input range. 0b = Bipolar range 1b = Unipolar range
5:4	FORMAT[1:0]	R/W	01b	Data format Select the output data resolution. 00b = 16-bit data 01b = 24-bit data 10b = 32-bit data 11b = Reserved
3:2	MODE[1:0]	R/W	01b	Speed mode Select the device speed mode. 00b = Low speed 01b = Mid speed 10b = High speed 11b = Reserved
1:0	FILTER[1:0]	R/W	00b	Digital filter Program the digital filter. See the Digital Filter section for more details. 00b = Sinc5 01b = Sinc4 10b = Sinc3 11b = Reserved

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11.1.14 CONFIG1 Register (Page = 1h, Address = 1h) [Reset = 88h]

Return to the Summary Table.

Figure 11-14. CONFIG1 Register

7	6	5	4	3	2	1	0
XTAL_EN	DOUT	CLK_SRC	CLK_DIV[1:0]		ERR_EN	R_CRC_EN	S_CRC_EN
R/W-1b	R/W-0b	R/W-0b	R/W-01b		R/W-0b	R/W-0b	R/W-0b

Table 11-16. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	XTAL_EN	R/W	1b	Crystal oscillator Enable the crystal oscillator buffer. If not using the buffer, disable to reduce power consumption. 0b = Crystal oscillator disabled 1b = Crystal oscillator enabled
6	DOUT	R/W	0b	ADS125R13 DOUT/$\overline{\text{DRDY}}$ pin behavior Select the DOUT/$\overline{\text{DRDY}}$ pin behavior when $\overline{\text{CS}}$ is high. 0b = DOUT/$\overline{\text{DRDY}}$ is Hi-Z 1b = DOUT/$\overline{\text{DRDY}}$ is active
5	CLK_SRC	R/W	0b	ADC clock source Select the clock source, external or internal oscillator. 0b = External 1b = Internal
4:3	CLK_DIV[1:0]	R/W	01b	ADC clock divisor Select the clock divisor (external and internal clock) 00b = div / 2 01b = div / 4 10b = div / 6 11b = div / 8
2	ERR_EN	R/W	0b	D1/$\overline{\text{ERROR}}$ pin Select the D1/$\overline{\text{ERROR}}$ pin function: error output or digital I/O. Error bit(s) that are asserted low in the STATUS1 register drives the D1/$\overline{\text{ERROR}}$ pin low. 0b = D1/$\overline{\text{ERROR}}$ pin is digital IO function 1b = D1/$\overline{\text{ERROR}}$ pin is an error output
1	R_CRC_EN	R/W	0b	Register map CRC Enable register map CRC 0b = Disabled 1b = Enabled
0	S_CRC_EN	R/W	0b	SPI CRC Enable SPI CRC. 0b = Disabled 1b = Enabled

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11.1.15 CONFIG2 Register (Page = 1h, Address = 2h) [Reset = 40h]

Return to the Summary Table.

Figure 11-15. CONFIG2 Register

7	6	5	4	3	2	1	0
AZ_DELAY[3:0]				DELAY[3:0]			
R/W-0100b				R/W-0000b			

Table 11-17. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	AZ_DELAY[3:0]	R/W	0100b	Autozero time delay Program a time delay for autozero operation. The time delay is used after signal reversal to allow for compete settling. Units are number of f_{MOD} cycles. 0000b = 0 0001b = 8 0010b = 16 0011b = 24 0100b = 32 0101b = 40 0110b = 48 0111b = 56 1000b = 64 1001b = 80 1010b = 96 1011b = 112 1100b = 128 1101b = 144 1110b = 160 1111b = 176
3:0	DELAY[3:0]	R/W	0000b	Conversion start time delay Program a time delay between synchronization and the start of conversions to allow for complete settling. Units are number of f_{MOD} cycles. 0000b = 0 0001b = 8 0010b = 16 0011b = 24 0100b = 32 0101b = 40 0110b = 48 0111b = 56 1000b = 64 1001b = 80 1010b = 96 1011b = 112 1100b = 128 1101b = 144 1110b = 160 1111b = 176

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11.1.16 CRC Register (Page = 1h, Address = 3h) [Reset = 00h]

Return to the Summary Table.

Figure 11-16. CRC Register

7	6	5	4	3	2	1	0
CRC[7:0]							
R/W-00000000b							

Table 11-18. CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CRC[7:0]	R/W	00000000b	Register map CRC value Write the CRC value. The CRC includes registers from both pages. See the Register CRC section for more details.

11.1.17 STATUS1 Register (Page = 1h, Address = 4h) [Reset = 07h]

Return to the Summary Table.

Figure 11-17. STATUS1 Register

7	6	5	4	3	2	1	0
RESERVED					$\overline{\text{ADC_ERR}}$	$\overline{\text{REG_ERR}}$	$\overline{\text{SPI_ERR}}$
R-0b					R-1b	R/W-1b	R/W-1b

Table 11-19. STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0b	Reserved
2	$\overline{\text{ADC_ERR}}$	R	1b	ADC error Cycle power or reset the device to clear the error. If the error persists, replace the device. 0b = ADC internal error 1b = No error
1	$\overline{\text{REG_ERR}}$	R/W	1b	Register CRC error Correct the CRC value register then write 1 to clear the error. 0b = Register CRC error 1b = No error
0	$\overline{\text{SPI_ERR}}$	R/W	1b	SPI CRC error Write 1 to clear the error then check the failed SPI command that caused the error. 0b = SPI CRC error 1b = No error

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11.1.18 DEV_ID Register (Page = 1h, Address = 5h) [Reset = XXh]

Return to the Summary Table.

Figure 11-18. DEV_ID Register

7	6	5	4	3	2	1	0
DEV_ID[7:0]							
R-xxxxxxxxb							

Table 11-20. DEV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEV_ID[7:0]	R	xxxxxxxxb	Device ID Identifies the device type. 00010000b = ADS125R11 00010011b = ADS125R13 00010100b = ADS125R14

11.1.19 REV_ID Register (Page = 1h, Address = 6h) [Reset = XXh]

Return to the Summary Table.

Figure 11-19. REV_ID Register

7	6	5	4	3	2	1	0
REV_ID[7:0]							
R-xxxxxxxxb							

Table 11-21. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REV_ID[7:0]	R	xxxxxxxxb	Die revision ID The die revision can change at any time without notice.

11.1.20 PAGE_PTR Register (Page = 1h, Address = Fh) [Reset = 00h]

Return to the Summary Table.

Figure 11-20. PAGE_PTR Register

7	6	5	4	3	2	1	0
PAGE_PTR[7:0]							
R/W-00000000b							

Table 11-22. PAGE_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PAGE_PTR[7:0]	R/W	00000000b	Register page pointer Used to access page 0 or page 1 registers. 00000000b = Page 0 registers 00000001b = Page 1 registers

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12 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

12.1 Application Information

The ADS125R1x devices are a family of high-resolution, 24-bit delta-sigma A/D converters. Optimal performance from the devices requires careful attention to support circuitry and printed circuit board (PCB) design.

Figure 12-1 shows the ADS125R11 connected to a differential input signal. The ADS125R14 has similar features, but supports a total of four differential or eight single-ended inputs. A 7.68MHz crystal oscillator is the clock source with connection to pins XTAL1/CLKIN and XTAL2. Internal oscillator or external clock input (XTAL1/CLKIN) are other clock options. The REF6025 voltage reference is internally buffered so it connects to the reference inputs without need of a buffer. Series resistors for the digital pins help to dampen ringing and peak drive current associated with high trace capacitance.

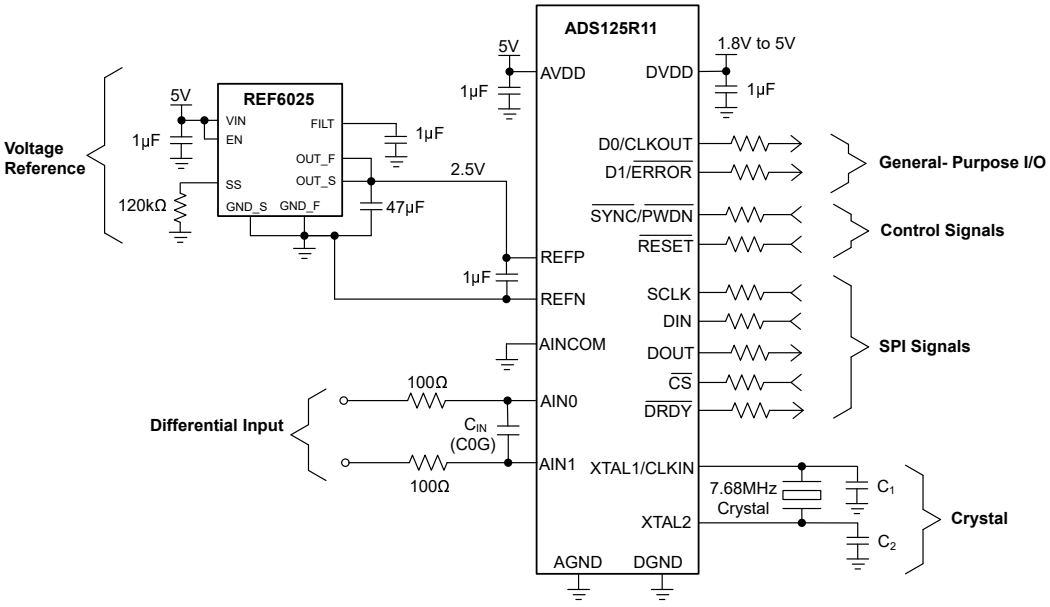


Figure 12-1. ADS125R11 Circuit Example

Figure 12-2 shows the ADS125R13 connected to five single-ended input signals with AINCOM as signal common (ground). Note the ADS125R13 uses one power supply (VDD) for analog and digital. Synchronization, reset and power-down control functions are available only through SPI for this device. The ADS125R13 supports two clock options: internal oscillator or external clock applied to CLKIN

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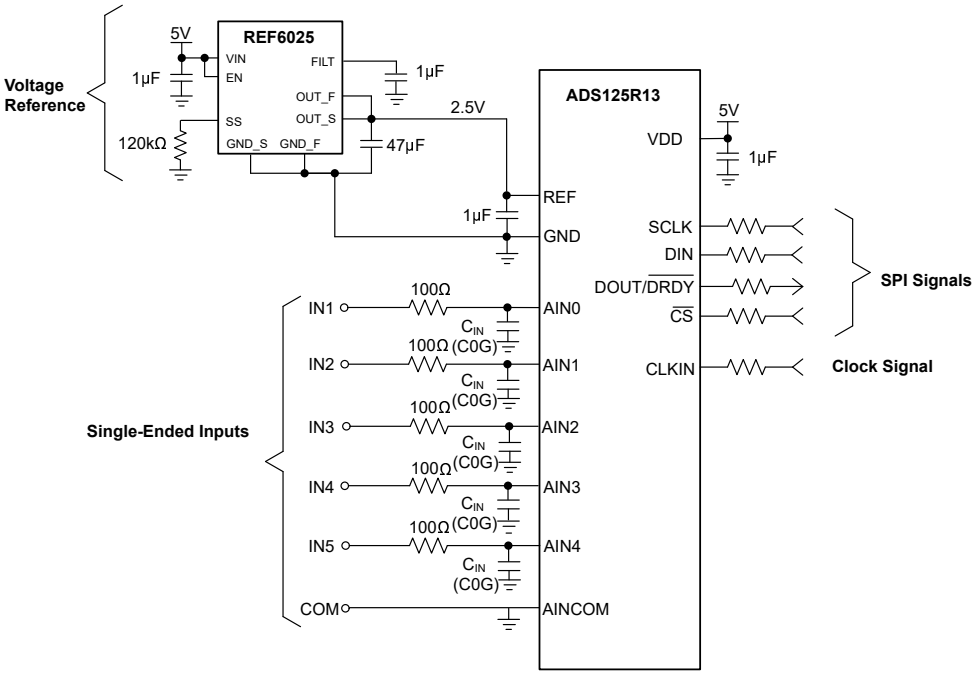


Figure 12-2. ADS125R13 Circuit Example

12.1.1 Analog Inputs

An input filter on the analog inputs reduces aliasing of out-of-band signals. If aliased, the out-of-band signals can affect in-band signal performance. A single RC filter is frequently all that is needed; see the Frequency Response section for the ADC aliasing frequency bands. Route the input signals using matched-length, short, direct traces and place the filter components close to the input pins. When possible, use adjacent ADC input pins for the signal and route as differential signal pairs to minimize noise pickup.

Use an input resistor of 4kΩ or less to minimize the effect of resistor noise to ADC noise. This is especially important for small-signal inputs. Consider the input impedance of the modulator loading down the input signal. The input buffer raises input impedance to decrease signal loading. To minimize input current of the measurement channel when using the input buffer, float unused inputs or tie the inputs to AVDD/2 (VDD/2).

The input capacitor depends on whether the buffer is used. With buffer, the recommended capacitance range is 1-100nF (C0G). Without buffer, a minimum C0G 100nF capacitor is recommended to maintain linearity performance. When using an external buffer, operate the buffer with the same AVDD power supply (VDD for ADS125R13) to avoid over-driven ADC inputs if the signal is out of range.

12.1.2 Reference Inputs

Select a voltage reference with low noise and drift and is able to drive the dynamic loading presented by the reference inputs. The REF6025 provides a buffered output designed to drive the reference inputs. When using an unbuffered voltage reference (such as the REF5425), buffer the voltage as shown in the application section of the *REF54 Precision Voltage Reference Family* datasheet.

Bypass the reference inputs with a capacitor in the range 1µF to 10µF placed directly across the inputs. To minimize pickup of ground noise, route the REFN input to the voltage reference ground terminal using an isolated trace. For the ADS125R13, route the voltage reference ground pin to the GND pin of the ADC, then make the connection to ground at the ADC.

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12.1.3 Clock Options

The ADCs has three clock options: crystal oscillator (ADS125R11 and ADS125R14), an external clock and internal oscillator. The choice of internal or external clock operation is selected though SPI register. When using external clock, be sure the clock signal is free from glitches and is physically separated from other clock signals. Keep digital signals away from the crystal oscillator circuit to avoid cross-coupling noise into the circuit.

12.1.4 SPI Serial Interface

The ADC uses SPI for communications. Figure 12-3 shows a 4-wire connection to an SPI controller. The data ready signal ($\overline{\text{DRDY}}$) connects to the controller ($\overline{\text{IRQ}}$) to trigger the data read operations. Series resistors source-terminate the SPI traces to dampen reflections generated in the traces.

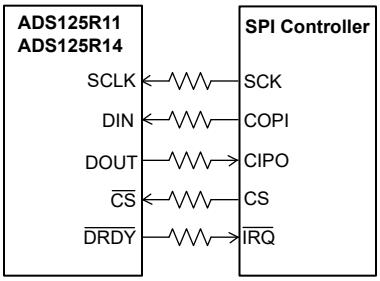


Figure 12-3. ADS125R11 and ADS125R14 to SPI Controller

Figure 12-4 shows the ADS125R13 SPI connection. The ADS125R13 interface is similar to the ADS125R11/R14 devices except the DOUT and $\overline{\text{DRDY}}$ functions are combined on the DOUT/$\overline{\text{DRDY}}$ pin. The DOUT/$\overline{\text{DRDY}}$ signal of the ADC is connected to the controller CIPO and $\overline{\text{IRQ}}$ pins.

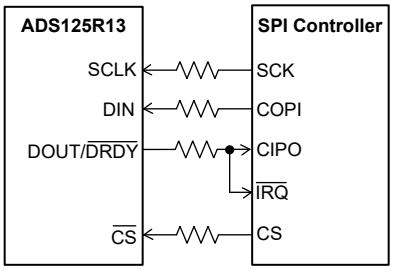


Figure 12-4. ADS125R13 to SPI Controller

Figure 12-5 shows the ADS125R11/R14 in a 2-wire connection. In this configuration, DIN and DOUT pins connect together, $\overline{\text{CS}}$ is grounded and $\overline{\text{DRDY}}$ is unconnected. The ADC automatically tri-states DOUT after the data read operation. Similarly, the external controller tri-states DIN and becomes a receiver when the ADC drives DOUT. In this example, $\overline{\text{DRDY}}$ is not used therefore the user software predicts when to read data based on the data period. Avoid using the continuous read mode (RDATAC) when DIN and DOUT are connected together. Keep in mind the ADS125R13 does not support 2-wire mode.

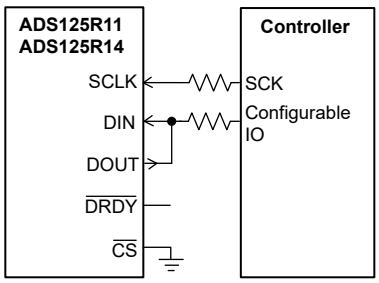


Figure 12-5. 2-Wire Interface

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12.1.5 Simultaneous Sampling

The ADS125R14 accepts up to eight signal inputs through the input multiplexer. In simultaneous-sampling systems, an ADC is needed for each signal input. Figure 12-6 shows a four-channel, simultaneous sampling system. The ADCs use individual chip select signals for the SPI. ADS125R11 #1 uses a crystal oscillator which drives a clock output signal (D0/CLKOUT) to the synchronize operation of the other ADCs. Conversions are synchronized by one $\overline{\text{SYNC}}$/$\overline{\text{PWDN}}$ signal for all devices. After the devices are synchronized, one $\overline{\text{DRDY}}$ signal is sufficient to monitor data ready of all devices.

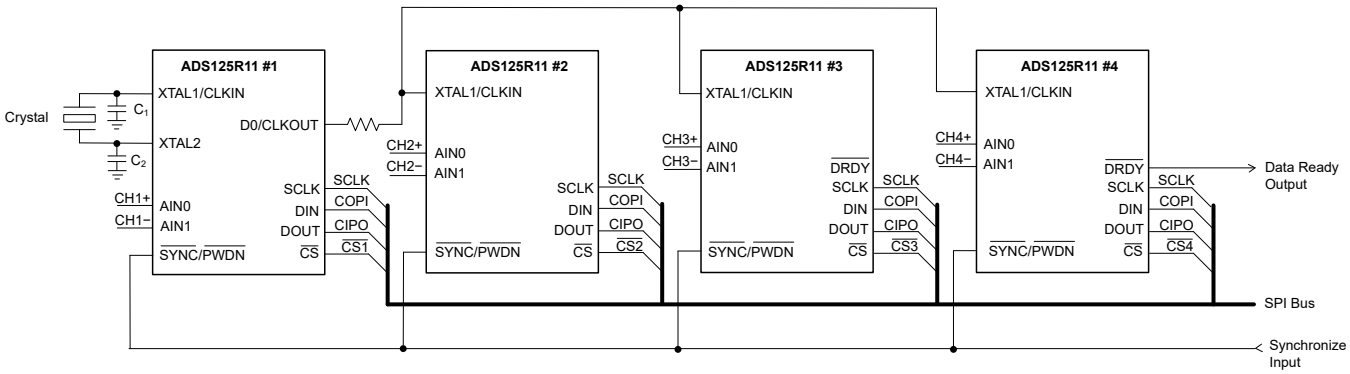


Figure 12-6. Simultaneous Sampling System

12.2 Initialization Setup

12.2.1 Initialization Procedure

1. $\overline{\text{DRDY}}$ drives high at power-up which indicates SPI is ready for operation. A clock signal is not necessary for SPI operation. See Figure 12-8 for the power-up sequence.
2. The ADC defaults to external clock operation. If using a crystal, the crystal start up time is 2ms typical, but can be longer depending on the crystal characteristics.
3. To select the internal oscillator, set the CLK_SRC bit of register CONFIG1 to 0 and disable the crystal oscillator circuit by setting the XTAL_EN bit of register CONFIG1 to 0.
4. Make other ADC configurations as necessary to the device registers. Note the $\overline{\text{DRDY}}$ pin pulses at the data rate period when the clock source is active.
5. If desired, perform offset and gain calibration for the configured gain, buffer mode and analog inputs.
6. The first conversion is fully settled after the ADC is synchronized. There is no need to discard data to account for filter settling. Be sure the reference voltage is fully settled before performing conversions.

12.3 Typical Applications

12.3.1 Resistive Bridge Sensor

The ADCs are high resolution 24-bit converters with low noise, low drift and high linearity. Wide ADC sampling dynamics capture dc signals, such as load cells bridge sensors, and ac signals up to 65kHz bandwidth to detect fast moving pressure and vibration signals. DC resolution and stability is especially important to provide repeatable measurement of small signals produced by resistive bridges. The input buffer and high gains provided by the ADC remove the need for additional components. This application analyzes thermal noise generated within the bridge and how the noise combines with the ADC noise. A resistive bridge sensor input is shown in Figure 12-7.

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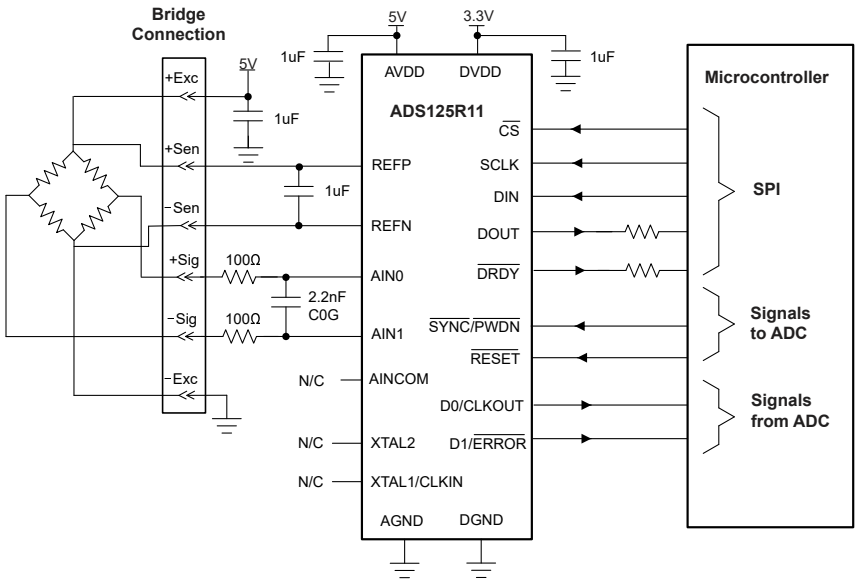


Figure 12-7. Resistive Bridge Sensor

12.3.1.1 Design Requirements

Table 12-1 are the design goals of the ADC.

Table 12-1. Design Goals

PARAMETER	TARGET VALUE
Signal range	10mV
Total noise	<400nV$_{RMS}$
Sample rate	1000SPS
Step input settling time	1.1ms

12.3.1.2 Detailed Design Procedure

A 5V excitation voltage used with a 2mV/V sensitivity bridge yields a 10mV signal. PGA gain of 128 provides the lowest noise measurement for the 10mV signal. The input buffer reduces signal loading of the bridge. A filter on the analog input reduces RFI and EMI interference and reduces aliasing of high frequency noise.

The resistor elements of the bridge are 1kΩ which results in an effective 1kΩ output impedance. The room-temperature thermal noise generated by a 1kΩ resistor is approximately 4nV/√Hz. Since the noise of the bridge and the ADC are uncorrelated, the noise and ADC are combined as root-mean-sum quantities to determine the total noise of the system. Integrated noise of the bridge is the thermal noise times the square root of the signal bandwidth. The signal bandwidth at 1000SPS sample rate = 0.442µx 1kHz = 442Hz. Thermal noise of the bridge is therefore 4nV/√Hz x √442Hz = 84nV. The ADC noise at 1kSPS, gain 128, buffer enabled in high speed mode = 370nV. The predicted overall noise is therefore $\sqrt{(84^2 + 370^2)}$ = 379nV.

12.3.1.3 Application Data

The measured noise of this application without the bridge connected = 358nV$_{RMS}$. With the 1kΩ bridge connected, the measured noise = 366nV$_{RMS}$. These results show that 1kΩ bridge sensor adds a negligible amount of overall noise to the ADC.

12.4 Power Supply Recommendations

The devices require an analog and a digital power supply. AVDD powers the ADC analog section (input multiplexer, SDCS and modulator) and DVDD powers the internal logic and digital I/O pins. The ADS125R13 combines the analog and digital power supplies on VDD.

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Figure 12-8 shows the power-up sequence (ADS125R13 VDD power supply threshold = AVDD threshold). $\overline{DRDY}$ and DOUT/$\overline{DRDY}$ signals are initially Hi-Z, then are at 0V until the power supplies achieve the threshold voltages. The SPI is ready for communication when $\overline{DRDY}$ transitions high. A clock signal is not required for SPI communication but can be applied before or after $\overline{DRDY}$ transitions high. The first conversion is started when the clock signal is applied and is ready when $\overline{DRDY}$ drives low. The first data is valid assuming the reference voltage is settled at power-on.

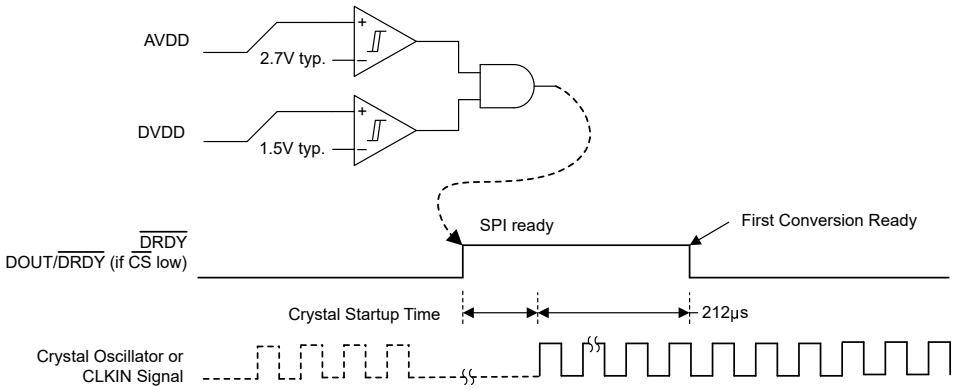


Figure 12-8. Power-on Operation

The power supplies do not require special sequencing and are able to be powered in any order and are tolerant of slow or fast ramp rates. However, make sure the analog and digital inputs do not exceed the respective analog power supply (AVDD) or digital power supply (DVDD) by 0.3V, (VDD for the ADS125R13), and are not below device ground by 0.3V including during power-up or power-down. Bypass the power supply pins with a 1µF to 10uF capacitor. Keep the analog power supply voltage ripple low (<1mV) when using switching power supplies to reduce noise coupling into the conversion result.

12.5 Layout

12.5.1 Layout Guidelines

To achieve datasheet performance, a minimum four-layer PCB is recommended with inner layers dedicated as solid ground and power planes. Best performance is achieved by a single ground plane for analog and digital. In some layout topologies, however, separate analog and digital grounds are necessary to help direct local digital currents away from the analog ground. For example, current flow from switching power supplies, pulsing LED indicators, relays, and so on. In this case, consider separate ground return paths for these loads. When separate analog and digital grounds are used, join the grounds at the ADC.

A power-plane layer is recommended for power supply routing. The top and bottom layers typically route analog and digital signals. Route the input signals as matched differential pairs as much as possible throughout the signal chain to minimize noise coupling. Place the input filter components close to the input pins. Avoid parallel trace runs between digital and analog signals to reduce noise coupling. Where necessary, cross the signals at right angles with ground fill-in between the layers where the signals need to cross. This layout is especially important for high-frequency digital signals such as the clock signal, SCLK and DOUT.

Place the voltage reference as close as possible to the ADC. Orient the voltage reference package such that the ground pin is directed to the REFN pin (GND pin of ADS125R13). Place the reference bypass capacitor across REFP and REFN at the ADC pins. The ADS125R13 combines the REFN, AGND and DGND pins into one pin (GND). Connect the voltage reference ground pin to the ADC GND pin by a dedicated trace and make this connection to ground at the ADC. Use a reference bypass capacitor for each ADC in multichannel systems and route REFP and REFN using wide traces or a power plane.

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12.5.2 Layout Example

Figure 12-9 shows a layout example of the resistive bridge sensor circuit of Figure 12-7. The 3mm x 3mm RUK package of the ADS125R11 is shown. A four-layer PCB is used, all signals on the top layer, solid inner and bottom layers for ground and split inner plane layer for AVDD and DVDD power. Ground pour of the signal layer is best practice to shield noise (ground pour not shown).

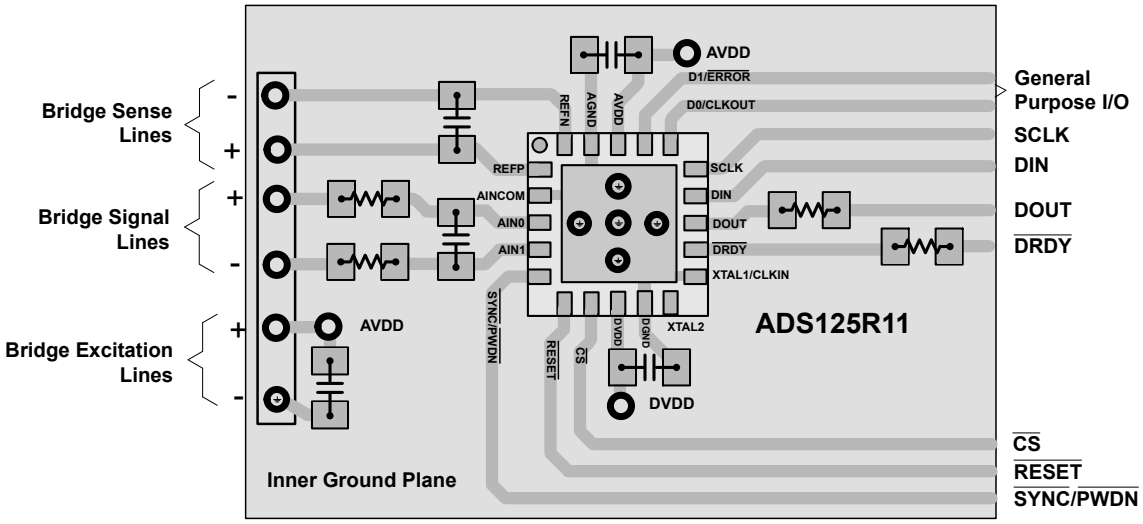


Figure 12-9. Layout Example for Resistive Bridge Sensor

See the *QFN and SON PCB Attachment* application note for details of attaching the WQFN package to the printed circuit board.

Figure 12-10 shows an example layout of the ADS125R11 crystal oscillator in the SSOP package option. Locate other clock signals away from the crystal and crystal PCB traces. Use a solid inner layer ground plane to help shield the crystal from interfering digital signals. Take into account the stray capacitance of the crystal PCB traces when selecting capacitors C_1 and C_2.

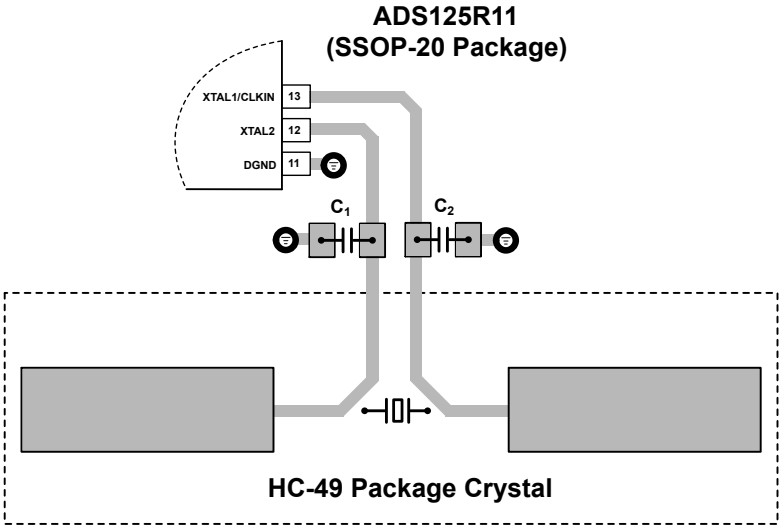


Figure 12-10. Example Layout for Crystal Oscillator Circuit

ADVANCE INFORMATION

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *REF60xx High-Precision Voltage Reference with Integrated ADC Drive Buffer* datasheet
- Texas Instruments, *QFN and SON PCB Attachment* application note

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

14 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2026	*	Initial Release

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)
PADS125R14IDBR	Preview	Preproduction	SSOP | 28	1000 | Reel	Yes	NiPdAu	Level-2-1YEAR-260C	–40 to 125	P125R14

(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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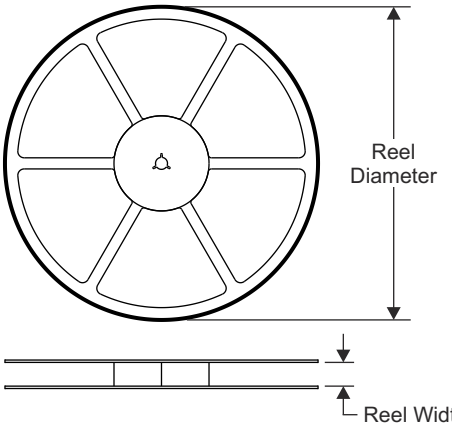
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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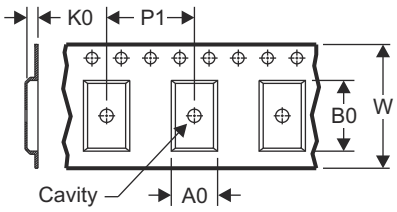
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15.1 Tape and Reel Information

REEL DIMENSIONS

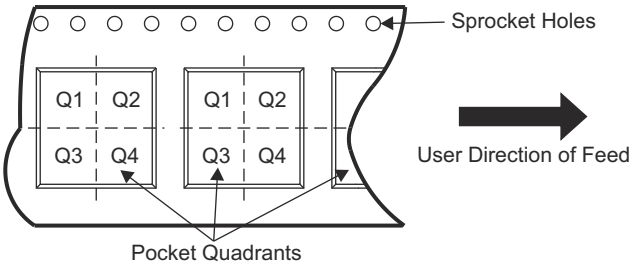


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

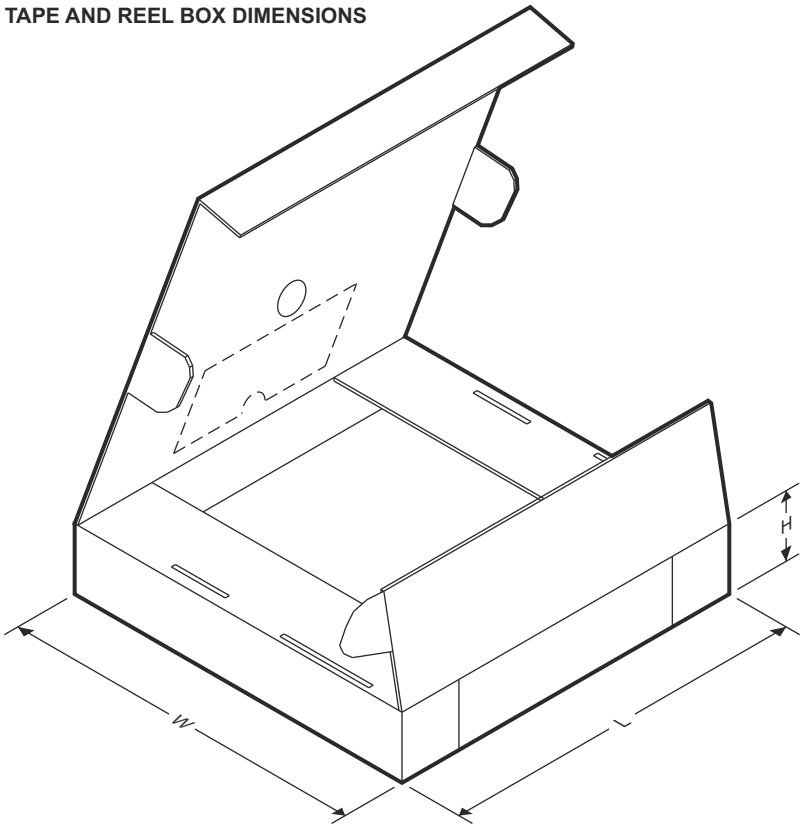


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PADS125R14IDBR	SSOP	DB	28	1000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PADS125R14IDBR	SSOP	DB	28	1000	356.0	356.0	35.0

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ADVANCE INFORMATION

15.2 Mechanical Data

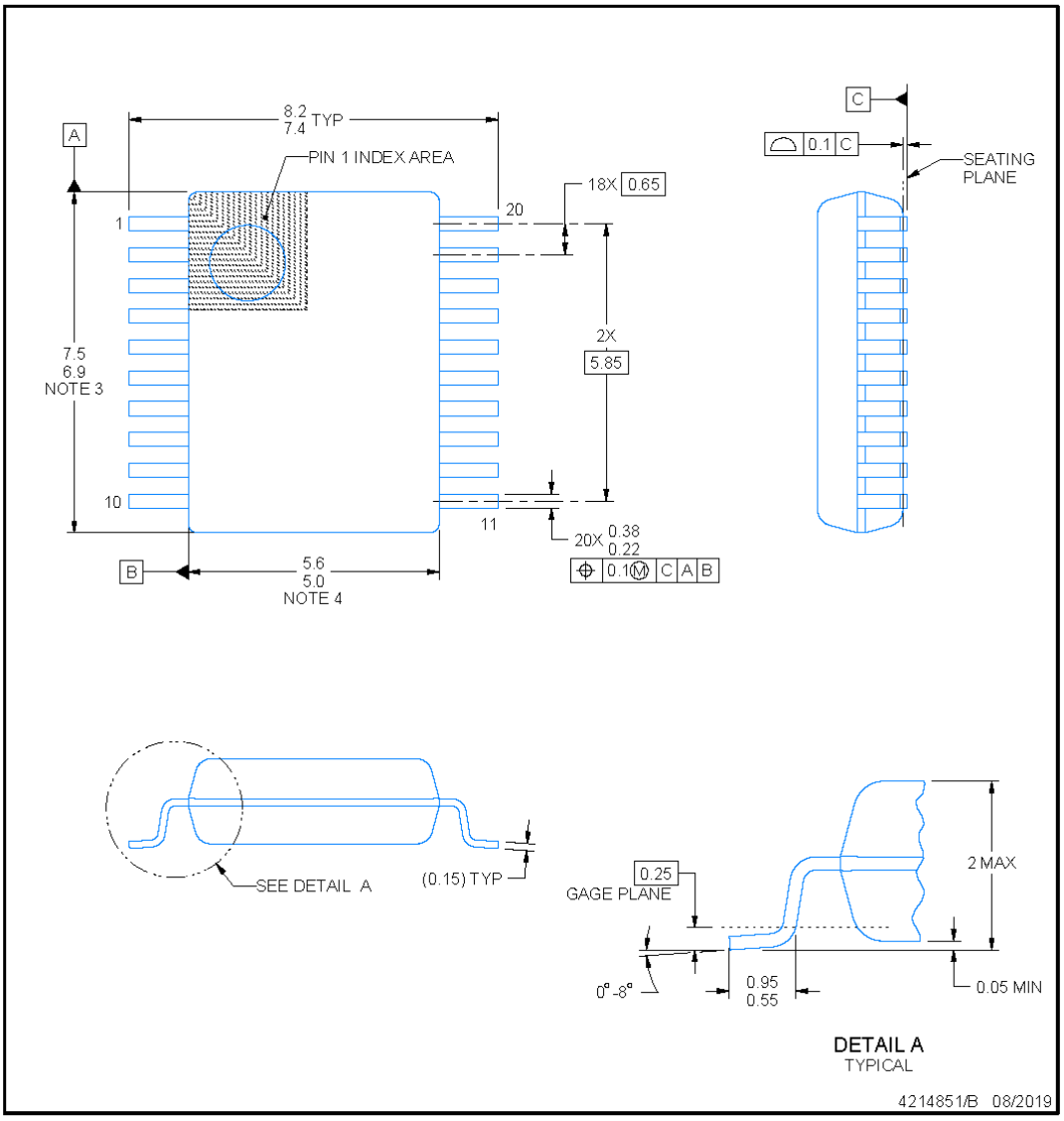
DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

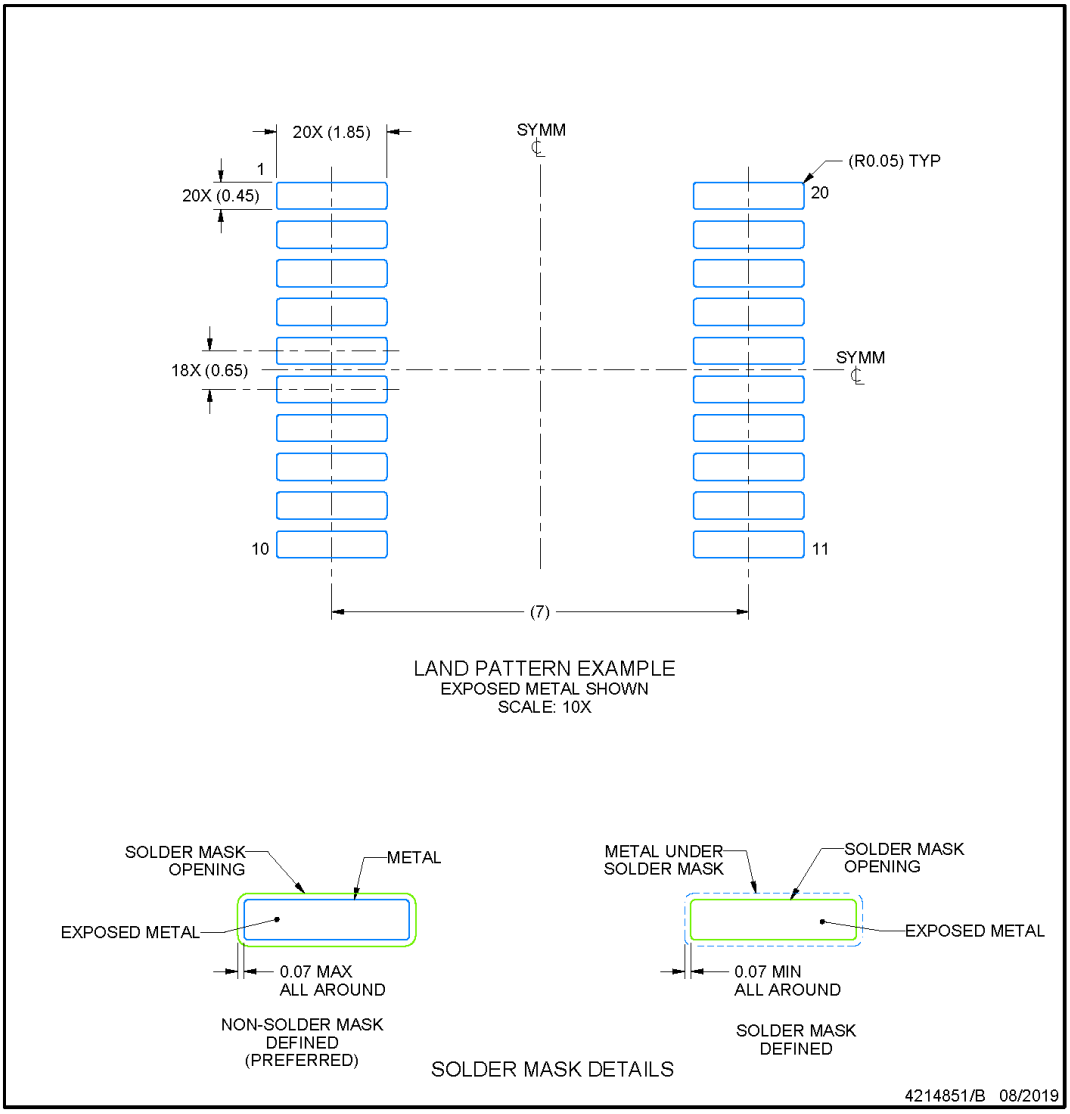
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

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EXAMPLE BOARD LAYOUT

DB0020A — **SSOP - 2 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

ADVANCE INFORMATION

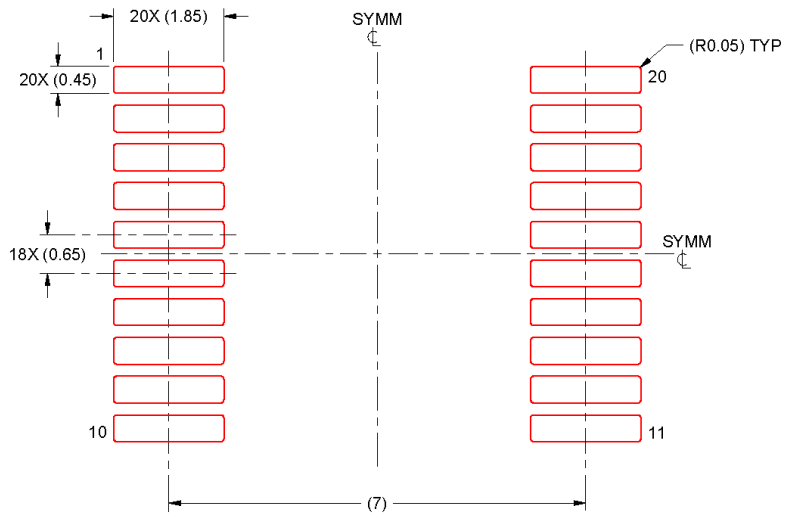
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ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DB0020A — **SSOP - 2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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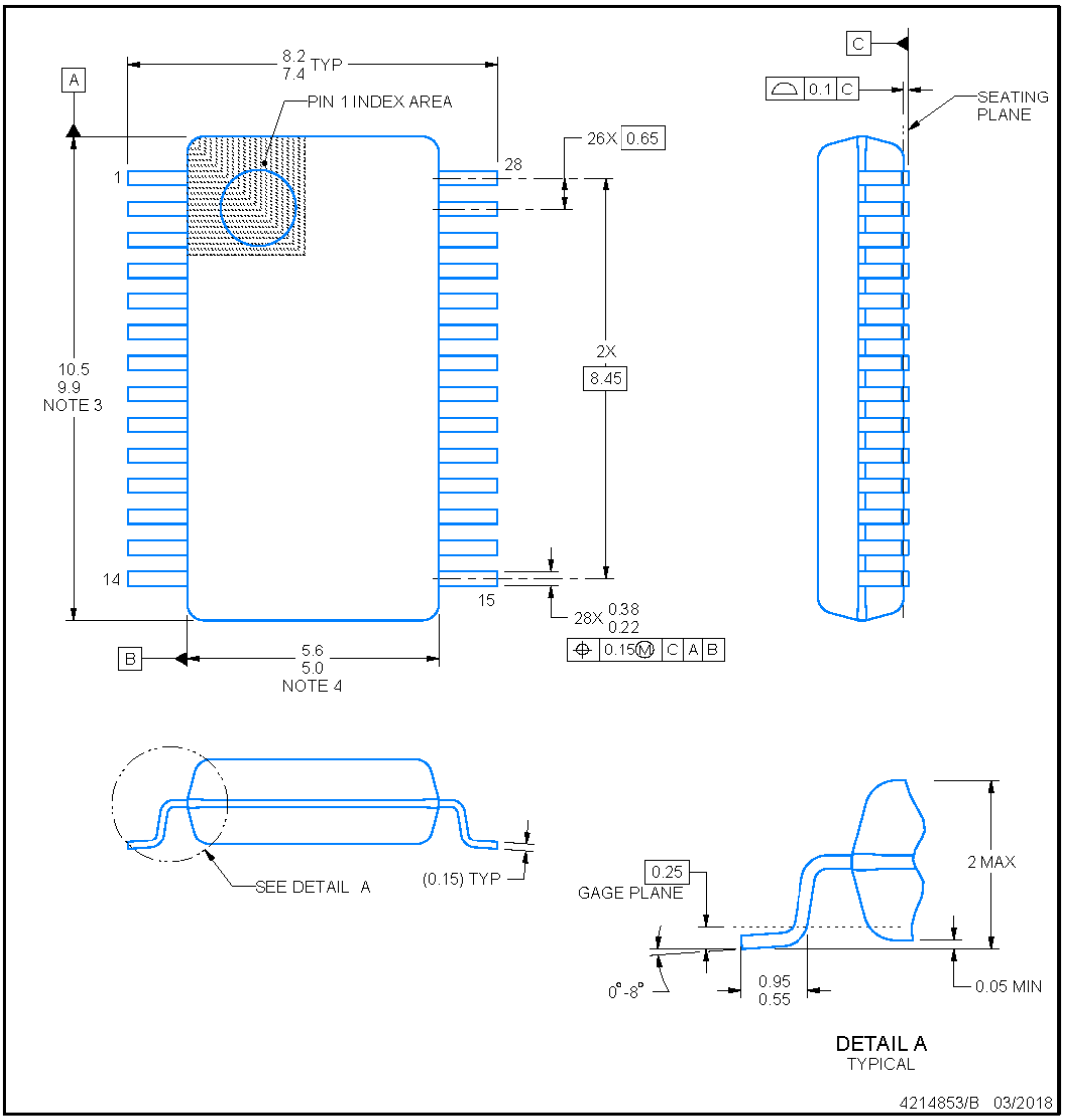


PACKAGE OUTLINE

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

www.ti.com

ADVANCE INFORMATION

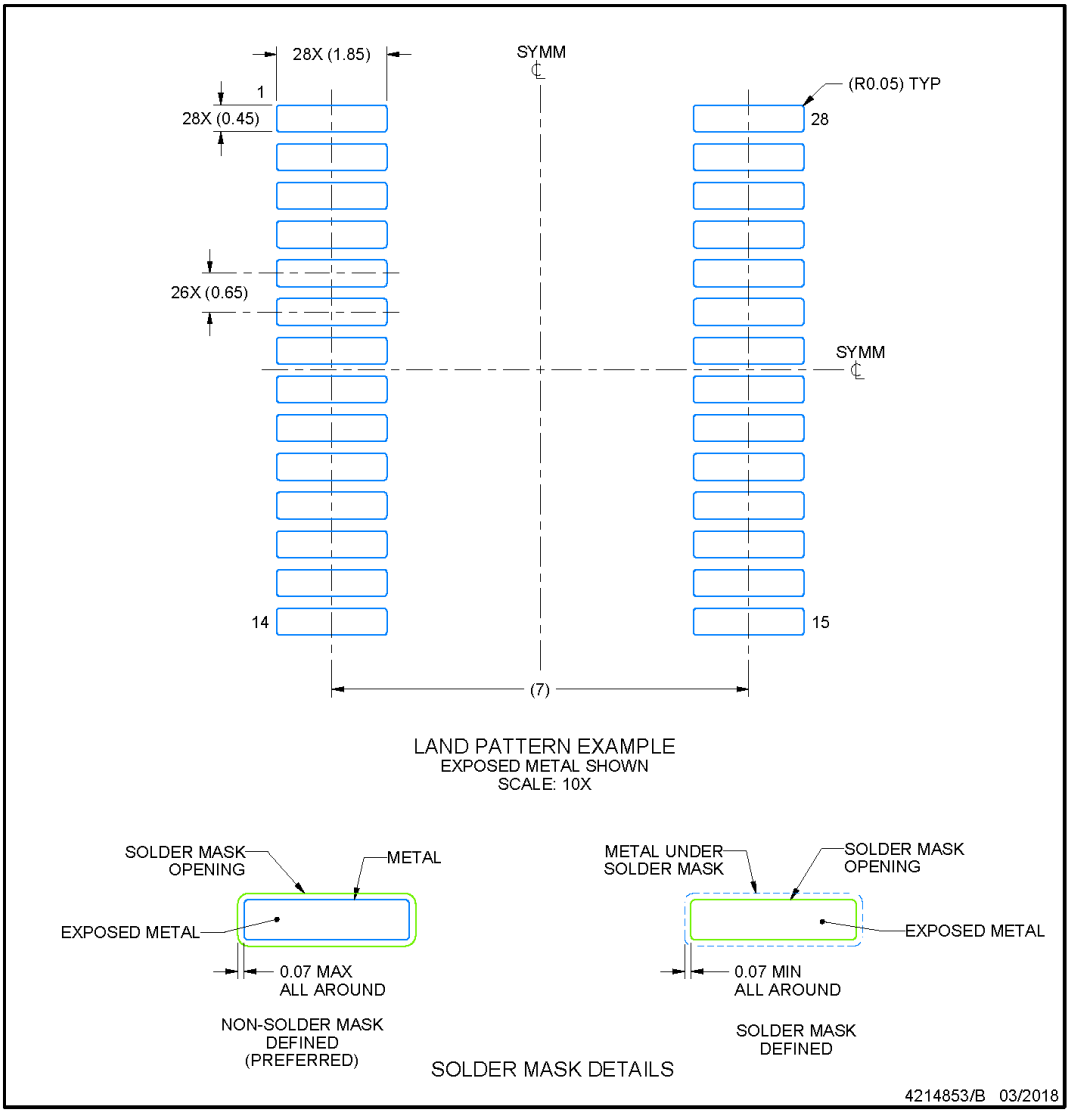
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ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DB0028A — **SSOP - 2 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

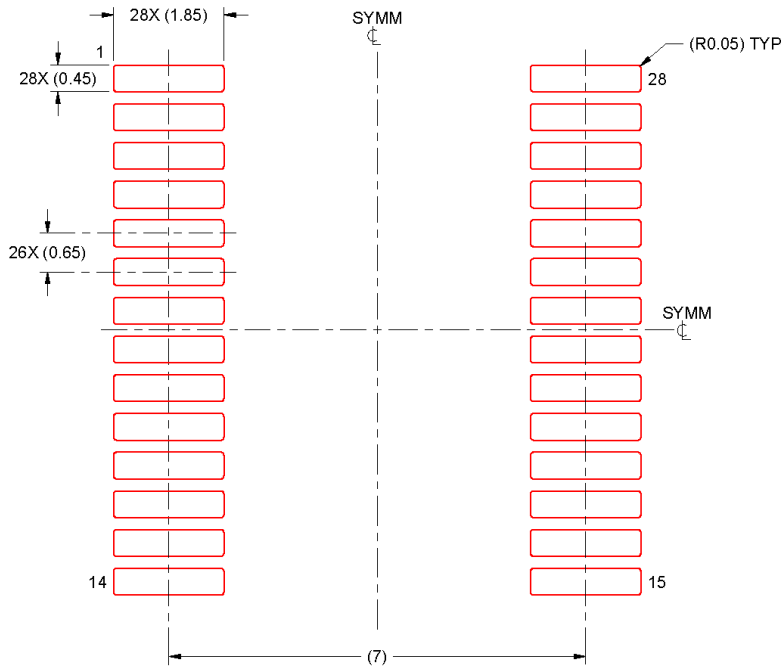
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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EXAMPLE STENCIL DESIGN

DB0028A — **SSOP - 2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

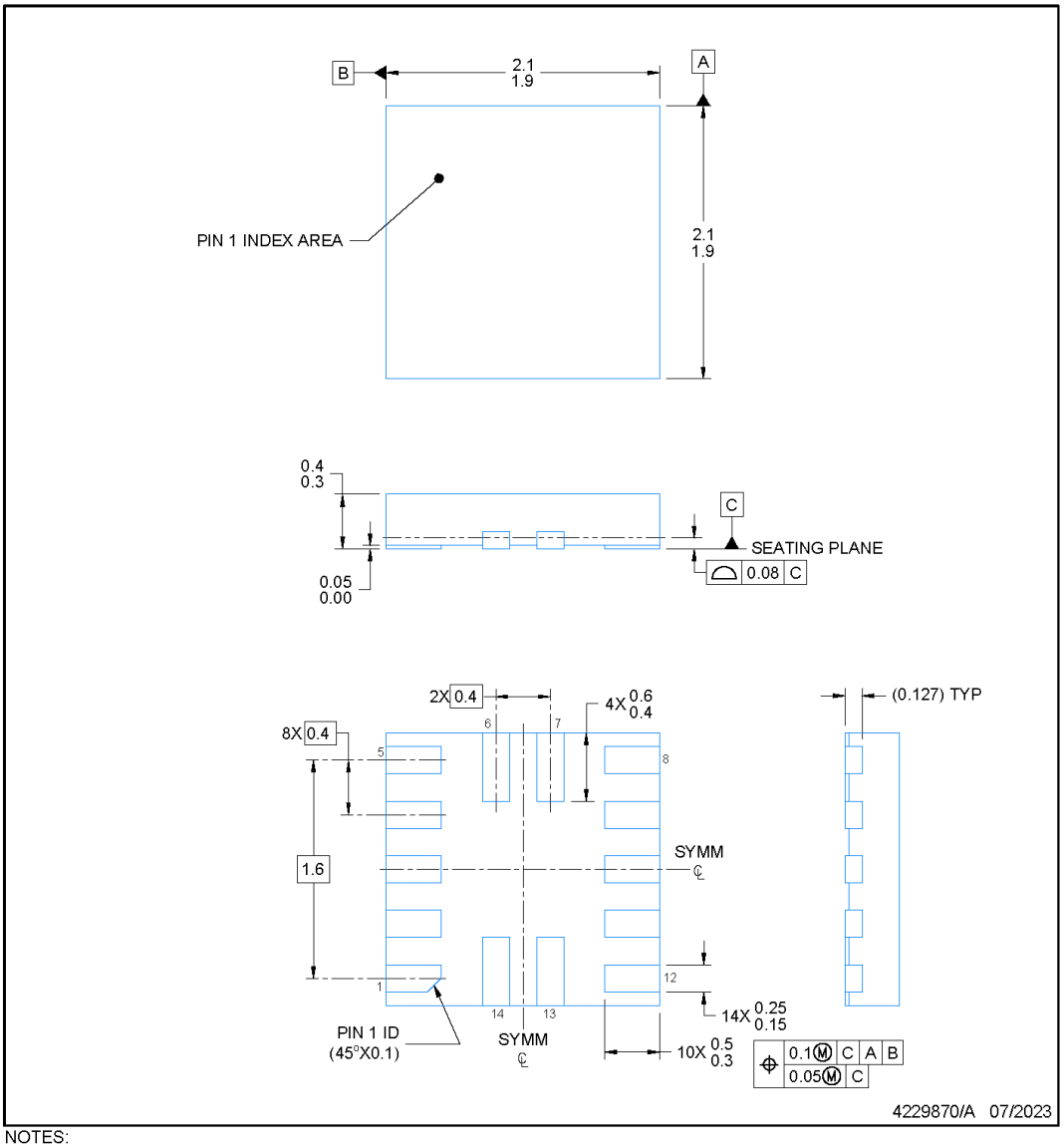
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ADVANCE INFORMATION

PACKAGE OUTLINE

RUC0014B — **X2QFN - 0.4 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

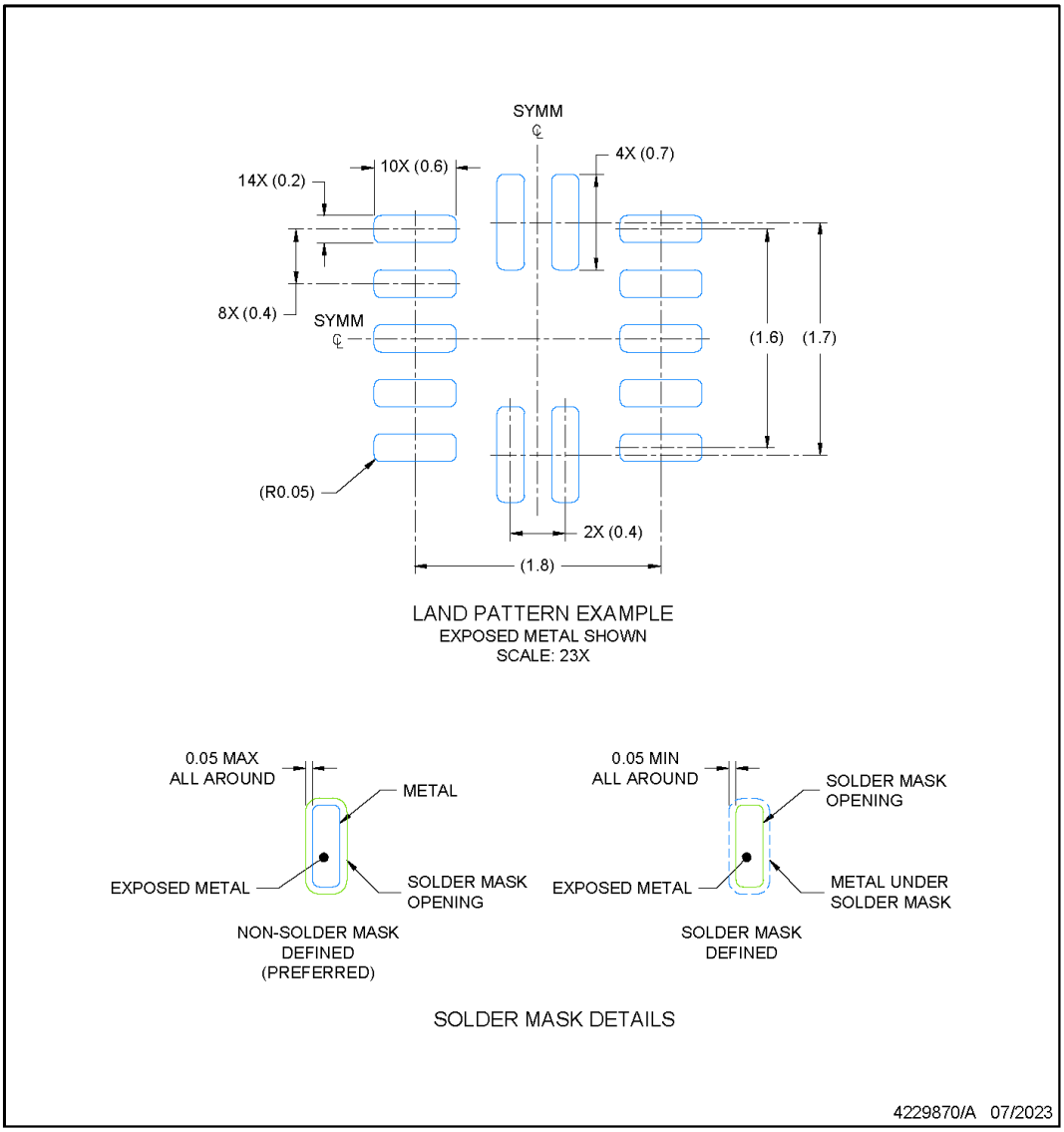
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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EXAMPLE BOARD LAYOUT

RUC0014B — **X2QFN - 0.4 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

ADVANCE INFORMATION

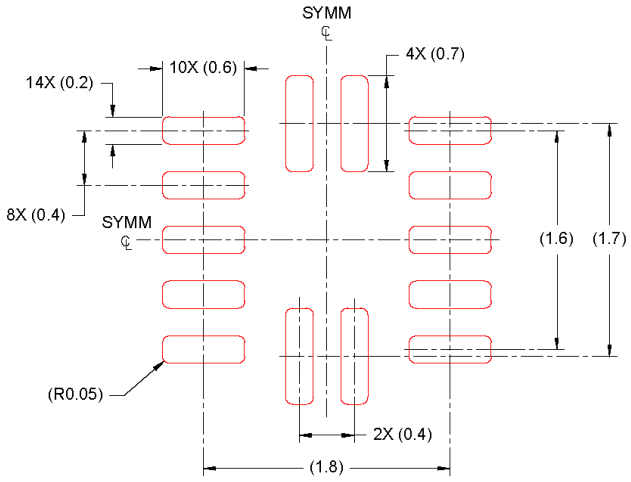
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ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RUC0014B — **X2QFN - 0.4 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4229870/A 07/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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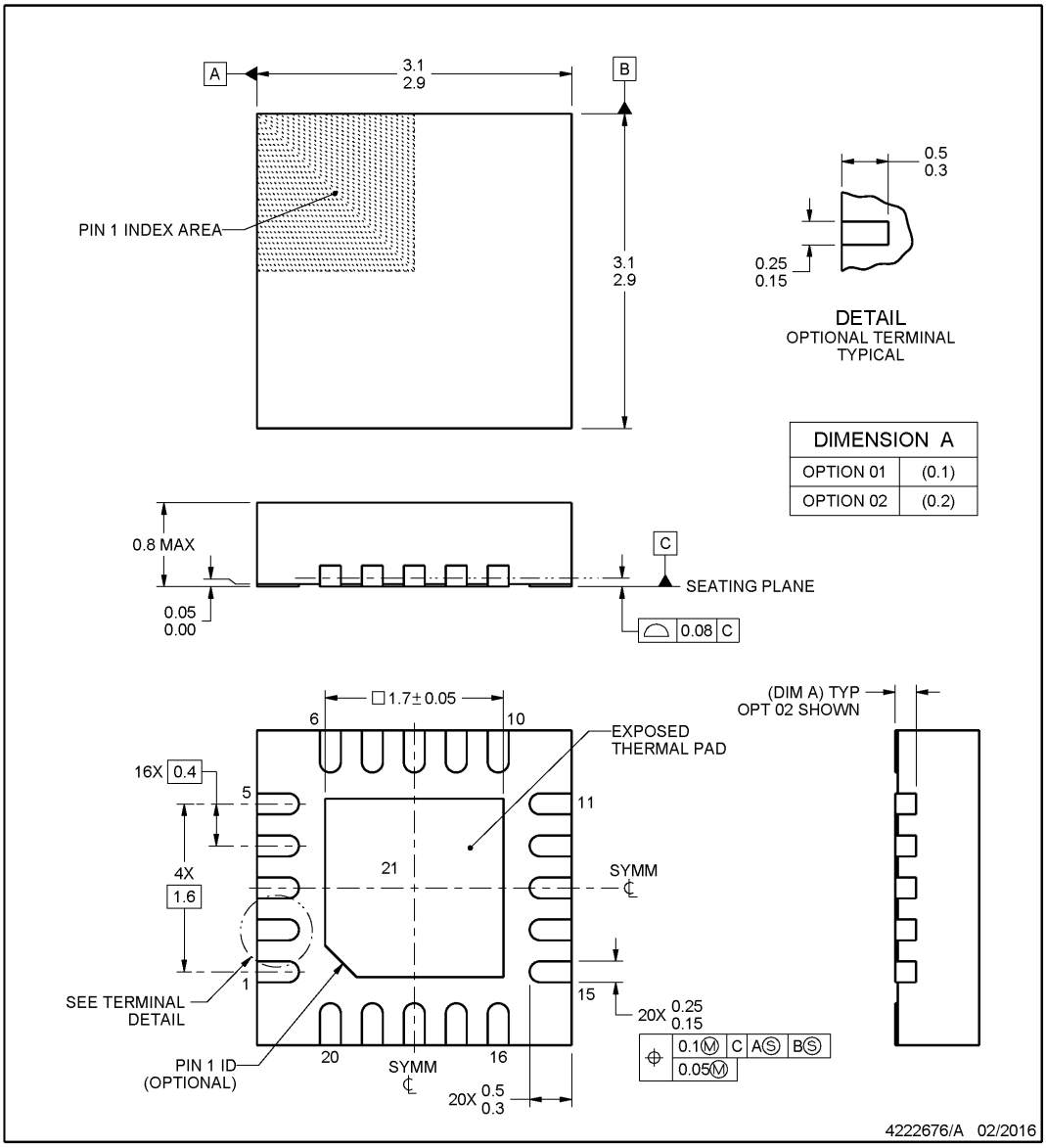
PACKAGE OUTLINE

RUK0020B



WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

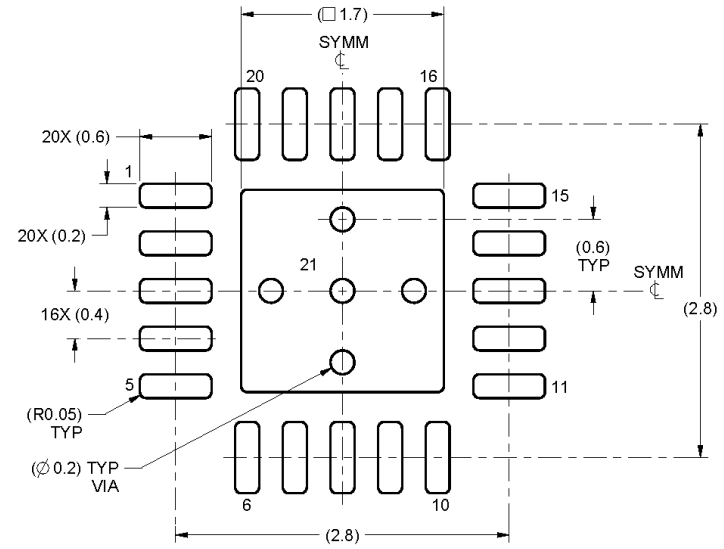
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ADVANCE INFORMATION

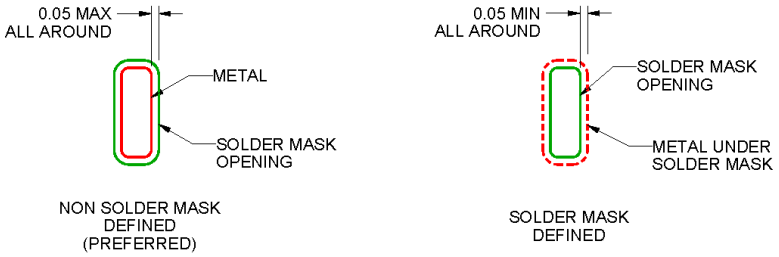
EXAMPLE BOARD LAYOUT

RUK0020B — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222676/A 02/2016

NOTES: (continued)

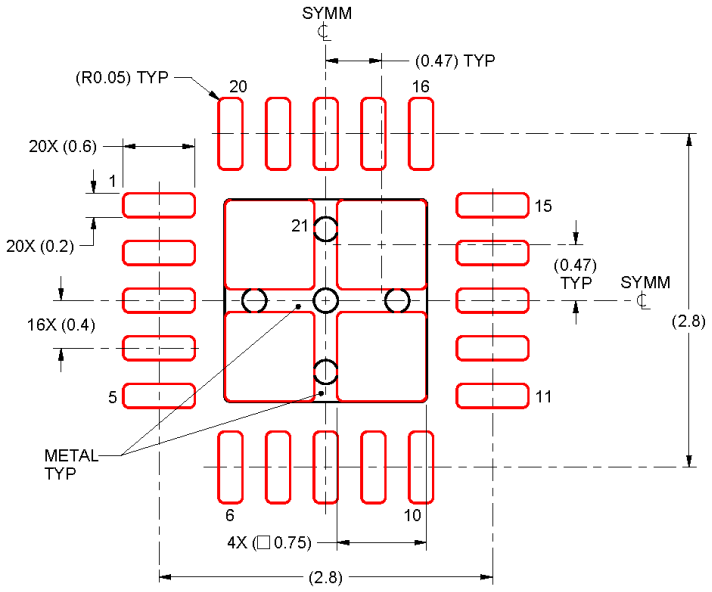
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

RUK0020B — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

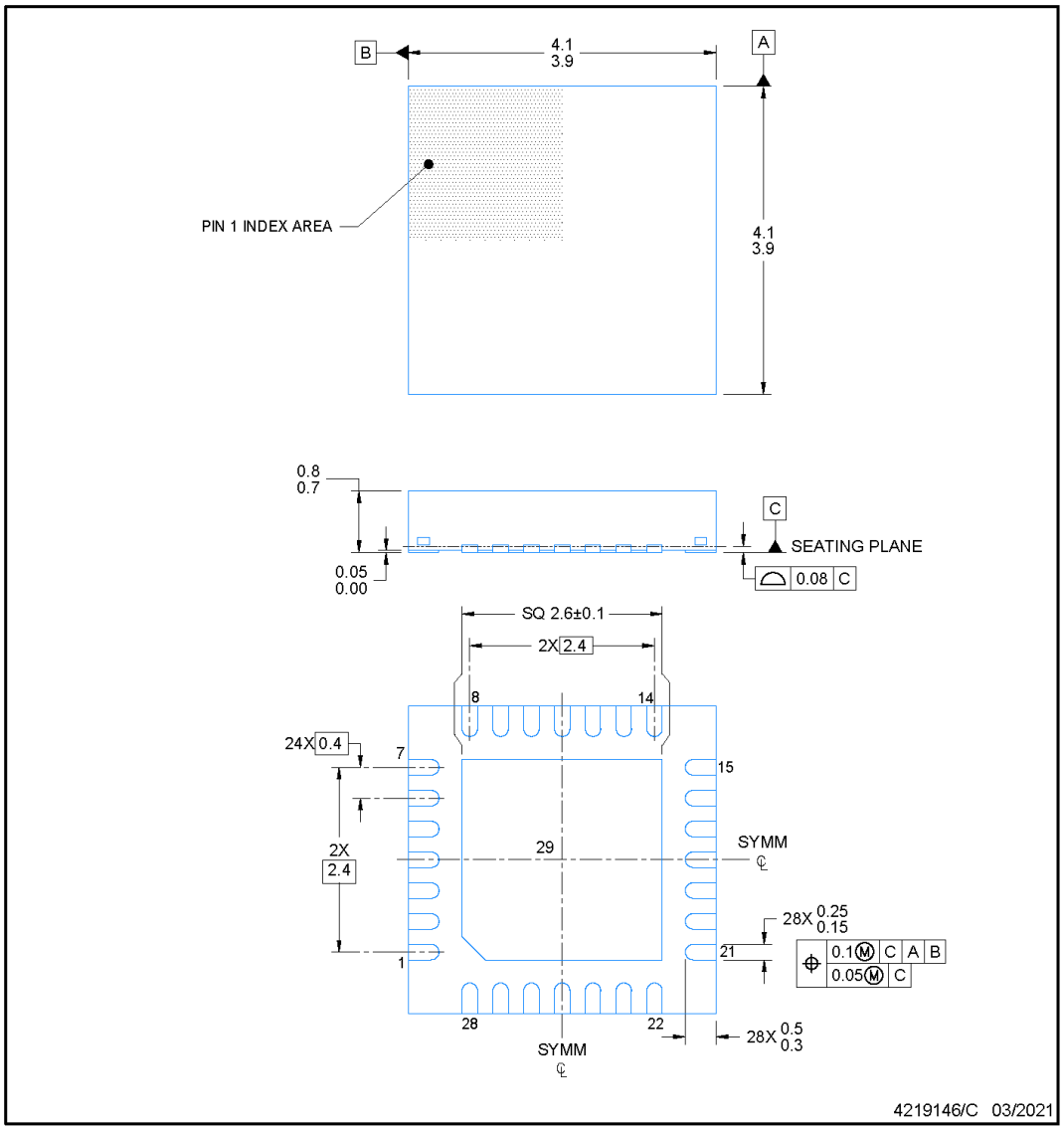
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ADVANCE INFORMATION

PACKAGE OUTLINE

RUY0028A — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

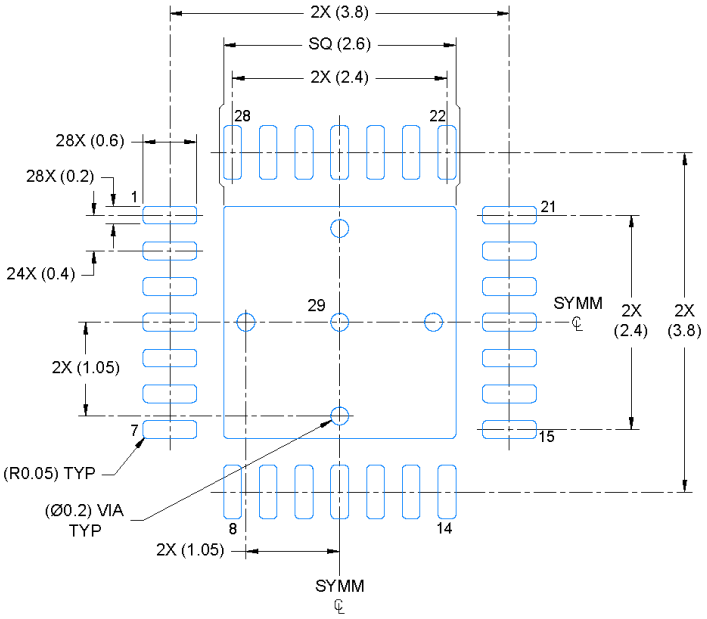
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

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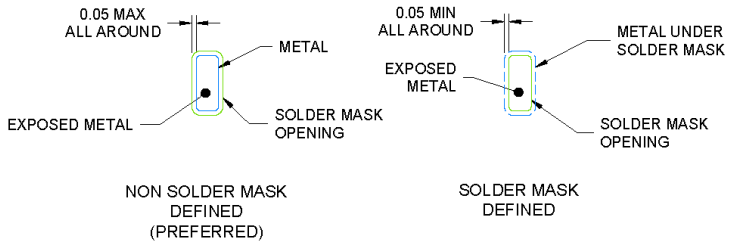
EXAMPLE BOARD LAYOUT

RUY0028A — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4219146/C 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

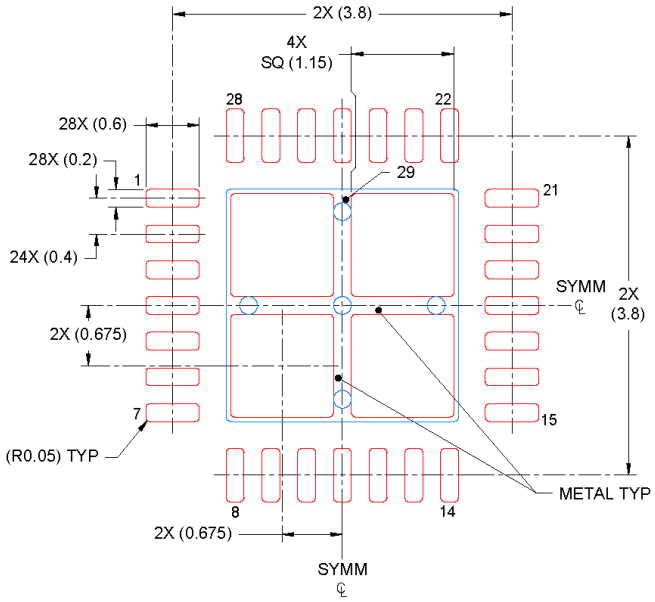
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ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RUY0028A — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 15X

4219146/C 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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