ADS1x1C0x Ultra-Small, Low-Power, 12- and 16-Bit, 6 and 4kSPS ADCs With PGA, Comparator, and Temperature Sensor

ADVANCE INFORMATION

1 Features

- Wide supply range: 1.74V to 5.5V
- Low current consumption:
  - 140µA in continuous-converison mode
- 12-bit data rate: 100SPS to 6kSPS
- 16-bit data rate: 10SPS to 4kSPS
- Single-cycle settling
- Internal temperature sensor
- Internal low-drift 1.024V reference
- Internal oscillator
- Four pin-selectable I^2C addresses
- ADS1x1C0xL compatible with 1.2V I^2C buses
- Digital comparator with ALERT output pin
- Operating temperature range: –40°C to +125°C

2 Applications

- Consumer electronics
- Portable instrumentation
- Leak detection in data centers
- Temperature measurement systems
- Factory automation and process control
- General purpose voltage and current monitoring

3 Description

The ADS101C0x and ADS111C0x (ADS1x1C0x) are precision, low-power, I^2C-compatible, 12- and 16-bit analog-to-digital converters (ADCs). The ADS1x1C0x integrate a low-drift voltage reference, oscillator, a programmable gain amplifier (PGA), a digital comparator, and high-accuracy temperature sensor. These features, along with the device wide power supply range from 1.74V to 5.5V, are useful for power- and space-constrained, sensor measurement applications.

The ADS101C0x and ADS111C0x perform conversions at data rates up to 6 and 4kSPS, respectively. The PGA offers gain settings from 1/6 to 16, allowing precise large- and small-signal measurements using the internal 1.024V reference. The ADS1x1C02 feature an input multiplexer (MUX) that allows four single-ended measurements, three differential measurements using AIN3 as a common reference, or two independent differential input pairs.

Package Information

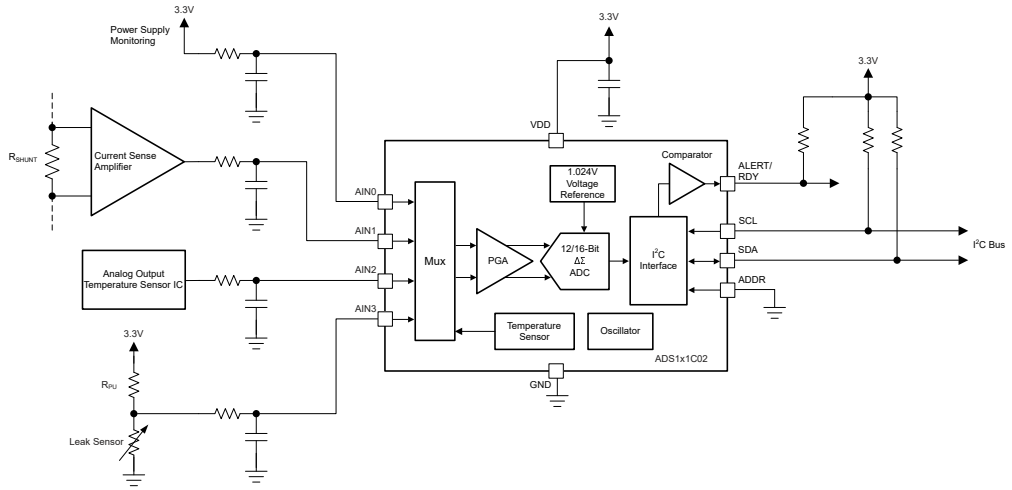
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS1x1C0x	RUG (X2QFN, 10)	1.50mm × 2.00mm
	DYN (TSOT, 10)	2.90mm × 2.80mm
	YCJ (DSBGA, 12)	1.38mm × 1.03mm

(1) For all available packages, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER	RESOLUTION(1)	DATA RATE (max)
ADS101C01	12-bit	6kSPS
ADS101C02	12-bit	6kSPS
ADS111C01	16-bit	4kSPS
ADS111C02	16-bit	4kSPS

(1) See the *Device Comparison Table* for details.



Server Card System Monitoring

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4 Device Comparison Table

DEVICE	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (SPS)	INPUT CHANNELS Differential (Single-Ended)	INTERFACE	DIGITAL I/O LEVELS
ADS101C01	12	6000	1 (1)	I²C	Ratiometric to VDD
ADS101C02	12	6000	2 (4)	I²C	Ratiometric to VDD
ADS111C01	16	4000	1 (1)	I²C	Ratiometric to VDD
ADS111C02	16	4000	2 (4)	I²C	Ratiometric to VDD
ADS101C01L	12	6000	1 (1)	I²C	Independent of VDD
ADS101C02L	12	6000	2 (4)	I²C	Independent of VDD
ADS111C01L	16	4000	1 (1)	I²C	Independent of VDD
ADS111C02L	16	4000	2 (4)	I²C	Independent of VDD
ADS101S02	12	6000	2 (4)	SPI	Ratiometric to VDD
ADS111S02	16	4000	2 (4)	SPI	Ratiometric to VDD

5 Pin Configuration and Functions

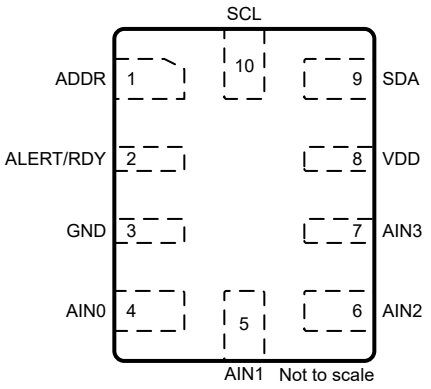


Figure 5-1. RUG Package, 10-Pin(Top View)

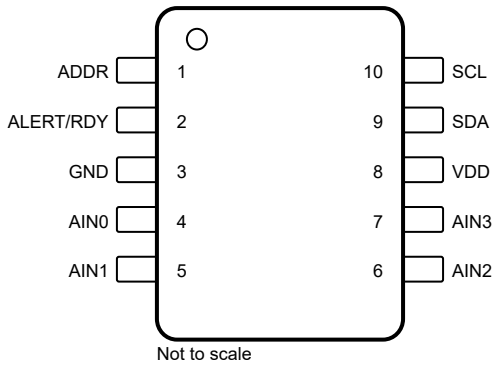


Figure 5-2. DYN Package, 10-Pin(Top View)

Table 5-1. Pin Functions: RUG and DYN Packages

PIN			TYPE	DESCRIPTION(1)
NO.	ADS1x1C01	ADS1x1C02		
1	ADDR	ADDR	Digital input	I²C target address select pin. See the *I²C Address Selection* section for details.
4	AIN0	AIN0	Analog input	Analog input 0
5	AIN1	AIN1	Analog input	Analog input 1
6	NC	AIN2	Analog input	Analog input 2 (ADS1x1C02 only)
7	NC	AIN3	Analog input	Analog input 3 (ADS1x1C02 only)
2	ALERT/RDY	ALERT/RDY	Digital output	Comparator output or conversion ready. Connect to VDD using a pullup resistor.(2)
3	GND	GND	Ground	Ground
9	SDA	SDA	Digital I/O	Serial data input and output. Connect to VDD using a pullup resistor.(2)
10	SCL	SCL	Digital input	Serial clock input. Connect to VDD using a pullup resistor.
8	VDD	VDD	Supply	Power supply. Connect a 0.1µF, power-supply decoupling capacitor to GND.

(1) See the *Unused Inputs and Outputs* section for unused pin connections.
(2) Open-drain output.

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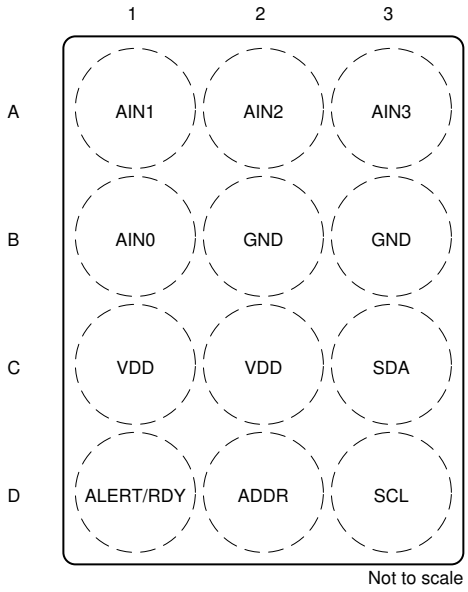


**Figure 5-3. YCJ Package,
12-Pin DSBGA(Top View)**

Table 5-2. Pin Functions: YCJ Package

PIN			TYPE	DESCRIPTION(1)
ADS1x1C01	ADS1x1C02	NAME		
D2	D2	ADDR	Digital input	I²C target address select pin. See the *I²C Address Selection* section for details.
B1	B1	AIN0	Analog input	Analog input 0
A1	A1	AIN1	Analog input	Analog input 1
—	A2	AIN2	Analog input	Analog input 2 (ADS1x1C02 only)
—	A3	AIN3	Analog input	Analog input 3 (ADS1x1C02 only)
D1	D1	ALERT/RDY	Digital output	Comparator output or conversion ready. Connect to VDD using a pullup resistor.(2)
B2, B3	B2, B3	GND	Ground	Ground
A2, A3	—	NC	—	No connect. Leave pin floating or connect to GND.
D3	D3	SCL	Digital input	Serial clock input. Connect to VDD using a pullup resistor.
C3	C3	SDA	Digital I/O	Serial data input and output. Connect to VDD using a pullup resistor.(2)
C1, C2	C1, C2	VDD	Supply	Power supply. Connect a 0.1µF, power-supply decoupling capacitor to GND.

(1) See the *Unused Inputs and Outputs* section for unused pin connections.
(2) Open-drain output.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	–0.3	7	V
Analog input voltage	AIN0, AIN1, AIN2, AIN3	GND – 0.3	VDD + 0.3	V
Digital input voltage	SCL, SDA, ADDR, ALERT/RDY	GND – 0.3	5.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Power supply	VDD to GND	1.74		5.5	V
ANALOG INPUTS(1)						
V_{AINx}	Absolute input voltage		GND		VDD	V
V_{IN}	Differential input voltage(2)(3)	Unipolar straight binary coding	0		V_{REF} / Gain	V
		Binary two's complement coding	$-V_{REF}$ / Gain		V_{REF} / Gain	
DIGITAL INPUTS						
	Input voltage		GND		5.5	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

(1) AIN_P and AIN_N denote the selected positive and negative inputs of the ADC.
(2) V_{REF} = 1.024V (typical)
(3) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3V or 5.5V (whichever is smaller) must be applied to this device. See Table 8-1 and Table 8-2 for more information.

6.4 Thermal Information

THERMAL METRIC(1)		DYN (TSOT)	RUG (X2QFN)	YCJ (DSBGA)	UNIT
		10 PINS	10 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	245.2	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	69.3	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	172	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	8.2	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	170.8	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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6.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at VDD = 1.74V to 5.5V, all data rates, all gain settings (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Absolute input current	GND ≤ V_{AINx} ≤ VDD, V_{IN} = 0V		±15		nA
	Differential input current	V_{CM} = VDD/2, –V_{REF}/Gain ≤ V_{IN} ≤ V_{REF}/Gain		±25		nA
	Common-mode input impedance	TBD		100		MΩ
	Differential input impedance	TBD		100		MΩ
SYSTEM PERFORMANCE						
	Resolution (no missing codes)	ADS101C01, ADS101C02, ADS101C01L, ADS101C02L	12			Bits
		ADS111C01, ADS111C02, ADS111C01L, ADS111C02L	16			
DR	Data rate	ADS101C01, ADS101C02, ADS101C01L, ADS101C02L	100, 500, 2000, 6000			SPS
		ADS111C01, ADS111C02, ADS111C01L, ADS111C02L	10, 100, 1000, 4000			
	Noise (input-referred)		See *Noise Performance* section			
INL	Integral nonlinearity (best fit)			TBD		ppm_{FSR}
	Gain settings		1/6, 1/4, 1/2, 1, 2, 4 ,8, 16			
	Offset error (input referred)	Differential inputs		±5		µV
		Single-ended inputs		±25		
	Offset drift	Differential inputs		40		nV/°C
		Single-ended inputs		150		
	Gain error	T_A = 25°C, including error of internal voltage reference	–0.5	±0.1	0.5	%
	Gain drift	Including drift of internal voltage reference		2.5	25	ppm/°C
V_{REF}	Reference voltage			1.024		V
CMRR	Common-mode rejection ratio	At dc		120		dB
		f_{CM} = 50Hz or 60Hz, DR = TBD		105		
PSRR	Power-supply rejection ratio	At dc		100		dB
OSCILLATOR						
f_{OSC}	Frequency			1000		kHz
	Accuracy	All data rates	–5		5	%
TEMPERATURE SENSOR						
	Temperature resolution	ADS101C01, ADS101C02, ADS101C01L, ADS101C02L		0.125		°C/LSB
		ADS111C01, ADS111C02, ADS111C01L, ADS111C02L		0.03125		
	Accuracy	T_A = –40°C to +125°C, ADS101C01, ADS101C02, ADS101C01L, ADS101C02L	–1	±0.25	1	°C
		T_A = –40°C to +125°C, ADS111C01, ADS111C02, ADS111C01L, ADS111C02L	–1	±0.25	1	
DIGITAL INPUTS/OUTPUTS						
V_{IL}	Logic input level, low	ADS1x1C0x	GND		0.3 VDD	V
		ADS1x1C0xL	GND		0.5	
V_{IH}	Logic input level, high	ADS1x1C0x	0.7 VDD		5.5	V
		ADS1x1C0xL	0.8		5.5	
V_{hys}	Hysteresis of Schmitt-trigger inputs		180			mV
V_{OL}	Logic output level, low	I_{OL} = 3mA	GND		0.3	V
I_{OL}	Low-level output current	V_{OL} = 0.4V, fast-mode plus, VDD = 1.74V to 2.0V	12			mA
		V_{OL} = 0.4V, fast-mode plus, VDD = 2.0V to 5.5V	20			
		V_{OL} = 0.6V, fast-mode	6			

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minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at VDD = 1.74V to 5.5V, all data rates, all gain settings (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Capacitance	Each pin			10	pF
	Input current	GND ≤ $V_{Digital\ Input}$ ≤ VDD	–1		1	µA
SUPPLY CURRENT AND POWER DISSIPATION						
I_{VDD}	Supply current	Power-down		2.5	10	µA
		Operating		140	220	
P_D	Power dissipation	VDD = 5.5V		0.9		mW
		VDD = 3.3V		0.5		
		VDD = 1.74V		0.2		

6.6 I²C Timing Requirements

over operating ambient temperature range and VDD = 1.74V to 5.5V, bus capacitance= 10pF to 400pF, and pullup resistor = 1kΩ (unless otherwise noted)

		MIN	MAX	UNIT
STANDARD-MODE				
f_{SCL}	SCL clock frequency	0	100	kHz
$t_{HD;STA}$	Hold time, (repeated) START condition. After this period, the first clock pulse is generated.	4		µs
t_{LOW}	Pulse duration, SCL low	4.7		µs
t_{HIGH}	Pulse duration, SCL high	4.0		µs
$t_{SU;STA}$	Setup time, repeated START condition	4.7		µs
$t_{HD;DAT}$	Hold time, data	0		µs
$t_{SU;DAT}$	Setup time, data	250		ns
t_r	Rise time, SCL, SDA		1000	ns
t_f	Fall time, SCL, SDA		250	ns
$t_{SU;STO}$	Setup time, STOP condition	4.0		µs
t_{BUF}	Bus free time, between STOP and START conditions	4.7		µs
$t_{VD;DAT}$	Valid time, data		3.45	µs
$t_{VD;ACK}$	Valid time, acknowledge		3.45	µs
FAST-MODE				
f_{SCL}	SCL clock frequency	0	400	kHz
$t_{HD;STA}$	Hold time, (repeated) START condition. After this period, the first clock pulse is generated.	0.6		µs
t_{LOW}	Pulse duration, SCL low	1.3		µs
t_{HIGH}	Pulse duration, SCL high	0.6		µs
$t_{SU;STA}$	Setup time, repeated START condition	0.6		µs
$t_{HD;DAT}$	Hold time, data	0		µs
$t_{SU;DAT}$	Setup time, data	100		ns
t_r	Rise time, SCL, SDA	20	300	ns
t_f	Fall time, SCL, SDA		250	ns
$t_{SU;STO}$	Setup time, STOP condition	0.6		µs
t_{BUF}	Bus free time, between STOP and START conditions	1.3		µs
$t_{VD;DAT}$	Valid time, data		0.9	µs
$t_{VD;ACK}$	Valid time, acknowledge		0.9	µs
t_{SP}	Pulse duration of spikes that must be suppressed by the input filter	0	50	ns

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over operating ambient temperature range and VDD = 1.74V to 5.5V, bus capacitance= 10pF to 400pF, and pullup resistor = 1kΩ (unless otherwise noted)

			MIN	MAX	UNIT
FAST-MODE PLUS					
f_{SCL}	SCL clock frequency		0	1000	kHz
$t_{HD;STA}$	Hold time, (repeated) START condition. After this period, the first clock pulse is generated.		0.26		µs
t_{LOW}	Pulse duration, SCL low		0.5		µs
t_{HIGH}	Pulse duration, SCL high		0.26		µs
$t_{SU;STA}$	Setup time, repeated START condition		0.26		µs
$t_{HD;DAT}$	Hold time, data		0		µs
$t_{SU;DAT}$	Setup time, data		50		ns
t_r	Rise time, SCL, SDA			120	ns
t_f	Fall time, SCL, SDA			120	ns
$t_{SU;STO}$	Setup time, STOP condition		0.26		µs
t_{BUF}	Bus free time, between STOP and START conditions		0.5		µs
$t_{VD;DAT}$	Valid time, data			0.45	µs
$t_{VD;ACK}$	Valid time, acknowledge			0.45	µs
t_{SP}	Pulse duration of spikes that must be suppressed by the input filter		0	50	ns
TIMEOUT					
	Timeout	TBD		TBD	TBD

6.7 Timing Diagram

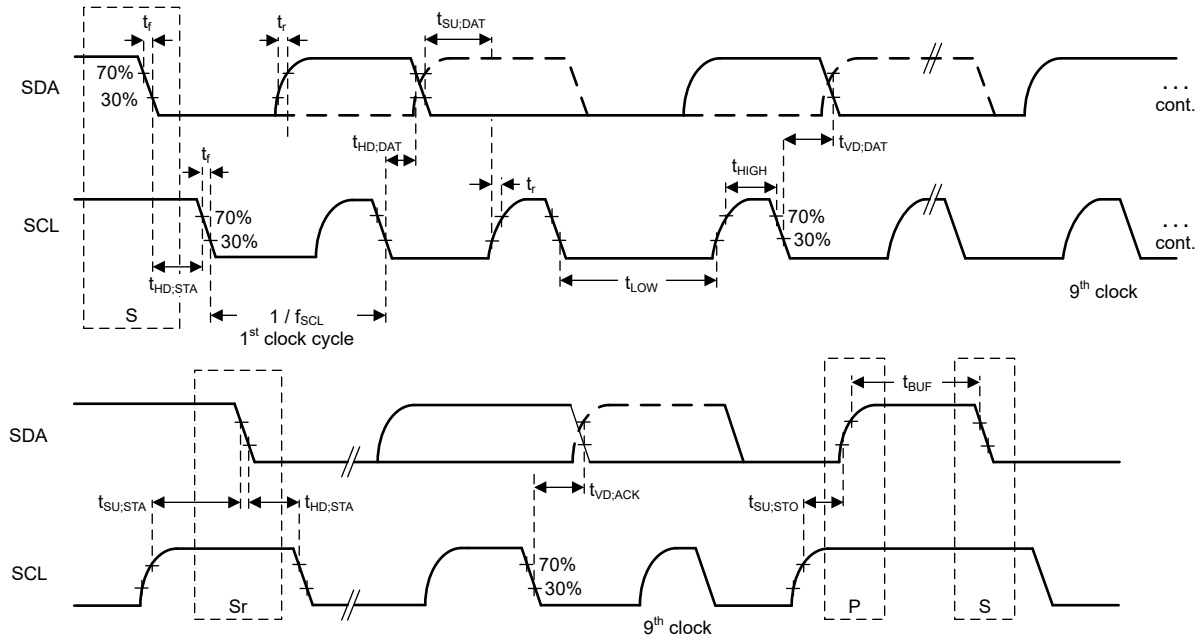


Figure 6-1. I²C Timing Requirements

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7 Parameter Measurement Information

7.1 Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called *oversampling ratio* (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

Table 7-1 and Table 7-2 show the input-referred noise in units of μV_{RMS} for the conditions shown. The effective resolution values are shown in parenthesis. The effective resolution is calculated from μV_{RMS} values using the following equation. Data are representative of typical noise performance at T_A = 25°C with the inputs shorted together externally using two's compliment data coding.

$$\text{Effective Resolution} = \ln\left[2 \times \frac{V_{REF}}{\text{Gain} \times V_{\text{RMS Noise}}}\right] \div \ln[2] \quad (1)$$

Table 7-1. Noise in μV_{RMS} (Effective Resolution) for 12-Bit Device at VDD = 3.3V

DATA RATE (SPS)	GAIN							
	1/6	1/4	1/2	1	2	4	8	16
100	45.4 (12)	32.8 (12)	15.9 (12)	8.1 (12)	4.6 (12)	4.6 (12)	4.6 (12)	4.6 (12)
500	90.6 (12)	60.9 (12)	29.3 (12)	15.0 (12)	7.7 (12)	7.6 (12)	7.4 (12)	7.3 (12)
2000	172 (12)	114 (12)	56.9 (12)	28.6 (12)	14.4 (12)	14.3 (12)	14.3 (12)	14.3 (12)
6000	412 (12)	274 (12)	136 (12)	68.3 (12)	35.8 (12)	35.8 (12)	35.4 (12)	34.7 (11.8)

Table 7-2. Noise in μV_{RMS} (Effective Resolution) for 16-Bit Device at VDD = 3.3V

DATA RATE (SPS)	GAIN							
	1/6	1/4	1/2	1	2	4	8	16
10	9.8 (16)	6.9 (16)	3.4 (16)	1.6 (16)	0.83 (16)	0.83 (16)	0.83 (16)	0.83 (16)
100	32.6 (16)	22.2 (16)	11.0 (16)	5.4 (16)	2.7 (16)	2.7 (16)	2.7 (16)	2.7 (16)
1000	112 (16)	74.5 (16)	37.2 (16)	18.6 (16)	9.2 (16)	9.2 (15.7)	9.2 (14.7)	9.2 (13.7)
4000	307 (15.3)	204 (15.3)	102 (15.3)	51.3 (15.3)	25.6 (15.3)	25.6 (14.3)	25.6 (13.3)	25.6 (12.3)

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8 Detailed Description

8.1 Overview

The ADS1x1C0x are a very small, low-power, 12- and 16-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs). The ADS1x1C0x consist of a ΔΣ ADC core with adjustable gain, an internal voltage reference, a clock oscillator, and an I^2C interface. These devices integrate a highly linear and accurate temperature sensor. All of these features are intended to reduce required external circuitry and improve performance. Figure 8-1 and Figure 8-2 show the ADS1x1C0x functional block diagrams.

The ADS1x1C0x ADC core measures a differential signal, V_{IN}, that is the difference of V_{AINP} and V_{AINN}. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. This architecture results in a very strong attenuation of any common-mode signals. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1x1C0x have two available conversion modes: single-shot and continuous-conversion. In single-shot conversion mode, the ADC performs one conversion of the input signal upon request, stores the conversion value to an internal 16-bit Device Conversion Register and then enters a power-down state. This mode is intended to provide significant power savings in systems that only require periodic conversions or when there are long idle periods between conversions. In continuous-conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion completes. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recently completed conversion.

8.2 Functional Block Diagrams

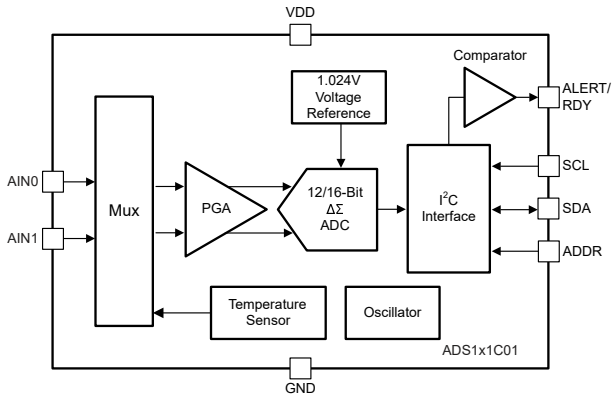


Figure 8-1. ADS1x1C01 Block Diagram

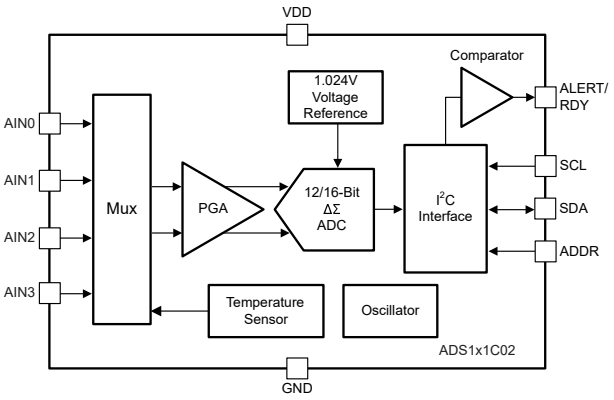


Figure 8-2. ADS1x1C02 Block Diagram

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8.3 Feature Description

8.3.1 Multiplexer

Figure 8-3 shows the input multiplexer (MUX) for the ADS1x1C02. The input multiplexer supports four single-ended measurements referenced to ground, three differential measurements using AIN3 as a common reference input, or two independent differential input pairs. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer. The multiplexer is configured by the MUX[2:0] bits.

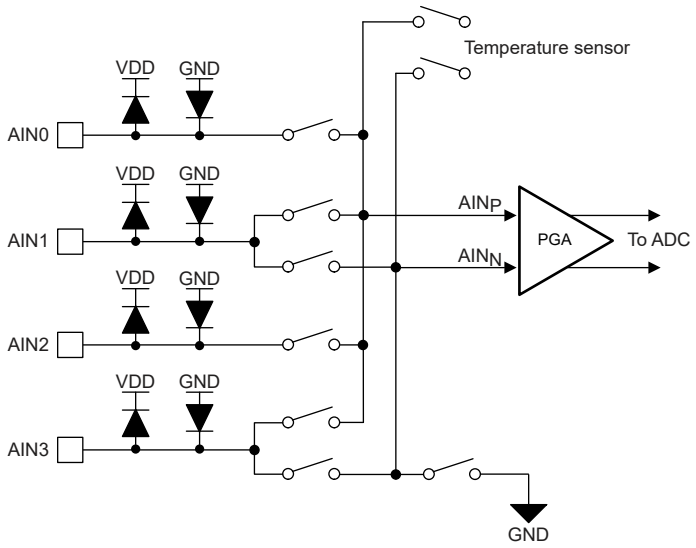


Figure 8-3. Input Multiplexer

The ADS1x1C01 does not have an input multiplexer and can measure either one differential signal or one single-ended signal. For single-ended measurements, connect the AIN1 pin to GND externally. In subsequent sections of this document, AIN_P refers to AIN0 and AIN_N refers to AIN1 for the ADS1x1C01.

Electrostatic discharge (ESD) diodes connected to VDD and GND protect the ADS1x1C0x analog inputs. Keep the absolute voltage of any input within the range shown in Equation 2 to prevent the ESD diodes from turning on.

$$GND - 0.3V < V_{AINx} < VDD + 0.3V \quad (2)$$

External Schottky clamp diodes or series resistors can be required to limit the input current to safe values (see the *Absolute Maximum Ratings*). Overdriving an unselected input on the device can affect conversions taking place on other input pins.

8.3.2 Voltage Reference

The ADS1x1C0x have an integrated 1.024V voltage reference. An external reference cannot be used with these devices. Errors associated with the internal voltage reference accuracy and the reference drift with temperature are included in the gain error and gain drift specifications in the *Electrical Characteristics* table.

8.3.3 Oscillator

The ADS1x1C0x have an integrated 1MHz oscillator. No external clock can be applied to operate these devices. The frequency at which the input signal is sampled is called the sampling frequency or the modulator frequency (f_{MOD}). The 1MHz oscillator frequency is internally divided by a factor of 4 to generate the modulator frequency, f_{MOD} = 250kHz. The internal oscillator drifts over temperature and time. The output data rate scales proportionally with the oscillator frequency.

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8.3.4 Output Data Rate and Conversion Time

The ADS1x1C0x offer programmable output data rates. Use the DR[1:0] bits to select output data rates of 100SPS, 500SPS, 2kSPS, or 6kSPS for ADS101C0x and 10SPS, 100SPS, 1kSPS, or 4kSPS for ADS111C0x. Conversions in the ADS1x1C0x settle within a single cycle. The conversion time is equal to 1 / DR.

8.3.5 Low-Noise PGA

The ADS1x1C0x integrate a low-noise, low-drift, high input impedance programmable gain amplifier (PGA). Use the PGA[2:0] bits to configure the PGA for gains of 1/6, 1/4, 1/2, 1, 2, 4, 8, or 16. Equation 3 and Equation 4 show how to calculate the full-scale range (FSR), based on the ADC conversion coding using the internal 1.024V reference.

$$FSR_{\text{Binary two's complement coding}} = \pm VREF / Gain \quad (3)$$

$$FSR_{\text{Unipolar straight binary coding}} = 0V \text{ to } +VREF / Gain \quad (4)$$

Use Equation 5 to calculate the LSB size from the FSR and device resolution, n. Table 8-1 summarizes the full-scale range and LSB size when using binary two's compliment coding for all the gain settings, and Table 8-2 shows the full-scale range and LSB size when using unipolar straight binary coding.

$$LSB = FSR / 2^n \quad (5)$$

Table 8-1. Full-Scale Range and LSB Size for Binary Two's Complement Coding

GAIN	FSR	LSB SIZE	
	Binary Two's Compliment	12 Bit	16 Bit
1/6	±6.144V(1)	3mV	187.5µV
1/4	±4.096V(1)	2mV	125µV
1/2	±2.048V	1mV	62.5µV
1	±1.024V	0.5mV	31.25µV
2	±0.512V	0.25mV	15.625µV
4	±0.256V	0.125mV	7.813µV
8	±0.128V	62.5µV	3.906µV
16	±0.064V	31.25µV	1.953µV

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3V to the analog inputs of the device.

Table 8-2. Full-Scale Range and LSB Size for Unipolar Straight Binary Coding

GAIN	FSR	LSB SIZE	
	Unipolar Straight Binary	12 Bit	16 Bit
1/6	6.144V(1)	1.5mV	93.75µV
1/4	4.096V(1)	1mV	62.5µV
1/2	2.048V	0.5mV	31.25µV
1	1.024V	0.25mV	15.625µV
2	0.512V	0.125mV	7.813µV
4	0.256V	62.5µV	3.906µV
8	0.128V	31.25µV	1.953µV
16	0.064V	15.625µV	0.9766µV

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3V to the analog inputs of the device.

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8.3.6 Temperature Sensor

The ADS1x1C0x provide an integrated precision temperature sensor to measure the die temperature. To enable the temperature sensor, set bit TS_EN = 1b. When the temperature sensor is enabled, the MUX[2:0] bit settings have no effect. Temperature readings follow the same process as the analog inputs for starting conversions and reading conversion results.

Temperature data formats differ between devices: the ADS101C0x use 12-bit representation while the ADS111C0x use 14-bit representation. The temperature data are left-justified within the 16-bit conversion register in both cases.

8.3.6.1 12-Bit Temperature Data Format (ADS101C0x)

The ADS101C0x temperature data are represented as a 12-bit result that is left-justified within the 16-bit conversion register. One 12-bit LSB equals 0.125°C. Negative numbers are represented in binary two's complement format, as shown in Table 8-3

Table 8-3. 12-Bit Temperature Data Format (ADS101C0x)

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0100 0000 0000	400h
75	0010 0101 1000	258h
50	0001 1001 0000	190h
25	0000 1100 1000	0C8h
0.25	0000 0000 0010	002h
0	0000 0000 0000	000h
–0.25	1111 1111 1110	FFEh
–25	1111 0011 1000	F38h
–40	1110 1100 0000	EC0h

8.3.6.2 Converting from Digital Codes to Temperature, 12-Bit Temperature Sensor Data

To convert from digital codes to temperature, first read the data bytes from the device and extract the 12-bit temperature value by right-shifting the result. Figure 8-4 shows the 12-bit temperature sensor data alignment within the 16-bit conversion register. The MSB of the 12-bit value determines the sign: 0b indicates a positive temperature and 1b indicates a negative temperature. For positive temperatures convert the 12-bit binary value to decimal and multiply the result by the temperature sensor LSB size, 0.125°C. For negative temperatures, the value is in two's compliment format. Invert all 12 bits and add 1b, convert to decimal, and multiply the result by the negative temperature sensor LSB size, –0.125°C.

1. Positive temperature example: The device reads back 258h. 258h × 0.125°C = 600 × 0.125°C = 75°C

2. Negative temperature example: The device reads back F38h. Subtract 1b and complement the result: F38h → 0C8h, 0C8h × (–0.125°C) = 200 × (–0.125°C) = –25°C

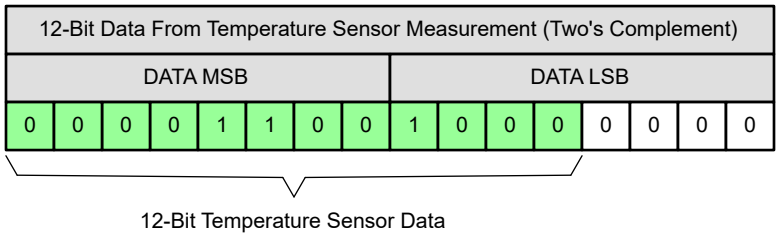


Figure 8-4. 12-Bit Temperature Sensor Data Alignment Within 16-Bit Conversion Register

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8.3.6.3 14-Bit Temperature Data Format (ADS101C0x)

The ADS111C0x temperature data are represented as a 14-bit result that is left-justified within the 16-bit conversion result. One 14-bit LSB equals 0.03125°C. Negative numbers are represented in binary two's complement format, as shown in Table 8-4

Table 8-4. 14-Bit Temperature Data Format (ADS111C0x)

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	01 0000 0000 0000	1000h
50	00 0110 0100 0000	0640h
25	00 0011 0010 0000	0320h
0.25	00 0000 0000 1000	0008h
0.03125	00 0000 0000 0001	0001h
0	00 0000 0000 0000	0000h
–0.25	11 1111 1111 1000	3FFFh
–25	11 1100 1110 0000	3CE0h
–40	11 1011 0000 0000	3B00h

8.3.6.4 Converting from Digital Codes to Temperature, 14-Bit Temperature Sensor Data

To convert from digital codes to temperature, first read the data bytes from the device and extract the 14-bit temperature value by right-shifting the result. Figure 8-5 shows the 14-bit temperature sensor data alignment within the 16-bit conversion result. The MSB of the 14-bit value determines the sign: 0b indicates a positive temperature and 1b indicates a negative temperature. For positive temperatures convert the 14-bit binary value to decimal and multiply the result by the temperature sensor LSB size, 0.03125°C. For negative temperatures, the value is in two's compliment format. Invert all 14 bits and add 1b, convert to decimal, and multiply the result by the negative temperature sensor LSB size, –0.03125°C.

1. Positive temperature example: The device reads back 0960h. 0960h × 0.03125°C = 2400 × 0.03125°C = 75°C

2. Negative temperature example: The device reads back 3CE0h. Subtract 1b and complement the result. 3CE0h → 0320h, 0320h × (–0.03125°C) = 800 × (–0.03125°C) = –25°C

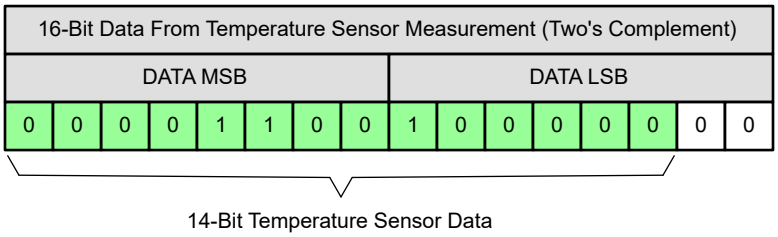


Figure 8-5. 14-Bit Temperature Sensor Data Alignment Within 16-Bit Conversion Result

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8.3.7 Digital Comparator

The ADS1x1C0x feature a programmable digital comparator that can issue an alert on the open-drain ALERT/RDY pin. The COMP_MODE bit configures the comparator as either a traditional comparator or a window comparator. In traditional comparator mode the ALERT/RDY pin asserts, when conversion data exceed the limit set in the high-threshold register (HIGH_TH). The comparator then deasserts only when the conversion data falls below the limit set in the low-threshold register (LOW_TH). In window comparator mode the ALERT/RDY pin asserts when the conversion data exceed the HIGH_TH register or fall below the LOW_TH register value. The ALERT/RDY pin can be configured as active high or active low by the COMP_POL bit.

In either window or traditional comparator mode, the comparator can be configured to latch after being asserted by the COMP_LAT bit. This setting causes the assertion to remain even if the input signal is not beyond the bounds of the threshold registers. This latched assertion can only be cleared by issuing an SMBus alert response or by reading the Conversion register. Figure 8-6 shows operational diagrams for both comparator modes with COMP_POL = 0b (active low).

The comparator can also be configured to activate the ALERT/RDY pin only after a set number of successive readings exceed the threshold values set in the Threshold Registers. The COMP_QUE[1:0] bits configure the comparator to wait for one, two, or four readings beyond the threshold before activating the ALERT/RDY pin. The COMP_QUE[1:0] bits can also disable the comparator function and put the ALERT/RDY pin into a high impedance state.

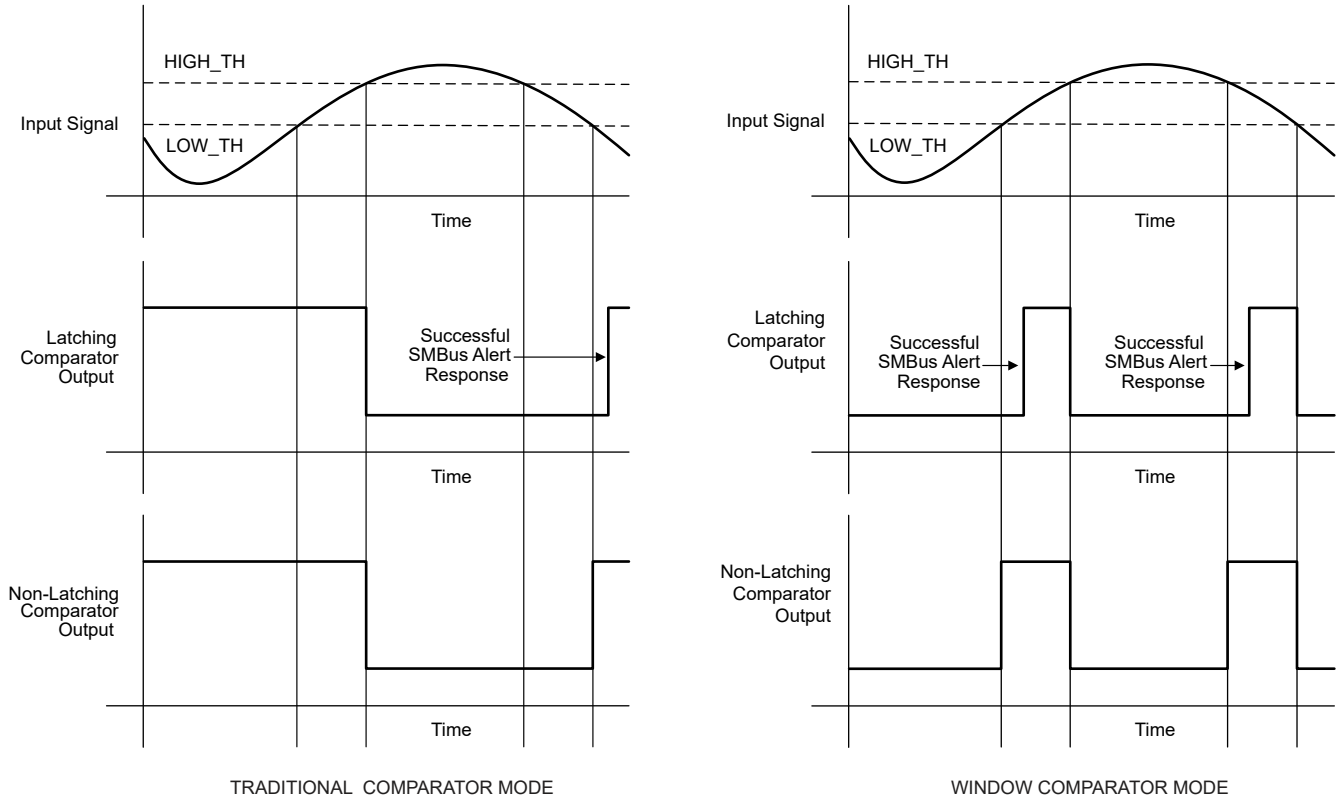


Figure 8-6. ALERT Pin Timing Diagram

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8.3.8 Conversion-Ready Pin

The open-drain ALERT/RDY pin can also be configured as a conversion-ready pin. Set the most-significant bit of the HIGH_TH register to 1b and the most-significant bit of the LOW_TH register to 0b to configure the pin as a conversion-ready pin. The COMP_POL bit continues to function as expected. Set the COMP_QUE[1:0] bits to any 2-bit value other than 11b to keep the ALERT/RDY pin enabled, and to allow the conversion-ready signal to appear at the ALERT/RDY pin output. The COMP_MODE and COMP_LAT bits have no effect when the ALERT/RDY pin is configured in this way.

As shown in Figure 8-7, the ADS1x1C0x provide an approximate 8µs conversion-ready pulse on the ALERT/RDY pin at the end of each conversion in continuous-conversion mode. In single-shot mode, the ALERT/RDY pin asserts high for the duration of a conversion and assert low at the end of a conversion if the COMP_POL bit is set to 0b.

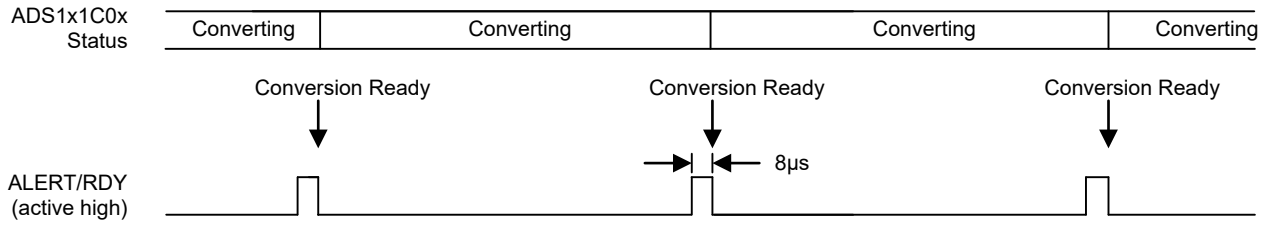


Figure 8-7. Conversion-Ready Pulse in Continuous-Conversion Mode (COMP_POL = 1b)

8.3.9 SMBus Alert Response

In latching comparator mode (COMP_LAT = 1b), the ALERT/RDY pin asserts when the comparator detects a conversion that exceeds the upper or lower threshold value. This assertion is latched and can be cleared only by reading conversion data, or by issuing a successful SMBus alert response and reading the asserting device I^2C address. If conversion data exceed the upper or lower threshold values after being cleared, the ALERT/RDY pin reasserts. This assertion does not affect conversions that are already in progress. The open-drain ALERT/RDY output allows several devices to share the same interface bus. When disabled (COMP_QUE[1:0] = 11b), the ALERT/RDY pin holds a high-impedance state so that the pin does not interfere with other devices on the same bus line.

When the controller senses that the ALERT/RDY pin has latched, the controller issues an SMBus alert command (00011001b) to the I^2C bus. Any ADS1x1C0x device on the I^2C bus with the ALERT/RDY pins asserted responds to the command with the target address. If more than one device on the I^2C bus assert the latched ALERT/RDY pin, arbitration during the address response portion of the SMBus alert determines which device clears assertion. The device with the lowest I^2C address always wins arbitration. If a device loses arbitration, the device does not clear the comparator output pin assertion. The controller then repeats the SMBus alert response until all devices have the respective assertions cleared. In window comparator mode, the SMBus alert status bit on SDA indicates a 1b if signals exceed the high threshold, and a 0b if signals exceed the low threshold. Figure 8-12 details the timing of the SMBus bit relative to the ALERT/RDY signal.

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8.4 Device Functional Modes

8.4.1 Power-Up and Reset

The ADS1x1C0x reset on power-up and set all bits in the Configuration register to the respective default settings. The ADS1x1C0x enter a power-down state after the reset process completes. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the ADS1x1C0x relieves systems with tight power-supply requirements from encountering a surge during power-up.

The ADS1x1C0x respond to the I^2C general-call reset command. When the ADS1x1C0x receive a general-call reset command (06h), an internal reset is performed as if the device is powered up.

8.4.2 Operating Modes

The ADS1x1C0x operate in one of two modes: single-shot conversion or continuous-conversion. The MODE bit selects the respective operating mode. Figure 8-8 shows the operation of the device in both single-shot conversion mode and continuous-converison mode.

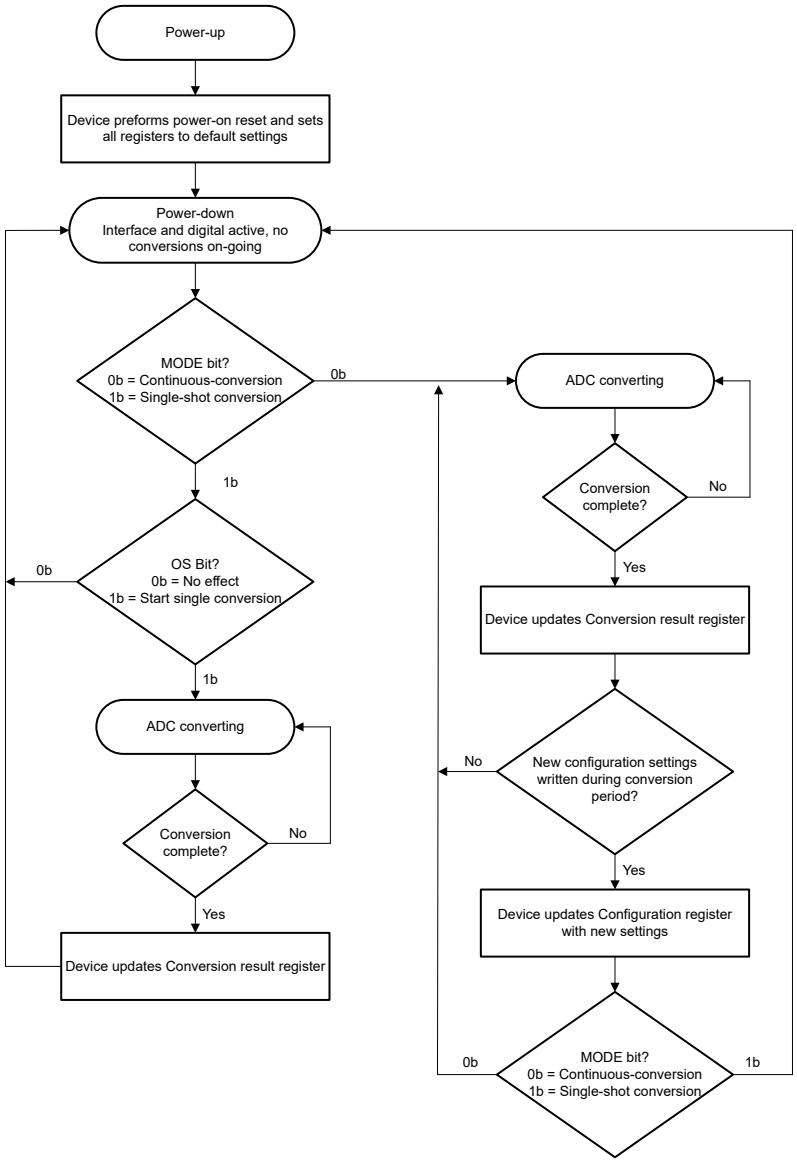


Figure 8-8. Operating Mode State Diagram

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8.4.2.1 Single-Shot Conversion Mode

When the MODE bit is set to 1b, the ADS1x1C0x enter a power-down state, and operate in single-shot conversion mode. This power-down state is the default state for the ADS1x1C0x when power is first applied. The ADS1x1C0x remain in this power-down state until a 1b is written to the operational status (OS) bit. When the OS bit is asserted, the device power up in approximately 25µs, resets the OS bit to 0b, and starts a single conversion. When conversion data are ready for retrieval, the device powers down again. The device still respond to commands, when in power down mode. Writing a 1b to the OS bit while a conversion is ongoing has no effect. To switch to continuous-conversion mode, write a 0b to the MODE bit.

8.4.2.2 Continuous-Conversion Mode

When the MODE bit is set to 0b, the ADS1x1C0x operate in continuous-conversion mode and perform conversions continuously. When a conversion completes, the ADS1x1C0x place the result in the Conversion register and immediately begin another conversion. When writing new configuration settings, the currently ongoing conversion completes with the previous configuration settings. Thereafter, continuous conversions with the new configurations settings start.

To switch to single-shot conversion mode, write a 1b to the MODE bit. The ongoing conversion stops immediately and the device transitions into the power-down state. To start a single-shot conversion write 1b to the OS bit. Resetting the ADS1x1C0x transitions the device to single-shot conversion mode.

8.5 Programming

8.5.1 I²C Interface

The ADS1x1C0x use an I²C-compatible (inter-integrated circuit) interface for serial communication. I²C is a 2-wire communication interface that allows communication of a controller device with multiple target devices on the same bus through the use of device addressing. Each target device on an I²C bus must have a unique address. Communication on the I²C bus always takes place between two devices: one acting as the controller and the other as the target. Both the controller and target can receive and transmit data, but the target can only read or write under the direction of the controller. The ADS1x1C0x always act as an I²C target devices.

An I²C bus consists of two lines: SDA and SCL. SDA carries data and SCL provides the clock. Devices on the I²C bus drive the bus lines low by connecting the lines to ground; the devices never drive the bus lines high. Instead, the bus wires are pulled high by pullup resistors; thus, the bus wires are always high when a device is not driving the lines low. As a result of this configuration, two devices do not conflict. If two devices drive the bus simultaneously, there is no driver contention.

See the *I²C-Bus Specification and User Manual* from NXP Semiconductors™ for more details.

8.5.2 I²C Address Selection

The ADS1x1C0x have one address pin (ADDR) that configures the I²C address of the devices. The ADDR pin can connect to GND, VDD, SDA, or SCL providing four different addresses to be selected with one pin. Table 8-5 shows the I²C address for the possible address pin connections.

The device decodes the I²C target address at the start of each transaction. For address selection, use the GND, VDD, or SCL connections first. If the SDA line is used for address selection, hold SDA low for at least 100ns after SCL goes low to provide proper address decoding during I²C communication.

Table 8-5. ADDR Pin Connection and Corresponding Target Address

ADDR PIN CONNECTION	TARGET ADDRESS
GND	1001000b
VDD	1001001b
SDA	1001010b
SCL	1001011b

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8.5.3 Serial Clock (SCL) and Serial Data (SDA)

The serial clock (SCL) line is used to clock data in and out of the device. The controller always drives the clock line. The ADS1x1C0x cannot act as a controller and, as a result, can never drive SCL.

The serial data (SDA) line allows for bidirectional communication between the controller and the ADS1x1C0x, the target. When the controller reads from the device, the ADS1x1C0x drive the data line. When the controller writes to an ADS1x1C0x device, the controller drives the data line.

Data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the SCL line is low. One clock pulse is generated for each data bit transferred. When in an idle state, the controller must hold SCL high.

After the SDA line settles, the SCL line is brought high and then is brought low. This pulse on SCL clocks the SDA bit into the receiver shift register.

8.5.4 I^2C Interface Speed

The ADS1x1C0x support the following I^2C interface speeds: Standard-mode (Sm) with bit rates up to 100kbit/s, fast-mode (Fm) with bit rates up to 400kbit/s, and Fast-mode plus (Fm+) with bit rates up to 1000kbit/s. High-speed mode (Hs-mode) is not supported.

8.5.5 I^2C Data Transfer Protocol

Figure 8-9 shows the format of the data transfer. The controller initiates all transactions with the ADS1x1C0x by generating a START (S) condition. A high-to-low transition on the SDA line while SCL is high defines a START condition. The bus is considered to be busy after the START condition.

Following the START condition, the controller sends the 7-bit target address corresponding to the address of the ADS1x1C0x that the controller wants to communicate with. The controller then sends an eighth bit that is a data-direction bit (R/$\overline{W}$). An R/$\overline{W}$ bit of 0b indicates a write operation, and an R/$\overline{W}$ bit of 1b indicates a read operation. After the R/$\overline{W}$ bit, the controller generates a ninth SCLK pulse and releases the SDA line to allow the ADS1x1C0x to acknowledge (ACK) the reception of the target address by pulling SDA low. If the device does not recognize the target address, the ADS1x1C0x holds SDA high to indicate a not acknowledge (NACK) signal.

Next follows the data transmission. If the transaction is a read (R/$\overline{W}$ = 1b), the ADS1x1C0x output data on SDA. If the transaction is a write (R/$\overline{W}$ = 0b), the controller outputs data on SDA. Data are transferred byte-wise, most significant bit (MSB) first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be acknowledged (via the ACK bit) by the receiver. If the transaction is a read, the controller issues the ACK bit. If the transaction is a write, the device issues the ACK bit.

The controller terminates all transactions by generating a STOP (P) condition. A low-to-high transition on the SDA line while SCL is high defines a STOP condition. The bus is considered free after t_{BUF} (bus-free time) following the STOP condition.

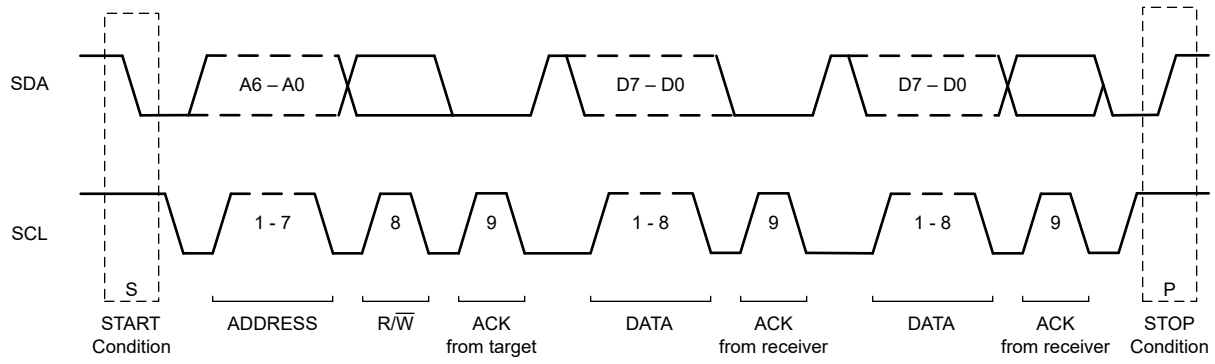


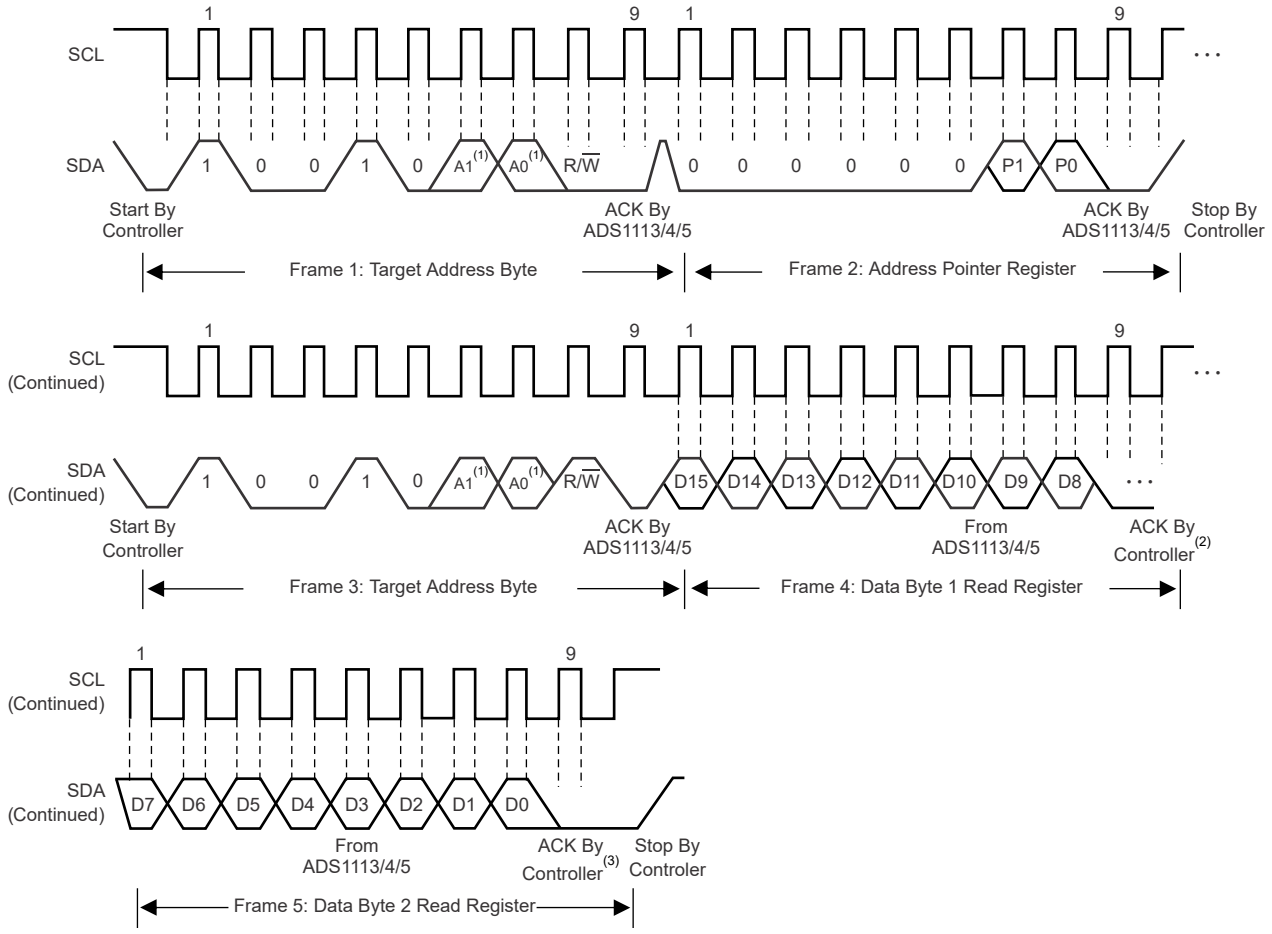
Figure 8-9. I^2C Data Transfer Format

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8.5.6 Writing To and Reading From the Registers

To access a specific register from the ADS1x1C0x, the controller must first write an appropriate value to the register address pointer bits P[2:0]. The Address Pointer register is written to directly after the target address byte, low R/$\overline{W}$ bit, and a successful target acknowledgment. After the Address Pointer register is written, the target acknowledges, and the controller issues a STOP or a repeated START condition.

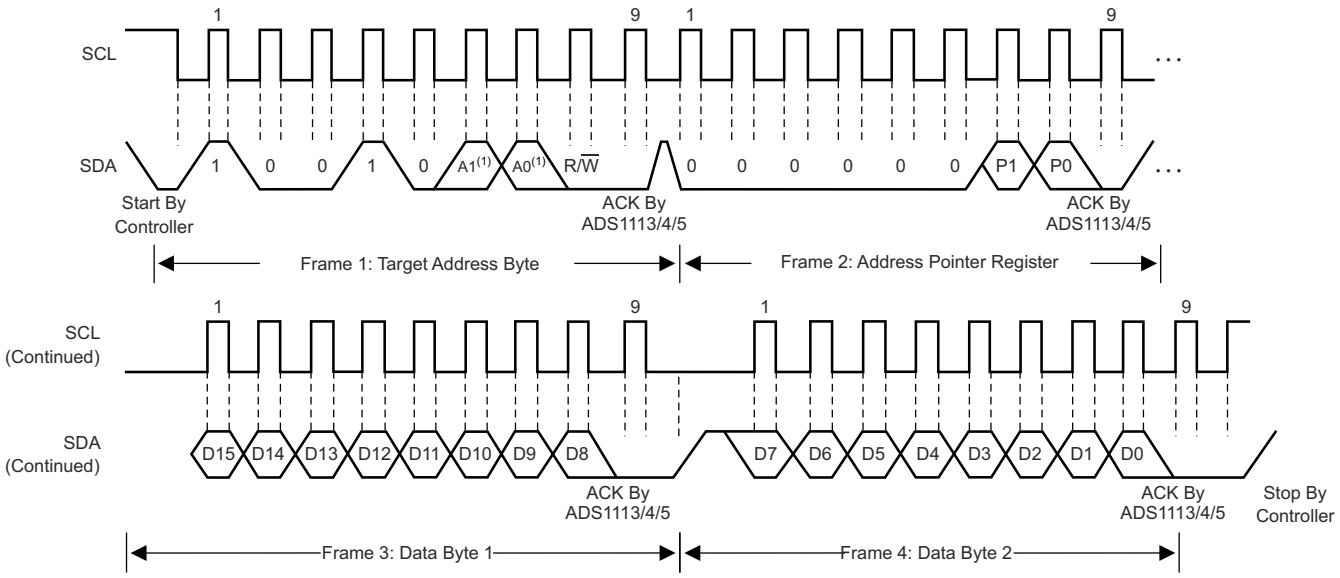
When reading from the ADS1x1C0x, the previous value written to the P[2:0] bits determines the register that is read. To change which register is read, a new value must be written to P[2:0]. To write a new value to P[2:0], the controller issues a target address byte with the R/$\overline{W}$ bit low, followed by the Address Pointer register byte. No additional data has to be transmitted, and a STOP condition can be issued by the controller. The controller can now issue a START condition and send the target address byte with the R/$\overline{W}$ bit high to begin the read. Figure 8-10 details this sequence. If repeated reads from the same register are desired, there is no need to continually send the Address Pointer register, because the ADS1x1C0x stores the value of P[2:0] until modified by a write operation. Figure 8-11 details the write sequence. However, for every write operation, the Address Pointer register must be written with the appropriate values. Figure 8-12 details the SMBus alert response sequence.



A. The values of A0 and A1 are determined by the ADDR pin.
B. The controller can leave SDA high to terminate a single-byte read operation.
C. The controller can leave SDA high to terminate a two-byte read operation.

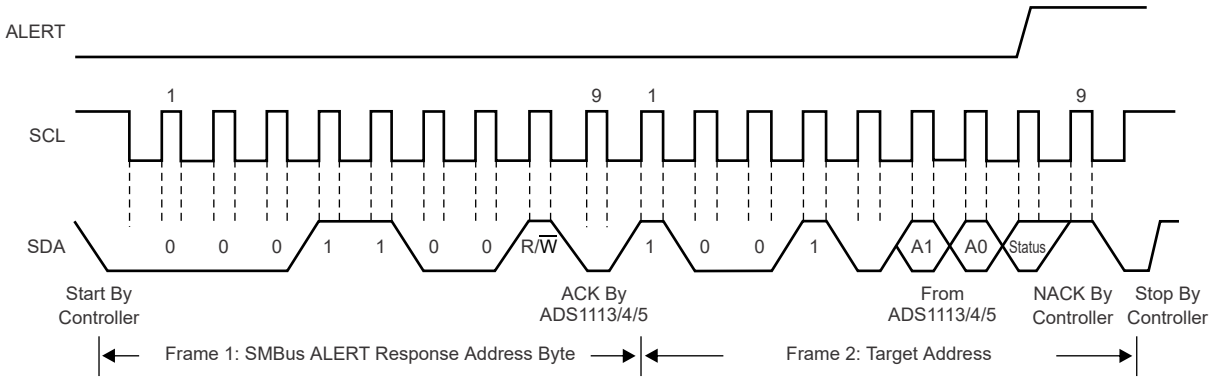
Figure 8-10. Timing Diagram for Reading From the ADS1x1C0x

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A. The values of A0 and A1 are determined by the ADDR pin.

Figure 8-11. Timing Diagram for Writing to the ADS1x1C0x



A. The values of A0 and A1 are determined by the ADDR pin.

Figure 8-12. Timing Diagram for SMBus Alert Response

8.5.7 Timeout

The ADS1x1C0x offer an I^{2}C timeout feature that can be used to recover communication when a serial interface transmission is interrupted. If the controller initiates contact with the ADS1x1C0x but subsequently remains idle for 25ms before completing a command, the ADS1x1C0x interface is reset. If the ADS1x1C0x interface resets because of a timeout condition, the controller must abort the transaction and restart the communication again by issuing a new START condition.

8.5.8 I^{2}C General-Call (Software Reset)

The ADS1x1C0x respond to the I^{2}C general-call address (0000000b) if the R/$\overline{W}$ bit is 0b. The devices acknowledge the general-call address and, if the next byte is 06h, the ADS1x1C0x reset the internal registers and enter a power-down state.

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8.6 Conversion Data Format

Conversion data are coded depending on the MUX[2:0] configuration. Configurations that use AIN_N = GND use unipolar straight binary data format, all other configurations use binary two's complement data format, MSB first (sign bit). Table 8-6 shows the conversion data format based on the MUX[2:0] settings.

Table 8-6. Conversion Data Format

MUX[2:0]	AIN_P	AIN_N	CONVERSION DATA FORMAT
000b	AIN0	AIN1	Binary Two's Compliment
001b	AIN0	AIN3	Binary Two's Compliment
010b	AIN1	AIN3	Binary Two's Compliment
011b	AIN2	AIN3	Binary Two's Compliment
100b	AIN0	GND	Unipolar Straight Binary
101b	AIN1	GND	Unipolar Straight Binary
110b	AIN2	GND	Unipolar Straight Binary
111b	AIN3	GND	Unipolar Straight Binary

Table 8-7 and Table 8-8 show the output coding for the 12- and 16-bit devices, respectively. In binary two's-complement format, the conversion data clips to positive and negative full-scale code values when the input signal exceeds the respective positive and negative full-scale values. In unipolar straight binary format, conversion data clips to full-scale or zero code values when the input signal exceeds full-scale or is below zero, respectively.

Table 8-7. Ideal Output Code Versus Input Signal (12-Bit Device)

DIFFERENTIAL INPUT VOLTAGE (V)	IDEAL OUTPUT CODE(1)	
	BINARY TWO'S-COMPLEMENT FORMAT	UNIPOLAR STRAIGHT BINARY FORMAT
≥ FSR × (2^{12} – 1) / 2^{12}	7FFh	FFFh
≥ FSR × (2^{11} – 1) / 2^{11}		FFEh
FSR / 2^{11}	001h	002h
0	000h	000h
–FSR / 2^{11}	FFFh	
–FSR × (2^{11} – 1) / 2^{11}	801h	
≤ –FSR	800h	

(1) Ideal output data, excluding offset, gain, linearity, and noise errors.

Table 8-8. Ideal Output Code Versus Input Signal (16-Bit Device)

DIFFERENTIAL INPUT VOLTAGE (V)	IDEAL OUTPUT CODE(1)	
	BINARY TWO'S-COMPLEMENT FORMAT	UNIPOLAR STRAIGHT BINARY FORMAT
≥ FSR × (2^{16} – 1) / 2^{16}	7FFFh	FFFFh
≥ FSR × (2^{15} – 1) / 2^{15}		FFFEh
FSR / 2^{15}	0001h	0002h
0	0000h	0000h
–FSR / 2^{15}	FFFFh	
–FSR × (2^{15} – 1) / 2^{15}	8001h	
≤ –FSR	8000h	

(1) Ideal output data, excluding offset, gain, linearity, and noise errors.

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9 Register Maps

The ADS1x1C0x have five registers that are accessible through the I²C interface using the Address Pointer register.

Table 9-1. ADS1x1C0x Registers Descriptions

Register Name	Register Address	Description
Conversion Register	00h	Contains the result of the last conversion
Configuration register	01h	Used to change the device operating modes and query the device status
LOW_TH Register	02h	Set the low threshold value used for the comparator function
HIGH_TH Register	03h	Set the high threshold value used for the comparator function
ID Register	04h	Distinguishes between 12- and 16-bit resolution devices.

Table 9-2 lists the register access codes.

Table 9-2. Register Access Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
-n		Value after reset or the default value

9.1 Address Pointer Register (address = N/A) [reset = N/A]

All five registers are accessed by writing to the Address Pointer register.

Figure 9-1. Address Pointer Register

7	6	5	4	3	2	1	0
RESERVED					P[2:0]		
W-00000b					W-000b		

Table 9-3. Address Pointer Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	W	00000b	Always write 00000b
2:0	P[2:0]	W	000b	**Register address pointer** 000b : Conversion register 001b : Configuration register 010b : LOW_TH register 011b : HIGH_TH register 100b : ID register

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9.2 Conversion Register (P[2:0] = 000b) [reset = 0000h]

The 16-bit Conversion register contains the result of the last conversion in binary two's-complement format for differential-measurement configurations or unipolar straight binary in single-ended measurement configurations. Following power-up, the Conversion register is cleared to 0000h, and remains 0000h until the first conversion completes. The register format is shown in Table 9-6

Table 9-4. 12-bit Device Conversion Register

15	14	13	12	11	10	9	8
D[11:4]							
R-00h							
7	6	5	4	3	2	1	0
D[3:0]				RESERVED1			
R-0h				R-0h			

1. ADS101C0x D[3:0] will always read back 0h

Table 9-5. 12-bit Device Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	D[11:0]	R	000h	12-bit conversion result
3:0	RESERVED	R	0h	Always reads back 0h

Table 9-6. 16-bit Device Conversion Register

15	14	13	12	11	10	9	8
D[15:8]							
R-00h							
7	6	5	4	3	2	1	0
D[7:0]1							
R-00h							

Table 9-7. 16-bit Device Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	D[15:0]	R	0000h	16-bit conversion result

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9.3 Configuration Register (P[2:0] = 001b) [reset = 8503h]

The 16-bit Configuration register controls the operating mode, input selection, data rate, gain, internal temperature sensor, and comparator modes. The register format is shown in Figure 9-2 and Figure 9-3.

Figure 9-2. Configuration Register: ADS1x1C01

15	14	13	12	11	10	9	8
OS	RESERVED			PGA[2:0]			MODE
R/W-1b	R/W-000b			R/W-010b			R/W-1b
7	6	5	4	3	2	1	0
DR[1:0]		TS_EN	COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE[1:0]	
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-11b	

Figure 9-3. Configuration Register: ADS1x1C02

15	14	13	12	11	10	9	8
OS	MUX[2:0]			PGA[2:0]			MODE
R/W-1b	R/W-000b			R/W-010b			R/W-1b
7	6	5	4	3	2	1	0
DR[1:0]		TS_EN	COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE[1:0]	
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-11b	

Table 9-8. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OS	R/W	1b	**Operational status or single-shot conversion start** This bit determines the operational status of the device. OS can only be written when in power-down state and has no effect when a conversion is ongoing. When writing: 0b : No effect 1b : Start a single conversion (when in power-down state) When reading: 0b : Device is currently performing a conversion 1b : Device is not currently performing a conversion
14:12	MUX[2:0]	R/W	000b	**Input multiplexer configuration (ADS1x1C02 only)** These bits configure the input multiplexer. Configurations that use AIN_N = GND use unipolar data format, all other configurations use two's complement data format, MSB first (sign bit). *These bits serve no function on the ADS1x1C01. The ADS1x1C01 always uses inputs AIN_P = AIN0 and AIN_N = AIN1.* 000b : AIN_P = AIN0 and AIN_N = AIN1 001b : AIN_P = AIN0 and AIN_N = AIN3 010b : AIN_P = AIN1 and AIN_N = AIN3 011b : AIN_P = AIN2 and AIN_N = AIN3 100b : AIN_P = AIN0 and AIN_N = GND 101b : AIN_P = AIN1 and AIN_N = GND 110b : AIN_P = AIN2 and AIN_N = GND 111b : AIN_P = AIN3 and AIN_N = GND
11:9	PGA[2:0]	R/W	010b	**Programmable gain amplifier configuration** These bits set the gain of the programmable gain amplifier. 000b : Gain = 1/6(1) 001b : Gain = 1/4(1) 010b : Gain = 1/2 011b : Gain = 1 100b : Gain = 2 101b : Gain = 4 110b : Gain = 8 111b : Gain = 16
8	MODE	R/W	1b	**Device operating mode** This bit controls the operating mode. 0b : Continuous-conversion mode 1b : Single-shot mode or power-down state

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Table 9-8. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	DR[1:0]	R/W	00b	**Data rate** These bits control the data rate setting. **ADS101C0x** 00b : 100SPS 01b : 500SPS 10b : 2kSPS 11b : 6kSPS **ADS111C0x** 00b : 10SPS 01b : 100SPS 10b : 1kSPS 11b : 4kSPS
5	TS_EN	R/W	0b	**Temperature sensor enable** This bit enables the internal temperature sensor for measurement. 0b : Disabled, ADC measures external input configured by MUX[2:0] 1b : Enabled, ADC measures internal temperature sensor
4	COMP_MODE	R/W	0b	**Comparator mode** This bit configures the comparator operating mode. 0b : Traditional comparator 1b : Window comparator
3	COMP_POL	R/W	0b	**Comparator polarity** This bit controls the polarity of the ALERT/RDY pin. 0b : Active low 1b : Active high
2	COMP_LAT	R/W	0b	**Latching comparator** This bit controls whether the ALERT/RDY pin latches after being asserted or clears after conversions are within the margin of the upper and lower threshold values. 0b : Nonlatching comparator. The ALERT/RDY pin does not latch when asserted. 1b : Latching comparator. The asserted ALERT/RDY pin remains latched until conversion data are read by the controller or an appropriate SMBus alert response is sent by the controller. The device with the ALERT/RDY pin asserted responds with the target address. The device with the lowest I^2C address always wins arbitration.
1:0	COMP_QUE[1:0]	R/W	11b	**Comparator queue and disable** These bits perform two functions. When set to 11b, the comparator is disabled and the ALERT/RDY pin is set to a high-impedance state. When set to any other value, the ALERT/RDY pin and the comparator function are enabled, and the set value determines the number of successive conversions exceeding the upper or lower threshold required before asserting the ALERT/RDY pin. 00b : Assert after one conversion 01b : Assert after two conversions 10b : Assert after four conversions 11b : Disable the comparator and set the ALERT/RDY pin to high impedance

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3V to the analog inputs of the device.

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9.4 LOW_TH Register (P[2:0] = 010b) [reset = 8000h]

The upper and lower threshold values used by the comparator are stored in two 16-bit registers and formatted to match the ADC conversion data format, either binary two's compliment or unipolar straight binary. The comparator is implemented as a digital comparator; therefore, the values in these registers must be updated whenever the PGA settings are changed. To use the comparator function of the ALERT/RDY pin, the HIGH_TH register value must always be greater than the LOW_TH register value. The LOW_TH threshold register formats are shown in the tables below for both 12- and 16-bit devices.

The conversion-ready function of the ALERT/RDY pin is enabled by setting the HIGH_TH register MSB to 1b and the LOW_TH register MSB to 0b. When set to the conversion-ready function, the ALERT/RDY pin outputs the state of the OS bit when in single-shot conversion mode, and provides a continuous-conversion ready pulse when in continuous-conversion mode.

Figure 9-4. 12-bit Device LOW_TH Register

15	14	13	12	11	10	9	8
LOW_TH[11:4]							
R/W-80h							
7	6	5	4	3	2	1	0
LOW_TH[3:0]				RESERVED			
R/W-0h				R-0h			

Table 9-9. 12-bit Device LOW_TH Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	LOW_TH[11:0]	R/W	800h	Low threshold value
3:0	RESERVED	R	0h	Always reads back 0h

Figure 9-5. 16-bit Device LOW_TH Register

15	14	13	12	11	10	9	8
LOW_TH[15:8]							
R/W-80h							
7	6	5	4	3	2	1	0
LOW_TH[7:0]							
R/W-00h							

Table 9-10. 16-bit Device LOW_TH Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	LOW_TH[15:0]	R/W	8000h	Low threshold value

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9.5 HIGH_TH Register (P[2:0] = 011b) [reset = 7FFFh]

The upper and lower threshold values used by the comparator are stored in two 16-bit registers and formatted to match the ADC conversion data format, either binary two's compliment or unipolar straight binary. The comparator is implemented as a digital comparator; therefore, the values in these registers must be updated whenever the PGA settings are changed. To use the comparator function of the ALERT/RDY pin, the HIGH_TH register value must always be greater than the LOW_TH register value. The HIGH_TH threshold register formats are shown in the tables below for both 12- and 16-bit devices.

Figure 9-6. 12-bit Device HIGH_TH Register

15	14	13	12	11	10	9	8
HIGH_TH[11:4]							
R/W-7Fh							
7	6	5	4	3	2	1	0
HIGH_TH[3:0]				RESERVED			
R/W-Fh				R-Fh			

Table 9-11. 12-bit Device HIGH_TH Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	HIGH_TH[11:0]	R/W	7FFh	High threshold value
3:0	RESERVED	R	0h	Always reads back 0h

Figure 9-7. 16-bit Device HIGH_TH Register

15	14	13	12	11	10	9	8
HIGH_TH[15:8]							
R/W-7Fh							
7	6	5	4	3	2	1	0
HIGH_TH[7:0]							
R/W-FFh							

Table 9-12. 16-bit Device HIGH_TH Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	HIGH_TH[15:0]	R/W	7FFFh	High threshold value

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9.6 ID Register (P[2:0] = 100b) [reset = 8000h])

The ID Register distinguishes between 12- and 16-bit resolution devices.

Figure 9-8. ID Register

15	14	13	12	11	10	9	8
RESOLUTION[15:14]		RESERVED[13:8]					
R-xxb		R-000000b					
7	6	5	4	3	2	1	0
RESERVED[7:0]							
R-00000000b							

Table 9-13. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESOLUTION	R	xxb	Resolution identifier 01 : 12-bit device 10 : 16-bit device
13:0	RESERVED	R	00000000000000b	Always reads back 00000000000000b

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The ADS1x1C0x are precision, 12- and 16-bit ΔΣ ADCs that offer many integrated features to ease the measurement of the most common sensor types including various types of temperature and bridge sensors. The following sections give example circuits and suggestions for using the ADS1x1C0x in various situations.

10.1.1 Serial Interface Connections

Figure 10-1 shows the principle serial interface connections for the ADS1x1C02.

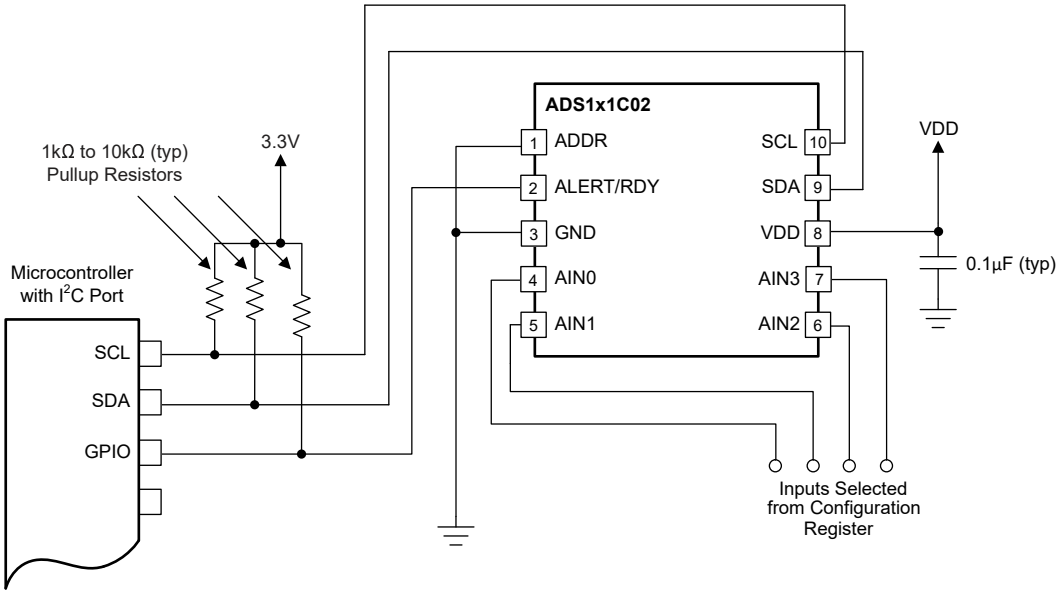


Figure 10-1. Serial Interface Connections

The ADS1x1C0x interface directly to I^2C controllers with standard-mode, fast-mode, and fast-mode plus bus speeds. The devices can be used on an I^3C bus because the devices do not perform clock-stretching.

Pullup resistors are required on both the SDA and SCL lines. The size of these resistors depends on the bus speed and capacitance of the bus lines. Higher-value resistors yield lower power consumption when the bus lines are pulled low, but increase the transition times on the bus, which limits the bus speed. Lower-value resistors allow higher interface speeds, but at the expense of higher power consumption when the bus lines are pulled low. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. See the *I^2C-Bus Specification and Users Manual* for details on pullup resistor sizing.

Add a pullup resistor on the ALERT/RDY line.

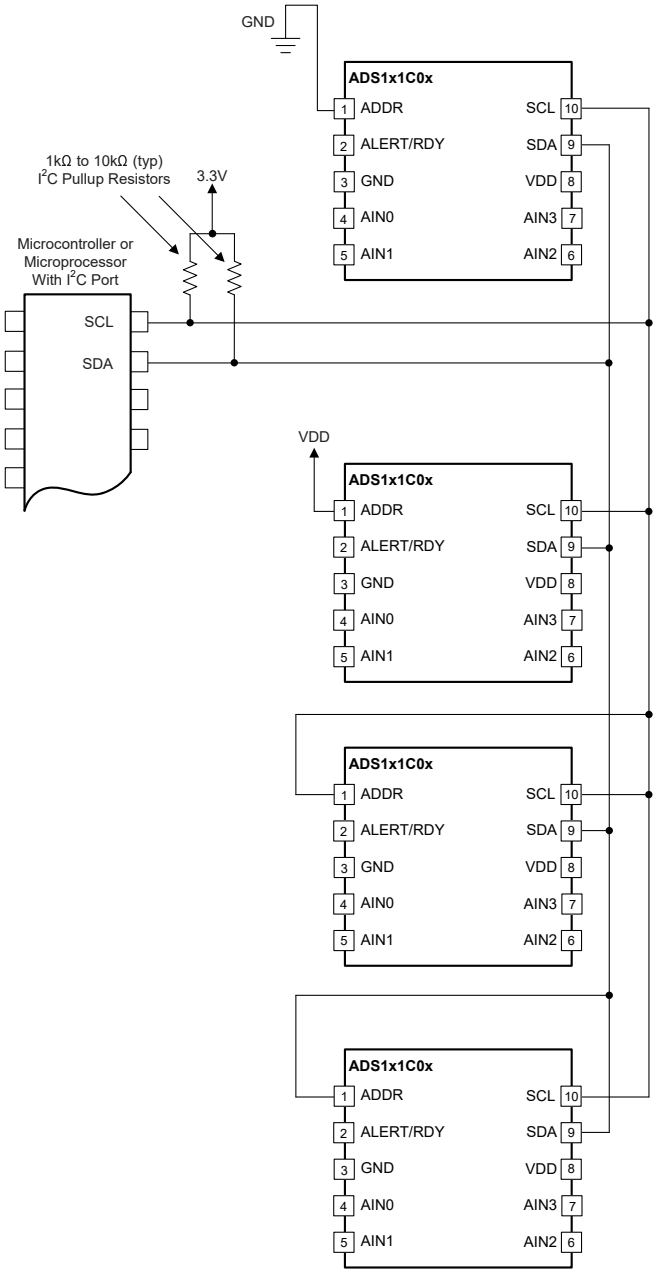
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10.1.2 Connecting Multiple Devices

Up to four ADS1x1C0x devices can be operated on a single I²C bus using different address pin configurations for each device. Use the address pin, ADDR, to set the ADS1x1C0x to one of four different I²C addresses. Use the GND, VDD, and SCL addresses first. If SDA is used as the device address, hold the SDA line low for at least 100ns after the SCL line goes low to make sure the device decodes the address correctly during I²C communication.

Figure 10-2 shows an example of four ADS1x1C0x devices on the same I²C bus. One set of pullup resistors is required per bus line. If needed, decrease the pullup resistor values to compensate for the additional bus capacitance presented by multiple devices and increased line length.



NOTE: The ADS1x1C0x power and input connections are omitted for clarity.

Figure 10-2. Connecting Multiple ADS1x1C0x Devices

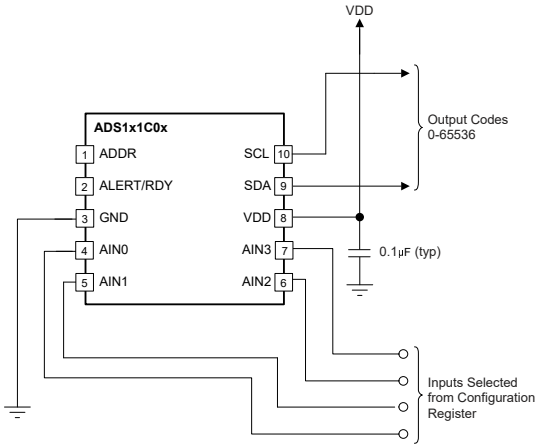
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10.1.3 Single-Ended Inputs

The ADS1x1C01 can measure one, and the ADS1x1C02 up to four, single-ended signals. The ADS1x1C01 can measure single-ended signals by connecting AIN1 to GND externally. The ADS1x1C02 measures single-ended signals by appropriate configuration of the MUX[2:0] bits.

Figure 10-3 shows a single-ended connection scheme for the ADS1x1C02. The single-ended signal ranges from 0V up to positive supply or +FS, whichever is lower. Negative voltages cannot be applied to these devices because the ADS1x1C0x can only accept positive voltages with respect to ground. The ADS1x1C0x do not lose linearity within the input range.

Single-ended configurations using the ADS1x1C02, output data in unipolar straight binary format. See the *Conversion Data Format* section for data coding information. Differential configurations provide better common-mode noise rejection than single-ended configurations.



Digital pin connections omitted for clarity.

Figure 10-3. Measuring Single-Ended Inputs

The ADS1x1C02 also allows AIN3 to serve as a common point for measurements by appropriate setting of the MUX[2:0] bits. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration, the ADS1x1C02 operates with inputs, where AIN3 serves as the common point. This ability improves the usable range over the single-ended configuration because negative differential voltages are allowed when GND < V_{AIN3} < VDD. However, common-mode noise attenuation is not offered.

10.1.4 Unused Inputs and Outputs

Follow the guidelines below for the connection of unused device pins:

- Either float unused analog inputs, or tie unused analog inputs to GND.
- Either float NC (not connected) pins, or tie the NC pins to GND.
- If the ALERT/RDY output pin is not used, leave this pin unconnected or tie this pin to VDD using a weak pullup resistor.

10.1.5 Input Protection

The ADS1x1C0x are fabricated in a small-geometry, low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADS1x1C0x can be permanently damaged by analog input voltages that exceed approximately 300mV beyond the rails for extended periods. Place current-limiting resistors in series with the analog inputs to protect against overvoltage events.

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10.1.6 Analog Input Filtering

Analog input filtering serves two purposes: limit the effect of aliasing during the sampling process and reduce external noise from being a part of the measurement.

Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC, also known as the *Nyquist frequency*. These frequency components fold back and show up in the actual frequency band of interest below half the sampling frequency. The filter response of the digital filter, as shown in Figure 10-4, repeats at multiples of the sampling frequency, also known as the modulator frequency (f_{MOD}). Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency, or multiples thereof, are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

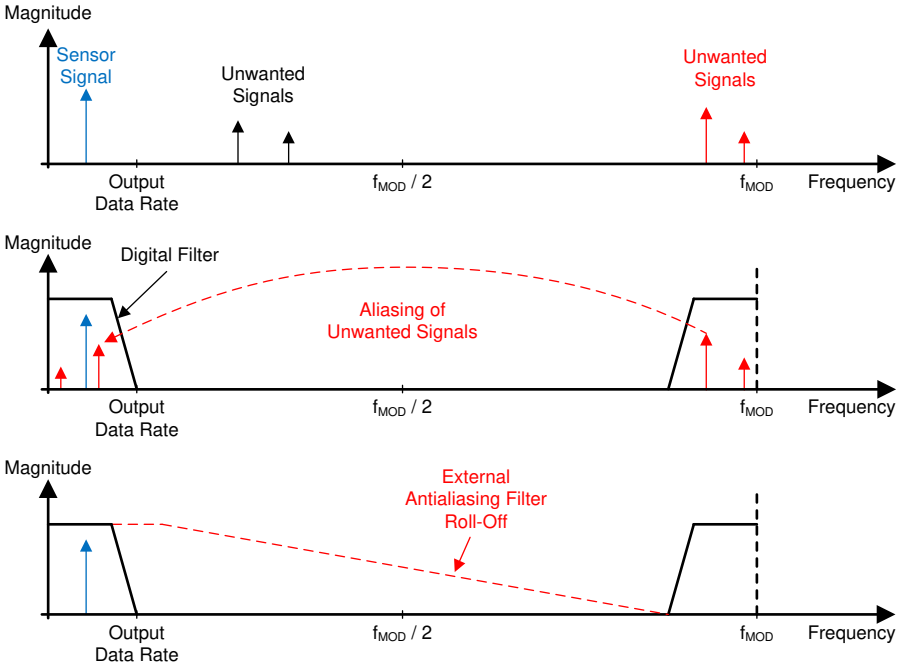


Figure 10-4. Effect of Aliasing

Many sensor signals are inherently band-limited (for example, the output of a thermocouple has a limited rate of change). In this case, the sensor signal does not alias back into the pass band when using a ΔΣ ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed circuit board (PCB) in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order resistor-capacitor (RC) filter is, in most cases, sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Generally, any signal beyond f_{MOD} / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS1x1C0x attenuate signals to a certain degree. In addition, noise components are typically smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or 10 times higher is generally a good starting point for a system design.

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10.1.7 Duty Cycling For Low Power

The noise performance of a ΔΣ ADC generally improves when lowering the output data rate because more samples of the internal modulator are averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates is not always required. For these applications, the ADS1x1C0x support duty cycling that yields significant power savings by periodically requesting high data rate readings at an effectively lower data rate.

The ADS111C0x operating in power-down mode can achieve an effective 10SPS data rate by executing single-shot conversions every 100ms under microcontroller control, with a 4kSPS data rate configured. A conversion at 4kSPS only requires approximately 0.25ms, so the device enters power-down state for the remaining 99.75ms. In this configuration, the device consumes approximately 1/400th the power consumed in continuous-conversion mode.

The duty cycling rate is completely arbitrary and is defined by the controller. The ADS1x1C0x offer lower data rates that do not implement duty cycling and improved noise performance if required.

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10.1.8 I²C Communication Sequence Example

This section provides an example of an I²C communication sequence between a microcontroller and a ADS1x1C02 configured with a target address of 1001000b (ADDR pin connected to GND) to start a single-shot conversion and subsequently read the conversion result.

Figure 10-5 lists a legend for Figure 10-6 to Figure 10-8.

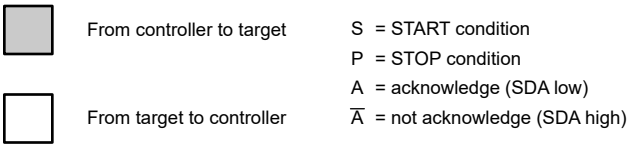


Figure 10-5. Legend for the I²C Sequence Diagrams

1. Write the Configuration register as shown in Figure 10-7 to configure the device. For example, when using the ADS1x1C02, write MUX[2:0] = 000b, PGA[2:0] = 010b, MODE = 1b, and DR[2:0] = 110b, and)S = 1b to start a single-shot conversion.

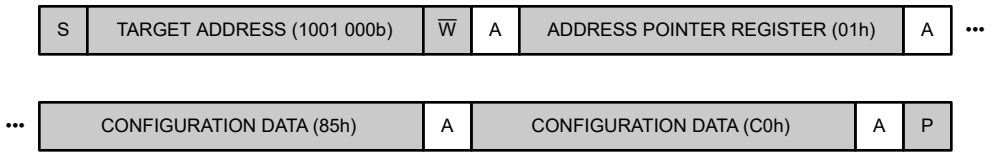


Figure 10-6. Write the Configuration Register

2. Wait at least t = 1 / DR ± 5% for the conversion to complete.

   Alternatively, poll the OS bit for a 1b as shown in Figure 10-7 to determine when the conversion result is ready for retrieval. This option does not work in continuous-conversion mode because the OS bit always reads 0b.



Figure 10-7. Read the Configuration Register to Check for OS = 1b

3. Then, as shown in Figure 10-8, read the Conversion register.





Figure 10-8. Read the Conversion Register

4. Start a new single-shot conversion by writing a 1b to the OS bit in the Configuration register.

   To save time, a new conversion can also be started (step 4) before reading the conversion result (step 3).

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10.2 Typical Applications

10.2.1 K-Type Thermocouple with Thermistor Cold-Junction Compensation

The application example in Figure 10-9 shows how to use the ADS1x1C02 to monitor a K-Type thermocouple using a linear PTC thermistor for cold-junction compensation.

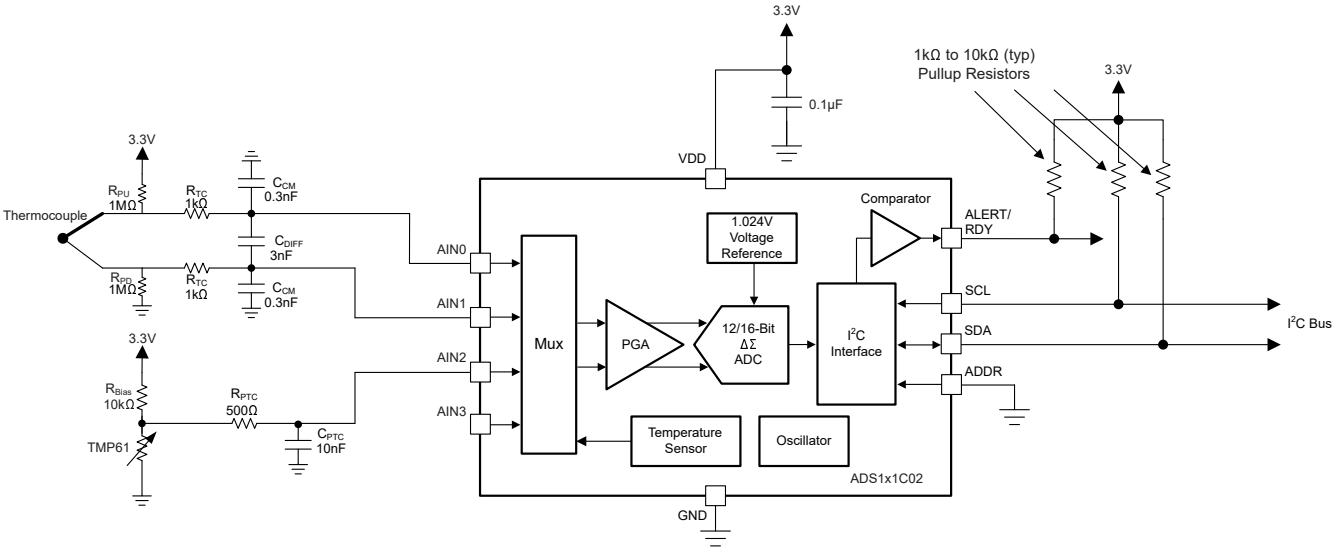


Figure 10-9. K-Type Thermocouple Measurement Using a Thermistor for Cold-Junction Compensation

10.2.1.1 Design Requirements

Table 10-1 lists the design requirements for this application.

Table 10-1. Design Requirements

DESIGN PARAMETER	VALUE
Supply Voltage	3.3V
Thermocouple Type	K
Thermocouple Temperature Measurement Range	–200°C to +1250°C
Thermistor Type	PTC
Thermistor Temperature Measurement Range	–40°C to +125°C
Measurement accuracy at T_A = 25°C(1)	±0.75

(1) Not accounting for error of the thermocouple and cold-junction temperature measurement; offset calibration at $T_{TC} = T_{CJ}$ = 25°C; no gain calibration.

10.2.1.2 Detailed Design Procedure

In this thermocouple measurement example, biasing resistors R_{PU} and R_{PD} set the common-mode voltage of the thermocouple to approximately mid-supply (VDD / 2) to keep the input voltages within the absolute input voltage range of the PGA. These biasing resistors are also useful in detecting an open thermocouple. An open thermocouple lead condition causes R_{PU} and R_{PD} to pull analog inputs AIN0 and AIN1 to VDD and GND respectively. Consequently, the ADC reads a full-scale value outside the normal measurement range, indicating a fault condition. Recommended values for R_{PU} and R_{PD} range from 1MΩ to 50MΩ to minimize self-heating and measurement errors.

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Although the device digital filter attenuates high-frequency noise, further improvement can be achieved by including a first-order passive RC filter at the input. The cutoff frequency of the differential filter (f_C) created by resistors R_{TC} and capacitor C_{DIFF} is calculated using Equation 6.

$$f_C = 1 / [2\pi \times (R_{TC} + R_{TC}) \times C_{DIFF}] \quad (6)$$

Additionally, common-mode capacitors (C_{CM}) provide attenuation of high-frequency common-mode noise. Select values for common-mode capacitors at least 10 times smaller than the differential capacitor to prevent common-mode noise conversion to differential noise.

The filter resistors R_{TC} also serve as current-limiting resistors. These resistors limit the current into analog inputs, AIN0 and AIN1, of the device to safe levels if an overvoltage on the inputs occurs. Care must be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs.

The highest resolution is obtained when the largest expected thermocouple voltage is slightly below the full-scale range of the ADC. For example, the maximum thermocouple voltage of a K-type thermocouple at T_{TC} = 1250°C with a cold-junction temperature T_{CJ} = 0°C is approximately 50.644mV, as defined in the tables published by the National Institute of Standards and Technology (NIST). If the cold junction drops below 0°C (minimum specified at –40°C), the output voltage increases. At T_{CJ} = –40°C, the output voltage becomes:

$$V_{TC} = 50.644\text{mV} - (-1.527\text{mV}) = 52.171\text{mV} \quad (7)$$

The maximum gain that can be applied with the 1.024V reference is then calculated as (1.024V / 52.171mV) = 19.6. The next smaller PGA gain setting the device offers is 16.

The device incorporates an internal high-precision temperature sensor to measure the cold junction temperature. Enable the internal temperature sensor by setting bit TS_EN = 1b. Optimal accuracy requires careful board layout to provide efficient thermal coupling between the cold junction and the device package.

The device does not perform automatic cold junction compensation (CJC). Perform CJC within the host controller using the following procedure:

1. Measure the thermocouple voltage, V_{TC}, between AIN0 and AIN1.
2. Measure the cold junction temperature, T_{CJ}, using the internal temperature sensor.
3. Convert T_{CJ} to an equivalent thermocouple voltage (V_{CJ}) using the NIST conversion tables.
4. Compute the total compensated voltage ($V_T = V_{TC} + V_{CJ}$)
5. Convert the compensated voltage (V_T) back to temperature using the NIST tables.

If the internal temperature sensor accuracy is insufficient or the device cannot be placed close enough to the cold junction for good thermal measurement. Use the additional ADC input channels to measure the cold-junction temperature externally using a thermistor or dedicated temperature sensor.

Figure 10-9 shows device uses AIN2 to measure a single-ended thermistor for cold junction compensation. The Texas Instruments TMP61 linear thermistor is selected for the linearity and consistent sensitivity of the device, enabling simple and accurate temperature-to-voltage conversion. A 10kΩ bias resistor is used with the TMP61 to form a voltage divider matched to the TMP61 nominal resistance (10kΩ at 25°C). In this application the thermistor is used for a more precise cold junction temperature measurement compared to the internal temperature sensor of the ADS1x1C0x.

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10.2.2 Server Card System Monitoring Application

Figure 10-10 shows an example for a server card monitoring system using the ADS1x1C02L. This example shows four single-ended measurements to monitor:

- the power supply,
- a current shunt using an external current shunt amplifier (INA185),
- temperature using an analog output temperature sensor (LMT70A),
- for liquid leaks with a resistive-based leak sensor.

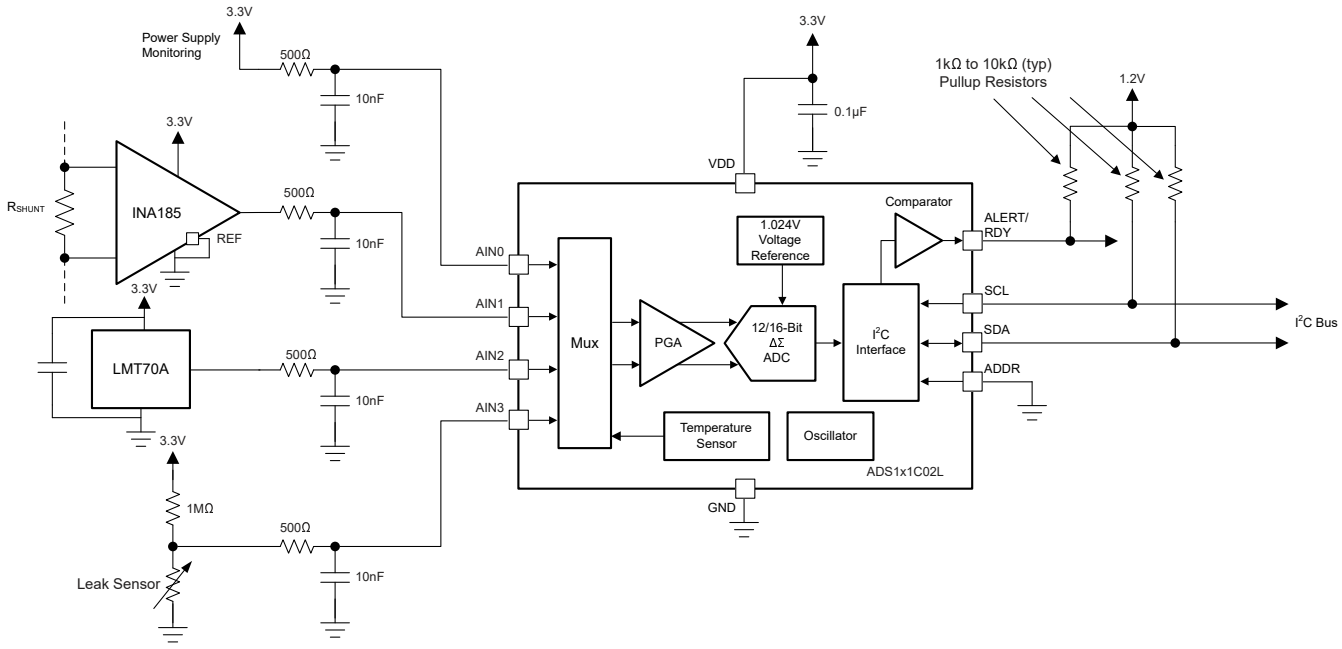


Figure 10-10. Server Card System Monitoring Application

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10.3 Power Supply Recommendations

The device requires a single unipolar supply, VDD, to power both the analog and digital circuitry of the device.

10.3.1 Power-Supply Sequencing

Wait approximately 150µs after VDD is stabilized before communicating with the device to allow the power-up reset process to complete.

10.3.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. As shown in Figure 10-11, VDD must be decoupled with at least a 0.1µF capacitor. The 0.1µF bypass capacitor supplies the momentary bursts of extra current required from the supply when the device is converting. Place the bypass capacitor as close to the power-supply pin of the device as possible using low-impedance connections. Use multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, do not use vias to connect capacitors to the device pins for better noise immunity. Using multiple vias in parallel lowers the overall inductance, and is beneficial for connections to ground planes.

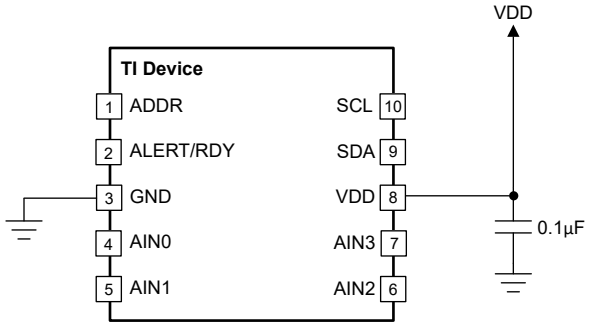


Figure 10-11. ADS1x1C02 Power-Supply Decoupling

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10.4 Layout

10.4.1 Layout Guidelines

The following basic recommendations for the ADS1x1C0x layout help achieve the best possible performance of the ADC.

- For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer.
- Use a ceramic capacitor (for example, X7R grade) for the power-supply decoupling capacitor. High-K capacitors (Y5V) are not recommended. Place the required capacitor as close as possible to the device pin using short, direct traces. Placing the bypass capacitor on the same layer as close to the device yields the best results.
- Use C0G or NP0 capacitors for the RC filters on the analog inputs.
- Route digital traces away from all analog inputs and associated components to minimize interference.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, another path must be found to return to the source and complete the circuit. If forced into a larger path, the chance that the signal radiates increases. Sensitive signals are more susceptible to EMI interference.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reducing the loop area enclosed by the source signal and the return current reduces the inductance in the path. Reducing the inductance reduces the EMI pickup and reduces the high-frequency impedance at the input of the device.
- Watch for parasitic thermocouples in the layout. Dissimilar metals going from each analog input to the sensor can create a parasitic thermocouple that can add an offset to the measurement. Differential inputs must be matched for both the inputs going to the measurement source.
- Fill void areas on signal layers with ground fill.

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10.4.2 Layout Example

Figure 10-12 shows a basic layout example for the ADS1x1C0x:

- C3 is the power supply decoupling capacitor. Place C3 as close as possible to the supply pin.
- Connect the GND pin to the ground plane.
- Differential antialiasing RC-filters are shown for the differential input pairs AIN0-AIN1 and AIN2-AIN3, respectively.
- R5, R6, and R7 are the I^2C bus pullup resistors.

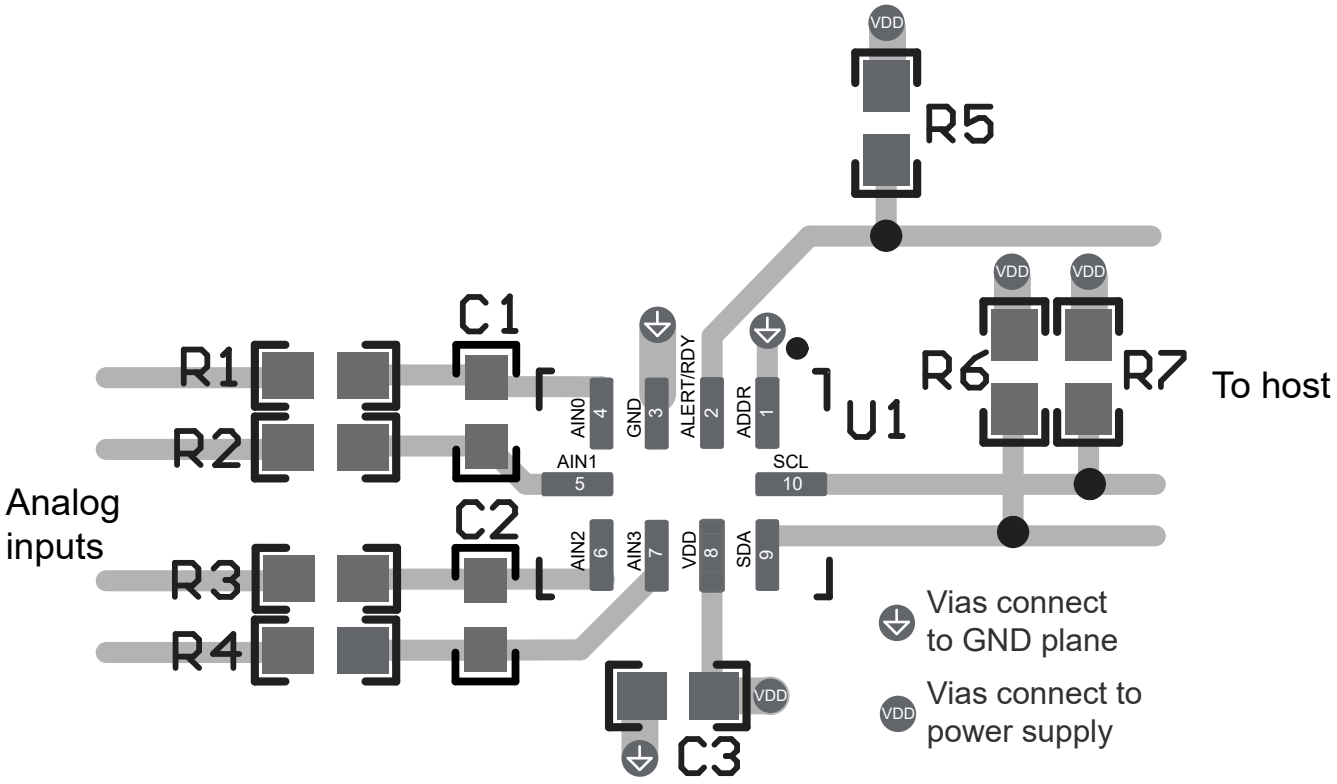


Figure 10-12. ADS1x1C02 X2QFN Package

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TMP61 ±1% 10kΩ Linear Thermistor With 0402 and 0603 Package Options* datasheet
- Texas Instruments, *LMT70A ±0.05°C Precision Analog Temperature Sensor, RTD and Precision NTC Thermistor IC* datasheet
- Texas Instruments, *INA185 26V, 350kHz, Bidirectional, High-Precision Current Sense Amplifier in UltraSmall (SOT-563) Package* datasheet

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PADS111C02IRUGR	Active	Preproduction	X2QFN (RUG) | 10	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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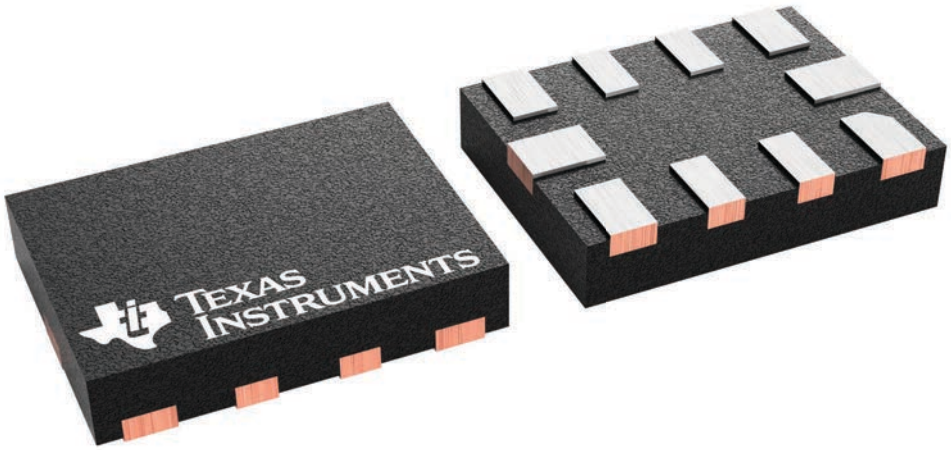
RUG 10

X2QFN - 0.4 mm max height

1.5 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

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Refer to the product data sheet for package details.



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