

ADC34DSO75 Quad Channel 14-Bit 3GSPS ADC With Event Detection and Internal Capture Memory

1 Features

- 14-bit, quad channel, 3GSPS ADC:
 - Thermal Noise: 68dBFS
 - Non-interleaved ADC architecture
 - Buffered analog inputs
 - Input full-scale: 1.4375Vpp
 - Full power input bandwidth (-3dB): 3GHz
 - Power consumption: 1.6W/channel (3GSPS)
 - Programmable FIR filter (up to 96-taps per channel)
- Digital storage oscilloscope (DSO) feature set:
 - Autonomous event detection via programmable thresholds
 - Cross-triggering across channels
 - Timestamping of detected events
 - Flexible event capture memory with up to 32720 samples/channel
 - Programmable pre-event and post-event capture windows
 - Programmable downsampler prior to memory
- OSPI for event readout:
 - 25MSPS clock rate, 200Mbps throughput
 - Supports daisy chaining of OSPI across chips
- CSPI for device control and configuration
- Voltage supply rails: 0.9V, 1.2V, and 1.8V

2 Applications

- Power supply glitch detection
- Spectrum analyzer
- High-speed digitizer
- Digital storage oscilloscope
- Wafer Inspection

3 Description

The ADC34DSO75 is a 14-bit, 3GSPS, quad channel analog to digital converter (ADC) with built-in event detection engine and internal capture memory to enable an integrated digital storage oscilloscope (DSO) feature set. The buffered analog inputs have an internal termination impedance of 100Ω or 200Ω and enable each ADC to achieve a full power input bandwidth of 3GHz (-3dB).

Each ADC channel has a dedicated event detection engine to control data capture and storage to on the chip memory for offload via OSPI. There are a number of event detection modes including absolute high threshold, low threshold, high and low threshold derived from an acquired baseline,

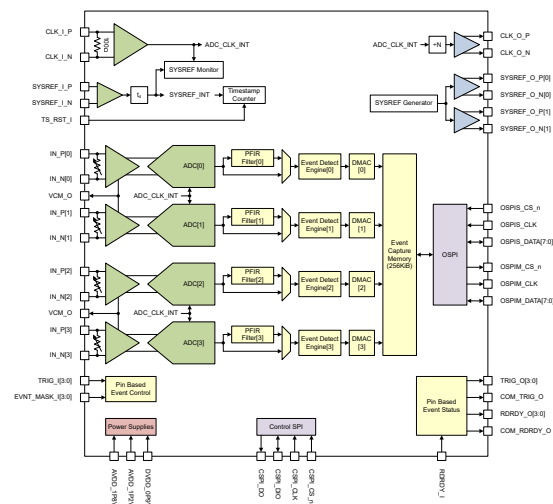
slope based triggering, and pin based triggering. Each ADC34DSO75 chip has a 256KiB memory which can be partitioned across the four channels of the ADC. Once an event is detected, the samples corresponding to the event can be written to the memory. Along with the event data, an event header (96 bytes per event) is stored in the memory and contains information about the event captured such as the event mode, voltage at event, and timestamp. The number of samples to be stored for the events is programmable for each channel and is based on pre and post event window sizes. The events are timestamp via a 64-bit counter in the event detection engine running at the full sample clock rate. The device has per channel pins for pin based triggering of events and also event detection status on the pins. The ADC34DSO75 has two SYSREF outputs to enable simple multi-device synchronization schemes.

The device configuration is done using the CSPI which is just a standard SPI bus. The on-chip memory is read out via an Octal Serial Peripheral Interface (OSPI). Multiple ADC chips can be daisy chained to enable a single (OSPI) interface to the host.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
ADC34DSO75	ANH (FCCSP, 289)	13.8mm × 13.8mm

- (1) For more information, see the [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram



4 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

4.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

4.3 Trademarks

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4.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2026	*	Initial Release

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PADC34DSO75IANH	Active	Preproduction	FCCSP (ANH) 289	119 JEDEC TRAY (5+1)	-	Call TI	Call TI	-	

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

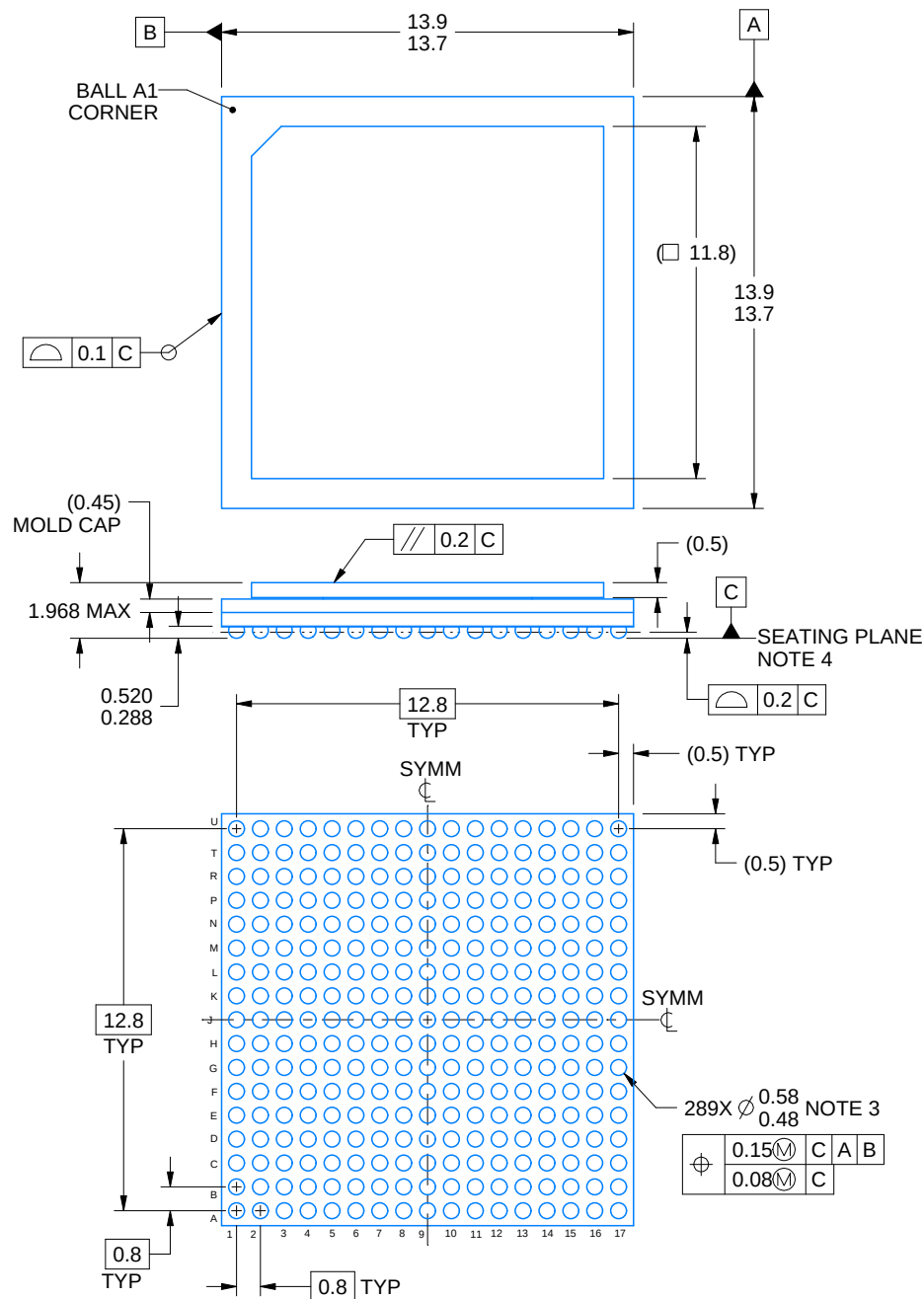
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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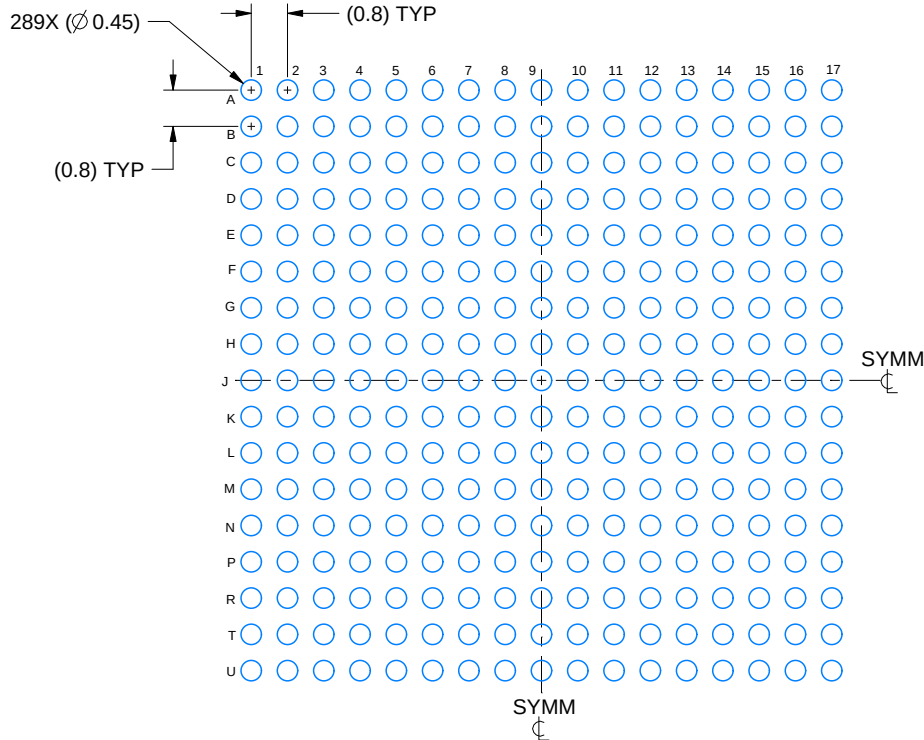
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, post reflow, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.

EXAMPLE BOARD LAYOUT

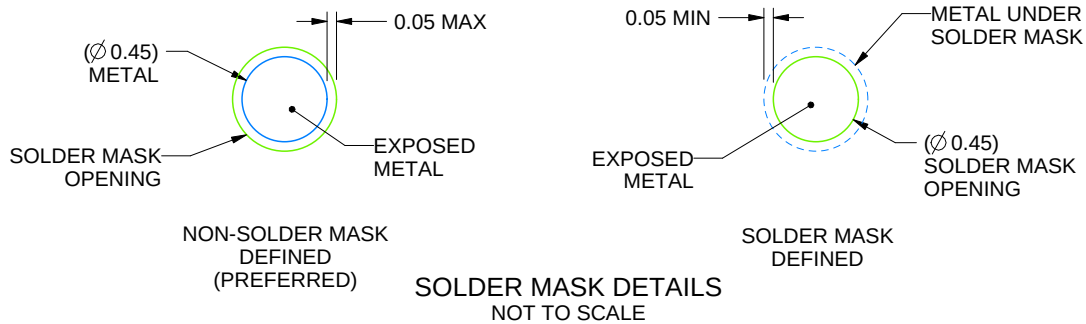
ANH0289A

FCCSP - 1.968 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 6X



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NOTES: (continued)

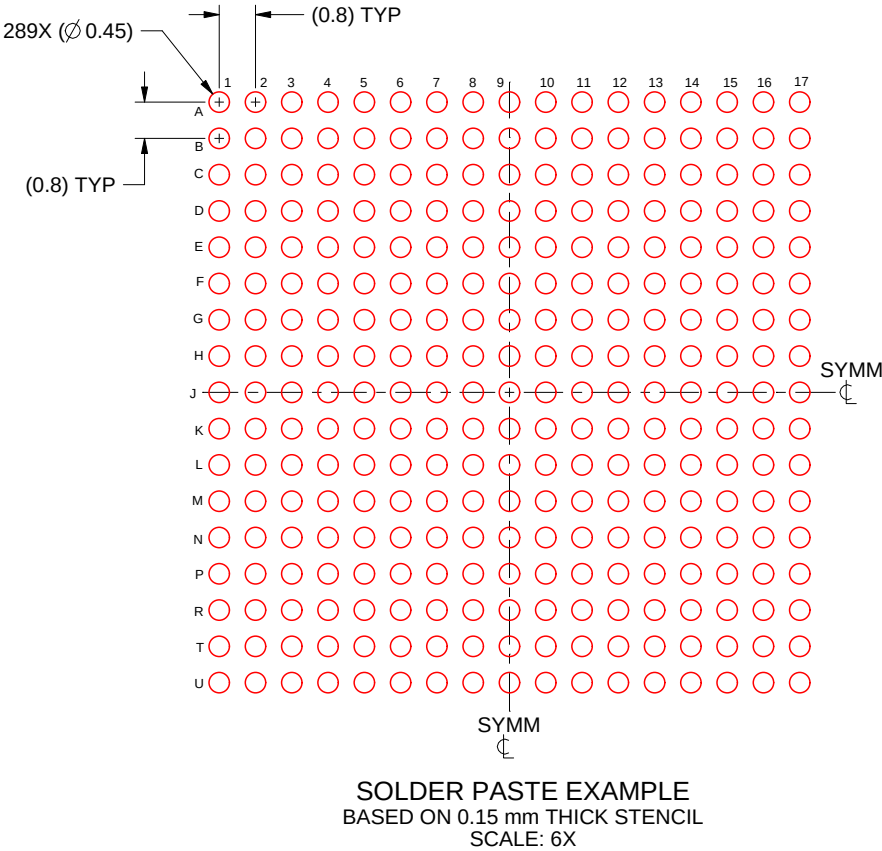
5. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SPRU811 (www.ti.com/lit/spru811).

EXAMPLE STENCIL DESIGN

ANH0289A

FCCSP - 1.968 mm max height

BALL GRID ARRAY



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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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