# ADC32RF72 Dual Channel 1.5GSPS 16-bit RF Sampling ADC

## 1 Features

- 16-bit, dual channel 1.5GSPS ADC
- Noise spectral density: -163.7dBFS/Hz
- Thermal Noise: 75.6dBFS
- Noise figure: 14.4dB
- Single core (non-interleaved) ADC architecture
- Aperture jitter: 40fs
- Buffered analog inputs
- Input fullscale: 1.44Vpp (4.1dBm)
- Full power input bandwidth (-3dB): 1.8GHz
- Ultra-low close-in residual phase noise:
  - −140dBc/Hz at 10kHz offset at 1GHz
- Spectral performance ($f_{IN}$ = 1GHz, -1dBFS):
  - $SNR_{flat}$: 72.1dBFS
  - HD2,3: 68dBc
  - Non HD2,3: 93dBFS
- 192-tap/ch programmable FIR equalizer filter
- 12-bit Fractional delay filter
- Digital down-converters (DDCs)
  - Up to 8 DDC
  - Complex output: /2, /3, /4, /5 to /32768 decimation
  - 48-bit NCO phase coherent frequency hopping
  - Fast frequency hopping: < 1µs
- JESD204B/C serial data interface
  - Maximum lane rate: 24.75Gbps
- Code error rate (CER): 1E-15 errors/sample
- Power consumption: 1.5W/channel (1.5GSPS)

## 2 Applications

- Phased array radar
- Wafer Inspection
- Spectrum analyzer
- Software defined radio (SDR)
- Electronic warfare
- High-speed digitizer
- Cable infrastructure
- Communications infrastructure

## 3 Description

The ADC32RF72 is a 16-bit, 1.5GSPS (non-interleaved), dual channel analog to digital converter (ADC). The device is designed for the highest signal-to-noise ratio (SNR) and delivers a noise spectral density of −163.7dBFS/Hz. Using internal averaging modes, the NSD can be improved to as low as -166.2dBFS/Hz. The buffered analog inputs support a programmable internal termination impedance of 50, 100, 200Ω with a full power input bandwidth of 1.8GHz (−3dB). The device lets the user select one input from IN1/2/3 in addition to IN0.

The device includes several digital processing features such as a 192-tap/ch programmable FIR filter for equalization, a 12-bit fractional delay filter as well as multiple digital down converters (DDCs). There are eight DDCs supporting decimation factors of /2, /3 and /5 up to /32768. The 48-bit NCOs support phase coherent frequency hopping.

The ADC32RF72 supports the JESD204B/C serial data interface with interface rates up to 24.75Gbps. The power efficient ADC architecture consumes 1.5W/ch at 1.5GSPS and provides power scaling with lower sampling rates.

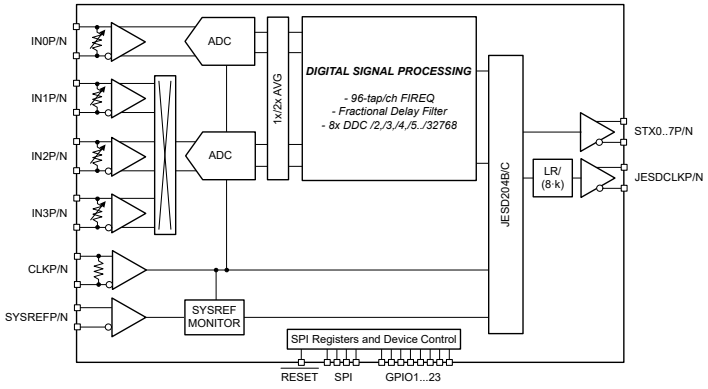
**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| ADC32RF72 | FCCSP | 13.8mm x 13.8mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

**Device Comparison**

| PART NUMBER | # OF CHANNELS |
|---|---|
| ADC32RF72 | 2 |
| ADC34RF72 | 4 |




**Block Diagram**

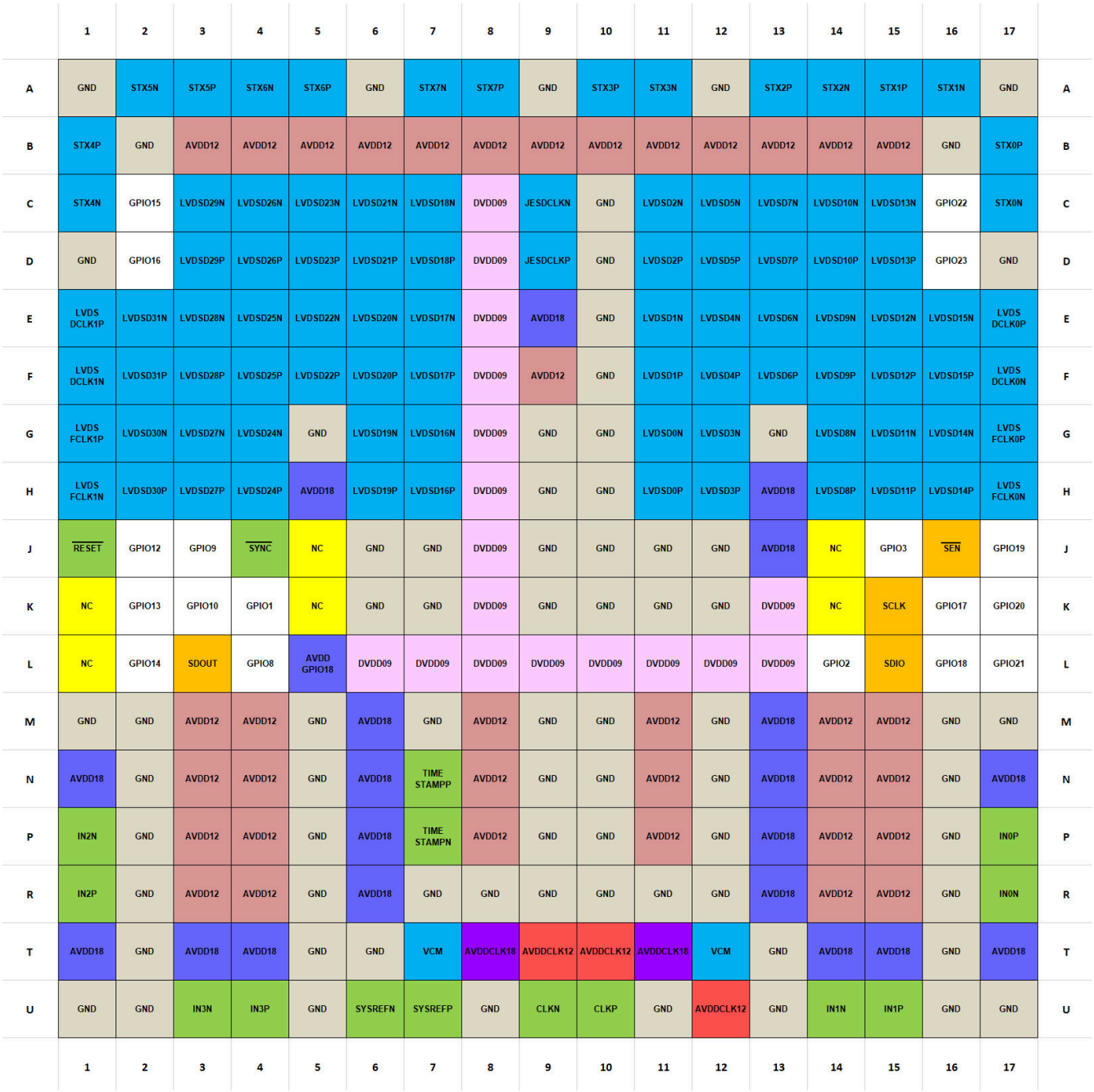
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# 4 Pin Configuration and Functions



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | STX5N | STX5P | STX6N | STX6P | GND | STX7N | STX7P | GND | STX3P | STX3N | GND | STX2P | STX2N | STX1P | STX1N | GND | A |
| B | STX4P | GND | AVDD12 | AVDD12 | AVDD12 | AVDD12 | AVDD12 | AVDD12 | AVDD12 | AVDD12 | AVDD12 | AVDD12 | AVDD12 | AVDD12 | AVDD12 | GND | STX0P | B |
| C | STX4N | GPIO15 | LVDSD29N | LVDSD26N | LVDSD23N | LVDSD21N | LVDSD18N | DVDD09 | JESDCLKN | GND | LVDSD2N | LVDSD5N | LVDSD7N | LVDSD10N | LVDSD13N | GPIO22 | STX0N | C |
| D | GND | GPIO16 | LVDSD29P | LVDSD26P | LVDSD23P | LVDSD21P | LVDSD18P | DVDD09 | JESDCLKP | GND | LVDSD2P | LVDSD5P | LVDSD7P | LVDSD10P | LVDSD13P | GPIO23 | GND | D |
| E | LVDS DCLK1P | LVDSD31N | LVDSD28N | LVDSD25N | LVDSD22N | LVDSD20N | LVDSD17N | DVDD09 | AVDD18 | GND | LVDSD1N | LVDSD4N | LVDSD6N | LVDSD9N | LVDSD12N | LVDSD15N | LVDS DCLK0P | E |
| F | LVDS DCLK1N | LVDSD31P | LVDSD28P | LVDSD25P | LVDSD22P | LVDSD20P | LVDSD17P | DVDD09 | AVDD12 | GND | LVDSD1P | LVDSD4P | LVDSD6P | LVDSD9P | LVDSD12P | LVDSD15P | LVDS DCLK0N | F |
| G | LVDS FCLK1P | LVDSD30N | LVDSD27N | LVDSD24N | GND | LVDSD19N | LVDSD16N | DVDD09 | GND | GND | LVDSD0N | LVDSD3N | GND | LVDSD8N | LVDSD11N | LVDSD14N | LVDS FCLK0P | G |
| H | LVDS FCLK1N | LVDSD30P | LVDSD27P | LVDSD24P | AVDD18 | LVDSD19P | LVDSD16P | DVDD09 | GND | GND | LVDSD0P | LVDSD3P | AVDD18 | LVDSD8P | LVDSD11P | LVDSD14P | LVDS FCLK0N | H |
| J | $\overline{\text{RESET}}$ | GPIO12 | GPIO9 | $\overline{\text{SYNC}}$ | NC | GND | GND | DVDD09 | GND | GND | GND | GND | AVDD18 | NC | GPIO3 | $\overline{\text{SEN}}$ | GPIO19 | J |
| K | NC | GPIO13 | GPIO10 | GPIO1 | NC | GND | GND | DVDD09 | GND | GND | GND | GND | DVDD09 | NC | SCLK | GPIO17 | GPIO20 | K |
| L | NC | GPIO14 | SDOUT | GPIO8 | AVDD GPIO18 | DVDD09 | DVDD09 | DVDD09 | DVDD09 | DVDD09 | DVDD09 | DVDD09 | DVDD09 | GPIO2 | SDIO | GPIO18 | GPIO21 | L |
| M | GND | GND | AVDD12 | AVDD12 | GND | AVDD18 | GND | AVDD12 | GND | GND | AVDD12 | GND | AVDD18 | AVDD12 | AVDD12 | GND | GND | M |
| N | AVDD18 | GND | AVDD12 | AVDD12 | GND | AVDD18 | TIME STAMPP | AVDD12 | GND | GND | AVDD12 | GND | AVDD18 | AVDD12 | AVDD12 | GND | AVDD18 | N |
| P | IN2N | GND | AVDD12 | AVDD12 | GND | AVDD18 | TIME STAMPN | AVDD12 | GND | GND | AVDD12 | GND | AVDD18 | AVDD12 | AVDD12 | GND | IN0P | P |
| R | IN2P | GND | AVDD12 | AVDD12 | GND | AVDD18 | GND | GND | GND | GND | GND | GND | AVDD18 | AVDD12 | AVDD12 | GND | IN0N | R |
| T | AVDD18 | GND | AVDD18 | AVDD18 | GND | GND | VCM | AVDDCLK18 | AVDDCLK12 | AVDDCLK12 | AVDDCLK18 | VCM | GND | AVDD18 | AVDD18 | GND | AVDD18 | T |
| U | GND | GND | IN3N | IN3P | GND | SYSREFN | SYSREFP | GND | CLKN | CLKP | GND | AVDDCLK12 | GND | IN1N | IN1P | GND | GND | U |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |

**Figure 4-1. 289-Ball Flip Chip BGA (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE (1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AVDD12 | B3,B4,B5,B6,B7,B8,B9, B10,B11,B12,B13,B14,B15,F9, M3,M4,M8,M11,M14, M15,N3,N4,N8,N11,N14, N15,P3,P4,P8,P11,P14, P15,R3,R4,R14,R15 | P | Analog 1.2V supply. Low noise LDO recommended. |

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**Table 4-1. Pin Functions (continued)**

| PIN | | TYPE (1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AVDDCLK12 | T9, T10, U12 | P | Clock power supply, 1.2V. Low noise LDO recommended |
| AVDD18 | E9,H5,H13,J13,M6,M13, N1,N6,N13,N17,P6,P13, R6,R13,T1,T3,T4,T14,T15, T17 | P | Analog 1.8V supply. Low noise LDO recommended |
| AVDDCLK18 | T8, T11 | P | Clock power supply, 1.8V. Low noise LDO recommended |
| AVDDGPIO18 | L5 | P | 1.8V power supply for GPIO pins. |
| CLKN, CLKP | U9, U10 | I | Differential clock input. Internal differential 100Ω termination and self bias to common mode voltage of 0.7V. Must be AC coupled externally. |
| DVDD09 | C8, D8, E8, F8,G8, H8, J8, K8, K13, L6,L7, L8, L9, L10, L11, L12, L13 | P | Digital power supply, 0.9V. Switching DC/DC regulator is recommended. |
| GND | A1,A6,A9,A12,A17,B2,B16, C10,D1,D10,D17,E10,F10,G5, G9,G10,G13,H9,H10, J6,J7,J9,J10,J11,J12,K6, K7,K9,K10,K11,K12,M1, M2,M5,M7,M9, M10,M12, M16,M17,N2,N5,N9,N10, N12,N16,P2,P5,P9,P10, P12,P16,R2,R5,R7,R8, R9,R10,R11,R12,R16,T2, T5,T6,T13,T16,U1,U2, U5,U8,U11,U13,U16,U17 | G | Ground, 0V |
| GPIO1, GPIO2, GPIO3 | K4, L14, J15 | I/O | The GPIO pins can be assigned different functions using SPI writes. See Section 7.5.1. |
| GPIO8, GPIO9, GPIO10 | L4, J3, K3, | I/O | |
| GPIO12 to GPIO23 | J2, K2, L2, C2, D2, K16,L16, J17, K17, L17, C16, D16 | I/O | |
| IN0N, IN0P | R17, P17 | I | Differential analog input, ch 0. Internal programmable 50, 100 and 200Ω termination. |
| IN1N, INIP | U14, U15 | I | Differential analog input, ch 1. Internal programmable 50, 100 and 200Ω termination. |
| IN2N, IN2P | P1, R1 | I | Differential analog input, ch 2. Internal programmable 50, 100 and 200Ω termination. |
| IN3N, IN3P | U3, U4 | I | Differential analog input, ch 3. Internal programmable 50, 100 and 200Ω termination. |
| JESDCLKN, JESDCLKP | C9, D9 | O | Differential JESD output clock. LVDS logic levels. Can be configured to serdes lane rate divided by (8x k). By default this feature is powered down and pins can be left floating. This output clock is derived directly from the internal SerDes PLL and does not provide deterministic latency. |
| LVDSDCLK0N, LVDSDCLK0P | F17, E17 | O | Differential LVDS bit clock output. Not yet supported in software. Leave as 'No Connect' |
| LVDSDCLK1N, LVDSDCLK1P | F1, E1 | O | |
| LVDSFCLK0N, LVDSFCLK0P | H17, G17 | O | Differential LVDS frame clock output. Not yet supported in software. Leave as 'No Connect' |
| LVDSFCLK1N, LVDSFCLK1P | H1, G1 | O | |


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**Table 4-1. Pin Functions (continued)**

| PIN | | TYPE (1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| LVDSD0N, LVDSD0P | G11, H11 | O | |
| LVDSD1N, LVDSD1P | E11, F11 | O | |
| LVDSD2N, LVDSD2P | C11, D11 | O | |
| LVDSD3N, LVDSD3P | G12, H12 | O | |
| LVDSD4N, LVDSD4P | E12, F12 | O | |
| LVDSD5N, LVDSD5P | C12, D12 | O | |
| LVDSD6N, LVDSD6P | E13, F13 | O | |
| LVDSD7N, LVDSD7P | C13, D13 | O | |
| LVDSD8N, LVDSD8P | G14, H14 | O | |
| LVDSD9N, LVDSD9P | E14, F14 | O | |
| LVDSD10N, LVDSD10P | C14, D14 | O | |
| LVDSD11N, LVDSD11P | G15, H15 | O | |
| LVDSD12N, LVDSD12P | E15, F15 | O | |
| LVDSD13N, LVDSD13P | C15, D15 | O | |
| LVDSD14N, LVDSD14P | G16, H16 | O | LVDS output interface<br>Not yet supported in software. Leave as 'No Connect' |
| LVDSD15N, LVDSD15P | E16, F16 | O | |
| LVDSD16N, LVDSD16P | G7, H7 | O | |
| LVDSD17N, LVDSD17P | E7, F7 | O | |
| LVDSD18N, LVDSD18P | C7, D7 | O | |
| LVDSD19N, LVDSD19P | G6, H6 | O | |
| LVDSD20N, LVDSD20P | E6, F6 | O | |
| LVDSD21N, LVDSD21P | C6, D6 | O | |
| LVDSD22N, LVDSD22P | E5, F5 | O | |
| LVDSD23N, LVDSD23P | C5, D5 | O | |
| LVDSD24N, LVDSD24P | G4, H4 | O | |
| LVDSD25N, LVDSD25P | E4, F4 | O | |
| LVDSD26N, LVDSD26P | C4, D4 | O | |
| LVDSD27N, LVDSD27P | G3, H3 | O | |
| LVDSD28N, LVDSD28P | E3, F3 | O | |

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**Table 4-1. Pin Functions (continued)**

| PIN | | TYPE (1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| LVDSD29N, LVDSD29P | C3, D3 | O | LVDS output interface<br>Not yet supported in software. Leave as 'No Connect' |
| LVDSD30N, LVDSD30P | G2, H2 | O | |
| LVDSD31N, LVDSD31P | E2, F2 | O | |
| NC | J5,J14,K1,K5,K14,L1 | - | Do not connect |
| $\overline{\text{RESET}}$ | J1 | I | Hardware reset. Active low. This pin has an internal 10kΩ pullup resistor to AVDD18. |
| SCLK | K15 | I | Serial interface clock input. This pin has an internal 10kΩ pulldown resistor. |
| SDIO | L15 | I/O | Serial interface data input/output. This pin has an internal 10kΩ pulldown resistor. |
| SDOUT | L3 | O | Serial interface data output. |
| $\overline{\text{SEN}}$ | J16 | I | Serial interface enable. Active low. This pin has an internal 10kΩ pullup resistor to AVDD18. |
| STX0N, STX0P | C17, B17 | O | Differential, high-speed serial JESD204B/C output data interface, lane 0 |
| STX1N, STX1P | A16, A15 | O | Differential, high-speed serial JESD204B/C output data interface, lane 1 |
| STX2N, STX2P | A14, A13 | O | Differential, high-speed serial JESD204B/C output data interface, lane 2 |
| STX3N, STX3P | A11, A10 | O | Differential, high-speed serial JESD204B/C output data interface, lane 3 |
| STX4N, STX4P | C1, B1 | O | Differential, high-speed serial JESD204B/C output data interface, lane 4 |
| STX5N, STX5P | A2, A3 | O | Differential, high-speed serial JESD204B/C output data interface, lane 5 |
| STX6N, STX6P | A4, A5 | O | Differential, high-speed serial JESD204B/C output data interface, lane 6 |
| STX7N, STX7P | A7, A8 | O | Differential, high-speed serial JESD204B/C output data interface, lane 7 |
| $\overline{\text{SYNC}}$ | J4 | I | JESD active low SYNC input. When SYNC is low and the device is configured, the device sends K characters on the JESD lanes. |
| SYSREFN, SYSREFP | U6, U7 | I | Differential SYSREF input (100Ω differential termination, self biased to 1.2V). AC and DC coupling is supported. |
| TIMESTAMPN, TIMESTAMPP | P7, N7 | I | Not yet supported in software. Can be connected to GND. |
| VCM | T7, T12 | O | Common mode voltage reference output. The two pins are internally shorted together. |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.


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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage range, AVDD18 | | –0.5 | 2.1 | V |
| Supply voltage range, AVDD12 | | –0.3 | 1.4 | |
| Supply voltage range, AVDDCLK18 | | –0.5 | 2.1 | |
| Supply voltage range, AVDDCLK12 | | –0.3 | 1.4 | |
| Supply voltage range, DVDD09 | | –0.3 | 1.2 | |
| Supply voltage range, AVDDGPIO18 | | –0.5 | 2.1 | |
| Voltage applied to input pins | IN0P/N, IN1P/N, IN2P/N, IN3P/N | –0.5 | 2.1 | |
| | CLKP/N | –0.3 | 1.4 | |
| | SYSREFP/N, TIMESTAMPP/N | –0.3 | 2.1 | |
| | GPIO1..23, $\overline{\text{RESET}}$, SCLK, $\overline{\text{SEN}}$, SDIO, $\overline{\text{SYNC}}$ | –0.5 | 2.1 | |
| Junction temperature, $T_J$ | | | 125 | ℃ |
| Storage temperature, $T_{stg}$ | | –65 | 150 | |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | 1000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | 150 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| AVDD18 | 1.8 V analog supply | | 1.75 | 1.8 | 1.85 | V |
| AVDD12 | 1.2 V analog supply | | 1.175 | 1.2 | 1.225 | |
| AVDDCLK18 | 1.8 V clock supply | | 1.75 | 1.8 | 1.85 | |
| AVDDCLK12 | 1.2 V clock supply | | 1.175 | 1.2 | 1.225 | |
| DVDD09 | 0.9 V digital supply | | 0.875 | 0.9 | 0.925 | |
| AVDDGPIO18 | 1.8 V GPIO Power Supply | | 1.75 | 1.8 | 1.85 | |
| $T_A$ | Operating free-air temperature | | –40 | | 105 | ℃ |
| $T_J$ | Operating junction temperature | | | | 110(1) | |

(1) Prolonged use above this junction temperature can increase the device failure-in-time (FIT) rate.

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## 5.4 Thermal Information

| THERMAL METRIC(1) | | ADC32RF72 ANH (BGA) 289 Balls | UNIT |
|---|---|---|---|
| $R_{\Theta JA}$ | Junction-to-ambient thermal resistance | 15.4 | °C/W |
| $R_{\Theta JC(top)}$ | Junction-to-case (top) thermal resistance | 0.5 | °C/W |
| $R_{\Theta JB}$ | Junction-to-board thermal resistance | 4.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.1 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 4.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

## 5.5 Electrical Characteristics - Power Consumption

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, ADC sampling rate = 1.5 GSPS, DDC Bypass mode, 50% clock duty cycle, nominal supply voltages and –1-dBFS differential input, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{AVDD18}$ | Supply current, 1.8V analog supply | Bypass mode LMFS = 4-2-1-1 | | 315 | 350 | mA |
| $I_{AVDD12}$ | Supply current, 1.2V analog supply | | | 915 | 1100 | |
| $I_{AVDDCLK18}$ | Supply current, 1.8V clock supply | | | 50 | 75 | |
| $I_{AVDDCLK12}$ | Supply current, 1.2V clock supply | | | 50 | 75 | |
| $I_{DVDD09}$ | Supply current, 0.9V digital supply | | | 1450 | 1800 | |
| $I_{AVDDGPIO18}$ | Supply current, 1.8V GPIO supply | | | 5 | | |
| $P_{DIS}$ | Power dissipation | | | 3.1 | | W |
| **POWER DOWN MODES** | | | | | | |
| $P_{DIS}$ | Fast power down mode power consumption | Fast wake up time | | 2.0 | | W |
| $P_{DIS}$ | Global power down mode power consumption | | | 0.4 | | |


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## 5.6 Electrical Characteristics - DC Specifications

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, ADC sampling rate = 1.5 GSPS, DDC Bypass mode, 50% clock duty cycle, nominal supply voltages and –1-dBFS differential input, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DC ACCURACY** | | | | | | |
| | No missing codes | | 16 | | | bits |
| DNL | Differential nonlinearity | $F_{IN}$ = 10 MHz | | 0.3 | | LSB |
| INL | Integral nonlinearity | $F_{IN}$ = 10 MHz | | 2.5 | | LSB |
| $V_{OS_ERR}$ | Offset error | | | 0.9 | | %FSR |
| $GAIN_{ERR}$ | Gain error | | | 1.0 | | %FSR |
| $GAIN_{Matching}$ | Gain matching across channels | | | 0.1 | | dB |
| **ADC ANALOG INPUTS (IN0P/N, IN1P/N, IN2P/N, IN3P/N)** | | | | | | |
| FS | Input full scale | Differential | | 1.4375 | | Vpp |
| $V_{ICM}$ | Input common model voltage | | 1.25 | 1.35 | 1.45 | V |
| $Z_{IN}$ | Differential input impedance | Differential at 100 MHz | | 100 | | Ω |
| $V_{OCM}$ | Output common mode voltage | | | 1.35 | | V |
| BW | Analog Input Bandwidth (-3dB) | | | 1.8 | | GHz |
| CMRR | Common mode rejection ratio | $F_{IN}$ = 100 MHz | | 30 | | dB |
| **CLOCK INPUT (CLKP/N)** | | | | | | |
| Input clock frequency | | | 500 | | 1500 | MHz |
| $V_{ID}$ | Differential input voltage | | 0.6 | 2.0 | 2.8 | Vpp |
| $V_{ICM}$ | Input common mode voltage | | | 0.7 | | V |
| $Z_{IN}$ | Differential input impedance | Differential at 1.5 GHz | | 100 | | Ω |
| Clock duty cycle | | | 30 | 50 | 70 | % |
| **SYSREF INPUT (SYSREFP/N)** | | | | | | |
| $V_{ID}$ | Differential input voltage | | 350 | 450 | 800 | mVpp |
| $V_{ICM}$ | Input common mode voltage | | 1.05 | 1.2 | 1.325 | V |
| **Digital Inputs (GPIO1..23, $\overline{\text{RESET}}$, SCLK, $\overline{\text{SEN}}$, SDIO, $\overline{\text{SYNC}}$)** | | | | | | |
| $V_{IH}$ | High level input voltage | | 1.15 | | | V |
| $V_{IL}$ | Low level input voltage | | | | 0.65 | V |
| $I_{IH}$ | High level input current | | -250 | | 250 | µA |
| $I_{IL}$ | Low level input current | | -250 | | 250 | µA |
| $C_I$ | Input capacitance | | | 2 | | pF |
| **DIGITAL OUTPUT (SDIO, SDOUT)** | | | | | | |
| $V_{OH}$ | High level output voltage | $I_{LOAD}$ = -400 µA | AVDDG PIO18– 0.1 | AVDDG PIO18 | | V |
| $V_{OL}$ | Low level output voltage | $I_{LOAD}$ = 400 µA | | | 0.1 | V |
| **CML SERDES OUTPUTS: STX[0..7]P/N** | | | | | | |
| $V_{OD}$ | SerDes transmitter output amplitude | differential peak-peak | | 950 | | mVpp |
| $V_{OCM}$ | SerDes transmitter output common mode | | | 450 | | mV |
| $Z_{TX}$ | SerDes transmitter single ended termination impedance | | | 50 | | Ω |
| | Transmitter short-circuit current | Transmitter pins shorted to any voltage between –0.25 V and 1.45 V | –100 | | 100 | mA |

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## 5.7 Electrical Characteristics - AC Specifications

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, ADC sampling rate = 1.5 GSPS, 100Ω termination, DDC Bypass mode, 50% clock duty cycle, nominal supply voltages and –1-dBFS differential input, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN(2) | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **AC ACCURACY** | | | | | | |
| $NSD_{flat}$ | Noise Spectral Density | $f_{IN}$ = 600MHz, $A_{IN}$ = -20dBFS | | –163.7 | | dBFS/Hz |
| NF | Noise Figure (100Ω termination) | $f_{IN}$ = 600MHz, $A_{IN}$ = -20dBFS | | 14.4 | | dB |
| SNR | Signal to noise ratio | $f_{IN}$ = 100MHz | | 73.0 | | dBFS |
| $SNR_{flat}$ (1) | Signal to noise ratio measured from 100MHz to FS/2 within the Nyquist zone | $f_{IN}$ = 100MHz | 72.0 | 75.3 | | dBFS |
| | | $f_{IN}$ = 600MHz | | 73.4 | | |
| | | $f_{IN}$ = 600MHz, $A_{IN}$ = -20dBFS | | 75.5 | | |
| | | $f_{IN}$ = 900MHz | | 72.1 | | |
| | | $f_{IN}$ = 1.4GHz | | 69.0 | | |
| $SINAD_{flat}$ (1) | Signal to noise and distortion ratio | $f_{IN}$ = 100MHz | | 74.3 | | dBFS |
| ENOB | Effective number of bits | $f_{IN}$ = 100MHz | | 11.8 | | Bits |
| THD | Total Harmonic Distortion (First five harmonics) | $f_{IN}$ = 100MHz | | 82 | | dBc |
| | | $f_{IN}$ = 600MHz | | 74 | | |
| | | $f_{IN}$ = 900MHz | | 68 | | |
| | | $f_{IN}$ = 1.4GHz | | 57 | | |
| HD2 | Second Harmonic Distortion | $f_{IN}$ = 100MHz | 74 | 88 | | dBc |
| | | $f_{IN}$ = 600MHz | | 77 | | |
| | | $f_{IN}$ = 900MHz | | 74 | | |
| | | $f_{IN}$ = 1.4GHz | | 64 | | |
| HD3 | Third Harmonic Distortion | $f_{IN}$ = 100MHz | 74 | 83 | | dBc |
| | | $f_{IN}$ = 600MHz | | 77 | | |
| | | $f_{IN}$ = 900MHz | | 68 | | |
| | | $f_{IN}$ = 1.4GHz | | 58 | | |
| Non HD2,3 | Spur free dynamic range (excluding HD2 and HD3) | $f_{IN}$ = 100MHz | 80 | 95 | | dBFS |
| | | $f_{IN}$ = 600MHz | | 90 | | |
| | | $f_{IN}$ = 900MHz | | 93 | | |
| | | $f_{IN}$ = 1.4GHz | | 79 | | |
| IMD3 | Two tone inter-modulation distortion | $f_1$ = 100MHz, $f_2$ = 200MHz, $A_{IN}$ = -7dBFS/tone | | 89 | | dBFS |
| | | $f_1$ = 0.9GHz, $f_2$ = 1.0GHz, $A_{IN}$ = -7dBFS/tone | | 76 | | |

(1) For detailed description of $SNR_{flat}$ and $NSD_{flat}$ see Section 6.
(2) $SNR_{flat}$, HD3 and Non HD23 minimum values are specified by final test; HD2 is specified by bench characterization.


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## 5.8 Timing Requirements

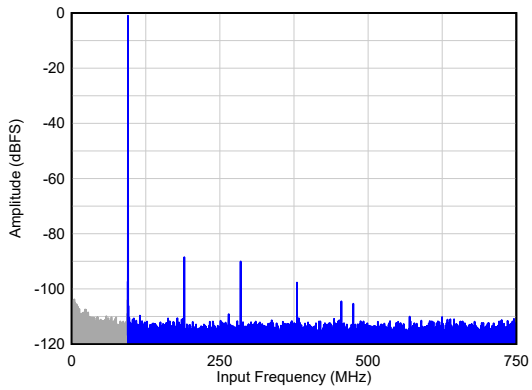
Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, ADC sampling rate = 1.5 GSPS, DDC Bypass mode, 50% clock duty cycle, nominal supply voltages and –1-dBFS differential input, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ADC Timing Specifications** | | | | | | |
| $T_{AD}$ | Aperture Delay | | | 0.15 | | ns |
| | Aperture Delay variation | | | 0.05 | | ns |
| $T_A$ | Aperture Jitter | | | 40 | | fs |
| CER | Code error rate | | | 1e-15 | | errors/ sample |
| | Wake up time | time to valid data (SNR within 2dB of data sheet values) after coming out of fast power down (JESD stays active) | | | 5 | µs |
| **LATENCY: $t_{PD}$ + $t_{ADC}$** | | | | | | |
| $t_{PD}$ | Propagation delay | | | 1 | | ns |
| $t_{ADC}$ | ADC latency from sampling instant to JESD output | DDC bypass, LMFS = 8411 | | 524 | | ADC clock cycles |
| **SERIAL PROGRAMMING INTERFACE (SCLK, SEN, SDIO) - Input** | | | | | | |
| $f_{CLK(SCLK)}$ | Serial clock frequency | | 1 | | 50 | MHz |
| $t_{S(SEN)}$ | SEN to rising edge of SCLK | | 10 | | | ns |
| $t_{H(SEN)}$ | SEN from rising edge of SCLK | | 10 | | | ns |
| $t_{SU(SDIO)}$ | SDIO to rising edge of SCLK | | 10 | | | ns |
| $t_{H(SDIO)}$ | SDIO from rising edge of SCLK | | 10 | | | ns |
| **SERIAL PROGRAMMING INTERFACE (SDIO, SDOUT) - Output** | | | | | | |
| $t_{(OZD)}$ | SDIO tri-state to driven | | | | 10 | ns |
| $t_{(ODZ)}$ | SDIO data to tri-state | | | | 14 | ns |
| $t_{(OD)}$ | SDIO valid from falling edge of SCLK | | | | 10 | ns |
| **Timing: SYSREFP/N** | | | | | | |
| $t_{s(SYSREF)}$ | Setup time, SYSREFP/N valid to rising edge of CLKP/N | | | 50 | | ps |
| $t_{h(SYSREF)}$ | Hold time, SYSREFP/N valid to rising edge of CLKP/N | | | 50 | | ps |
| **CML SerDes Outputs: STX[0..7]P/N** | | | | | | |
| $f_{Serdes}$ | SerDes bit rate | | 4.0 | | 24.75 | Gbps |
| $R_J$ | Random jitter | | | 0.45 | | ps |
| $D_J$ | Deterministic jitter | | | 12.5 | | ps |
| $T_J$ | Total jitter, peak-peak | | | 19.7 | | ps |

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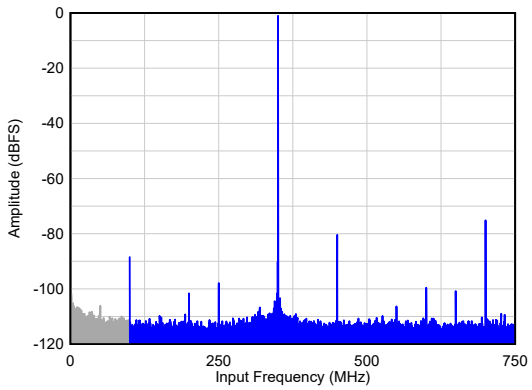
## 5.9 Typical Characteristics

Typical values are at $T_A$ = 25°C, ADC sampling rate = 1.5GSPS, 50% clock duty cycle, nominal supplies and –1dBFS differential input, 100Ω termination, unless otherwise noted



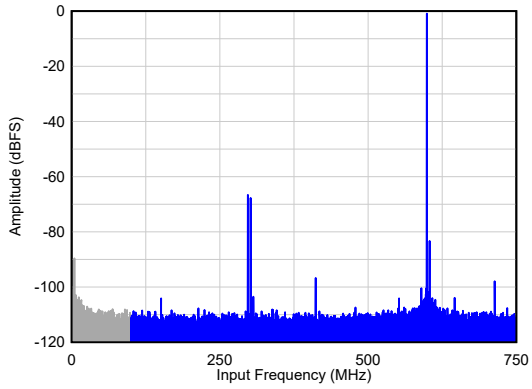

$SNR_{flat}$ = 74.6dBFS

**Figure 5-1. Single Tone FFT at $F_{IN}$ = 100MHz**



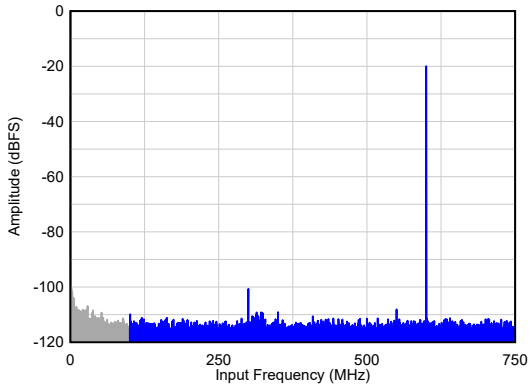

$SNR_{flat}$ = 73.7dBFS

**Figure 5-2. Single Tone FFT at $F_{IN}$ = 300MHz**



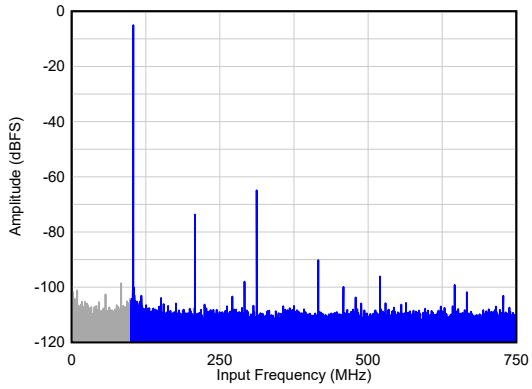

$SNR_{flat}$ = 71.5dBFS

**Figure 5-3. Single Tone FFT at $F_{IN}$ = 900MHz**



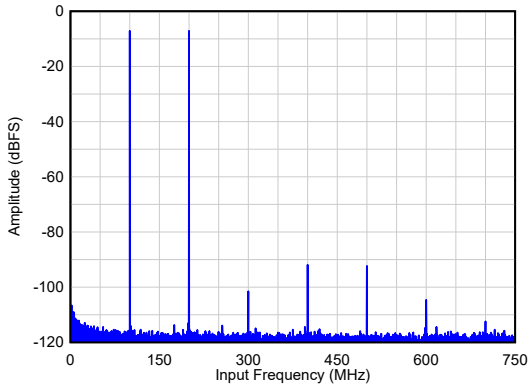

$SNR_{flat}$ = 74.6dBFS, $A_{IN}$ = -20dBFS

**Figure 5-4. Single Tone FFT at $F_{IN}$ = 900MHz**




$SNR_{flat}$ = 67.8dBFS

**Figure 5-5. Single Tone FFT at $F_{IN}$ = 1400MHz**



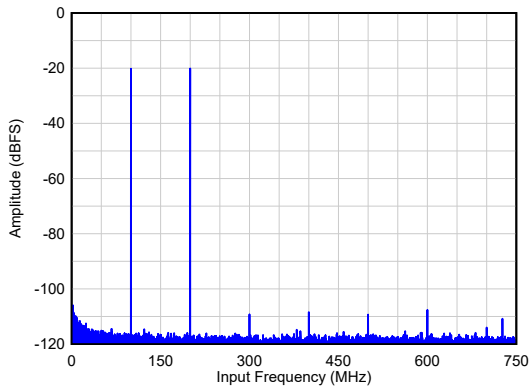

$A_{IN}$ = -7dBFS/tone

**Figure 5-6. Two Tone FFT at $F_{IN}$ = 100/200MHz**


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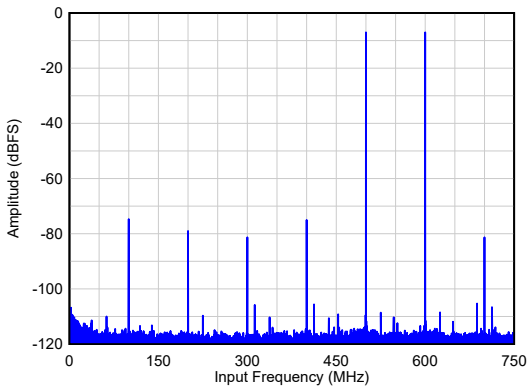
## 5.9 Typical Characteristics (continued)

Typical values are at $T_A$ = 25°C, ADC sampling rate = 1.5GSPS, 50% clock duty cycle, nominal supplies and –1dBFS differential input, 100Ω termination, unless otherwise noted



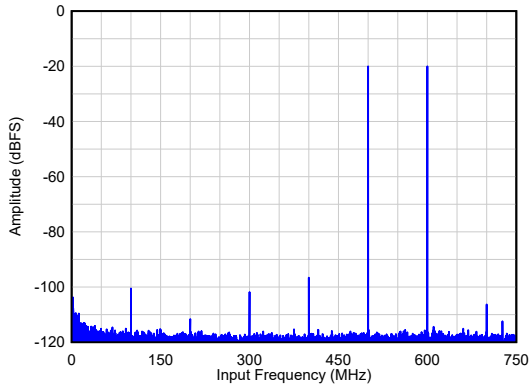

$A_{IN}$ = -20dBFS/tone

**Figure 5-7. Two Tone FFT at $F_{IN}$ = 100/200MHz**




$A_{IN}$ = -7dBFS/tone

**Figure 5-8. Two Tone FFT at $F_{IN}$ = 900/1000MHz**




$A_{IN}$ = -20dBFS/tone

**Figure 5-9. Two Tone FFT at $F_{IN}$ = 900/1000MHz**

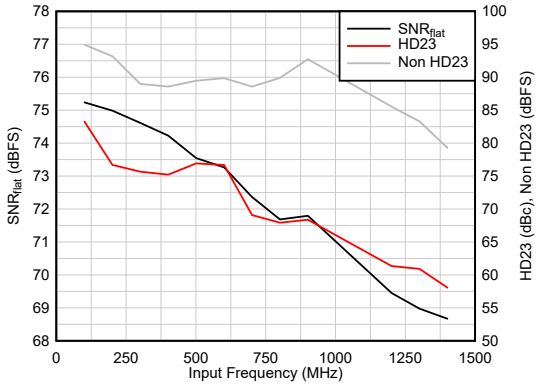
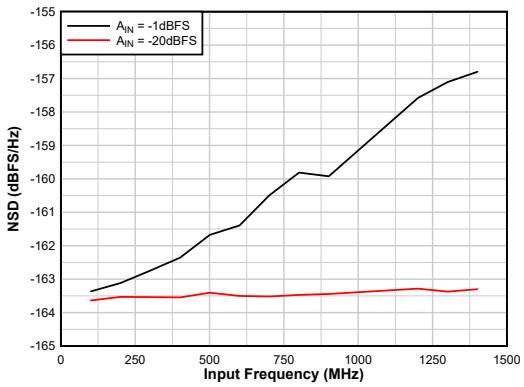
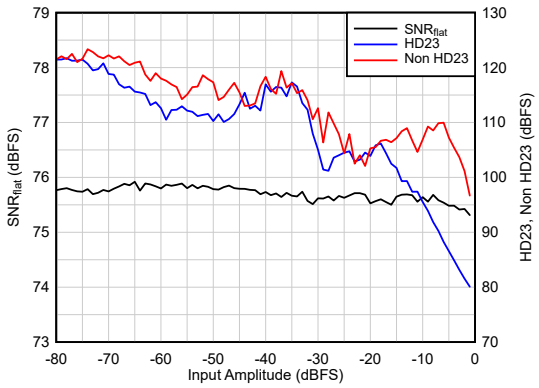



**Figure 5-10. AC Performance vs $F_{IN}$**




Termination = 50ohm

**Figure 5-11. NSD Performance vs $F_{IN}$**



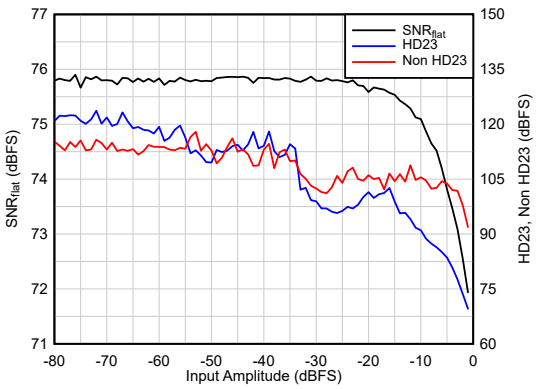

$F_{IN}$ = 100MHz

**Figure 5-12. AC Performance vs $A_{IN}$**

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## 5.9 Typical Characteristics (continued)

Typical values are at $T_A$ = 25°C, ADC sampling rate = 1.5GSPS, 50% clock duty cycle, nominal supplies and –1dBFS differential input, 100Ω termination, unless otherwise noted




$F_{IN}$ = 900MHz

**Figure 5-13. AC Performance vs $A_{IN}$**

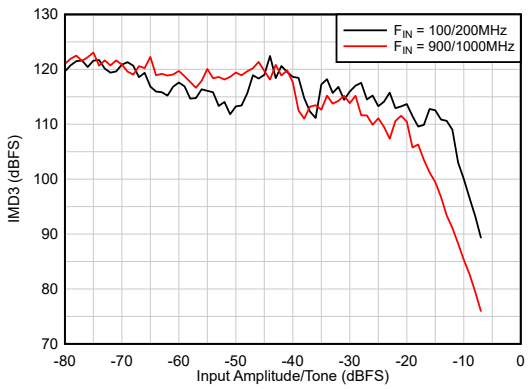
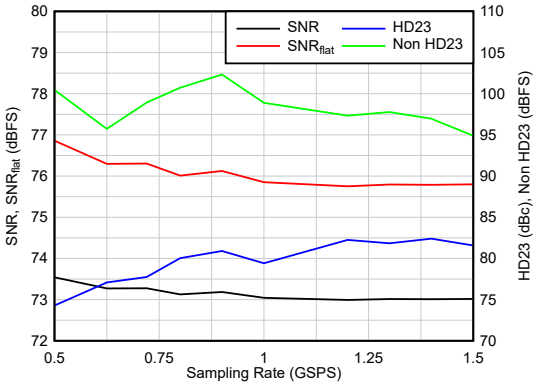



**Figure 5-14. IMD3 Performance vs $A_{IN}$**




$F_{IN}$ = 100MHz

**Figure 5-15. AC Performance vs $F_S$**

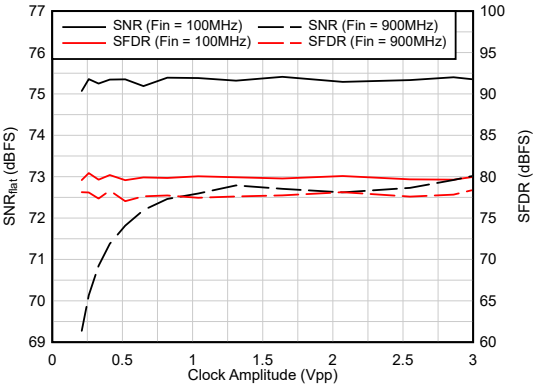



**Figure 5-16. AC Performance vs Clock Amplitude**

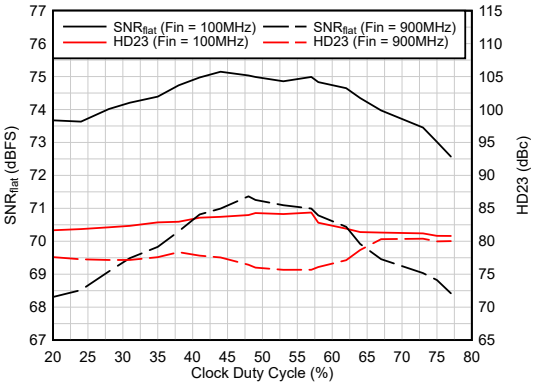



**Figure 5-17. AC Performance vs Clock Duty Cycle**

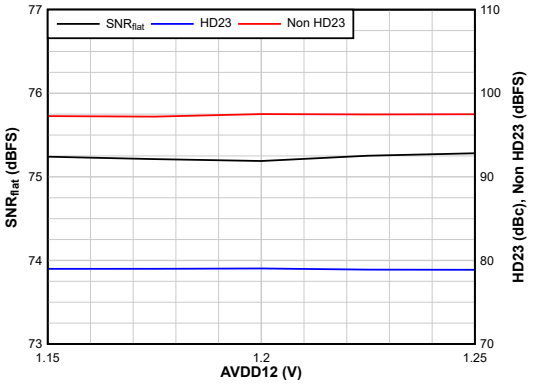



**Figure 5-18. AC Performance vs AVDD12 Supply**


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## 5.9 Typical Characteristics (continued)

Typical values are at $T_A$ = 25°C, ADC sampling rate = 1.5GSPS, 50% clock duty cycle, nominal supplies and –1dBFS differential input, 100Ω termination, unless otherwise noted

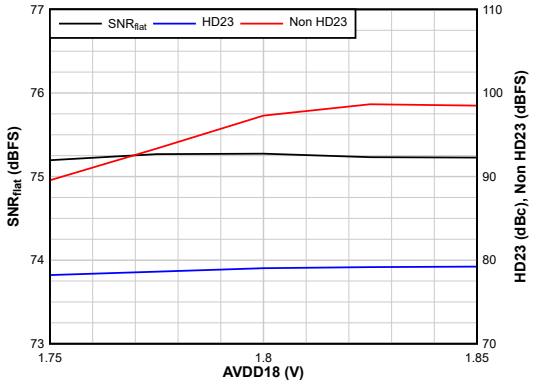



**Figure 5-19. AC Performance vs AVDD18 Supply**

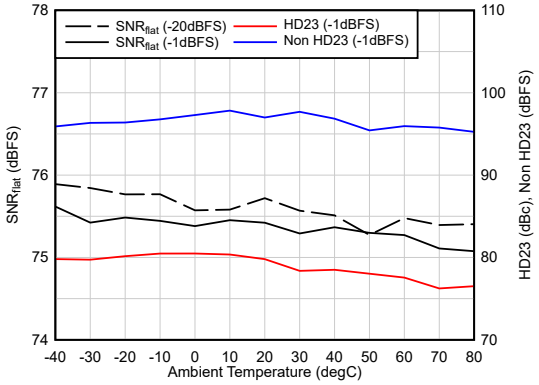
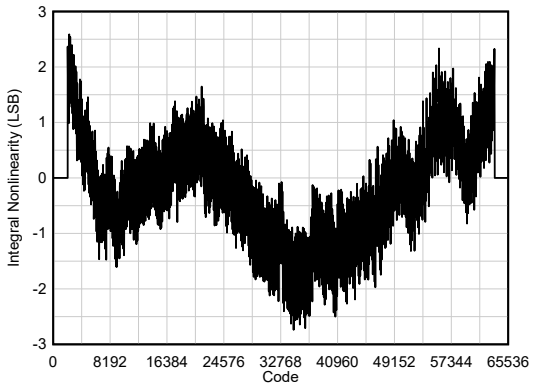
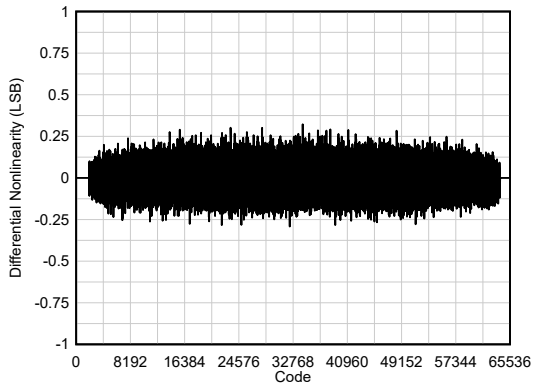



**Figure 5-20. AC Performance vs Temperature**




$F_{IN}$ = 100MHz

**Figure 5-21. INL vs Code**




$F_{IN}$ = 100MHz

**Figure 5-22. DNL vs Code**

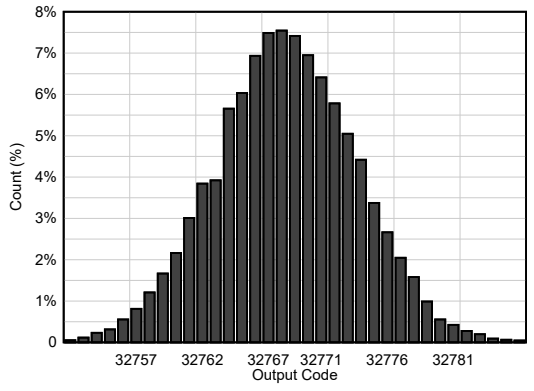



**Figure 5-23. Idle Channel Histogram**

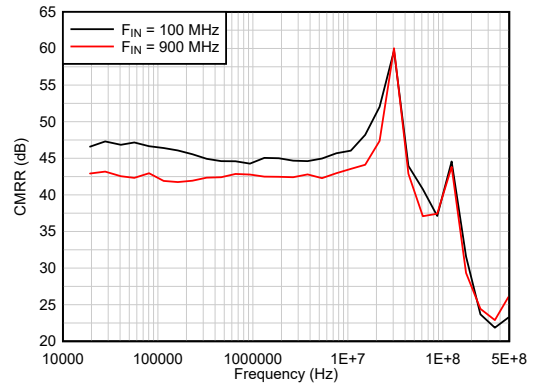



**Figure 5-24. CMRR**

## 5.9 Typical Characteristics (continued)

Typical values are at $T_A$ = 25°C, ADC sampling rate = 1.5GSPS, 50% clock duty cycle, nominal supplies and –1dBFS differential input, 100Ω termination, unless otherwise noted

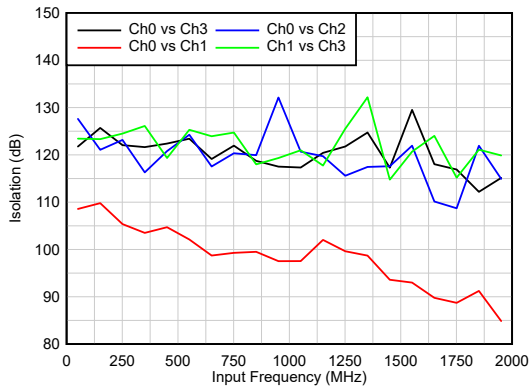
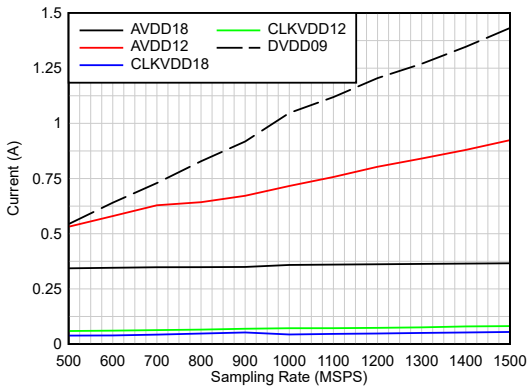
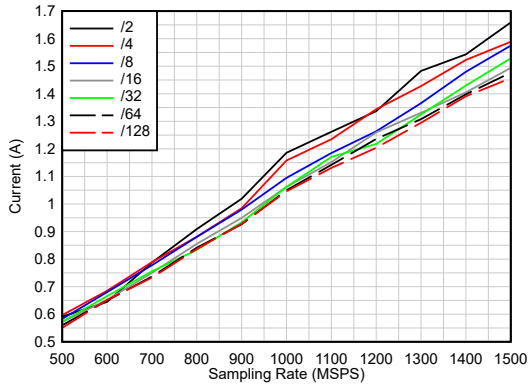



**Figure 5-25. Channel Isolation**



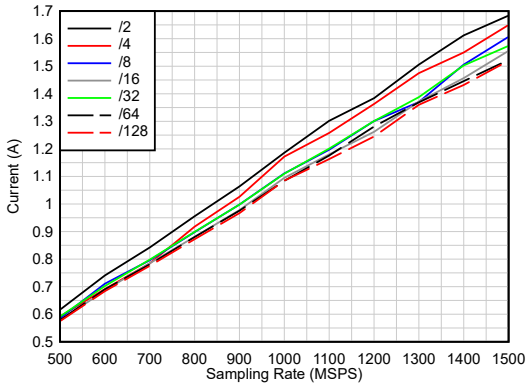

LMFS = 4-2-1-1

**Figure 5-26. Currents vs Sampling Rate**



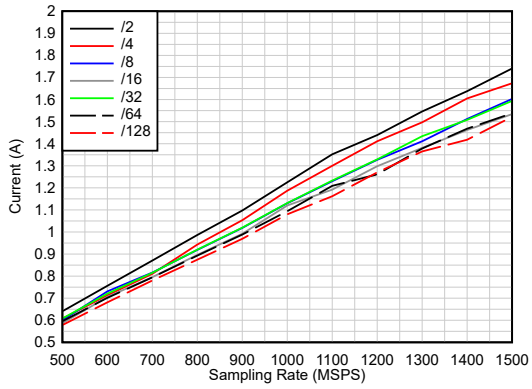

Dual band, LMFS = 8-4-1-1

**Figure 5-27. DVDD09 current vs Decimation**



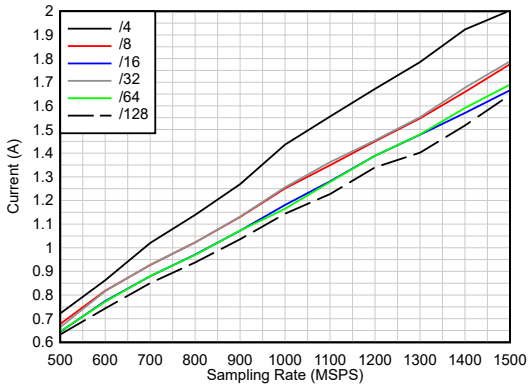

Dual band, LMFS = 4-4-2-1

**Figure 5-28. DVDD09 current vs Decimation**




Quad band, LMFS = 8-8-2-1

**Figure 5-29. DVDD09 current vs Decimation**



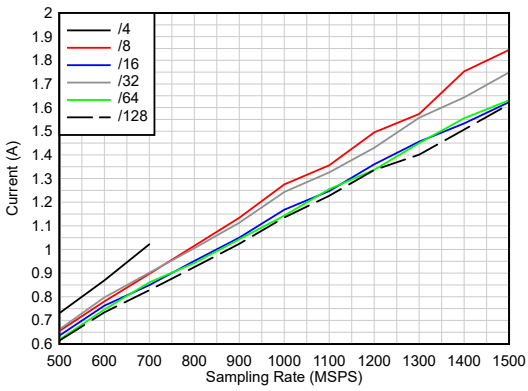

Quad band, LMFS = 4-8-4-1

**Figure 5-30. DVDD09 current vs Decimation**


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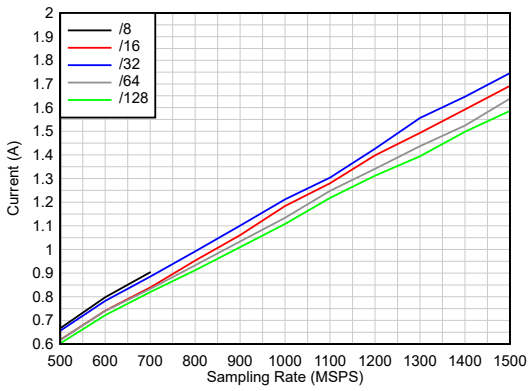
## 5.9 Typical Characteristics (continued)

Typical values are at $T_A$ = 25°C, ADC sampling rate = 1.5GSPS, 50% clock duty cycle, nominal supplies and –1dBFS differential input, 100Ω termination, unless otherwise noted



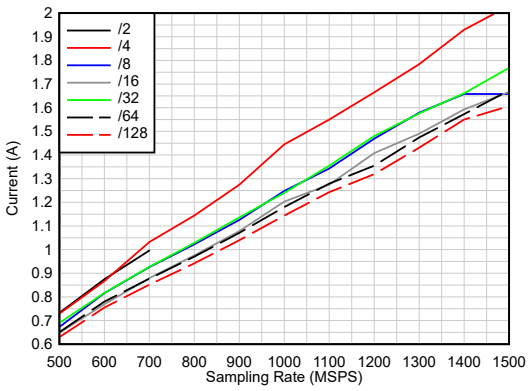

Quad band, LMFS = 2-8-8-1

**Figure 5-31. DVDD09 current vs Decimation**



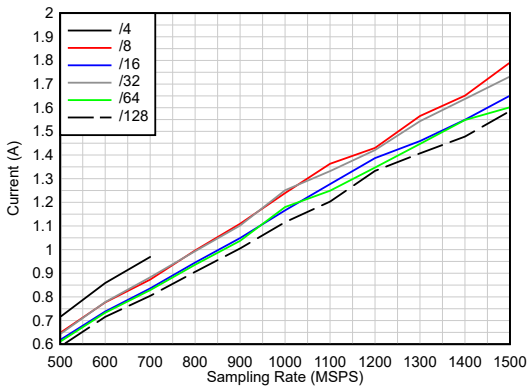

Quad band, LMFS = 1-8-16-1

**Figure 5-32. DVDD09 current vs Decimation**



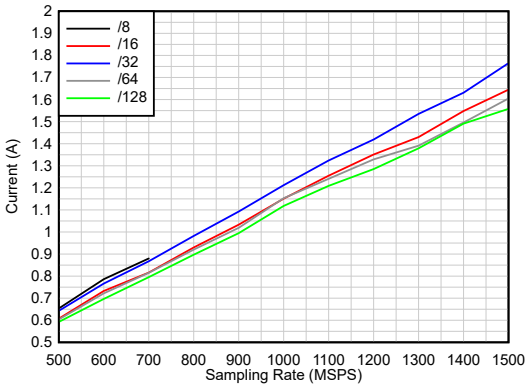

Octal band, LMFS = 8-16-4-1

**Figure 5-33. DVDD09 current vs Decimation**




Octal band, LMFS = 4-16-8-1

**Figure 5-34. DVDD09 current vs Decimation**




Octal band, LMFS = 2-16-16-1

**Figure 5-35. DVDD09 current vs Decimation**

# 6 Parameter Measurement Information

The ADC32RF72 has 1/f noise with a corner frequency of approximately 100MHz. To better illustrate the true noise floor for high performance and RF sampling applications, the ADC noise performance is specified in the following two ways.

SNR: Measured across the full Nyquist zone including 1/f noise

$SNR_{flat}$, $NSD_{flat}$: Measured in the flat noise region from 100MHz to FS/2 (750MHz)

Reducing the measurement bandwidth by 100MHz (starting at 100MHz instead of 0Hz) improves the SNR by approximately 0.6dB (10log(750MHz/650MHz) = 10log(0.06) = 0.62dB) assuming flat, uniform noise across the Nyquist zone.

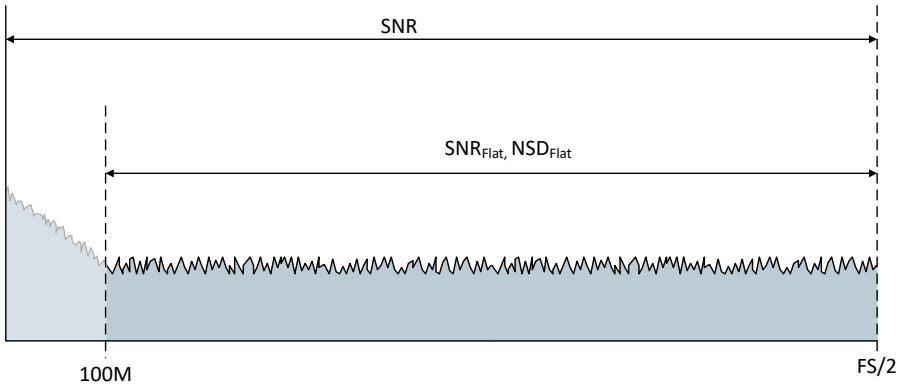



**Figure 6-1. SNR (DC to FS/2) vs $SNR_{flat}$ (100MHz to FS/2)**

Assuming $NSD_{flat}$ = -163.7dBFS/Hz

$SNR_{flat}$ calculates to:

-(-163.7dBFS/Hz + 10log(650MHz)) = -(-163.7 + 88.1)dBFS = 75.6dBFS (1)

The 1/f noise is approximately 76.4dBFS. The 1/f noise measurement is shown in Figure 6-2 with a resolution bandwidth of approximately 6MHz. The SNR for full Nyquist zone including 1/f noise calculates to:

$SNR_{1/f}$ + $SNR_{flat}$ = (2)

$$SNR_{1/f} + SNR_{flat} = 10log\sqrt{\left(10^{\frac{-SNR_{1/f}}{20}}\right)^2 + \left(10^{\frac{-SNR_{flat}}{20}}\right)^2} = 10log\sqrt{\left(10^{\frac{-76.4}{20}}\right)^2 + \left(10^{\frac{-75.6}{20}}\right)^2} = 73dBFS$$

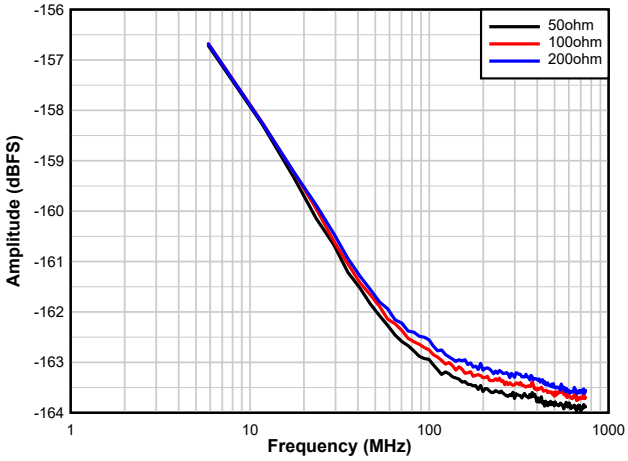



**Figure 6-2. 1/f Noise Measurement**


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# 7 Detailed Description

## 7.1 Overview

The ADC32RF72 is a 16-bit, 1.5GSPS (non-interleaved), dual channel analog to digital converter (ADC). The design maximizes signal-to-noise ratio (SNR) and delivers a noise spectral density of -163.7dBFS/Hz. When providing the input signal to 2 ADC inputs, the NSD can be improved to as low as -166.2dBFS/Hz using internal digital averaging. The device lets the user select ADC0 and any of the 3 remaining ADC channels - two ADC channels (ADC0/1) on the same side of the package for 2x averaging or on the opposite side (ADC0/2) of the package for best isolation.

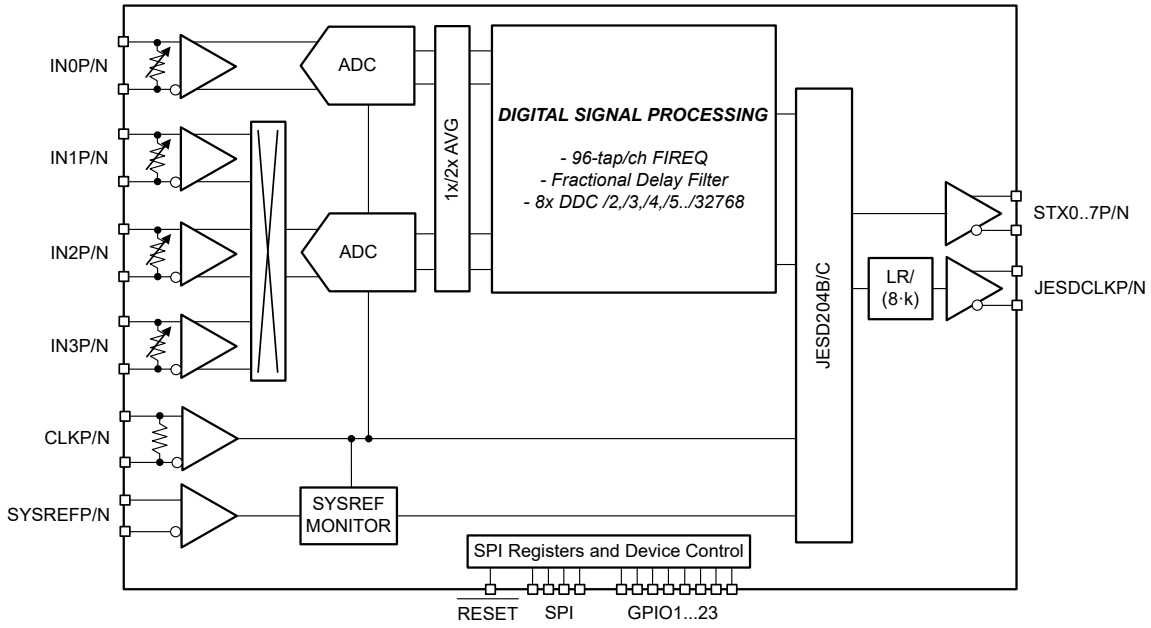
The analog signal input is buffered and supports a programmable internal termination impedance of 50Ω, 100Ω and 200Ω. The full power input bandwidth is 1.8GHz (-3dB) and the device supports direct RF sampling with input frequencies in from DC through L-band. The ADC32RF72 is designed for low residual phase noise to support high performance radar applications.

The device includes several digital processing features such as a 192-tap/ch programmable FIR filter for equalization, a 12-bit fractional delay filter as well as multiple digital down converters (DDCs). There are eight digital down converters supporting decimation factors of /2, /3 and /5. The 48-bit NCOs support phase coherent frequency hopping. Using the GPIO pins for NCO frequency control, frequency hopping can be achieved in less than 1µs. The digital down converters provide support for a wide range of instantaneous bandwidth (IBW) requirements, from wide band mode with /2 complex decimation to narrow bandwidth channels with complex decimation of /32768. The final /2 decimation stage features programmable filter coefficients.

The device supports the JESD204B/C serial data interface using 64b/66b and 8b/10b encoding with subclass 1 deterministic latency using data rates up to 24.75Gbps. Using both interface options, the ADC32RF7xcan output both full spectrum (DDC bypass) and decimated data. Furthermore, the SerDes PLL (lane rate /(8x k)) can be output to the FPGA to simplify system clocking.

The device requires 3 different power rails: 1.8V, 1.2V and 0.9V.

## 7.2 Functional Block Diagram




**Block Diagram**

## 7.3 Feature Description

### *7.3.1 Analog Inputs*

The analog inputs of the ADC32RF72 have internal buffers which isolate the sampling capacitor from the external input circuitry. The analog inputs have a programmable, differential split termination with internal biasing as shown in Figure 7-1. The differential termination can be selected to differential 50Ω, 100Ω or 200Ω via SPI register write. Both AC-coupling and DC-coupling of the analog inputs is supported.

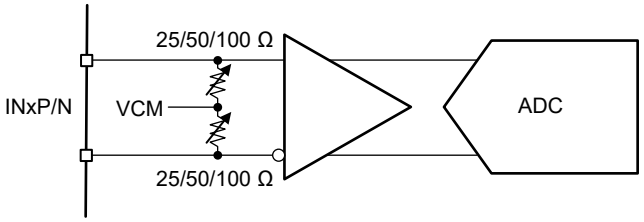



**Figure 7-1. Analog input (internal) circuitry**

The following parameters can be programmed:

**Table 7-1. Input Termination Programming (x = 0,1,2,3)**

| System Parameter Name | Size (bits) | Default | Reset | Description |
|---|---|---|---|---|
| ADC{x}_INPUT_TERM_SEL | 2 | 0 | R/W | Select ADC{x} input termination setting<br>0: 50Ω differential<br>1: 100Ω differential<br>2: 200Ω differential |

#### 7.3.1.1 Input Bandwidth

The input bandwidth (-3dB) with internal 50Ω, 100Ω and 200Ω differential termination is shown in Figure 7-2 along with the S11 responses (Figure 7-2). With 100Ω termination the input bandwidth is approximately 1.8GHz (-3dB). Figure 7-4 shows the frequency response with 100Ω termination using the external matching network shown in Figure 7-5.

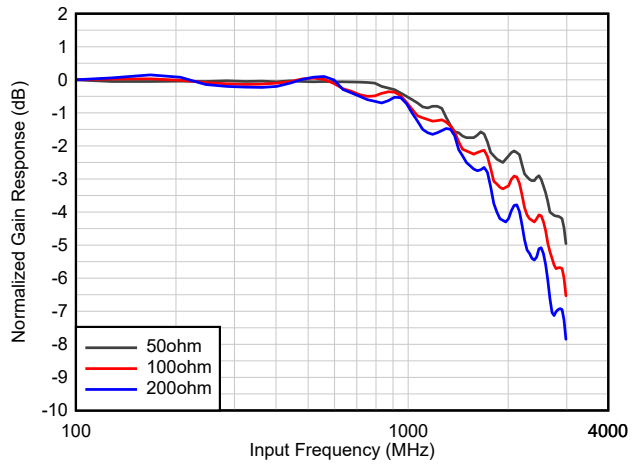



**Figure 7-2. Input Bandwidth Plot (6dB pad)**

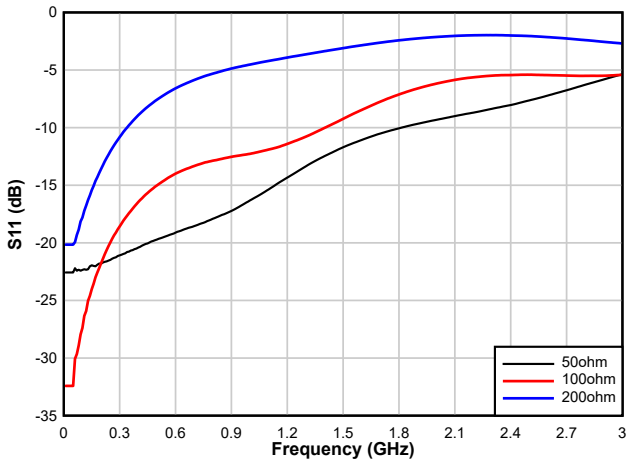



**Figure 7-3. S11 vs Frequency (each normalized to input termination)**


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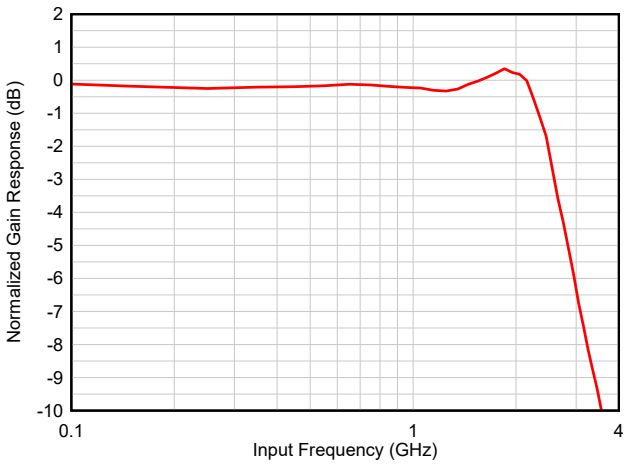



**Figure 7-4. Input Bandwidth Plot**

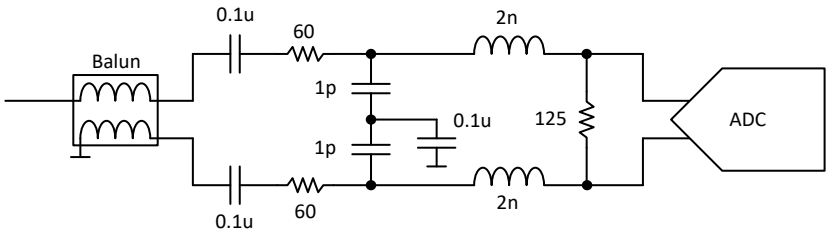
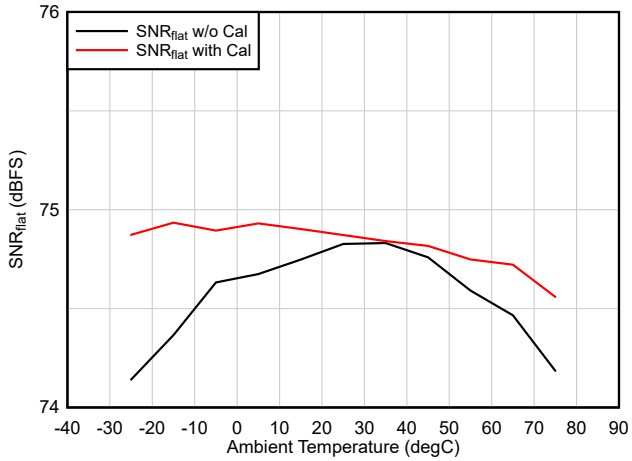



**Figure 7-5. External Matching Network**

#### 7.3.1.2 Background Calibration

The ADC32RF72 uses internal background calibration to maintain a high AC performance over temperature. The calibration is performed periodically and does not require any user control or input signal, and so on. During calibration, small changes to the signal offset are observed (approximately 30LSB). This calibration can be frozen to avoid any disturbance during measurements using SPI writes or GPIO control.




$F_{IN}$ = 100MHz, $A_{IN}$ = -1dBFS, Calibration at 25°C

**Figure 7-6. $SNR_{flat}$ vs Temperature vs Calibration**

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### 7.3.2 ADC Channel Selection and Power Down Modes

There are 4 different ADC channels (Ch0...3) available however channel 0 always has to be enabled. The user can select any of the remaining 3 via the channel enable control shown below in the system parameters. This is a static configuration that needs to be set at power up.

The device supports three different power down modes that can be controlled via GPIO pins or SPI register writes:

- Fast Power Down: individual channel power down with shorter wake up time but higher power consumption. JESD interface stays active.
- Power Down: individual channel power down. JESD interface can be adjusted and power down unused lanes.
- Global Power Down: power down of entire chip for lowest power consumption (enabled via function call).

**Table 7-2. Power Down Modes Comparison**

| Power Down Mode | Wake Up Time | Power Consumption (typ) | Comment |
|---|---|---|---|
| Fast Power Down | ~ 5 us | ~ 2.0W | JESD interface stays active |
| Global Power Down | depends on JESD interface | ~ 0.4W | JESD interface powered down |

The power down modes can be can be programmed using the following parameters:

**Table 7-3. Power Down Modes Programming**

| System Parameter Name | Size | Default | Access | Description |
|---|---|---|---|---|
| ADC_EN_BITMAP | 4 | 3 | R/W | Select two out of the 4 ADCs.<br>3: Channel 0 and 1 are active.<br>5: Channel 0 and 2 are active.<br>9: Channel 0 and 3 are active. |
| ADC_CH_PDN_VAL | 4 | 0 | R/W | Individual ADC channel power down setting. Each ADC gets one bit. If the bit is set, the corresponding channel is powered down. ADC_CH_PDN_SRC_SEL needs to be set to 1 for this setting to take effect.<br>Bit 0: ADC0 power down control.<br>Bit 1: ADC1 power down control.<br>Bit 2: ADC2 power down control.<br>Bit 3: ADC3 power down control. |
| ADC_CH_PDN_SRC_SEL | 1 | 0 | R/W | Select if channel power down signal is coming from a GPIO or SPI.<br>0: Channel power down is from GPIO.<br>1: Channel power down is coming from ADC_CH_PDN_VAL. |
| ADC_CH_PDN_MODE | 1 | 0 | R/W | Select the channel power down mode.<br>0: Normal PDN (least power consumption for each channel).<br>1: Fast PDN (faster power up time but higher power consumption). |


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### 7.3.3 Sampling Clock Input

The clock input has internal 100Ω differential termination with self biasing to VCM = 0.7V, enabling external AC coupling (see Figure 7-7).

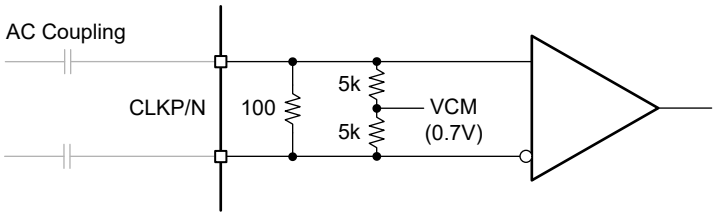



**Figure 7-7. Internal Sampling Clock Circuitry**

The internal sampling clock path is designed for ultra-low residual phase noise contribution. The sampling clock circuitry requires a dedicated low noise power supply for best performance. The internal aperture clock phase noise is also sensitive to clock amplitude. For best performance, the clock amplitude must be larger than 1Vpp.

**Table 7-4. Internal Aperture Clock Noise at 1GHz**

| Frequency Offset (MHz) | Phase Noise (dBc/Hz) | Amplitude Noise (dBc/Hz) |
|---|---|---|
| 0.001 | −130 | −139 |
| 0.01 | −140 | −149 |
| 0.1 | −150 | −155 |
| 1 | −155 | −159 |

The following parameters can be programmed:

**Table 7-5. Clock Register Programming**

| System Parameter Name | Size | Default | Reset | Description |
|---|---|---|---|---|
| ADC_CLK_FREQ_HZ | 33 | 0 | R/W | 33-bit unsigned number that represent the sampling clock frequency in Hz. |

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### 7.3.4 SYSREF

The SYSREF input signal is used for multi-chip synchronization and resets the internal LMFC counter. The device must be armed in anticipation of a SYSREF signal; the device is sensitive to the first SYSREF edge after the device is armed.

The internal SYSREF capture includes a programmable analog delay $t_d$, a SYSREF monitor as well as a programmable digital integer clock cycle delay $z^{-n}$ as shown in Figure 7-8.

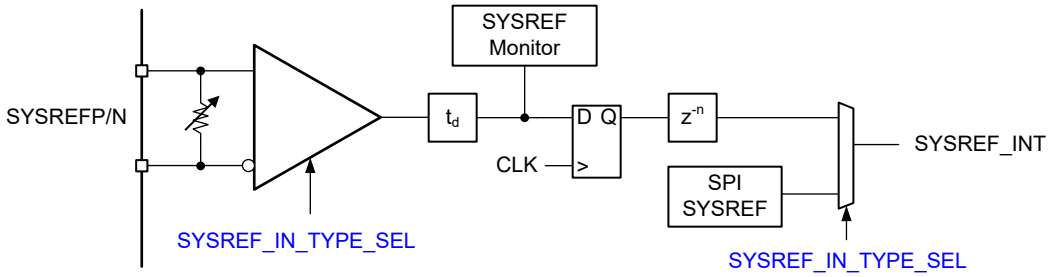



**Figure 7-8. SYSREF Input Internal Path**

The SYSREF input signal can be AC or DC coupled (selected via SPI register option) as shown in Figure 7-9. The SYSREF input has internal 100Ω termination for DC coupling and internal biasing when using AC coupling.

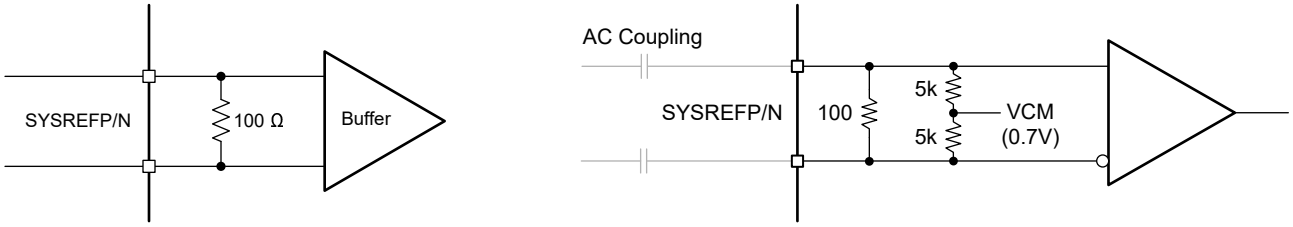



**Figure 7-9. SYSREF Input Circuitry and Edge Alignment (Left Side: DC Coupling, Right Side: AC Coupling)**

The following parameters can be programmed:

**Table 7-6. SYSREF Configuration Programming**

| System Parameter Name | Size | Default | Reset | Description |
|---|---|---|---|---|
| SYSREF_IN_TYPE_SEL | 2 | 0 | R/W | Select input SYSREF type:<br>0: DC coupled LVDS SYSREF input.<br>1: AC coupled SYSREF input.<br>2: not used.<br>3: Internally generated SYSREF using SPI write. |
| SYSREF_DIG_DEL | 8 | 0 | R/W | Digital SYSREF internal delay ($z^{-n}$) in clock cycles of CLK.<br>0...255: Number of device clock cycles delay that is applied to digital SYSREF before use. |


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#### 7.3.4.1 SYSREF Monitor

The SYSREF monitor compares the incoming SYSREF signal to the ADC sampling clock by latching the incoming SYSREF signal with copies of the sampling clock that have an analog delay. The latched outputs are processed internally through the SYSREF processing block and the final output is provided to the user. The latched flop outputs are used to check if there exists enough margin between the CLK and SYSREF rising edges (set up and hold times). If a set up and hold violation is detected, a programmable delay $t_d$ can be used to adjust the SYSREF delay such that there is adequate margin between CLK and SYSREF for SYSREF to be latched properly.

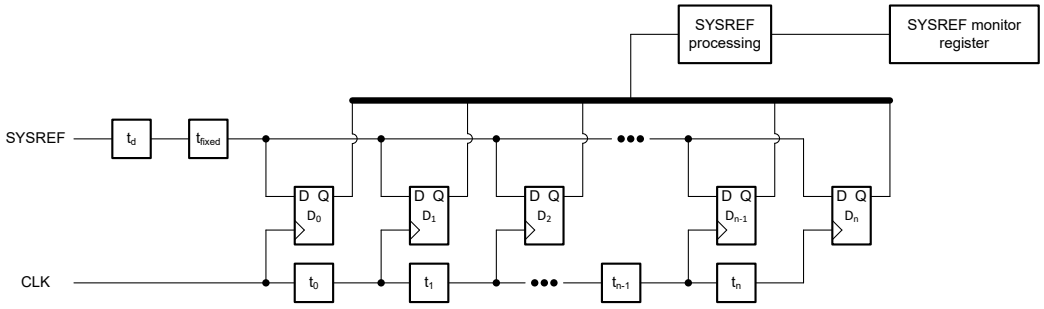



**Figure 7-10. SYSREF Detection Circuitry**

The following parameters can be programmed:

**Table 7-7. SYSREF Configuration Programming**

| System Parameter Name | Size | Default | Access | Description |
|---|---|---|---|---|
| SYSREF_MONITOR_NUM_POLLS | 8 | 1 | R/W | Sets the number of SYSREF rising edges to be detected before SYSREF_MONITOR_OUT is updated. Higher values of SYSREF_MONITOR_NUM_POLLS can be used to gauge the SYSREF edge spread since each flop output is ORed with all of the previous outputs until SYSREF_MONITOR_NUM_POLLS SYSREF rising edges are seen.<br>1...255: Number of SYSREF rising edges to be seen before SYSREF_MONITOR_OUT is updated. |
| SYSREF_MONITOR_TD_COARSE | 4 | 0 | R/W | Sets the number of coarse delays (45ps) in the $t_d$ block. |
| SYSREF_MONITOR_TD_FINE | 4 | 0 | R/W | Sets the fine delay in the $t_d$ block.<br>td_fine = (floor(SYSREF_MONITOR_TD_FINE/2)*15ps) + ((SYSREF_MONITOR_TD_FINE%2)*4ps) |
| SYSREF_MONITOR_OUT | 8 | 0 | R | SYSREF monitor output. Bit 0 corresponds to the earliest CLK edge and bit 7 corresponds to the latest CLK edge.<br>The SYSREF_MONITOR_OUT can only be in one of the following states and can be interpreted as follows:<br>State 0: One or more zeros followed by one or more ones. A rising of SYSREF transition is in the SYSREF monitor window and set up and hold violation is detected. SYSREF_LAT must be delayed until all zeros or all ones are observed.<br>State 1: all zeros. CLK is leading SYSREF_LAT and SYSREF_LAT is latched properly by the next CLK rising edge.<br>State 2: all ones CLK is lagging SYSREF_LAT and SYSREF_LAT is latched properly by the current CLK rising edge. |

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### 7.3.5 Digital Signal Processor (DSP) Features

The device includes several different digital features in the digital signal processing block:

- 12-bit fractional delay with one sampling clock cycle range and a delay step size equal to $1/(2^{12} * t_{CLK})$
- Programmable FIR filter for equalization with up to 96-taps per channel
- Multiple digital down converters (DDCs) supporting decimation factors of /2, /3 and /5 up to /32768
- Additional programmable FIR filter for equalization post decimation

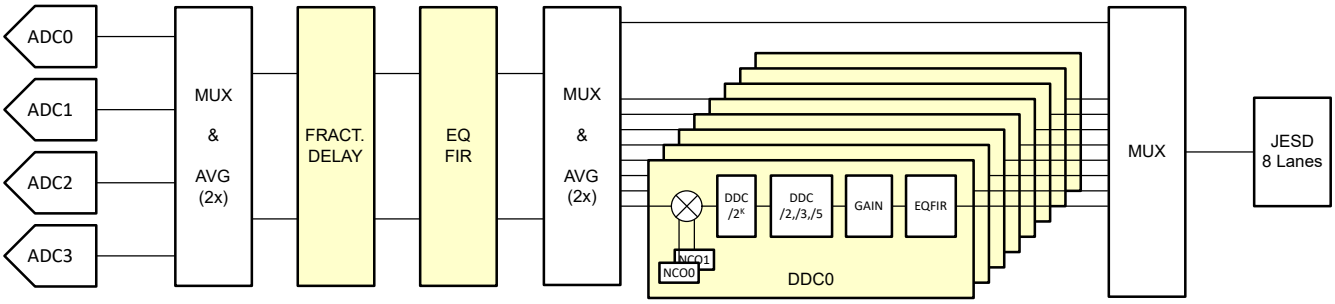



**Figure 7-11. Digital signal processing chain**


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#### 7.3.5.1 DSP Input Mux

There are 4 digital multiplexers at the input of the DSP blocks as shown in Figure 7-12. The bus is referred to adc_out[3:0] where each index refers to the unique output stream of a particular ADC, meaning, the ADC0 output is adc_out[0] and so on. The output of each DSP_IN mux corresponds to a single DSP input data stream for the DSP blocks. The aggregate set of DSP input data streams is referred to as dsp_in[3:0]. dsp_in[0] corresponds to the 0th DSP input data stream. Each DSP input data stream can be sourced from one of the following:

- One of two adc_out streams (adc_out[0] and any one of the others). This is denoted by C(2,1).
- The average of two adc_out streams.

**Note**

The nomenclature C($n$,$k$) represents the possible combinations of choosing $k$ items from a set containing $n$ distinct items.
For example, assuming we have a set adc_out={adc0,adc1,adc2,adc3}, there are 6 distinct ways to select two items from the set which can be seen here: C(adc_out,2)={{ADC0,ADC1},{ADC0,ADC2},{ADC0,ADC3},{ADC1,ADC2},{ADC1,ADC3},{ADC2,ADC3}}

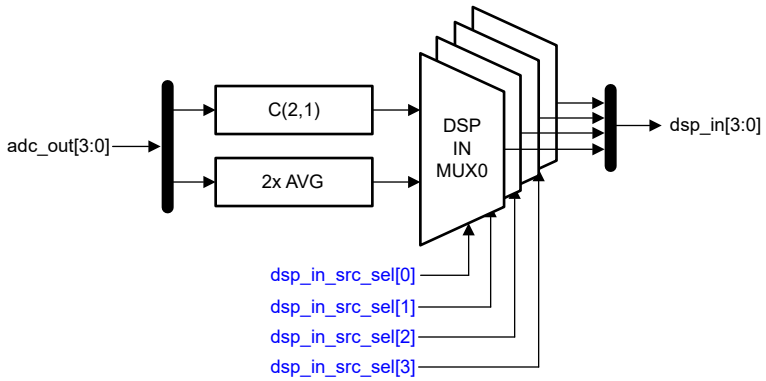



**Figure 7-12. DSP Input Mux Overview**

The following parameters can be programmed:

**Table 7-8. DSP Input Mux Configuration Programming (x = 0,1,2,3)**

| System Parameter Name | Size | Default | Access | Description |
|---|---|---|---|---|
| DSP_IN_SRC_SEL{x} | 4 | 0,1,2,3 | R/W | Select the input data source for the dsp_in[0..3] input stream to the DSP blocks.<br>0: ADC0 data.<br>1: ADC1 data.<br>2: ADC2 data.<br>3: ADC3 data.<br>4: 2x average of ADC0 and ADC1.<br>5: 2x average of ADC0 and ADC2.<br>6: 2x average of ADC0 and ADC3.<br>7: 2x average of ADC1 and ADC2.<br>8: 2x average of ADC1 and ADC3.<br>9: 2x average of ADC2 and ADC3.<br>Others: not used |

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### 7.3.5.2 Fractional Delay

The device includes an optional programmable 12-bit fractional digital delay after the DSP input mux (see Figure 7-13). There are two independent digital fractional delay blocks - FDF0 and FDF1. Each FDF block is connected to two input streams (dsp_in[1:0] or dsp_in[3:2]) where each input stream has a programmable fractional delay value, $t_{d00}$ and $t_{d01}$ for dsp_in[1:0] and $t_{d10}$ and $t_{d11}$ for dsp_in[3:2]. The FDF blocks output a total of four data streams (fdf_out[3:0]) where each output stream corresponds to a distinct fractionally delayed input stream.

The fractional delay is a *true time delay* implementation with a linear phase across frequencies. The fractional delay calculates to:

Fractional Delay [sampling clock period] = Delay / 4096x $T_S$ (sampling period).

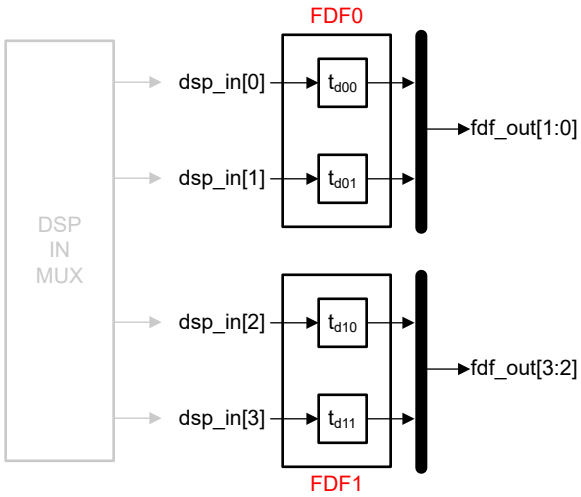



**Figure 7-13. Fractional Delay Feature**

As an example, a setting of 2048 equals ½ a clock cycle delay as shown in Figure 7-14. The magnitude error is less than −80dB (vs desired delay).

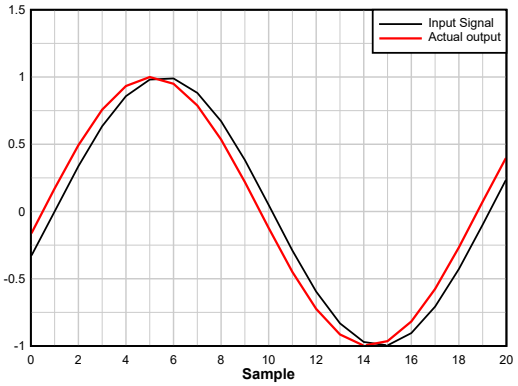



**Figure 7-14. Fractional delay = ½ clock cycle (delay setting = 2048)**

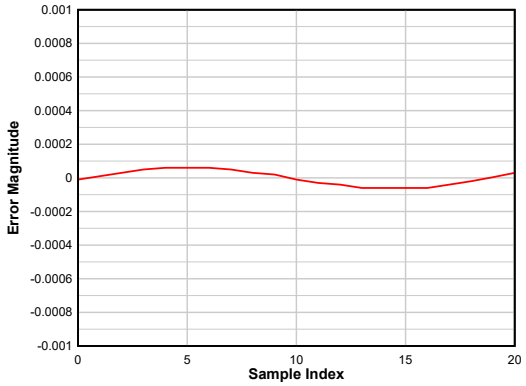



**Figure 7-15. Error magnitude (desired vs actual waveform)**


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The fractional delay is configured via SPI register writes and the programmed delay is internally translated into filter coefficients. The filter response is shown in Figure 7-16 and Figure 7-17. The passband is approximately 85% of the Nyquist zone. Reprogramming the fractional delay can take up to 2µs to update the filter coefficients.

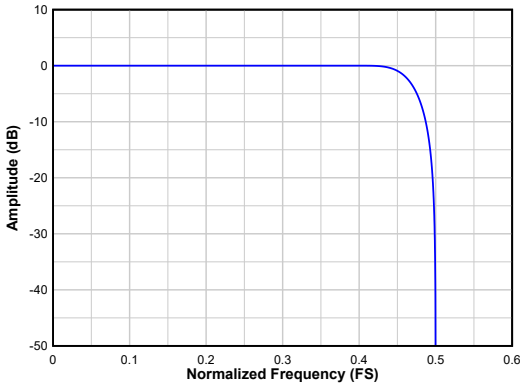



**Figure 7-16. Filter response of the fractional delay FIR**

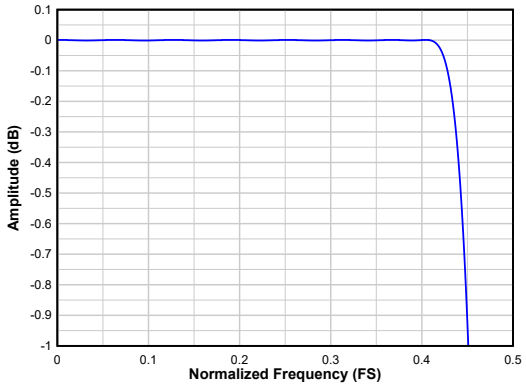



**Figure 7-17. Filter response of the fractional delay FIR (zoom)**

The fractional delay can be can be programmed using the following parameters:

**Table 7-9. Fractional Delay Configuration Programming**

| System Parameter Name | Size | Default | Access | Description |
|---|---|---|---|---|
| FDF0_DELAY_VAL_0_LSB | 8 | 0 | R/W | Bits [7:0] of the fractional delay value for 0th input data stream to FDF0. |
| FDF0_DELAY_VAL_0_MSB | 4 | 0 | R/W | Bits [11:8] of the fractional delay value for 0th input data stream to FDF0. |
| FDF0_DELAY_VAL_1_LSB | 8 | 0 | R/W | Bits [7:0] of the fractional delay value for 1st input data stream to FDF0. |
| FDF0_DELAY_VAL_1_MSB | 4 | 0 | R/W | Bits [11:8] of the fractional delay value for 1st input data stream to FDF0. |
| FDF1_DELAY_VAL_0_LSB | 8 | 0 | R/W | Bits [7:0] of the fractional delay value for 0th input data stream to FDF1. |
| FDF1_DELAY_VAL_0_MSB | 4 | 0 | R/W | Bits [11:8] of the fractional delay value for 0th input data stream to FDF1. |
| FDF1_DELAY_VAL_1_LSB | 8 | 0 | R/W | Bits [7:0] of the fractional delay value for 1st input data stream to FDF1. |
| FDF1_DELAY_VAL_1_MSB | 4 | 0 | R/W | Bits [11:8] of the fractional delay value for 1st input data stream to FDF1. |

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#### 7.3.5.3 Programmable FIR Filter for Equalization

The ADC32RF7x includes an integrated programmable FIR filter block referred to as an equalizer (EQ). As illustrated in Figure 7-18, there are two EQ blocks (EQ0 and EQ1) which are located at the output of the fractional delay filters (FDF0/1). Each EQ block can source the input data stream from either dsp_in directly or from the preceding FDF block. There are a total of four output data streams (eq_out[3:0]) where each output stream corresponds to a distinct filtered input stream.

Each of the two equalizers (EQ0/EQ1) include up to 192-taps (16-bit) shared across two input streams.

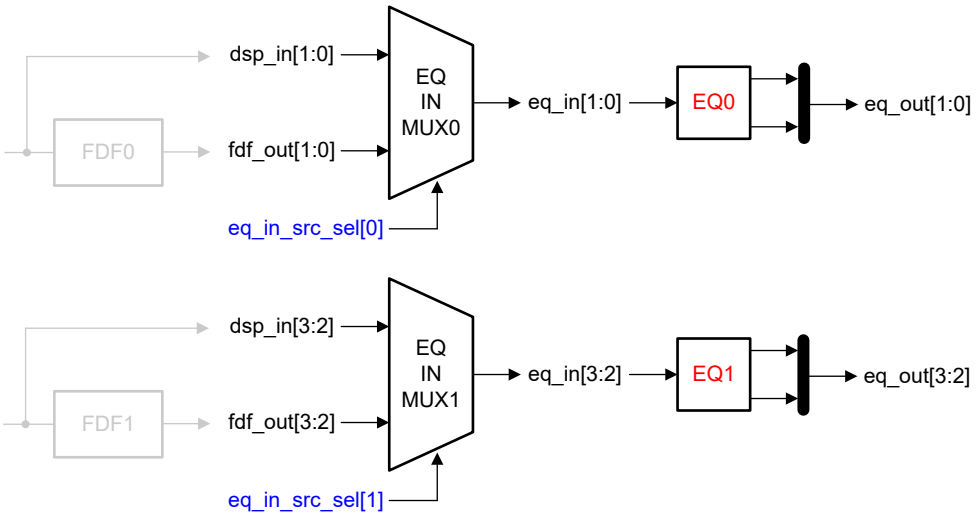



**Figure 7-18. FIR Equalizer Configurations**

Each EQ supports several different configurations with up to 192-taps per EQFIR as shown in Figure 7-19.

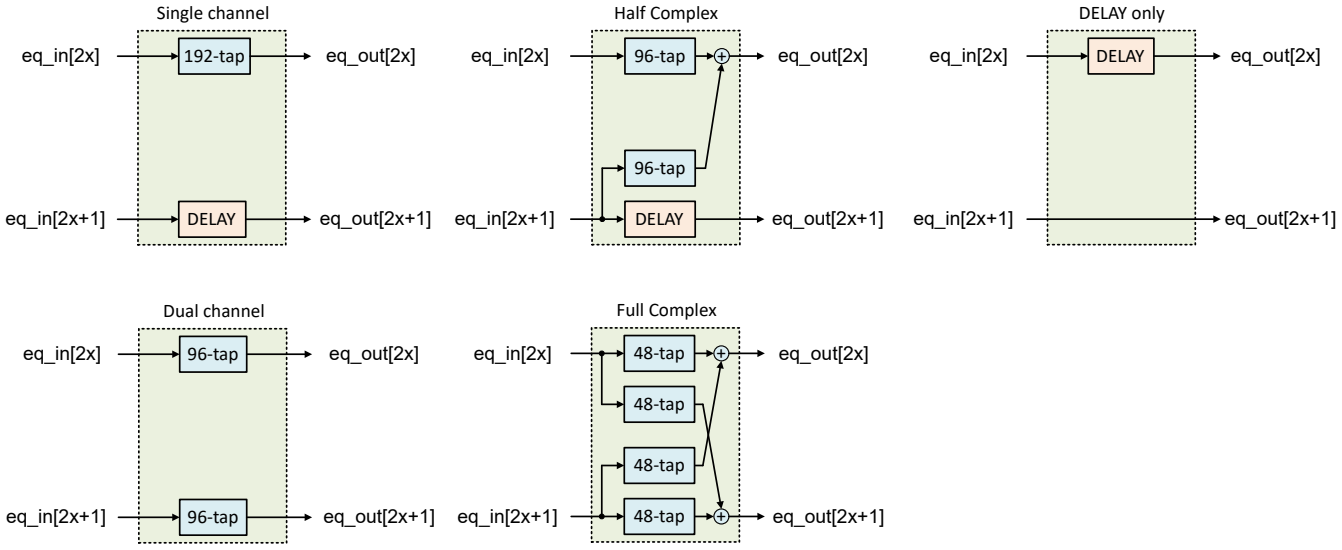



**Figure 7-19. FIR Equalizer Configurations for EQ0 (x=0) and EQ1 (x=1)**


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The power consumption scales linearly with sampling rate and with # of taps used. Unused taps can be set to 0.

The digital equalizer can be can be programmed using the following parameters:

**Table 7-10. EQ{x} Configuration Programming (x= 0,1)**

| System Parameter Name | Size | Default | Access | Description |
|---|---|---|---|---|
| EQ{x}_IN_SRC_SEL | 1 | 0 | R/W | Select EQ{x} input data source.<br>0: EQ{x} input from DSP_IN[2x+1, 2x].<br>1: EQ{x} input from FDF_OUT[2x+1, 2x]. |
| EQ{x}_MODE_SEL | 3 | 0 | R/W | Select EQ{x} mode.<br>0: Single channel mode.<br>1: Dual channel mode.<br>2: Half complex mode.<br>3: Full complex mode.<br>4: Delay only mode. |
| EQ{x}_DEL_VAL | 8 | 0 | R/W | EQ{x} delay value. The effect of this setting is dependent on the EQ{x} mode.<br>0...255: Number of device clock cycles delay that is applied when EQ{x} is in a mode with a programmable delay. |
| EQ{x}_NUM_TAPS | 8 | 0 | R/W | Number of taps to be used by EQ{x} in a given mode. Can be any value when in single channel mode. Has to be even in dual channel mode and half complex mode. Has to be divisible by four in full complex mode.<br>1...192: Number of taps to be used by EQ{x}. |
| EQ{x}_TAPS | 3072 | 0 | R/W | Set the 192 taps of the EQ{x} block.<br>Single channel mode: Up to 192 taps are applied to eq_input[2x].<br>Dual channel mode: Up to 96 taps per eq_input. First 96 taps apply to eq_input[2x]. Second 96 taps apply to eq_input[2x+1].<br>Half complex mode: Up to 96 taps per eq_input. First 96 taps apply to eq_input[2x]. Second 96 taps apply to eq_input[2x+1].<br>Full complex mode: Up to 96 taps per eq_input. First 96 taps apply to eq_input[2x]; the first 48 of those taps apply to eq_output[2x]. Second 96 taps apply to eq_input[2x+1]; the first 48 of those taps apply to eq_output[2x]. |

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#### 7.3.5.4 DSP Output Mux

There are several different multiplexers available at the output of the DSP prior to the DDCs.

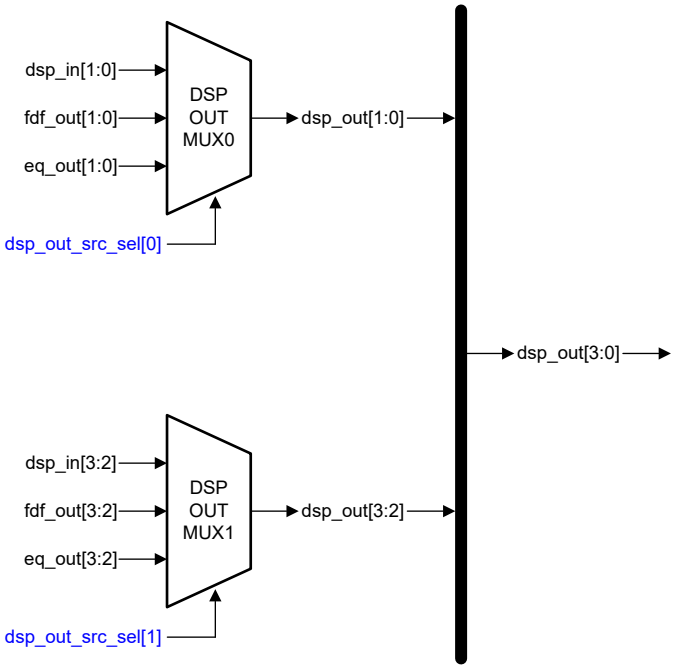



**Figure 7-20. DSP Output Mux**

The following parameters can be programmed:

**Table 7-11. Input Selection to the DDC Programming (x = 0 or 1)**

| System Parameter Name | Size | Default | Access | Description |
|---|---|---|---|---|
| DSP_OUT_SRC_SEL{x} | 2 | 0 | R/W | Select the output data source for DSP_OUT_MUX{x} from the DSP blocks.<br>0: dsp_in[2x+1,2x] as output of DSP_OUT_MUX{x}.<br>1: fdf_out[2x+1,2x] as output of DSP_OUT_MUX{x}.<br>2: eq_out[2x+1,2x] as output of DSP_OUT_MUX{x}. |


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#### 7.3.5.5 Digital Down Converter (DDC)

The ADC32RF7x includes 8 digital down converters (DDCs) with independent NCOs. Each DDC supports base decimation factors of 2, 3 or 5 with decimation ratios from /2 to /32768 (/3 .. /96 and /5... /80). The maximum decimation setting allowed is dependent on sampling rate, number of DDCs, sample repeat factor (only with factors of 2) and the JESD output resolution 'N' due to the 4Gbps minimum SERDES lane rate required by the device. Additionally, the final /2 stage supports programmable coefficients.

A crossbar mux is used to connect any DDC input to any ADC or the output of the 2x averaging block. The ADC32RF7x DDCs can be configured to have independent decimation factors (binary factors only).

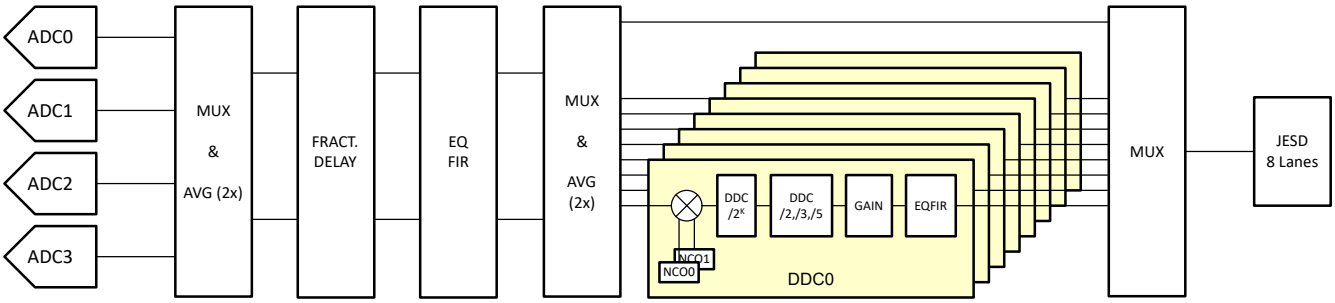



**Figure 7-21. Multi-Band Decimation Filter**

Real and complex decimation is supported and the passband is approximately 80% of the decimated bandwidth.

**Table 7-12. Complex Decimation Setting vs Output Bandwidth**

| Decimation Factor | Complex Output Bandwidth per DDC | Real Output Bandwidth per DDC |
|---|---|---|
| N | 0.8x $F_S$ / N | 0.8x $F_S$ / (2N) |

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#### 7.3.5.5.1 Decimation Filter Input

There are several different multiplexers available at the input of each of the 8x DDC as shown in Figure 7-22. Each DDC has a DDC_REAL_DATA_MUX and DDC_INPUT_DATA_TYPE_MUX. The DDC input data type is based on the ddc_mode setting.

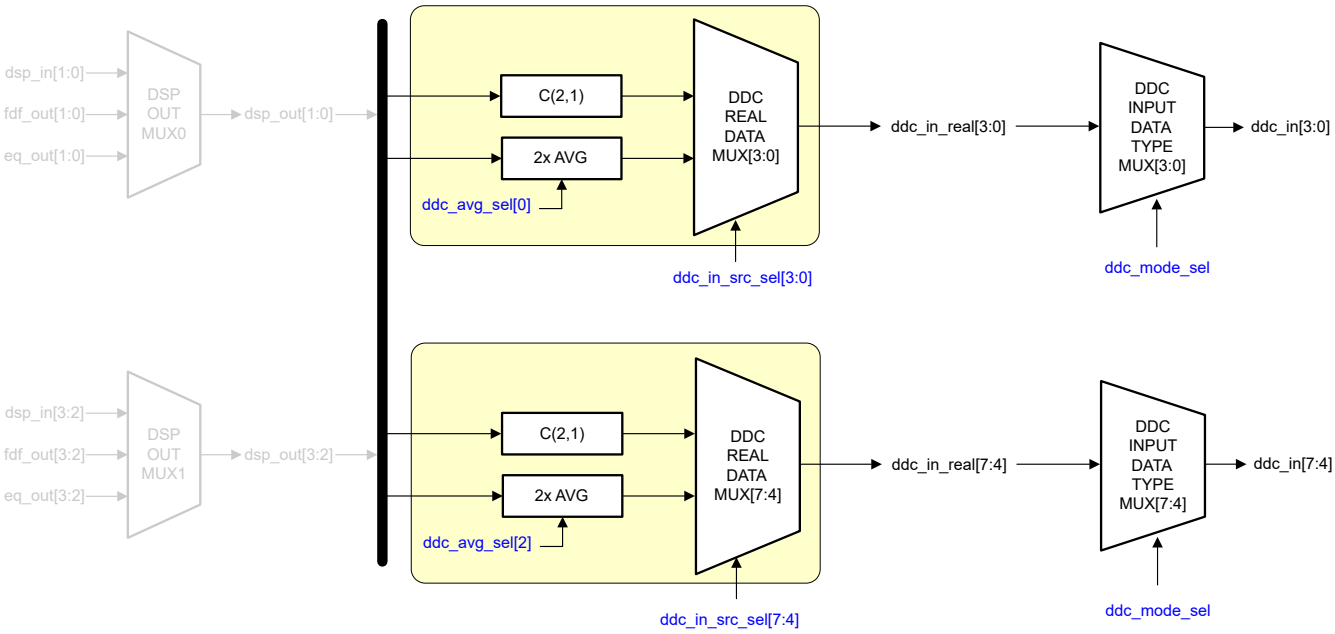



**Figure 7-22. DDC Input Data Muxing**

The following parameters can be programmed:

**Table 7-13. Input Selection to the DDC Programming**

| System Parameter Name | Size | Default | Access | Description |
|---|---|---|---|---|
| DDC_AVG__SEL{0,2} | 3 | .. | R/W | Select the two data streams to be averaged in the 2x AVG as a shared input for the multiplexers DDC_REAL_DATA_MUX[3:0]/[7:4].<br>0: Average of dsp_out[0] and dsp_out[1].<br>1: Average of dsp_out[0] and dsp_out[2].<br>2: Average of dsp_out[0] and dsp_out[3].<br>3: Average of dsp_out[1] and dsp_out[2].<br>4: Average of dsp_out[1] and dsp_out[3].<br>5: Average of dsp_out[2] and dsp_out[3]. |
| DDC_IN_SRC_SEL{0..7} | 5 | .. | R/W | Select the data source for DDC{0..7}. All DDC data must come exclusively from only one of the multiplexers.<br>0: dsp_out[0] as real input to the DDC.<br>1: dsp_out[1] as real input to the DDC.<br>2: dsp_out[2] as real input to the DDC.<br>3: dsp_out[3] as real input to the DDC.<br>4: Output of the first 2x AVG block (DDC_AVG_SEL_0/2) block as real input to the DDC.<br>5: Output of the second 2x AVG block (DDC_AVG_SEL_1/3) block as real input to the DDC.<br>6: Average of dsp_out[0], dsp_out[1], dsp_out[2], and dsp_out[3] as real input to the DDC. |


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**Table 7-13. Input Selection to the DDC Programming (continued)**

| System Parameter Name | Size | Default | Access | Description |
|---|---|---|---|---|
| DDC_EN_CTRL | 8 | 0 | R/W | Individual DDC enable control. Each bit corresponds to one DDC where the LSB corresponds to DDC0. If the enable bit is set then the corresponding DDC is enabled.<br>Bit 0: DDC0 power down control.<br>Bit 1: DDC1 power down control.<br>Bit 2: DDC2 power down control.<br>Bit 3: DDC3 power down control.<br>Bit 4: DDC4 power down control.<br>Bit 5: DDC5 power down control.<br>Bit 6: DDC6 power down control.<br>Bit 7: DDC7 power down control. |
| DDC_MODE_SEL | 3 | 0 | R/W | Select the DDC mode which is shared across all DDCs.<br>0: Pass-through mode; The particular DDC is unused<br>1: Real input (from the DDC_REAL_DATA_MUX) given to the DDCs is low pass filtered and down sampled by the decimation factor.<br>2: Real input (from the DDC_REAL_DATA_MUX) given to the DDCs is mixed with an NCO to produce a complex output. The complex output is low pass filtered and down sampled by the decimation factor. |

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#### *7.3.5.5.2 Decimation Modes*

There are 2 different decimation modes supported and all 8x DDCs must be configured to the same mode:

- **Real decimation**: The real input is low pass filtered and the filter output is down sampled by the decimation factor (M). The output of the DDC block in this mode is a real signal and detailed DDC chain is shown in Figure 7-23.
- **Complex decimation with real input**: The DDC is given a real input that is mixed with an NCO to produce a complex output. The complex output is low pass filtered and down sampled by the decimation factor (M). The output of the DDC block in this mode is a complex signal and detailed DDC chain is shown in Figure 7-25.

Each DDC has an enable control signal. If the DDC is disabled, the output is zero. The following blocks are part of the DDC signal chain:

- **Decimation**: The possible decimation factors are B x $2^N$ where the base factor B can be 1, 3 or 5 and N can be a maximum of 15 for B = 1, 5 for B = 3 and 4 for B = 5.

  When the base factor is 3 or 5, all the DDCs must share the same decimation factor setting. However, when the base factor is 1 (decimations factors that are powers of 2), having an independent decimation factors per DDC is possible since each DDC has a samples repeater block. When each DDC is configured to a different decimation factor, the samples repeater for each DDC is adjusted so that all the DDC outputs are rate matched to highest data rate DDC. For example, if two DDCs are active and one is configured in decimation by 4 and the other in decimation by 16, the DDC configured for decimation by 16 automatically gets rate matched to the decimation by 4 rate by repeating the samples by a factor of 4. Upon successful configuration, the repeat factor can be readback for each DDC.

  **Note**

  Independent decimation factors are not supported when any DDC is configured for decimation by 2. When decimation by 2 is used all other DDCs must be also be set to by 2.

  **Repeat Factor**: The repeat factor is adjusted automatically for each DDC in cases where the effective JESD line rate is below the lower threshold of 4Gbps. The repeat factor block is not available with base factors of 3 and 5.
- **DDC_PFIR**: The ADC32RF72 has an integrated programmable FIR filter block in the decimation chain where the last stage filter is completely programmable. This feature is only available with decimation factors that are powers of 2 (B = 1). The block is referred to as the DDC_PFIR. Each DDC_PFIR has up to 96 total taps (across both inputs in complex decimation) with 17-bit resolution.
- **DDC coarse gain (G)**: The fixed digital gain can be applied to each DDC path where the gain G is an element of {0dB, 3dB, 6dB} and controllable for each DDC through the ddc_coarse_gain[7:0] signal.
- **DDC_EQ**: The DDC_EQ supports all the same modes the as the Digital DSP EQ.

  **Note**

  This EQ is not available for decimation factors of 2 and 3.
- **DDC_COMPLEX_GAIN**: Each DDC has a programmable complex gain. In real decimation mode, only the real part of the gain is applied. The gain is in steps of 0.1dB from 0dB to 6dB; an independent gain setting is available for the real and imaginary parts.

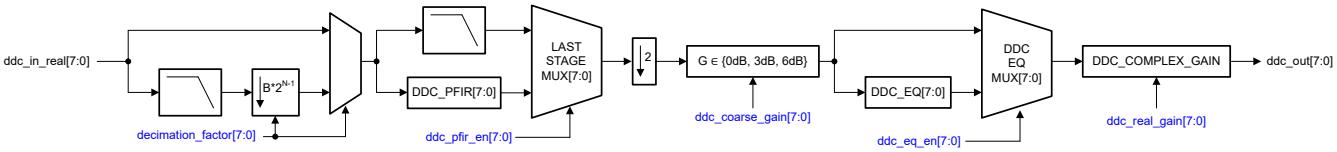



**Figure 7-23. Real Decimation Signal Chain (decimation factors that are powers of 2 (B = 1))**


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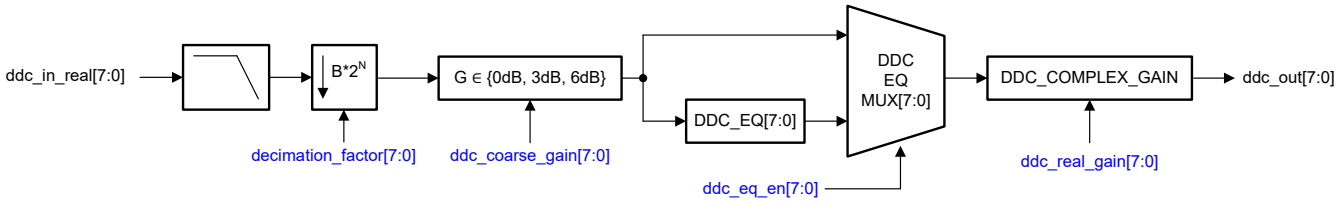



**Figure 7-24. Real Decimation Signal Chain (decimation factors of 3 and 5 (B = 3, 5)**

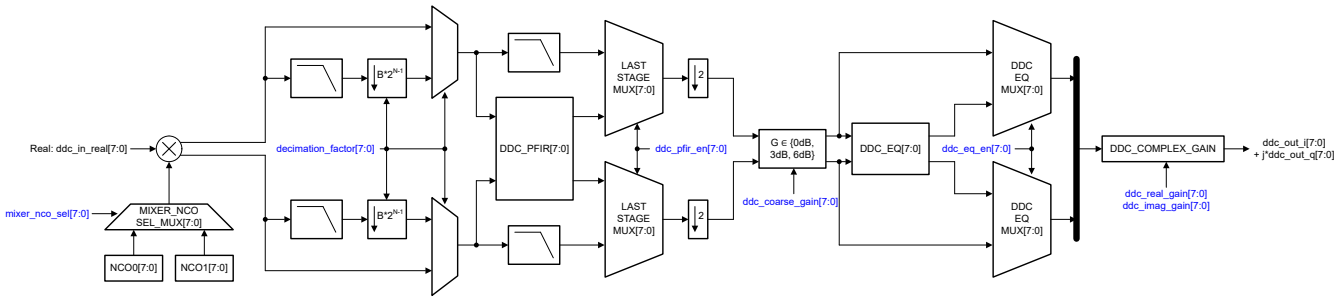



**Figure 7-25. Complex Decimation Signal Chain (decimation factors of 2 (B = 1)**

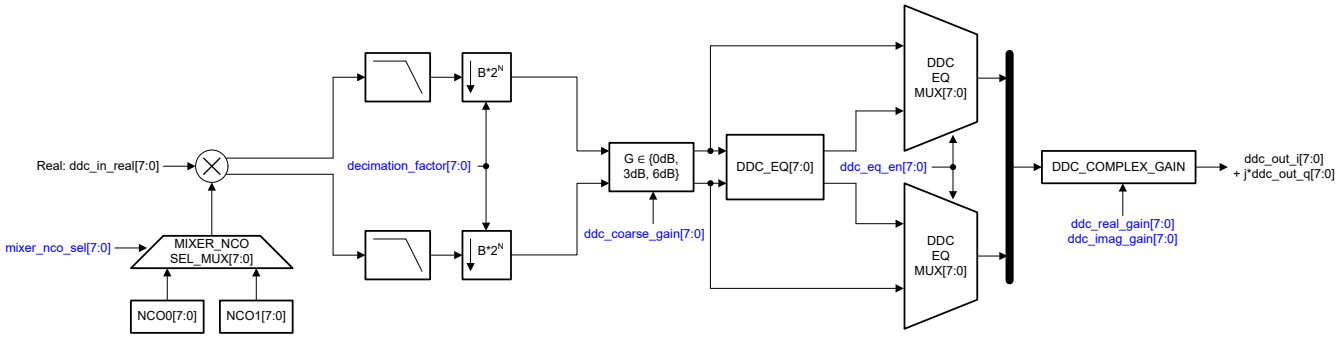



**Figure 7-26. Complex Decimation Signal Chain (decimation factors of 3 and 5 (B = 3, 5)**

The following parameters can be programmed:

**Table 7-14. Input Selection to the DDC Programming**

| Function Name | Size | Default | Access | Description |
|---|---|---|---|---|
| DDC{0..7}_DECIMATION_FACTOR_LSB | 8 | 1 | R/W | Set bits[15:0] of the 16-bit decimation factor for the DDC. Possible decimation factors are: [2, 3, 4, 5, 6, 8, 10, 12, 16, 20, 24, 32, 40, 48, 64, 80, 96, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, 32768] |
| DDC{0..7}_DECIMATION_FACTOR_MSB | 8 | 0 | R/W | |
| DDC{0..7}_REPEAT_FACTOR_LSB | 8 | 1 | R | Bits[13:0] of the 14-bit repeat factor for the DDC. |
| DDC{0..7}_REPEAT_FACTOR_MSB | 6 | 0 | R | |
| DDC{0..7}_PFIR_EN | 1 | 0 | R/W | Control the DDC_PFIR enable.<br>0: DDC_PFIR is disabled and a fixed decimation filter is used as the last stage filter.<br>1: DDC_PFIR is enabled and a programmable decimation filter is used as the last stage filter. |
| DDC{0..7}_PFIR_MODE_SEL | 1 | 0 | R/W | Select the DDC_PFIR mode.<br>0: Single channel mode.<br>1: Dual channel mode. |
| DDC{0..7}_PFIR_NUM_TAPS | 7 | 0 | R/W | Number of taps to be used by DDC_PFIR in a given mode. Can be any value when in single channel mode. Has to be even in dual channel mode.<br>1...96: Number of taps to be used by the DDC_PFIR. |

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**Table 7-14. Input Selection to the DDC Programming (continued)**

| Function Name | Size | Default | Access | Description |
|---|---|---|---|---|
| DDC{0..7}_PFIR_TAPS | 3072 | 0 | R/W | Set the 96 taps of the DDC_PFIR block. Only 17 bits are written.<br>Single channel mode: Up to 96 taps are applied to ddc_pfir_input[0].<br>Dual channel mode: Up to 48 taps per ddc_pfir_input. First 48 taps apply to ddc_pfir_input[0]. Second 48 taps apply to ddc_pfir_input[1]. |
| DDC{0..7}_EQ_EN | 1 | 0 | R/W | Control the DDC_EQ enable.<br>0: DDC_EQ is disabled and bypassed.<br>1: DDC_EQ is enabled and the DDC_EQ filter is applied to the DDC output. |
| DDC{0..7}_EQ_MODE_SEL | 3 | 0 | R/W | Select the DDC_EQ mode.<br>0: Single channel mode.<br>1: Dual channel mode.<br>2: Half complex mode.<br>3: Full complex mode.<br>4: Delay only mode. |
| DDC{0..7}_EQ_DEL_VAL | 7 | 0 | R/W | DDC_EQ delay value. The effect of this setting is dependent on the DDC_EQ mode.<br>0...127: Number of device clock cycles delay that is applied when DDC_EQ is in a mode with a programmable delay. |
| DDC{0..7}_EQ_NUM_TAPS | 7 | 0 | R/W | Number of taps to be used by DDC_EQ in a given mode. Can be any value when in single channel mode. Has to be even in dual channel mode and half complex mode. Has to be divisible by four in full complex mode.<br>1...96: Number of taps to be used by DDC_EQ. |
| DDC{0..7}_EQ_TAPS | 1536 | 0 | R/W | Set the 96 taps of the DDC_EQ block.<br>Single channel mode: Up to 96 taps are applied to ddc_eq_input[0].<br>Dual channel mode: Up to 48 taps per ddc_eq_input. First 48 taps apply to ddc_eq_input[0]. Second 48 taps apply to ddc_eq_input[1].<br>Half complex mode: Up to 48 taps per ddc_eq_input. First 48 taps apply to ddc_eq_input[0]. Second 48 taps apply to ddc_eq_input[1].<br>Full complex mode: Up to 48 taps per ddc_eq_input. First 48 taps apply to ddc_eq_input[0]; the first 24 of those taps apply to ddc_eq_output[0]. Second 48 taps apply to ddc_eq_input[1]; the first 24 of those taps apply to ddc_eq_output[0]. |
| DDC{0..7}_COARSE_GAIN | 3 | 0 | R/W | Set a fixed digital gain in the DDC data path before the DDC_EQ.<br>0: 0dB digital gain.<br>3: 3dB digital gain.<br>6: 6dB digital gain (useful when using complex decimation). |
| DDC{0..7}_REAL_GAIN | 6 | 0 | R/W | Real part of the complex gain applied to the DDC output. The gain is in 0.1dB steps starting from to 0dB to 6dB.<br>0..60: Effective gain is DDC_REAL_GAIN*0.1dB |
| DDC{0..7}_IMAG_GAIN | 6 | 0 | R/W | Imaginary part of the complex gain applied to the DDC output (used in complex decimation modes). The gain is in 0.1dB steps starting from to 0dB to 6dB.<br>0..60: Effective imaginary gain is DDC_IMAG_GAIN*0.1dB |


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#### 7.3.5.5.3 Decimation Filter Response

This section provides the different decimation filter responses with a normalized ADC sampling rate. The complex filter pass band is approximately 80% (−0.1dB) of the decimated bandwidth with a minimum of 85dB stop band rejection.

The decimation filter responses are normalized to the ADC sampling clock frequency $F_S$. One example (decimation by 4) is illustrated in Figure 7-28 and Figure 7-29. The filter responses for all other decimation filter plots are available in the product folder.

The decimation filter plots are interpreted as follows: Each figure contains the filter pass-band, transition bands and alias or stop-bands as shown in Figure 7-27. The x-axis shows the offset frequency (after the NCO frequency shift) normalized to the ADC sampling rate $F_S$.

For example, in the divide-by-4 complex setup, the output data rate is $F_S$ / 4 complex with a Nyquist zone of $F_S$ / 8 or 0.125 × $F_S$. The transition band (colored in blue) is centered around 0.125 × $F_S$ and the alias transition band is centered at 0.375 × $F_S$. The stop-bands (colored in red), which alias on top of the pass-band, are centered at 0.25 × $F_S$ and 0.5 × $F_S$. The stop-band attenuation is greater than 85dB.

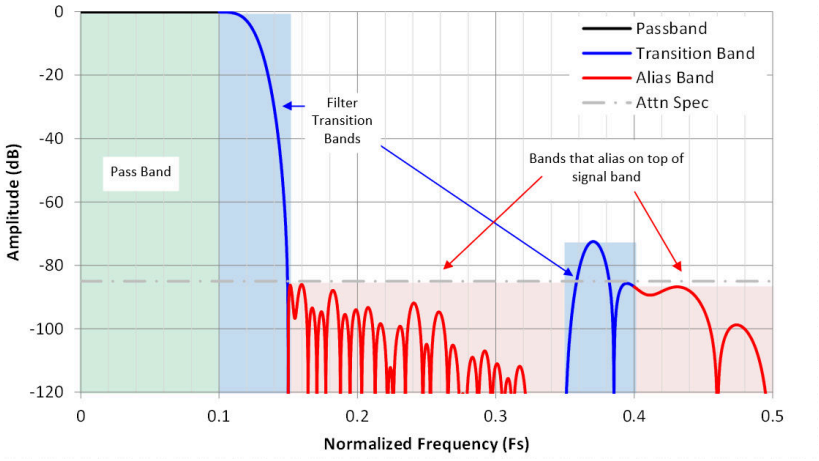



**Figure 7-27. Interpretation of the Decimation Filter Plots**

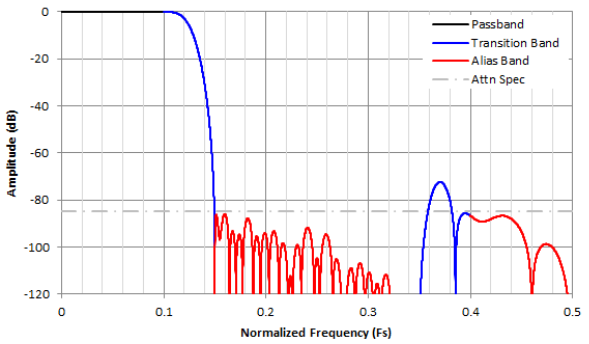



**Figure 7-28. Decimation by 4 Filter Response**

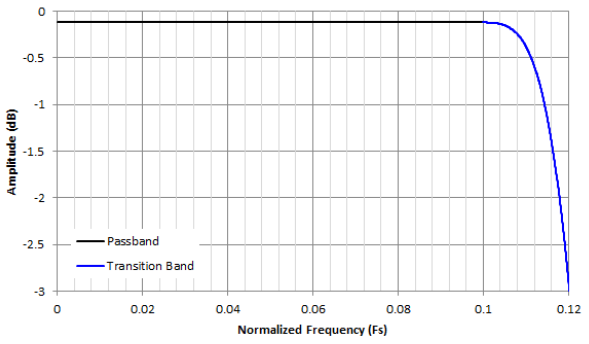



**Figure 7-29. Decimation by 4 Passband Ripple Response**

#### *7.3.5.5.4 Numerically Controlled Oscillator (NCO)*

FS = ADC sampling rate (MSPS)

Each digital down-converter (DDC) uses a 48-bit numerically controlled oscillator (NCO) to fine tune the frequency placement prior to the digital filtering as shown in Figure 7-30. The NCO frequency range is $-F_S/2$ to $F_S/2$ and is dictated by a frequency control word (FCW) and phase offset.

There are two different NCO frequencies for each DDC. The desired NCO frequency is programmed via SPI and can be selected using SPI or the GPIO pins. When using the GPIO pins for NCO frequency control, frequency hopping can be achieved in less than 1µs.

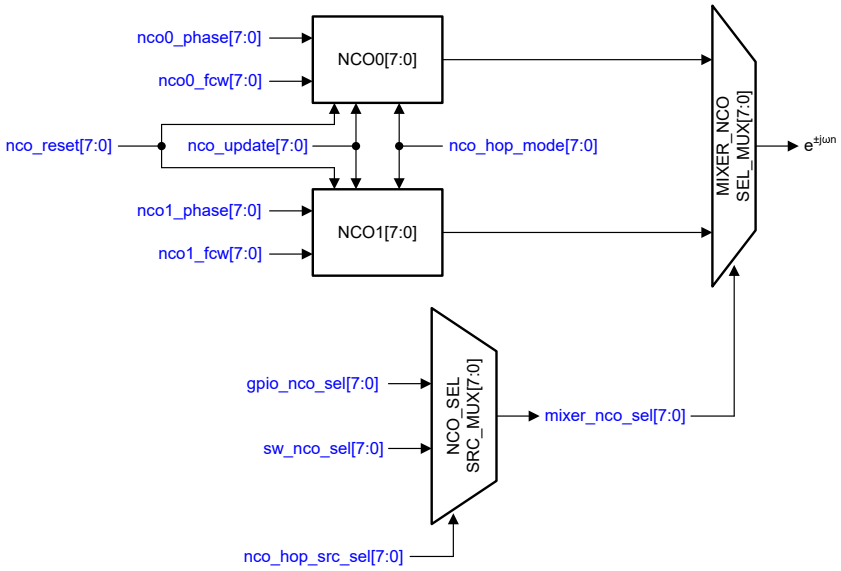



**Figure 7-30. NCO block diagram with all control signals**

Infinite Phase Coherent NCO: With a phase coherent NCO, all frequencies are synchronized to a single event using SYSREF. This enables an infinite amount of frequency hops without the need to reset the NCO as phase coherency is maintained between frequency hops. This is illustrated in Figure 7-31 (right). When returning to the original frequency $f_1$, the NCO phase appears as if the NCO had never changed frequencies.

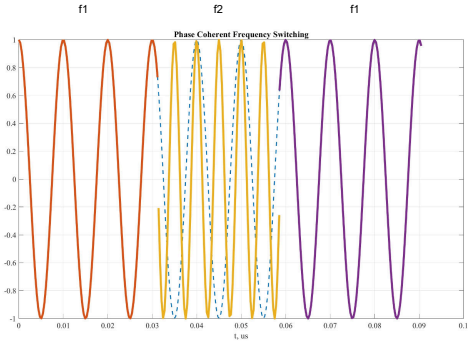



**Figure 7-31. Infinite Phase Coherent NCO Frequency Switching**


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The oscillator generates a complex exponential sequence of: $e^{j\omega n}$ (default) or $e^{-j\omega n}$

where: frequency (ω) is specified as a signed number by the 48-bit FCW

The complex exponential sequence is multiplied with the real input from the ADC to mix the desired carrier to a frequency equal to $f_{IN} + f_{NCO}$. The NCO frequency can be tuned from $-F_S/2$ to $+F_S/2$ and is processed as a signed, 2s complement number.

The FCW setting is set by the 48-bit register value given and calculated as:

$$\text{NCO frequency (0 to + } F_S/2\text{): NCO} = f_{NCO} \times 2^{48} / F_S \quad (3)$$

$$\text{NCO frequency (-}F_S/2\text{ to 0): NCO} = (f_{NCO} + F_S) \times 2^{48} / F_S \quad (4)$$

where:

- NCO = FCW (decimal value)
- $f_{NCO}$ = Desired NCO frequency (MHz)
- $F_S$ = ADC sampling rate (MSPS)

#### *7.3.5.5.4.1 NCO Update*

The NCO FCW and phase can be updated dynamically. Additionally, the NCO update signal can be masked for each DDC (nco_update_mask[7:0]). The NCO update signal can be sourced from software (sw_nco_sync), or by leaking the internal SYSREF (SYSREF_INT) to update the NCOs. Updating the NCO FCW and phase is a two step process:

1. The new FCW and phase must be written
2. An nco_update signal must be issued to apply the new NCO settings

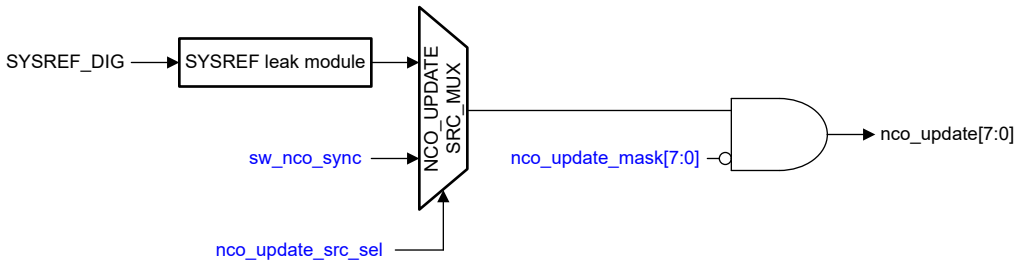



**Figure 7-32. NCO Update With All Control Signals**

The nco_update_mask[7:0] is used to mask the nco_update signal from specific DDCs, thereby; allowing the update of the NCO for only a subset of the DDCs. When the NCO update signal is sourced from software (sw_nco_sync), the nco_update_mask for DDC [x] and DDC[x+1], where $x \in \{0,2,4,6\}$, must be configured identically as the sw_nco_sync signal is shared for DDC [x] and DDC[x+1].

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#### 7.3.5.5.4.2 NCO RESET

The NCO phase accumulator can be reset for each NCO through an nco_reset signal. The NCO reset can be masked for each DDC (nco_reset_mask[7:0]). The NCO reset signal can be sourced from software (sw_nco_sync) or the NCOs can be armed through a GPIO to be reset on the next SYSREF edge.

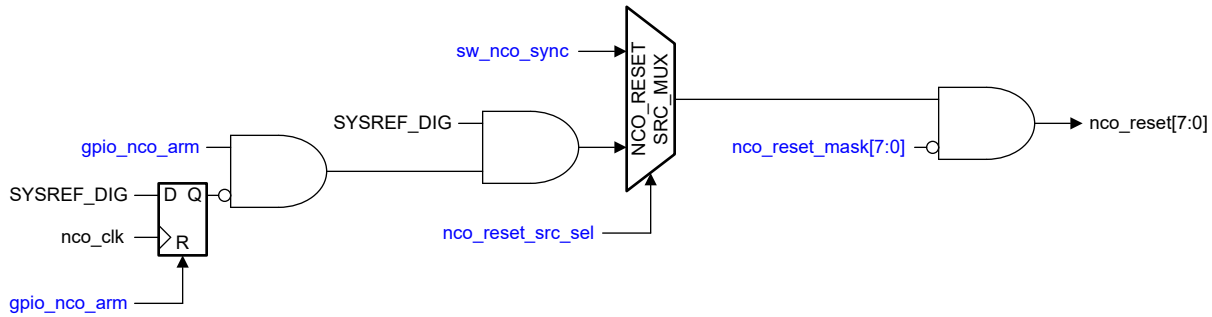



**Figure 7-33. NCO RESET With All Control Signals**

The gpio_nco_arm NCO reset path is used to synchronize multiple NCOs across devices from a host device. The host device can launch the gpio_nco_arm on the falling edge of the SYSREF to give the maximum time for the gpio_nco_arm signal to reach all devices prior to the next SYSREF edge.


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The following registers can be programmed:

**Table 7-15. Mixer and NCO Programming**

| System Parameter Name | Size | Default | Access | Description |
|---|---|---|---|---|
| DDC_NCO_UPDATE_SRC_SEL | 1 | 0 | R/W | Select the source of the NCO update signal.<br>0: The NCO update signal is sourced from software.<br>1: Leaking the internal SYSREF (SYSREF_DIG) to update the NCOs. |
| DDC_NCO_RESET_SRC_SEL | 1 | 0 | R/W | Select the source of the NCO reset signal.<br>0: The NCO reset signal is sourced from software.<br>1: The GPIO arm signal (gpio_nco_arm) arms the NCO module so that an NCO update signal is issued on the next rising edge of SYSREF. |
| DDC_NCO_UPDATE_MASK | 8 | 0 | R/W | Per DDC NCO update signal masking control. If the NCO update source is from software, DDC[x] and DDC[x+1], where x ∈ {0,2,4,6}, must be configured identically. Setting the mask bit to 1 makes sure the respective DDC NCOs are masked from the NCO update signal.<br>Bit 0: DDC0 NCO update mask control.<br>Bit 1: DDC1 NCO update mask control.<br>Bit 2: DDC2 NCO update mask control.<br>Bit 3: DDC3 NCO update mask control.<br>Bit 4: DDC4 NCO update mask control.<br>Bit 5: DDC5 NCO update mask control.<br>Bit 6: DDC6 NCO update mask control.<br>Bit 7: DDC7 NCO update mask control. |
| DDC_NCO_RESET_MASK | 8 | 0 | R/W | Per DDC NCO reset signal masking control. If the NCO reset source is from software, DDC[x] and DDC[x+1], where x ∈ {0,2,4,6}, must be configured identically. Setting the mask bit to 1 makes sure the respective DDC NCOs are masked from the NCO reset signal.<br>Bit 0: DDC0 NCO update reset control.<br>Bit 1: DDC1 NCO update reset control.<br>Bit 2: DDC2 NCO update reset control.<br>Bit 3: DDC3 NCO update reset control.<br>Bit 4: DDC4 NCO update reset control.<br>Bit 5: DDC5 NCO update reset control.<br>Bit 6: DDC6 NCO update reset control.<br>Bit 7: DDC7 NCO update reset control. |
| DDC{0..7}_NCO_HOP_SRC_SEL | 1 | 0 | R/W | Select the source of the NCO hoping signal for the DDC.<br>0: NCO selection (frequency hopping) through GPIO (one GPIO function per DDC).<br>1: NCO selection (frequency hopping) through software. |
| DDC{0..7}_NCO_HOP_MODE | 1 | 0 | R/W | Select the NCO mode when hopping.<br>0: Not used<br>1: Phase coherent hopping mode where the original phase of the NCOs is always maintained across hops. |
| DDC{0..7}_NCO{0,1}_FCW | 48 | 0 | R/W | 48-bit FCW word for NCO{0,1} |
| DDC{0..7}_NCO{0,1}_PHASE | 19 | 0 | R/W | 19-bit phase offset for NCO{0,1} |

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### 7.3.6 Digital Output Interface

The ADC32RF7x supports two different digital output data interfaces:

1. JESD204B/C: This interface uses up to 8 serial output lanes supporting data rates of up to 16Gbps/lane (JESD204B), and up to 24.75Gbps/lane (JESD204C).
2. LVDS: Not yet supported in software

#### 7.3.6.1 JESD204B/C Interface

The ADC32RF7x uses the JESD204B/C high-speed serial interface to transfer data from the ADC to the receiving logic device. ADC32RF7x serialized lanes are capable of operating up to 24.75Gbps using JESD204C and up to 15Gbps using JESD204B. The device supports up to 2 JESD links (operated at the same lane rate) and lane options of 1,2,4 or 8 lanes. Figure 7-34 shows an internal block diagram of the JESD204 interface as well as the configuration parameters for each of the two links.

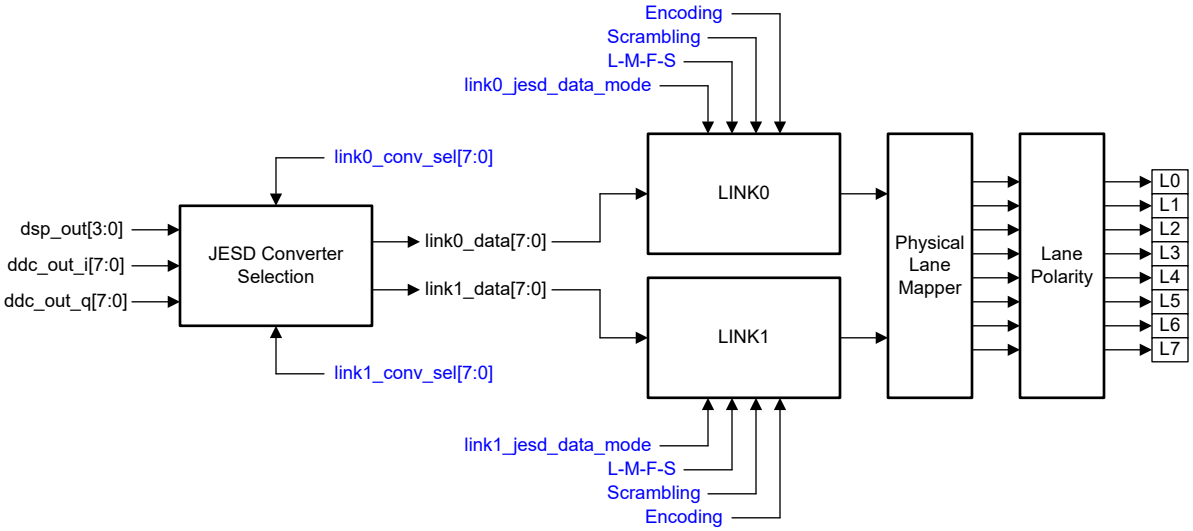



**Figure 7-34. JESD204 Block Diagram**

The following parameters and constraints need to be considered when configuring the JESD204B/C interface.

**Range of L, M, F, S, N and N'**

- L: Number of lanes: L ∈ {1,2,4,8}
- M: Number of converters: M ∈ {1,2,4,8}; for M=16 (octal band decimation), the JESD interface needs to configured to 2 links with M=8 per link
- F: Number of octets per frame: F ∈ {1,2,...,$F_{max}$}
- S: Number of samples per converter: $S$ ∈ {1,2,4}
- N': Sample resolution with padding: N' = 8·L·F/(M·S), and N' ∈ {16,24,32}
- N: Sample resolution without padding: N' ∈ {16,24} and N <= N'

**Constraints on F and N'**

- N' = 16 => $F_{max}$ = 64
- N' ∈ {24,32} => $F_{max}$ = 64
- N= 32 => F must be a multiple of 4.

**Constraints on Number of Lanes (L) and Lane Rate (LR)**

- JESD TX lane rate LR: 4.0Gbps to 24.75Gbps
- L = 8 is only allowed for JESD TX Link 0 and not for JESD TX link 1


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### Constraints on Decimation Factor (D) and Repeat Factor (R)

- Sample repeat factor R = $2^p$, $p \in \mathbb{N}^+$
- D <= 4: R = 1
- D%3 = 0: R = 1
- D%5 = 0: R = 1
- D > 4: D/R >= 4

### Constraints on JESD TX Converter Selection

- Selected converter C ∈ {0,1,...,19}, see Table 7-16
- Converters can be presented in any order within the set above
- In addition the constraints in Table 7-17 apply.

**Table 7-16. Converter Selection**

| CONVERTER | SELECTION NUMBER |
|---|---|
| DDC0_I | 0 |
| DDC0_Q | 1 |
| ... | ... |
| DDC7_Q | 15 |
| ADC0 | 16 |
| ADC1 | 17 |

**Table 7-17. Valid JESD Configurations**

| JESD DATA MODE | DECIMATION FACTOR D | NUMBER OF CONVERTERS M PER LINK | CONVERTERS AVAILABLE FOR SELECTION | CONVERTERS NUMBERS AVAILABLE FOR SELECTION |
|---|---|---|---|---|
| JESD_DATA_MODE_DSP_OUT | 1 (DDC BYPASS) | 1,2 | ADC0, ADC1 | 16,17 |
| JESD_DATA_MODE_DDC_OUT | 2,3 | 1,2,4 | DDC0_IQ, DDC1_IQ, DDC4_IQ, DDC5_IQ | 0,1,2,3,8,9,10,11 |
| | 4,5 | 1,2,4,8 | DDC0_IQ, ...DDC7_IQ | 0,1,2....14,15 |
| | 8,16,32... | | | |
| | 6,10,12,20,... | | | |

The following parameters can be programmed:

**Table 7-18. JESD TX Link Registers (x: 0 = LINK0, 1 = LINK1)**

| System Parameter Name | Size | Default | Reset | Description |
|---|---|---|---|---|
| LINK{x}_SCR_EN | 1 | 0 | RW | Control the JESD scrambler enable.<br>0: JESD scrambler is disabled.<br>1: JESD scrambler is enabled. |
| LINK{x}_JESD_TYPE | 1 | 0 | RW | Select the JESD type and must be set identically to the ENCODING setting.<br>0: 8b10b<br>1: 64b66b |
| LINK{x}_ENCODING | 1 | 0 | RW | Select the JESD encoding. Must be set identically to the JESD_TYPE setting.<br>0: 8b10b encoding.<br>1: 64b66b encoding. |
| LINK{x}_JESD_DATA_MODE | 2 | 0 | RW | Select the JESD data source.<br>0: DDC_OUT provided to JESD.<br>1: DSP_OUT provided to JESD.<br>2: not used<br>3: not used |

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**Table 7-18. JESD TX Link Registers (x: 0 = LINK0, 1 = LINK1) (continued)**

| System Parameter Name | Size | Default | Reset | Description |
|---|---|---|---|---|
| LINK{x}_JESD_LANES | 4 | 4 | RW | Set the JESD lanes (L) parameter for the link.<br>0: LINK is disabled.<br>1: JESD L parameter set to 1.<br>2: JESD L parameter set to 2.<br>4: JESD L parameter set to 4.<br>8: JESD L parameter set to 8. |
| LINK{x}_JESD_CONVERTERS | 4 | 2 | RW | Set the JESD converters (M) parameter for the link.<br>0: LINK is disabled.<br>1: JESD M parameter set to 1.<br>2: JESD M parameter set to 2.<br>4: JESD M parameter set to 4.<br>8: JESD M parameter set to 8. |
| LINK{x}_JESD_OCTETS_PER_FRAME | 7 | 1 | RW | Set the JESD octets per frame (F) parameter for the link. The max value is for F is 64. If N' is 32 then F must be a multiple of 4.<br>1...64: JESD F parameter value. |
| LINK{x}_JESD_SAMPLES_PER_CONVERTER | 3 | 1 | RW | Set the JESD samples per converter (S) parameter for the link.<br>1: JESD S parameter set to 1.<br>2: JESD S parameter set to 2.<br>4: JESD S parameter set to 4. |
| LINK{x}_JESD_K_OR_E | 8 | 32 | RW | Set either the JESD frames per multi-frame (K) or the multi-blocks per extended multi-block (E). This field is the K parameter when 8b10b encoding is used or E when 64b66b encoding is used. |
| LINK{x}_CONV_SEL_{y} | 5 | 16 | RW | Select the data source of the {y} converter in the link. (y=0..7)<br>0: DDC0 in-phase component data.<br>1: DDC0 quadrature component data.<br>2: DDC1 in-phase component data.<br>3: DDC1 quadrature component data.<br>4: DDC2 in-phase component data.<br>5: DDC2 quadrature component data.<br>6: DDC3 in-phase component data.<br>7: DDC3 quadrature component data.<br>8: DDC4 in-phase component data.<br>9: DDC4 quadrature component data.<br>10: DDC5 in-phase component data.<br>11: DDC5 quadrature component data.<br>12: DDC6 in-phase component data.<br>13: DDC6 quadrature component data.<br>14: DDC7 in-phase component data.<br>15: DDC7 quadrature component data.<br>16: ADC0 data from DSP_OUT.<br>17: ADC1 data from DSP_OUT.<br>18: ADC2 data from DSP_OUT.<br>19: ADC3 data from DSP_OUT. |
| JESD_SYNC_N_SRC_SEL | 2 | 0 | RW | Set the SYNC_N signal source for 8b10b.<br>0: GPIO0 used as SYNC_N input.<br>2: SYNC_N is internally generated through software. |


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**Table 7-18. JESD TX Link Registers (x: 0 = LINK0, 1 = LINK1) (continued)**

| System Parameter Name | Size | Default | Reset | Description |
|---|---|---|---|---|
| JESD_PHY_LANE{y}_DATA_SEL | 3 | 0,1 | RW | Set the physical lane data source for the lane{y}. (y = 0..7).<br>0: JESD logical lane 0 used as the lane data.<br>1: JESD logical lane 1 used as the lane data.<br>2: JESD logical lane 2 used as the lane data.<br>3: JESD logical lane 3 used as the lane data.<br>4: JESD logical lane 4 used as the lane data.<br>5: JESD logical lane 5 used as the lane data.<br>6: JESD logical lane 6 used as the lane data.<br>7: JESD logical lane 7 used as the lane data. |
| JESD_PHY_LANE_POLARITY_CTRL | 8 | 0 | RW | Set the individual physical lane polarity. If the bit is set, the corresponding physical lane polarity is inverted.<br>Bit 0: JESD physical lane 0 polarity control.<br>Bit 1: JESD physical lane 1 polarity control.<br>Bit 2: JESD physical lane 2 polarity control.<br>Bit 3: JESD physical lane 3 polarity control.<br>Bit 4: JESD physical lane 4 polarity control.<br>Bit 5: JESD physical lane 5 polarity control.<br>Bit 6: JESD physical lane 6 polarity control.<br>Bit 7: JESD physical lane 7 polarity control. |

#### *7.3.6.1.1 JESD204B Initial Lane Alignment (ILA)*

The receiving device starts the initial lane alignment process by deasserting the $\overline{\text{SYNC}}$ signal. When a logic low state is detected on the $\overline{\text{SYNC}}$ input, the ADC starts transmitting comma characters (K28.5) to establish the code group synchronization, as shown in Figure 7-35. When synchronization is completed, the receiving device reasserts the $\overline{\text{SYNC}}$ signal and the ADC starts the initial lane alignment sequence with the next local multi-frame clock (LMFC) boundary. The ADC transmits four multi-frames, each containing K frame (K is SPI programmable). Each of the multi-frames contains the frame start and frame end symbols. The second multi-frame also contains the JESD204B link configuration data.

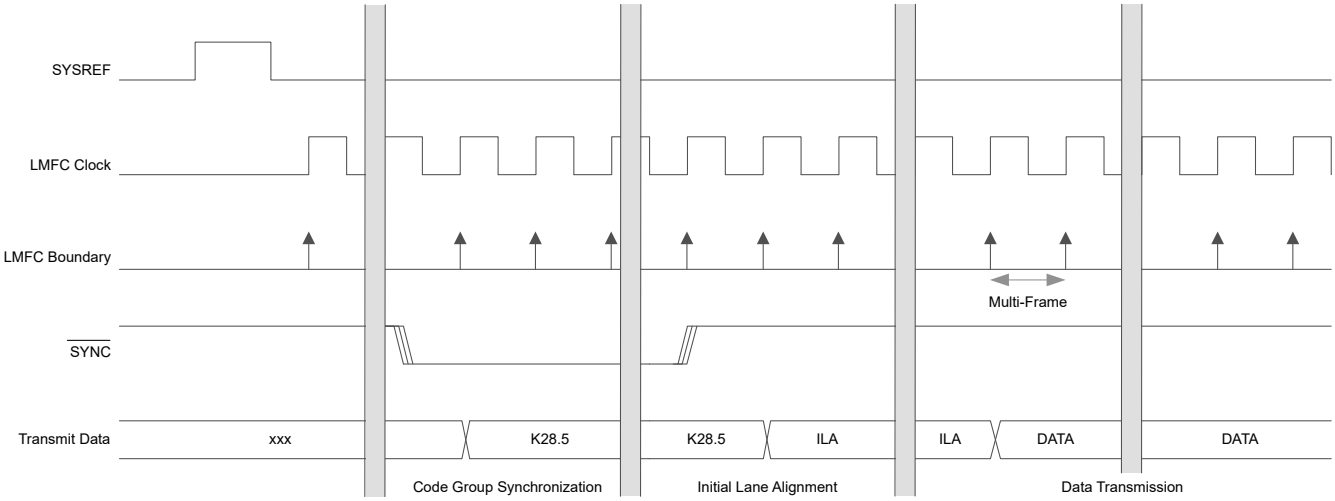



**Figure 7-35. JESD204B Internal Timing Diagram**

#### 7.3.6.1.2 $\overline{\text{SYNC}}$ Signal

The $\overline{\text{SYNC}}$ signal is issued using one of two different methods:

1. Use the $\overline{\text{SYNC}}$ input pin to issue a SYNC request
2. The synchronization command is issued via SPI

#### 7.3.6.1.3 JESD204B/C Frame Assembly

The JESD204B/C standard defines the following parameters:

- L: number of lanes per link
- M: number of converters per device
- F: number of octets per frame clock period
- S: number of samples per frame

#### 7.3.6.1.4 JESD204B/C Frame Assembly in Bypass Mode

Table 7-19 lists the available JESD204B/C formats and corresponding valid sampling rate ranges for the ADC32RF7x. The sampling rates are limited by the minimum and maximum SERDES line rate as well as ADC sampling clock frequencies. The JESD204B/C frame assembly for the different lanes is shown in Table 7-20.

**Table 7-19. JESD Mode Options: Bypass Mode**

| OUTPUT RESOLUTION (Bits) | L | M | F | S | JESD204B: Lane Rate (Gbps) | JESD204B RATIO [$f_{SERDES}/F_S$] | JESD204C: Lane Rate (Gbps) | JESD204C RATIO [$f_{SERDES}/F_S$] |
|---|---|---|---|---|---|---|---|---|
| 16 | 8 | 2 | 1 | 2 | $F_S$ x 16 x 10 / 8 x M / L | 5 | $F_S$ x 16 x 66 / 64 x M / L | 4.125 |
| | 4 | 2 | 1 | 1 | | 10 | | 8.25 |
| | 2 | 2 | 2 | 1 | | 20 | | 16.5 |
| | 4 | 1 | 1 | 2 | | 5 | | 4.125 |
| | 2 | 1 | 1 | 1 | | 10 | | 8.25 |
| | 1 | 1 | 2 | 1 | | 20 | | 16.5 |

**Table 7-20. Example JESD Sample Frame Assembly: Bypass Mode**

| OUTPUT LANE | LMFS = 8-2-1-2 | LMFS = 4-2-1-1 | LMFS = 2-2-2-1 | LMFS = 4-1-1-2 | LMFS = 2-1-1-1 | LMFS = 1-1-2-1 |
|---|---|---|---|---|---|---|
| STX0 | $A_0$[15:8] | $A_0$[15:8] | $A_0$[15:0] | $A_0$[15:8] | $A_0$[15:8] | $A_0$[15:0] |
| STX1 | $A_0$[7:0] | $A_0$[7:0] | $B_0$[15:0] | $A_0$[7:0] | $A_0$[7:0] | |
| STX2 | $A_1$[15:8] | $B_0$[15:8] | | $A_1$[15:8] | | |
| STX3 | $A_1$[7:0] | $B_0$[7:0] | | $A_1$[7:0] | | |
| STX4 | $B_0$[15:8] | | | | | |
| STX5 | $B_0$[7:0] | | | | | |
| STX6 | $B_1$[15:8] | | | | | |
| STX7 | $B_1$[7:0] | | | | | |


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#### 7.3.6.1.5 JESD204B/C Frame Assembly With Real Decimation

Table 7-21 lists the available JESD204B/C interface configurations and corresponding SerDes lane rates. The boundary conditions are:

- JESD204B: lane rates from 4 (min) to 15Gbps (max)
- JESD204C: lane rates from 4 (min) to 24.75Gbps (max)

Examples of JESD204B/C frame assemblies are illustrated in Table 7-21 to Table 7-23.

**Table 7-21. JESD Mode Options: Real Decimation**

| Output Resolution (bit) | L | M | F | S | JESD204B: Lane Rate (Gbps) | JESD204B: RATIO [$f_{SERDES}/(F_S/N)$] | JESD204C: Lane Rate (Gbps) | JESD204C: RATIO [$f_{SERDES}/(F_S/N)$] |
|---|---|---|---|---|---|---|---|---|
| 16 | 4 | 2 | 1 | 1 | $F_S$ x 20 x M / D / L | 10 | $F_S$ x 16 x 66 / 64 x M / D / L | 8.25 |
| | 2 | 2 | 2 | 1 | | 20 | | 16.5 |
| | 1 | 2 | 4 | 1 | | 40 | | 33 |
| | 2 | 1 | 1 | 1 | | 10 | | 8.25 |
| | 1 | 1 | 2 | 1 | | 20 | | 16.5 |
| 24 | 2 | 2 | 3 | 1 | $F_S$ x 30 x M / D / L | 30 | $F_S$ x 24 x 66 / 64 x M / D / L | 24.75 |
| | 1 | 2 | 6 | 1 | | 60 | | 49.5 |
| | 1 | 1 | 3 | 1 | | 30 | | 24.75 |

D: Decimation setting

**Table 7-22. Example JESD Frame Assembly: Real Decimation 16-bit output - Dual and Single Band**

| OUTPUT LANE | LMFS = 4-2-1-1 | LMFS = 2-2-2-1 | LMFS = 1-2-4-1 | | LMFS = 2-1-1-1 | LMFS = 1-1-2-1 |
|---|---|---|---|---|---|---|
| STX0 | $A_0$ [15:8] | $A_0$ [15:0] | $A_0$ [15:0] | $B_0$ [15:0] | $A_0$ [15:8] | $A_0$ [15:0] |
| STX1 | $A_0$ [7:0] | $B_0$ [15:0] | | | $A_0$ [7:0] | |
| STX2 | $B_0$ [15:8] | | | | | |
| STX3 | $B_0$ [7:0] | | | | | |
| STX4..7 | | | | | | |

**Table 7-23. Example JESD Sample Frame Assembly: Real Decimation 24-bit output - Dual and Single Band**

| OUTPUT LANE | LMFS = 2-2-3-1 | LMFS = 1-2-6-1 | | LMFS = 1-1-3-1 |
|---|---|---|---|---|
| STX0 | $A_0$ [23:0] | $A_0$ [23:0] | $B_0$ [23:0] | $A_0$ [23:0] |
| STX1 | $B_0$ [23:0] | | | |
| STX2..7 | | | | |

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#### *7.3.6.1.6 JESD204B,C Frame Assembly With Complex Decimation*

Table 7-24 lists the available JESD204B,C interface configurations and corresponding SerDes lane rates. The boundary conditions are:

- JESD204B: lane rates from 4 (min) to 15Gpbs (max)
- JESD204C: lane rates from 4 (min) to 24.75Gbps (max)

The JESD204B/C frame assemblies are shown in Table 7-25 (16-bit) and Table 7-29 (24-bit).

When using octal band DDC, two separate JESD links need to be configured because the M (# of converters per link) cannot exceed 8 as shown in Table 7-25. For example for octal band DDC using 8 JESD lanes each of the two links can be configured as LMFS = 4-8-4-1. The internal JESD output mux can be used to assign specific SerDes lanes to each link.

**Table 7-24. JESD Mode Options: Complex Decimation**

| Output Resolution (bit) | L | M | F | S | JESD204B: Lane Rate (Gbps) | JESD204B: RATIO [$f_{SERDES}/(F_S/N)$] | JESD204C: Lane Rate (Gbps) | JESD204C: RATIO [$f_{SERDES}/(F_S/N)$] |
|---|---|---|---|---|---|---|---|---|
| 16 | 8 | 8 | 2 | 1 | $F_S \times 16 \times 10 / 8 \times M / D / L$ | 20 | $F_S \times 16 \times 66 / 64 \times M / D / L$ | 16.5 |
| | 4 | 8 | 4 | 1 | | 40 | | 33 |
| | 2 | 8 | 8 | 1 | | 80 | | 66 |
| | 1 | 8 | 16 | 1 | | 160 | | 132 |
| | 8 | 4 | 1 | 1 | | 10 | | 8.25 |
| | 4 | 4 | 2 | 1 | | 20 | | 16.5 |
| | 2 | 4 | 4 | 1 | | 40 | | 33 |
| | 1 | 4 | 8 | 1 | | 80 | | 66 |
| | 8 | 2 | 1 | 2 | | 5 | | 4.125 |
| | 4 | 2 | 1 | 1 | | 10 | | 8.25 |
| | 2 | 2 | 2 | 1 | | 20 | | 16.5 |
| | 1 | 2 | 4 | 1 | | 40 | | 33 |
| 24 | 8 | 8 | 3 | 1 | $F_S \times 24 \times 10 / 8 \times M / D / L$ | 30 | $F_S \times 24 \times 66 / 64 \times M / D / L$ | 24.75 |
| | 4 | 8 | 6 | 1 | | 60 | | 49.5 |
| | 2 | 8 | 12 | 1 | | 120 | | 99 |
| | 1 | 8 | 24 | 1 | | 240 | | 198 |
| | 8 | 4 | 3 | 2 | | 15 | | 12.375 |
| | 4 | 4 | 3 | 1 | | 30 | | 24.75 |
| | 2 | 4 | 6 | 1 | | 60 | | 49.5 |
| | 1 | 4 | 12 | 1 | | 120 | | 99 |
| | 8 | 2 | 3 | 4 | | 7.5 | | 6.1875 |
| | 4 | 2 | 3 | 2 | | 15 | | 12.375 |
| | 2 | 2 | 3 | 2 | | 30 | | 24.75 |
| | 1 | 2 | 6 | 1 | | 60 | | 49.5 |

D: complex decimation setting


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**Table 7-25. Example JESD Frame Assembly: Complex Decimation, Octal Band, 16-bit Output**
**Note: the LMFS configuration is Per JESD Link**

| JESD LINK | OUTPUT LANE | LMFS = 4-8-4-1 | LMFS = 2-8-8-1 | | LMFS = 1-8-16-1 | | | |
|---|---|---|---|---|---|---|---|---|
| LINK0 | STX0 | $AI_0$ [15:0], $AQ_0$ [15:0] | $AI_0$ [15:0], $AQ_0$ [15:0] | $BI_0$ [15:0], $BQ_0$ [15:0] | $AI_0$ [15:0], $AQ_0$ [15:0] | $BI_0$ [15:0], $BQ_0$ [15:0] | $CI_0$ [15:0], $CQ_0$ [15:0] | $DI_0$ [15:0], $DQ_0$ [15:0] |
| | STX1 | $BI_0$ [15:0], $BQ_0$ [15:0] | $CI_0$ [15:0], $CQ_0$ [15:0] | $DI_0$ [15:0], $DQ_0$ [15:0] | | | | |
| | STX2 | $CI_0$ [15:0], $CQ_0$ [15:0] | | | | | | |
| | STX3 | $DI_0$ [15:0], $DQ_0$ [15:0] | | | | | | |
| LINK1 | STX4 | $EI_0$ [15:0], $EQ_0$ [15:0] | $EI_0$ [15:0], $EQ_0$ [15:0] | $FI_0$ [15:0], $FQ_0$ [15:0] | $EI_0$ [15:0], $EQ_0$ [15:0] | $FI_0$ [15:0], $FQ_0$ [15:0] | $GI_0$ [15:0], $GQ_0$ [15:0] | $HI_0$ [15:0], $HQ_0$ [15:0] |
| | STX5 | $FI_0$ [15:0], $FQ_0$ [15:0] | $GI_0$ [15:0], $GQ_0$ [15:0] | $HI_0$ [15:0], $HQ_0$ [15:0] | | | | |
| | STX6 | $GI_0$ [15:0], $GQ_0$ [15:0] | | | | | | |
| | STX7 | $HI_0$ [15:0], $HQ_0$ [15:0] | | | | | | |

**Table 7-26. Example JESD Frame Assembly: Complex Decimation, Quad Band, 16-bit Output**

| OUTPUT LANE | LMFS = 8-8-2-1 | LMFS = 4-8-4-1 | LMFS = 2-8-8-1 | | LMFS = 1-8-16-1 | | | |
|---|---|---|---|---|---|---|---|---|
| STX0 | $AI_0$ [15:0] | $AI_0$ [15:0], $AQ_0$ [15:0] | $AI_0$ [15:0], $AQ_0$ [15:0] | $BI_0$ [15:0], $BQ_0$ [15:0] | $AI_0$ [15:0], $AQ_0$ [15:0] | $BI_0$ [15:0], $BQ_0$ [15:0] | $CI_0$ [15:0], $CQ_0$ [15:0] | $DI_0$ [15:0], $DQ_0$ [15:0] |
| STX1 | $AQ_0$ [15:0] | $BI_0$ [15:0], $BQ_0$ [15:0] | $CI_0$ [15:0], $CQ_0$ [15:0] | $DI_0$ [15:0], $DQ_0$ [15:0] | | | | |
| STX2 | $BI_0$ [15:0] | $CI_0$ [15:0], $CQ_0$ [15:0] | | | | | | |
| STX3 | $BQ_0$ [15:0] | $DI_0$ [15:0], $DQ_0$ [15:0] | | | | | | |
| STX4 | $CI_0$ [15:0] | | | | | | | |
| STX5 | $CQ_0$ [15:0] | | | | | | | |
| STX6 | $DI_0$ [15:0] | | | | | | | |
| STX7 | $DQ_0$ [15:0] | | | | | | | |

**Table 7-27. Example JESD Frame Assembly: Complex Decimation, Dual Band, 16-bit Output**

| OUTPUT LANE | LMFS = 8-4-1-1 | LMFS = 4-4-2-1 | LMFS = 2-4-4-1 | | LMFS = 1-4-8-1 | | | |
|---|---|---|---|---|---|---|---|---|
| STX0 | $AI_0$ [15:8] | $AI_0$ [15:0] | $AI_0$ [15:0] | $AQ_0$ [15:0] | $AI_0$ [15:0] | $AQ_0$ [15:0] | $BI_0$ [15:0] | $BQ_0$ [15:0] |
| STX1 | $AI_0$ [7:0] | $AQ_0$ [15:0] | $BI_0$ [15:0] | $BQ_0$ [15:0] | | | | |
| STX2 | $AQ_0$ [15:8] | $BI_0$ [15:0] | | | | | | |
| STX3 | $AQ_0$ [7:0] | $BQ_0$ [15:0] | | | | | | |
| STX4 | $BI_0$ [15:8] | | | | | | | |
| STX5 | $BI_0$ [7:0] | | | | | | | |
| STX6 | $BQ_0$ [15:8] | | | | | | | |
| STX7 | $BQ_0$ [7:0] | | | | | | | |

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**Table 7-28. Example JESD Frame Assembly: Complex Decimation, Single Band, 16-bit Output**

| OUTPUT LANE | LMFS = 8-2-1-2 | LMFS = 4-2-1-1 | LMFS = 2-2-2-1 | | LMFS = 1-2-4-1 | | | |
|---|---|---|---|---|---|---|---|---|
| STX0 | $AI_0$ [15:8] | $AI_0$ [15:8] | $AI_0$ [15:8] | $AI_0$ [7:0] | $AI_0$ [15:8] | $AI_0$ [7:0] | $AQ_0$ [15:8] | $AQ_0$ [7:0] |
| STX1 | $AI_0$ [7:0] | $AI_0$ [7:0] | $AQ_0$ [15:8] | $AQ_0$ [7:0] | | | | |
| STX2 | $AQ_0$ [15:8] | $AQ_0$ [15:8] | | | | | | |
| STX3 | $AQ_0$ [7:0] | $AQ_0$ [7:0] | | | | | | |
| STX4 | $AI_1$ [15:8] | | | | | | | |
| STX5 | $AI_1$ [7:0] | | | | | | | |
| STX6 | $AQ_1$ [15:8] | | | | | | | |
| STX7 | $AQ_1$ [7:0] | | | | | | | |

**Table 7-29. Example JESD Frame Assembly: Complex Decimation, Octal Band, 24-bit Output**
**Note: the LMFS configuration is Per JESD Link**

| JESD LINK | OUTPUT LANE | LMFS = 4-8-6-1 | LMFS = 2-8-12-1 | | LMFS = 1-8-24-1 | | | |
|---|---|---|---|---|---|---|---|---|
| LINK0 | STX0 | $AI_0$ [23:0], $AQ_0$ [23:0] | $AI_0$ [23:0], $AQ_0$ [23:0] | $BI_0$ [23:0], $BQ_0$ [23:0] | $AI_0$ [23:0], $AQ_0$ [23:0] | $BI_0$ [23:0], $BQ_0$ [23:0] | $CI_0$ [23:0], $CQ_0$ [23:0] | $DI_0$ [23:0], $DQ_0$ [23:0] |
| | STX1 | $BI_0$ [23:0], $BQ_0$ [23:0] | $CI_0$ [23:0], $CQ_0$ [23:0] | $DI_0$ [23:0], $DQ_0$ [23:0] | | | | |
| | STX2 | $CI_0$ [23:0], $CQ_0$ [23:0] | | | | | | |
| | STX3 | $DI_0$ [23:0], $DQ_0$ [23:0] | | | | | | |
| LINK1 | STX4 | $EI_0$ [23:0], $EQ_0$ [23:0] | $EI_0$ [23:0], $EQ_0$ [23:0] | $FI_0$ [23:0], $FQ_0$ [23:0] | $EI_0$ [23:0], $EQ_0$ [23:0] | $FI_0$ [23:0], $FQ_0$ [23:0] | $GI_0$ [23:0], $GQ_0$ [23:0] | $HI_0$ [23:0], $HQ_0$ [23:0] |
| | STX5 | $FI_0$ [23:0], $FQ_0$ [23:0] | $GI_0$ [23:0], $GQ_0$ [23:0] | $HI_0$ [23:0], $HQ_0$ [23:0] | | | | |
| | STX6 | $GI_0$ [23:0], $GQ_0$ [23:0] | | | | | | |
| | STX7 | $HI_0$ [23:0], $HQ_0$ [23:0] | | | | | | |

**Table 7-30. Example JESD Frame Assembly: Complex Decimation, Quad Band, 24-bit Output**

| OUTPUT LANE | LMFS = 8-8-3-1 | LMFS = 4-8-6-1 | LMFS = 2-8-12-1 | | LMFS = 1-8-24-1 | | | |
|---|---|---|---|---|---|---|---|---|
| STX0 | $AI_0$ [23:0] | $AI_0$ [23:0], $AQ_0$ [23:0] | $AI_0$ [23:0], $AQ_0$ [23:0] | $BI_0$ [23:0], $BQ_0$ [23:0] | $AI_0$ [23:0], $AQ_0$ [23:0] | $BI_0$ [23:0], $BQ_0$ [23:0] | $CI_0$ [23:0], $CQ_0$ [23:0] | $DI_0$ [23:0], $DQ_0$ [23:0] |
| STX1 | $AQ_0$ [23:0] | $BI_0$ [23:0], $BQ_0$ [23:0] | $CI_0$ [23:0], $CQ_0$ [23:0] | $DI_0$ [23:0], $DQ_0$ [23:0] | | | | |
| STX2 | $BI_0$ [23:0] | $CI_0$ [23:0], $CQ_0$ [23:0] | | | | | | |
| STX3 | $BQ_0$ [23:0] | $DI_0$ [23:0], $DQ_0$ [23:0] | | | | | | |
| STX4 | $CI_0$ [23:0] | | | | | | | |
| STX5 | $CQ_0$ [23:0] | | | | | | | |
| STX6 | $DI_0$ [23:0] | | | | | | | |
| STX7 | $DQ_0$ [23:0] | | | | | | | |


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**Table 7-31. Example JESD Frame Assembly: Complex Decimation, Dual Band, 24-bit Output**

| OUTPUT LANE | LMFS = 8-4-3-2 | LMFS = 4-4-3-1 | LMFS = 2-4-6-1 | | LMFS = 1-4-12-1 | | | |
|---|---|---|---|---|---|---|---|---|
| STX0 | $AI_0$ [23:0] | $AI_0$ [23:0] | $AI_0$ [23:0] | $AQ_0$ [23:0] | $AI_0$ [23:0] | $AQ_0$ [23:0] | $BI_0$ [23:0] | $BQ_0$ [23:0] |
| STX1 | $AQ_0$ [23:0] | $AQ_0$ [23:0] | $BI_0$ [23:0] | $BQ_0$ [23:0] | | | | |
| STX2 | $AI_1$ [23:0] | $BI_0$ [23:0] | | | | | | |
| STX3 | $AQ_1$ [23:0] | $BQ_0$ [23:0] | | | | | | |
| STX4 | $BI_0$ [23:0] | | | | | | | |
| STX5 | $BQ_0$ [23:0] | | | | | | | |
| STX6 | $BI_1$ [23:0] | | | | | | | |
| STX7 | $BQ_1$ [23:0] | | | | | | | |

**Table 7-32. Example JESD Frame Assembly: Complex Decimation, Single Band, 24-bit Output**

| OUTPUT LANE | LMFS = 8-2-3-4 | LMFS = 4-2-3-2 | LMFS = 2-2-3-1 | LMFS = 1-2-6-1 | |
|---|---|---|---|---|---|
| STX0 | $AI_0$ [23:0] | $AI_0$ [23:0] | $AI_0$ [23:0] | $AI_0$ [23:0] | $AQ_0$ [23:0] |
| STX1 | $AQ_0$ [23:0] | $AQ_0$ [23:0] | $AQ_0$ [23:0] | | |
| STX2 | $AI_1$ [23:0] | $AI_1$ [23:0] | | | |
| STX3 | $AQ_1$ [23:0] | $AQ_1$ [23:0] | | | |
| STX4 | $AI_2$ [23:0] | | | | |
| STX5 | $AQ_2$ [23:0] | | | | |
| STX6 | $AI_3$ [23:0] | | | | |
| STX7 | $AQ_3$ [23:0] | | | | |

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#### 7.3.6.2 JESD Output Reference Clock

The ADC provides an option to output the SERDES reference clock to the FPGA (see Figure 7-36). This JESD reference clock is configured to be SerDes lane rate / (8x k) where k can be any integer between 4 and 255. This provides a high flexibility of supported reference clock frequencies.

The output clock can be configured to be single ended LVCMOS or differential LVDS. This circuit is powered down by default. If not used, the JESDCLKP/N pins is left floating.

The JESD output clock is derived directly from the internal SERDES PLL and does not provide deterministic latency.

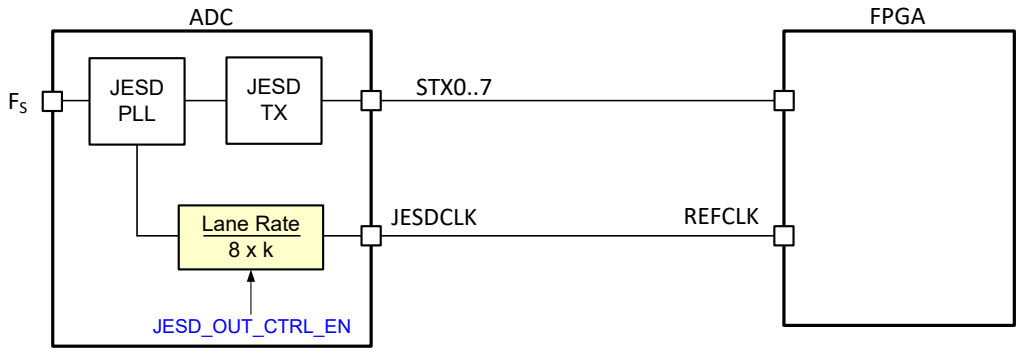



**Figure 7-36. JESD reference clock output for the FPGA SERDES PLL**

The JESD clock output can be can be programmed using the following parameters:

**Table 7-33. JESD clock output Configuration Programming**

| System Parameter Name | Size | Default | Access | Description |
|---|---|---|---|---|
| JESD_OUT_EN_CTRL | 1 | 0 | R/W | Enable control for JESD output.<br>0: JESD output is disabled.<br>1: JESD output is enabled. |
| JESD_OUT_DIV0 | 8 | 0 | R/W | Bits [7:0] of JESD clock output divider factor. |
| JESD_OUT_DIV1 | 8 | 0 | R/W | Bits [12:8] of JESD clock output divider factor. |


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## 7.4 Device Functional Modes

The device has 2 different operating modes (see also Figure 7-37). Any two out of the four input channels can be selected for either operating mode.

1. Normal operation: one ADC core per input channel. This is the lowest power consumption per channel mode.
2. 2x averaging: The input signal is externally connected to 2 ADC channels. Internally the output of two ADCs is averaged for SNR improvement (best improvement = 3dB).

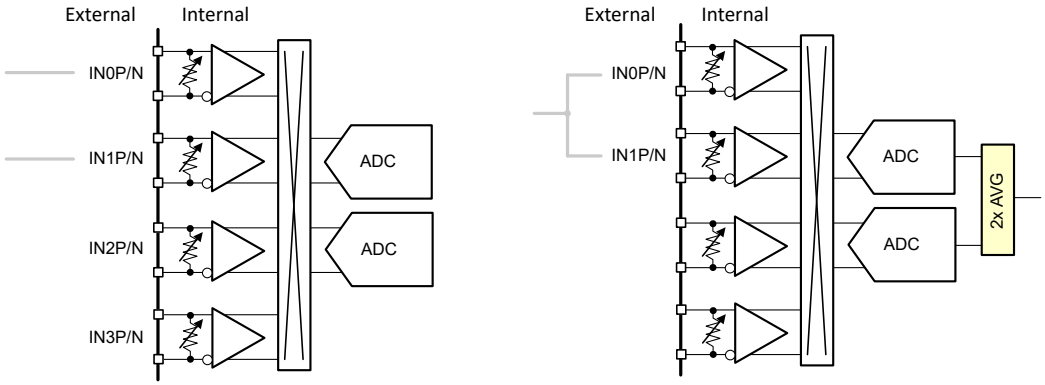



**Figure 7-37. Operating modes: normal operation (left) and 2x averaging (right)**

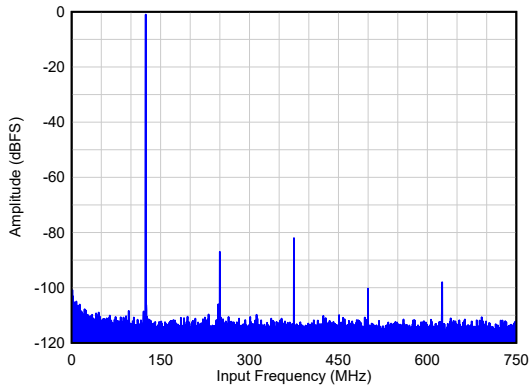
**Table 7-34. Mode Comparison (typical)**

| Operating Mode | # of Output Channels | $SNR_{flat}$ at $F_{IN}$ = 125MHz, $A_{IN}$ = −1dBFS | $SNR_{flat}$ at $F_{IN}$ = 125MHz, $A_{IN}$ = −20dBFS | $NSD_{flat}$ at $F_{IN}$ = 125MHz, $A_{IN}$ = −20dBFS |
|---|---|---|---|---|
| Normal | 2 | 74.8dBFS | 75.5dBFS | −163.6dBFS/Hz |
| 2x Averaging | 1 | 77.5dBFS | 78.3dBFS | −166.4dBFS/Hz |

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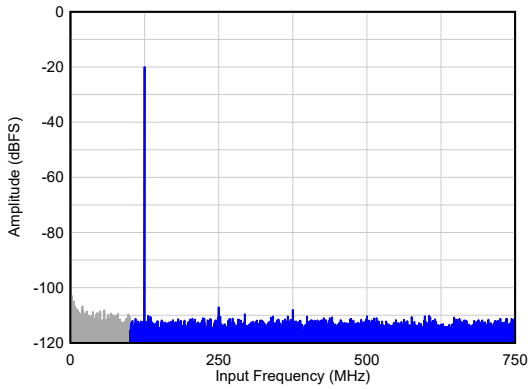
### 7.4.1 Device Operating Mode Comparison

Following are comparison measurements of the different operating modes for the same input signal configuration.



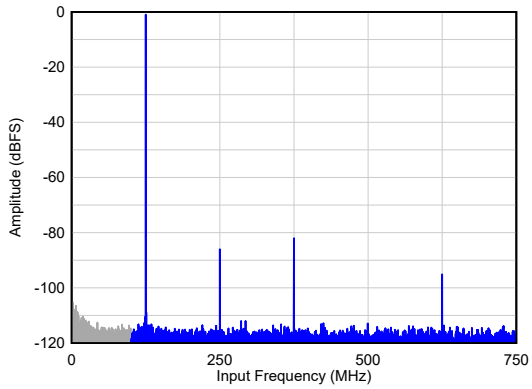

$F_{IN}$ = 125MHz, $A_{IN}$ = -1dBFS, $SNR_{flat}$ = 74.8dBFS

**Figure 7-38. Single tone FFT, Normal Mode**



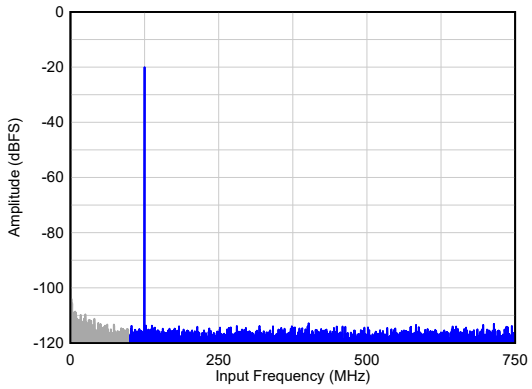

$F_{IN}$ = 125MHz, $A_{IN}$ = -20dBFS, $SNR_{flat}$ = 75.5dBFS

**Figure 7-39. Single tone FFT, Normal Mode**




$F_{IN}$ = 125MHz, $A_{IN}$ = -1dBFS, $SNR_{flat}$ = 77.5dBFS

**Figure 7-40. Single tone FFT, 2x Average Mode**




$F_{IN}$ = 200MHz, $A_{IN}$ = -20dBFS, $SNR_{flat}$ = 78.2dBFS

**Figure 7-41. Single tone FFT, 2x Average Mode**


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## 7.5 Programming

The device is primarily configured and controlled using the serial programming interface (SPI). However, there are digital features and functions available that can be configured via SPI and controlled/used via GPIO pins.

### *7.5.1 GPIO Control*

The device has 24 GPIO pins. Four are fixed function and the remaining 20 can be configured independently for different functions using the SPI.

**Table 7-35. GPIO: FIxed Functions**

| PIN NAME | FUNCTION | PIN # |
|---|---|---|
| $\overline{\text{RESET}}$ | Hardware RESET | J1 |
| SCLK | SPI SCLK | K15 |
| SDIO | SPI DIN/DOUT | L15 |
| SDOUT | SPI DOUT | L3 |
| $\overline{\text{SEN}}$ | SPI EN | J16 |
| $\overline{\text{SYNC}}$ | SYNC for JESD 8b/10b | J4 |

**Table 7-36. GPIO: Configurable Functions**

| FUNCTION | PIN No. | No. of PINS | DESCRIPTION |
|---|---|---|---|
| NCO CONTROL | ANY | 1..8 | The pin selects between 2 NCO frequencies for each DDC.<br>There are 8 DDCs and each NCO/DDC can be mapped to a specific GPIO pins. Using one GPIO pin for multiple/all DDCs is possible.<br>Functional only when using NCOs.<br>Low: nco_0 of each active DDC is selected.<br>High: nco_1 of each active DDC is selected. |
| OVR | | 1 | OR-ed outputs of each ADC OVR signal.<br>Low: no ADC is in saturation.<br>High: an ADC is in saturation. |
| NCO SYSREF ARM | | 1 | The GPIO pin is used to enable resetting the NCO phase to 0 with the next SYSREF rising edge. |
| CALIBRATION FREEZE | | 1 | Low: device background calibration is active.<br>High: device background calibration is inactive. |
| GLOBAL POWER DOWN | | 1 | Device global power down.<br>Low: device is powered up.<br>High: device is powered down. |
| FAST POWER DOWN | | 1 | Device global power down.<br>Low: device is powered up.<br>High: device is powered down. |

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### 7.5.2 SPI Register Write

The internal registers can be programmed following these steps:

1. Drive the $\overline{SEN}$ pin low (all SPI rising and falling clock edges need to occur while $\overline{SEN}$ driven low).
2. Set the R/W bit to 0 (bit A15 of the 16-bit address).
3. Initiate a serial interface cycle by specifying the address of the register (A[14:0]) whose content is written and
4. Write the 8-bit data that are latched in on the SCLK rising edges

Figure 7-42 shows the timing requirements for the serial register write operation.

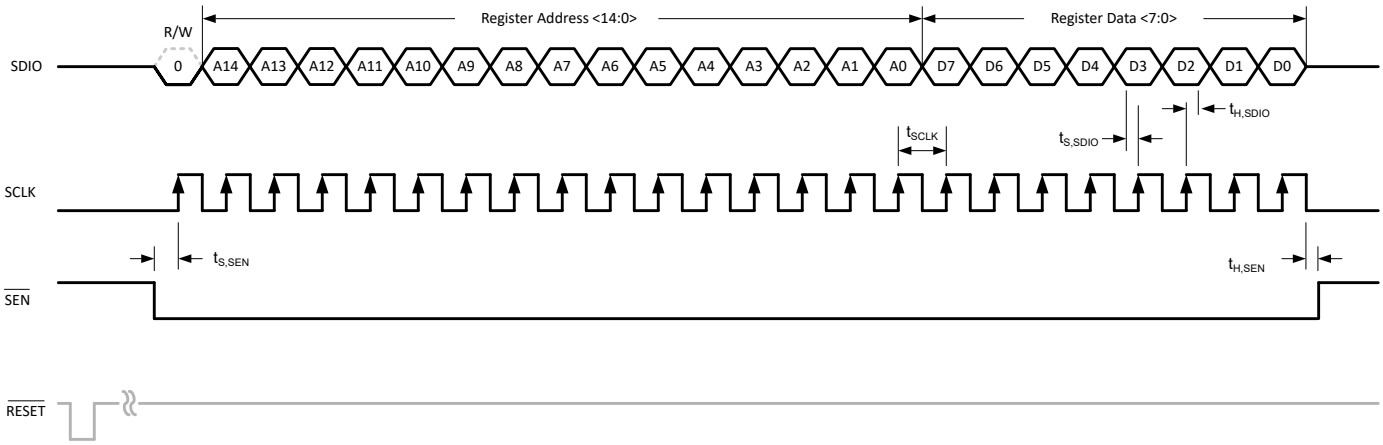



**Figure 7-42. Serial Register Write Timing Diagram**

### 7.5.3 SPI Register Read

The device includes a mode where the contents of the internal registers can be read back using the SDIO pin. This readback mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the $\overline{SEN}$ pin low (all SPI rising and falling clock edges need to occur while $\overline{SEN}$ driven low).
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers.
3. Initiate a serial interface cycle specifying the address of the register (A[14:0]) whose content must be read
4. The device launches the contents (D[7:0]) of the selected register on the SDIO pin on SCLK falling edge
5. The external controller can capture the contents on the SCLK rising edge

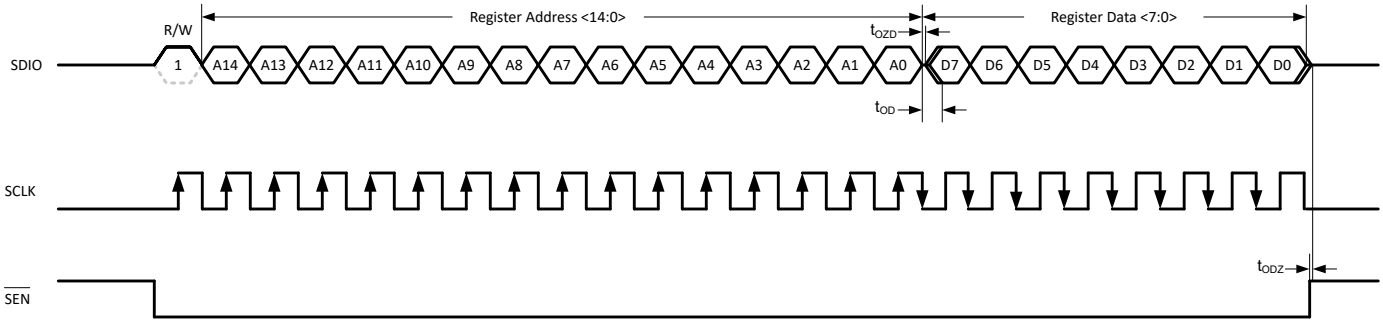



**Figure 7-43. Serial Register Read Timing Diagram**


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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The ADC32RF72 can be used in a wide range of applications including radar, frequency and/or time domain digitizer and spectrum analyzer, test and communications equipment and software-defined radios (SDRs). The Typical Applications section describe two configurations that meet the needs of a number of these applications.

## 8.2 Typical Application: Spectrum Analyzer

This section demonstrates the use of ADC32RF72 as a wideband RF sampling receiver. The device is flexible and can be used as either a 2-channel receiver or as a single channel receiver with better noise floor using internal digital averaging. The ADC is driven by single-ended RF amplifiers and the conversion to differential signaling is achieved by a transformer (balun). The device includes digital down-converters (DDCs) in both dual-channel and single-channel modes to mix the desired frequency band to baseband and down-sample the data to reduce the interface rate. The block diagram for the wideband RF sampling receiver is shown in Figure 8-1 where the device is configured in single-channel mode for best noise density.

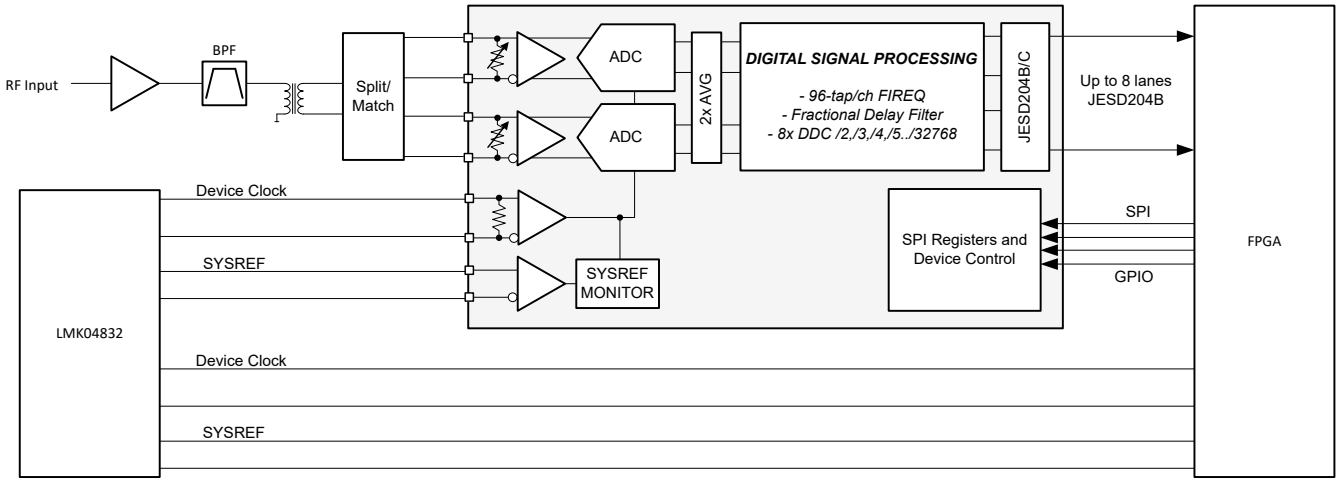



**Figure 8-1. Wideband RF Sampling Receiver**

### *8.2.1 Design Requirements*

#### 8.2.1.1 Input Signal Path: Wideband Receiver

Appropriate band limiting filters are used to reject unwanted frequencies in the receive signal path. A 1:2 (for 100Ω effective termination impedance) or a 1:1 (for 50Ω effective termination impedance) balun transformer is needed to convert the single ended RF input to differential for input to the ADC. The balun must have good amplitude (< 0.5dB) and phase balance (less than 2deg) within the frequency range of interest. A back-to-back balun configuration often times gives better SFDR performance. Table 8-1 lists several recommended baluns for different impedance ratios and frequency ranges. The S-parameters of the ADC input can be used to design the front end matching network.

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**Table 8-1. Recommended Baluns**

| PART NUMBER | MANURACTURER(1) | IMPEDANCE RATIO | AMPLITUDE BALANCE (dB) | PHASE BALANCE (°) | FREQUENCY RANGE |
|---|---|---|---|---|---|
| BAL-0003SMG | Marki Microwave | 1:2 | 0.1 | 3 | 0.5MHz to 3GHz |
| TCM2-43X+ | Minicircuits | 1:2 | 0.5 | 7 | 10MHz to 4GHz |
| TCM2-33WX+ | Minicircuits | 1:2 | 0.7 | 4 | 10MHz to 3GHz |
| TC1-1-13M+ | Minicircuits | 1:1 | 0.5 | 2-3 | 10MHz to 3GHz |

(1) See the Third-Party Products Disclaimer .

#### 8.2.1.2 Clocking

The device clock inputs must be AC-coupled to the device to provide the rated performance. The clock source must have low jitter (integrated phase noise) for the ADC to meet the stated SNR performance, especially when operating at higher input frequencies. The clock signal can be filtered with a band pass filter to remove some of the broad band clock noise. The JESD204B/C data converter system (ADC and FPGA) requires additional SYSREF and device clocks. The LMK04828 or LMK04832 devices are designed to generate these clocks. Depending on the ADC clock frequency and jitter requirements. The device can also be used as a system clock synthesizer or as a device clock and SYSREF distribution device when using multiple ADC32RF72 devices in a system.

### *8.2.2 Detailed Design Procedure*

#### 8.2.2.1 Sampling Clock Requirements

To maximize the SNR performance of the ADC, a very low jitter (< 50fs) sampling clock is required. Figure 8-2 shows the estimated SNR performance versus input frequency versus external clock jitter. The internal ADC aperture jitter also has some dependency to the clock amplitude (gets more sensitive with higher input frequency) as shown in Figure 8-3. When using averaging or decimation, the SNR for a single ADC core must be estimated first before adding the SNR improvement from internal averaging or decimation.

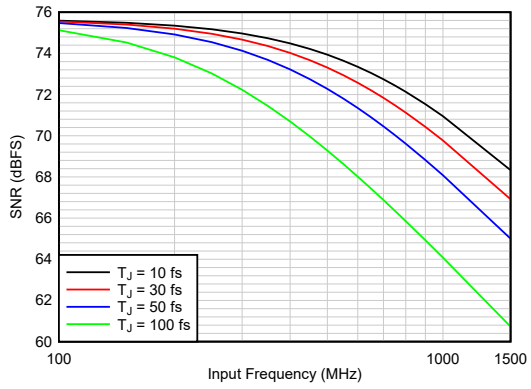



**Figure 8-2. SNR vs $T_{Jitter}$**

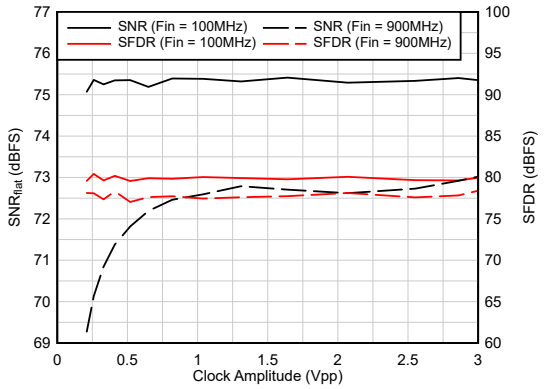



**Figure 8-3. AC Performance vs Clock Amplitude**


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### 8.2.3 Application Performance Plots

The following application curves demonstrate performance with 2x internal averaging configuration. The input frequency is 900MHz and input amplitudes of -1 and -20dBFS are shown in DDC bypass mode as well as 8x complex decimation.

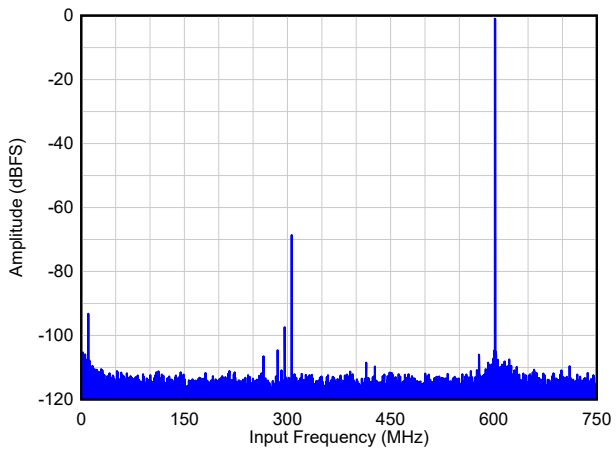



**Figure 8-4. $F_{IN}$ = 900MHz, $A_{IN}$ = -1dBFS, 2x Averaging, DDC Bypass**

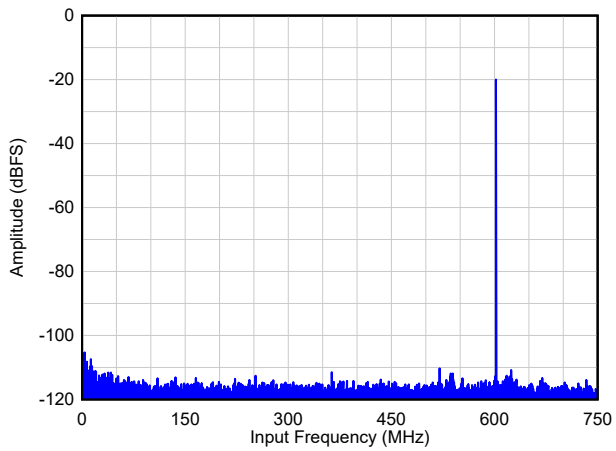



**Figure 8-5. $F_{IN}$ = 900MHz, $A_{IN}$ = -20dBFS, 2x Averaging, DDC Bypass**

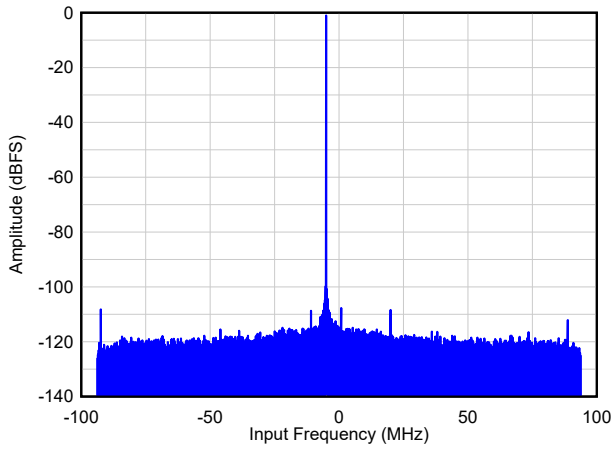



**Figure 8-6. $F_{IN}$ = 900MHz, $A_{IN}$ = -1dBFS, 2x Averaging, 8x complex decimation**

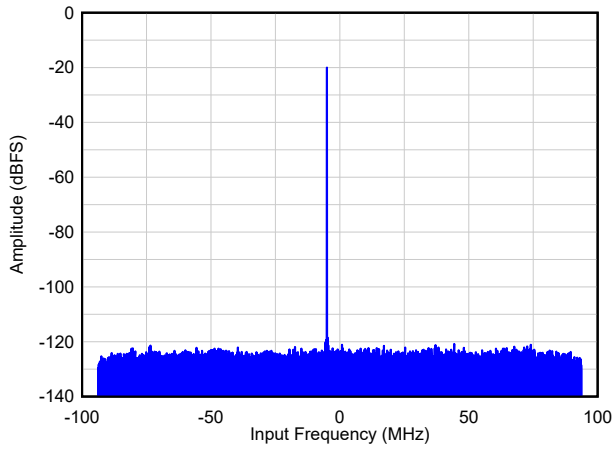



**Figure 8-7. $F_{IN}$ = 900MHz, $A_{IN}$ = -20dBFS, 2x Averaging, 8x complex decimation**

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## 8.3 Typical Application: Time Domain Digitizer

The ADC32RF72 offers several features such as low code error rate (CER), very low noise floor and high SNR and programmable, fractional digital delay that makes the device a great fit for time domain digitizer and oscilloscope applications. The block diagram for a typical time domain sampling signal chain in Figure 8-8 with the ADC32RF72 configured in dual-channel mode with 2x internal digital averaging for best noise density.

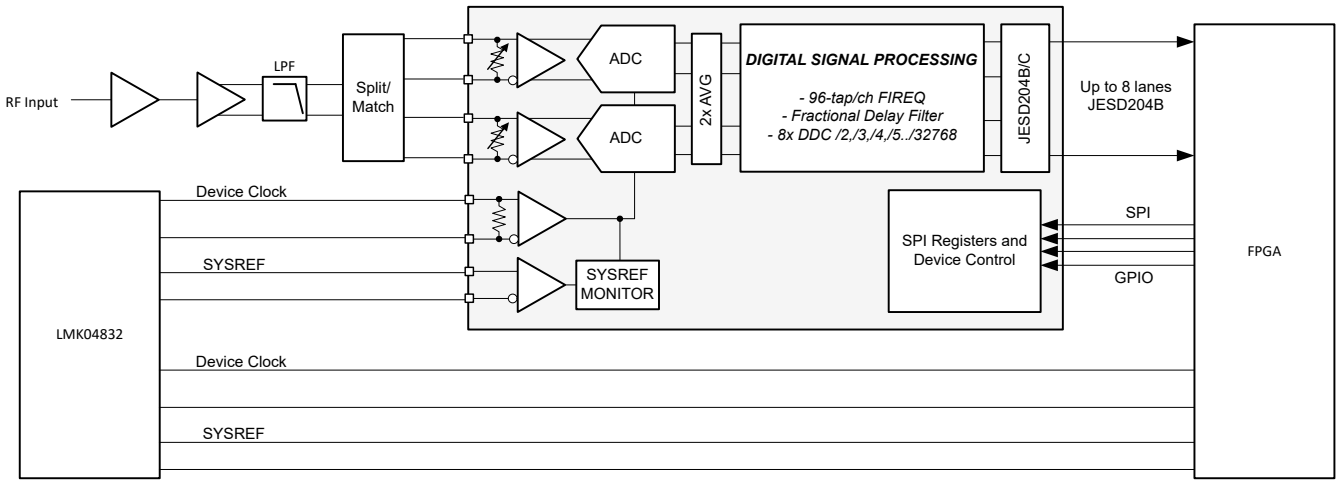



**Figure 8-8. Time Domain Digitizer**

### *8.3.1 Design Requirements*

#### 8.3.1.1 Input Signal Path: Time Domain Digitizer

Most time-domain digitizers are required to be DC-coupled to monitor DC or low-frequency signals. This requirement forces the design to use DC-coupled, fully differential amplifiers to convert from single-ended signaling at the front panel to differential signaling at the ADC. This design uses a differential amplifier. The LMH5401 amplifier has an 8GHz, gain-bandwidth product that is sufficient to support a 1GHz bandwidth digitizer. The LMH5401 has a gain of 8dB and a noise figure of 11dB.

An antialiasing, low-pass filter is positioned at the input of the ADC to limit the bandwidth of the input signal into the ADC. This amplifier also band-limits the front-end noise to prevent aliased noise from degrading the signal-to-noise ratio of the overall system. Design this filter for the maximum input signal bandwidth specified by the oscilloscope. The input bandwidth can then be reconfigured through the use of digital filters in the FPGA or ASIC to limit the oscilloscope input bandwidth to a bandwidth less than the maximum.

Table 8-2 lists a number of recommended amplifiers frequency ranges.

**Table 8-2. Recommended single ended to differential amplifiers**

| PART NUMBER | BANDWIDTH | POWER CONSUMPTION |
|---|---|---|
| THS4509 | 1.9GHz | 125mW |
| LMH5401 | 8GHz | 185mW |
| TRF1305 | 7GHz | 495mW |


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### 8.3.2 Application Performance Plots

The following shows a captured pulse response.

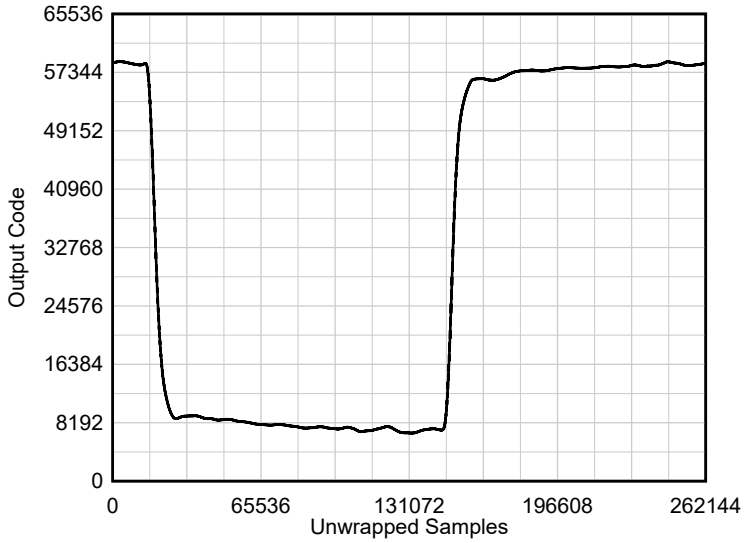



**Figure 8-9. 100MHz Pulse response**

## 8.4 Initialization Set Up

After power-up, the internal registers must be initialized to the default values through a hardware reset by applying a low pulse on the $\overline{\text{RESET}}$ pin, as shown in Figure 8-10. Any given power rail needs to reach 90% of the value before starting the next power rail.

1. Apply 0.9V DVDD09 digital power supply
2. Apply 1.2V AVDD12 and CLKVDD12 power supplies
3. Apply 1.8V power supplies (AVDD18, GPIOVDD18, DVDD18), in no specific order
4. Apply sampling clock
5. Apply hardware reset. After hardware reset is released, the default registers are loaded from internal fuses.
6. Start programming the internal registers using the SPI register writes. The internal calibration starts automatically and a register can be read back to check the status of the calibration.

For power down, the inverse sequence can be followed.

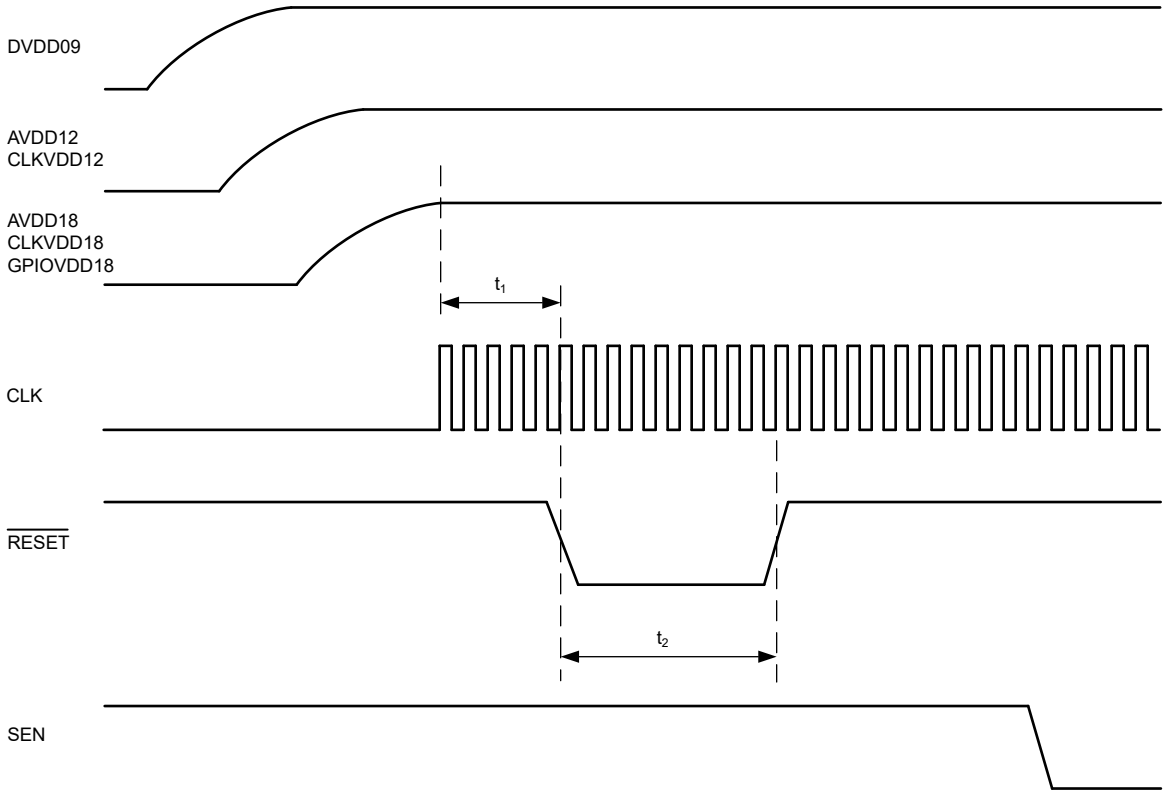



**Figure 8-10. Initialization of Serial Registers After Power-Up**

**Table 8-3. Power Up Timing**

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_1$ | Power-on delay: delay from power up to active low RESET pulse | 1 | | | us |
| $t_2$ | Reset pulse width: active low RESET pulse width | 100 | | | ns |


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## 8.5 Power Supply Recommendations

The device requires 3 different power supply voltages: the internal analog circuitry operate off 1.8V and 1.2V rails while the digital logic uses a 0.9V rail. Figure 8-11 shows a typical power supply example using a switching regulator for the digital 0.9V supply and low noise LDOs for the analog supplies. The voltage regulators must be sequenced for both power up and power down as shown in Section 8.4.

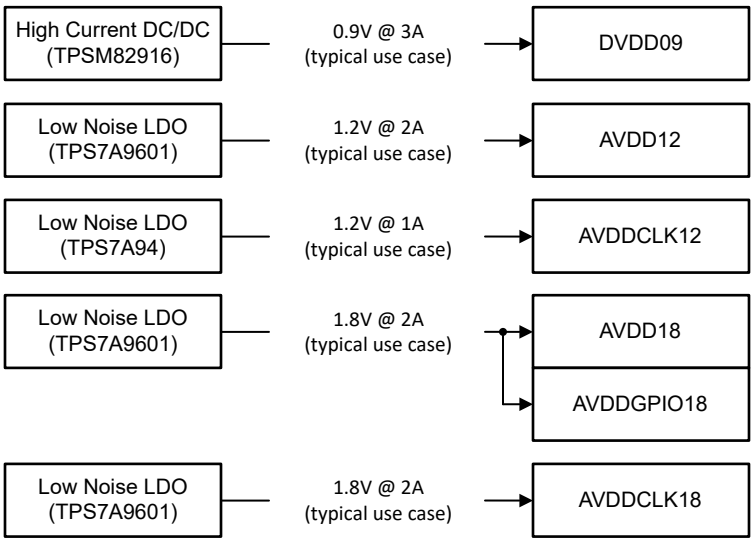



**Figure 8-11. Power supply rails and regulator examples**

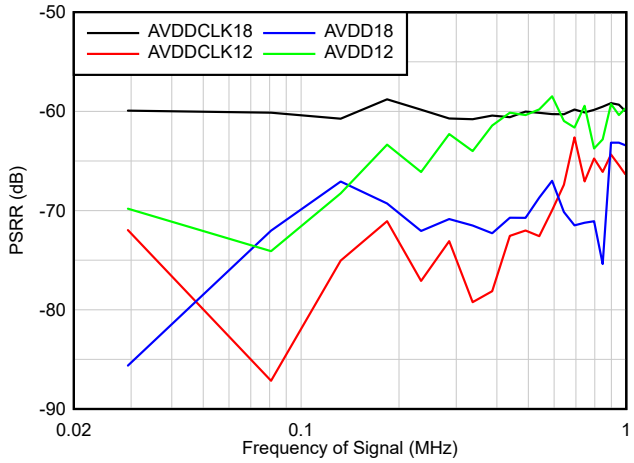



**Figure 8-12. PSRR**

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## 8.6 Layout

### 8.6.1 Layout Guidelines

There are several critical signals which require specific care during board design:

1. Analog input and clock signals
   - Traces must be as short as possible and vias must be avoided where possible to minimize impedance discontinuities.
   - Traces must be routed using loosely coupled 100Ω differential traces.
   - Differential trace lengths must be matched as close as possible to minimize phase imbalance and HD2 degradation.
2. Digital JESD204B/C output interface
   - Traces must be routed using tightly coupled 100Ω differential traces.
3. Power and ground connections
   - Provide low resistance connection paths to all power and ground pins.
   - Use power and ground planes instead of traces.
   - Avoid narrow, isolated paths which increase the connection resistance.
   - Use a signal/ground/power circuit board stackup to maximize coupling between the ground and power plane.

### 8.6.2 Layout Example

The following screen shots show the top and bottom layer of the ADC32RF7x EVM.

- The input signal traces are routed as differential, tightly coupled traces on the top layer of the EVM. Care is taken to maintain symmetry between positive and negative input with matched trace length to minimize phase imbalance. Similar for the sampling clock input.
- JESD204B/C output interface lanes are routed differential and length matched on the top layer.
- Bypass caps are close to the power pins on the bottom layer.

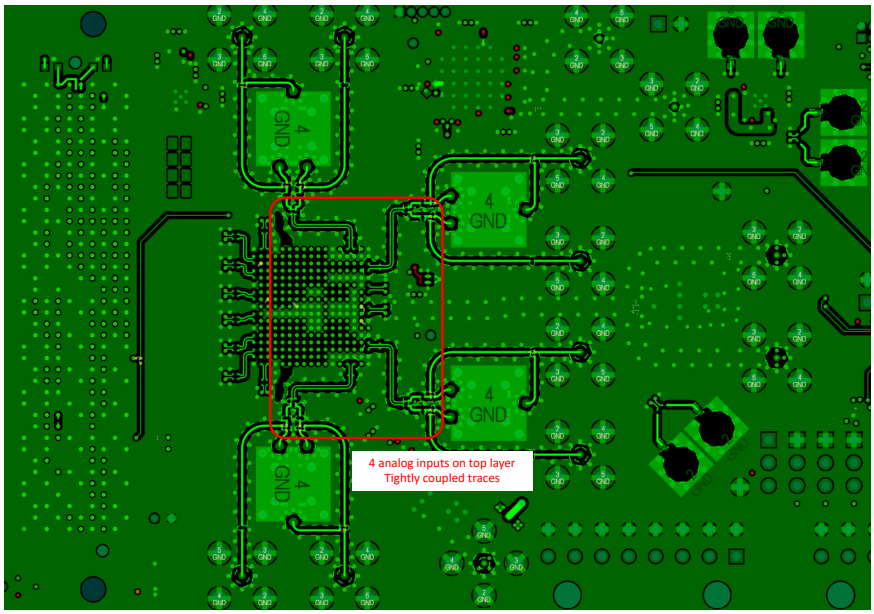



**Figure 8-13. Top Layer**


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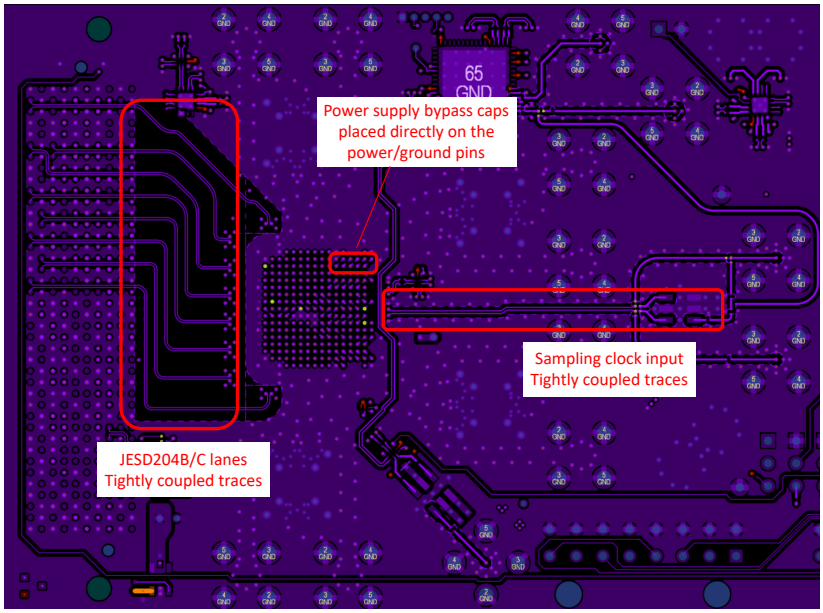



**Figure 8-14. Bottom Layer**

# 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 9.1 Documentation Support

### *9.1.1 Related Documentation*

- Texas Instruments, *Evaluating High-Speed, RF ADC Converter Front-end Architectures* application note

### *9.1.2 Third-Party Products Disclaimer*

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## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| November 2025 | * | Initial Release |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ADC32RF72IANH | Active | Production | FCCSP (ANH) \| 289 | 119 \| JEDEC TRAY (5+1) | Yes | Call TI \| Other | Level-3-260C-168 HR | -40 to 105 | ADC32RF72 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

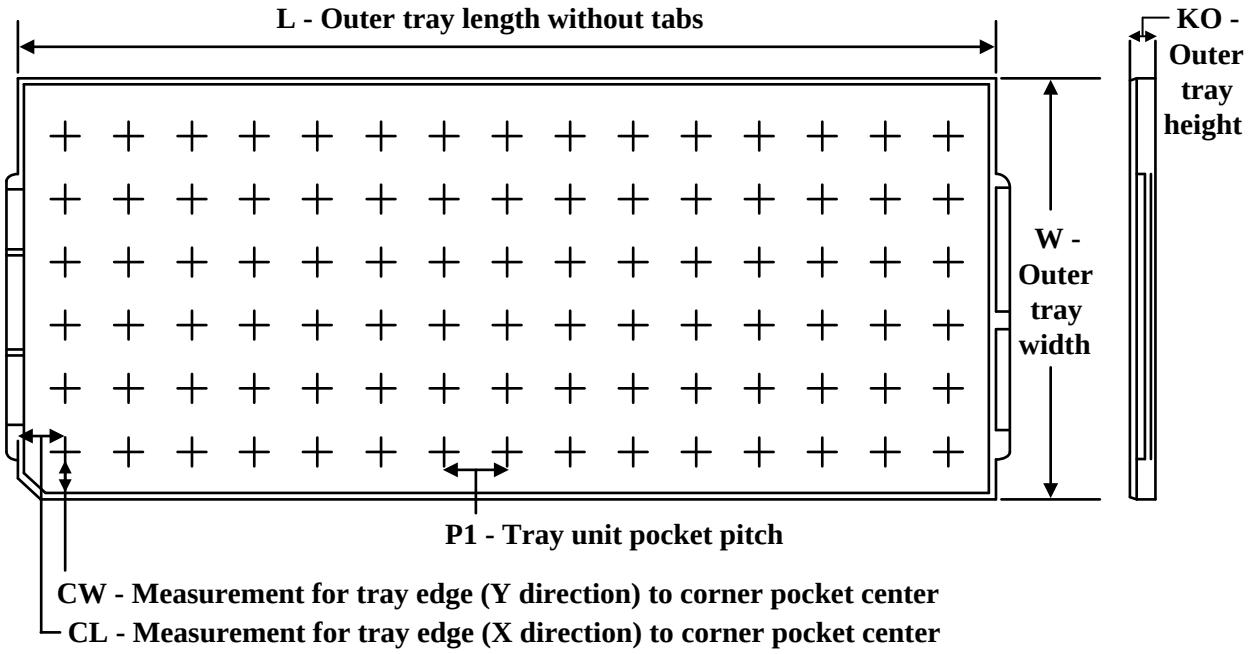
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

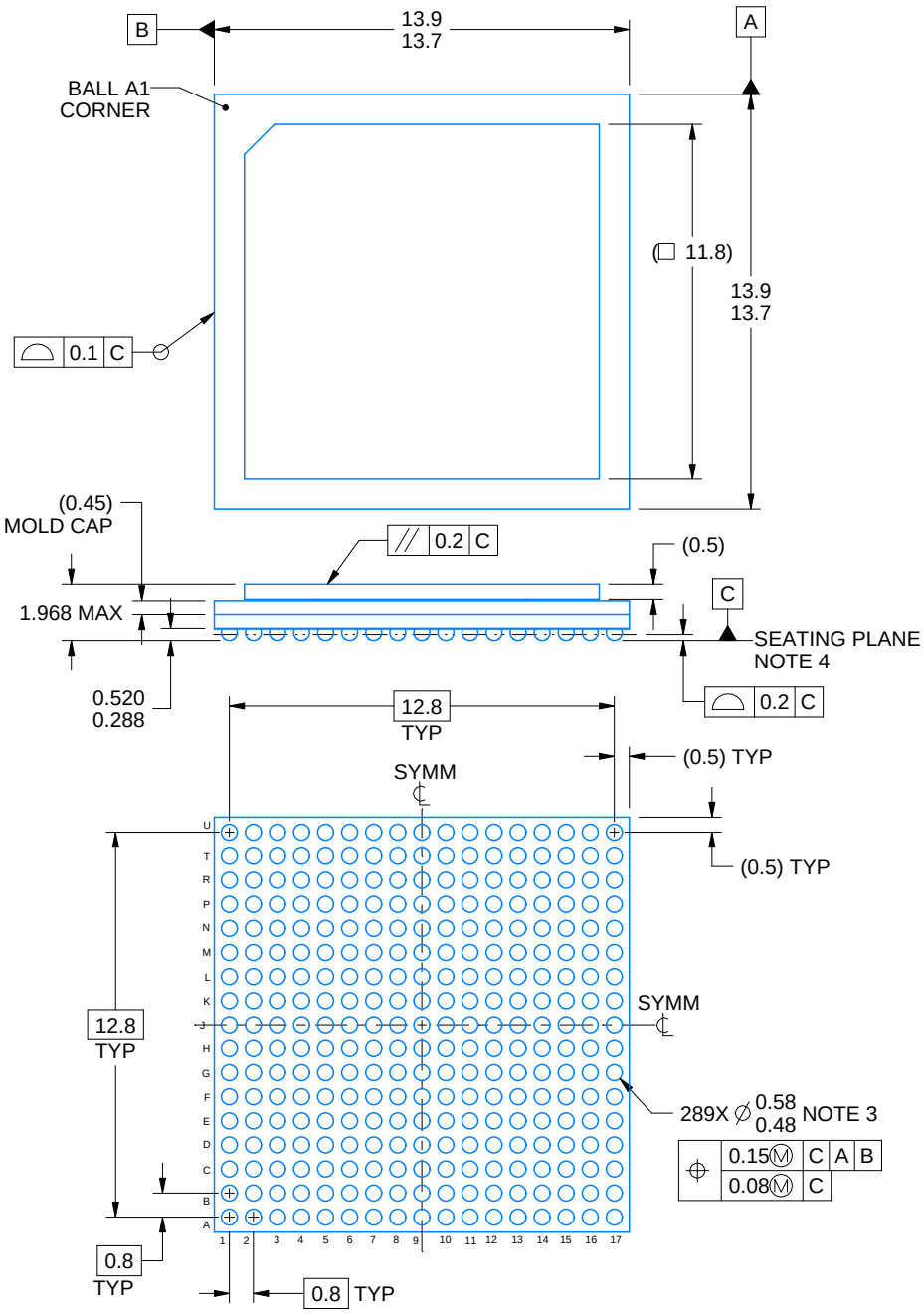
| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC32RF72IANH | ANH | FCCSP | 289 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 18.1 | 12.7 | 12.9 |
| ADC32RF72IANH | ANH | FCCSP | 289 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 18.1 | 12.7 | 12.9 |

# PACKAGE OUTLINE

## ANH0289A

## FCCSP - 1.968 mm max height

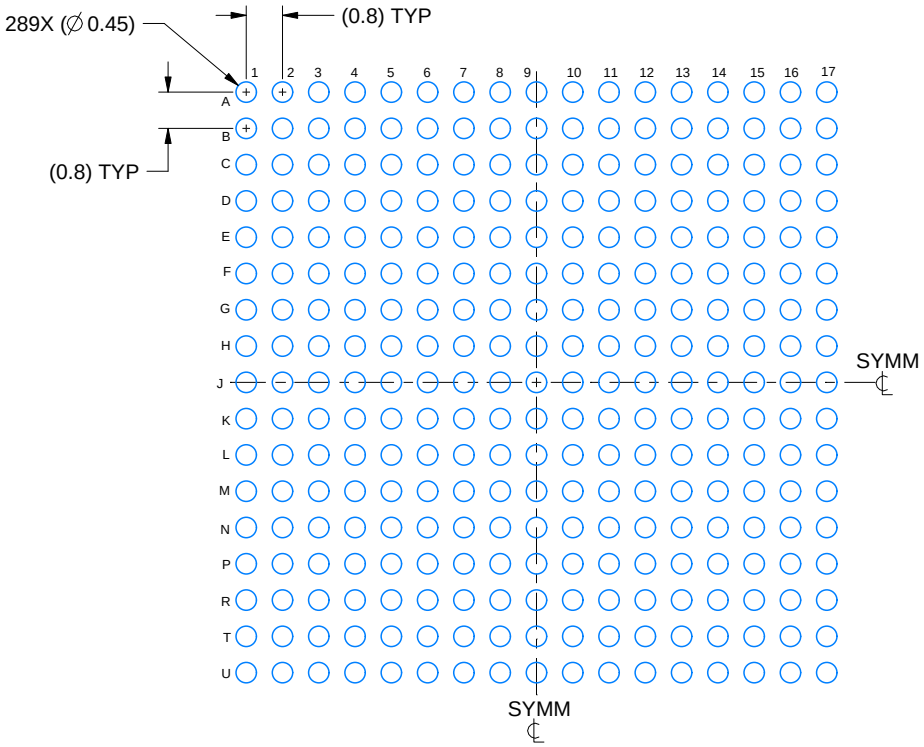
BALL GRID ARRAY



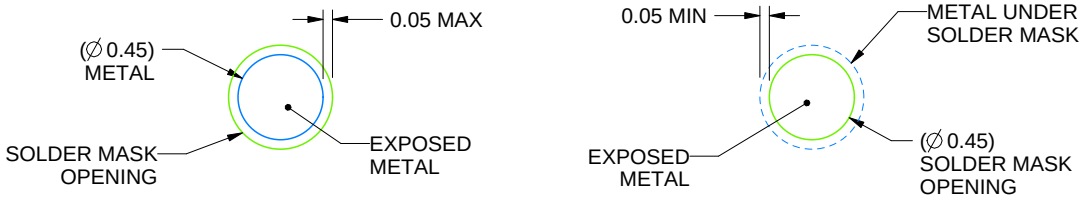

4230247/C 03/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, post reflow, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 6X

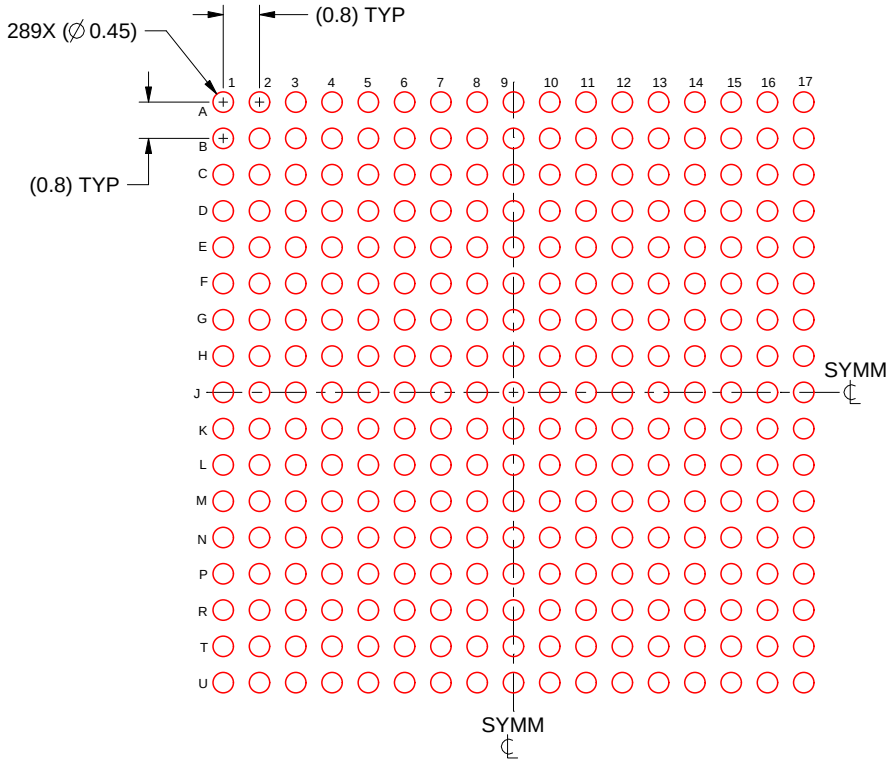



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

5. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SPRU811 (www.ti.com/lit/spru811).




SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 6X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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