ADC12L063 12-Bit, 62 MSPS, 354 mW A/D Converter with Internal Sample-and-Hold

Check for Samples: ADC12L063

FEATURES

- **Single Supply Operation**
- **Low Power Consumption**
- **Power Down Mode**
- **On-Chip Reference Buffer**

APPLICATIONS

- **Ultrasound and Imaging**
- **Instrumentation**
- **Cellular Base Stations/Communications Receivers**
- **Sonar/Radar**
- **xDSL**
- **Wireless Local Loops**
- **Data Acquisition Systems**
- **DSP Front Ends**

KEY SPECIFICATIONS

- **Resolution: 12 Bits**
- **Conversion Rate: 62 MSPS (min)**
- **Bandwidth: 170 MHz**
- **DNL: ±0.5 LSB(typ)**
- **INL: ±1.0 LSB(typ)**
- **SNR: 66 dB(typ)**
- **SFDR: 78 dB(typ)**
- **Data Latency: 6 Clock Cycles**
- **Supply Voltage: +3.3V ± 300 mV**
- **Power Consumption, 62 MHz: 354 mW(typ)**

DESCRIPTION

The ADC12L063 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 62 Megasamples per second (MSPS), minimum. This converter uses a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize die size and power consumption while providing excellent dynamic performance. Operating on a single 3.3V power supply, this device consumes just 354 mW at 62 MSPS, including the reference current. The Power Down feature reduces power consumption to just 50 mW.

The differential inputs provide a full scale input swing equal to $\pm V_{REF}$ with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. For ease of use, the buffered, high impedance, single-ended reference input is converted on-chip to a differential reference for use by the processing circuitry. Output data format is 12-bit offset binary.

This device is available in the 32-lead LQFP package and will operate over the industrial temperature range of −40°C to +85°C.

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Connection Diagram

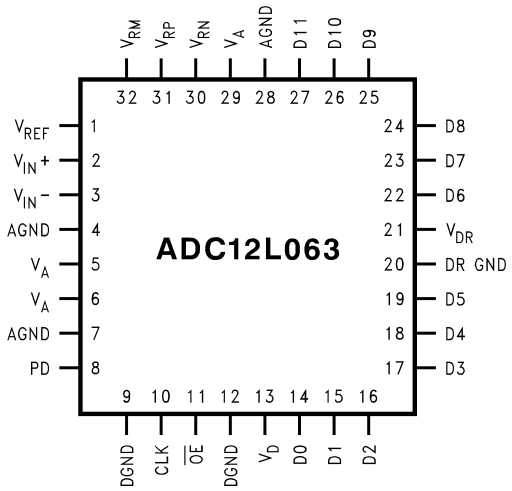

Figure 1. 32-Lead LQFP
See NEY0032A Package

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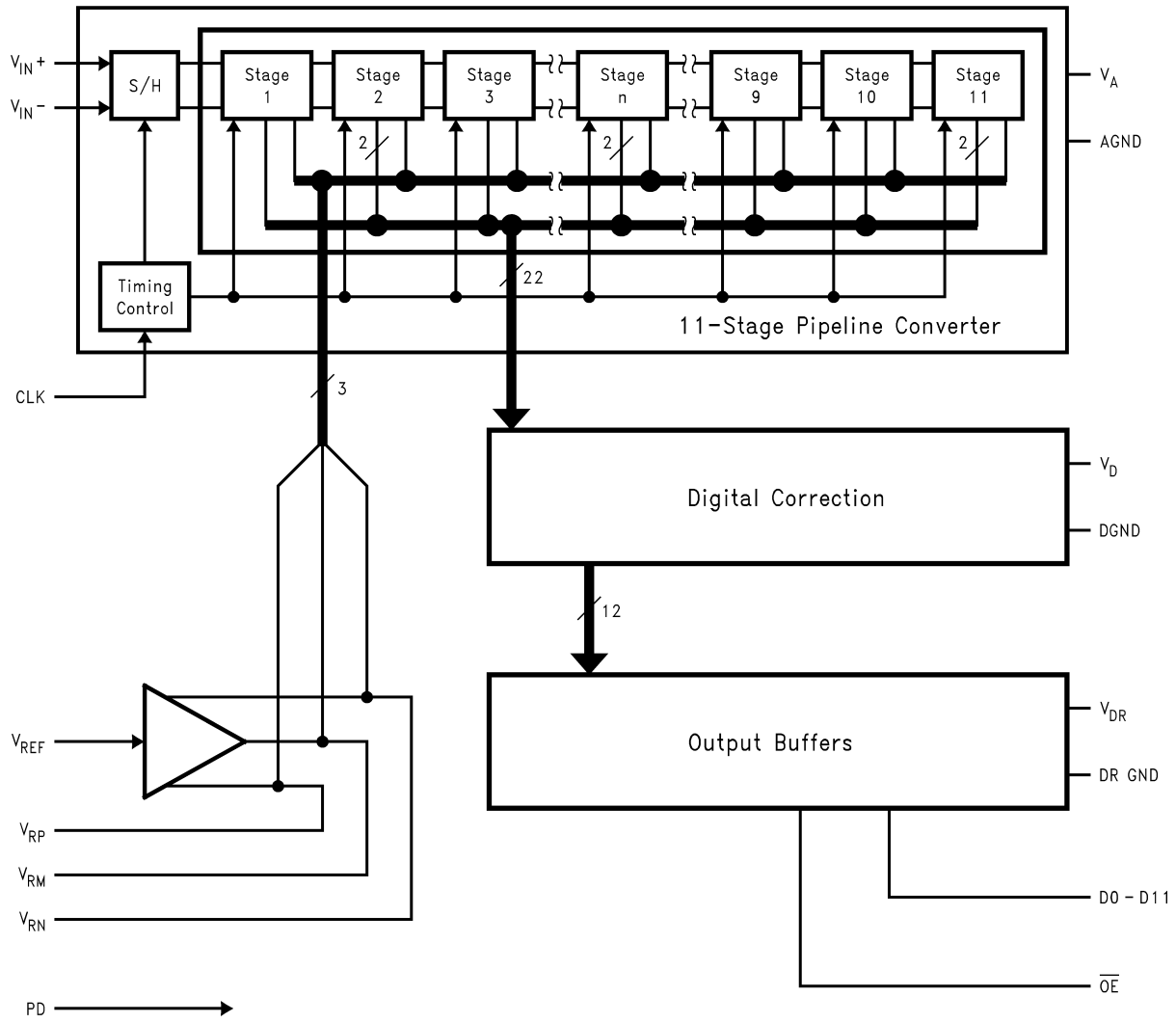
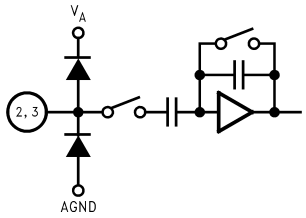
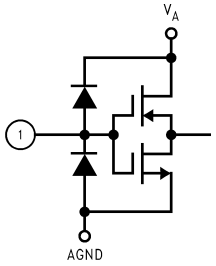
Block Diagram



PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
2	V_{IN}^+		Non-Inverting analog signal Input. With a 1.0V reference voltage the input signal level is 1.0 V_{P-P}.
3	V_{IN-}		Inverting analog signal Input. With a 1.0V reference voltage the input signal level is 1.0 V_{P-P}. This pin may be connected to V_{CM} for single-ended operation, but a differential input signal is required for best performance.
1	V_{REF}		Reference input. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. V_{REF} is 1.0V nominal and should be between 0.8V and 1.2V.

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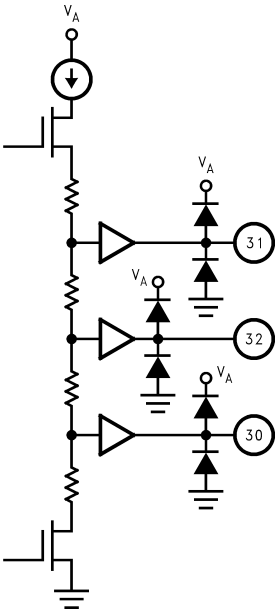
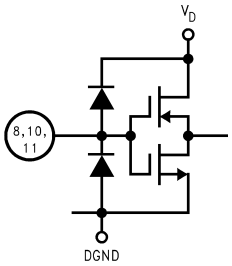
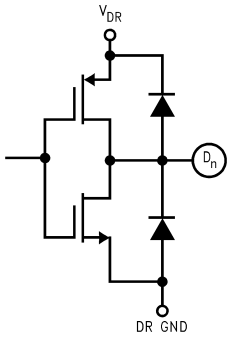
PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS (continued)

Pin No.	Symbol	Equivalent Circuit	Description
31	V_{RP}		These pins are high impedance reference bypass pins only. Connect a 0.1 µF capacitor from each of these pins to AGND. DO NOT connect anything else to these pins.
32	V_{RM}		
30	V_{RN}		
DIGITAL I/O			
10	CLK		Digital clock input. The range of frequencies for this input is 1 MHz to 70 MHz (typical) with specified performance at 62 MHz. The input is sampled on the rising edge of this input.
11	$\overline{OE}$		$\overline{OE}$ is the output enable pin that, when low, enables the TRI-STATE data output pins. When this pin is high, the outputs are in a high impedance state.
8	PD		PD is the Power Down input pin. When high, this input puts the converter into the power down mode. When this pin is low, the converter is in the active mode.
14–19, 22–27	D0–D11		Digital data output pins that make up the 12-bit conversion results. D0 is the LSB, while D11 is the MSB of the offset binary output word.
ANALOG POWER			
5, 6, 29	V_A		Positive analog supply pins. These pins should be connected to a quiet +3.3V source and bypassed to AGND with 0.1 µF monolithic capacitors located within 1 cm of these power pins, and with a 10 µF capacitor.
4, 7, 28	AGND		The ground return for the analog supply.
DIGITAL POWER			
13	V_D		Positive digital supply pin. This pin should be connected to the same quiet +3.3V source as is V_A and bypassed to DGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor, both located within 1 cm of the power pin. Decouple this pin from the V_A pins.
9, 12	DGND		The ground return for the digital supply.

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PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS (continued)

Pin No.	Symbol	Equivalent Circuit	Description
21	V_{DR}		Positive digital supply pin for the ADC12L063's output drivers. This pin should be connected to a voltage source of +2.5V to V_D and bypassed to DR GND with a 0.1 µF monolithic capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF tantalum capacitor. The voltage at this pin should never exceed the voltage on V_D. All bypass capacitors should be located within 1 cm of the supply pin.
20	DR GND		The ground return for the digital supply for the ADC12L063's output drivers. This pin should be connected to the system digital ground, but not be connected in close proximity to the ADC12L063's DGND or AGND pins. See LAYOUT AND GROUNDING for more details.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

V_A, V_D, V_{DR}		4.2V
$\|V_A – V_D\|$		≤ 100 mV
Voltage on Any Input or Output Pin		−0.3V to V_A or V_D +0.3V
Input Current at Any Pin (4)		±25 mA
Package Input Current (4)		±50 mA
Package Dissipation at T_A = 25°C		See (5)
ESD Susceptibility	Human Body Model (6)	2500V
	Machine Model (6)	250V
Soldering Temperature, Infrared, 10 sec. (7)		235°C
Storage Temperature		−65°C to +150°C

(1) All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A, V_D or V_{DR}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. In the 32-pin LQFP, θ_{JA} is 79°C/W, so P_DMAX = 1,582 mW at 25°C and 823 mW at the maximum operating ambient temperature of 85°C. Note that the power consumption of this device under normal operation will typically be about 374 mW (354 typical power consumption + 20 mW TTL output loading). The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.
(7) The 235°C reflow temperature refers to infrared reflow. For Vapor Phase Reflow (VPR), the following Conditions apply: Maintain the temperature at the top of the package body above 183°C for a minimum 60 seconds. The temperature measured on the package body must not exceed 220°C. Only one excursion above 183°C is allowed per reflow cycle.

Operating Ratings (1)(2)

Operating Temperature	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_A, V_D)	+3.0V to +3.60V
Output Driver Supply (V_{DR})	+2.5V to V_D
V_{REF} Input	0.8V to 1.2V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

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Operating Ratings (1)(2) (continued)

CLK, PD, $\overline{OE}$	−0.05V to V_D + 0.05V
V_{IN} Input	−0V to (V_A − 0.5V)
|AGND–DGND|	≤100mV

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Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = V_{DR} = +3.3V, PD = 0V, V_{REF} = +1.0V, f_{CLK} = 62 MHz, t_r = t_f = 2 ns, C_L = 20 pF/pin. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}:** all other limits T_A = T_J = 25°C (1)(2)(3)

Symbol	Parameter	Conditions		Typical (4)	Limits (4)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits
INL	Integral Non Linearity (5)			±1.0	**±2.4**	LSB(max)
DNL	Differential Non Linearity			±0.5		LSB(max)
GE	Gain Error	Positive Error		−0.8		%FS(max)
		Negative Error		+0.1	**±3**	%FS(max)
	Offset Error (V_{IN}+ = V_{IN}−)			+0.1	**±0.9**	%FS(max)
	Under Range Output Code			0	**0**	
	Over Range Output Code			4095	**4095**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{CM}	Common Mode Input Voltage			1.0		V
C_{IN}	V_{IN} Input Capacitance (each pin to GND)	V_{IN} = 1.0 Vdc + 1 V_{P-P}	(CLK LOW)	8		pF
			(CLK HIGH)	7		pF
V_{REF}	Reference Voltage (6)			1.00	**0.8** **1.2**	V(min) V(max)
	Reference Input Resistance			100		MΩ(min)

(1) The inputs are protected as shown below. Input voltages above V_A or below GND will not damage this device, provided current is limited per Note 4 under the Absolute Maximum Ratings Table. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 3.3V, the full-scale input voltage must be ≤3.4V to ensure accurate conversions. See Figure 2
(2) To ensure accuracy, it is required that $|V_A – V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-bit LSB is 488 µV.
(4) Typical figures are at T_A = T_J = 25°C, and represent most likely parametric norms. Test limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive and negative full-scale.
(6) Optimum dynamic performance will be obtained by keeping the reference input in the 0.8V to 1.2V range. The LM4051CIM3-ADJ or the LM4051CIM3-1.2 bandgap voltage reference is recommended for this application.

DC and Logic Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D= V_{DR} = +3.3V, PD = 0V, V_{REF} = +1.0V, f_{CLK} = 62 MHz, t_r = t_f = 2 ns, C_L = 20 pF/pin. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}:** all other limits T_A = T_J = 25°C (1)(2)(3)

Symbol	Parameter	Conditions	Typical (4)	Limits (4)	Units (Limits)
CLK, PD, $\overline{OE}$ DIGITAL INPUT CHARACTERISTICS					
$V_{IN(1)}$	Logical “1” Input Voltage	V_D = 3.3V		**2.0**	V(min)
$V_{IN(0)}$	Logical “0” Input Voltage	V_D = 3.0V		**0.8**	V(max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN}^+, V_{IN}^- = 3.3V	10		µA
$I_{IN(0)}$	Logical “0” Input Current	V_{IN}^+, V_{IN}^- = 0V	−10		µA
C_{IN}	Digital Input Capacitance		5		pF
D0–D11 DIGITAL OUTPUT CHARACTERISTICS					

(1) The inputs are protected as shown below. Input voltages above V_A or below GND will not damage this device, provided current is limited per Note 4 under the Absolute Maximum Ratings Table. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 3.3V, the full-scale input voltage must be ≤3.4V to ensure accurate conversions. See Figure 2
(2) To ensure accuracy, it is required that $|V_A – V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-bit LSB is 488 µV.
(4) Typical figures are at T_A = T_J = 25°C, and represent most likely parametric norms. Test limits are specified to TI's AOQL (Average Outgoing Quality Level).

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DC and Logic Electrical Characteristics (continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = V_{DR}$ = +3.3V, PD = 0V, V_{REF} = +1.0V, f_{CLK} = 62 MHz, $t_r = t_f$ = 2 ns, C_L = 20 pF/pin. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_A = T_J$ = 25°C (1)(2)(3)

Symbol	Parameter	Conditions	Typical (4)	Limits (4)	Units (Limits)
$V_{OUT(1)}$	Logical "1" Output Voltage	I_{OUT} = −0.5 mA		**2.7**	V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_{OUT} = 1.6 mA		**0.4**	V(max)
I_{OZ}	TRI-STATE Output Current	V_{OUT} = 3.3V	100		nA
		V_{OUT} = 0V	−100		nA
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V	−20		mA(min)
$-I_{SC}$	Output Short Circuit Sink Current	$V_{OUT} = V_{DR}$	20		mA(min)
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD Pin = DGND, V_{REF} = 1.0V PD Pin = V_{DR}	102 4	**140**	mA(max) mA
I_D	Digital Supply Current	PD Pin = DGND PD Pin = V_{DR}, f_{CLK} = 0	5.3 2	**7**	mA(max) mA
I_{DR}	Digital Output Supply Current	PD Pin = DGND, (5) PD Pin = V_{DR}, f_{CLK} = 0	<1 0		mA(max) mA
	Total Power Consumption	PD Pin = DGND, C_L = 0 pF (6) PD Pin = V_{DR}, f_{CLK} = 0	354 50	**485**	mW mW
PSRR1	Power Supply Rejection	Rejection of Full-Scale Error with V_A = 3.0V vs 3.6V	58		dB
PSRR2	Power Supply Rejection	SNR Degradation w/10 MHz, 250 mV_{P-P} riding on V_A	−53		dB
DYNAMIC CONVERTER CHARACTERISTICS					
BW	Full Power Bandwidth	0 dBFS Input, Output at −3 dB	170		MHz
SNR	Signal-to-Noise Ratio	f_{IN} = 1 MHz, Differential V_{IN} = −0.5 dBFS	66		dB
		f_{IN} = 10 MHz, Differential V_{IN} = −0.5 dBFS	66	**63.3**	dB(min)
SINAD	Signal-to-Noise and Distortion	f_{IN} = 1 MHz, Differential V_{IN} = −0.5 dBFS	65		dB
		f_{IN} = 10 MHz, Differential V_{IN} = −0.5 dBFS	65	**62**	dB
ENOB	Effective Number of Bits	f_{IN} = 1 MHz, Differential V_{IN} = −0.5 dBFS	10.6		Bits
		f_{IN} = 10 MHz, Differential V_{IN} = −0.5 dBFS	10.3	**10.0**	Bits
THD	Total Hamonic Distortion	f_{IN} = 1 MHz, Differential V_{IN} = −0.5 dBFS	−80		dB
		f_{IN} = 10 MHz, Differential V_{IN} = −0.5 dBFS	−74	**−65**	dB(max)
SFDR	Spurious Free Dynamic Range	f_{IN} = 1 MHz, Differential V_{IN} = −0.5 dBFS	82		dB
		f_{IN} = 10 MHz, Differential V_{IN} = −0.5 dBFS	78		dB(min)
IMD	Intermodulation Distortion	f_{IN} = 9.5 MHz and 10.5 MHz, each = −7 dBFS	−75		dBFS

(5) I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent). $I_{DR} = V_{DR}(C_0 \times f_0 + C_1 \times f_1 + ...C_{11} \times f_{11})$ where V_{DR} is the output driver power supply voltage, C_n is total capacitance on the output pin, and f_n is the average frequency at which that pin is toggling.

(6) Excludes I_{DR}. See Note 5.

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AC Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D$, V_{DR} = +3.3V, PD = 0V, V_{REF} = +1.0V, f_{CLK} = 62 MHz, $t_r = t_f$ = 2 ns, C_L = 20 pF/pin. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_A = T_J$ = 25°C (1)(2)(3)(4)

Symbol	Parameter	Conditions	Typical (5)	Limits (5)	Units (Limits)
f_{CLK}[1]	Maximum Clock Frequency		70	**62**	MHz(min)
f_{CLK}[2]	Minimum Clock Frequency		1		MHz
	Recommended Clock Duty Cycle		50	40	%(min)
				60	%(max)
t_{CH}	Clock High Time			**6.5**	ns(min)
t_{CL}	Clock Low Time			**6.5**	ns(min)
t_{CONV}	Conversion Latency			**6**	Clock Cycles
t_{OD}	Data Output Delay after Rising CLK Edge	V_{DR} = 2.5V	12		ns
		V_{DR} = 3.3V	9	**13**	ns(max)
t_{AD}	Aperture Delay		2		ns
t_{AJ}	Aperture Jitter		1.2		ps rms
t_{DIS}	Data outputs into TRI-STATE Mode		10		ns
t_{EN}	Data Outputs Active after TRI-STATE		10		ns
t_{PD}	Power Down Mode Exit Cycle		20		t_{CLK}

(1) The inputs are protected as shown below. Input voltages above V_A or below GND will not damage this device, provided current is limited per Note 4 under the Absolute Maximum Ratings Table. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 3.3V, the full-scale input voltage must be ≤3.4V to ensure accurate conversions. See Figure 2

(2) To ensure accuracy, it is required that $|V_A – V_D| \leq 100$ mV and separate bypass capacitors are used at each power supply pin.

(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-bit LSB is 488 µV.

(4) Timing specifications are tested at TTL logic levels, V_{IL} = 0.4V for a falling edge and V_{IH} = 2.4V for a rising edge.

(5) Typical figures are at $T_A = T_J$ = 25°C, and represent most likely parametric norms. Test limits are specified to TI's AOQL (Average Outgoing Quality Level).

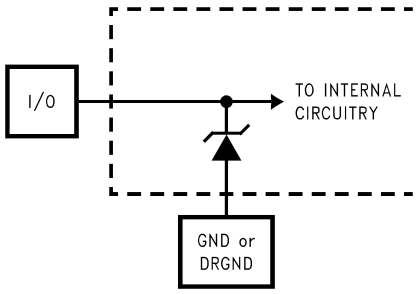

Figure 2.

Specification Definitions

APERTURE DELAY is the time after the rising edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

COMMON MODE VOLTAGE (V_{CM}) is the d.c. potential present at both signal inputs to the ADC.

CONVERSION LATENCY See PIPELINE DELAY.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB

DUTY CYCLE s the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error − Offset Error (1)

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC12L063 is ensured not to have any missing codes.

NEGATIVE FULL SCALE ERROR is the difference between the input voltage ($V_{IN}^+ - V_{IN}^-$) just causing a transition from negative full scale to the next code and its ideal value of 0.5 LSB.

OFFSET ERROR is the difference between the ideal differential input voltage ($V_{IN}^+ - V_{IN}^- = 0V$) and the actual input voltage required to cause a transition from an output code 2047 to 2048.

OUTPUT DELAY is the time delay after the rising edge of the clock before the data update is presented at the output pins.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC12L063, PSRR1 is the ratio of the change in Full-Scale Error that results from a change in the dc power supply voltage, expressed in dB. PSRR2 is a measure of how well an a. c. signal riding upon the power supply is rejected at the output.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or dc.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of

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the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB or dBc, of the rms total of the first nine harmonic levels at the output to the rms value of the input frequency at the output. It is calculated as

$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_{10}^2}{f_1^2}} \quad (2)$$

where

- f_1 is the fundamental (input) frequency
- f_2 through f_{10} are the first 9 harmonic frequencies.

Timing Diagram

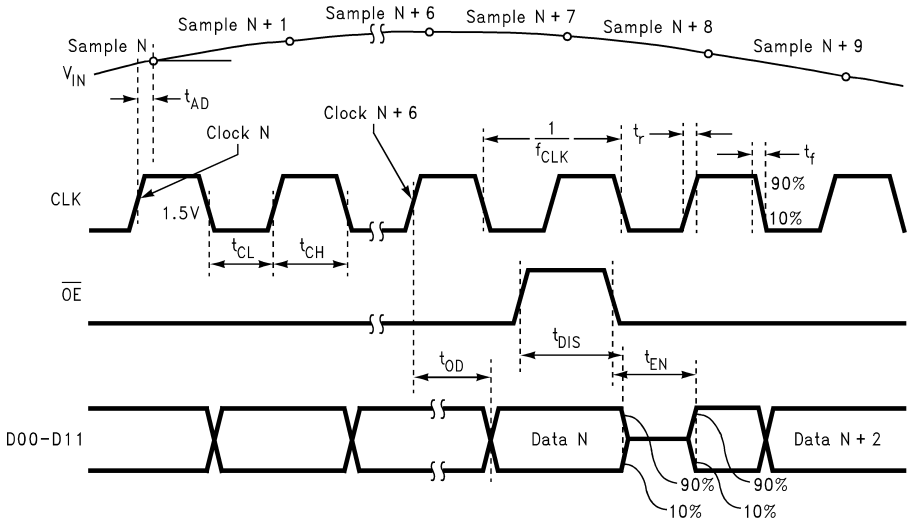

Figure 3. Output Timing

Transfer Characteristic

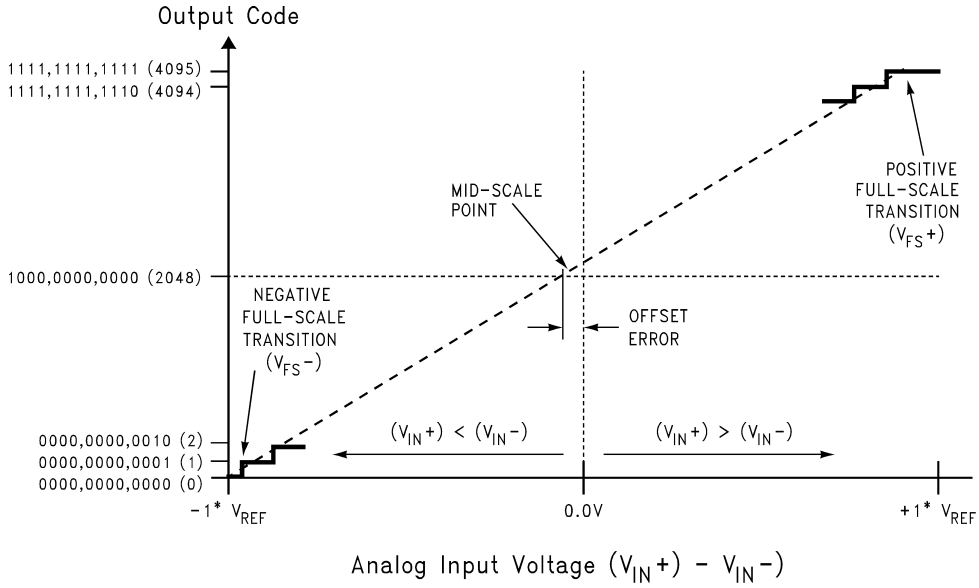

Figure 4. Transfer Characteristic

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Typical Performance Characteristics

$V_A = V_D = V_{DR} = 3.3V$, $f_{CLK} = 62MHz$, $f_{IN} = 10$ MHz unless otherwise stated

DNL vs. V_A

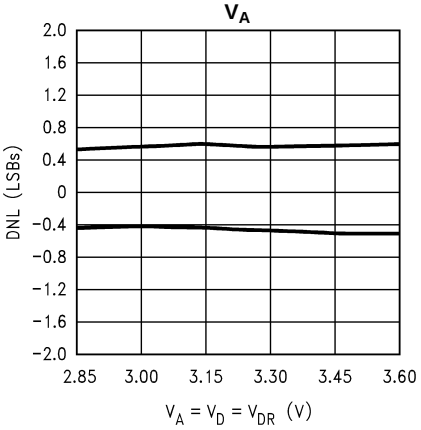

Figure 5.

DNL vs. Clock Duty Cycle

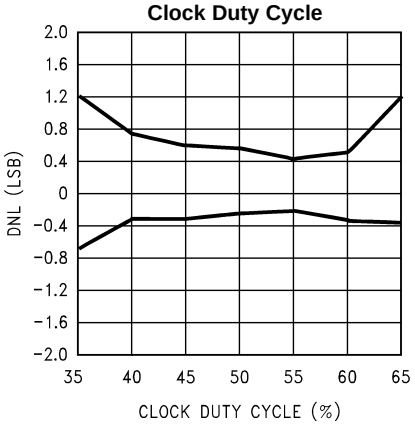

Figure 6.

DNL vs. Temperature

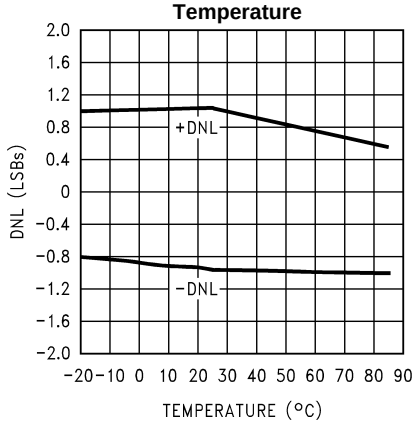

Figure 7.

INL vs. V_A

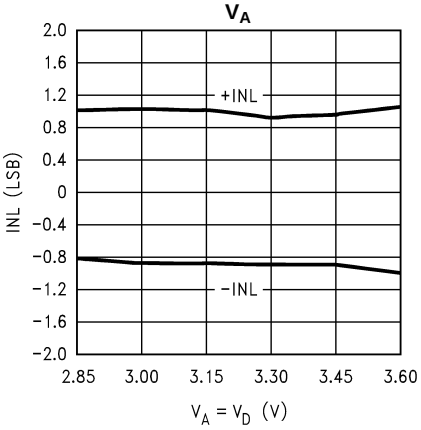

Figure 8.

INL vs. Clock Duty Cycle

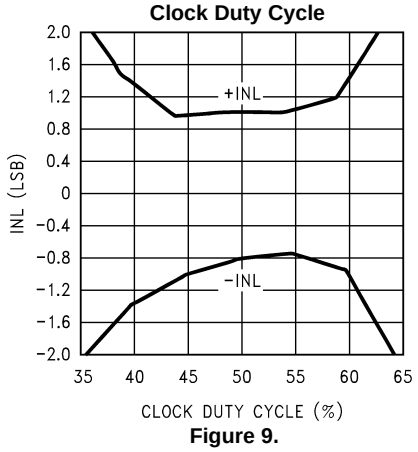

Figure 9.

INL vs. Temperature

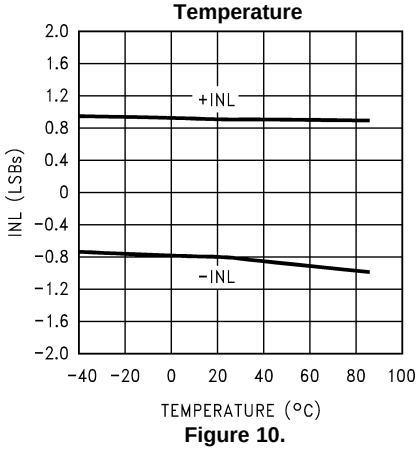

Figure 10.

Typical Performance Characteristics (continued)

$V_A = V_D = V_{DR} = 3.3V$, $f_{CLK} = 62MHz$, $f_{IN} = 10$ MHz unless otherwise stated

SNR vs. V_A

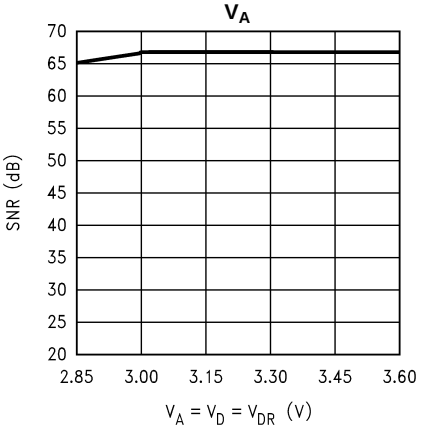

Figure 11.

SNR vs. f_{CLK}

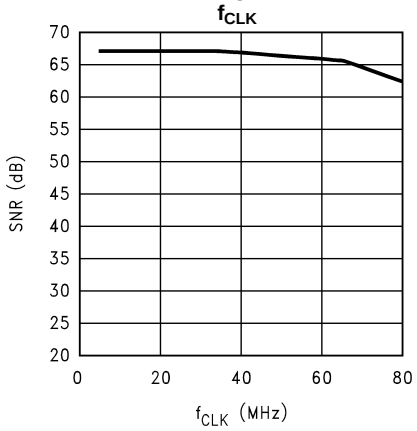

Figure 12.

SNR vs. Clock Duty Clock Cycle

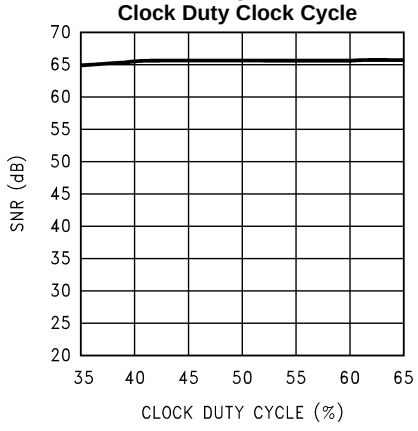

Figure 13.

SNR vs. V_{REF}

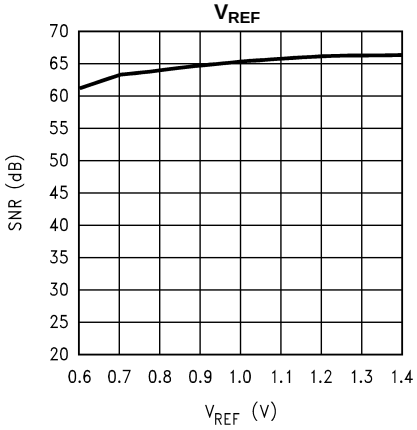

Figure 14.

SNR vs. Temperature

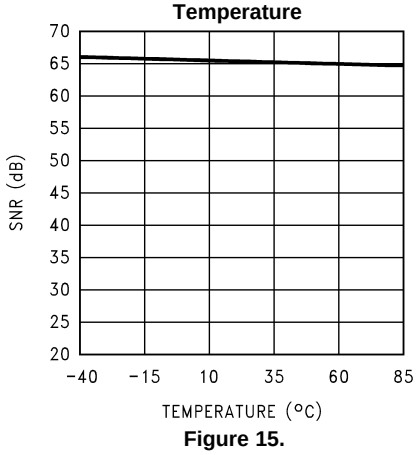

Figure 15.

THD vs. V_A

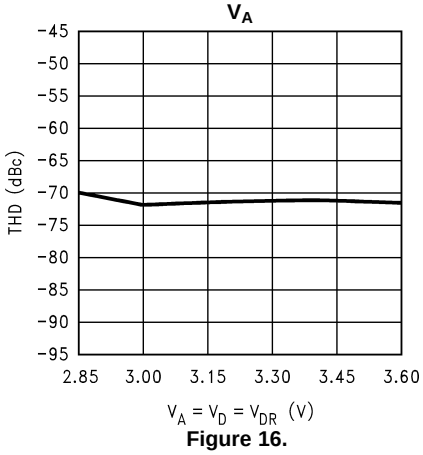

Figure 16.

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Typical Performance Characteristics (continued)

$V_A = V_D = V_{DR} = 3.3V$, $f_{CLK} = 62MHz$, $f_{IN} = 10$ MHz unless otherwise stated

THD vs. f_{CLK}

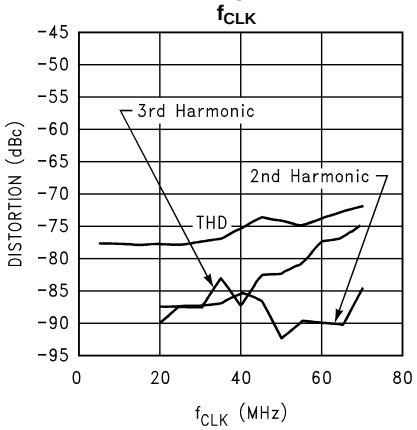

Figure 17.

THD vs. Clock Duty Cycle

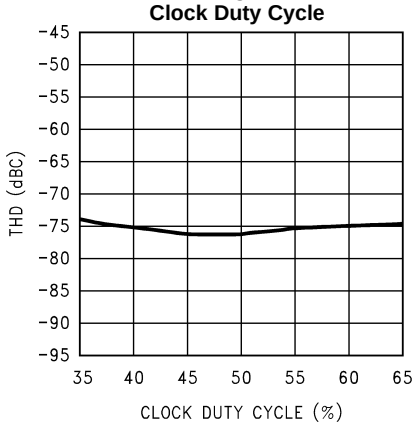

Figure 18.

THD vs. V_{REF}

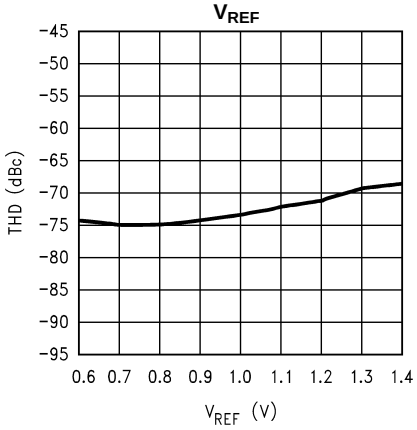

Figure 19.

THD vs. Temperature

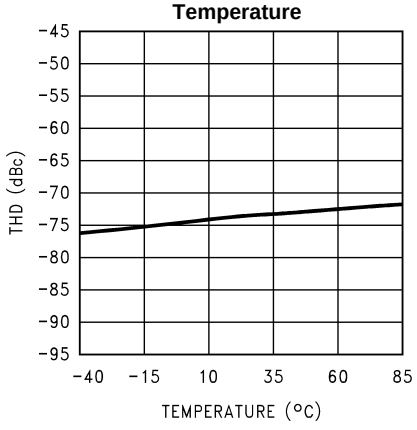

Figure 20.

SINAD vs. V_A

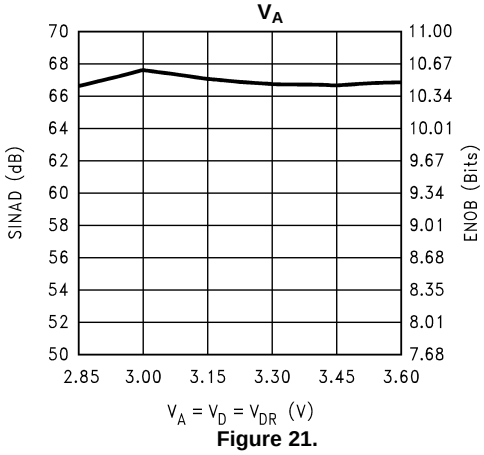

Figure 21.

SINAD vs. f_{CLK}

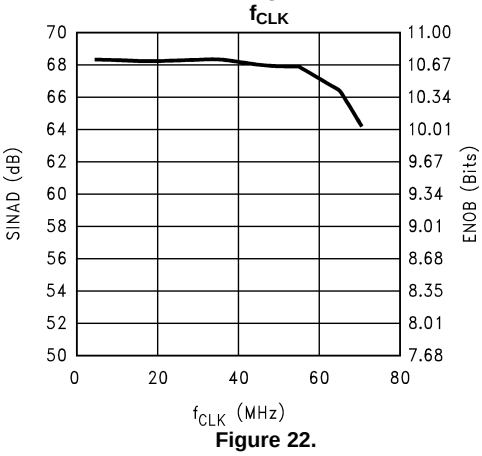

Figure 22.

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Typical Performance Characteristics (continued)

$V_A = V_D = V_{DR} = 3.3V$, $f_{CLK} = 62MHz$, $f_{IN} = 10$ MHz unless otherwise stated

SINAD vs. Duty Cycle

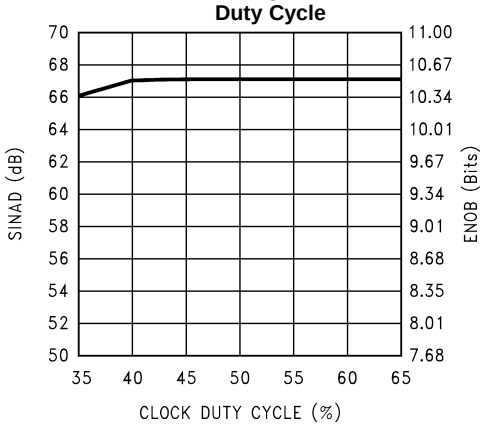

Figure 23.

SINAD vs. V_{REF}

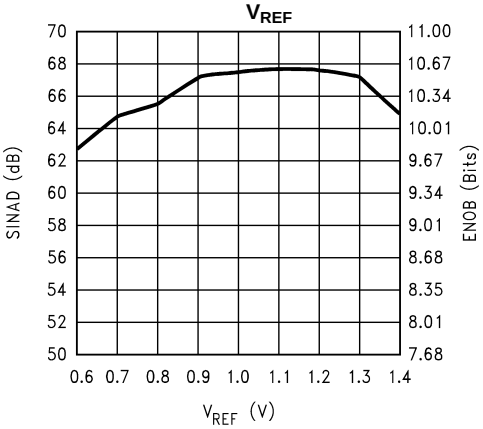

Figure 24.

SINAD vs. Temperature

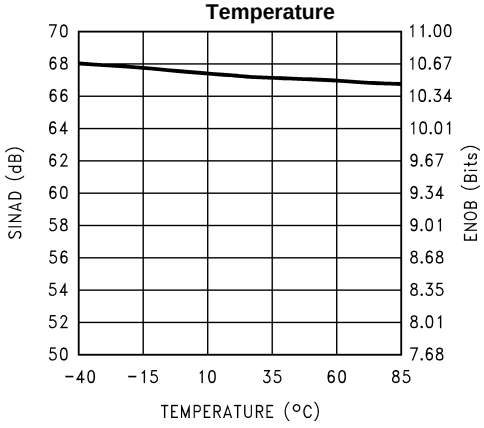

Figure 25.

SFDR vs. V_A

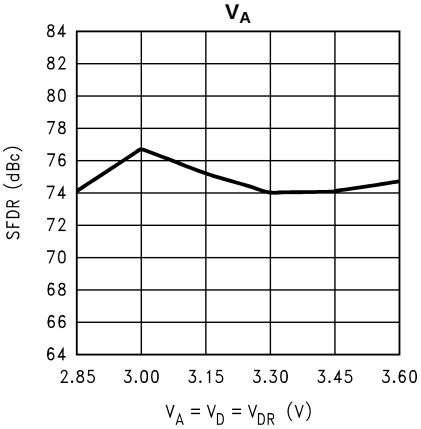

Figure 26.

SFDR vs. f_{CLK}

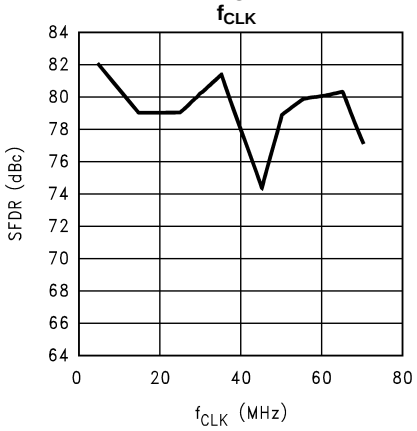

Figure 27.

SFDR vs. Duty Cycle

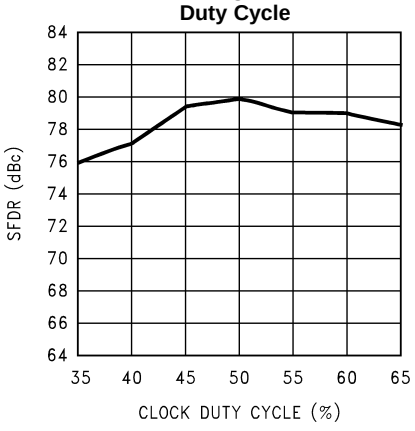

Figure 28.

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Typical Performance Characteristics (continued)

$V_A = V_D = V_{DR} = 3.3V$, $f_{CLK} = 62MHz$, $f_{IN} = 10$ MHz unless otherwise stated

SFDR vs. V_{REF}

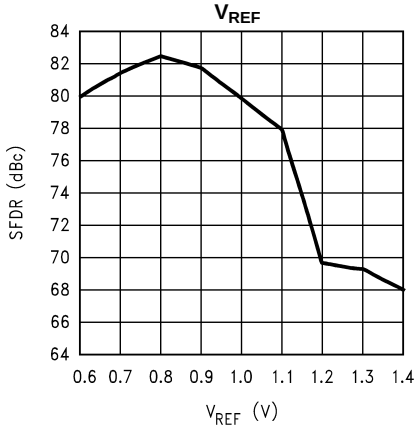

Figure 29.

SFDR vs. Temperature

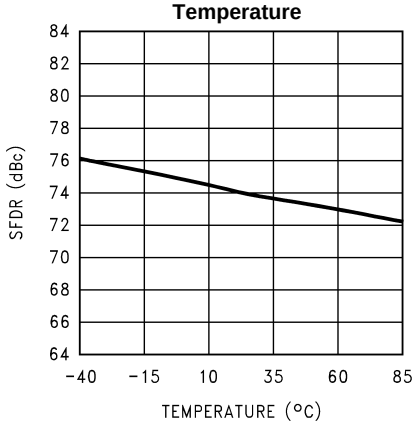

Figure 30.

FUNCTIONAL DESCRIPTION

Operating on a single +3.3V supply, the ADC12L063 uses a pipelined architecture and has error correction circuitry to help ensure maximum performance.

Differential analog input signals are digitized to 12 bits. Each analog input signal should have a peak-to-peak voltage equal to the input reference voltage, V_{REF}, and be centered around $V_{REF}/2$. Table 1 and Table 2 indicate the input to the output relationship of the ADC12L063. As indicated in Table 2, biasing one input to $V_{REF}/2$ and driving the other input with its full range signal results in a 6 dB reduction of the output range, limiting it to the range of ¼ to ¾ of the minimum output range obtainable if both inputs were driven with complimentary signals. Signal Inputs explains how to avoid this signal reduction.

Table 1. Input to Output Relationship—Differential Input

V_{IN}^+	V_{IN}^-	Output
V_{CM} −0.5* V_{REF}	V_{CM} +0.5* V_{REF}	0000 0000 0000
V_{CM} −0.25* V_{REF}	V_{CM} +0.25* V_{REF}	0100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000
V_{CM} +0.25* V_{REF}	V_{CM} −0.25* V_{REF}	1100 0000 0000
V_{CM} +0.5* V_{REF}	V_{CM} −0.5* V_{REF}	1111 1111 1111

Table 2. Input to Output Relationship—Single-Ended Input

V_{IN}^+	V_{IN}^-	Output
V_{CM} −V_{REF}	V_{CM}	0000 0000 0000
V_{CM} −0.5* V_{REF}	V_{CM}	0100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000
V_{CM} +0.5* V_{REF}	V_{CM}	1100 0000 0000
V_{CM} +V_{REF}	V_{CM}	1111 1111 1111

The output word rate is the same as the clock frequency, which can be between 1 MSPS and 70 MSPS (typical). The analog input voltage is acquired at the rising edge of the clock and the digital data for that sample is delayed by the pipeline for 6 clock cycles.

A logic high on the power down (PD) pin reduces the converter power consumption to 50 mW.

Applications Information

OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC12L063:

$3.0\ V \le V_A \le 3.6V$

$V_D = V_A$

$1.5V \le V_{DR} \le V_D$

$1\ MHz \le f_{CLK} \le 70\ MHz$

$0.8V \le V_{REF} \le 1.2V$

Analog Inputs

The ADC12L063 has two analog signal inputs, V_{IN}^+ and V_{IN}^-. These two pins form a differential input pair. There is one reference input pin, V_{REF}.

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Reference Pins

The ADC12L063 is designed to operate with a 1.0V reference, but performs well with reference voltages in the range of 0.8V to 1.2V. Lower reference voltages will decrease the signal-to-noise ratio (SNR) of the ADC12L063. Increasing the reference voltage (and the input signal swing) beyond 1.2V will degrade THD for a full-scale input. It is very important that all grounds associated with the reference voltage and the input signal make connection to the analog ground plane at a single point to minimize the effects of noise currents in the ground path.

The three Reference Bypass Pins (V_{RP}, V_{RM} and V_{RN}) are made available for bypass purposes only. These pins should each be bypassed to ground with a 0.1 µF capacitor. DO NOT LOAD these pins.

Signal Inputs

The signal inputs are V_{IN}^+ and V_{IN}^-. The input signal, V_{IN}, is defined as

$$V_{IN} = (V_{IN}^+) - (V_{IN}^-) \quad (3)$$

Figure 31 shows the expected input signal range.

Note that the nominal input common mode voltage, V_{CM}, is $V_{REF}/2$, minimum and the nominal input signals each run between the limits of AGND and 1.0V with V_{REF} = 1.0V. If the differential input signal increases above 2 V_{P-P}, the minimum input common mode voltage should increase proportionally. The Peaks of the input signals should never exceed the voltage described as

$$\text{Peak Input Voltaged} = V_A - 1.0 \quad (4)$$

to maintain dynamic performance.

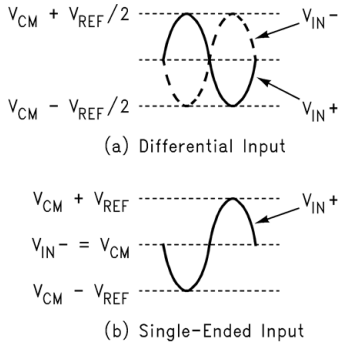

Figure 31. Expected Input Signal Range

The ADC12L063 performs best with a differential input with each input centered around V_{CM} (minimum of 0.5V). The peak-to-peak voltage swing at both V_{IN}^+ and V_{IN}^- should not exceed the value of the reference voltage or the output data will be clipped. The two input signals should be exactly 180° out of phase from each other and of the same amplitude. For single frequency inputs, angular errors result in a reduction of the effective full scale input. For a complex waveform, however, angular errors will result in distortion.

For angular deviations of up to 10 degrees from these two signals being 180 out of phase, the full scale error in LSB can be described as approximately

$$E_{FS} = \text{dev}^{1.79}$$

where

- Dev is the angular difference between the two signals having a 180° relative phase relationship to each other (see Figure 32) (5)

Drive the analog inputs with a source impedance less than 100Ω.

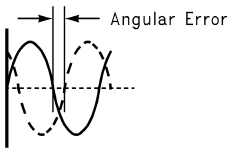

Figure 32. Angular Errors Between the Two Input Signals Will Reduce the Output Level or Cause Distortion

For differential operation, each analog input signal should have a peak-to-peak voltage equal to the input reference voltage, V_{REF}, and be centered around V_{CM}. For single ended operation, one of the analog inputs should be connected to the d.c. common mode voltage of the driven input. The peak-to-peak differential input signal should be twice the reference voltage to maximize SNR and SINAD performance (Figure 31b). For example, set V_{REF} to 1.0V, bias V_{IN}^- to 1.0V and drive V_{IN}^+ with a signal range of 0V to 2.0V. Because very large input signal swings can degrade distortion performance, better performance with a single-ended input can be obtained by reducing the reference voltage when maintaining a full-range output. Table 1 and Table 2 indicate the input to output relationship of the ADC12L063.

The V_{IN}^+ and the V_{IN}^- inputs of the ADC12L063 consist of an analog switch followed by a switched-capacitor amplifier. The capacitance seen at the analog input pins changes with the clock level, appearing as 8 pF when the clock is low, and 7 pF when the clock is high. Although this difference is small, a dynamic capacitance is more difficult to drive than is a fixed capacitance, so choose the driving amplifier carefully. The LMH6702, LMH6628, LMH6622 and LMH6655 are good amplifiers for driving the ADC12L063.

The internal switching action at the analog inputs causes energy to be output from the input pins. As the driving source tries to compensate for this, it adds noise to the signal. To prevent this, use 33Ω series resistors at each of the signal inputs with a 10 pF capacitor across the inputs, as can be seen in Figure 34 and Figure 35. These components should be placed close to the ADC because the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter the input. The 10 pF capacitor value is for undersampling application and should be replaced with a 68 pF capacitor for Nyquist application.

DIGITAL INPUTS

Digital inputs consist of CLK, $\overline{OE}$ and PD.

CLK

The **CLK** signal controls the timing of the sampling process. Drive the clock input with a stable, low jitter clock signal in the range of 1 MHz to 70 MHz with rise and fall times of less than 2 ns. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°.

The **CLK** signal also drives an internal state machine. If the **CLK** is interrupted, or its frequency is too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the lowest sample rate to 1 MSPS.

The **CLOCK** signal also drives an internal state machine. If the clock is interrupted, or its frequency is too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade.

The duty cycle of the clock signal can affect the performance of any A/D Converter. Because achieving a precise duty cycle is difficult, the ADC12L063 is designed to maintain performance over a range of duty cycles. While it is specified and performance is ensured with a 50% clock duty cycle, performance is typically maintained over a clock duty cycle range of 35% to 65%.

The clock line should be series terminated in the characteristic impedance of that line at the clock source. If the clock line is longer than

$$\frac{t_r}{6 \times t_{prop}} \quad (6)$$

where

- t_r is the clock rise t_{prop} is the propagation rate of the signal along the trace

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The **CLOCK** pin should be a.c. terminated with a series RC such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C = \frac{1.2 \times 10^{-9} \times l}{Z_o}$$

where

- "l" is the line length in inches
- Z_o is the characteric impedance of the clock line (7)

This termination should be located as close as possible to, but within one centimeter of, the ADC12L063 clock pin as shown in Figure 33. A typical propagation rate on FR4 material is about 150ps/inch, or about 60ps/cm.

$\overline{\text{OE}}$

The $\overline{\text{OE}}$ pin, when high, puts the output pins into a high impedance state. When this pin is low the outputs are in the active state. The ADC12L063 will continue to convert whether this pin is high or low, but the output can not be read while the $\overline{\text{OE}}$ pin is high.

PD

The PD pin, when high, holds the ADC12L063 in a power-down mode to conserve power when the converter is not being used. The power consumption in this state is 50 mW. The output data pins are undefined in this mode. Power consumption during power-down is not affected by the clock frequency, or by whether there is a clock signal present. The data in the pipeline is corrupted while in the power down mode.

OUTPUTS

The ADC12L063 has 12 TTL/CMOS compatible Data Output pins. The offset binary data is present at these outputs while the $\overline{\text{OE}}$ and PD pins are low. While the t_{OD} time provides information about output timing, a simple way to capture a valid output is to latch the data on the *rising edge* of the conversion clock (pin 10).

Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can cause on-chip ground noise and couple into the analog circuitry, degrading dynamic performance. Adequate bypassing and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond the specified 20 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could be an apparent reduction in dynamic performance.

To minimize noise due to output switching, minimize the load currents at the digital outputs. This can be done by connecting buffers between the ADC outputs and any other circuitry (74ACQ541, for example). Only one input should be connected to each output pin. Additionally, inserting series resistors of 47Ω to 56Ω at the digital outputs, close to the ADC pins, will isolate the outputs from trace and other circuit capacitances and limit the output currents, which could otherwise result in performance degradation. See Figure 33.

While the ADC12L063 will operate with V_{DR} voltages down to 2.5V, t_{OD} increases with reduced V_{DR}. Be careful of external timing when using reduced V_{DR}.

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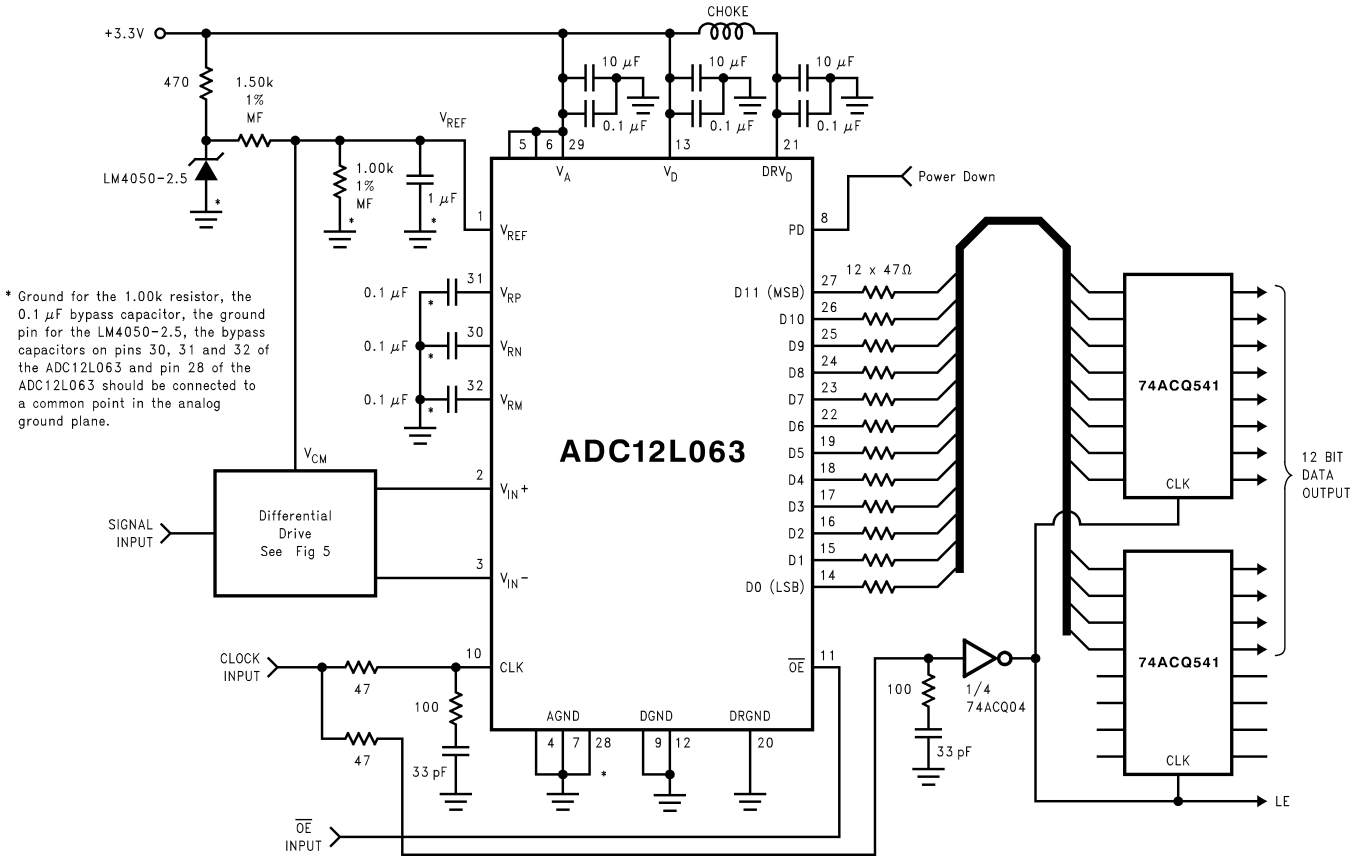

Figure 33. Simple Application Circuit with Single-Ended to Differential Buffer

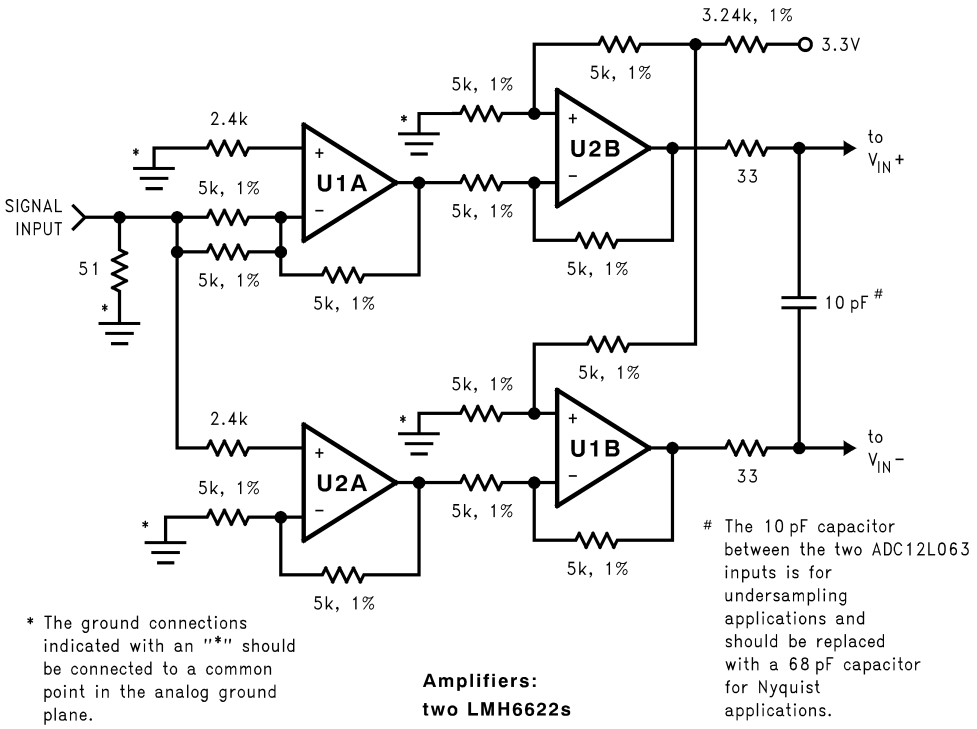

Figure 34. Differential Drive Circuit of Figure 33

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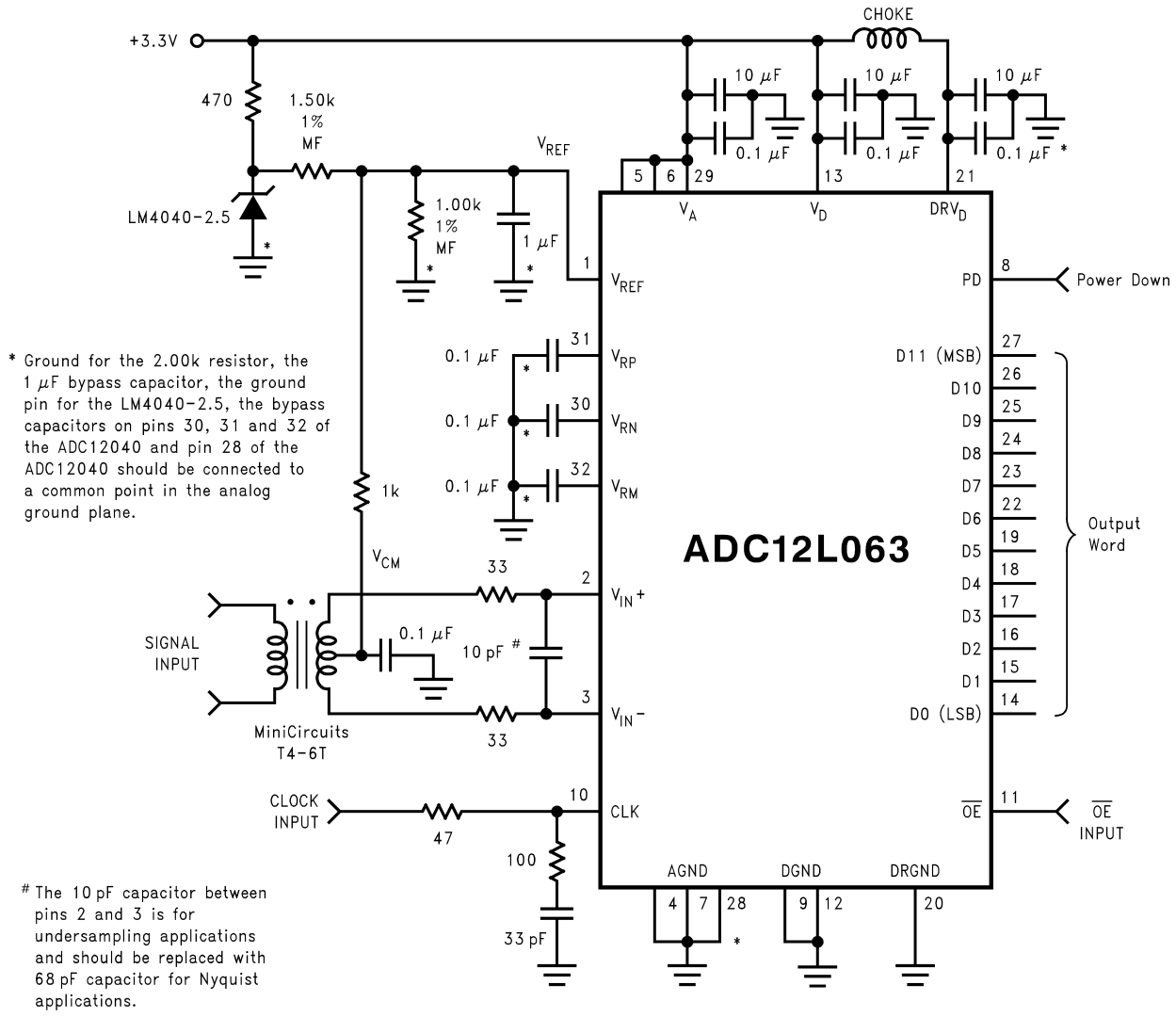

Figure 35. Driving the Signal Inputs with a Transforme

POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 10 µF capacitor and with a 0.1 µF ceramic chip capacitor within a centimeter of each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC12L063 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during turn on and turn off of power.

The V_{DR} pin provides power for the output drivers and may be operated from a supply in the range of 2.5V to V_D (nominal 3.3V). This can simplify interfacing to 3V devices and systems. **DO NOT operate the V_{DR} pin at a voltage higher than V_D.**

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC12L063 between these areas, is required to achieve specified performance.

The ground return for the data outputs (DR GND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DR GND pins should NOT be connected to system ground in close proximity to any of the ADC12L063's other ground pins.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74LS, 74HC(T) and 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families.

The effects of the noise generated from the ADC output switching can be minimized through the use of 47Ω to 56Ω resistors in series with each data output line. Locate these resistors as close to the ADC output pins as possible.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

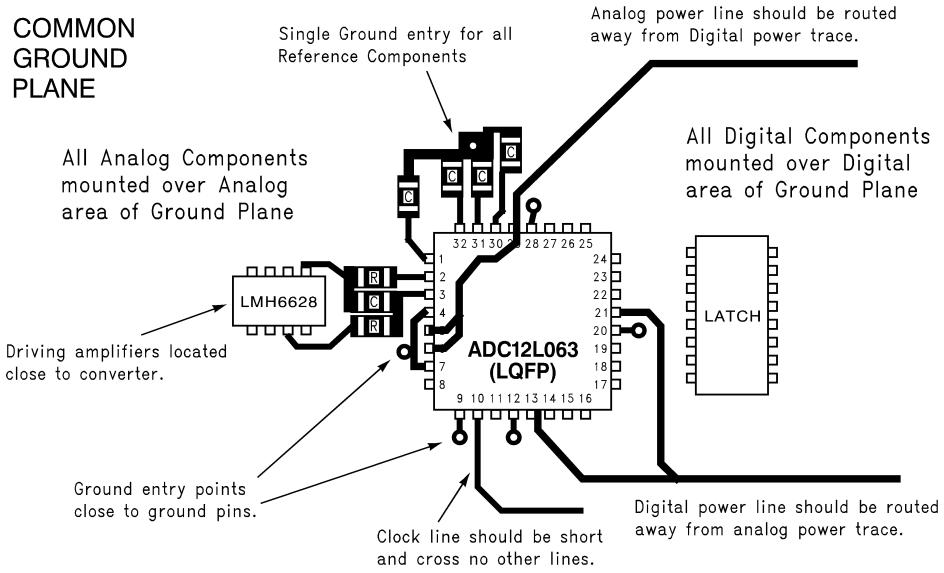

Figure 36. Example of a Suitable Layout

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90° crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

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Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should *not* be placed side by side, even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the analog ground plane.

Figure 36 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog ground plane. All digital circuitry and I/O lines should be placed over the digital ground plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the analog ground plane at a single point. All ground connections should have a low inductance path to ground.

DYNAMIC PERFORMANCE

To achieve the best dynamic performance, the clock source driving the CLK input must be free of jitter. Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in Figure 37.

As mentioned in LAYOUT AND GROUNDING, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

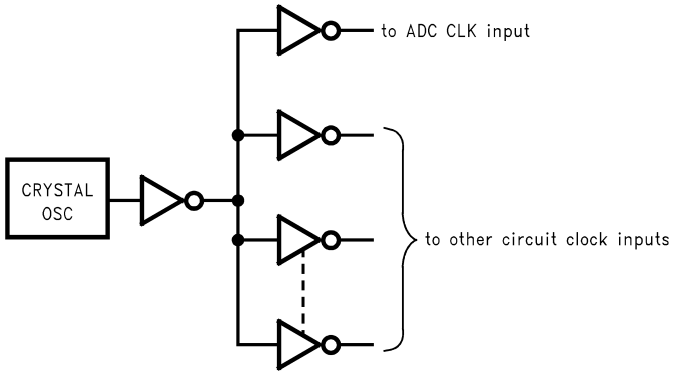

Figure 37. Isolating the ADC Clock from other Circuitry with a Clock Tree

COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 100 mV beyond the supply rails (more than 100 mV below the ground pins or 100 mV above the supply pins). Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital components (e.g., 74F and 74AC devices) to exhibit overshoot or undershoot that goes above the power supply or below ground. A resistor of about 50Ω to 100Ω in series with any offending digital input, close to the signal source, will eliminate the problem.

Do not allow input voltages to exceed the supply voltage, even on a transient basis. Not even during power up or power down.

Be careful not to overdrive the inputs of the ADC12L063 with a device that is powered from supplies outside the range of the ADC12L063 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can couple into the analog circuitry, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital areas on the pc board will reduce this problem.

Additionally, bus capacitance beyond the specified 20 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could, again, be an apparent reduction in dynamic performance.

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The digital data outputs should be buffered (with 74ACQ541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC12L063, which reduces the energy coupled back into the converter output pins by limiting the output current. A reasonable value for these resistors is 47Ω to 56Ω.

Using an inadequate amplifier to drive the analog input. As explained in Signal Inputs, the capacitance seen at the input alternates between 8 pF and 7 pF, depending upon the phase of the clock. This dynamic load is more difficult to drive than is a fixed capacitance.

If the amplifier exhibits overshoot, ringing, or any evidence of instability, even at a very low level, it will degrade performance. A small series resistor at each amplifier output and a capacitor across the analog inputs (as shown in Figure 34 and Figure 35) will improve performance. The LMH6702, LMH6622 and LMH6628 have been successfully used to drive the analog inputs of the ADC12L063.

Also, it is important that the signals at the two inputs have exactly the same amplitude and be exactly 180º out of phase with each other. Board layout, especially equality of the length of the two traces to the input pins, will affect the effective phase between these two signals. Remember that an operational amplifier operated in the non-inverting configuration will exhibit more time delay than will the same device operating in the inverting configuration.

Operating with the reference pins outside of the specified range. As mentioned in Reference Pins, V_{REF} should be in the range of

$$0.8V \le V_{REF} \le 1.2V \quad (8)$$

Operating outside of these limits could lead to performance degradation.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR and SINAD performance.

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REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	26

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC12L063CIVY/NOPB	Active	Production	LQFP (NEY) | 32	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12L0 63CIVY
ADC12L063CIVY/NOPB.A	Active	Production	LQFP (NEY) | 32	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12L0 63CIVY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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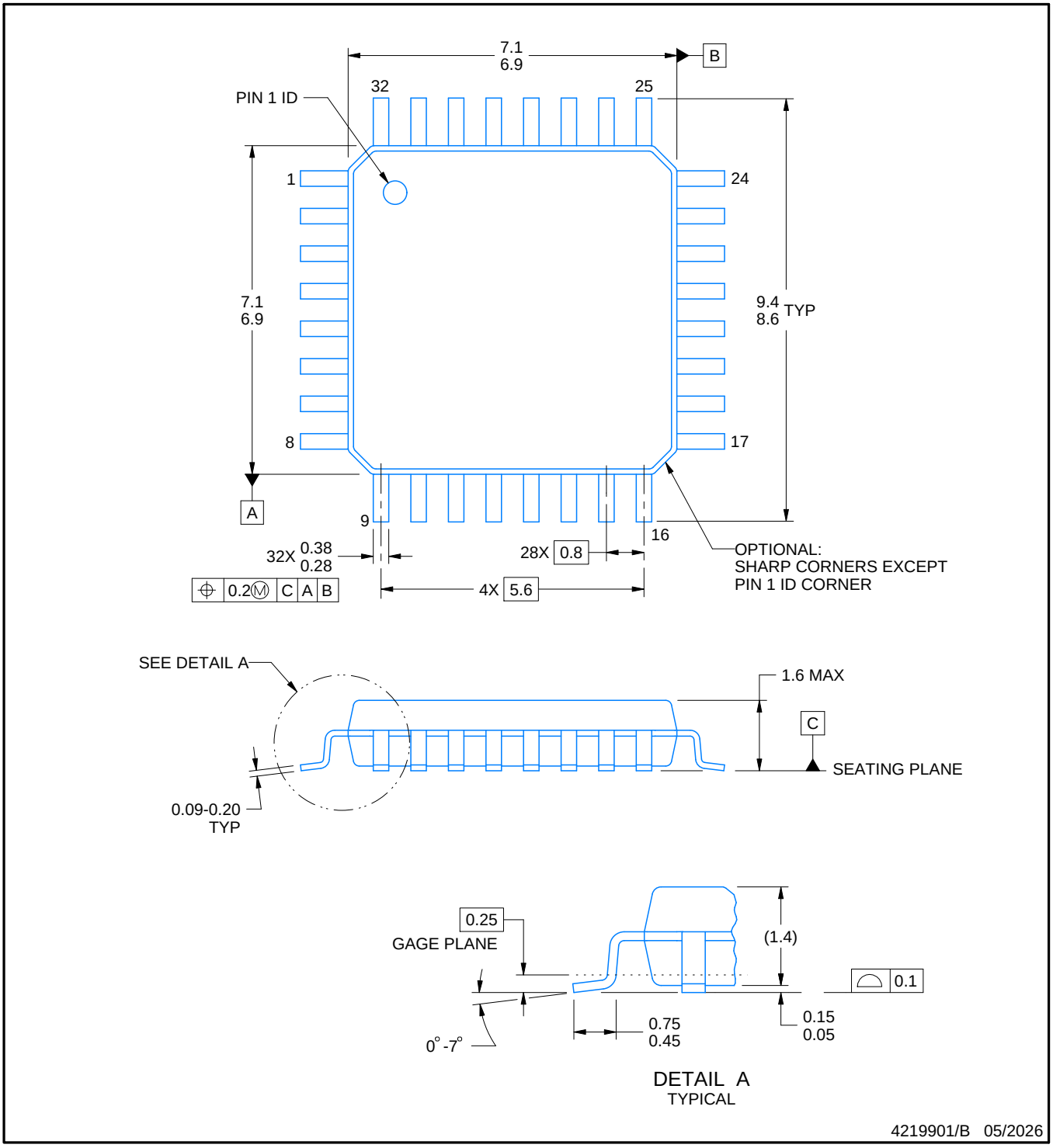
PACKAGE OUTLINE

NEY0032A

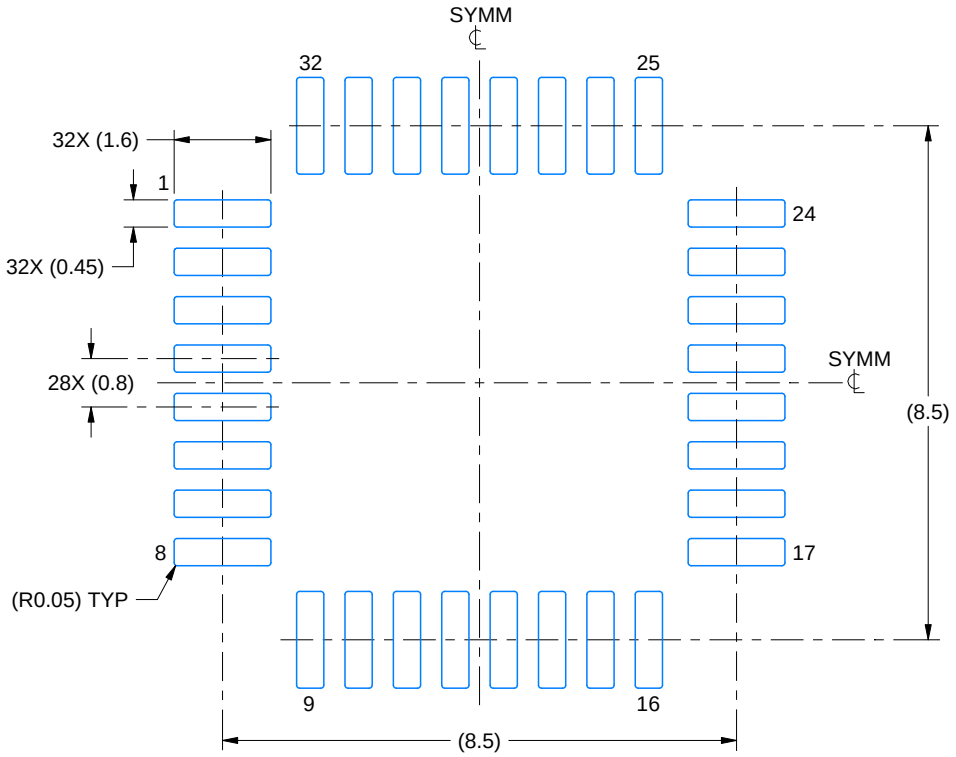
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

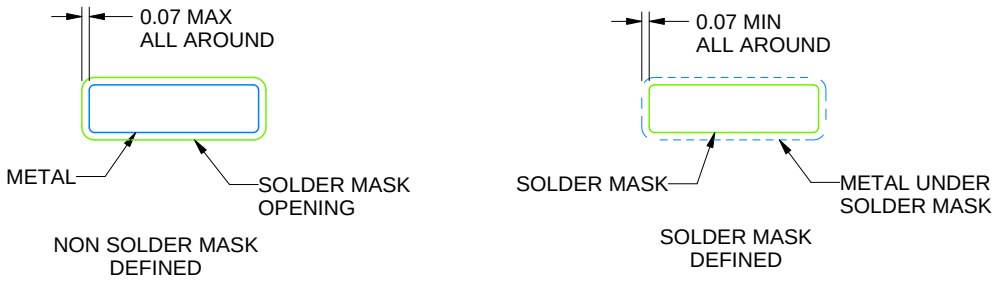


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4219901/B 05/2026

NOTES: (continued)

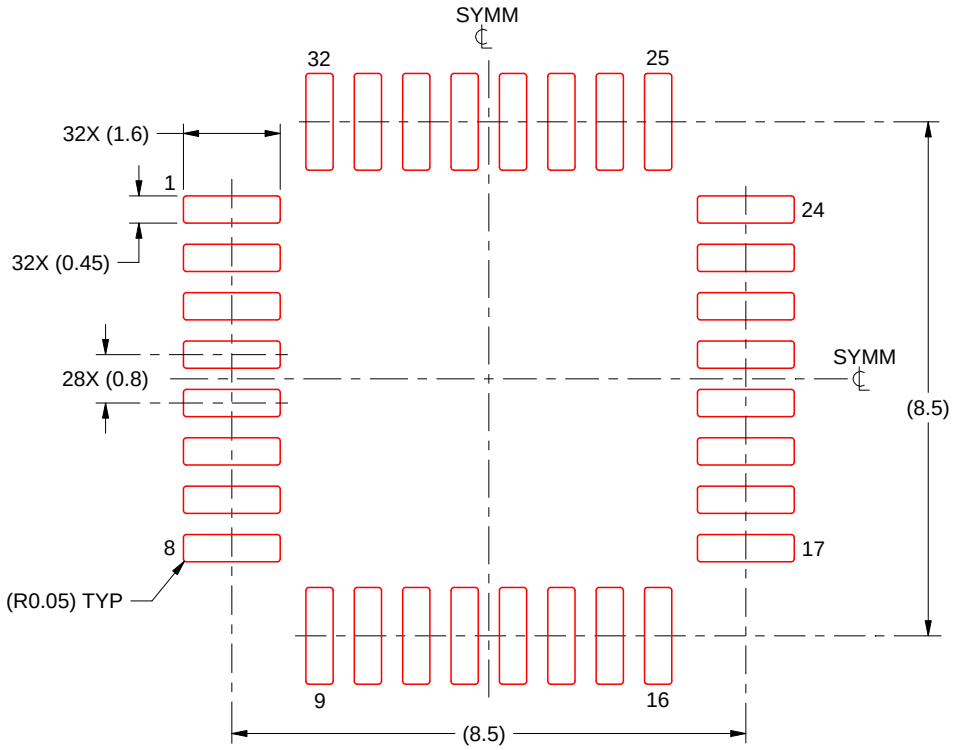
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NEY0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
SCALE 8X

4219901/B 05/2026

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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