ADC12DL080 Dual 12-Bit, 80 MSPS, A/D Converter for IF Sampling

Check for Samples: ADC12DL080

FEATURES

- **Single +3.3V Supply Operation**
- **Internal Sample-and-Hold**
- **Internal or External Reference**
- **Outputs 2.4V to 3.6V Compatible**
- **Power Down Mode**
- **Duty Cycle Stabilizer**
- **Pin Compatible with ADC12DL040, ADC12DL065, ADC12DL066**

APPLICATIONS

- **Instrumentation**
- **Communications Receivers**
- **Sonar/Radar**
- **xDSL, Cable Modems**

KEY SPECIFICATIONS

- **Resolution: 12 Bits**
- **Max Conversion Rate: 80 MSPS**
- **DNL: ±0.4 LSB (typ)**
- **SNR (f_{IN}=40MHz): 69 dB (typ)**
- **SNR (f_{IN}=200MHz): 67 dB(typ)**
- **SFDR (f_{IN}=40MHz): 82 dB (typ)**
- **SFDR (f_{IN}=200MHz): 81 dB (typ)**
- **Power Consumption**
  - **Operating: 447 mW (typ)**
  - **Power Down Mode: 50 mW (typ)**

DESCRIPTION

The ADC12DL080 is a dual, low power monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 80 Megasamples per second (MSPS). This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption while providing excellent dynamic performance and a 600 MHz Full Power Bandwidth. Operating on a single +3.3V power supply, the ADC12DL080 achieves 11.0 effective bits at Nyquist and consumes just 447mW at 80 MSPS. The Power Down feature reduces power consumption to 50 mW.

The differential inputs provide a full scale differential input swing equal to 2 times V_{REF} with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. Duty cycle stabilization and output data format are selectable. The output data can be set for offset binary or two's complement.

To ease interfacing to lower voltage systems, the digital output driver power pins of the ADC12DL080 can be connected to a separate supply voltage in the range of 2.4V to the analog supply voltage. This device is available in the 64-lead TQFP package and will operate over the industrial temperature range of −40°C to +85°C. An evaluation board is available to ease the evaluation process.

Connection Diagram

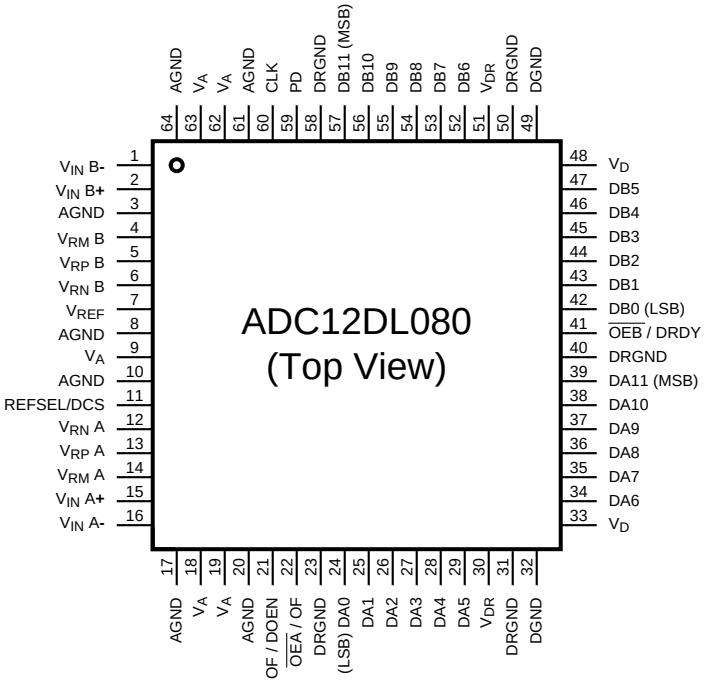
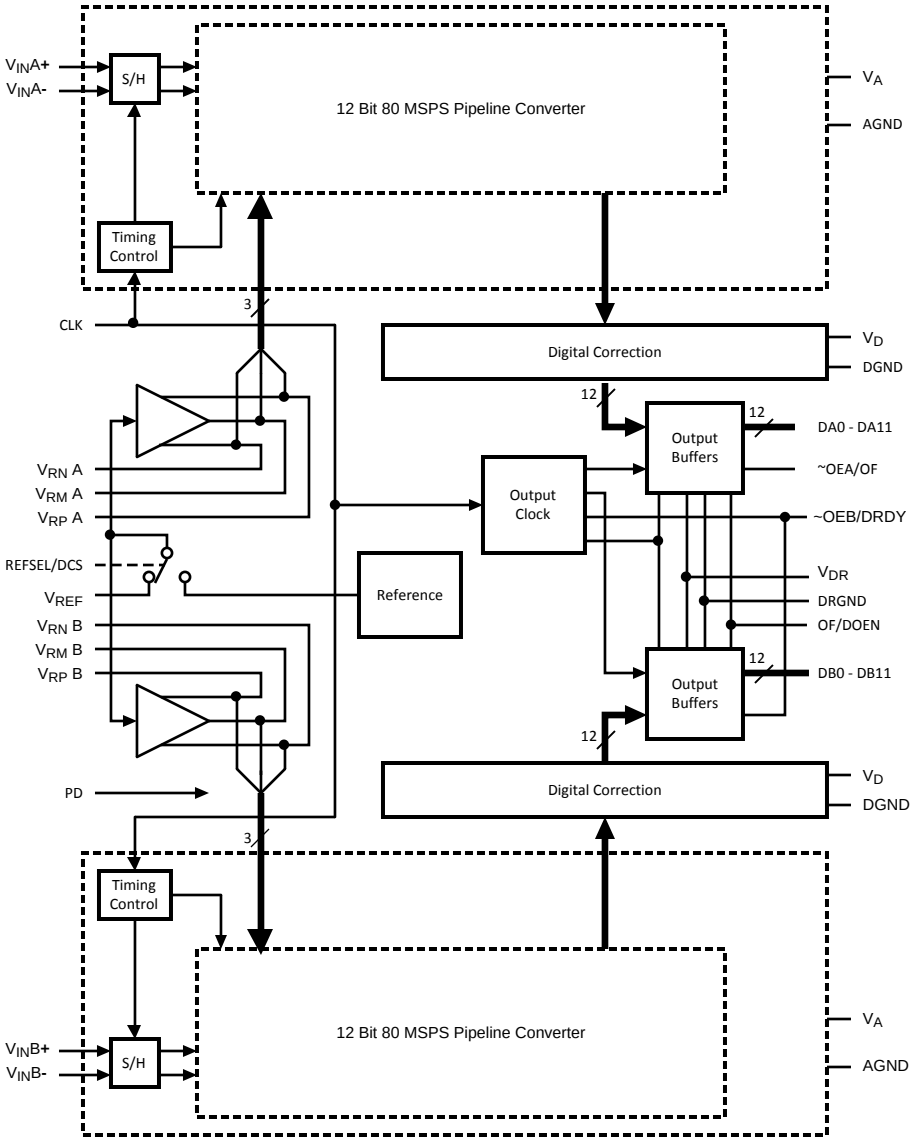
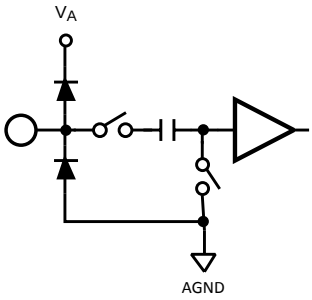
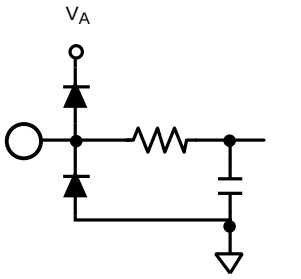
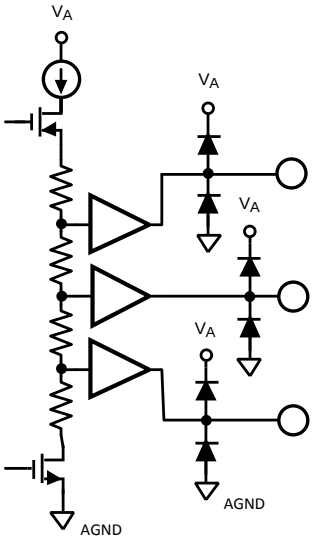


Figure 1. TQFP Package
See Package Number PAG0064A

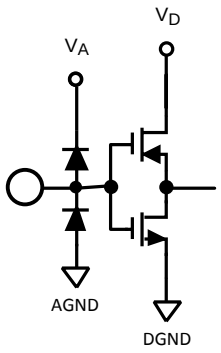
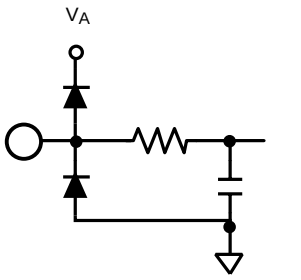
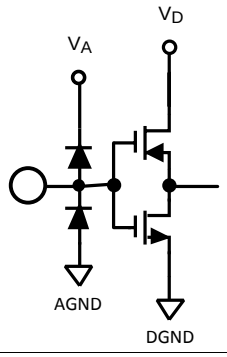
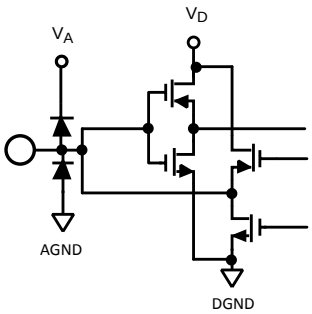
Block Diagram



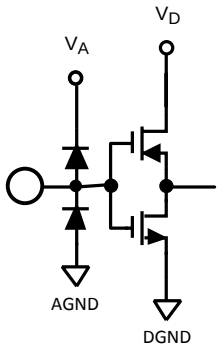
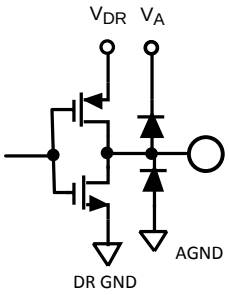
Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
15 2	$V_{IN}A+$ $V_{IN}B+$		Differential analog input pins. With a 1.0V reference voltage the differential full-scale input signal level is 2.0 V_{P-P} with each input pin voltage centered on a common mode voltage, V_{CM}. The negative input pins may be connected to V_{CM} for single-ended operation, but a differential input signal is required for best performance.
16 1	$V_{IN}A-$ $V_{IN}B-$		
7	V_{REF}		This pin is used in conjunction with REFSEL/DCS (pin 11) to select the internal 1.0V reference, or as the external reference input. If V_{REF} is tied HIGH, the internal 1.0V reference is selected. REFSEL/DCS must be LOW or tied to $V_{RM}A$ or $V_{RM}B$. If a voltage in the range of 0.8V to 1.2V is applied to this pin, that voltage is used as the reference. V_{REF} should be bypassed to AGND with a 0.1 µF low ESL capacitor when an external reference is used. The nominal external reference voltage is 1.0V but values in the range of 0.8V to 1.2V may be used. REFSEL/DCS must be HIGH or REFSEL/DCStied to $V_{RM}A$ or $V_{RM}B$. See Table 3 in for more information.
11	REFSEL/DCS		This pin is used in conjunction with V_{REF} (pin 7) to select the reference source and turn the Duty Cycle Stabilizer (DCS) on or off. When REFSEL/DCS is LOW and V_{REF} is HIGH, the internal 1.0V reference is selected and DCS is On. When REFSEL/DCS is HIGH, an external reference voltage in the range of 0.8V to 1.2V should be applied to the V_{REF} input. DCS is On. With this pin connected to $V_{RM}A$ or $V_{RM}B$, DCS is Off. See Table 3 in REFSEL/DCS for more information.
13 5	$V_{RP}A$ $V_{RP}B$		These are reference bypass pins. These pins should each be bypassed to ground with a 0.1 µF capacitor. A 10 µF capacitor should be placed between the $V_{RP}A$ and $V_{RN}A$ pins and between the $V_{RP}B$ and $V_{RN}B$ pins. These pins should not be loaded.
14 4	$V_{RM}A$ $V_{RM}B$		
12 6	$V_{RN}A$ $V_{RN}B$		

Pin Descriptions and Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent Circuit	Description
DIGITAL I/O			
60	CLK		Digital clock input. The range of frequencies for this input is as specified in the electrical tables with ensured performance at 80 MHz. The inputs are sampled on the rising edge.
21	OF/DOEN		OF/DOEN selects the output format (OF) or enables the DRDY output (DOEN). The state of this pin also controls the function of pins 22 and 41. When OF/DOEN is tied to $V_{RM}A$ or $V_{RM}B$, DRDY is enabled. Pin 41 is used as the DRDY output strobe, and pin 22 is used to select the output format. Output Enable for channels A and B are not available in this mode. When OF/DOEN is LOW, the output data format is offset binary. With OF/DOEN tied HIGH, the output format is 2's complement. See Table 4 in OF/DOEN, $\overline{OEA}$/OF, and $\overline{OEB}$/DRDY for more information.
22	$\overline{OEA}$/OF		Output Enable for Channel A ($\overline{OEA}$) or Output format (OF). The function of this pin is controlled by the state of pin 21. When DRDY is enabled (pin 21 tied to $V_{RM}A$ or $V_{RM}B$) this pin sets the output format. When LOW, the output data format is offset binary. When HIGH, the output format is 2's complement. When DRDY is not enabled (pin 21 is LOW or HIGH) this pin is the Output Enable for Channel A. When LOW the outputs for Channel A are active. When HIGH, the outputs for Channel A are in a high impedance state. See Table 4 in OF/DOEN, $\overline{OEA}$/OF, and $\overline{OEB}$/DRDY for more information.
41	$\overline{OEB}$/DRDY		Output Enable for Channel B ($\overline{OEB}$) or Data Ready Output strobe (DRDY). The function of this pin is controlled by the state of pin 21. When DRDY is enabled (pin 21 tied to $V_{RM}A$ or $V_{RM}B$) this pin is the DRDY output. The data outputs are synchronized with the falling edge of this signal. This signal switches at the same rate as the input clock. When DRDY is not enabled (pin 21 is LOW or HIGH) this pin is the Output Enable for Channel B. When LOW the outputs for Channel B are active. When HIGH, the outputs for Channel B are in a high impedance state. See Table 4 in OF/DOEN, $\overline{OEA}$/OF, and $\overline{OEB}$/DRDY for more information.

Pin Descriptions and Equivalent Circuits (continued)

Pin No.	Symbol	Equivalent Circuit	Description
59	PD		PD is the Power Down input pin. When high, this input puts the converter into the power down mode. When this pin is low, the converter is in the active mode.
24–29 34–39	DA0–DA5 DA6-DA11		Digital data output pins that make up the 12-bit conversion results of their respective converters. DA0 and DB0 are the LSBs, while DA11 and DB11 are the MSBs of the output word. Output levels are TTL/CMOS compatible. Optimum loading is < 10pF.
42–47 52–57	DB0–DB5 DB6-DB11		
ANALOG POWER			
9, 18, 19, 62, 63	V_A		Positive analog supply pins. These pins should be connected to a quiet +3.3V source and bypassed to AGND with 0.1 µF capacitors located near the power pins, and with a 10 µF capacitor.
3, 8, 10, 17, 20, 61, 64	AGND		The ground return for the analog supply.
DIGITAL POWER			
33, 48	V_D		Positive digital supply pin. This pin should be connected to the same quiet +3.3V source as is V_A and be bypassed to DGND with a 0.1 µF capacitor located near the power pins, and with a 10 µF capacitor.
32, 49	DGND		The ground return for the digital supply.
30, 51	V_{DR}		Positive driver supply pin for the ADC12DL080's output drivers. This pin should be connected to a voltage source of +2.4V to V_D and be bypassed to DRGND with a 0.1 µF capacitor. This supply should also be bypassed with a 10 µF capacitor. V_{DR} should never exceed the voltage on V_D. All 0.1 µF bypass capacitors should be located near the supply pin.
23, 31, 40, 50, 58	DRGND		The ground return for the digital supply for the ADC12DL080's output drivers. These pins should be connected to the system digital ground, but not be connected in close proximity to the ADC12DL080's DGND or AGND pins. See LAYOUT AND GROUNDING (Layout and Grounding) for more details.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

V_A, V_D, V_{DR}		4.2V
$\|V_A–V_D\|$		≤ 100 mV
Voltage on Any Input or Output Pin		−0.3V to (V_A or V_D +0.3V)
Input Current at Any Pin (4)		±25 mA
Package Input Current (4)		±50 mA
Package Dissipation at T_A = 25°C		See (5)
ESD Susceptibility	Human Body Model (6)	2500V
	Machine Model (6)	250V
	Charge Device Model	750V
Soldering Temperature, Infrared, 10 sec. (7)		235°C
Storage Temperature		−65°C to +150°C
Soldering process must comply with Reflow Temperature Profile specifications. Refer to www.ti.com/packaging. (7)		

(1) All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. In the 64-pin TQFP, θ_{JA} is 50°C/W, so P_DMAX = 2 Watts at 25°C and 800 mW at the maximum operating ambient temperature of 85°C. Note that the power consumption of this device under normal operation will typically be about 497 mW (447 typical power consumption + 50 mW TTL output loading). The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.
(7) Reflow Reflow temperature profiles are different for lead-free and non-lead-free packages.

Operating Ratings (1)(2)

Operating Temperature	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_A, V_D)	+3.0V to +3.6V
Output Driver Supply (V_{DR})	+2.4V to V_D
CLK, PD, OF/DOEN, $\overline{OEA}$/OF, $\overline{OEB}$/DRDY	−0.05V to (V_D + 0.05V)
Analog Input Pins	0V to 2.6V
V_{CM}	1.0V to 2.0V
$\|AGND–DGND\|$	≤100mV
Clock Duty Cycle (DCS On)	30% to 70%
Clock Duty Cycle (DCS Off)	40% to 60%

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

Converter Electrical Characteristics[1][2][3]

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, External V_{REF} = +1.0V, f_{CLK} = 80 MHz, f_{IN} = 40 MHz, C_L = 10 pF/pin, Duty Cycle Stabilizer On. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C

Parameter		Test Conditions		Typical[4]	Limits[4]	Units (Limits)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits (min)
INL	Integral Non Linearity[5]	f_{IN} = 0, Best Fit Method		±0.9	**±3.5**	LSB (max)
DNL	Differential Non Linearity	f_{IN} = 0		±0.4	**±1.0**	LSB (max)
PGE	Positive Gain Error			±0.3	**±3.5**	%FS (max)
NGE	Negative Gain Error			±0.3	**±3.5**	%FS (max)
TC GE	Gain Error Tempco	−40°C ≤ T_A ≤ +85°C		10		ppm/°C
V_{OFF}	Offset Error (V_{IN}+ = V_{IN}−)			-0.2	**+0.75** **-1.1**	%FS (max) %FS (min)
TC V_{OFF}	Offset Error Tempco	−40°C ≤ T_A ≤ +85°C		16		ppm/°C
	Under Range Output Code			0	**0**	
	Over Range Output Code			4095	**4095**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{CM}	Common Mode Input Voltage			1.5	1.0	V (min)
					2.0	V (max)
V_{RM}A, V_{RM}B	Reference Output Voltage			1.5		V
C_{IN}	V_{IN} Input Capacitance (each pin to GND)	V_{IN} = 1.5 Vdc ±0.5V	(CLK LOW)	8		pF
			(CLK HIGH)	7		pF
V_{REF}	External Reference Voltage[6]			1.00	**0.8** **1.2**	V (min) V (max)
	Reference Input Resistance			1		MΩ (min)
DYNAMIC CONVERTER CHARACTERISTICS						
FPBW	Full Power Bandwidth	0 dBFS Input, Output at −3 dB		600		MHz
SNR	Signal-to-Noise Ratio[7]	f_{IN} = 40 MHz, V_{IN} = −1 dBFS		69.3	**67**	dBFS (min)
		f_{IN} = 200 MHz, V_{IN} = −1 dBFS		67		dBFS
SINAD	Signal-to-Noise and Distortion[7]	f_{IN} = 40 MHz, V_{IN} = −1 dBFS		69	**66.5**	dBFS (min)
		f_{IN} = 200 MHz, V_{IN} = −1 dBFS		66.5		dBFS
ENOB	Effective Number of Bits[7]	f_{IN} = 40 MHz, V_{IN} = −1 dBFS		11	**10.75**	Bits (min)
		f_{IN} = 200 MHz, V_{IN} = −1 dBFS		10.75		Bits
THD	Total Harmonic Distortion	f_{IN} = 40 MHz, V_{IN} = −1 dBFS		−80	**-71**	dBc (min)
		f_{IN} = 200 MHz, V_{IN} = −1 dBFS		−76.8		dBc
H2	Second Harmonic Distortion	f_{IN} = 40 MHz, V_{IN} = −1 dBFS		−85	**-73**	dBc (min)
		f_{IN} = 200 MHz, V_{IN} = −1 dBFS		−84		dBc

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per Note 4 of the Absolute Maximum Ratings Table. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is +3.3V, the full-scale input voltage must be ≤+3.4V to ensure accurate conversions. See Figure 2.
(2) To ensure accuracy, it is required that $|V_A – V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-bit LSB is 488 µV.
(4) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are to AOQL (Average Outgoing Quality Level).
(5) Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive and negative full-scale.
(6) Optimum performance will be obtained by keeping the reference input in the 0.8V to 1.2V range. The LM4051CIM3-ADJ (SOT-23 package) is recommended for external reference applications.
(7) This parameter is specified in units of dBFS - indicating the equivalent value that would be attained with a full-scale input signal

Converter Electrical Characteristics[1][2][3] (continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, External V_{REF} = +1.0V, f_{CLK} = 80 MHz, f_{IN} = 40 MHz, C_L = 10 pF/pin, Duty Cycle Stabilizer On. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C

Parameter		Test Conditions	Typical[4]	Limits[4]	Units (Limits)
H3	Third Harmonic Distortion	f_{IN} = 40 MHz, V_{IN} = −1 dBFS	−82	**-74**	dBc (min)
		f_{IN} = 200 MHz, V_{IN} = −1 dBFS	−81		dBc
SFDR	Spurious Free Dynamic Range	f_{IN} = 40 MHz, V_{IN} = −1 dBFS	82	**73**	dBc (min)
		f_{IN} = 200 MHz, V_{IN} = −1 dBFS	81		dBc
IMD	Intermodulation Distortion	f_{IN} = 19.6 MHz and 20.2 MHz, each = −6.5 dBFS	−70		dBFS
INTER-CHANNEL CHARACTERISTICS					
	Channel—Channel Offset Match		±0.3		%FS
	Channel—Channel Gain Match		±0.4		%FS
	Crosstalk	10 MHz Tested, Channel; 20 MHz Other Channel	90		dBc

DC and Logic Electrical Characteristics[1][2][3]

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, External V_{REF} = +1.0V, f_{CLK} = 80 MHz, f_{IN} = 40 MHz, C_L = 10 pF/pin, Duty Cycle Stabilizer On. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C

Parameter		Test Conditions		Typical[4]	Limits[4]	Units (Limits)
DIGITAL INPUT CHARACTERISTICS						
$V_{IN(1)}$	Logical “1” Input Voltage	V_D = 3.6V			**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	V_D = 3.0V			**1.0**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = 3.3V		10		µA
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V		−10		µA
C_{IN}	Digital Input Capacitance			5		pF
DIGITAL OUTPUT CHARACTERISTICS						
$V_{OUT(1)}$	Logical “1” Output Voltage	I_{OUT} = −0.5 mA	V_{DR} = 2.5V		**2.3**	V (min)
			V_{DR} = 3V		**2.7**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	I_{OUT} = 1.6 mA, V_{DR} = 3V			**0.4**	V (max)
I_{OZ}	TRI-STATE Output Current	V_{OUT} = 2.5V or 3.3V		100		nA
		V_{OUT} = 0V		−100		nA
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V		−20		mA
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = V_{DR}		20		mA
C_{OUT}	Digital Output Capacitance			5		pF

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per Note 4 of the Absolute Maximum Ratings Table. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is +3.3V, the full-scale input voltage must be ≤+3.4V to ensure accurate conversions. See Figure 2.
(2) To ensure accuracy, it is required that $|V_A–V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-bit LSB is 488 µV.
(4) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are to AOQL (Average Outgoing Quality Level).

DC and Logic Electrical Characteristics[1][2][3] (continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, External V_{REF} = +1.0V, f_{CLK} = 80 MHz, f_{IN} = 40 MHz, C_L = 10 pF/pin, Duty Cycle Stabilizer On. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C

Parameter		Test Conditions	Typical[4]	Limits[4]	Units (Limits)
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD Pin = DGND, V_{REF} = V_A PD Pin = V_D	112.5 15	**136**	mA (max) mA
I_D	Digital Supply Current	PD Pin = DGND PD Pin = V_D , f_{CLK} = 0	23 0	**26**	mA (max) mA
I_{DR}	Digital Output Supply Current	PD Pin = DGND, C_L = 10 pF[5] PD Pin = V_D, f_{CLK} = 0	15 0		mA mA
	Total Power Consumption	PD Pin = DGND, C_L = 10 pF[6] PD Pin = V_D	447 50	**535**	mW (max) mW
PSRR	Power Supply Rejection Ratio	Rejection of Full-Scale Error with V_A = 3.0V vs. 3.6V	80		dB

(5) I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent). I_{DR}=V_{DR}(C_0 x f_0 + C_1 x f_1 +....C_{11} x f_{11}) where V_{DR} is the output driver power supply voltage, C_n is total capacitance on the output pin, and f_n is the average frequency at which that pin is toggling.
(6) Excludes I_{DR}. See Note 5.

AC Electrical Characteristics[1][2][3][4]

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, External V_{REF} = +1.0V, f_{CLK} = 80 MHz, f_{IN} = 40 MHz, C_L = 10 pF/pin, Duty Cycle Stabilizer On. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C

Parameter		Test Conditions	Typical[5]	Limits[5]	Units (Limits)
f_{CLK^1}	Maximum Clock Frequency			**80**	MHz (min)
f_{CLK^2}	Minimum Clock Frequency		10		MHz
t_{CH}	Clock High Time	Duty Cycle Stabilizer On	6.25	3.75	ns (min)
t_{CL}	Clock Low Time	Duty Cycle Stabilizer On	6.25	3.75	ns (min)
t_{CH}	Clock High Time	Duty Cycle Stabilizer Off	6.25	5	ns (min)
t_{CL}	Clock Low Time	Duty Cycle Stabilizer Off	6.25	5	ns (min)
t_r, t_f	Clock Rise and Fall Times		2		ns (max)
t_{CONV}	Conversion Latency			**7**	Clock Cycles
t_{OD}	Data Output Delay after Rising Clock Edge		7.5	**3.5** **11**	ns (min) ns (max)
t_{OSU}	Output Set up time from data output transition to rising edge of DRDY	See[6]	7.2	4	ns (min)
t_{OH}	Output Hold time from rising edge of DRDY to next data output transition	See[6]	5.3	4	ns (min)
t_{AD}	Aperture Delay		2		ns
t_{AJ}	Aperture Jitter		0.3		ps rms
t_{DIS}	Data outputs into Hi-Z Mode		10		ns
t_{EN}	Data Outputs Active after Hi-Z Mode		10		ns

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per Note 4 of the Absolute Maximum Ratings Table. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is +3.3V, the full-scale input voltage must be ≤+3.4V to ensure accurate conversions. See Figure 2.
(2) To ensure accuracy, it is required that $|V_A–V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-bit LSB is 488 µV.
(4) Timing specifications are tested at TTL logic levels, V_{IL} = 0.4V for a falling edge and V_{IH} = 2.4V for a rising edge.
(5) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are to AOQL (Average Outgoing Quality Level).
(6) This parameter is ensured by design and/or characterization and is not tested in production.

AC Electrical Characteristics[1][2][3][4] (continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, External V_{REF} = +1.0V, f_{CLK} = 80 MHz, f_{IN} = 40 MHz, C_L = 10 pF/pin, Duty Cycle Stabilizer On. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C

Parameter		Test Conditions	Typical[5]	Limits[5]	Units (Limits)
t_{PD}	Power Down Mode Exit Cycle	0.1 µF on pins 4,5,6,12,13,14; 10 µF between pins 5, 6 and between pins 12, 13	100		µs

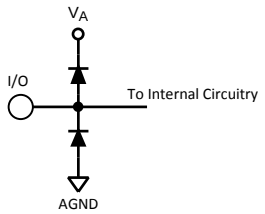


Figure 2.

SPECIFICATION DEFINITIONS

APERTURE DELAY is the time after the rising edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common d.c. voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

CROSSTALK is coupling of energy from one channel into the other channel.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error − Negative Full Scale Error (1)

Gain Error can also be expressed as Positive Gain Error and Negative Gain Error, which are:

PGE = Positive Full Scale Error - Offset Error

NGE = Offset Error - Negative Full Scale Error

GAIN ERROR MATCHING is the difference in gain errors between the two converters divided by the average gain of the converters.

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a best fit straight line. The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{FS}/2^n$, where "V_{FS}" is the full scale input voltage and "n" is the ADC resolution in bits.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC12DL080 is ensured not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages [$(V_{IN}+) – (V_{IN}-)$] required to cause a transition from code 2047 to 2048.

OUTPUT DELAY is the time delay after the rising edge of the clock before the data update is presented at the output pins.

OVER RANGE RECOVERY TIME is the time required after V_{IN} goes from a specified voltage out of the normal input range to a specified voltage within the normal input range and the converter makes a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC12DL080, PSRR1 is the ratio of the change in Full-Scale Error that results from a change in the d.c. power supply voltage, expressed in dB. PSRR2 is a measure of how well an a.c. signal riding upon the power supply is rejected at the output.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_{10}^2}{f_1^2}} \tag{2}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_{10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

SECOND HARMONIC DISTORTION (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

THIRD HARMONIC DISTORTION (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagram

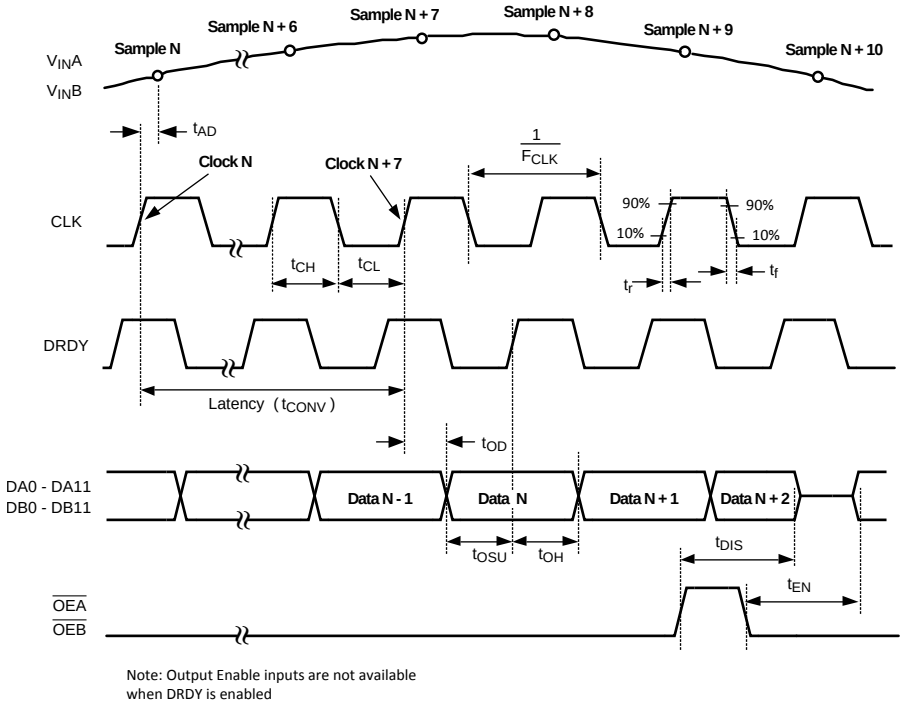


Figure 3. Output Timing

Transfer Characteristic

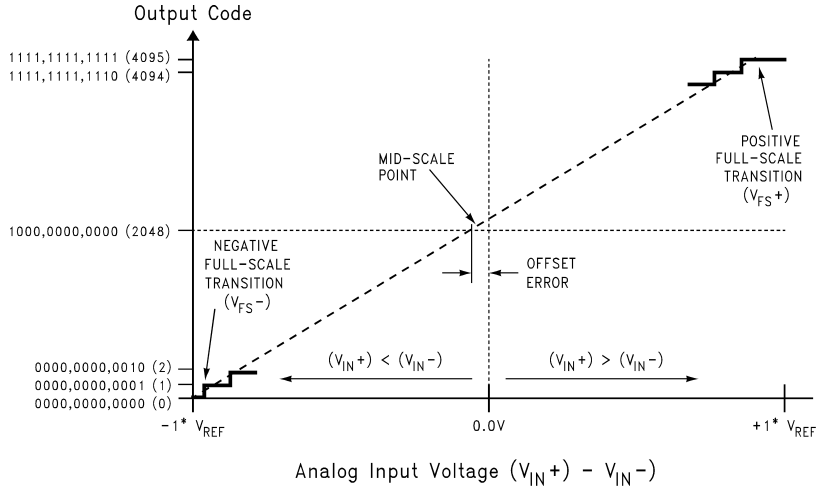


Figure 4. Transfer Characteristic

Typical Performance Characteristics DNL, INL

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +2.5V$, PD = 0V, External $V_{REF} = +1.0V$, $f_{CLK} = 80$ MHz, $f_{IN} = 0$, $C_L = 10$ pF/pin, Duty Cycle Stabilizer On. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_J = 25°C$

DNL

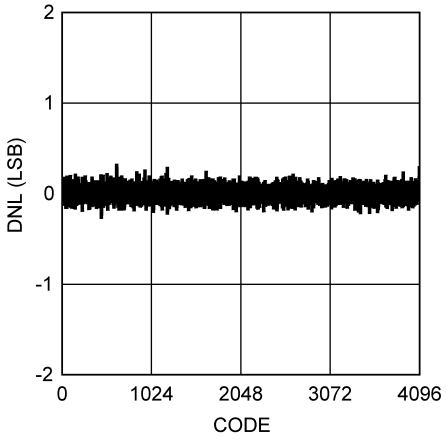


Figure 5.

INL

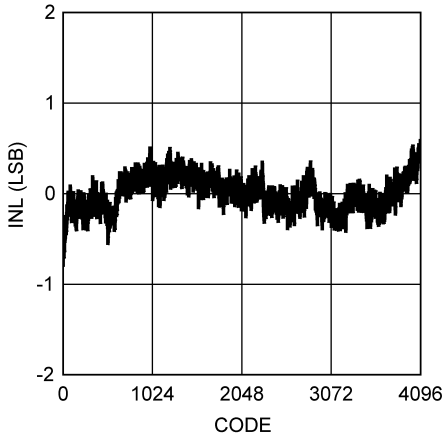


Figure 6.

DNL vs. f_{CLK}

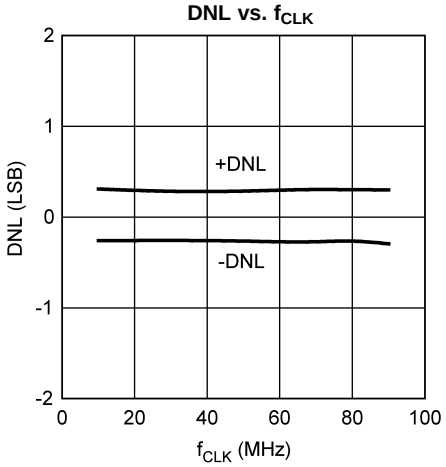


Figure 7.

INL vs. f_{CLK}

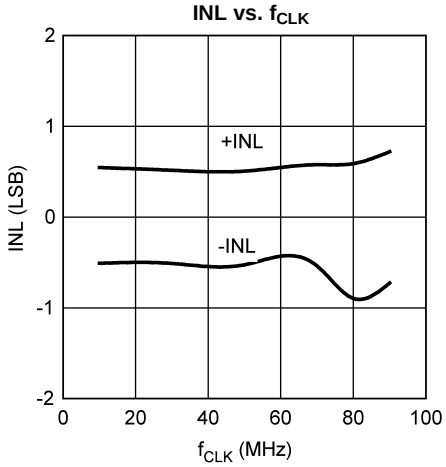


Figure 8.

DNL vs. Clock Duty Cycle

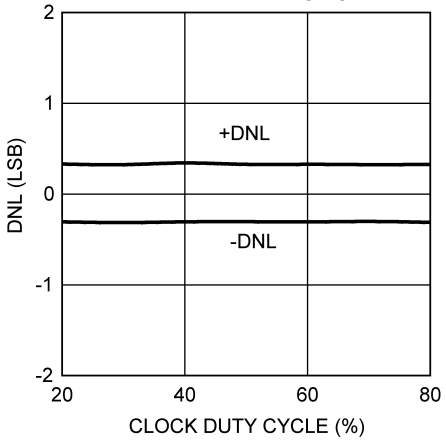


Figure 9.

INL vs. Clock Duty Cycle

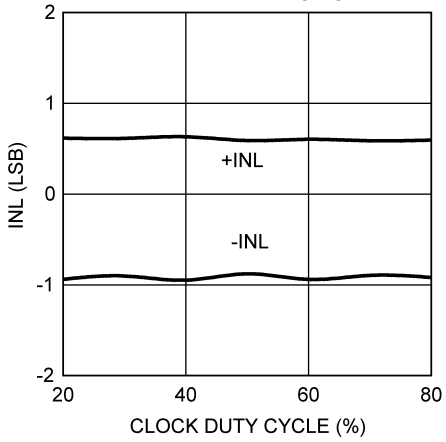


Figure 10.

Typical Performance Characteristics DNL, INL (continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, External V_{REF} = +1.0V, f_{CLK} = 80 MHz, f_{IN} = 0, C_L = 10 pF/pin, Duty Cycle Stabilizer On. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C

DNL vs. Temperature

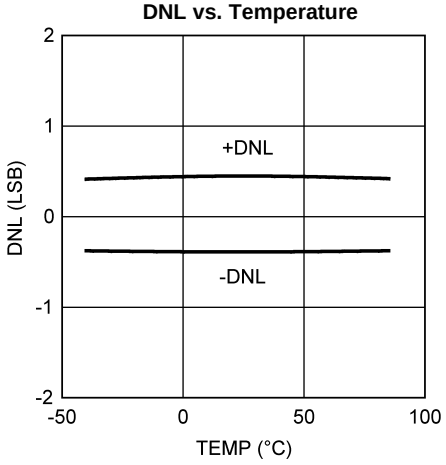


Figure 11.

INL vs. Temperature

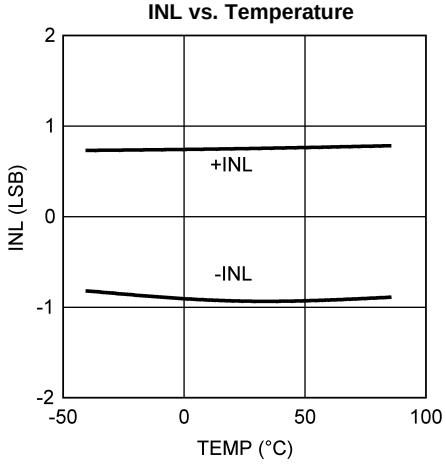


Figure 12.

DNL vs. V_{DR}, V_A = V_D = 3.6V

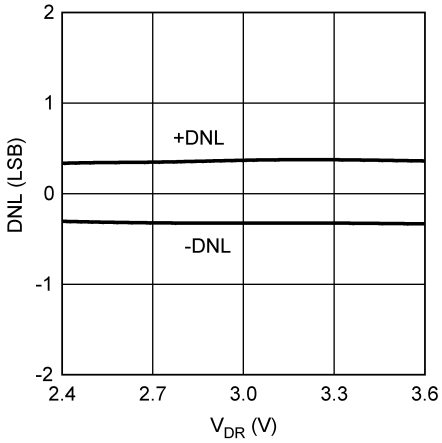


Figure 13.

INL vs. V_{DR}, V_A = V_D = 3.6V

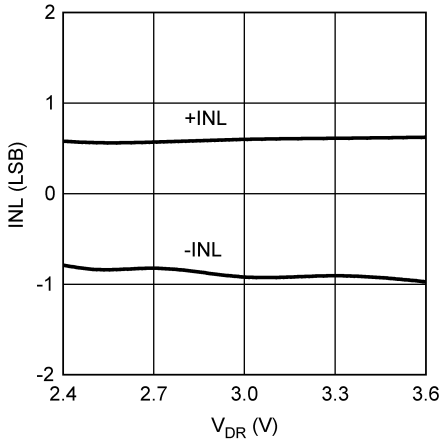


Figure 14.

DNL vs. V_A

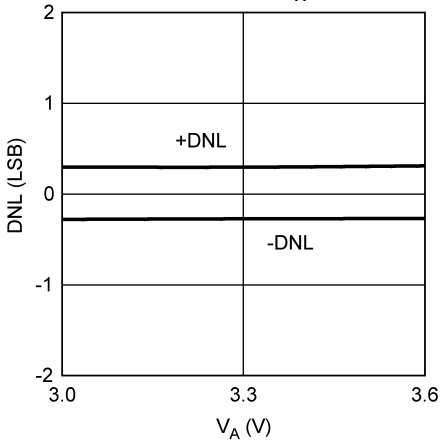


Figure 15.

INL vs. V_A

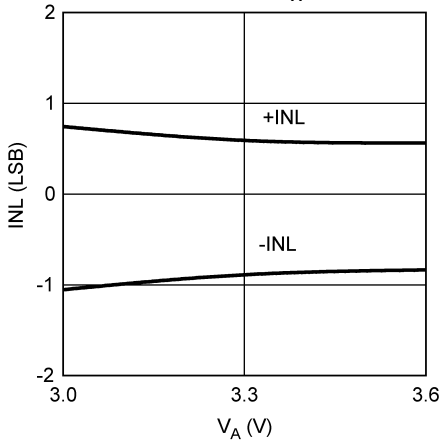


Figure 16.

Typical Performance Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, External V_{REF} = +1.0V, f_{CLK} = 80 MHz, f_{IN} = 40 MHz, C_L = 10 pF/pin, Duty Cycle Stabilizer On. Units for SNR and SINAD are dBFS. Units for SFDR and Distortion are dBc. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C

SNR, SINAD, SFDR vs. V_A

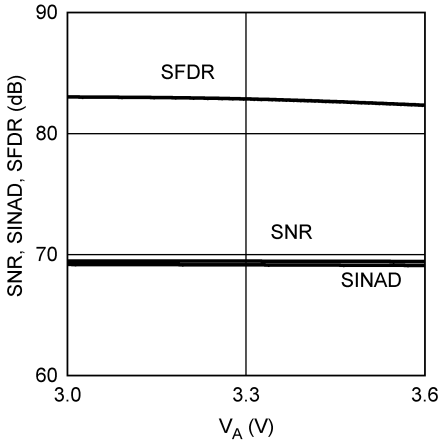


Figure 17.

Distortion vs. V_A

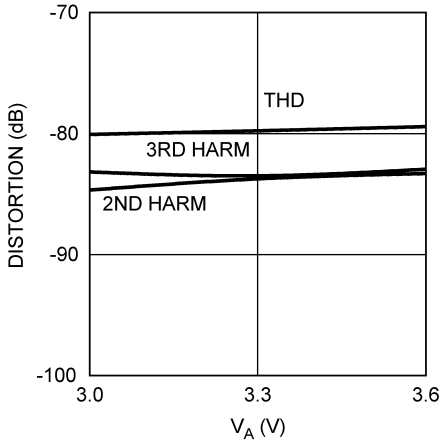


Figure 18.

SNR,SINAD,SFDR vs. V_{DR}, V_A = V_D = 3.6V

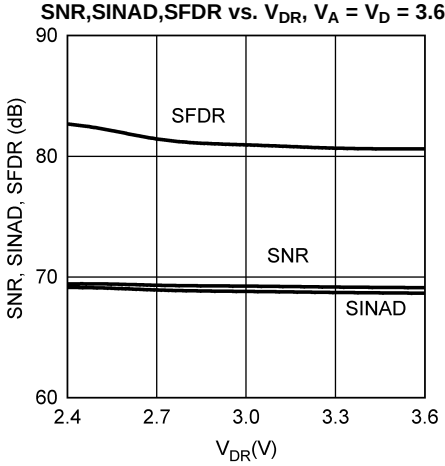


Figure 19.

Distortion vs. V_{DR}, V_A = V_D = 3.6V

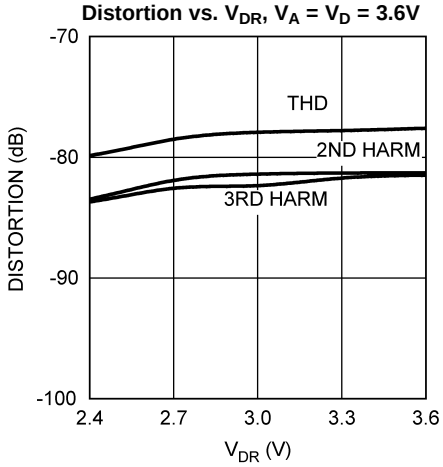


Figure 20.

SNR, SINAD, SFDR vs. V_{CM}

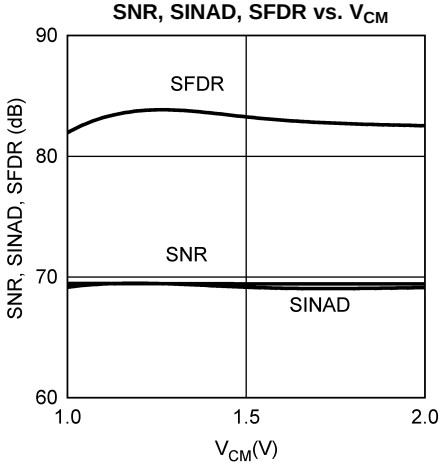


Figure 21.

Distortion vs. V_{CM}

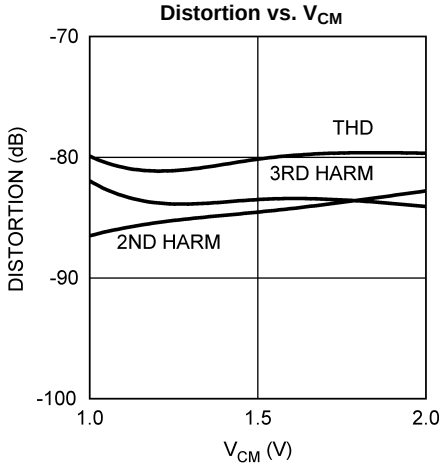


Figure 22.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, External V_{REF} = +1.0V, f_{CLK} = 80 MHz, f_{IN} = 40 MHz, C_L = 10 pF/pin, Duty Cycle Stabilizer On. Units for SNR and SINAD are dBFS. Units for SFDR and Distortion are dBc. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C

SNR, SINAD, SFDR vs. f_{CLK}

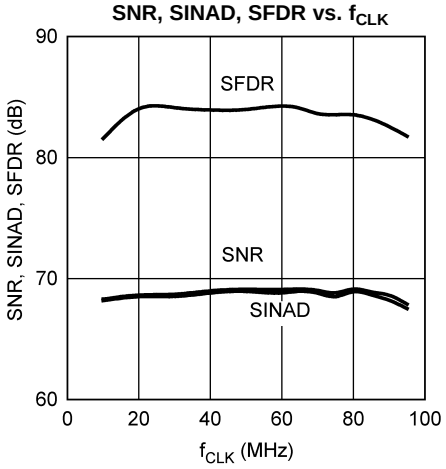


Figure 23.

Distortion vs. f_{CLK}

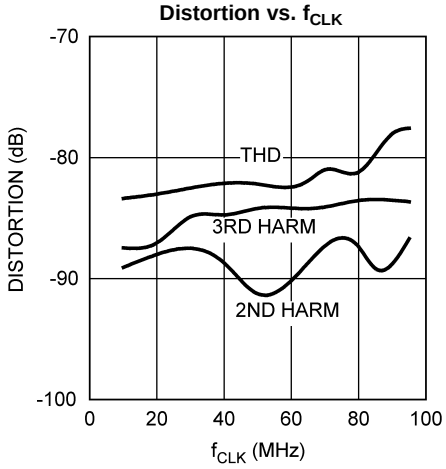


Figure 24.

SNR, SINAD, SFDR vs. Clock Duty Cycle

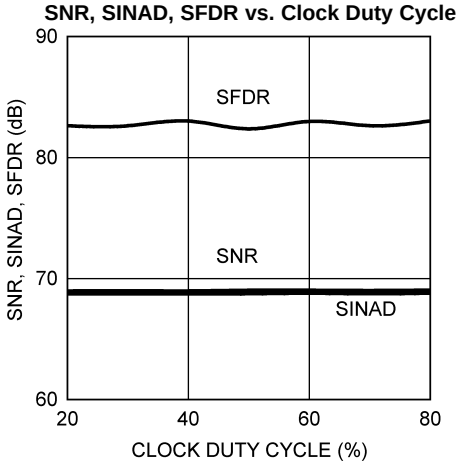


Figure 25.

Distortion vs. Clock Duty Cycle

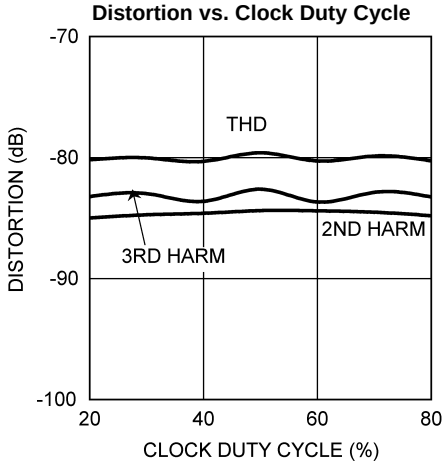


Figure 26.

SNR, SINAD, SFDR vs. Clock Duty Cycle (DCS=OFF)

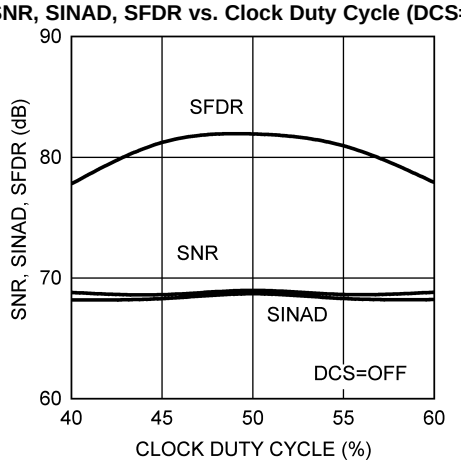


Figure 27.

Distortion vs. Clock Duty Cycle (DCS=OFF)

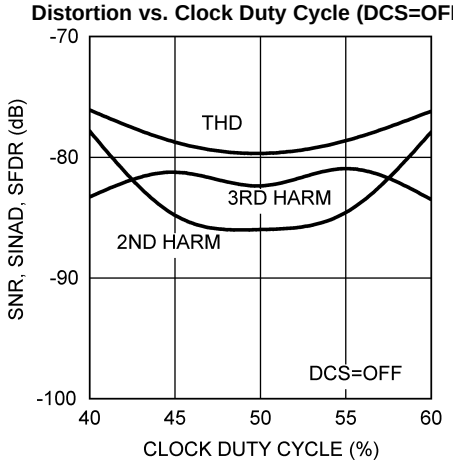


Figure 28.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, External V_{REF} = +1.0V, f_{CLK} = 80 MHz, f_{IN} = 40 MHz, C_L = 10 pF/pin, Duty Cycle Stabilizer On. Units for SNR and SINAD are dBFS. Units for SFDR and Distortion are dBc. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C

SNR, SINAD, SFDR vs. V_{REF}

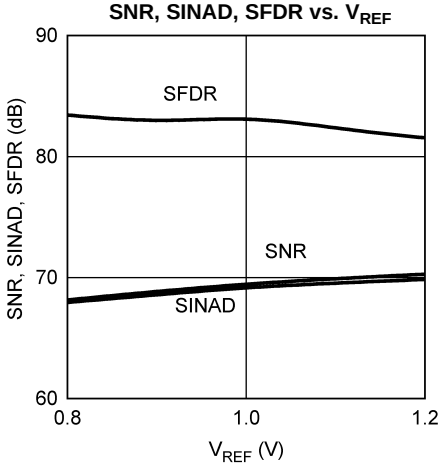


Figure 29.

Distortion vs. V_{REF}

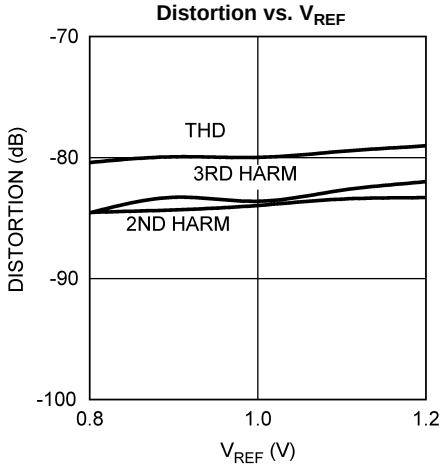


Figure 30.

SNR, SINAD, SFDR vs. f_{IN}

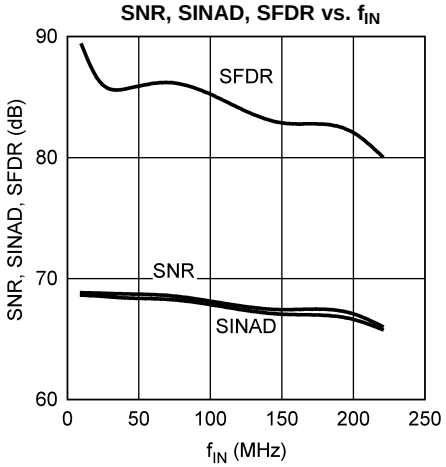


Figure 31.

Distortion vs. f_{IN}

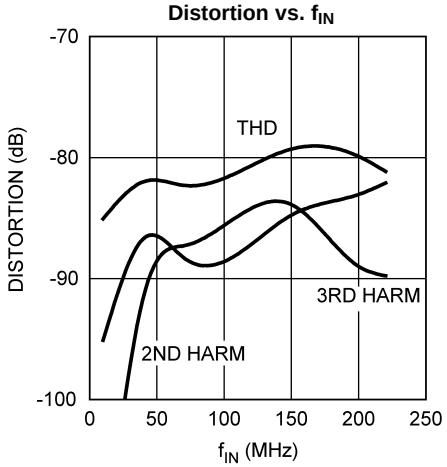


Figure 32.

SNR, SINAD, SFDR vs. Temperature

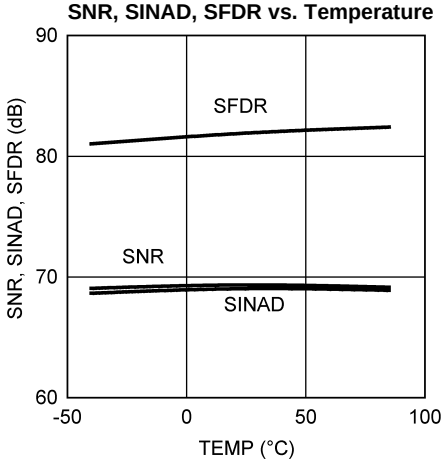


Figure 33.

Distortion vs. Temperature

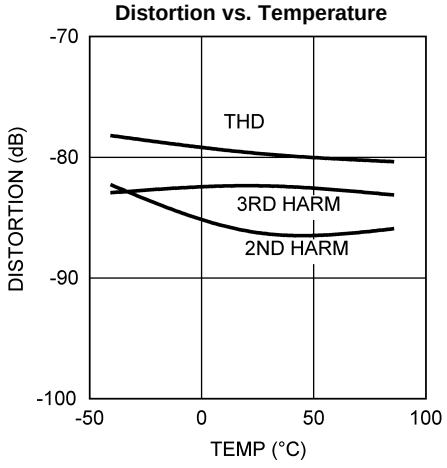


Figure 34.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, External V_{REF} = +1.0V, f_{CLK} = 80 MHz, f_{IN} = 40 MHz, C_L = 10 pF/pin, Duty Cycle Stabilizer On. Units for SNR and SINAD are dBFS. Units for SFDR and Distortion are dBc. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C

t_{OD} vs. V_{DR}, V_A = V_D = 3.6V

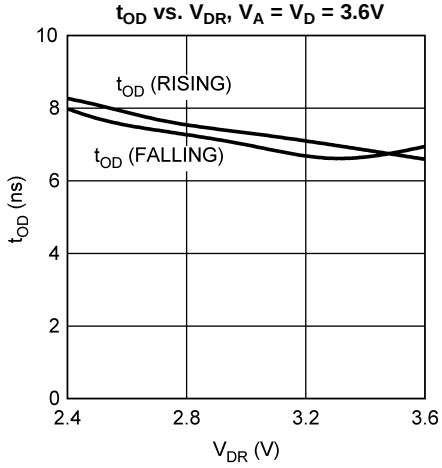


Figure 35.

Spectral Response @ 20 MHz Input

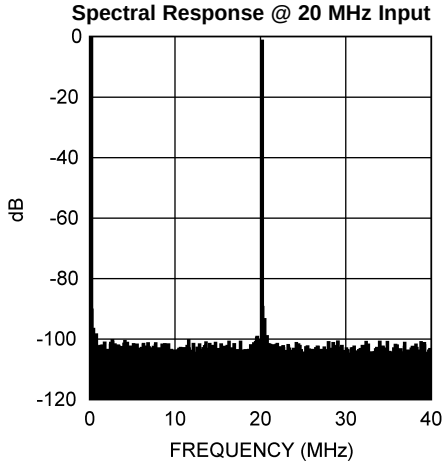


Figure 36.

Spectral Response @ 39 MHz Input

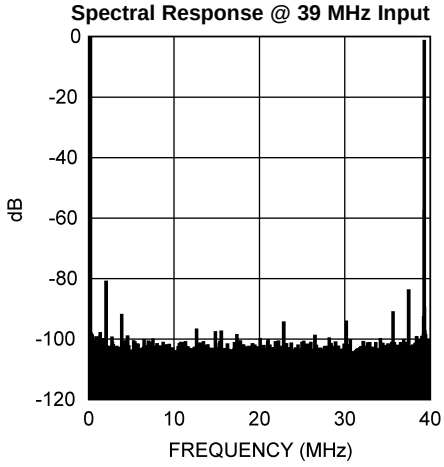


Figure 37.

Spectral Response @ 200 MHz Input

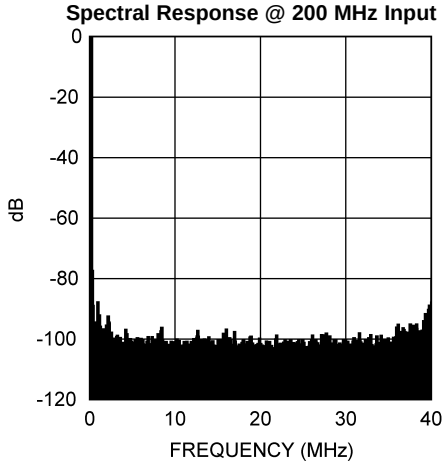


Figure 38.

Intermodulation Distortion, $f_{IN}1$= 19.6 MHz, $f_{IN}2$ = 20.2 MHz

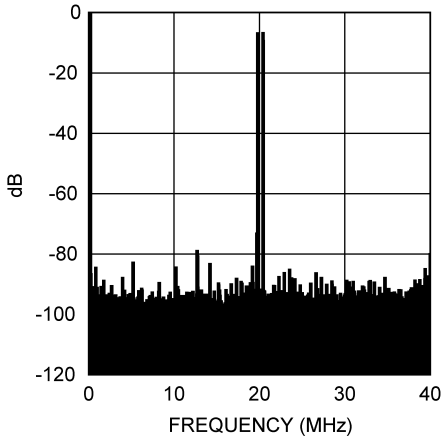


Figure 39.

Power Consumtion vs. f_{CLK}

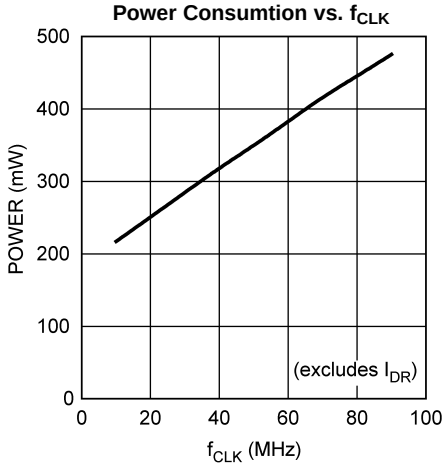


Figure 40.

FUNCTIONAL DESCRIPTION

Operating on a single +3.3V supply, the ADC12DL080 uses a pipeline architecture and has error correction circuitry to help ensure maximum performance. The differential analog input signal is digitized to 12 bits. The user has the choice of using an internal 1.0 Volt or an external reference. Any external reference is buffered on-chip to ease the task of driving that pin.

The output word rate is the same as the clock frequency, which can be between 10 MSPS and 80 MSPS (typical) with fully specified performance at 80 MSPS. The analog input for both channels is acquired at the rising edge of the clock and the digital data for a given sample is delayed by the pipeline for 7 clock cycles. Duty cycle stabilization and output data format are selectable. The output data format can be set for offset binary or two's complement.

A logic high on the power down (PD) pin reduces the converter power consumption to 50 mW.

APPLICATIONS INFORMATION

OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC12DL080:

$3.0V \le V_A \le 3.6V$

$V_D = V_A$

$2.4V \le V_{DR} \le V_D$

$10\ MHz \le f_{CLK} \le 80\ MHz$

$0.8V \le V_{REF} \le 1.2V$ (for an external reference)

$1.0V \le V_{CM} \le 2.0V$

Analog Inputs

There is one reference input pin, V_{REF}, which is used to select an internal reference, or to supply an external reference. The ADC12DL080 has two analog signal input pairs, V_{IN} A+ and V_{IN} A- for one converter and V_{IN} B+ and V_{IN} B- for the other converter. Each pair of pins forms a differential input pair.

Reference Pins

The ADC12DL080 is designed to operate with an internal 1.0V reference or an external 1.0V reference, but performs well with external reference voltages in the range of 0.8V to 1.2V. Lower reference voltages will decrease the signal-to-noise ratio (SNR) of the ADC12DL080. Increasing the reference voltage (and the input signal swing) beyond 1.2V may degrade THD for a full-scale input, especially at higher input frequencies.

It is important that all grounds associated with the reference voltage and the analog input signal make connection to the ground plane at a single, quiet point to minimize the effects of noise currents in the ground path.

The six Reference Bypass Pins (V_{RP}A, V_{RM}A, V_{RN}A, V_{RP}B, V_{RM}B and V_{RN}B) are made available for bypass purposes. All these pins should each be bypassed to ground with a 0.1 µF capacitor. A 10 µF capacitor should be placed between the V_{RP}A and V_{RN}A pins and between the V_{RP}B and V_{RN}B pins, as shown in Figure 43. This configuration is necessary to avoid reference oscillation, which could result in reduced SFDR and/or SNR.

Smaller capacitor values than those specified will allow faster recovery from the power down mode, but may result in degraded noise performance. Loading any of these pins other than V_{RM}A and V_{RM}B may result in performance degradation.

The nominal voltages for the reference bypass pins are as follows:

$V_{RM} = 1.5\ V$

$V_{RP} = V_{RM} + V_{REF} / 2$

$V_{RN} = V_{RM} - V_{REF} / 2$

User choice of an on-chip or external reference voltage is provided. The internal 1.0 Volt reference is in use when the the V_{REF} pin is connected to V_A. If a voltage in the range of 0.8V to 1.2V is applied to the V_{REF} pin, that is used for the voltage reference. When an external reference is used, the V_{REF} pin should be bypassed to ground with a 0.1 µF capacitor close to the reference input pin. There is no need to bypass the V_{REF} pin when the internal reference is used.

Signal Inputs

The signal inputs are V_{IN} A+ and V_{IN}A− for one ADC and V_{IN}B+ and V_{IN}B− for the other ADC . The input signal, V_{IN}, is defined as

$$V_{IN}\ A = (V_{IN}A+) - (V_{IN}A-) \quad (3)$$

for the "A" converter and

$$V_{IN}\ B = (V_{IN}B+) - (V_{IN}B-) \quad (4)$$

for the "B" converter. Figure 41 shows the expected input signal range. Note that the common mode input voltage, V_{CM}, should be in the range of 1.0V to 2.0V.

The peaks of the individual input signals should never exceed 2.6V.

The ADC12DL080 performs best with a differential input signal with each input centered around a common mode voltage, V_{CM}. The peak-to-peak voltage swing at each analog input pin should not exceed the value of the reference voltage or the output data will be clipped.

The two input signals should be exactly 180° out of phase from each other and of the same amplitude. For single frequency inputs, angular errors result in a reduction of the effective full scale input. For complex waveforms, however, angular errors will result in distortion.

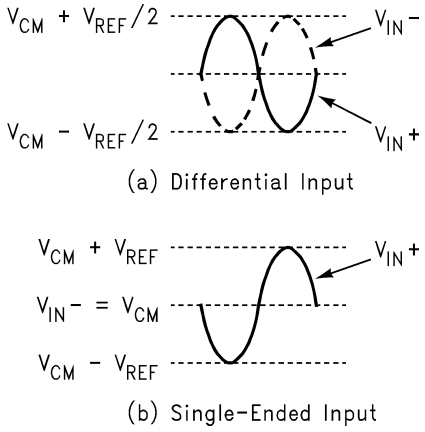


Figure 41. Expected Input Signal Range

For single frequency sine waves the full scale error in LSB can be described as approximately

$$E_{FS} = 4096\ (\ 1 - \sin\ (90° + dev)) \quad (5)$$

Where dev is the angular difference in degrees between the two signals having a 180° relative phase relationship to each other (see Figure 42). Drive the analog inputs with a source impedance less than 100Ω.

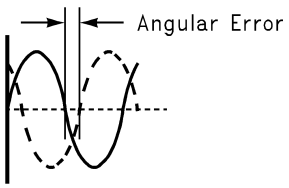


Figure 42. Angular Errors Between the Two Input Signals Will Reduce the Output Level or Cause Distortion

For differential operation, each analog input pin of the differential pair should have a peak-to-peak voltage equal to the reference voltage, V_{REF}, be 180 degrees out of phase with each other and be centered around V_{CM}.

Single-Ended Operation

Performance with differential input signals is better than with single-ended signals. For this reason, single-ended operation is not recommended. However, if single ended-operation is required and the resulting performance degradation is acceptable, one of the analog inputs should be connected to the d.c. mid point voltage of the driven input. The peak-to-peak input signal at the driven input pin should be twice the reference voltage to maximize SNR and SINAD performance (Figure 41*b*). For example, set V_{REF} to 1.0V, bias V_{IN}− to 1.5V and drive V_{IN}+ with a signal range of 0.5V to 2.5V.

Because very large input signal swings can degrade distortion performance, better performance with a single-ended input can be obtained by reducing the reference voltage when maintaining a full-range output. Table 1 and Table 2 indicate the input to output relationship of the ADC12DL080.

Table 1. Input to Output Relationship – Differential Input

V_{IN}^+	V_{IN}^-	Binary Output	2's Complement Output
$V_{CM} - V_{REF}/2$	$V_{CM} + V_{REF}/2$	0000 0000 0000	1000 0000 0000
$V_{CM} - V_{REF}/4$	$V_{CM} + V_{REF}/4$	0100 0000 0000	1100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000	0000 0000 0000
$V_{CM} + V_{REF}/4$	$V_{CM} - V_{REF}/4$	1100 0000 0000	0100 0000 0000
$V_{CM} + V_{REF}/2$	$V_{CM} - V_{REF}/2$	1111 1111 1111	0111 1111 1111

Table 2. Input to Output Relationship – Single-Ended Input

V_{IN}^+	V_{IN}^-	Binary Output	2's Complement Output
$V_{CM} - V_{REF}$	V_{CM}	0000 0000 0000	1000 0000 0000
$V_{CM} - V_{REF}/2$	V_{CM}	0100 0000 0000	1100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000	0000 0000 0000
$V_{CM} + V_{REF}/2$	V_{CM}	1100 0000 0000	0100 0000 0000
$V_{CM} + V_{REF}$	V_{CM}	1111 1111 1111	0111 1111 1111

Driving the Analog Inputs

The V_{IN}+ and the V_{IN}− inputs of the ADC12DL080 consist of an analog switch followed by a switched-capacitor amplifier. As the internal sampling switch opens and closes, current pulses occur at the analog input pins, resulting in voltage spikes at the signal input pins. As the driving source attempts to counteract these voltage spikes, it may add noise to the signal at the ADC analog input. To help isolate the pulses at the ADC input from the amplifier output, use RCs at the inputs, as can be seen in Figure 43 and Figure 44. These components should be placed close to the ADC inputs because the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter that input.

For Nyquist applications the RC pole should be at the ADC sample rate. The ADC input capacitance in the sample mode should be considered when setting the RC pole. For wideband undersampling applications, the RC pole should be set at about 1.5 to 2 times the maximum input frequency to maintain a linear delay response. The values of the RC shown in Figure 43 and Figure 44 are suitable for applications with input frequencies up to approximately 70MHz.

Input Common Mode Voltage

The input common mode voltage, V_{CM}, should be in the range of 1.0V to 2.0V and be a value such that the peak excursions of the analog signal does not go more negative than ground or more positive than 2.6V. See Reference Pins.

DIGITAL INPUTS

Digital TTL/CMOS compatible inputs consist of CLK, REFSEL/DCS, OF/DOEN, $\overline{OEA}$/OF, $\overline{OEB}$/DRDY. The $\overline{OEB}$/DRDY pin may also be configured as the DRDY output.

CLK

The **CLK** signal controls the timing of the sampling process. Drive the clock input with a stable, low jitter clock signal in the range of 10 MHz to 80 MHz. The higher the input frequency, the more critical it is to have a low jitter clock. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°.

The **CLK** signal also drives an internal state machine. If the **CLK** is interrupted, or its frequency too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the lowest sample rate.

The clock line should be terminated at its source in the characteristic impedance of that line. Take care to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 for information on setting characteristic impedance.

It is highly desirable that the the source driving the ADC **CLK** pin only drive that pin. However, if that source is used to drive other things, each driven pin should be a.c. terminated with a series RC to ground such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PD} \times L}{Z_o} \tag{6}$$

where t_{PD} is the signal propagation rate down the clock line, "L" is the line length and Z_O is the characteristic impedance of the clock line. This termination should be as close as possible to the ADC clock pin but beyond it as seen from the clock source. Typical t_{PD} is about 150 ps/inch (60 ps/cm) on FR-4 board material. The units of "L" and t_{PD} should be the same (inches or centimeters).

The duty cycle of the clock signal can affect the performance of the A/D Converter. Because achieving a precise duty cycle is difficult, the ADC12DL080 has a Duty Cycle Stabilizer which can be enabled using the REFSEL/DCS pin. It is designed to maintain performance over a clock duty cycle range of 30% to 70% at 80 MSPS.

REFSEL/DCS

This pin is used in conjunction with V_{REF} (pin 7) to select the reference source and turn the Duty Cycle Stabilizer (DCS) on or off.

When REFSEL/DCS is LOW and V_{REF} is HIGH, the internal 1.0V reference is selected and DCS is On.

When REFSEL/DCS is HIGH, an external reference voltage in the range of 0.8V to 1.2V should be applied to the VREF input. DCS is On.

With this pin connected to V_{RM}A or V_{RM}B, DCS is Off.

When enabled, duty cycle stabilization can compensate for clock inputs with duty cycles ranging from 30% to 70% and generate a stable internal clock, improving the performance of the part.

Table 3. V_{REF}, REFSEL/DCS Pin Functions

REFSEL/DCS (pin 11)	V_{REF} (pin 7)	Reference	DCS
Logic LOW	Logic HIGH	Internal 1.0 V	ON
Logic High	0.8 to 1.2V	External	ON
V_{RM}A or V_{RM}B	Logic High	Internal 1.0V	OFF
V_{RM}A or V_{RM}B	0.8 to 1.2V	External	OFF

OF/DOEN, $\overline{OEA}$/OF, and $\overline{OEB}$/DRDY

OF/DOEN (pin 21) selects the output format (OF) or enables the DRDY output (DOEN). The state of this pin also controls the function of pins 22 ($\overline{OEA}$/OF) and 41 ($\overline{OEB}$/DRDY).

When OF/DOEN is tied to $V_{RM}A$ or $V_{RM}B$, DRDY is enabled. Pin 41 is used as the DRDY output strobe, and pin 22 is used to select the output format. Output Enable for channels A and B are not available in this mode.

When OF/DOEN is LOW, the output data format is offset binary. With OF/DOEN tied HIGH, the output format is 2's complement.

The following table describes the function of these pins.

Table 4. OF/DOEN, $\overline{OEA}$/OF, $\overline{OEB}$/DRDY Pin Functions

Pin 21 State	Pin 21 Function	Pin 22 Function	Pin 41 Function
$V_{RM}A$ or $V_{RM}B$	DRDY output is enabled	Output Format LOW = Offset Binary HIGH = 2's Complement	DRDY Output
Logic LOW	Output Format = Offset Binary	Output Enable for Channel A LOW = outputs are enabled HIGH = outputs are in high impedance state	Output Enable for Channel B LOW = outputs are enabled HIGH = outputs are in high impedance state
Logic HIGH	Output Format = 2's Complement		

PD

The PD pin, when high, holds the ADC12DL080 in a power-down mode to conserve power when the converter is not being used. The output data pins are undefined and the data in the pipeline is corrupted while in the power down mode.

The Power Down Mode Exit Cycle time is determined by the value of the components on pins 4, 5, 6, 12, 13 and 14. These capacitors loose their charge in the Power Down mode and must be recharged by on-chip circuitry before conversions can be accurate. Smaller capacitor values allow slightly faster recovery from the power down mode, but can result in a reduction in SNR, SINAD and ENOB performance.

OUTPUTS

The ADC12DL080 has 12 TTL/CMOS compatible Data Output pins for each output. Valid data is present at these outputs while the $\overline{OE}$ and PD pins are low. Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can cause on-chip ground noise and couple into the analog circuitry, degrading dynamic performance. Adequate bypassing, limiting output capacitance and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond the specified 10 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could be an apparent reduction in dynamic performance.

To minimize noise due to output switching, minimize the load currents at the digital outputs. This can be done by connecting buffers (74LVTH162374, for example) between the ADC outputs and any other circuitry. Only one driven input should be connected to each output pin. Additionally, inserting series resistors of about 100Ω at the digital outputs, close to the ADC pins, will isolate the outputs from trace and other circuit capacitances and limit the output currents, which could otherwise result in performance degradation. See Figure 43.

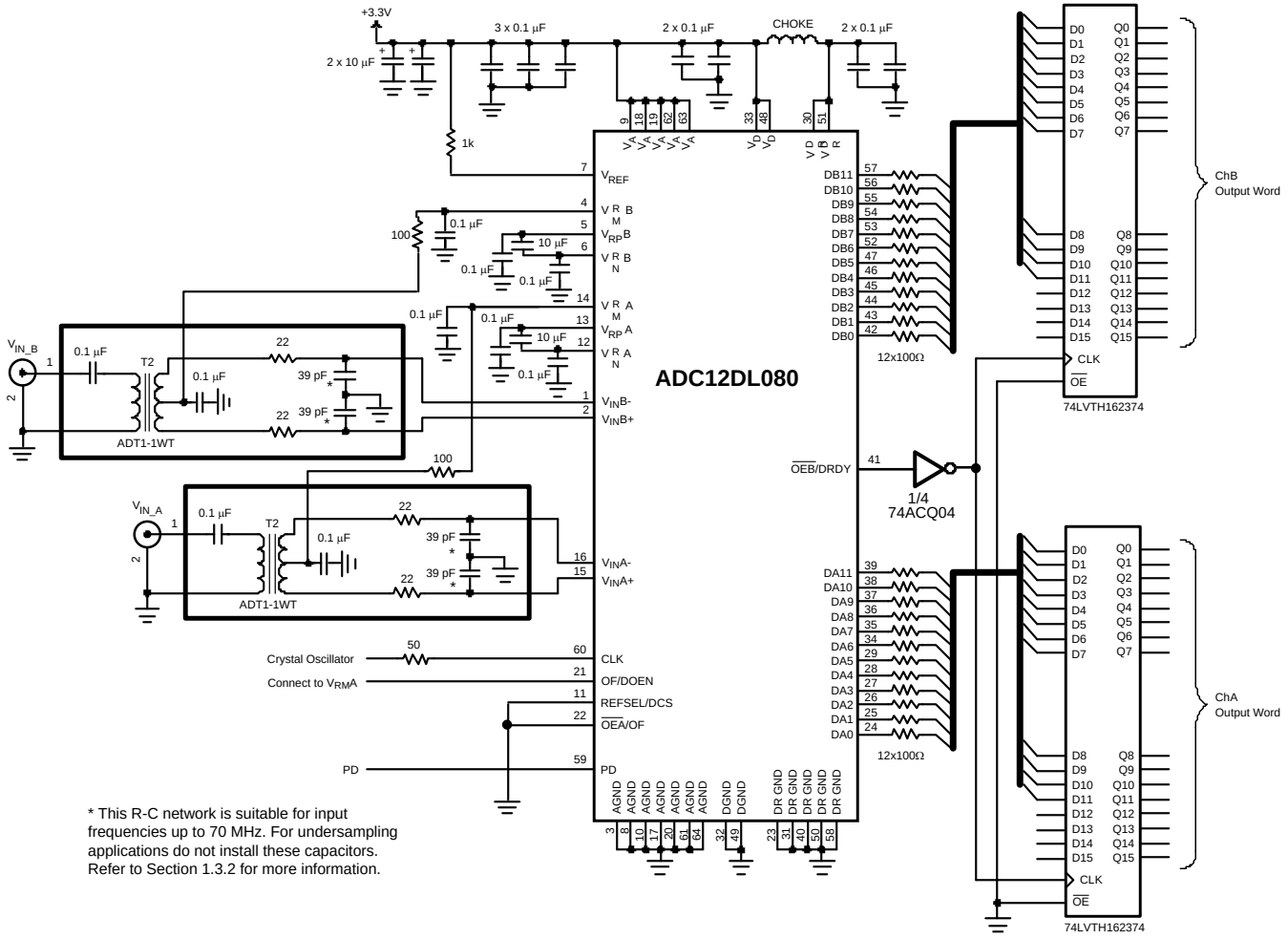


Figure 43. Application Circuit using Transformer Drive Circuit

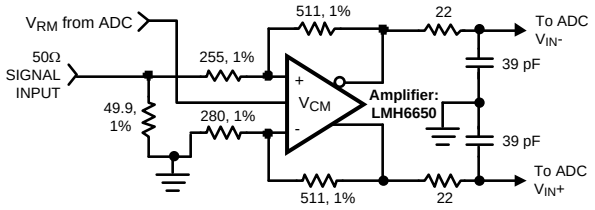


Figure 44. Optional Amplifier Drive for Circuit in Figure 43

POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 10 µF capacitor and with a 0.1 µF ceramic chip capacitor near each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC12DL080 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during power turn on and turn off.

The V_{DR} pin provides power for the output drivers and may be operated from a supply in the range of 2.4V to V_D. This can simplify interfacing to lower voltage devices and systems. Note, however, that t_{OD} increases with reduced V_{DR}. **DO NOT operate the V_{DR} pin at a voltage higher than V_D.**

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC12DL080 between these areas, is required to achieve specified performance.

The ground return for the data outputs (DR GND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DR GND pins should NOT be connected to system ground in close proximity to any of the ADC12DL080's other ground pins.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74LS, 74HC(T) and 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families.

The effects of the noise generated from the ADC output switching can be minimized through the use of 100Ω resistors in series with each data output line. Locate these resistors as close to the ADC output pins as possible.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90° crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

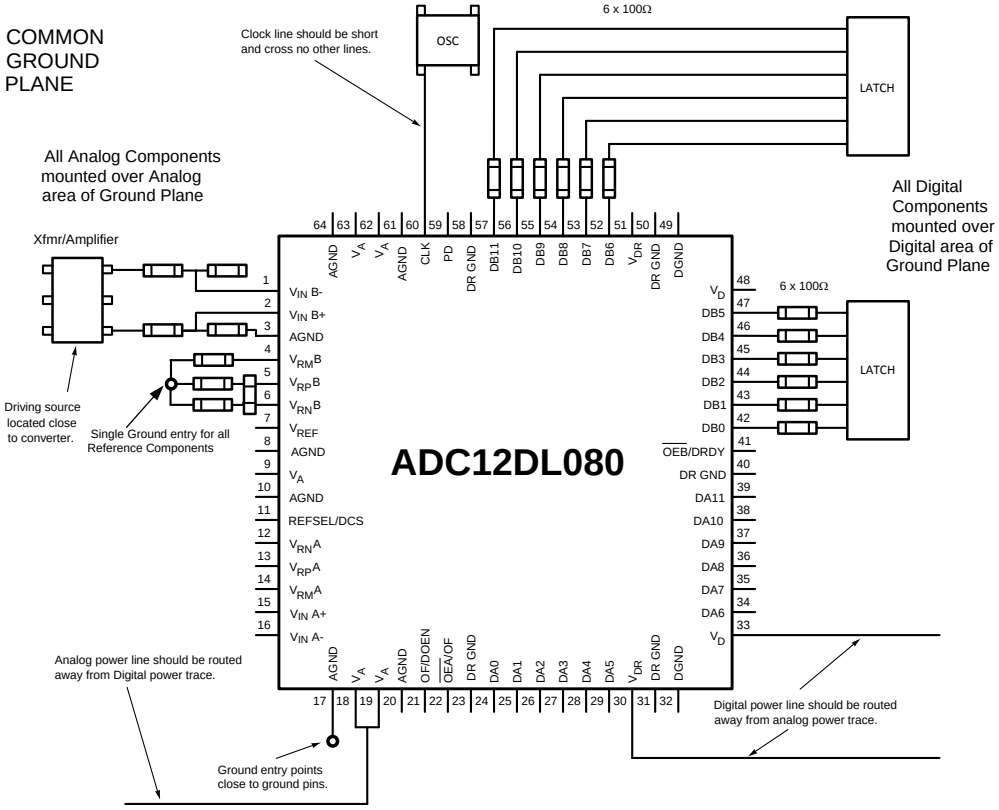


Figure 45. Example of a Suitable Layout

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should *not* be placed side by side, even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

Figure 45 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed in the analog area of the board. All digital circuitry and I/O lines should be placed in the digital area of the board. The ADC12DL080 should be between these two areas. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single, quiet point. All ground connections should have a low inductance path to ground.

DYNAMIC PERFORMANCE

To achieve the best dynamic performance, the clock source driving the CLK input must be free of jitter. Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in Figure 46. The gates used in the clock tree must be capable of operating at frequencies much higher than those used if added jitter is to be prevented.

Best performance will be obtained with a differential input drive, compared with a single-ended drive, as discussed in Single-Ended Operation and Driving the Analog Inputs.

As mentioned in LAYOUT AND GROUNDING, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

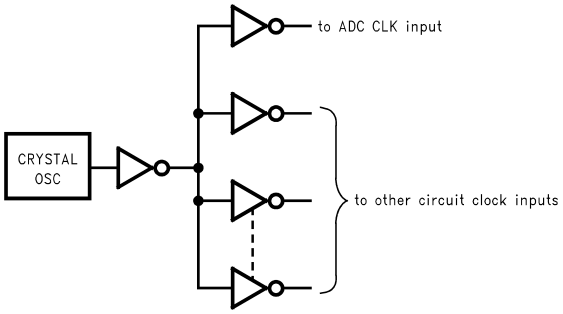


Figure 46. Isolating the ADC Clock from other Circuitry with a Clock Tree

7.0 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 100 mV beyond the supply rails (more than 100 mV below the ground pins or 100 mV above the supply pins). Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital components (e.g., 74F and 74AC devices) to exhibit overshoot or undershoot that goes above the power supply or below ground. A resistor of about 47Ω to 100Ω in series with any offending digital input, close to the signal source, will eliminate the problem.

Do not allow input voltages to exceed the supply voltage, even on a transient basis. Not even during power up or power down.

Be careful not to overdrive the inputs of the ADC12DL080 with a device that is powered from supplies outside the range of the ADC12DL080 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can couple into the analog circuitry, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital areas on the pc board will reduce this problem. Additionally, bus capacitance beyond the specified 10 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could, again, be an apparent reduction in dynamic performance.

The digital data outputs should be buffered (with 74ACQ541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC12DL080, which reduces the energy coupled back into the converter output pins by limiting the output current. A reasonable value for these resistors is 100Ω.

Using an inadequate amplifier to drive the analog input. As explained in Signal Inputs, the capacitance seen at the input alternates between 8 pF and 7 pF, depending upon the phase of the clock. This dynamic load is more difficult to drive than is a fixed capacitance. If the amplifier exhibits overshoot, ringing, or any evidence of instability, even at a very low level, it will degrade performance. A small series resistor at each amplifier output and a capacitor at the analog inputs (as shown in Figure 44) will improve performance.

Also, it is important that the signals at the two inputs have exactly the same amplitude and be exactly 180º out of phase with each other. Board layout, especially equality of the length of the two traces to the input pins, will affect the effective phase between these two signals. Remember that an operational amplifier operated in the non-inverting configuration will exhibit more time delay than will the same device operating in the inverting configuration.

Operating with the reference pins outside of the specified range. As mentioned in Reference Pins, V_{REF} should be in the range of

$$0.8V \le V_{REF} \le 1.2V \quad (7)$$

Operating outside of these limits could lead to performance degradation.

Inadequate network on Reference Bypass pins (V_{RP}A, V_{RN}A, V_{RM}A, V_{RP}B, V_{RN}B and V_{RM}B). As mentioned in Reference Pins, these pins should be bypassed with 0.1 µF capacitors to ground at V_{RM}A and V_{RM}B and with a 10 µF between pins V_{RP}A and V_{RN}A and between V_{RP}B and V_{RN}B for best performance.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR and SINAD performance.

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	29

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC12DL080CIVS/NO.A	Active	Production	TQFP (PAG) | 64	160 | EIAJ TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12DL080 CIVS
ADC12DL080CIVS/NOPB	Active	Production	TQFP (PAG) | 64	160 | EIAJ TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADC12DL080 CIVS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

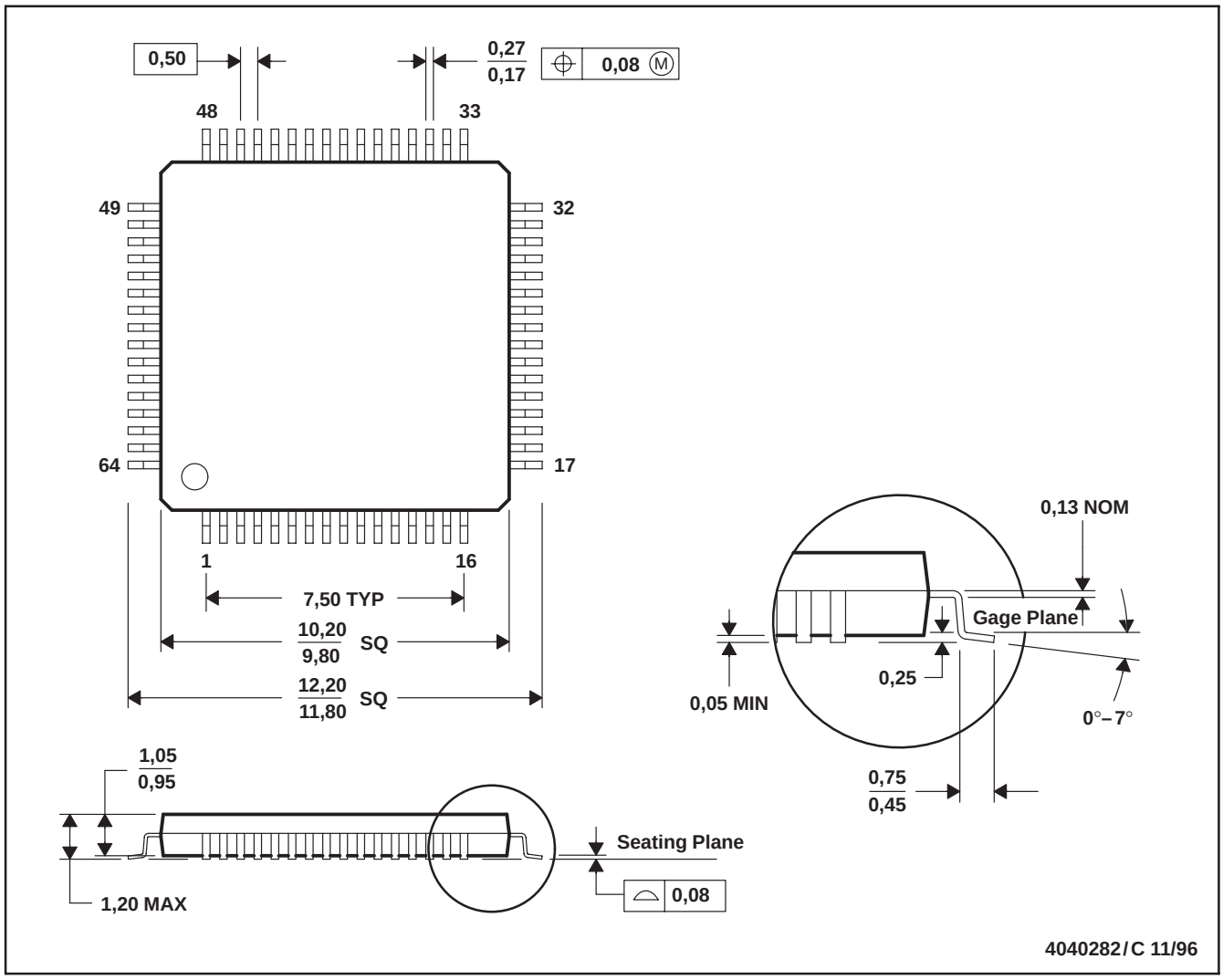
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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