

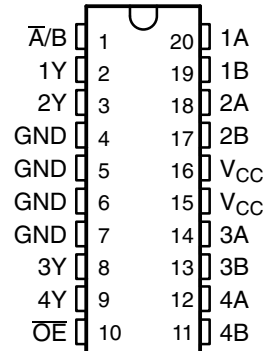
# 74AC11257

## QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS049C – MARCH 1989 – REVISED MAY 2004

- 3-State Outputs Interface Directly With System Bus
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- 500-mA Typical Latch-Up Immunity at 125°C
- Provides Bus Interface From Multiple Sources in High-Performance Systems

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



### description/ordering information

This device is designed to multiplex signals from 4-bit data sources to four output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ( $\overline{OE}$ ) input is at a high logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### ORDERING INFORMATION

| $T_A$         | PACKAGE†   |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------|---------------|-----------------------|------------------|
| –40°C to 85°C | PDIP – N   | Tube          | 74AC11257N            | 74AC11257N       |
|               | SOIC – DW  | Tube          | 74AC11257DW           | AC11257          |
|               |            | Tape and reel | 74AC11257DWR          |                  |
|               | SSOP – DB  | Tape and reel | 74AC11257DBR          | AE257            |
|               | TSSOP – PW | Tube          | 74AC11257PW           | AE257            |
|               |            | Tape and reel | 74AC11257PWR          |                  |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLE

| INPUTS |               |      |   | OUTPUT<br>Y |
|--------|---------------|------|---|-------------|
| OE     | SELECT<br>A/B | DATA |   |             |
|        |               | A    | B |             |
| H      | X             | X    | X | Z           |
| L      | L             | L    | X | L           |
| L      | L             | H    | X | H           |
| L      | H             | X    | L | L           |
| L      | H             | X    | H | H           |



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 **TEXAS  
INSTRUMENTS**

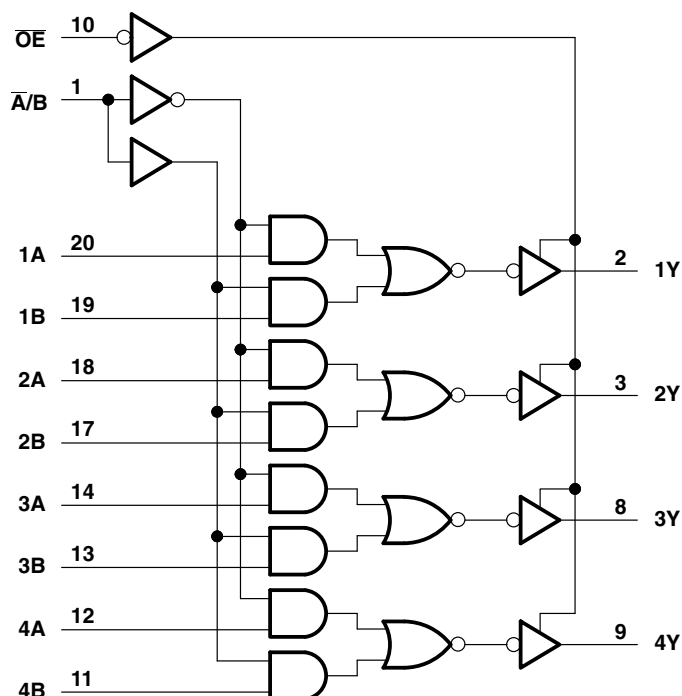
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# QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS049C – MARCH 1989 – REVISED MAY 2004

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                |                            |
|----------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$                                 | –0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1)                        | –0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, $V_O$ (see Note 1)                       | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )  | ±20 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) | ±50 mA                     |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )     | ±50 mA                     |
| Continuous current through $V_{CC}$ or GND                     | ±100 mA                    |
| Package thermal impedance, $\theta_{JA}$ (see Note 2):         |                            |
| DB package                                                     | 70°C/W                     |
| DW package                                                     | 58°C/W                     |
| N package                                                      | 60°C/W                     |
| PW package                                                     | 83°C/W                     |

Storage temperature range,  $T_{stg}$  ..... –65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**74AC11257**  
**QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER**  
**WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 3)**

|                     |                                    | MIN                     | NOM  | MAX      | UNIT |
|---------------------|------------------------------------|-------------------------|------|----------|------|
| $V_{CC}$            | Supply voltage                     | 3                       | 5    | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 3\text{ V}$   | 2.1  |          | V    |
|                     |                                    | $V_{CC} = 4.5\text{ V}$ | 3.15 |          |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$ | 3.85 |          |      |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 3\text{ V}$   |      | 0.9      | V    |
|                     |                                    | $V_{CC} = 4.5\text{ V}$ |      | 1.35     |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$ |      | 1.65     |      |
| $V_I$               | Input voltage                      | 0                       |      | $V_{CC}$ | V    |
| $V_O$               | Output voltage                     | 0                       |      | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          | $V_{CC} = 3\text{ V}$   |      | –4       | mA   |
|                     |                                    | $V_{CC} = 4.5\text{ V}$ |      | –24      |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$ |      | –24      |      |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 3\text{ V}$   |      | 12       | mA   |
|                     |                                    | $V_{CC} = 4.5\text{ V}$ |      | 24       |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$ |      | 24       |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |                         |      | 10       | ns/V |
| $T_A$               | Operating free-air temperature     | –40                     |      | 85       | °C   |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS                   | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     |           | MIN  | MAX     | UNIT          |
|-----------|-----------------------------------|----------|--------------------------|-----|-----------|------|---------|---------------|
|           |                                   |          | MIN                      | TYP | MAX       |      |         |               |
| $V_{OH}$  | $I_{OH} = -50\text{ }\mu\text{A}$ | 3 V      | 2.9                      |     |           | 2.9  |         | V             |
|           |                                   | 4.5 V    | 4.4                      |     |           | 4.4  |         |               |
|           |                                   | 5.5 V    | 5.4                      |     |           | 5.4  |         |               |
|           | $I_{OH} = -4\text{ mA}$           | 3 V      | 2.58                     |     |           | 2.48 |         |               |
|           |                                   | 4.5 V    | 3.94                     |     |           | 3.8  |         |               |
|           | $I_{OH} = -24\text{ mA}$          | 5.5 V    | 4.94                     |     |           | 4.8  |         |               |
|           |                                   | 5.5 V    |                          |     |           | 3.85 |         |               |
| $V_{OL}$  | $I_{OL} = 50\text{ }\mu\text{A}$  | 3 V      |                          |     | 0.1       |      | 0.1     | V             |
|           |                                   | 4.5 V    |                          |     | 0.1       |      | 0.1     |               |
|           |                                   | 5.5 V    |                          |     | 0.1       |      | 0.1     |               |
|           | $I_{OL} = 12\text{ mA}$           | 3 V      |                          |     | 0.36      |      | 0.44    |               |
|           |                                   | 4.5 V    |                          |     | 0.36      |      | 0.44    |               |
|           | $I_{OL} = 24\text{ mA}$           | 5.5 V    |                          |     | 0.36      |      | 0.44    |               |
|           |                                   | 5.5 V    |                          |     |           |      | 1.65    |               |
| $I_{OZ}$  | $V_O = V_{CC}$ or GND             | 5.5 V    |                          |     | $\pm 0.5$ |      | $\pm 5$ | $\mu\text{A}$ |
| $I_I$     | $V_I = V_{CC}$ or GND             | 5.5 V    |                          |     | $\pm 0.1$ |      | $\pm 1$ | $\mu\text{A}$ |
| $I_{CC}$  | $V_I = V_{CC}$ or GND, $I_O = 0$  | 5.5 V    |                          |     | 8         |      | 80      | $\mu\text{A}$ |
| $C_i$     | $V_I = V_{CC}$ or GND             | 5 V      |                          | 3.5 |           |      |         | pF            |
| $C_o$     | $V_O = V_{CC}$ or GND             | 5.5 V    |                          | 8   |           |      |         | pF            |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



# QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | $T_A = 25^\circ\text{C}$ |     |      | MIN | MAX  | UNIT |
|-----------|-----------------|----------------|--------------------------|-----|------|-----|------|------|
|           |                 |                | MIN                      | TYP | MAX  |     |      |      |
| $t_{PLH}$ | A or B          | Y              | 1.5                      | 5.6 | 8.1  | 1.5 | 8.9  | ns   |
| $t_{PHL}$ |                 |                | 1.5                      | 6.2 | 9    | 1.5 | 10.1 |      |
| $t_{PLH}$ | $\bar{A}/B$     | Any Y          | 1.5                      | 6.1 | 9.2  | 1.5 | 10.2 | ns   |
| $t_{PHL}$ |                 |                | 1.5                      | 6.6 | 10   | 1.5 | 11.2 |      |
| $t_{PZH}$ | $\bar{OE}$      | Any Y          | 1.5                      | 5.6 | 8.2  | 1.5 | 9.1  | ns   |
| $t_{PZL}$ |                 |                | 1.5                      | 7.5 | 10.4 | 1.5 | 11.8 |      |
| $t_{PHZ}$ | $\bar{OE}$      | Any Y          | 1.5                      | 5.6 | 7.6  | 1.5 | 8.3  | ns   |
| $t_{PLZ}$ |                 |                | 1.5                      | 6.2 | 8.8  | 1.5 | 9.6  |      |

switching characteristics, over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | $T_A = 25^\circ\text{C}$ |     |     | MIN | MAX | UNIT |
|-----------|-----------------|----------------|--------------------------|-----|-----|-----|-----|------|
|           |                 |                | MIN                      | TYP | MAX |     |     |      |
| $t_{PLH}$ | A or B          | Y              | 1.5                      | 3.6 | 5.8 | 1.5 | 6.4 | ns   |
| $t_{PHL}$ |                 |                | 1.5                      | 4.1 | 6.5 | 1.5 | 7.2 |      |
| $t_{PLH}$ | $\bar{A}/B$     | Any Y          | 1.5                      | 4   | 6.5 | 1.5 | 7.2 | ns   |
| $t_{PHL}$ |                 |                | 1.5                      | 4.4 | 7.1 | 1.5 | 7.9 |      |
| $t_{PZH}$ | $\bar{OE}$      | Any Y          | 1.5                      | 3.8 | 5.9 | 1.5 | 6.5 | ns   |
| $t_{PZL}$ |                 |                | 1.5                      | 5   | 7.6 | 1.5 | 8.6 |      |
| $t_{PHZ}$ | $\bar{OE}$      | Any Y          | 1.5                      | 4.5 | 6.4 | 1.5 | 7.6 | ns   |
| $t_{PLZ}$ |                 |                | 1.5                      | 4.8 | 6.9 | 1.5 | 7.6 |      |

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

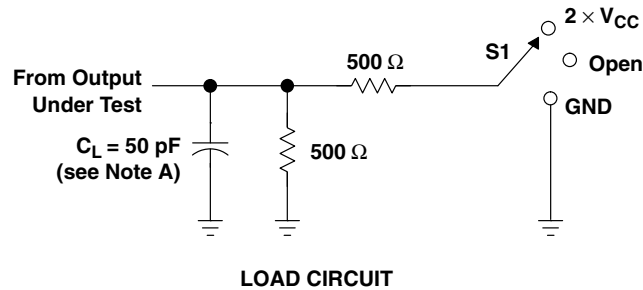
| PARAMETER |                               | TEST CONDITIONS  |                                           | TYP | UNIT |
|-----------|-------------------------------|------------------|-------------------------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | Outputs enabled  | $C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$ | 37  | pF   |
|           |                               | Outputs disabled |                                           | 11  |      |

74AC11257

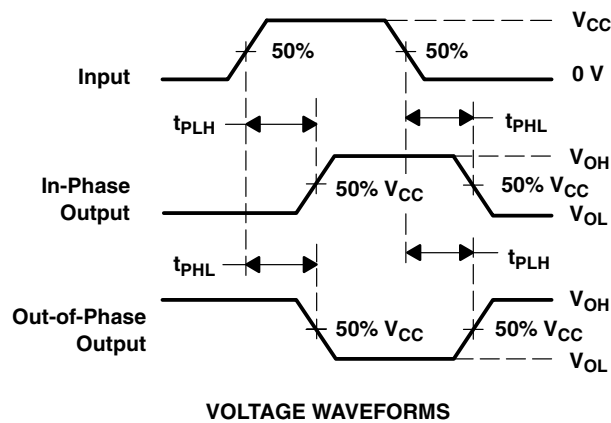
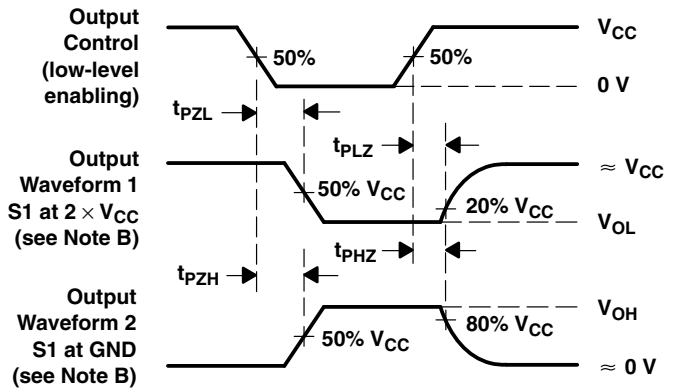
# QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">74AC11257DW</a> | Last Time Buy | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AC11257             |
| 74AC11257DW.A               | Last Time Buy | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AC11257             |
| <a href="#">74AC11257N</a>  | Last Time Buy | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | 74AC11257N          |
| 74AC11257N.A                | Last Time Buy | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | 74AC11257N          |
| <a href="#">74AC11257PW</a> | Active        | Production           | TSSOP (PW)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AE257               |
| 74AC11257PW.A               | Active        | Production           | TSSOP (PW)   20 | 70   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AE257               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

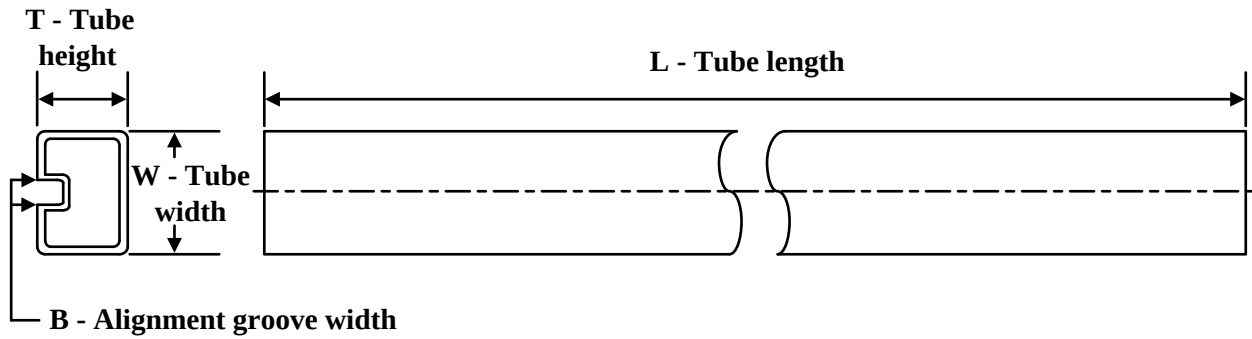
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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## TUBE



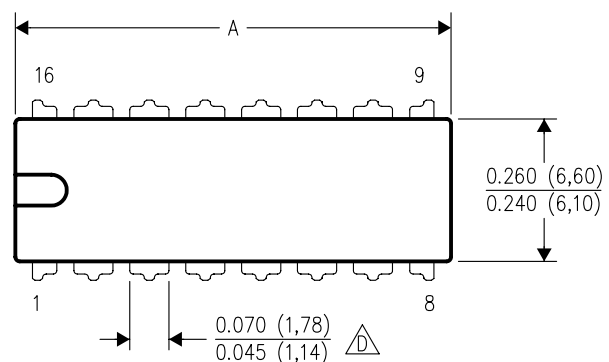
\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 74AC11257DW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| 74AC11257DW.A | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| 74AC11257N    | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| 74AC11257N.A  | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| 74AC11257PW   | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| 74AC11257PW.A | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |

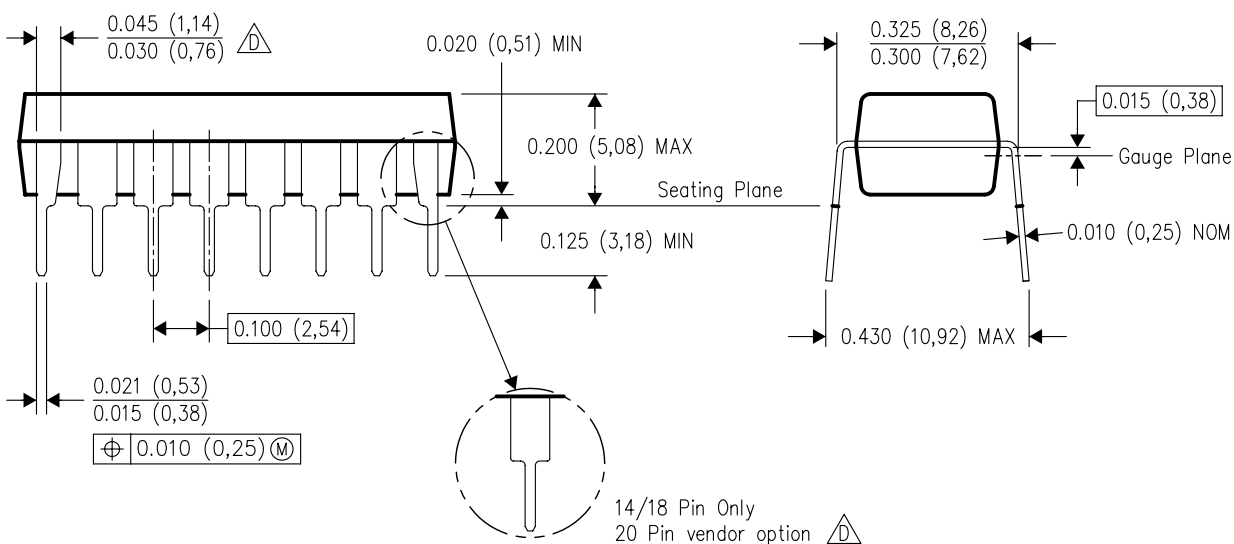
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



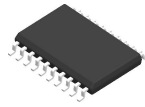
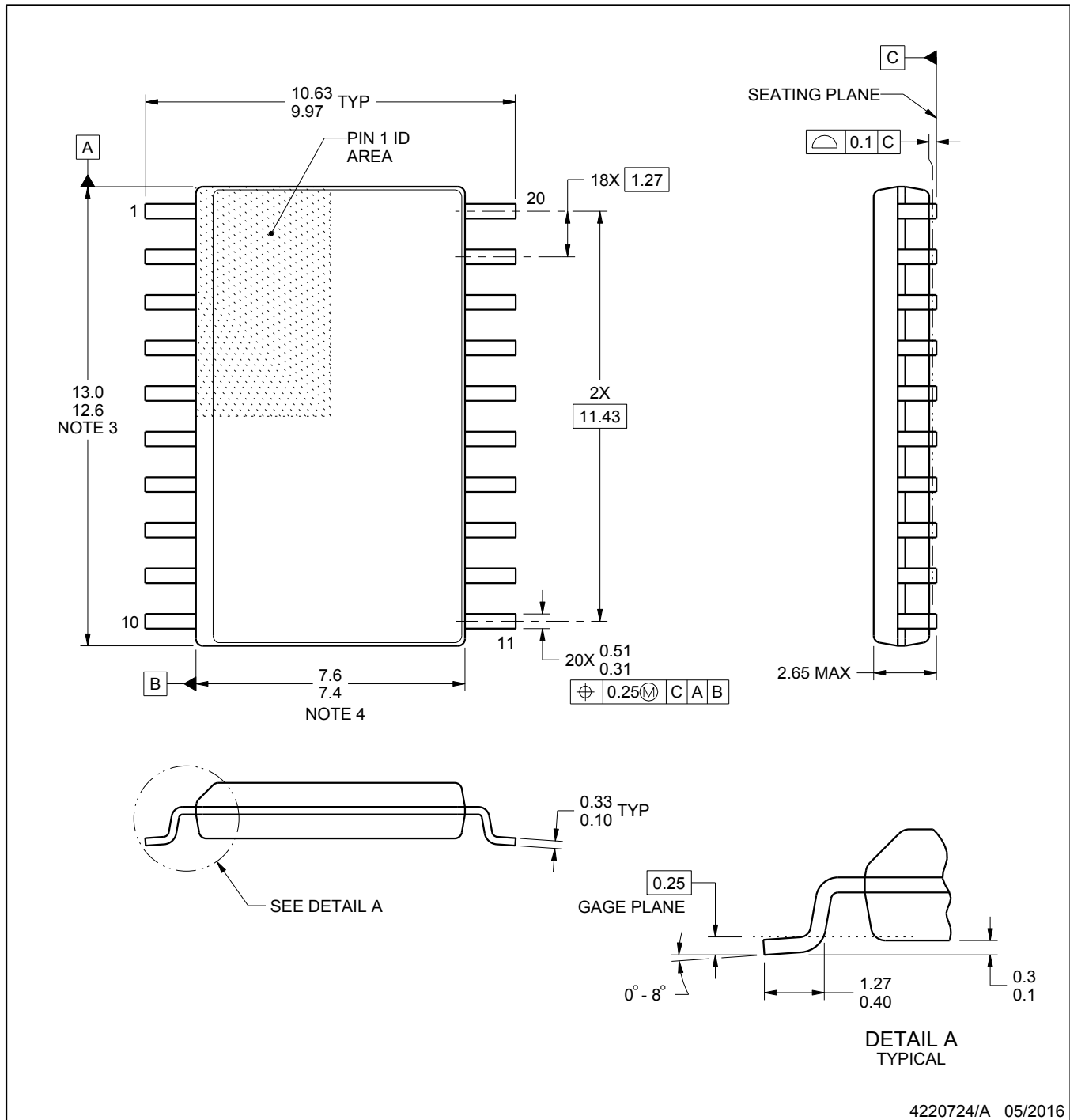
| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



## NOTES:

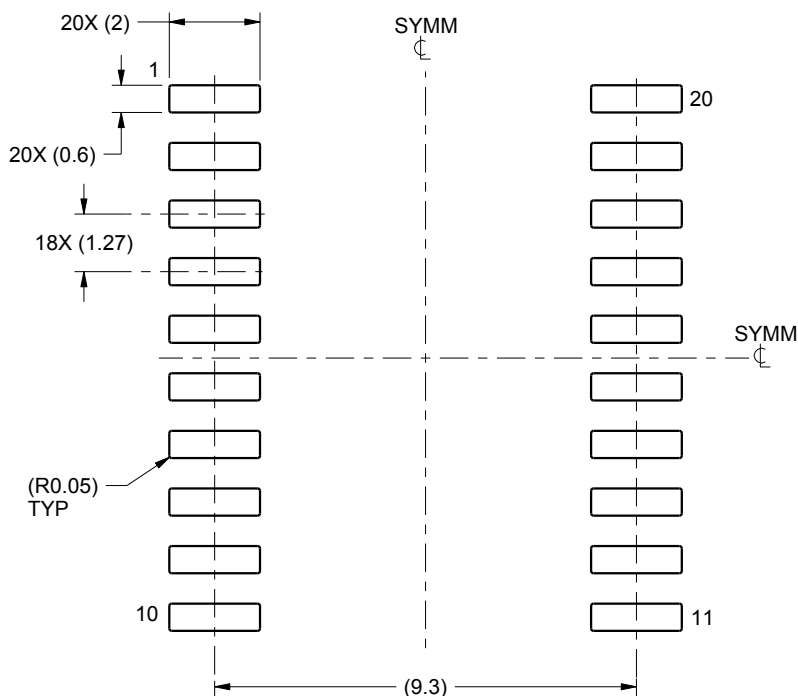
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

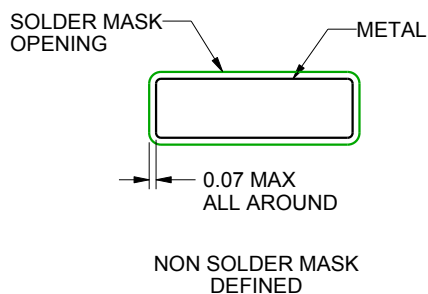
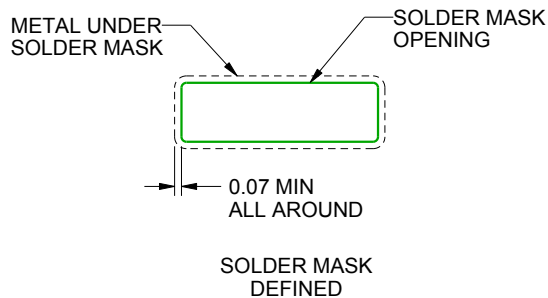
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

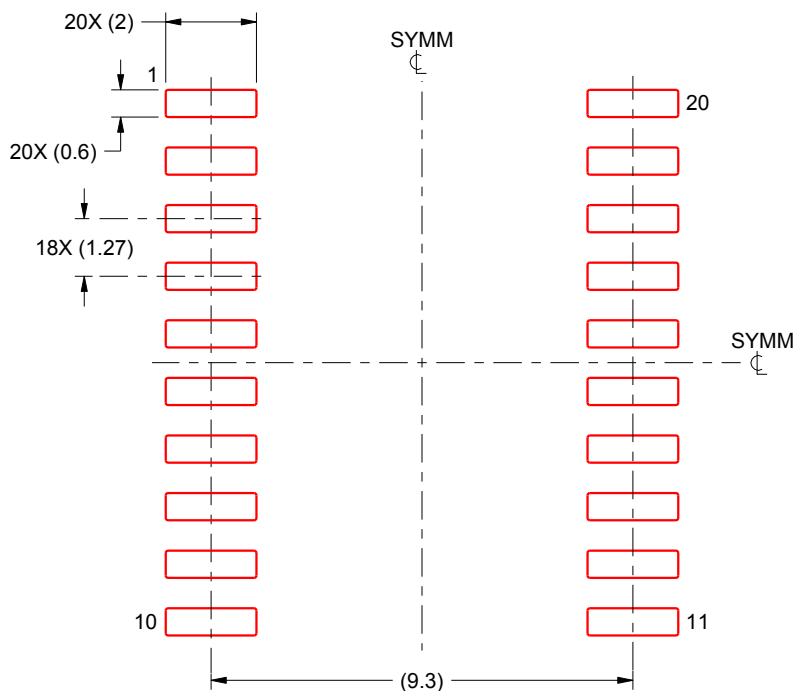
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

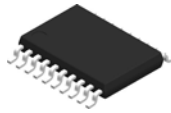
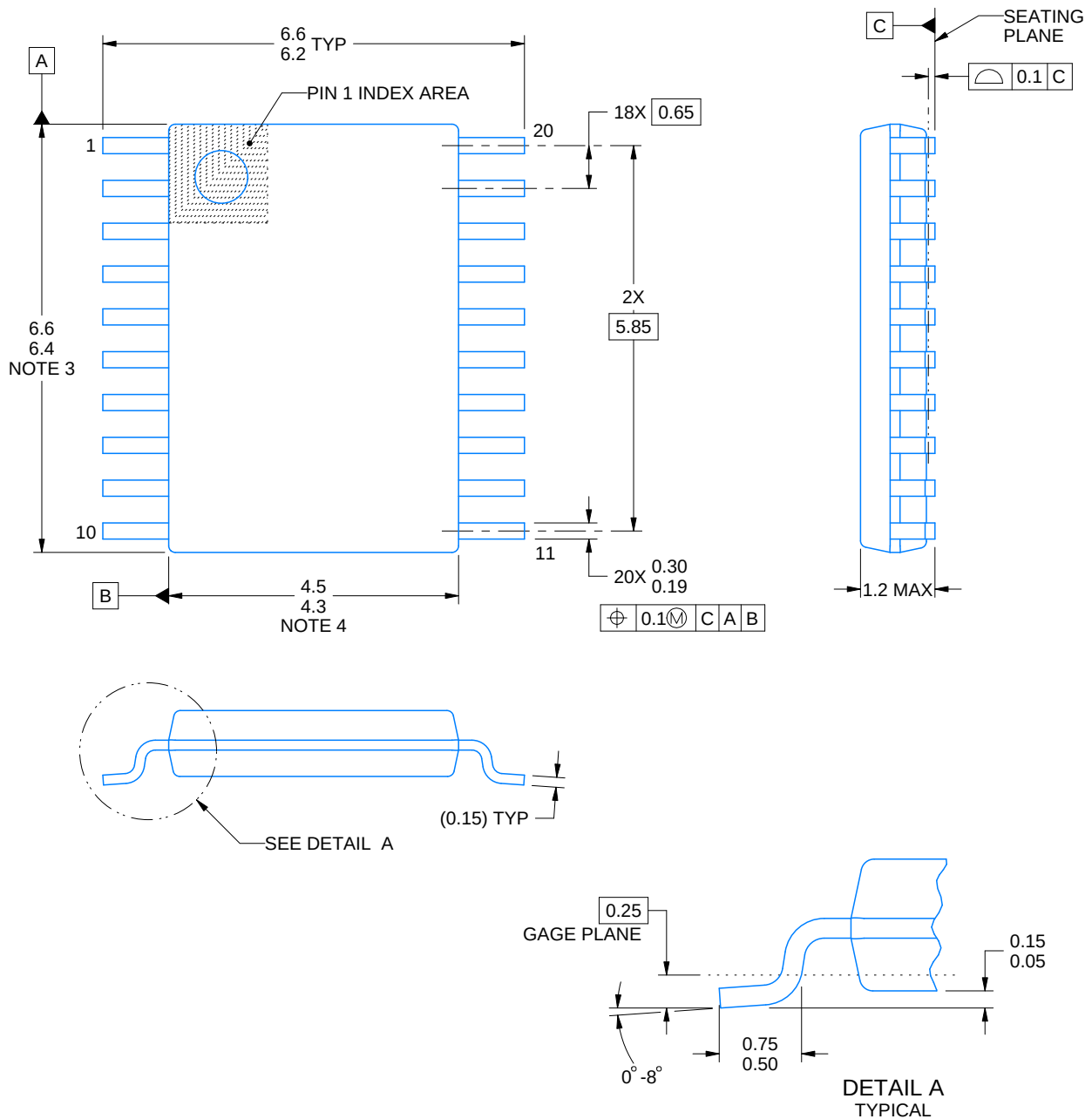


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220206/A 02/2017

## NOTES:

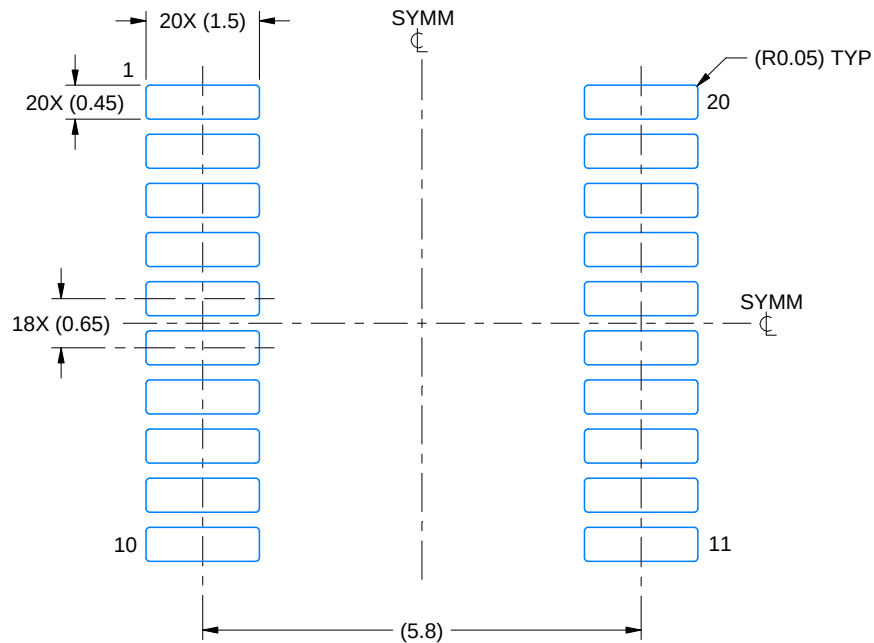
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

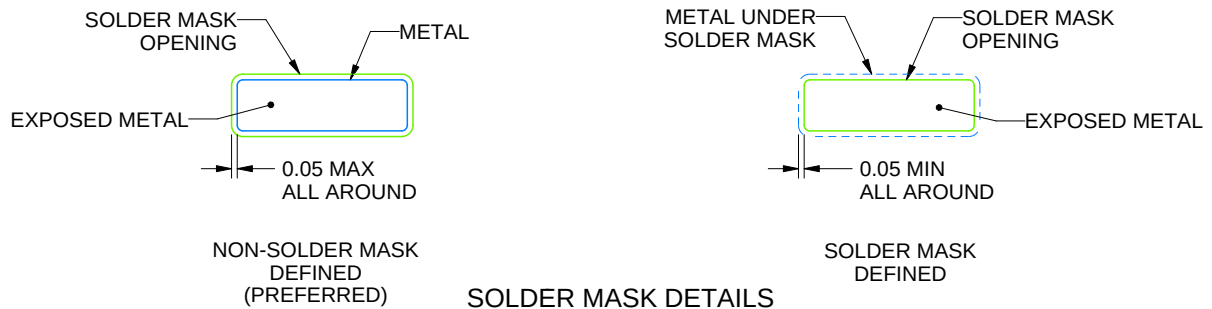
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

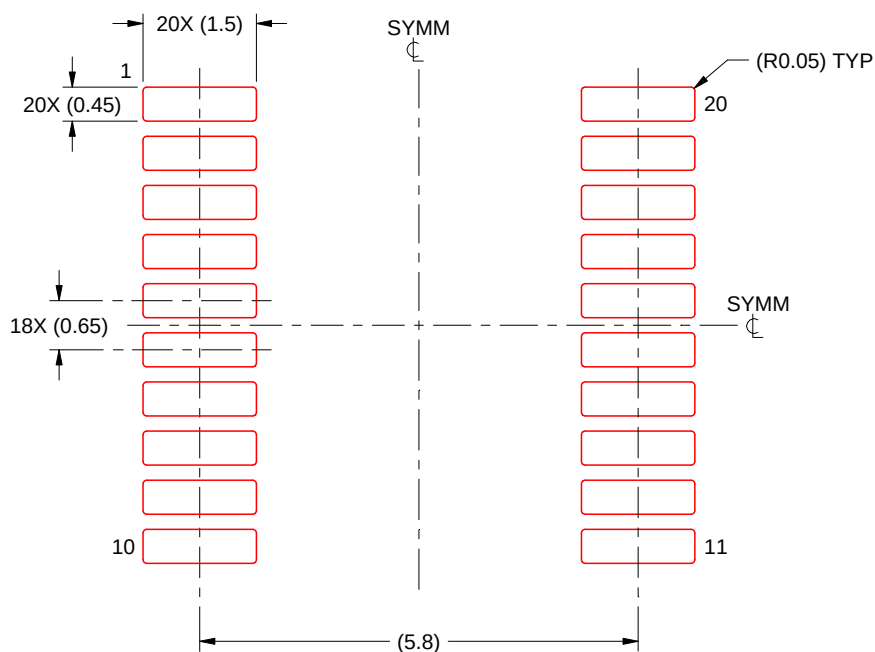
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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