TEXAS INSTRUMENTS
2N7001T-Q1
SCES906A – FEBRUARY 2020 – REVISED JULY 2020

2N7001T-Q1 Single-bit Dual-supply Buffered Voltage Signal Converter

1 Features

- Up and down translation across 1.65 V to 3.6 V
- AEC-Q100 automotive qualified
- Operating temperature grade 1: –40°C to +125°C
- Maximum quiescent current (I_{CCA} + I_{CCB}) of 14 µA (125°C maximum)
- Up to 100 Mbps support across the full supply range
- V_{CC} Isolation Feature
  - If either V_{CC} input is below 100 mV, the output becomes high-impedance
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JEDEC JS-001
  - 2000-V human body model
  - 1000-V charged-device model

2 Applications

- MCU/FPGA/processor GPIO translation
- Communications modules to processor translation
- Push-pull I/O buffering

3 Description

The AEC-Q100 qualified 2N7001T-Q1 device is a single-bit buffered voltage signal converter that uses two separate configurable power-supply rails to up or down translate a unidirectional signal. The device is operational with both V_{CCA} and V_{CCB} supplies down to 1.65 V and up to 3.60 V. V_{CCA} defines the input threshold voltage on the A input. V_{CCB} defines the output drive voltage on the B output.

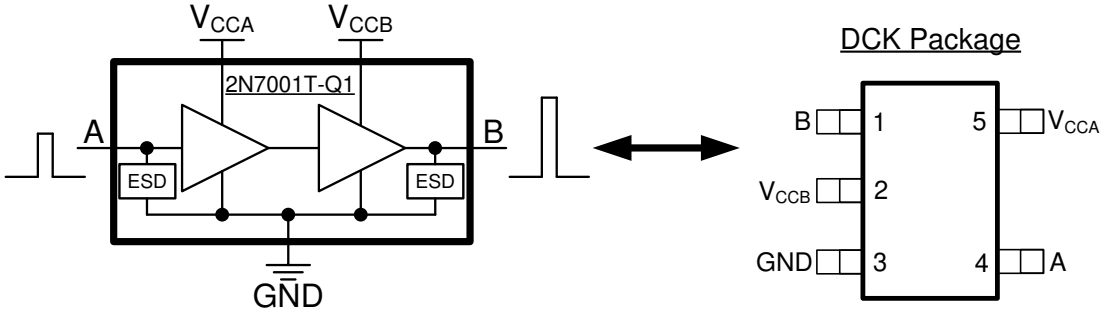
This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry ensures that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specific voltage while the device is powered down.

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} is less than 100 mV, the output port (B) enters a high-impedance state.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
2N7001TDCKRQ1	SC70 (5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Block Diagram and Pin Configuration

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2020) to Revision A (July 2020)	Page
• Changed device status from "Advance Information to "Production Data"	1
• Updated the numbering format for tables, figures and cross-references throughout the document	1

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5 Pin Configuration and Functions

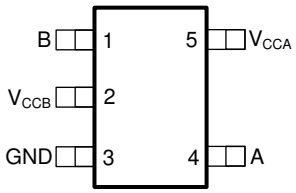


Figure 5-1. DCK Package 5-Pin SC70 Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DCK		
B	1	O	Data Output. This pin is referenced to V_{CCB}.
V_{CCB}	2	—	Output Supply voltage. 1.65V ≤ V_{CCB} ≤ 3.6 V.
GND	3	—	Ground
A	4	I	Data Input. This pin is referenced to V_{CCA}.
V_{CCA}	5	—	Input Supply voltage. 1.65V ≤ V_{CCA} ≤ 3.6 V.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		–0.5	4.2	V
V_{CCB}			–0.5	4.2	V
V_I	Input voltage(2)		–0.5	4.2	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.2	V
V_O	Voltage range applied to any output in the high or low state(2) (3)		–0.5	V_{CCB} + 0.2	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current		–50	50	mA
I_{CC}	Continuous output current through V_{CCA}, V_{CCB}, or GND		–100	100	mA
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2V maximum if the output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		1.65	3.6	V
V_{CCB}	Supply voltage		1.65	3.6	V
V_{IH}	High-level input voltage	V_{CCA} = 1.65 V - 1.95V	V_{CCA} x 0.65		
		V_{CCA} = 2.30 V - 2.70V	1.6		
		V_{CCA} = 3.00 V - 3.60V	2.0		
V_{IL}	Low-level input voltage	V_{CCA} = 1.65 V - 1.95V		V_{CCA} x 0.35	
		V_{CCA} = 2.30 V - 2.70V		0.7	
		V_{CCA} = 3.00 V - 3.60V		0.8	
V_I	Input voltage		0	3.6	V
V_O	Output voltage	Active State	0	V_{CCB}	V
		Tri-State	0	3.6	
Δt/Δv	Input transition rise and fall rate			100	ns/V
T_A	Operating free-air temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		2N7001T-Q1 DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	253.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	162.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	140.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	69.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	139.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		VCCA	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OH}	High Level Output Voltage	$V_I = V_{IH}$	I_{OH} = -100 µA	1.65 V - 3.6 V	1.65 V - 3.6 V	V_{CCB}-0.1			V
			I_{OH} = -8 mA	1.65 V	1.65 V	1.2			
			I_{OH} = -9 mA	2.30 V	2.30 V	1.75			
			I_{OH} = -12 mA	3.00 V	3.00 V	2.3			
V_{OL}	Low Level Output Voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	1.65 V - 3.6 V	1.65 V - 3.6 V			0.1	V
			I_{OL} = 8 mA	1.65 V	1.65 V			0.45	
			I_{OL} = 9 mA	2.30 V	2.30 V			0.55	
			I_{OL} = 12 mA	3.00 V	3.00 V			0.7	
I_{off}	Partial power down current	V_I or V_O = 0 V - 3.6 V		0 V	0 V - 3.6 V	–8		8	µA
		V_I or V_O = 0 V - 3.6 V		0 V - 3.6 V	0 V	–8		8	
I_{CCA}	V_{CCA} Supply Current	$V_I = V_{CCA}$ or GND; I_o = 0 mA		1.65 V - 3.6 V	1.65 V - 3.6 V			8	µA
				0 V	3.60 V	–8			
				3.60 V	0 V			8	
I_{CCB}	V_{CCB} Supply Current	$V_I = V_{CCA}$ or GND; I_o = 0 mA		1.65 V - 3.6 V	1.65 V - 3.6 V			8	µA
				0 V	3.60 V			8	
				3.60 V	0 V	–8			
I_{CCA} + I_{CCB}	Combined Supply Current	$V_I = V_{CCA}$ or GND; I_o = 0 mA		1.65 V - 3.6 V	1.65 V - 3.6 V			14	µA
C_I	Input Capacitance	V_I = 1.65V DC + 1 MHz, -16 dBm sine wave		3.30V	0V		2		pF
C_O	Output Capacitance	V_O = 1.65V DC + 1 MHz, -16 dBm sine wave		0V	3.30V		4		pF

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		VCCA	VCCB	MIN	MAX	UNIT
t_{pd}	Propagation delay	1.65 V - 1.95 V	1.65 V - 1.95 V	0.5	20	ns
			2.30 V - 2.70 V	0.5	17	ns
			3.00 V - 3.60 V	0.5	14	ns
		2.30 V - 2.70 V	1.65 V - 1.95 V	0.5	18	ns
			2.30 V - 2.70 V	0.5	15	ns
			3.00 V - 3.60 V	0.5	12	ns
		3.00 V - 3.60 V	1.65 V - 1.95 V	0.5	16	ns
			2.30 V - 2.70 V	0.5	13	ns
			3.00 V - 3.60 V	0.5	10	ns

6.7 Operating Characteritics: T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pdA}	Power Dissipation Capacitance - Port A	I_O = 0 mA, C_L = 0 pF, f = 1 MHz $t_r = t_f$ = 1 ns	$V_{CCA} = V_{CCB}$ = 1.8 V		1		pF
			$V_{CCA} = V_{CCB}$ = 2.5 V		1.3		
			$V_{CCA} = V_{CCB}$ = 3.3 V		1.8		

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PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pdB}	Power Dissipation Capacitance - Port B	I_O = 0 mA, C_L = 0 pF, f = 1 MHz $t_r = t_f$ = 1 ns	$V_{CCA} = V_{CCB}$ = 1.8 V		12		pF
			$V_{CCA} = V_{CCB}$ = 2.5 V		15		
			$V_{CCA} = V_{CCB}$ = 3.3 V		18		

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6.8 Typical Characteristics

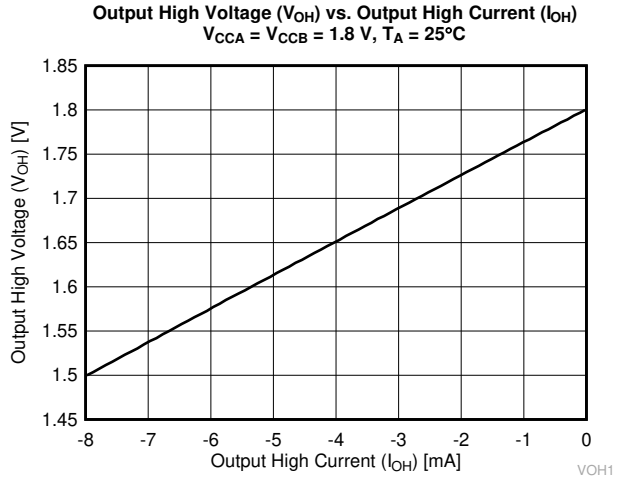


Figure 6-1. V_{OH} vs I_{OH}, 1.8 V

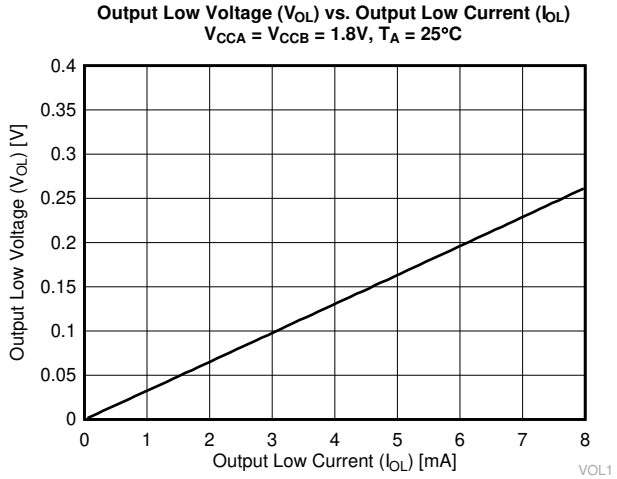


Figure 6-2. V_{OL} vs I_{OL}, 1.8 V

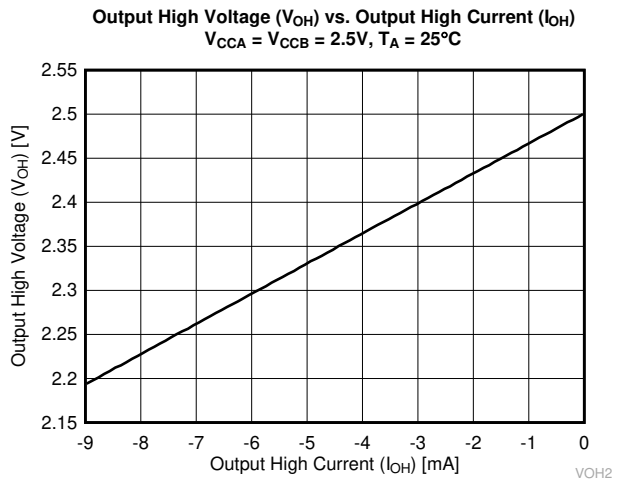


Figure 6-3. V_{OH} vs I_{OH}, 2.5 V

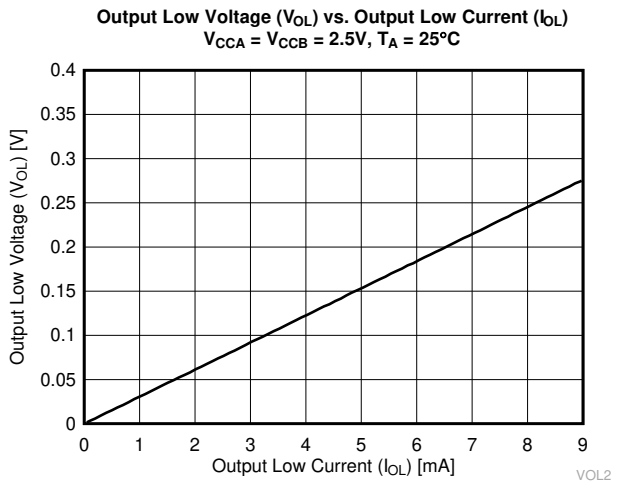


Figure 6-4. V_{OL} vs I_{OL}, 2.5 V

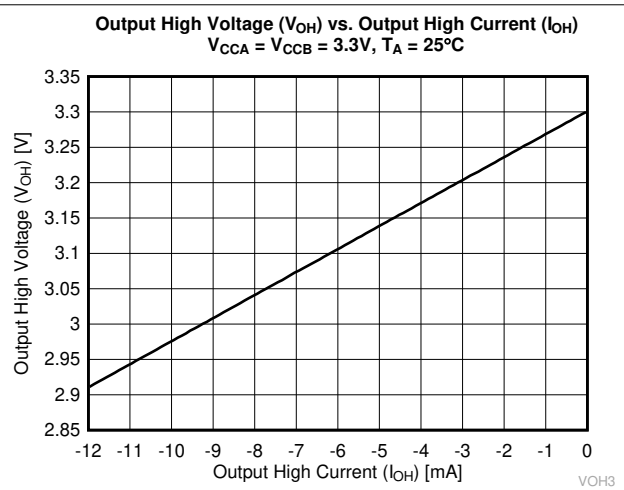


Figure 6-5. V_{OH} vs I_{OH}, 3.3 V

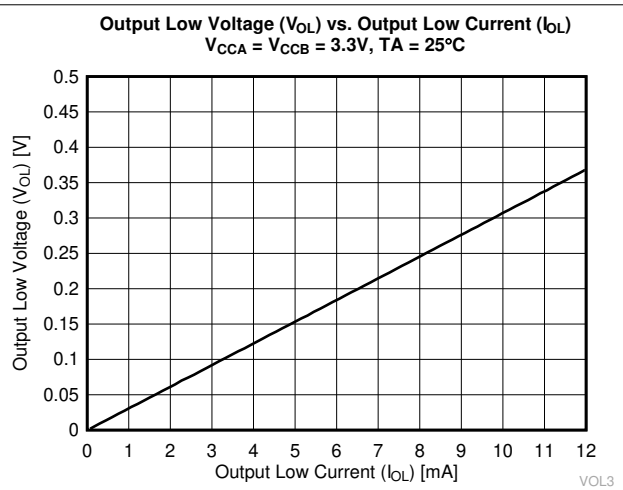


Figure 6-6. V_{OL} vs I_{OL}, 3.3 V

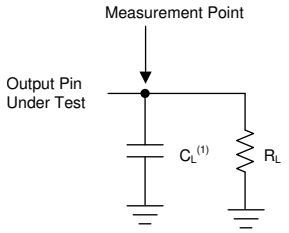
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7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- Z_O = 50 Ω
- dv/dt ≤ 1 ns/V

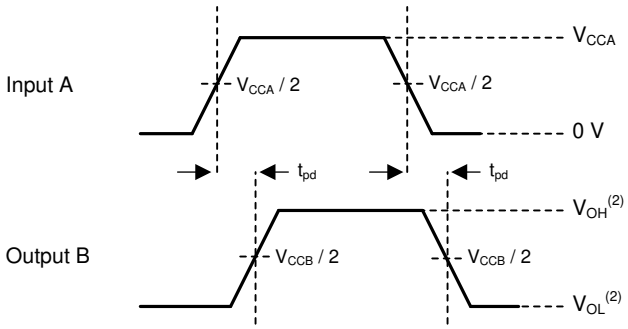


A. C_L includes probe and jig capacitance.

Figure 7-1. Load Circuit

Table 7-1. Load Circuit Conditions

Parameter		V_{CC}	R_L	C_L
t_{pd}	Propagation (delay) time	1.65 V – 3.6 V	2 kΩ	15 pF



A. V_{CCI} is the supply pin associated with the input port.

B. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L and C_L.

Figure 7-2. Propagation Delay

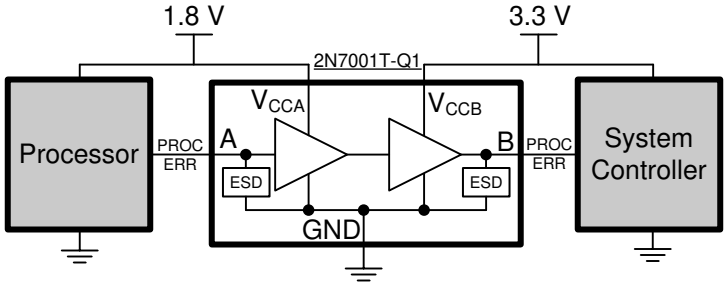
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8 Detailed Description

8.1 Overview

The 2N7001T-Q1 is an automotive AEC-Q100 qualified single-bit dual-supply buffered voltage signal converter that can be used to up or down-translate a single unidirectional signal. The device is operational with both V_{CCA} and V_{CCB} supplies down to 1.65 V and up to 3.60 V. V_{CCA} defines the input threshold voltage on the A input while V_{CCB} defines the output voltage on the B output.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Up-Translation or Down-Translation from 1.65 V to 3.60 V

The V_{CCA} and V_{CCB} pins can both be supplied by a voltage range from 1.65 V to 3.6 V. This voltage range makes the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, and 3.3 V).

8.3.2 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Raings* must be followed at all times.

8.3.3 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance shown in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, shown in the *Absolute Maximum Ratings*, and the maximum input leakage current, shown in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

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8.3.4 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as shown in Figure 8-1.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

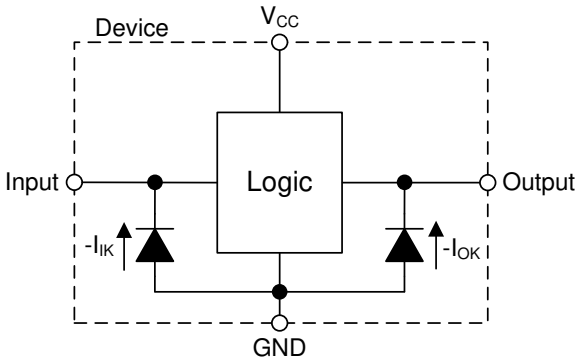


Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.5 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input pin or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

8.3.6 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the input supply voltage (V_{CCA}), as long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

8.4 Device Functional Modes

Table 8-1 lists the functional modes of the 2N7001T-Q1 device.

Table 8-1. Function Table

INPUT	OUTPUT
L (Referenced to V_{CCA})	L (Referenced to V_{CCB})
H (Referenced to V_{CCA})	H (Referenced to V_{CCB})

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The 2N7001T-Q1 device can be used in level-translation applications for interfacing between devices or systems that are operating at different interface voltages.

9.2 Typical Applications

9.2.1 Processor Error Up Translation

Figure 9-1 shows an example of the 2N7001T-Q1 being used in a unidirectional logic level-shifting application.

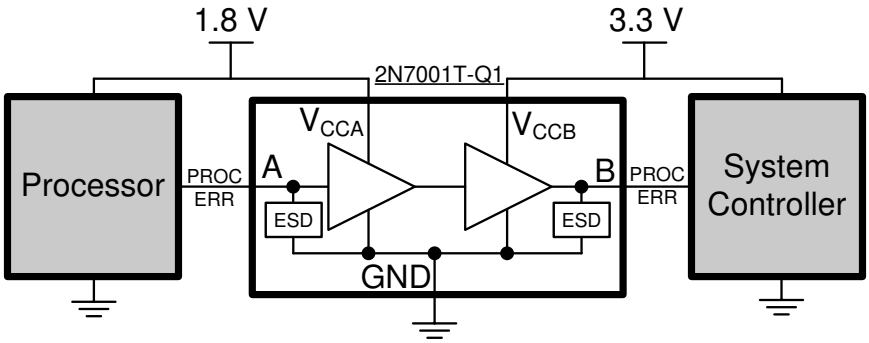


Figure 9-1. Processor Error Up Translation Application

9.2.1.1 Design Requirements

For this design example, use the parameters shown in Table 9-1.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage supply	1.8 V
Output voltage supply	3.3 V

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - The supply voltage of the upstream device (device that is driving input pin A) will determine the appropriate input voltage range. For a valid logic-high, the value must exceed the high-level input voltage (V_{IH}) of the input port. For a valid logic low the value must be less than the low-level input voltage (V_{IL}) of the input port.
- Output voltage range
  - The supply voltage of the downstream device (device that output pin B is driving) will determine the appropriate output voltage range.

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9.2.1.3 Application Curve

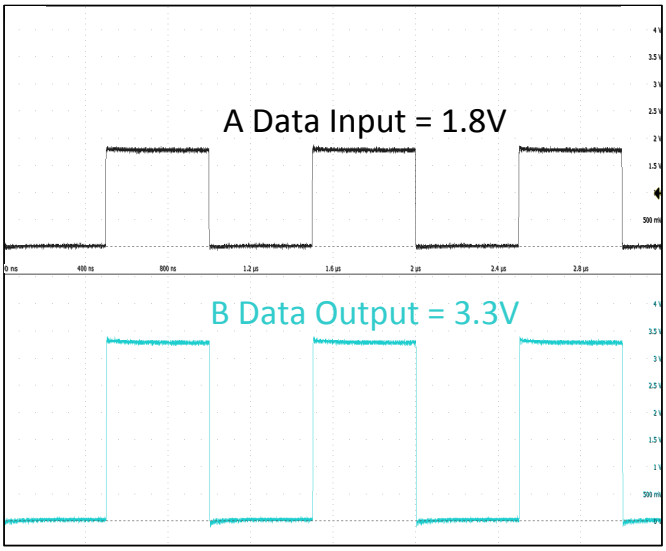


Figure 9-2. Up Translation (1.8 V to 3.3 V) at 1 MHz

9.2.2 Discrete FET Translation Replacement

The 2N7001T-Q1 device is an excellent option for replacing discrete translators, as shown in Figure 9-3, and has the following benefits regarding discrete translation implementations:

- A single device vs a four component solution
- Minimized implementation size
- Lower power consumption
- V_{CC} isolation feature
- Higher data rates
- Integrated ESD protection
- Improved glitch performance

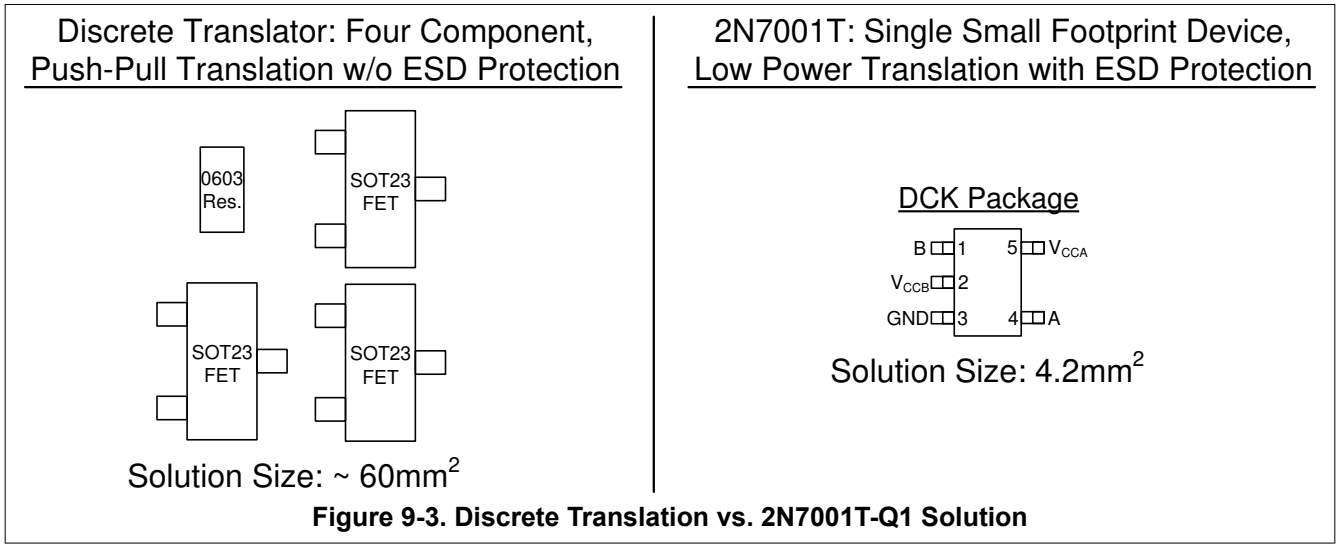


Figure 9-3. Discrete Translation vs. 2N7001T-Q1 Solution

10 Power Supply Recommendations

The 2N7001T-Q1 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. The V_{CCA} and V_{CCB} power-supply rails accept any supply voltage that range from 1.65 V to 3.6 V. The A input and B output are referenced to V_{CCA} and V_{CCB} respectively allowing up or down translation among the 1.8-V, 2.5-V, and 3.3-V voltage nodes. A 0.1 µF bypass capacitor is recommended on all V_{CC} pins.

Always apply a ground reference to the GND pin first. However, there are no additional requirement for power supply sequencing.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1 µF capacitor is recommended, but transient performance can be improved by having both 1 µF and 0.1 µF capacitors in parallel as bypass capacitors.
- Use short trace lengths to avoid excessive loading.

11.2 Layout Example

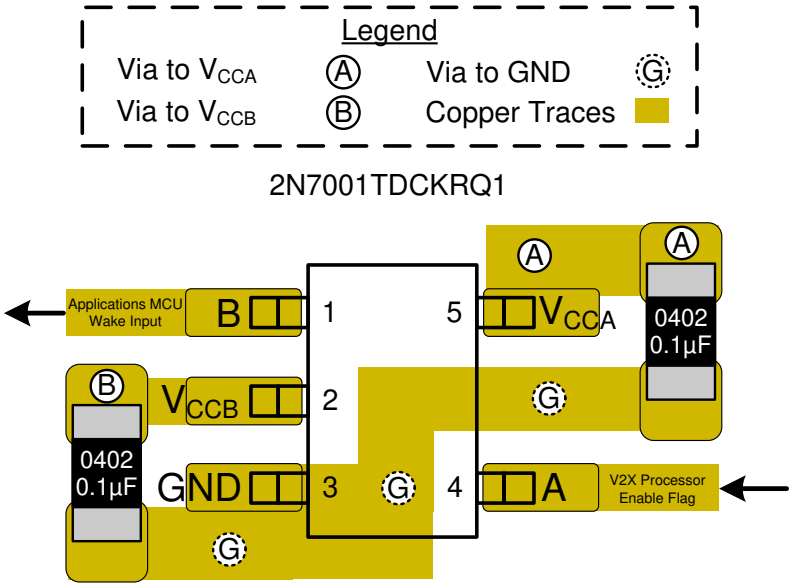


Figure 11-1. DCK Package Example Layout

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, Common Risks with FET Translation and Advantages of 2N7001T application report
- Texas Instruments, Implications of Slow or Floating CMOS Inputs application report
- Texas Instruments, Designing and Manufacturing with TI's X2SON Packages application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
2N7001TQDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	W9
2N7001TQDCKRQ1.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	W9

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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OTHER QUALIFIED VERSIONS OF 2N7001T-Q1 :

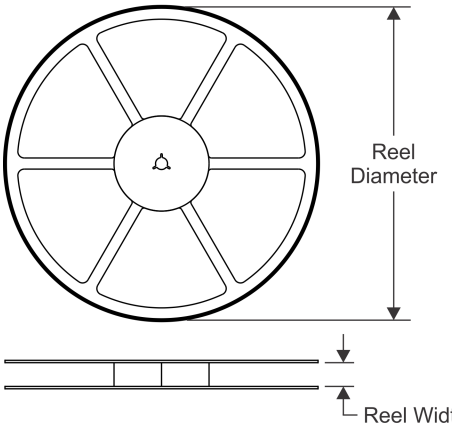
- Catalog : 2N7001T

NOTE: Qualified Version Definitions:

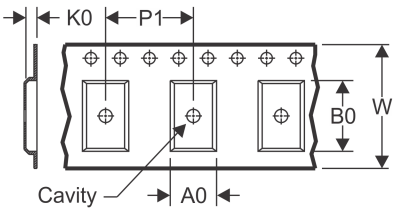
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

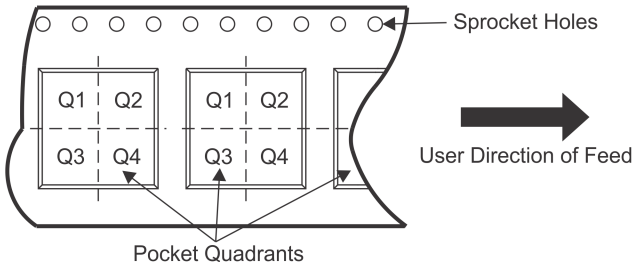


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

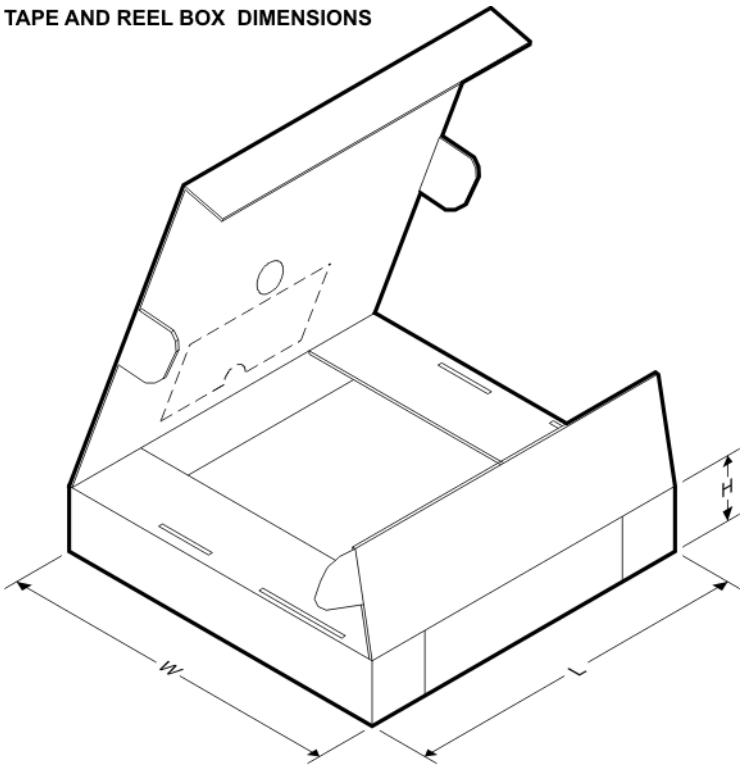
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
2N7001TQDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

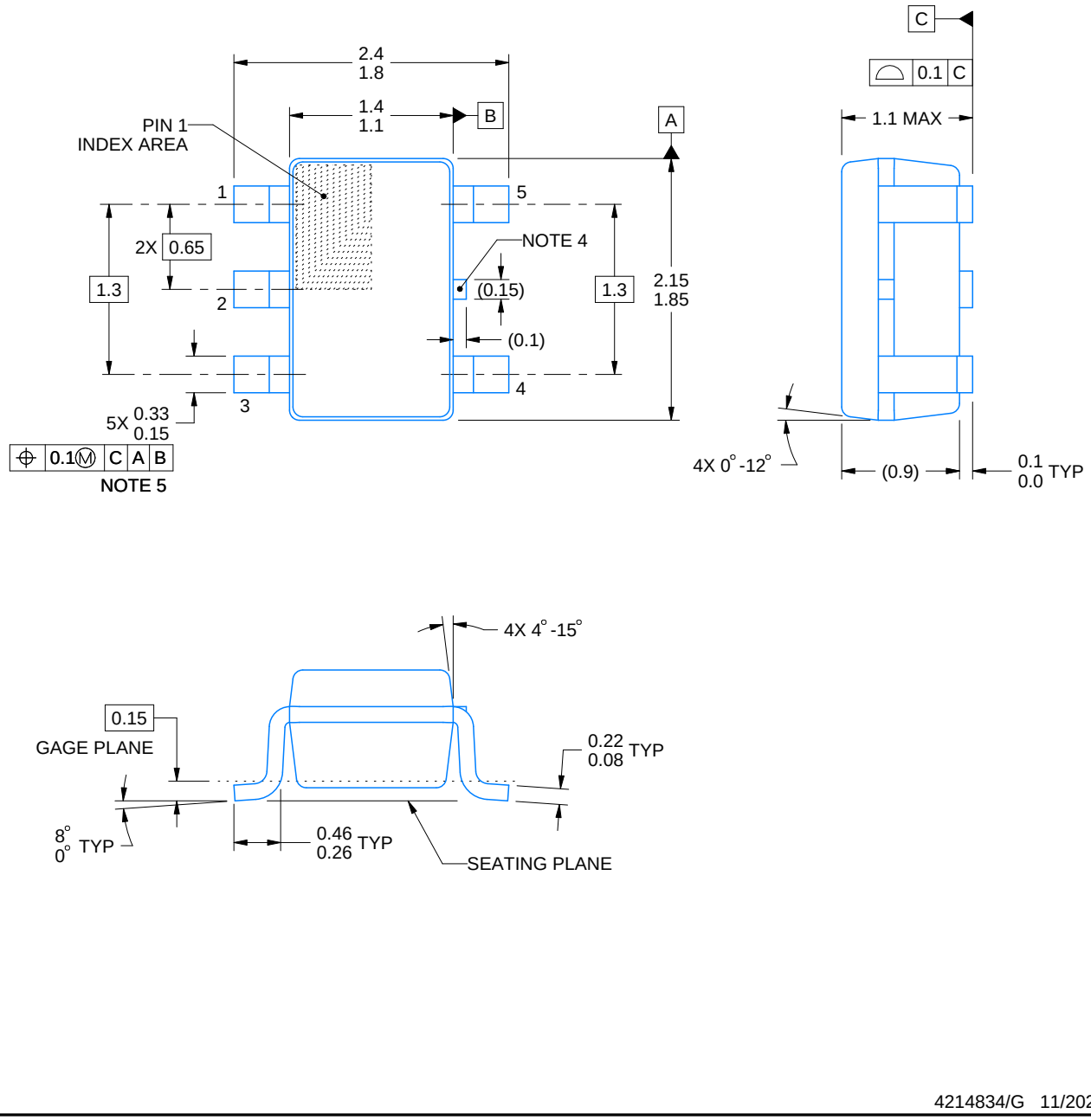
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
2N7001TQDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

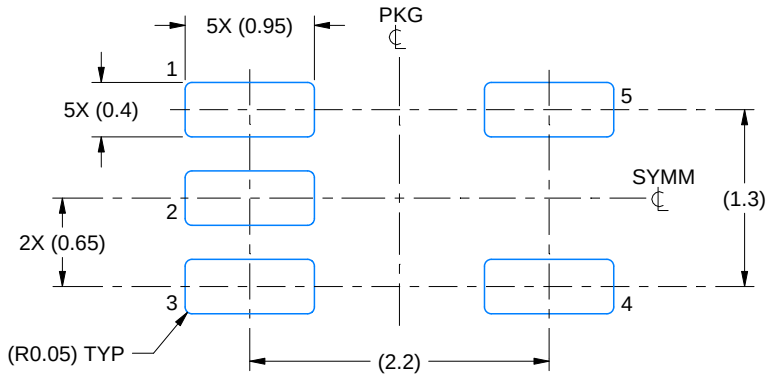
SMALL OUTLINE TRANSISTOR



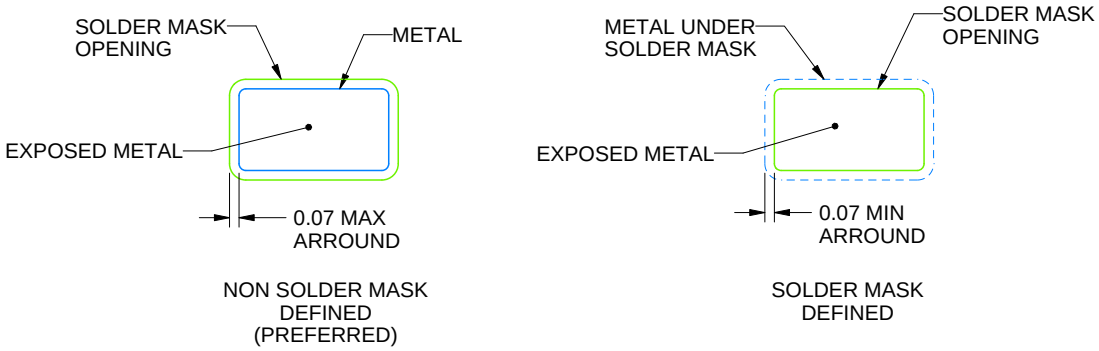
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

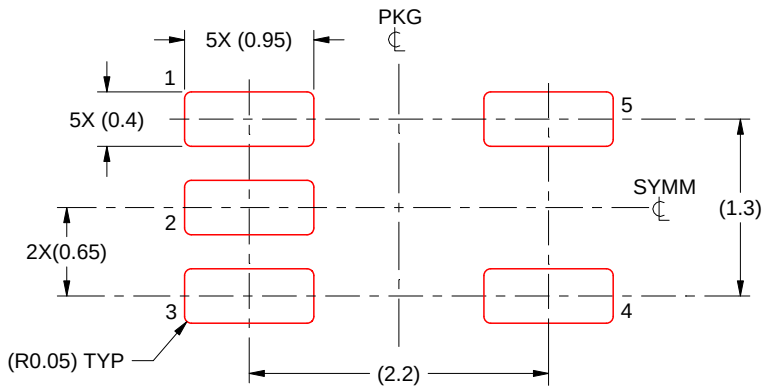


SOLDER MASK DETAILS

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NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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