- **Multifunction Monitoring IC Designed to Work With an Intelligent Host Controller:**
  - **Provides Accurate State of Charge Information for Rechargeable Batteries**
  - **Enhances Power and Charge Management in the System**
- **Supply Operation Down to 2.4 V; Ideal for Single-Cell Li-Ion or Li-Pol Applications**
- **Communicates Over Single-Wire SDQ™ Serial Interface**
- **Resolves Signals Down to 3.05 μVh**
- **High-Accuracy Coulometric Charge and Discharge Current Integration**
- **Differential Current Sense Input**
- **Automatic and Continuous Offset Calibration and Compensation**
- **32 Bytes of General-Purpose RAM, 224 Bytes of FLASH, and 8 Bytes of Secure ID ROM**
- **Internal Temperature Sensor With 0.25°K Resolution Eliminates the Need for an External Thermistor**
- **Programmable Digital Output Port**
- **Battery-Pack Removal Detection Input Places the IC in the Sleep Mode When System Is Not Present**
- **High-Accuracy Internal Timebase Eliminates External Crystal Oscillator**
- **Low Power Consumption:**
  - **Operating: 40 μA**
  - **Sleep: 1.5 μA**

description

PW PACKAGE
(TOP VIEW)

The bq2023 is an advanced battery monitoring IC that accurately measures the charge and discharge currents in rechargeable battery packs. Intended for pack integration, the bq2023 contains all the necessary functions to form the basis for an accurate battery gas gauge in cellular phones, PDAs, or other portable products.

Gas gauging is accomplished by coulomb counting (i.e., measuring the charge input to and subsequently removed from the battery). The bq2023 achieves that by measuring the differential voltage drop across a low-value series sense resistor between the negative terminal of the battery and the battery-pack negative contact. An internal voltage-to-frequency converter (VFC) converts this voltage into charge and discharge counts. The VFC is capable of resolving signals down to 3.05 μV. By using the accumulated counts in the charge, discharge, and self-discharge registers, an intelligent host controller can determine battery state-of-charge information. To improve accuracy, the bq2023 continuously measures and compensates offset errors in the VFC.

The bq2023 works with the host controller in the portable system to implement the battery management system. The host controller interprets the bq2023 data and communicates meaningful battery data to the end-user or power-management system. The SDQ single-wire bus architecture allows multiple bq2023s to exist on the same communications node simultaneously.

The bq2023 provides 224 bytes of flash memory, 8-bytes of secure ID ROM, and 32 bytes of RAM. The nonvolatile memory maintains formatted battery monitor information, identification codes, warranty information, or other critical battery parameters while the battery is temporarily shorted or deeply discharged.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	8-LEAD TSSOP (PW)
–20°C to 70°C	bq2023PW

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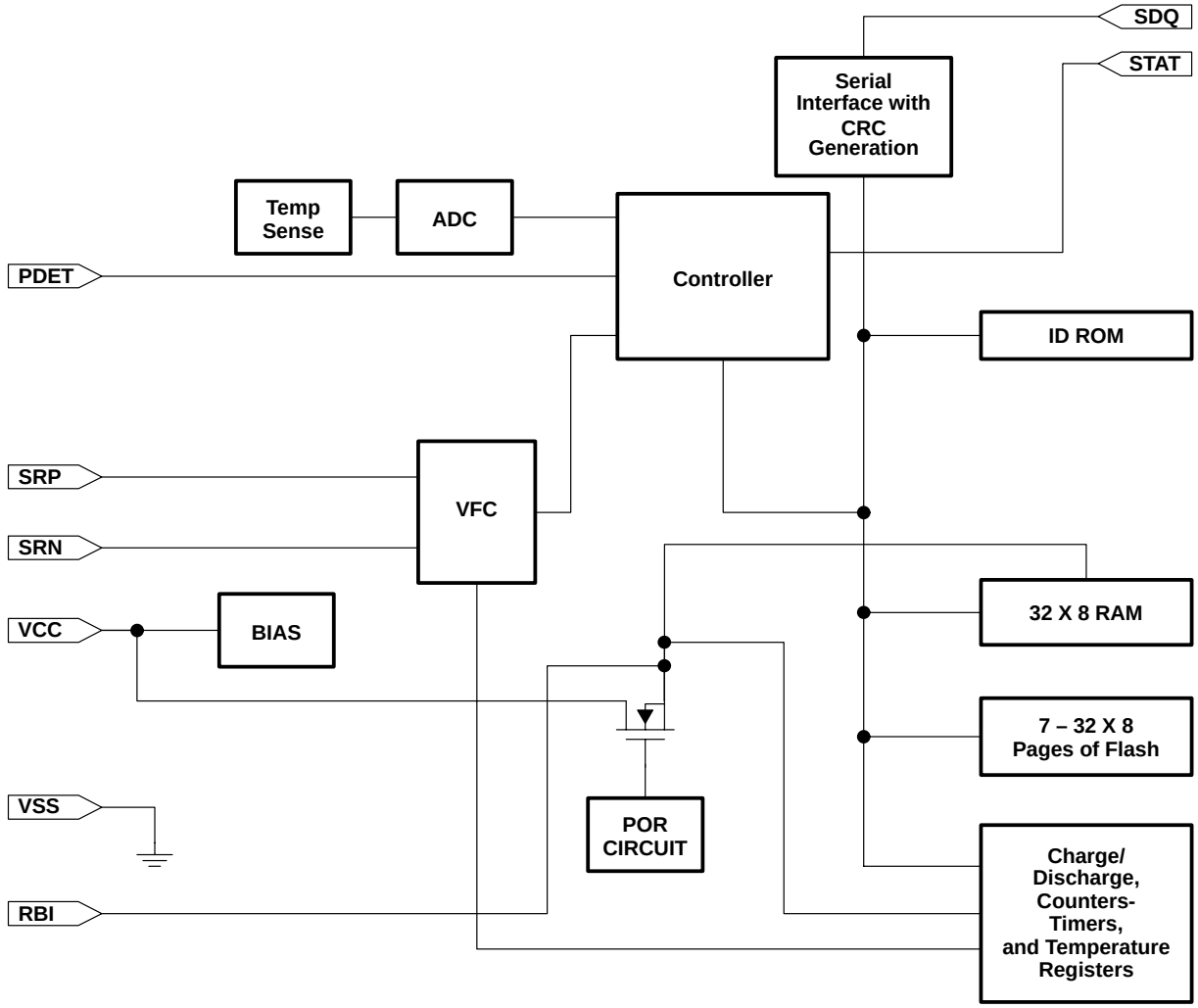
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PDET	5	I	Pack removal detection input
RBI	1	I/O	Register backup input when $V_{CC} < V_{(POR)}$, V_{CC} output when $V_{CC} > V_{(POR)}$
SDQ	4	I/O	Single-wire data input/output port
SRN	6	I	Current sense input 2
SRP	7	I	Current sense input 1
STAT	8	O	Open-drain status output
V_{CC}	2	I	Supply voltage
V_{SS}	3		Ground

detailed description

register backup

The RBI input pin is used with a storage capacitor or external supply to provide backup potential to the internal RAM and registers while V_{CC} is below the minimum operating voltage.

single-wire data input/output port

SDQ is a single-wire serial communications interface port. This bidirectional input/output communicates the information to the host system. SDQ is compatible with Dallas Semiconductor's 1-wire™ interface.

pack removal detection

A low-level PDET input places the bq2023 in sleep mode and turns off the open-drain output of the STAT pin.

current sense inputs

The bq2023 interprets charge and discharge activity by monitoring and integrating the voltage drop, $V_{(SR)}$, across pins SRP and SRN. The SRP input connects to the sense resistor and the negative terminal of the battery. The SRN input connects to the sense resistor and the negative terminal of the pack. $V_{(SRP)} < V_{(SRN)}$ indicates discharge, and $V_{(SRP)} > V_{(SRN)}$ indicates charge.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage (V_{CC} with respect to GND) . . . . . –0.3 V to +7 V
Input voltage, V_I (SRP, SRN, PDET, RBI all with respect to GND) . . . . . –0.3 V to V_{CC} + 0.3 V
Pullup voltage V_{PU}(SDQ and STAT pins) . . . . . –0.3 V to +7 V
Output current, I_O (STAT pin) . . . . . 5 mA
Output current, I_O(SDQ pin) . . . . . 3 mA
Operating free-air temperature range, T_A . . . . . –20°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature (soldering, 10 s) . . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Operation range with flash write or erase capability, V_{CC}	2.8		5.0	V
Operation range without flash write or erase capability, V_{CC}	2.4		5.0	
Pullup voltage on SDQ and STAT pins, $V_{(PU)}$	2.4		6.0	
Supply current, $I_{CC(OP)}$, See Note 1		35	60	µA
Supply current, $I_{CC(OP)}$, See Note 2		32	40	
Sleep current, $I_{(SLEEP)}$, See Note 3		1.0	1.5	µA
Register back-up current, $I_{(RBI)}$, See Note 4			20	nA
Operating ambient temperature, T_A	–20		70	°C
Power-on reset voltage, $V_{(POR)}$	2.0		2.34	V

NOTES: 1. V_{CC} = 5 V, flash write or erase not active
2. V_{CC} = 4.2 V, flash write or erase not active
3. V_{CC} = 4.2 V, flash write or erase not active, excludes SDR register maintenance
4. RBI pin only, $V_{CC} < V_{(POR)}$

1-wire is a trademark of Dallas Semiconductor.

electrical characteristics over recommended operating free-air temperature range and supply voltage (unless otherwise noted)

dc

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Digital output low SDQ and STAT pin	I_{OL} = 1 mA			0.4	V
I_{OL}	Digital output low sink current on SDQ pin				1	mA
V_{IL}	Digital input low SDQ pin				0.7	V
V_{IH}	Digital input high SDQ pin		1.7			V
$V_{IH(PDETH)}$	Digital input high PDET pin		V_{CC}–0.1		V_{CC}+0.3	V
R_{SR}	SR input impedance	0.1 V < (V_{SRP},V_{SRN}) < V_{CC}	10			MΩ

ac

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(POR)}$	Power on reset delay	Delay required to attempt communication after V_{CC} > 2.4 V			500	ms
$t_{d(PDET)}$	PDET delay	Sleep delay time after PDET transitions from high to low (and all sleep conditions have been met)			1	ms
$t_{d(SDQ)}$	SDQ wake-up delay	Wakeup delay after SDQ activity detected (see Note 5)			300	µs

NOTE 5: Assured by design. Not production tested.

timer characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$E_{(TMR)}$	Timer accuracy error		–4%		4%	

characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{(RES)}$	Reported temperature resolution			0.25		°K
$E_{(T)}$	Reported temperature accuracy		–4		4	°K

VFC characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(SR)}$	Input voltage: V_{SRP}–V_{SRN}		–100		100	mV
$G_{(VFC)}$	Charge/discharge gain	T_A = 22°C, V_{CC} = 3.6 V, See Note 6	91.1	94.1	97.1	Hz/V
$G_{(VCC)}$	Supply voltage gain coefficient	T_A = 22°C, See Note 6		–0.54	–1.25	%/V
$G_{(TCO)}$	Temperature gain coefficient	Slope for T_A = –20°C to 70°C, See Note 6	–0.05		0.06	%/°C
		Total deviation for T_A = –20°C to 70°C, See Note 6		–1.5%	–2.2%	
		Slope for T_A = 0°C to 50°C, See Note 6	–0.04		0.05	%/°C
		Total deviation for T_A = 0°C to 50°C, See Note 6		–0.58%	–1.2%	
INL	Integral nonlinearity	See Note 6	–0.1%	0.04%	0.2%	
$V_{(COS)}$	Auto compensated offset	See Note 6	–15.8		11.4	µV
		0°C < T_A < 50°C, 2.4 V < V_{CC} < 4.2 V, See Note 6	–12.1		7.2	µV

NOTE 6: –100 mV < ($V_{(SRP)}$ – $V_{(SRN)}$) < 100 mV

flash memory characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention	See Note 7			5	Years
	Flash programming write-cycles	See Note 7	10,000			Cycles
$t_{(BYTERPROG)}$	Byte programming time	See Note 7			200	µs
$t_{(BLKERASE)}$	Block-erase time	60 µs +30 µs/byte, See Note 7			1,500	µs
$I_{CC(PROG)}$	Flash-write supply current	V_{CC} = 5, See Note 7			30	mA
$I_{CC(ERASE)}$	Flash-erase supply current	V_{CC} = 5, See Note 7			30	mA

NOTE 7: Assured by design. Not production tested.

SDQ communication timing specification over recommended operating temperature and pull-up voltage (unless otherwise noted) (See Figures 2 through 6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(SLOT)}$	Bit cycle time (See Figure 1)	See Note 8	60		120	µs
$t_{(LOW1)}$	Write bit one time (See Figure 1)		1		15	
$t_{(LOW0)}$	Write bit zero time (See Figure 2)	$t_{(LOW0)}$ must be less than $t_{(SLOT)}$, See Note 8	60		120	µs
$t_{(REC)}$	Recovery time (See Figure 2)	See Note 8	1			µs
$t_{(LOWR)}$	Read bit strobe time (See Figure 3)	See Note 8	1		15	µs
$t_{(RDV)}$	Read data valid time (See Figure 3)	See Note 8	t_{LOWR}		15	µs
$t_{(REL)}$	Read data release time (See Figure 4)	See Note 8			30	µs
$t_{(RSTL)}$	Reset time low (See Figure 5)	$t_{(RSTL)} + t_{(R)} < 960$ µs, See Note 8	480			µs
$t_{(RSTH)}$	Reset time high (See Figure 5)	See Note 8	300			µs
$t_{(PDH)}$	Presence pulse delay (See Figure 5)	See Note 8	15		60	µs
$t_{(PDL)}$	Presence pulse delay (See Figure 5)	See Note 8	60		240	µs

NOTE 8: 5-kΩ pullup on SDQ pin

timing requirements

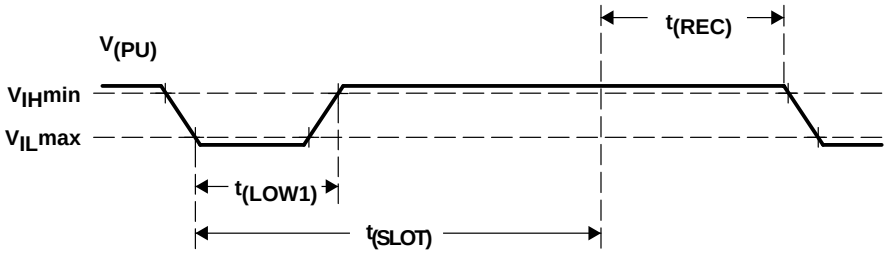


Figure 1. SDQ Write Bit-ONE Timing Diagram

timing requirements (continued)

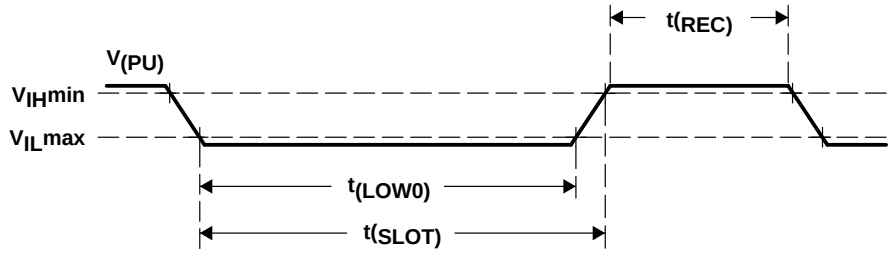


Figure 2. SDQ Write Bit-ZERO Timing Diagram

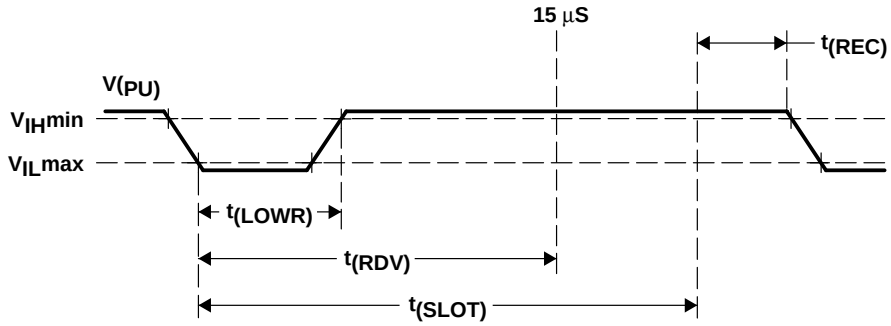


Figure 3. SDQ Read Bit-One Timing Diagram

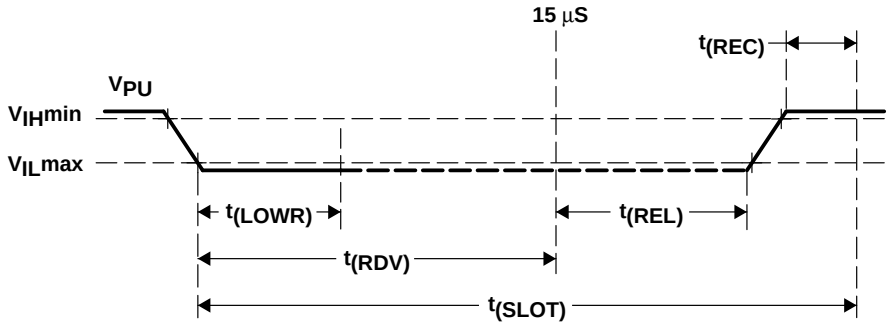


Figure 4. SDQ Read Bit-Zero Timing Diagram

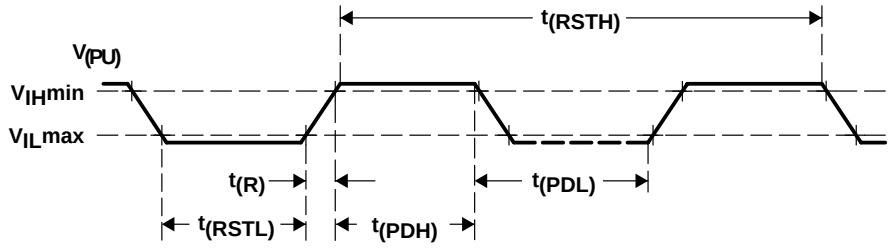


Figure 5. SDQ RESET Timing Diagram

TYPICAL CHARACTERISTICS

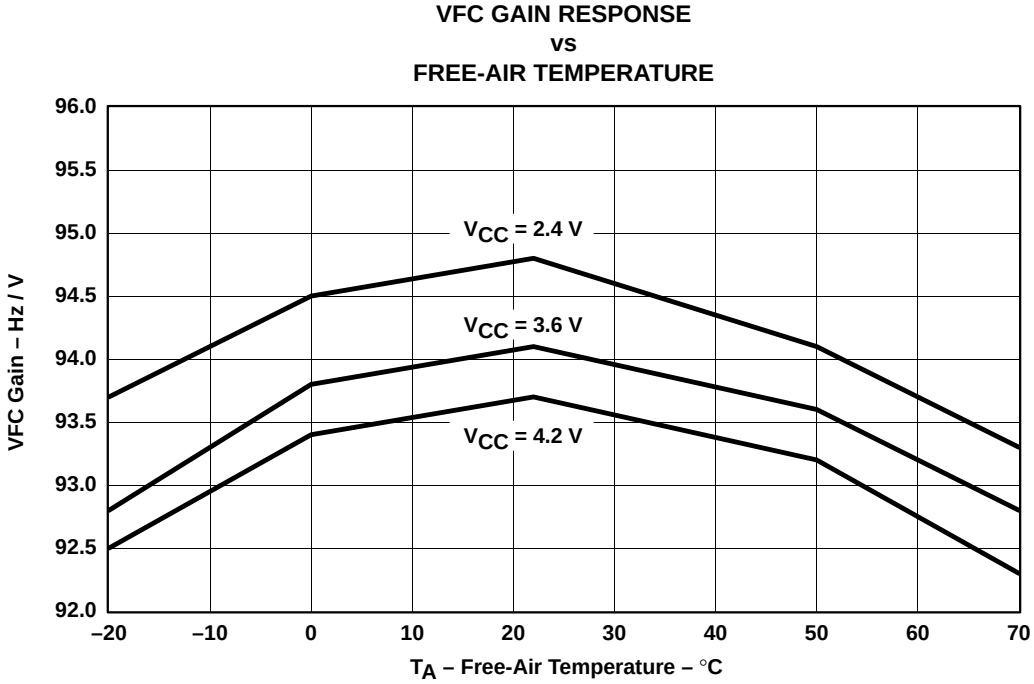


Figure 6

APPLICATION INFORMATION

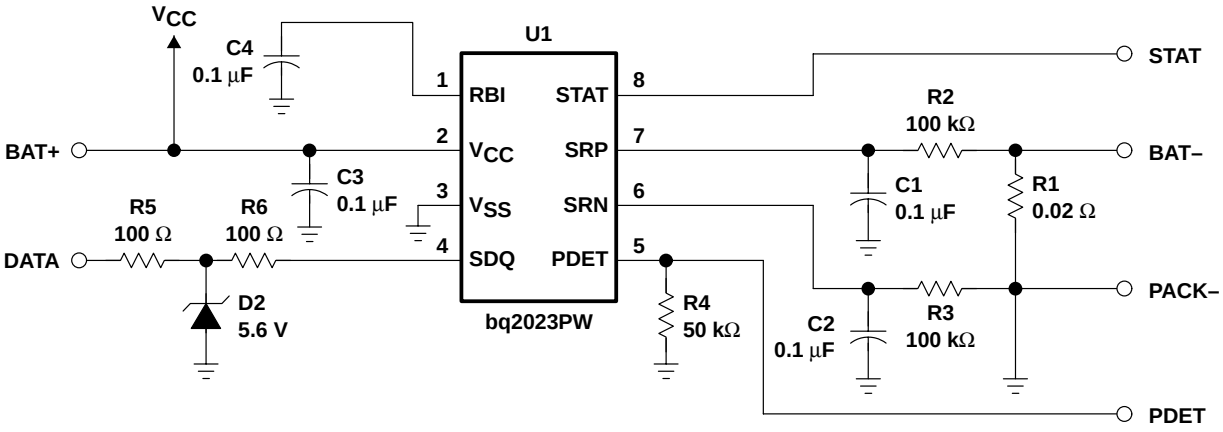


Figure 7. Typical Application Diagram for Single-Cell Li-Ion or Li–Pol Pack

APPLICATION INFORMATION

functional description

The bq2023 measures the differential voltage drop across a low-value series sense resistor between the negative terminal of the battery and the battery-pack ground contact. An internal VFC (voltage-to-frequency converter) converts this voltage into charge and discharge counts. The VFC is capable of resolving signals down to 3.05 μV. By using the accumulated counts in the charge, discharge, and self-discharge registers, an intelligent host controller can determine battery state-of-charge information. To improve accuracy, the bq2023 automatically self-calibrates every hour and continuously compensates offset errors in the VFC every hour.

Access to the registers and control of the bq2023 is accomplished through a single-wire interface command protocol which includes placing the device in the low-power mode, hardware register reset, and flash programming.

charge and discharge count operation

Table 1 shows the main counters and registers of the bq2023. The bq2023 accumulates charge and discharge counts into two count registers, the discharge count register (DCR) and the charge count register (CCR). The DCR or CCR independently counts depending on the signal between pins SRP and SRN.

During discharge, the DCR and the discharge time counter (DTC) are active. If (V_{SRP}–V_{SRN}) is less than zero, indicating a discharge, the DCR counts at a rate equivalent to one count per 3.05 μV-hr, and the DTC counts at 1.1378 counts per second (4096 counts = 1 hour). For example, if it is assumed that no rollover of the DTC register is incipient, a negative 24.42 mV signal between pins SRP and SRN produces 8000 DCR counts and 4096 DTC counts each hour.

During charge, the CCR and the charge time counter (CTC) are active. If (V_{SRP}–V_{SRN}) is greater than zero, indicating a charge, the CCR counts at a rate equivalent to one count per 3.05 μV-hr, and the CTC counts at 1.1378 counts per seconds. In this case a +24.42mV signal produces 8000 CCR counts and 4096 CTC counts (assuming no rollover) each hour.

The DTC and the CTC are 16-bit registers, which roll over at FFFF hex. If a rollover occurs, the corresponding bit in the mode register is set, and the counter increments at 1/256 of the normal rate (16 counts per hour).

For self-discharge calculation, the self-discharge count register (SCR) counts at a rate equivalent to 1 count every hour at a nominal 25°C and doubles approximately every 10°C up to 60°C. The SCR count rate is halved every 10°C below 25°C down to 0°C. The value in SCR is useful in determining an estimation of the battery self-discharge based on capacity and storage temperature conditions.

Table 1. bq2023 Counters

NAME	DESCRIPTION	RANGE	RAM SIZE
DCR	Discharge count register	$V_{(SR)} < V_{SS}$ (Maximum = –100 mV) 3.05 μVh/LSB	16-bit
CCR	Charge count register	$V_{(SR)} > V_{SS}$ (Maximum = 100 mV) 3.05 μVh/LSB	16-bit
SCR	Self-discharge count register	1 count/hour at 25°C	16-bit
DTC	Discharge time counter	1 count/0.8789s if STD is clear 1 count/225s if STD is set	16-bit
CTC	Charge time counter	1 count/0.8789s if STC is clear 1 count/225s if STC is set	16-bit

APPLICATION INFORMATION

functional description (continued)

low-power sleep mode

In order to minimize power consumption, the bq2023 offers a low-power sleep mode. Table 2 shows the active registers during normal and sleep modes.

Table 2. Operational States

MODE	ACTIVE REGISTERS
Normal	CCE, DCR, CTC, DTC, SDR, TEMPH, TEMPL
Sleep	SDR, TEMPH, TEMPL

There are two methods for entering the sleep mode.

sleep mode as a result of charge/discharge inactivity

The bq2023 enters sleep mode if battery current (i.e., voltage difference between the SRP and SRN pins) is less than the WOE threshold, and the SLEN bit (in the MODE/WOE register) is set, and there is no communication activity on the SDQ pin for approximately one hour. The bq2023 wakes on either a low to high or high to low transition on the SDQ pin. The SLEN bit is set during power-on-reset. Table 2 shows the available WOE thresholds.

Table 3. WOE Thresholds

WOE3–1 (HEX)	VWOE (μV)
0h	N/A
1h	21.35
2h	18.30
3h	15.25
4h	12.20
5h	9.15
6h	6.10
7h†	3.05

† Default

sleep mode as a result of change PDET input

PDET input can also place the bq2023 in sleep mode. The bq2023 enters sleep mode in response to PDET input going low. This happens regardless of the state of the SLEN bit (in the MODE/WOE register). In order to wake up the bq2023, several conditions need to be considered:

- A low-to-high transition on PDET will wake the device, if
  - SLEN = 0, or
  - SLEN = 1 and the device was awake when PDET was pulled low.
  - To ensure proper wake-up sequence it is recommended that the host initiate either a low to high or high to low transition on the SDQ pin.
- A low-to-high transition will not wake the device if
  - SLEN = 1 and the device was asleep when PDET was pulled low.

Note that PDET signal should be tied to the V_{CC} during a POR condition.

APPLICATION INFORMATION

functional description (continued)

current sense offset

The bq2023 automatically self-calibrates and compensates for current offset. The self-calibration is performed once every hour.

gas gauge control registers

The host maintains the charge/discharge and self-discharge count registers (CCR, CTC, DCR, DTC, and SCR). To facilitate this, the bq2023 provides the CLR register to clear an individual counter or register pair. The host system clears a register by writing the corresponding register bit to 1. When the bq2023 completes the clear action, the corresponding bit in the CLR register is automatically reset to 0. Clearing the DTC or CTC registers also clears the corresponding STC or STD bit in the MODE register.

device temperature measurement

The bq2023 reports die temperature in units of °K through register pair TEMPH-TEMPL. See the TMP register description for more details.

register interface

Information exchange between the host system and the bq2023 is through the data register interface. See Table 4. The register set consists of a 271-location address space of 8-bit bytes segmented into:

Table 4. bq2023 Memory Map

ADDRESS	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x010F	DCRH	Discharge-count register high byte							
0x010E	DCRL	Discharge-count register low byte							
0x010D	CCRH	Charge-count register high byte							
0x010C	CCRL	Charge-count register low byte							
0x010B	SCRH	Self-discharge count register high byte							
0x010A	SCRL	Self-discharge count register low byte							
0x0109	DTCH	Discharge-timer–counter register high byte							
0x0108	DTCL	Discharge-timer-counter register low byte							
0x0107	CTCH	Charge-timer-counter register high byte							
0x0106	CTCL	Charge-timer-counter register low byte							
0x0105	MODE/WOE	RSVD	SLEN	STC	STD	WOE2	WOE1	WOE0	RSVD
0x0104	CLR	RSVD	POR	STAT	CTC	DTC	SCR	CCR	DCR
0x0103	TEMPH	Temperature high byte							
0x0102	TEMPL	Temperature low byte							
0x0101	FED	RSVD	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0
0x0100		Reserved							
0x00E0-0x00FF	RAM	Page 7, 32 bytes of RAM							
0x00C0-0x00DF	Flash	Page 6, 32 bytes of flash							
0x00A0-0x00BF	Flash	Page 5, 32 bytes of flash							
0x0080-0x009F	Flash	Page 4, 32 bytes of flash							
0x0060-0x007F	Flash	Page 3, 32 bytes of flash							
0x0040-0x005F	Flash	Page 2, 32 bytes of flash							
0x0020-0x003F	Flash	Page 1, 32 bytes of flash							
0x0000-0x001F	Flash	Page 0, 32 bytes of flash							

APPLICATION INFORMATION

functional description (continued)

memory

ID ROM

The bq2023 has 64 bits of ID ROM as shown in Table 5. Forty-eight bits of this data field and the family code can be factory programmed with a unique and secure product serialization. Contact Texas Instruments for details.

Table 5. 64-Bit ID ROM

8-BIT CRC CODE		48-BIT SERIAL NUMBER		8-BIT FAMILY CODE	
MSB	LSB	MSB	LSB	MSB	LSB

flash

Table 6 shows the memory map of the 224 x 8-bit flash section of the bq2023. The flash memory is configured into seven 32-byte pages. To modify the flash, data are first written to the communication buffer with the write data-memory command and then verified by reading an 8-bit CRC (cyclic redundancy check) from the bq2023 that confirms proper receipt of the data. These are then programmed into flash by issuing the programming verification code. For further details on reading and programming the flash, refer to the memory function commands section of this data sheet.

Table 6. 224 Bytes Flash Data Memory Map

ADDRESS (HEX)	PAGE
00C0–00DF	Page 6
00A0–00BF	Page 5
0080–009F	Page 4
0060–007F	Page 3
0040–005F	Page 2
0020–003F	Page 1
0000–001F	Page 0

pack removal detection

The PDET input pin can detect removal of the battery pack from the device it is powering. Also, it can ensure that external devices driven by the STAT output are not active after a battery pack is removed. When the PDET input is low, the bq2023 immediately enters sleep mode and turns off the open-drain output of the STAT pin.

SDQ serial communication

The host reads memory or registers, and programs the bq2023 through a hierarchical command structure. Figure 8 illustrates this command structure and shows that ROM function commands select the bq2023 before the registers or memory can be read or modified. A successful completion of the command selects or activates the bq2023, allowing it to respond to further commands. All bytes sent and received by the bq2023 are transmitted least significant bit first.

To validate the data transmitted from the bq2023, the host may generate a CRC value from the data as they are received. This generated value is compared to the CRC value transmitted by the bq2023. If the two CRC values match, the transmission is error-free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. For more details, see the CRC generation section of this data sheet.

APPLICATION INFORMATION

initialization and selected states

initialization

After the SDQ pin has been driven low for at least 480 μs and then is driven high, the bq2023 will issue a presence pulse. After the presence pulse is sent, the bq2023 is initialized.

selected

After successful completion of a ROM function command, the bq2023 is in the selected state.

ROM function commands

Figure 8 illustrates the four ROM function commands. On the successful completion of a ROM function command, the bq2023 will respond to a memory/status function command.

read ROM

When the bq2023 is initialized, the read ROM command, 33 hex, directs the bq2023 to transmit the contents of the 64 bit ID ROM in order, starting with the least significant bit 0. After the bq2023 transmits the 64th bit, the bq2023 is in the selected state.

match ROM

When the bq2023 is initialized, the match ROM command, 55 hex, directs the bq2023 to compare the next 64 bits received to its own ID ROM contents. If each of the received bits matches, then the bq2023 is selected.

search ROM

When the bq2023 is initialized, the search ROM command, F0 hex, directs the bq2023 to transmit each bit of the ID ROM twice but in a different form each time, and then to receive a bit. First the true value of the bit is transmitted; then the complement of the bit is transmitted. Then, the bq2023 receives a bit. This received bit is compared to the true bit. This process is repeated and the bq2023 compares all bits received to the contents of the ID ROM. If the received bits match the contents of the ID ROM the bq2023 is selected.

skip ROM

When the bq2023 is initialized, the SKIP ROM command, CC hex, directs the bq2023 to be selected.

memory function commands

Six memory function commands allow reading of all registers, flash, and RAM, and allow modification of flash and RAM locations. There are two types of read-memory command, the write data memory, the program profile byte command, and the flash erase command. The bq2023 responds to the memory function commands only after it is selected by a ROM function command.

read memory-page CRC

The read memory/page CRC command reads part or all of the 271 memory addresses shown in the register map with 8-bit CRCs generated at 32-byte page boundaries.

The flowchart in Figure 9 illustrates that when the bq2023 is in the selected state, the read memory/page CRC command, C3 hex, directs the bq2023 to load the next two bytes (low byte and high byte of the starting address) into the address counter. Individual bytes of address and data are transmitted least significant bit first. An 8-bit CRC of the command byte and address bytes is computed and transmitted by the bq2023. When the bq2023 detects a start frame for read time slots it transmits data from the 271 bytes of data memory field as pointed to by the address counter. After each byte of data is transmitted, the address counter is incremented. If the end of a page is reached, the bq2023 calculates and transmits an 8-bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte to the last byte of the current page. Once the 8-bit CRC has been transmitted, data are transmitted from memory as pointed to by the address counter, which at this point is the start of the next page. This sequence will continue until the final page and its accompanying CRC are transmitted. The read memory/page CRC command sequence can be terminated at any point by issuing a reset pulse.

APPLICATION INFORMATION

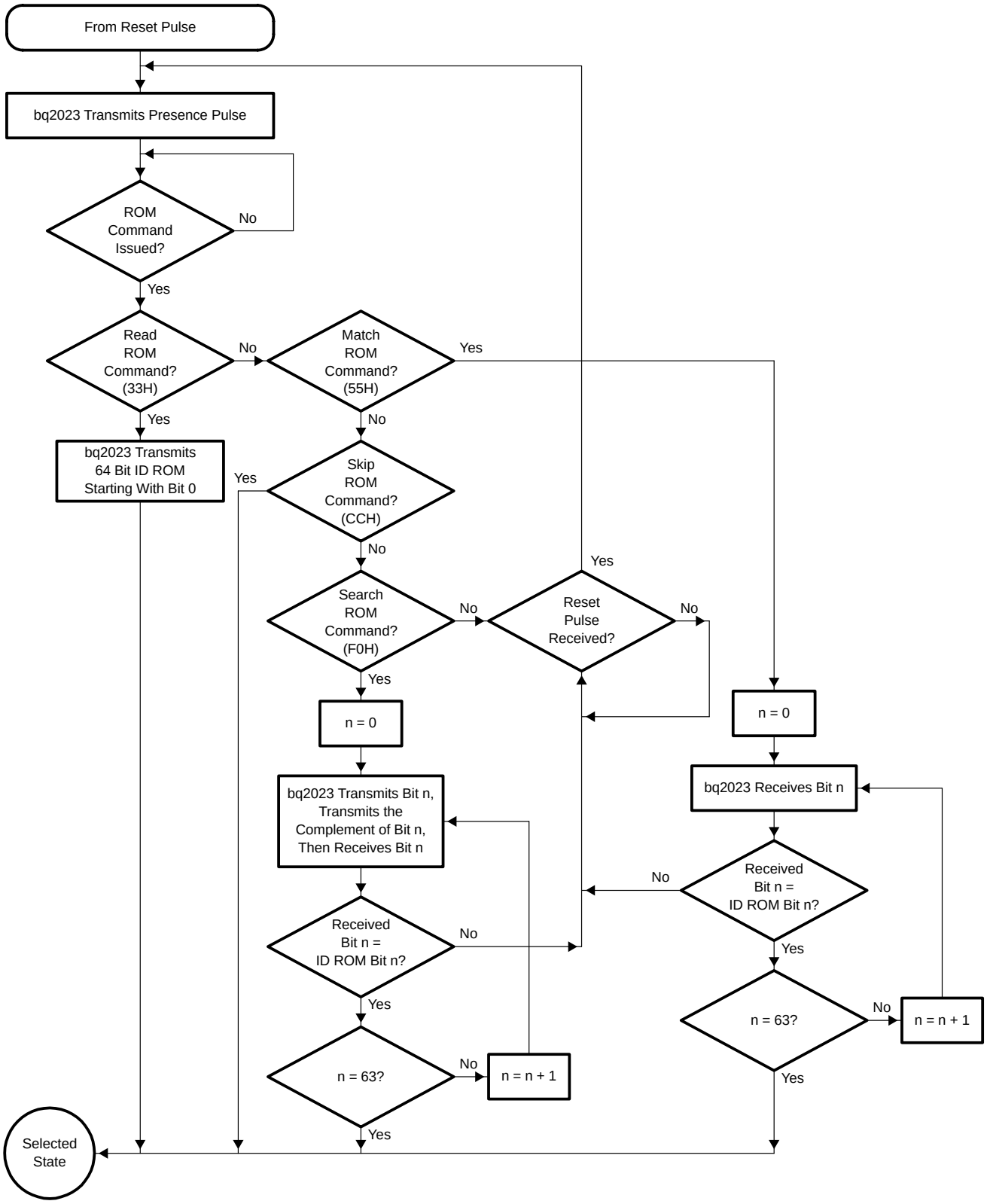


Figure 8. ROM Command Flow Chart

APPLICATION INFORMATION

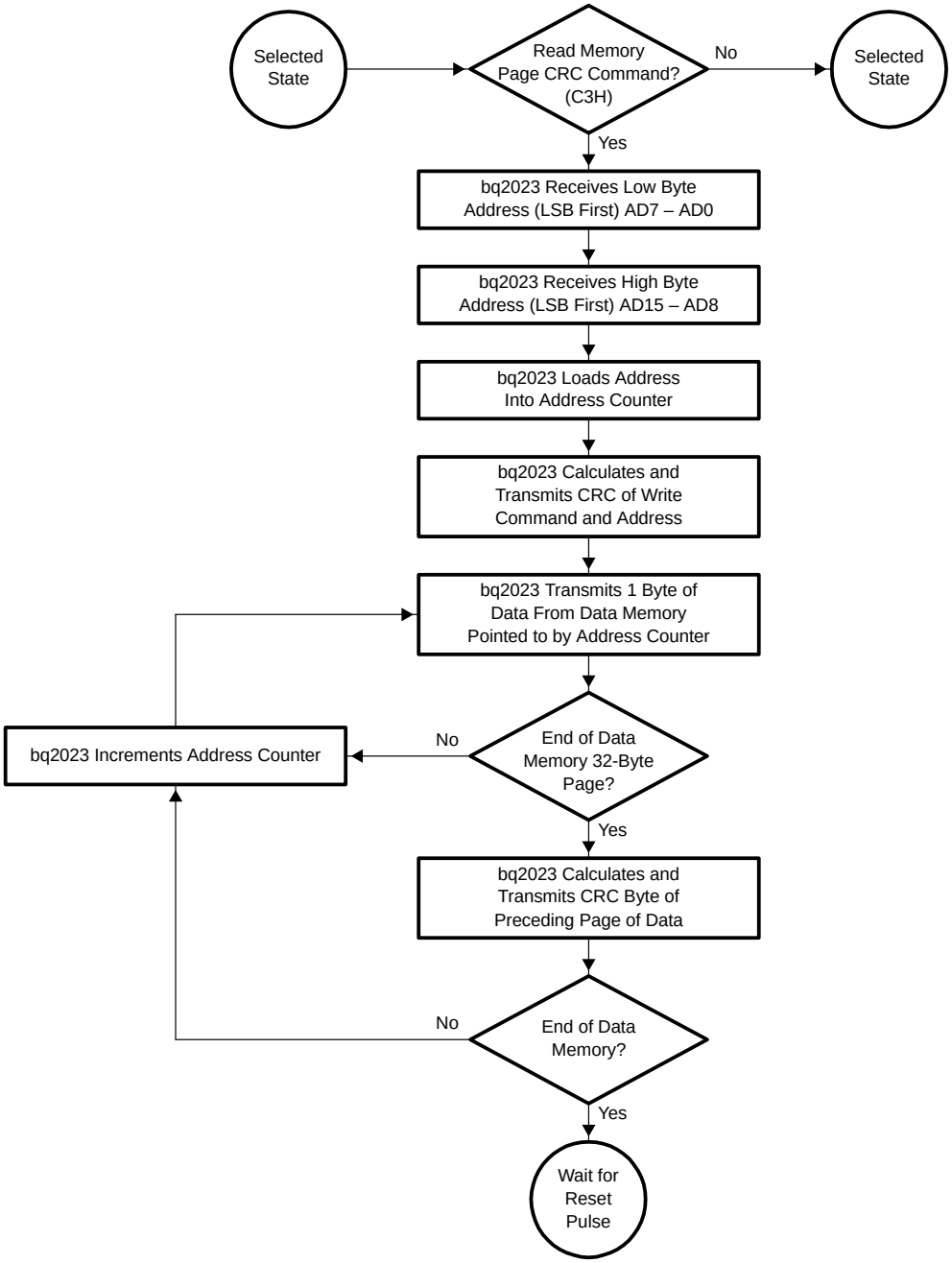


Figure 9. Read Memory and Generate PAGE CRC Command Flow

APPLICATION INFORMATION

read memory/field CRC

The read memory/field CRC command reads part or all of the 271 memory addresses shown in the register map with an 8-bit CRC generated at the end of the 271-byte register map.

The flowchart in figure 10 illustrates when the bq2023 is in the selected state. The read memory/field CRC command, F0 hex, directs the bq2023 to load the next two bytes, low byte and high byte of the starting address, into the address counter. Individual bytes of address and data are transmitted least significant bit first. An 8-bit CRC of the command byte and address bytes is computed and transmitted by the bq2023. When the bq2023 detects a start frame for read time slots, it transmits data from the 271 available registers bytes as pointed to by the address counter. After each byte of data is transmitted, the address counter is incremented. This process repeats until the end of the register map is reached. At the end of the data field, the bq2023 calculates and transmits another 8-bit CRC of all data bytes read from the initial starting byte through the last byte of memory.

The read memory/field CRC command sequence can be terminated at any point by issuing a reset pulse.

write data memory

The write data memory command programs the 224 bytes of flash and modifies RAM registers that can be written. Data are first written into a communication buffer. When programming flash, the contents of the communication buffer are ANDed with the contents of the flash memory field when the programming code is issued. Before programming, data in flash will appear as 1s. When writing to non-flash registers, the bq2023 copies data from the communication buffer into the byte to be modified.

The flowchart in Figure 11 illustrates that when the bq2023 is in the selected state, the write data memory command, 0F hex, directs the bq2023 to load the next two bytes (low byte and high byte of the starting address) into the address counter. Eight bits of data are transmitted to the bq2023. Individual bytes of address and data are transmitted least significant bit first. The bq2023 calculates and transmits an 8-bit CRC based on the write data memory command, address, and data. The highest starting address of the bq2023 is 10F hex.

After verifying the CRC, the host issues the programming code, 5A hex. Then the communication buffer is logically ANDed with the contents of the flash byte pointed to by the address register.

NOTE:

If the address is greater than DF or not equal to 101 hex, no programming code is required, because the write is to a RAM register.

The data are then transmitted back to the host from flash to verify that the byte was correctly programmed or written. If the address is less than 10F hex and is a modifiable location, then the next byte of data may be transmitted to the bq2023 from the host. The bq2023 calculates the 8-bit CRC by loading the least significant byte of the address register and shifting in the new data. This CRC is then transmitted for verification.

The write data memory command sequence can be terminated at any point by issuing a reset pulse.

APPLICATION INFORMATION

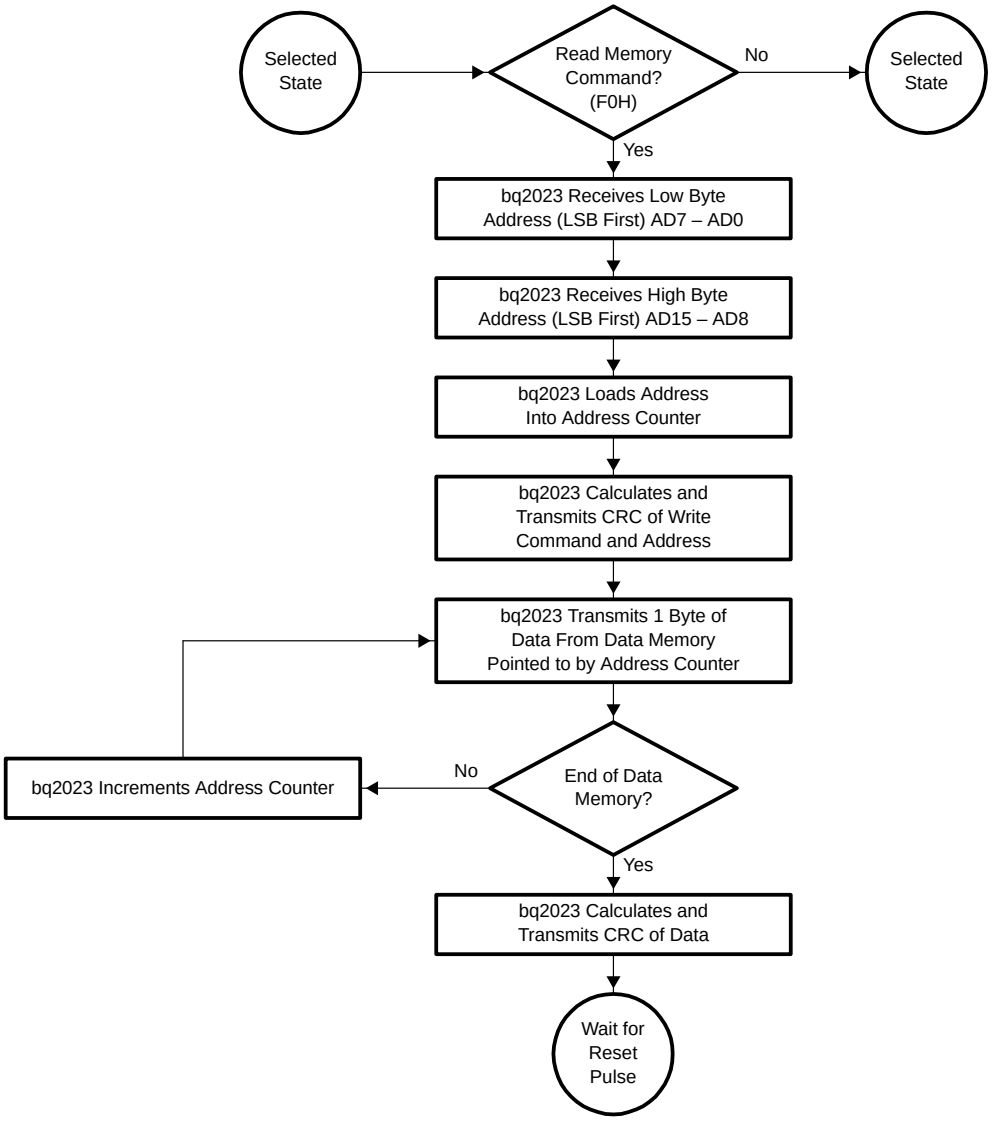


Figure 10. Read Data Memory With Field CRC Command Flow

APPLICATION INFORMATION

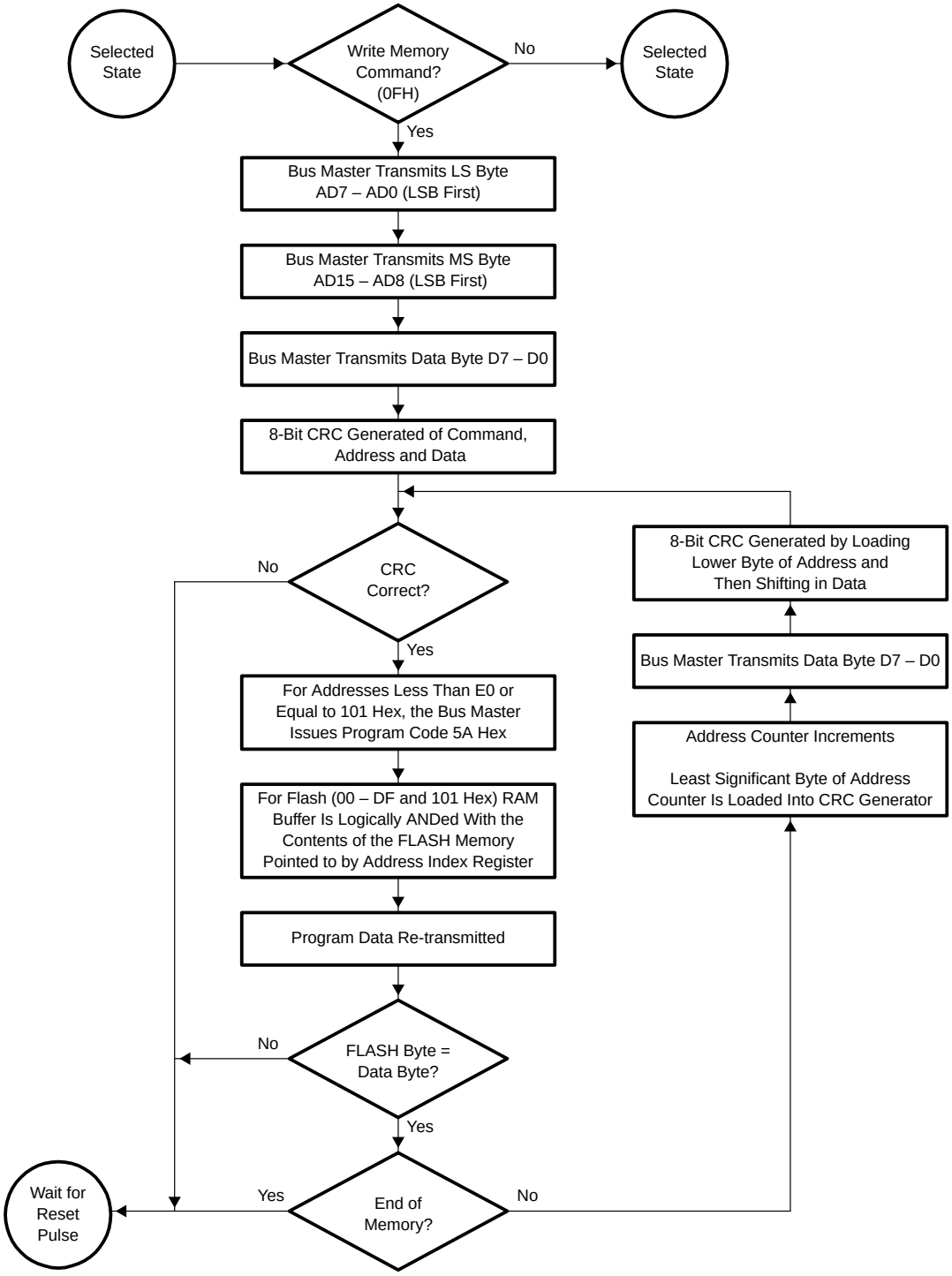


Figure 11. Write Memory Command Flow

APPLICATION INFORMATION

program profile byte

The program profile byte provides the user a convenient method to differentiate the programming profile required by the bq2023 from other similar products. The flowchart in Figure 12 illustrates that when the bq2023 is in the selected state, the program profile byte, 99 hex, directs the bq2023 to transmit the value 55 hex.

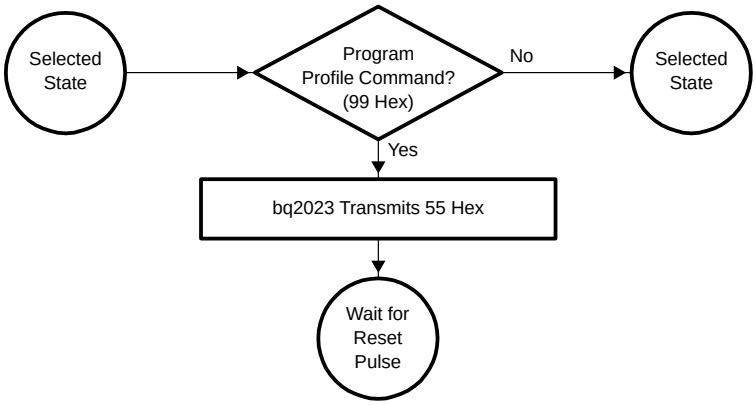


Figure 12. PROGRAM PROFILE Command Flow

flash erase command sequence

The flash erase command erases individual pages of flash. The flowchart in Figure 13 illustrates when a ROM command has selected the bq2023, 40 hex directs the bq2023 into the erase page mode. The host then transmits the 16-bit page erase codes found in Table 6 for the desired page to be erased.

Table 7. Page Erase Codes

FLASH PAGE	CODE (HEX)
0	0000
1	0020
2	0040
3	0060
4	0080
5	00A0
6	00C0

An 8-bit CRC of the command byte and page code is computed and transmitted by the bq2023. If the CRC is correct, the host then transmits code 5A hex to begin the erase.

APPLICATION INFORMATION

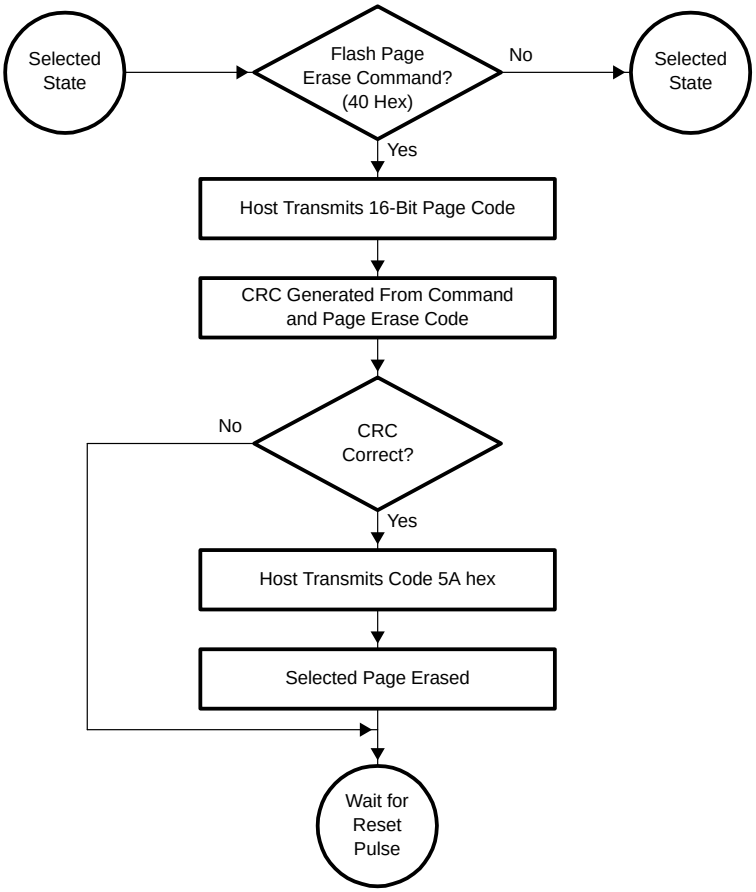


Figure 13. FLASH Erase Command

bq2023 registers

physical address space

The highest address decoded by the bq2023 is 0x011f. Physical registers located between 0x0020 and 0x00ff are repeated on 256-byte boundaries, starting at 0x0120. Any write to address 0x0120 and above can cause a data overwrite to FLASH and/or RAM.

register maintenance

The host system is responsible for register maintenance. To facilitate this maintenance, the bq2023 has a clear register (TMP/CLR) that resets the specific counter or register pair to zero. The host system clears a register by writing the corresponding register bit to 1. When the bq2023 completes the reset, the corresponding bit in the TMP/CLR register is automatically reset to 0, which saves the host an extra write/read cycle. Clearing the DTC register clears the STD bit and sets the DTC count rate to the default value of 1 count per 0.8789 s. Clearing the CTC register clears the STC bit and sets the CTC count rate to the default value of 1 count per 0.8789 s.

APPLICATION INFORMATION

bq2023 registers (continued)

Table 8. bq2023 Register Map

ADDRESS	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x010F	DCRH	Discharge count register high byte							
0x010E	DCRL	Discharge count register low byte							
0x010D	CCRH	Charge count register high byte							
0x010C	CCRL	Charge count register low byte							
0x010B	SCRH	Self discharge count register high byte							
0x010A	SCRL	Self-discharge count register low byte							
0x0109	DTCH	Discharge timer counter register high byte							
0x0108	DTCL	Discharge timer count register low byte							
0x0107	CTCH	Charge timer counter register high byte							
0x0106	CTCL	Charge timer counter register low byte							
0x0105	MODE/WOE	RSVD	SLEN	STC	STD	WOE2	WOE1	WOE0	RSVD
0x0104	CLR	RSVD	POR	STAT	CTC	DTC	SCR	CCR	DCR
0x0103	TEMPH	Temperature high byte							
0x0102	TEMPL	Temperature low byte							
0x0101	FED	RSVD	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0
0x0100		Reserved							
0x00E0-0x00FF	RAM	Page 7, 32 bytes of RAM							
0x00C0-0x00DF	Flash	Page 6, 32 bytes of flash							
0x00A0-0x00BF	Flash	Page 5, 32 bytes of flash							
0x0080-0x009F	Flash	Page 4, 32 bytes of flash							
0x0060-0x007F	Flash	Page 3, 32 bytes of flash							
0x0040-0x005F	Flash	Page 2, 32 bytes of flash							
0x0020-0x003F	Flash	Page 1, 32 bytes of flash							
0x0000-0x001F	Flash	Page 0, 32 bytes of flash							

register descriptions

id ROM

The factory programmed ID ROM can be programmed to customers specification. Contact Texas Instruments for details.

discharge count registers (DCRH/CRL0

The DCRH high-byte register (address 010F hex) and the DCRL low-byte register (address 010E hex), which contain the count of the discharge, are incremented whenever $V_{SRP} < V_{SRN}$ (1 LSB = 3.05 μV-hr). These registers continue to count beyond FFFF hex, so proper register maintenance should be done by the host system. The TMP/CLR register forces the reset of both the DCRH and DCRL to zero when the DCR bit is set.

charge count registers (CCRH/CCRL)

The CCRH high-byte register (address 010D hex) and the CCRL low-byte register (address 010C hex), which contain the count of the charge, are incremented whenever $V_{SRP} > V_{SRN}$ (1 LSB = 3.05 μV-hr). These registers continue to count beyond FFFF hex, so proper register maintenance should be done by the host system. The TMP/CLR register forces the reset of both the CCRH and CCRL to zero when the CCR bit is set.

APPLICATION INFORMATION

register descriptions (continued)

self-discharge count registers (SCRH/SCRL)

The SCRH high-byte register (address 010B hex) and the SCRL low-byte register (address 010A hex) contain the self-discharge count. This register is continually updated in both the normal operating and sleep modes of the bq2023. The counts in these registers are incremented on the basis of time and temperature. The SCR counts at 1 count per hour at 20–30°C and doubles every 10°C to greater than 60°C (16 counts/hour). The count halves every 10°C below 20–30°C to less than 0°C (1 count/8 hours). These registers continue to count beyond FFFF hex, so proper register maintenance should be done by the host system. The TMP/CLR register forces the reset of both the SCRH and SCRL to zero when the SDR bit is set. During device sleep the bq2023 wakes approximately every hour for 4 seconds to maintain the self-discharge registers.

discharge time count registers (DTCH/DTCL)

The DTCH high-byte register (address 0109 hex) and the DTCL low-byte register (address 0108 hex) determine the length of time that $V_{SRP} < V_{SRN}$, indicating a discharge. The counts in these registers are incremented at 4096 counts per hour. If the DTCH/DTCL register continues to count beyond FFFF hex, the STD bit is set in the MODE/WOE register indicating a rollover. Once set, DTCH and DTCL increment at 16 counts per hour.

NOTE:

If a second rollover occurs, STD is cleared. Access to the bq2023 should be timed to clear DTCH/DTCL more often than every 170 days. The TEMP/CLR register forces the reset of both the DTCH and DTCL to zero when the DTC bit is set.

charge time count registers (CTCH/CTCL)

The CTCH high-byte register (address 0107 hex) and the CTCL low-byte register (address 0106 hex) determine the length of time that $V_{SRP} > V_{SRN}$, indicating a charge. The counts in these registers are incremented at 4096 counts per hour. If the CTCH/CTCL registers continue to count beyond FFFF hex, the STC bit is set in the MODE/WOE register, indicating a rollover. Once set, CTCH and CTCL increment at 16 counts per hour.

NOTE:

If a second rollover occurs, STC is cleared. Access to the bq2023 should be timed to clear CTCH/CTCL more often than every 170 days. The TMP/CLR register forces the reset of both the CTCH and CTCL to zero when the CTC bit is set.

mode, wake-up enable register (MOE/WOE)

The Mode/WOE register (address 0105 hex) contains the SLEEP ENABLE bit, the STC and STD bits, and wake-up enable information as described below:

MODE/WOE BITS							
7	6	5	4	3	2	1	0
RSVD	SLEN	STC	STD	WOE2	WOE1	WOE0	RSVD

RSVD BIT7 is a reserved bit and must always be set to 0. This bit is cleared on Power-on-Reset.

SLEN The SLEN bit allows the bq2023 to enter sleep mode. The bq2023 enters sleep mode if battery current (i.e., voltage difference between the SRP and SRN pins) is less than WOE threshold, the SLEN bit is set, and there is no communication activity on the SDQ pin for approximately one hour. The bq2023 wakes on either a low-to-high or high-to-low transition on the SDQ pin. The SLEN bit is set during power-on-reset or after a wake-up condition.

NOTE:

Entering sleep mode does not clear this bit. It must be cleared by the host. This bit is set during power-on-reset.

APPLICATION INFORMATION

register descriptions (continued)

STC and STD The slow time charge (STC) and slow time discharge (STD) flags indicate if the CTC or DTC registers have rolled over beyond FFFF hex. STC set to 1 indicates a CTC rollover; STD set to 1 indicates a DTC rollover. These bits are in indeterminate states on power-on-reset.

WOE[2..0] The wake-up output enable (WOE) bits (bits 3–1) set the wake-up enable signal level. Whenever $|V_{SRP} - V_{SRN}| < V_{WOE}$, and the SLEN bit is set the bq2023 will enter sleep mode, after approximately one hour of inactivity on SDQ pin. Setting all of these bits to zero will cause the device to sleep if SLEN is set and there is no SDQ activity, regardless of V_{SRP}-V_{SRN} voltage. Refer to Table 3 for the various WOE values. All WOE bits are set to 1 on power-on-reset.

RSVD BIT0 is a reserved bit and must always be set to 0. This bit is cleared on power-on-reset.

clear register (CLR)

As described in the table below, the bits in the CLR register (address 0104 hex) clear the DCR, CCR, SCR, DTC and CTC registers, determine if a power-on-reset occurred, and set the state of the STAT pin.

CLR BITS							
7	6	5	4	3	2	1	0
RSVD	POR	STAT	CTC	DTC	SCR	CCR	DCR

RSVD Reserved for future use.

POR The POR bit (bit 6) indicates a power-on-reset has occurred. This bit is set when VCC has gone below the POR level. This bit can be set and cleared by the host, but setting has no effect.

STAT The STAT bit (bit 5) sets the state of the open drain output of the STAT pin. A 1 turns off the open drain output while a 0 turns the output on. This bit is set to a 1 on power-on-reset.

CTC The CTC bit (bit 4) clears the CTCH, CTCL registers and the STC bit. A 1 clears the corresponding registers and bit. After the registers are cleared, the CTC bit is cleared. This bit is cleared on power-on-reset.

DTC The DTC bit (bit 3) clears the DTCH, DTCL registers and the STD bit. A 1 clears the corresponding registers and bit. After the registers are cleared, the DTC bit is cleared. This bit is cleared on power-on-reset.

SCR The SCR bit (bit 2) clears both the SCRH and SCRL registers. Writing a 1 to this bit clears the SCRH and SCRL register. After these registers are cleared, the SCR bit is cleared. This bit is cleared on power-on-reset.

CCR The CCR bit (bit 1) clears both the CCRH and CCRL registers. Writing a 1 to this bit clears the CCRH and CCRL registers. After these registers are cleared, the CCR bit is cleared. This bit is cleared on power-on-reset.

DCR The DCR bit (bit 0) clears both the DCRH and DCRL registers to 0. Writing a 1 to this bit clears the SCRH and SCRL register. After these registers are cleared, the SCR bit is cleared. This bit is cleared on power-on-reset.

temperature registers

The TMPH register (address 0103 hex) and the TMPL register (address 0102 hex) report die temperature in hex format in increments of 0.25°K. These read-only temperature registers count at 1 count/0.25K. The read at 25°C (i.e., 298°K) will be 0x4A8 hex.

APPLICATION INFORMATION

register descriptions (continued)

flash erase disable (FED) register

The FED register (address 101 hex) contains the bits that disable the flash erase on page boundaries. When a bit is cleared, the corresponding page of flash can no longer be programmed or erased. Once a disable erase page bit has been set, it cannot be cleared. This register is a flash register, programmed using the write memory command protocol, and it requires issuing the program code 5A hex after CRC verification.

FED BITS							
7	6	5	4	3	2	1	0
RSVD	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

RSVD Reserved for future use.

PAGE6 The PAGE6 bit disables PROGRAM/ERASE for flash memory locations C0 through DF hex when set to 0.

PAGE5 The PAGE5 bit disables PROGRAM/ERASE for flash memory locations A0 through BF hex when set to 0.

PAGE4 The PAGE4 bit disables PROGRAM/ERASE for flash memory locations 80 through 9F hex when set to 0.

PAGE3 The PAGE3 bit disables PROGRAM/ERASE for flash memory locations 60 through 7F hex when set to 0.

PAGE2 The PAGE2 bit disables PROGRAM/ERASE for flash memory locations 40 through 5F hex when set to 0.

PAGE1 The PAGE1 bit disables PROGRAM/ERASE for flash memory locations 20 through 3F hex when set to 0.

PAGE0 The PAGE0 bit disables PROGRAM/ERASE for flash memory locations 00 through 1F hex when set to 0.

CRC generation

The bq2023 has an 8-bit CRC stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the bq2023 to determine if the ROM data have been received error-free by the bus master. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$. The CRC generator circuit is shown in Figure 14.

Under certain conditions, the bq2023 also generates an 8-bit CRC value using the same polynomial function shown above and provides this value to the bus master to validate the transfer of command, address, and data bytes from the bus master to the bq2023. The bq2023 receives data bytes for the write memory and flash page erase commands. It computes an 8-bit CRC for the command, address, and data bytes of each of these commands and then outputs this value to the bus master to confirm proper transfer. Similarly the bq2023 computes an 8-bit CRC for the command and address bytes received from the bus master for the Read Memory commands to confirm that these bytes have been received correctly.

In each case where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function given above and compare the calculated value to either the 8-bit CRC value stored in the 64-bit ROM portion of the bq2023 (for ROM reads) or the 8-bit CRC value computed within the bq2023. The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry on the bq2023 that prevents a command sequence from proceeding if the CRC stored in or calculated by the bq2023 does not match the value generated by the bus master.

APPLICATION INFORMATION

CRC generation (continued)

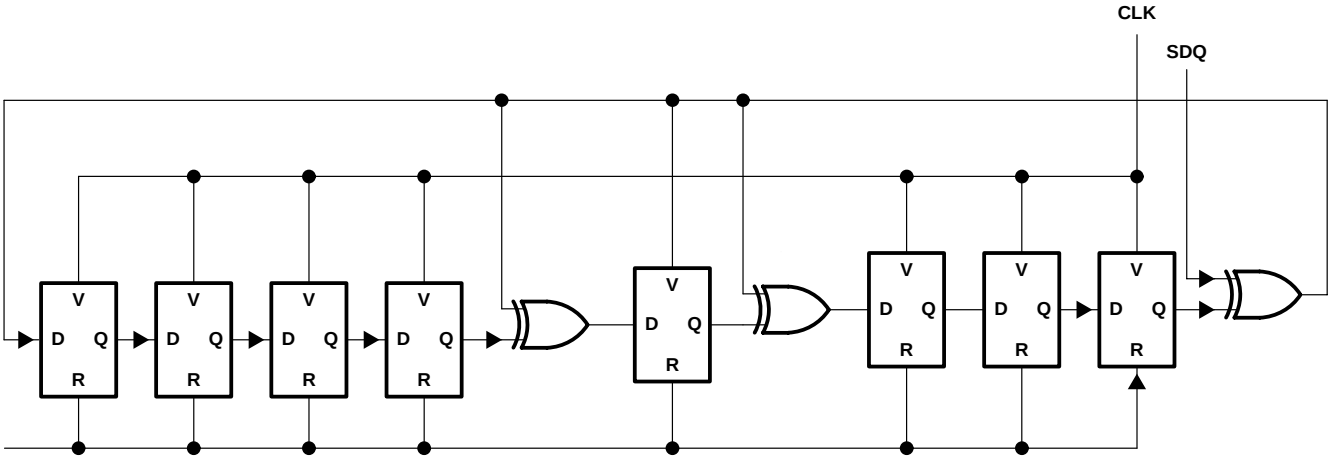


Figure 14. 8-Bit CRC Generator Circuit ($X^8 + X^5 + X^4 + 1$)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ2023PW	Last Time Buy	Production	TSSOP (PW) | 8	100 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	2023
BQ2023PW.B	Last Time Buy	Production	TSSOP (PW) | 8	100 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	2023
BQ2023PWR	Last Time Buy	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	2023
BQ2023PWR.B	Last Time Buy	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	2023

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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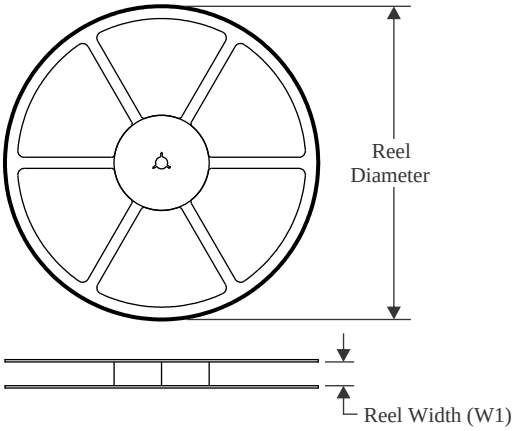
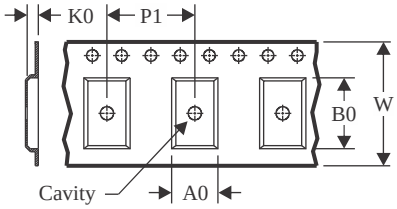
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

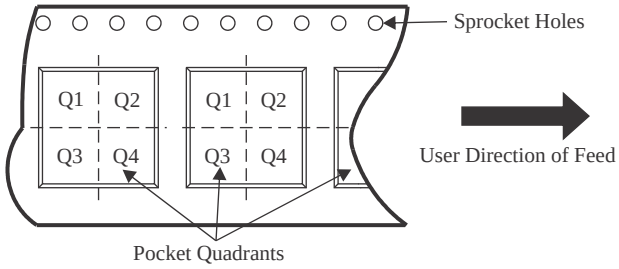


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

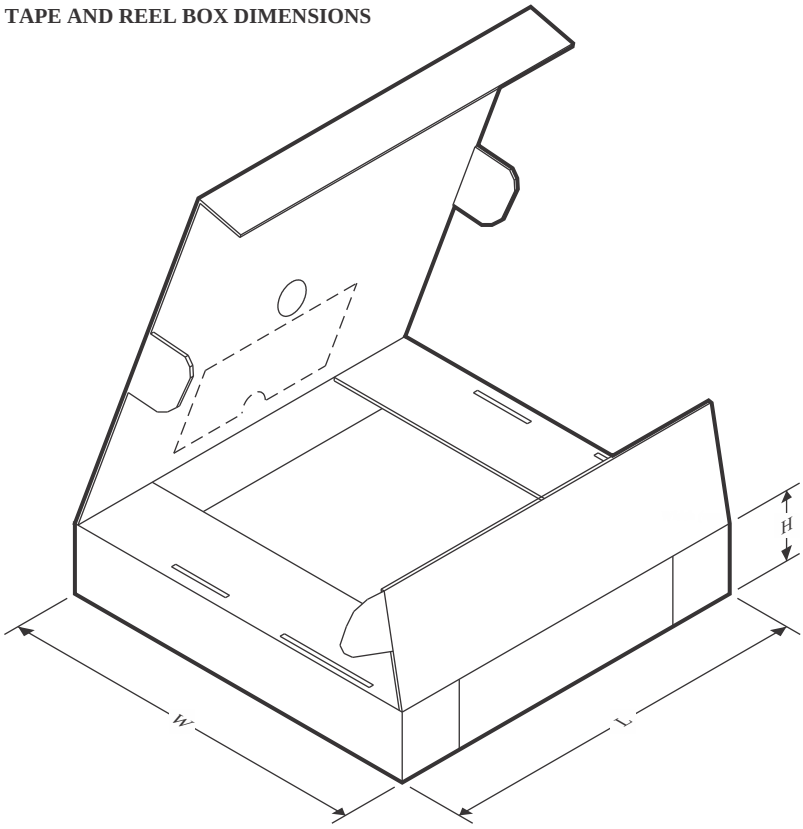
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2023PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

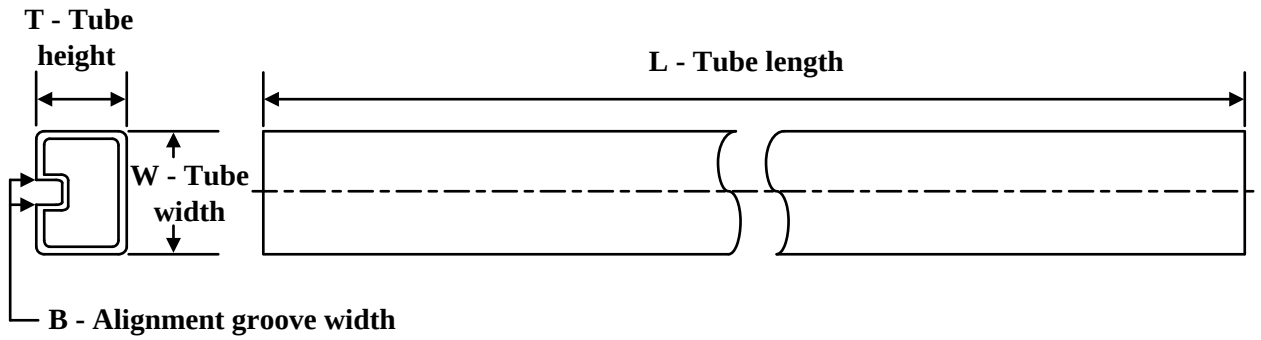
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2023PWR	TSSOP	PW	8	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

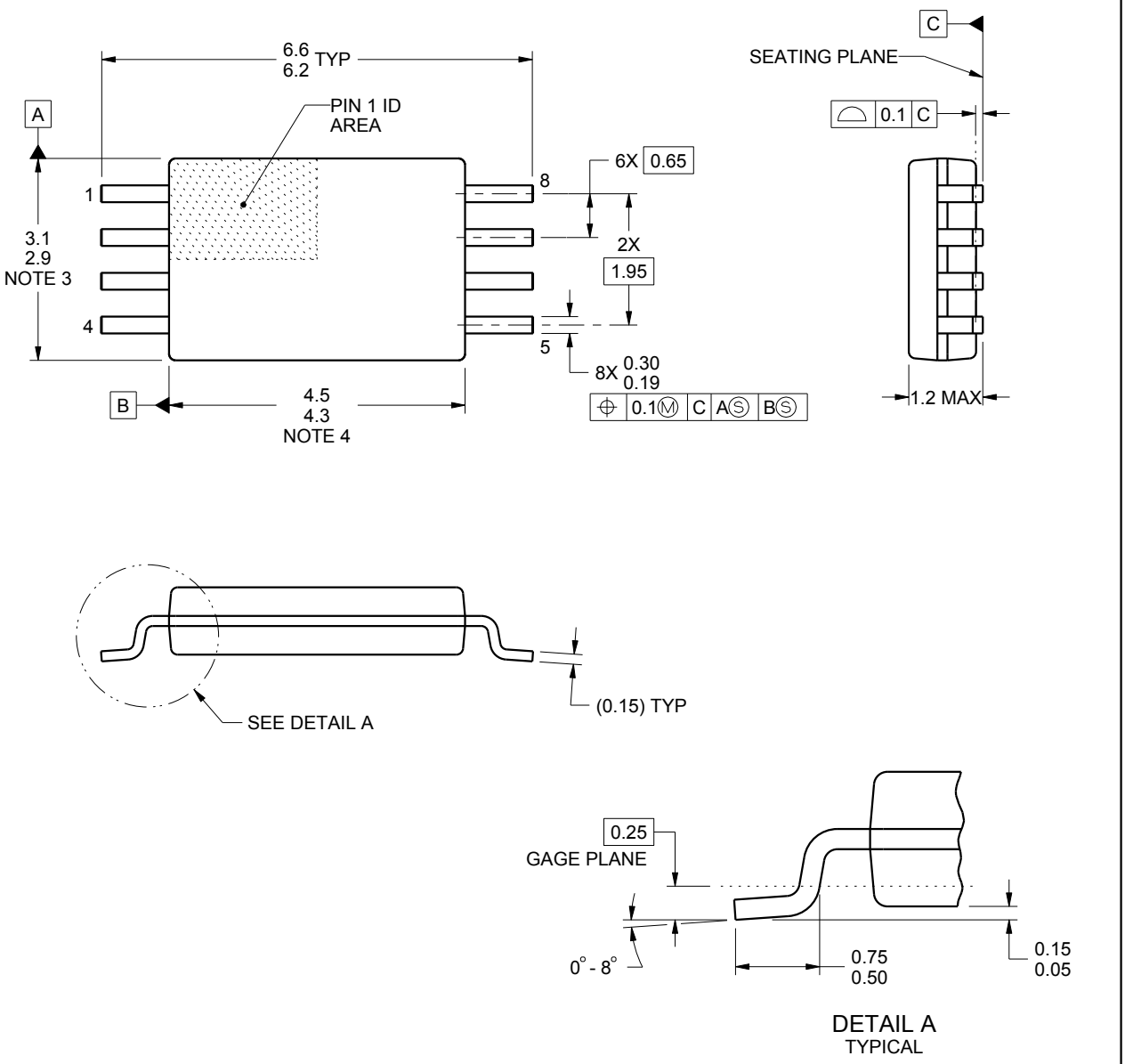
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ2023PW	PW	TSSOP	8	100	300	8.5	3250	4
BQ2023PW.B	PW	TSSOP	8	100	300	8.5	3250	4

PACKAGE OUTLINE

PW0008A

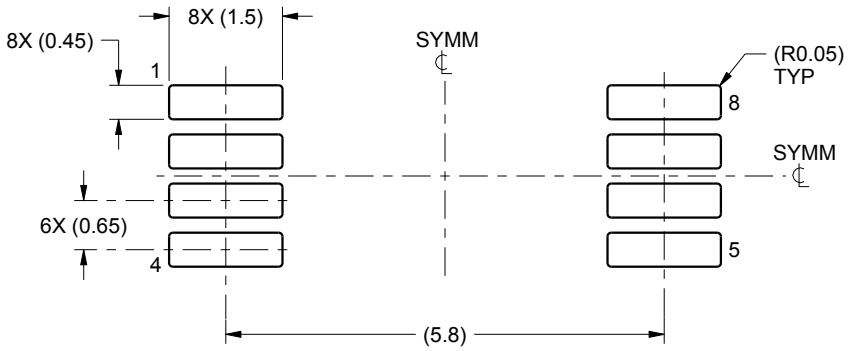
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

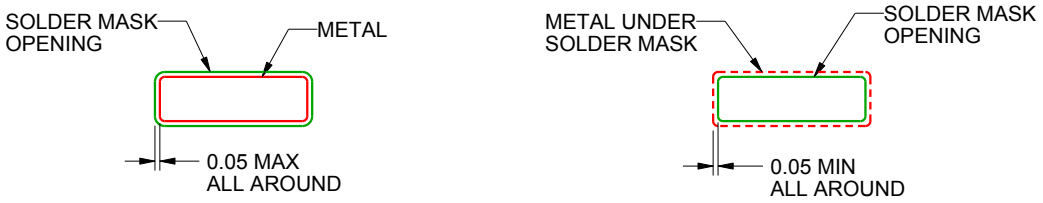


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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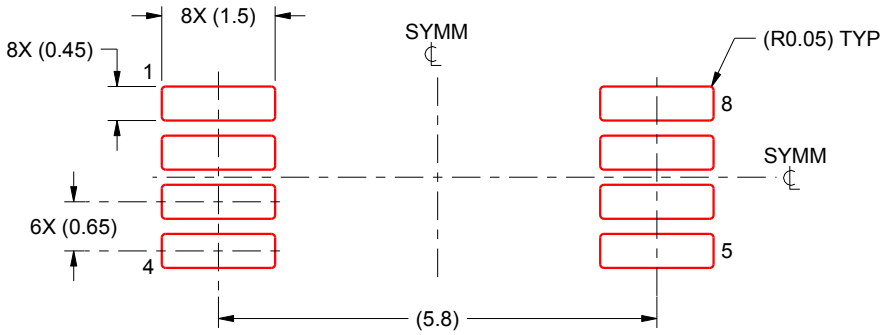
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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