Application Report

Voltage Reference Selection and Design Tips For Data Converters

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ABSTRACT

When designing a data converter system it is important to choose the correct voltage reference for the application. Every data converter, such as an Analog-to-digital converter (ADC) or Digital-to-analog converter (DAC), requires a voltage reference (VREF) that is either integrated into the data converter or supplied from an external source. Just like the resolution of an ADC, voltage references have critical performance attributes that separate voltage references into tiers of accuracy. Due to this it is necessary to be able to choose the correct voltage reference to achieve the highest resolution given the system considerations.

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Trademarks

1 Introduction

Voltage references (VREF) are beneficial and often necessary for high-accuracy signal chain applications. This is because a standard signal chain contains a data converter, such as the Analog-to-digital converter (ADC) or Digital-to-analog converter (DAC), which measure or create a precise signal. In the signal chain, the voltage reference output is typically the most precise voltage available to a data converter because many signal chain applications are sensitive to variations in gain error or noise error. It is important to consider how an error might impact the system. Understanding the various voltage reference errors of voltage reference errors is important for recognizing the benefits and limitations of integrated voltage references versus external voltage references.

2 Analog-to-Digital Converter Error

Understanding voltage reference specifications is necessary to evaluate the right voltage reference for the signal chain application. The main errors affecting the signal chain elements such as an ADC are gain error, noise error, and dynamic error. In ADCs, the gain error is a static error that effects every sample in a continuous sampling period of an ADC and can be reduced or eliminated with calibration. Noise error is an error that affect every sample independently and randomly and is inherent to semiconductor devices and architectures. Examples of noise error are 1/f noise and broadband noise. In ADCs, the noise will affect all the measurements and it cannot be eliminated but it can be attenuated through filtering or by using digital processing techniques. Dynamic error is an error that is caused by fast switching voltage rails or change in load current. This is often associated with the input rails of the ADC but dynamic error also applies to any fast switching on output of the voltage reference. Dynamic error in this document is focused around droop error which is related to the data converter architecture and voltage reference output stage. Gain, noise, and dynamic errors will be affected by the voltage reference performance. Table 2-1 covers general guidelines on voltage reference to ADC/DAC pairings but there is still flexibility based on system requirements. The background behind these choices will be covered in this document.

Table 2-1. Example Voltage Reference Recommendation to Data Converters

ADC RESOLUTION	ADC RECOMMENDATION	DAC RESOLUTION	DAC RECOMMENDATION	VOLTAGE REFERENCE RECOMMENDATION
10-b	ADS7948	8-b	DAC43608	TL431LI, TLV431
12-b	ADS7822	10-b	DAC53608	LM4040-N, LM4050-N, REF30
14-b to 16-b	ADS8324, ADS8381	12-b	DAC61402	REF31, REF33, REF4132
16-b to 18-b	ADS1112, ADS1287	14-b to 16-b	DAC8802	REF34, REF50
18-b+	ADS8900B, ADS127L01	16-b+	DAC11001A	REF70

3 Voltage Reference DC Error

DC error in a voltage references is a culmination of a variety of statics errors. It is important to understand how this error exists and its origin to better understand when it will impact the measurements and system as a whole. DC error in a voltage reference will affect the signal chain as a gain error in a data converter such as an ADC or as an offset for level shifting applications. The importance of gain error on ADC will depend on the measurements that are being performed as it will have a larger impact on DC or very low frequency measurements such as measuring voltage and current. This gain error will also be evident in time-domain based measurements. Table 2-1 shows example voltage reference recommendations based on ADC resolution based on voltage reference DC error to have a low gain error in the system. Refer to *Voltage Reference Selection Basics* for an understanding of key parameters regarding voltage references.

3.1 Initial Accuracy and Solder Shift

Initial accuracy of a system dictates how close a reference voltage is to its nominal voltage at 25C. This voltage deviation typically has a guaranteed max deviation that is given in percent. Typical values of initial accuracy are 0.05% to 2% (500 – 20,000 ppm). This wide range of initial accuracy values can be used to separate reference voltages into different tiers of accuracy such as in Table 3-1. Initial accuracy is also only valid for the specified conditions on the electrical characteristics table.

Table 3-1. Initial Accuracy

ACCURACY	RANGE
High	< 0.1%
Medium	0.1% - 0.5%
Low	> 0.5%

One common misconception is that the reference voltage error measured on a soldered PCB board at 25C is just a component of initial accuracy. This statement is incorrect because every device that is soldered will experience an initial thermal shock that can affect the initial accuracy of the device. The deviation due to solder shift is not always reported on a datasheet but even if the solder shift is not reported, this a physical phenomena that will always be present. If a design requires a device to go through multiple solder reflows then the expected deviation will be much larger. It is very difficult to separate solder shift and initial accuracy on a soldered device. Note that the initial accuracy and solder shift do not include the effects of accuracy shifts from long term shift, thermal hysteresis, or thermal drift.

Initial accuracy and solder shift are gain errors that can both be calibrated and this is common in very high resolution systems but not so often in low resolution systems due to calibration cost. In low resolution systems it is important to consider is that the initial accuracy and solder shift can be the largest DC errors a voltage reference. If there is no calibration in the system then the initial accuracy will be a dominant factor and it will be important to choose the device with the best accuracy to lower the total error. In higher resolution systems the initial accuracy and solder shift must be calibrated out as even a 0.1% difference in accuracy across devices can severely degrade the performance of 18-bit resolution systems. Therefore these gain errors are typically calibrated out by measuring the output voltage of the voltage reference at 25C to know the deviation. By knowing this value the effect becomes negligible or non-existent as it can be taken into account in the digital calculations.

3.2 Temperature Drift

Temperature Drift is the change in reference voltage over temperature. This specification is usually defined by the box method technique. More details on how the box method is calculated are in TI's *Voltage reference selection basics white paper*. There are several considerations when it comes to choosing the correct temperature drift due to the non-linear nature. One consideration is that the drift is usually defined as an average and can be bigger or smaller in particular regions. The shape of the temperature drift curve will vary in a linear or non-linear way based on the reference architecture and the curvature correction methods used. One common misconception is that the voltage reference core, buried zener or bandgap, will dictate the final temperature drift curvature of the device. This is not the case because most voltage reference cores have surrounding circuitry for trimming and adjusting the temperature curvature which will adjust the original core temperature shape. Table 3-2 shows the relationship between temperature drift and percent error to demonstrate how temperature drift can be compared to accuracy.

Table 3-2. Temperature Coefficient Into Percent Error

TEMP COEFFICIENT (ppm/°C)	ERROR FROM 0°C to 70°C (%)	ERROR FROM -40°C to 85°C (%)	ERROR FROM -40°C to 125°C (%)
1	0.0070	0.0125	0.0165
5	0.0350	0.0625	0.0825
10	0.0700	0.1250	0.1650
50	0.3500	0.6250	0.8250
100	0.7000	1.2500	1.6500

3.3 Line Regulation

Line regulation is defined as change in the output voltage of a reference with respect to change in the supply voltage in the specified region. Line regulation error directly gets translated into gain error. This is critical for battery operated systems where input varies as the battery power goes down. A LDO with good line regulation spec is used as the supply for the reference to improve the line regulation performance of the system. This also applies to systems where the VIN will vary on the input of the voltage reference due to other loads on the same rail.

4 DC Error Calculations

To ensure that a system meets the gain error specifications, it is important to characterize the gain error into a usable value. This is important because gain error affects the signal chain in a different way than dynamic error and noise error. For example, when a voltage reference supplies the reference for an ADC, the DC errors of the voltage reference will combine with the gain error of the ADC. When measuring a signal, this means that the gain error will scale proportionally to the in ADC analog signal as shown in Figure 4-1. The gain error will appear as an inaccuracy on the final ADC conversion but this can be minimized with calibration. The max gain error will appear closer to the positive or negative full scale value of the ADC.

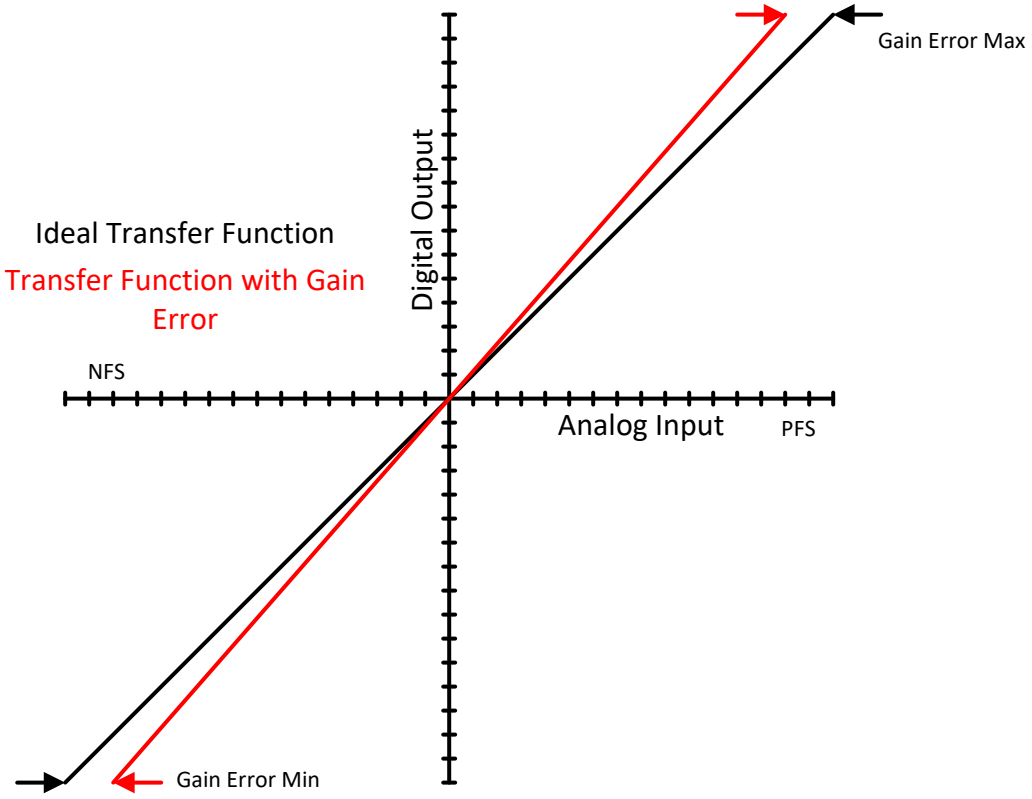

Figure 4-1. ADC Input to Output With Gain Error

An issue with characterizing the signal chain error with an integrated voltage reference is that typically internal voltage references are not fully characterized as in depth as external voltage references and often lack maximum worst case values. Due to this it is difficult to calculate the worst case gain error of the system. This challenge can be resolved by using an external voltage reference. The main reason to know the extrema is because not every system will have the same level of calibration. If a signal chain only has gain error calibration at 25C the gain error will be decreased at 25C. If the same system experiences any environmental variations then the gain error will change and be unaccounted which can take a sensitive system out of tolerance. There are many applications where the internal voltage reference is sufficient but in other applications it might not exists internally.

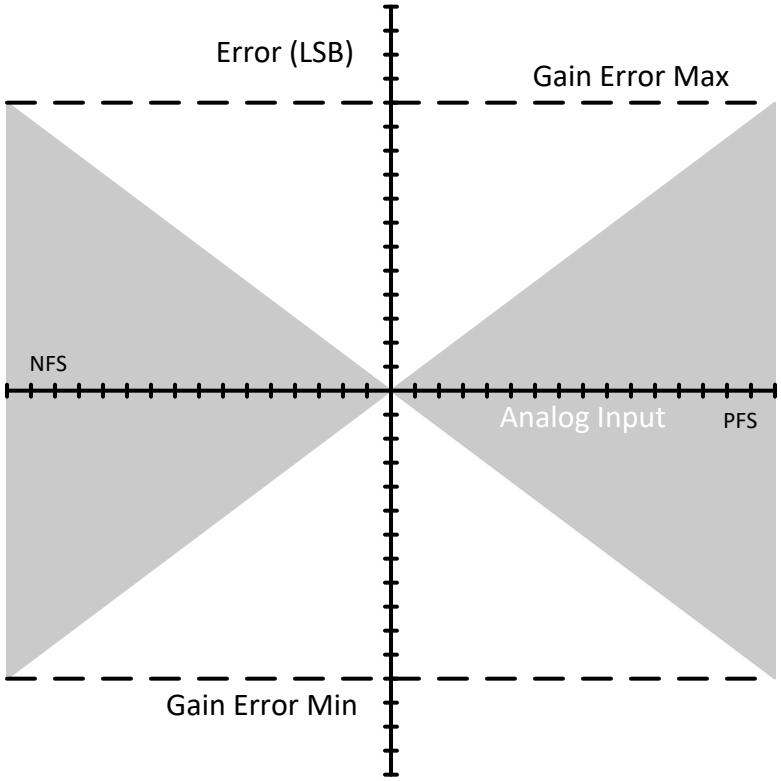

Figure 4-2. ADC Gain Error

There are two ways to calculate error in a system: worst-case and root sum squared (RSS). The main difference between the error calculations is how the individual errors of a system are combined. In worse case error all the errors are additive of the maximum extrema of each specification which results in an error value that encompass every device variation. The worst case error is calculated as the additive value of all the errors as shown in Equation 1 and it covers all the test conditions and limits. A alternative to the worst-case method is the RSS method that is based on statistical tolerance analysis as shown in Equation 2 that applies when all the terms are uncorrelated. In the real world, the error will be between the worst-case and RSS method of results but closer to the RSS result.

$$\text{Worst Case Error}_{VREF} = \text{Accuracy} + \text{TempCo} + \text{TempHyst} + \text{Long Term Drift} + 1/f\ \text{Noise} + ... \quad (1)$$

$$\text{RSS Error}_{VREF} = \sqrt{(\text{Accuracy})^2 + (\text{TempCo})^2 + (\text{TempHyst})^2 + (\text{Long Term Drift})^2 + (1/f\ \text{Noise})^2 + ...} \quad (2)$$

The total gain error for a voltage reference is a culmination of all the errors such as initial accuracy, temperature coefficient, etc. To calculate the total error, all the errors must be in common units such as ppm (parts-per million). The voltage reference total gain error can be further reduced with calibration, as calibration can eliminate the static errors such as initial accuracy and temperature drift as shown in Table 4-1. For the purposes of this example, errors such as solder shift, long term drift, load regulation, line regulation, and solder shift among others have been omitted but they can be included to calculate a more accurate representation of the VREF total error. Other errors that were not mentioned can be found in Table 2-1. Table 4-1 shows how all the errors are combined using the RSS method.

Table 4-1. REF3425 Example

GAIN ERROR	GAIN ERROR VALUE	GAIN ERROR VALUE (ppm)
Initial Accuracy	0.05%	500
Temperature Drift (TempCo)	6 ppm/°C	990 (40°C to 125°C)
Temperature Drift Post Calibration (80% Reduction)	1.2 ppm/°C	198 (40°C to 125°C)
Thermal Hysteresis (TempHyst)	Cycle 1: 30 ppm, Cycle 2: 10ppm	40
1/f noise	15 uV_{P-P}	15
Worst Case Total	0.1545%	1545
RSS Total	0.111%	1110
RSS Total with 25C Calibration	0.0991%	991
RSS Total with 25C & TempCo Calibration	0.0202%	202

In Table 4-1 it is possible to see the comparison of total gain error under different conditions and the importance of calibration. By using Equation 3 and a known ADC resolution, the LSBs that will be affected by the gain error of the signal chain can be calculated.

$$LSB = \text{Gain Error}_{ppm} * 2^{N-bits} \quad (3)$$

5 Calibration

System calibration is often necessary in many signal chain applications to eliminate gain and offset errors. Calibration can remove the voltage reference DC error which will reduce the gain error but the amount of will depend on the calibration method. We can separate calibration into two main calibration categories, single point calibration and multipoint calibration and this can be seen in Table 5-1.

Table 5-1. Voltage Reference Calibration Methods

	SINGLE POINT CALIBRATION	MULTIPOINT CALIBRATION
Initial Accuracy	X	X
Solder Shift	X	X
Thermal Hysteresis	X	X
Temperature Drift		X

Single point calibration is calibration that is performed at one temperature point. This temperature point is usably either 25C or typical operating temperature of the system. The benefit of this type if calibration is that it can remove voltage reference DC errors post calibration. This type of calibration can be done multiple ways: factory calibration, start-up calibration, run time calibration. Factory calibration is performed at the assembly and test site. In the assembly and test site, the data converter input or output can be compared to a very precise voltage standard. By using the difference between the values, the ADC or microcontroller can store the value internally and adjust the output based on the measured difference. The benefit of this calibration is that measurements can be performed to a high precision and the signal chain system won't need its own built in self test. The drawback is that the calibration cannot be performed at the site of operation, it cannot take into account any drift due to aging, and it cannot predict the temperature operating conditions of the system. Start-up calibration and run-time calibration are single point calibration tests that are beneficial because they can remove the voltage reference DC error at the site of operation. This means that any effect of temperature and aging in the system will be taken into account but due to the lack of precise voltage standards, the precision of this calibration might not match the precision of a factory calibration. The inclusion of a built in self test for start-up or run-time calibration might require additional components which can increase the complexity of the system.

One of the main drawbacks to single point calibration is that it is only valid at a single temperature point and significant temperature variations will cause DC errors in the voltage reference that will increase the gain error of the data converter. Multi-point calibration is able to fix this draw back because calibration can be performed at multiple temperature points. In Figure 5-1 is it possible to see how much the temperature drift error gets reduced by using a multipoint calibration and creating a temperature profile based on differences that can be

used to adjust the final measurements. Typically the gain error correction will multiplicative to the end result of the data conversion. In this example a 3-point calibration decreased the temperature drift error by 3x and a 6 point decreased the error by over 10x. In this example, the final curvature of the 3-point and 6-point calibration lines were created by calculating the slope in between the measured points and then subtracting that result from the uncalibrated value. By knowing the error of the system, a designer can eliminate gain error digitally by multiplying the data converter result by the ratio of (uncalibrated VREF / calibrated VREF).

The temperature calibration is more effective in a smaller temperature windows due to this it is important to know the operating temperature the device will experience. In Figure 5-1 the uncalibrated waveform is a second order function but this can vary between devices. It is possible to get a first order to higher order curvatures. The temperature drift will vary from device to device which can be difficult to calibrate out the error across multiple devices with the same profile so it is recommended to calibrate each voltage reference with a unique profile. The drawback of multipoint calibration is the increase of cost, calibration time, and not all temperature curvatures are easy to calibrate. It can be attractive to choose a more precise voltage reference which better temperature drift to avoid performing multipoint calibration.

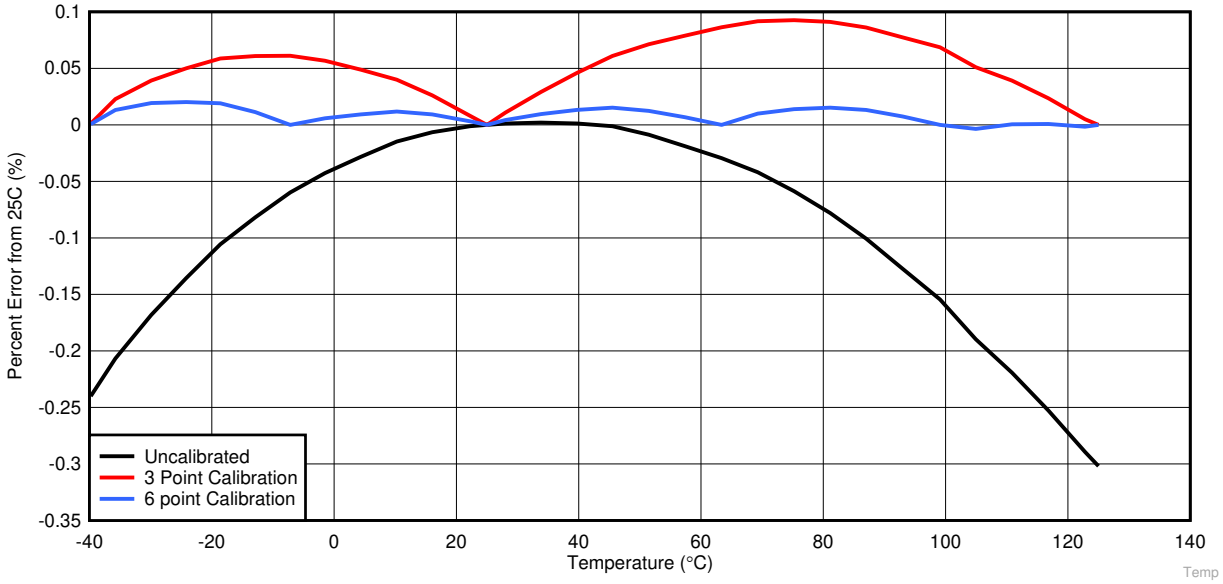

Figure 5-1. Temperature Drift Error With Calibration Profiles

In Table 3-2 the temperature drift error is converted into a percent error which makes it easily comparable to initial accuracy error. Keep in mind that this error is the maximum worst case deviation from 25C in a uncalibrated system. Most devices will not reach a deviation this high. It is often more practical in low resolution systems to choose the device with the lowest temperature drift specification as temperature calibration can be time consuming and costly. In high resolution systems it gets more complicated because the temperature drift needs to be minimized to maximize the ADC performance especially if the signal chain has signal conditioning components that will have their own temperature drift.

6 Voltage Reference Noise Error

Noise error is important because cannot be eliminated completely in any system with calibration and it will appear different on subsequent samples from a data converter. It difficult to achieve a consistent resolution in high precision data converter systems when there are large amounts of noise from the voltage reference. Noise can be divided into two categories: 1/f noise and broadband noise.

6.1 1/f Noise

1/f noise is a low frequency noise in the 0.1Hz to 10Hz range also known as flicker noise. This noise is troublesome due to how low the frequency range is and it is difficult to filter it out because large sampling time requirement. When performing DC measurements, this noise has a greater impact than broadband noise because it cannot be practically filtered out due to how low frequency it is. The only way to reduce the 1/f noise from a reference voltage is to go choose the lowest noise reference voltage and voltage option because noise scales with output voltage.

6.2 Broadband Noise

Broadband noise is a flat noise that spans the complete frequency range of the device also known as wideband noise. Unlike 1/f noise, broadband noise affects the whole frequency range relatively equally; it is practical to filter out as much noise as possible with either a RC filter or with digital filtering techniques. All circuits have broadband noise but they also have a bandwidth limitation that limits the effect of the broadband noise so the noise is not infinite. Broadband noise is specified as either output noise from 10Hz to 10kHz or as output voltage noise density. Conversion between output noise outside and output noise density can be found in the precision labs noise series. One problem that a designer might run into is that noise is inversely proportional to quiescent current and therefore it is difficult to achieve low noise in a low power system.

6.3 Power Supply Rejection Ratio

Power supply rejection ratio (PSRR) is a translation factor of the input noise to the output. It is defined for wide frequency range (10Hz to 10Mhz). Most series voltage references have a strong PSRR due to their inherent architecture, and this makes them suitable to handling noisy power lines especially with bypass and load capacitors. PSRR can be improved by making sure the input to the voltage reference is an LDO and not a switching device. It is analogous to dynamic impedance in case of shunt references as shunt voltage references will not have a PSRR as high as series voltage references. A large supply decoupling capacitor will help to improve the PSRR performance in case of noisy supply which can help with the over all high frequency noise.

6.4 Noise Example

When looking at noise in a signal chain it is important to see how it will affect the dynamic performance of an ADC. This is because SNR is one of the most important values when looking at AC and high frequency measurements which are common across many applications. the most common equation for SNR is shown in Equation 4 because this is the highest SNR level for an Ideal N bit ADC.

$$SNR_{ADC} = 6.02 \times N + 1.76\,dB \tag{4}$$

To see the effect of the external voltage reference it is necessary to look at the total noise at the ADC in Equation 5. The Total ADC noise (rms) is the combination of the uncorrelated noises from the ADC and voltage reference. Because they are uncorrelated, if we want the voltage reference to have a minimal impact on the SNR the VREF noise must be at least 5 times smaller than the ADC noise as shown in Equation 6.

$$\text{Total ADC Noise (rms)} = \frac{AVREF}{2\sqrt{2}} \times 10^{-\frac{SNR_{ADC}}{20}} \tag{5}$$

$$\text{Allowed VREF Noise (rms)} \leq \frac{\text{Total ADC Noise}}{5} \tag{6}$$

In a voltage reference data sheet, noise is represented as flicker noise and wideband noise.

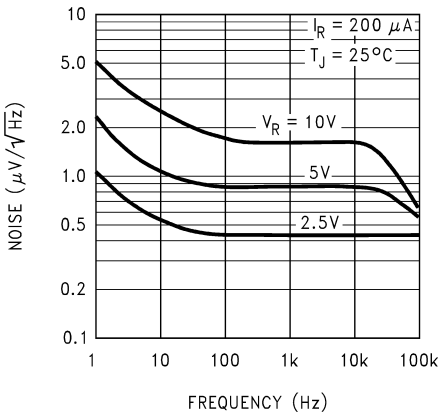

Figure 6-1. LM4050 Noise Voltage vs Frequency

In Figure 6-1 the frequency domain plot is given from 1Hz to the complete frequency range. In this plot the noise level k = 432nV/√(Hz) and a corner frequency Fc = 65Hz. Also the lower limit for flicker noise (FL) = 0.1Hz and the higher frequency limit (FH) is 10Hz. With this information the RMS flicker noise can be calculated as...

$$\frac{1}{f}\,\text{Noise}(\text{rms}) = k * \sqrt{Fc} * \sqrt{\ln\left(\frac{FH}{FL}\right) + (FH - FL)} \tag{7}$$

An alternative view of flicker noise is presented in Figure 6-2 and wideband noise is shown in Figure 6-3.

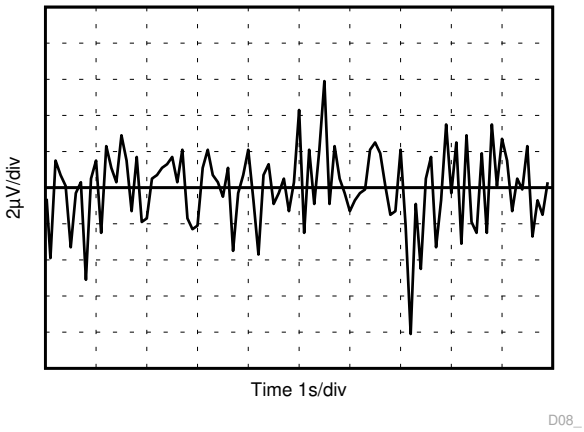

Figure 6-2. REF3425 0.1Hz to 10Hz Noise

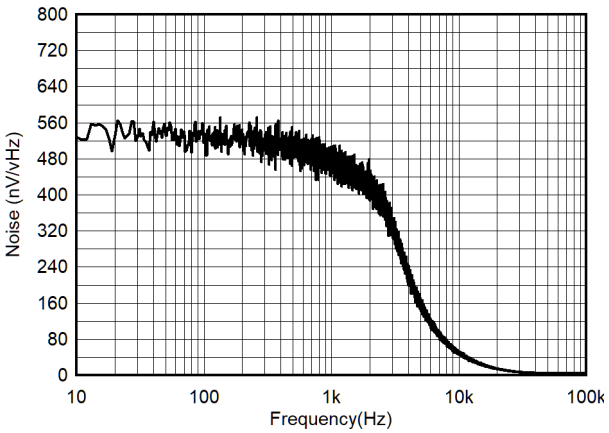

Figure 6-3. REF3425 Noise Performance 10Hz to 100kHz

In this case flicker noise is calculated in Equation 8.

$$\frac{1}{f}\,\text{Noise}(\text{rms}) = \frac{V_{P-P}}{6.6} \tag{8}$$

Flicker noise can't be filtered out. Hence allowed wideband noise will be calculated based on the ADC SNR requirement. Equation 9 shows how to find the wideband noise limit because the flicker noise cannot be filtered out.

$$\text{Wideband VREF Noise}(\text{Nw}) = \sqrt{\left(\frac{1}{f}\,\text{VREF Noise}\right) - (\text{Allowed VREF Noise})} \tag{9}$$

If allowed wide band noise is more than total wide band noise of the reference than we need to filter out the extra wide band noise component. Equation 10 shows how to calculate the cut off frequency.

$$\text{Allowed Frequency} = \left(\frac{\text{Wideband noise (rms)}}{\text{Nw}}\right)^2 \quad (10)$$

7 Dynamic Error (Voltage Reference Driving Capability)

SAR ADC logic first samples input before starting digital conversion. After that it samples VREF at appropriate cap for every bit conversion. Hence a charge re-distribution takes place on every bit conversion on reference pin of the ADC. The magnitude of peak current is proportional to the clock frequency of the data converter. MSB conversion requires maximum charge at the cap and LSB requires minimum charge. Hence current varies from MSB to LSB conversion. This current variation will change the output according to its output impedance. This variation gets translated into non- linear error.

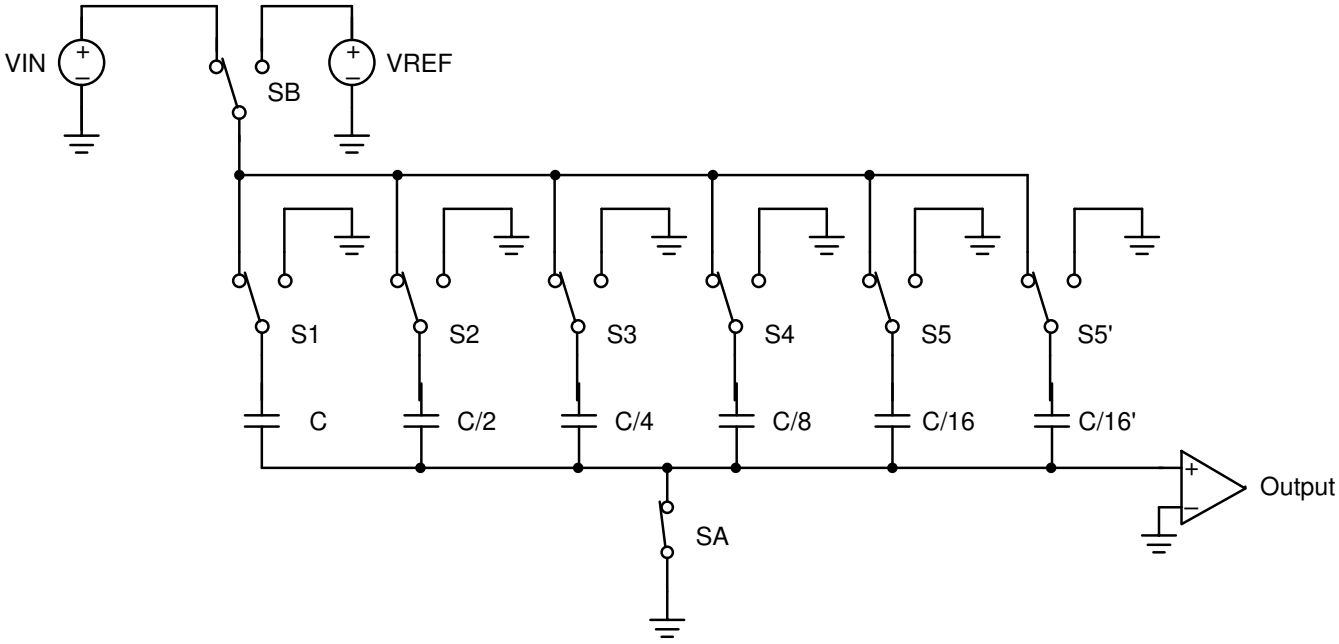

Figure 7-1. SAR ADC Sampling Architecture

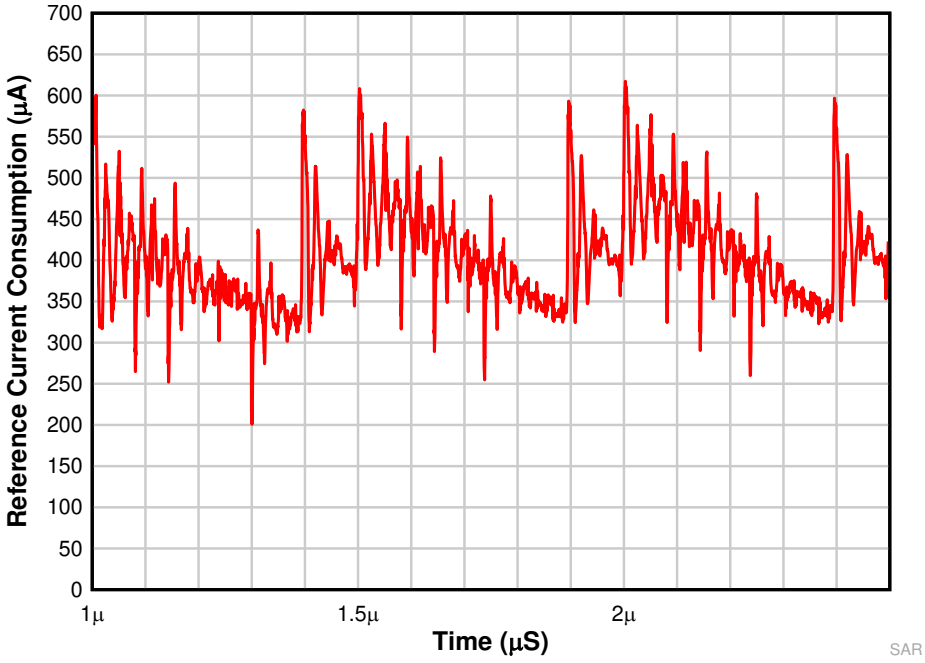

Figure 7-2. SAR ADC VREF Current Consumption

Figure 7-2 shows plot for transient current at 12 bit TI SAR AD7049 at AVDD (Reference pin) for 1V input when REF3433-Q1 is used as reference and sampling (CS) frequency is 2 MHz and 64-MHz Clock frequency. The load cap at reference pin is 10 µF. The current is measured by measuring drop across 500 Ω placed between reference pin of ADC and REF3433Q.

Time period for each conversion is 0.5 µs. The data conversion takes place from 3rd clock to 14th clock from MSB to LSB (which is first half of one cycle){reference – ADC data sheet}.Each clock during the conversion is giving current spike due to charge redistribution. We can see that current spike is nonlinear varying from MSB to LSB. Max current taken by reference pin SAR ADC during conversion is 600 µA for 1-V input. This current varies with input magnitude. This leads to a nonlinear variation in the output of the reference device which introduces harmonic distortion in the ADC output as the *Voltage-reference impact on total harmonic distortion white paper* shows.

To increase switching load driving capability, a capacitor must be placed very near to reference pin of SAR ADC. Stability of the reference must also be considered while selecting the cap.

If the current demand is very high (in case a reference is driving more than one ADC), a low noise buffer at the output can be used with it.

The other care about is the trace resistance from output pin of shunt reference to the reference pin of ADC. Max voltage drop across trace must be much less than LSB/2 . Voltage drop across the trace will be = Rtrace × Imax. This will directly get added to the load regulation error. One needs to also minimize trace lengths to reduce the trace inductance. To minimize this error the reference must be placed very close to the VREF pin of the ADC. If the reference has VOUT sense pin then problem of trace resistance can be eliminated by connecting output sense pin to reference pin of ADC.

8 References

- Texas Instruments, *TI Precision Labs - ADCs*
- Texas Instruments, *Voltage-reference impact on total harmonic distortion white paper*
- Texas Instruments, *Voltage reference selection basics white paper*
- Texas Instruments, *Choosing the Voltage Reference for Your Automotive Application - Application Brief*
- Texas Instruments, *Tips and tricks for designing with voltage references E-book*

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2018) to Revision A (March 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	2
• Added REF70 to table 2-1	2
• Added ADC and DAC recommendations to table 2-1	2
• Updated noise example	8

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