Application Report

Designing With the MSP430FR4xx and MSP430FR2xx ADC

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ABSTRACT

Designing an application with the analog-to-digital converter (ADC) requires several considerations to optimize for power and performance. This application report discusses the basics of how a designer should analyze a data sheet and user's guide to properly design an application. It discusses the fundamentals of how to optimize a design based on the external requirements and available ADC configurations. The goal is to consider various ADC parameters before writing a single line of code. This helps avoiding any unnecessary design changes later in the development process.

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Trademarks

1 Overview of the MSP430FR4xx and MSP430FR2xx ADC Module

The ADC module of the MSP430FR4xx and MSP430FR2xx microcontrollers (MCUs) supports fast 10-bit or 12-bit analog-to-digital conversions. Depending on the device (see the device-specific data sheet for details), the module implements a 10-bit or 12-bit SAR core together with sample select control and a window comparator. The ADC IP described here is called the FR2xx/FR4xx ADC to distinguish it from the ADC12_B module that is used in the MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx devices.

FR2xx/FR4xx ADC features include:

- Greater than 200-ksps maximum conversion rate
- Monotonic 10-bit or 12-bit converter with no missing codes
- Sample-and-hold with programmable sampling periods controlled by software or timers
- Conversion initiation by software or different timers
- Software-selectable on-chip reference or external reference
- Twelve individually configurable external input channels
- Conversion channel for on-chip temperature sensor
- Selectable conversion clock source
- Single-channel, repeat-single-channel, sequence, and repeat-sequence conversion modes
- Window comparator for low-power monitoring of input signals
- Interrupt vector register for fast decoding of six ADC interrupts

2 Comparison Between the FR2xx/FR4xx ADC and ADC12_B

2.1 Outline of ADC12_B

In the MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx MCUs, The ADC12_B module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, and up to 32 independent conversion-and-control buffers (ADC12MEM0 to ADC12MEM31). The conversion-and-control buffer allows up to 32 independent analog-to-digital converter (ADC) samples to be converted and stored without any CPU intervention.

ADC12_B supports 8 differential or 16 single-ended external inputs. ADC12_B has a dedicated memory control register for each input channel. This allows the user to set unique properties such as voltage reference input and provides a separate memory buffer for each channel of the ADC. For the ADC12_B on the FR59xx, 32 such memory control registers (ADC12MCTL0 to ADC12MCTL31) are provided. When a group of channels is sampled, the conversions results are stored sequentially and can be read after all the channels have completed sampling.

2.2 Outline of FR2xx/FR4xx ADC

In the MSP430FR4xx and MSP430FR2xx MCUs, a single-ended external analog input is selected by the analog input multiplexer from 12 external and 4 internal analog signals. The 1.2-V VREF can be output to a device-specific external channel. The on-chip temperature sensor can be internally connected to channel A12. The 1.5-V VREF can be internally connected to channel A13.

In both the FR2xx/FR4xx ADC and the ADC12_B, 8-, 10-, or 12-bit resolution can be selected. In the FR2xx/FR4xx ADC module, the ADCCTL2.ADCRES bit field is used, and the default setting is 10 bit. In the ADC12_B module, the ADC12CTL2.ADC12RES bit field is used, and the default setting is 12 bit.

In MSP430FR4xx and MSP430FR2xx MCUs, the DMA is not supported. In MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx MCUs, the DMA is supported in the ADC12_B.

In MSP430FR4xx and MSP430FR2xx MCUs, the interrupt vector register ADCIV has six interrupt flag sources including three from the window comparator function. More ADC12_B interrupts are handled using the ADC12IV.

For the ADC clock source and sampling rate, MODOSC, ACLK, MCLK and SMCLK can be set as ADC clock. The conversion time can be calculated in (resolution bits + 2) × $1/f_{ADCCLK}$. The sampling time can be set by ADCSHTx.ADCCTL0 to 4, 8, 16, and up to 1024 ADC clock cycles. The sampling time should be equal or larger than the minimum sampling time specified in MSP430FR4xx or MSP430FR2xx device-specific data sheet. This value is related to the equivalent internal and external resistance and capacitance, resolution, and voltage.

2.3 FR2xx/FR4xx ADC Pin Selection and Board Design

In the MSP430FR413x and MSP430FR203x MCUs, the ADC pin selection is set in the SYSCFG2 register. For other FR4xx MCUs, the ADC pin selection is set in the PxSEL0 and PxSEL1 registers. Because there is only one pair of power supply pins (DVCC and DVSS) in FR4xx MCUs, to achieve good ADC performance, board design should avoid system noise:

- Place decoupling capacitors as close as possible to DVCC.
- Select the reference voltage carefully.
- Do not layout high-frequency toggled digital signals close to power lines or ADC input signals.
- Do not toggle I/O pins while the ADC is working.
- Find more design guidance for the ADC on www.ti.com.

2.4 Key Parameters Comparison

Table 2-1 lists the key timing and linearity parameters to compare a few products with the FR2xx/FR4xx ADC and the ADC12_B. For more details, see the device-specific data sheet.

Table 2-1. Parameter Comparison

Parameter	Description	Condition	Device		
			MSP430FR2355	MSP430FR2311	MSP430FR58xx
			FR2xx/FR4xx ADC 12-Bit Mode	FR2xx/FR4xx ADC 10-Bit Configuration	ADC12_B Single-Ended Mode
f_{ADCCLK}	ADC clock frequency		4.4 MHz max	5.5 MHz max	5.4 MHz max
t_{Sample}	Sampling time	Notes	0.61 µs min(1)	2 µs min	1 µs min
$t_{CONVERT}$	Conversion time		14 × 1/f_{ADCCLK}	12 × 1/f_{ADCCLK} (3)	14 × 1/$f_{ADC12CLK}$ (2)
E_I	Integral linearity error	Veref+ reference	±2.5 LSB	±2 LSB	±2.2 LSB
E_D	Differential linearity error	Veref+ reference	±1 LSB	±1 LSB	-0.99 + 1 LSB
E_O	Offset error	Veref+ reference	±1.5 LSB	±6.5 mV	±1.5 mV
E_G	Gain error	Veref+ reference	±3 LSB	±2 LSB	±2.5 LSB
E_T	Total unadjusted error	Veref+ reference	±4 LSB	±2 LSB	±3.5 LSB

(1) The FR2355 minimum sampling time test conditions are: R_S = 1000 Ω, R_I = 4000 Ω, C_I = 5.5 pF, $C_{external}$ = 8.0 pF. Approximately 9.01 Tau (τ) are required for an error of less than ±0.5 LSB in 12-bit mode.
(2) The FR58xx minimum sampling time test conditions are: R_S = 400 Ω, R_I = 4 kΩ, C_I = 15 pF, C_{pext}= 8 pF
(3) The FR2311 minimum sampling time test conditions are: R_S = 1000 Ω, R_I = 36000 Ω, C_I = 3.5 pF. Approximately 8 Tau (τ) are required for an error of less than ±0.5 LSB.

3 Tailoring the ADC and Reference Voltages to Your Application

Each application is unique and has different reference voltage considerations. As an example, when connecting a sensor to the ADC front-end, you would need to consider the voltage dynamic range, the sensor settling time, powering and disabling the sensor when needed for an energy optimized application. After these considerations are understood, the ADC reference can be tailored for various applications through the configuration registers. Consideration areas for the reference voltage are described in the following sections.

3.1 Reference Voltages

A reference voltage is a fixed voltage that ideally should not have any temperature- or supply-dependent variations. An ADC requires a reference voltage that has a negative and positive side as a reference point for the ADC input signal. The ADC then translates the input signal to a digital value (ADC code) based on the signal relative to the reference voltage. The application code deciphers the ADC code in reference to the input signal voltage. Figure 3-1 shows a linear translation graph of a reference voltage to an ADC code.

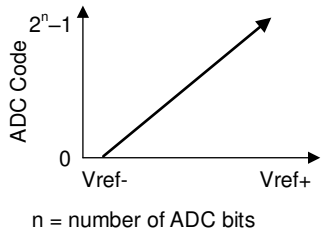


Figure 3-1. Input Signal Voltage vs ADC Code

The maximum ADC code value is calculated by (2^n – 1) where n is the number of ADC resolution bits. The positive side of the reference voltage translates to the highest ADC code. If an input signal is higher than the reference voltage, the measurement is then saturated to the maximum ADC code value. For example, if the ADC is 12 bits, the maximum ADC code is (2^{12} – 1) = 4095 injecting a voltage above the device specification into the ADC pins can cause permanent damage to the pin or the device itself. For more information, see the data sheet parameter on analog input voltage range. For measuring voltages that exceed the input range of the ADC, external circuitry can be required to adjust external voltage to the optimal ADC input range (for example, voltage dividers or amplifiers).

3.2 Internal and External Reference Voltage

All MSP430™ ADCs have integrated internal reference voltages. The ADC also allows external references to be attached if the internal reference performance is not sufficient or if an alternate reference voltage is required.

Deciding between internal and external reference needs to be determined early in the design cycle by considering the various conditions of the application. If the reference voltage is used to source multiple devices or external sensors, consider the current load. The MSP430 reference voltage output can only handle a maximum load as stated in the data sheet.

The MSP430FR215x, MSP430FR235x, MSP430FR247x, MSP430FR267x internal shared reference in the ADC module can generate three selectable 1.5 V, 2.0 V, or 2.5 V. Other FR2xx/FR4xx devices include a fixed-voltage reference. AVCC is also a selectable reference voltage. Using AVCC as a reference achieves lower power. however, it measures analog voltages radiometric to a potential imprecise and changing AVCC voltage. For some applications, this may be exactly what is desired (for example, measuring full-bridge sensors that are also powered by AVCC).

Another factor that could affect the reference voltage is the dependence on temperature. The reference voltage temperature drift is located in the device-specific data sheet. If an application is in an environment with large temperature swings and accuracy is required over the entire temperature range, evaluate if the internal reference temperature coefficient is good enough. If not, consider using one of TI's external reference solutions with a low temperature coefficient and connect use the VeREF+ input on the MSP430 device.

Another consideration between the internal and the external reference is the analog reference voltage offset. All internal references have a voltage offset that needs to be taken into consideration and TLV calibration data can be used to reduce this. However, using an external reference voltage for the ADC would have a smaller voltage

offset relative to the internal reference. The external reference may also be calibrated to obtain the closest reference voltage target. Provide some headroom when selecting the right reference voltage for the application so that the signal is not saturated during conversion or the signal attenuated.

3.3 Signal Resolution

Signal resolution determines how accurate a signal can be measured when translated into a digital value since the digital value is finite. The smaller the signal resolution, the better the signal accuracy one can capture. Signal resolution is calculated based on the ADC reference voltage and the number of ADC bits. First, determine your input signal voltage peak-to-peak. Then, select the smallest reference voltage larger than the peak voltage to be captured. This provides the finest signal resolution when calculating it in code. Signal resolution can be calculated using Equation 1.

$$\text{Signal resolution} = \frac{V_{R+} - V_{R-}}{2^n} \quad (1)$$

- n = ADC conversion resolution

Assuming VREF+ = 2.5 V, VREF- = 0 V, and n = 12 bits, the signal resolution can be calculated using Equation 2.

$$\text{Signal resolution} = \frac{2.5V}{2^{12}} = \frac{2.5V}{4096} = 610\ \mu V/\text{bit} \quad (2)$$

As an example, if your sensor output dynamic range is between 0 V to 1.8 V and you want to use the internal reference, you would select the reference voltage of 2 V. This allows the input signal to not saturate the ADC while providing the finest resolution.

Based on the signal resolution, you can calculate the ideal ADC code from the input voltage. To calculate the ADC code, assuming VREF+ is 2.5 V, 1-V input voltage, and 12-bit resolution, and Equation 3 where Equation 1 has been solved for the signal applies.

$$\text{ADC code} = \frac{\text{Input voltage}}{\text{Signal resolution}} = \frac{1V}{610\ \mu V/\text{bit}} = 1638 \quad (3)$$

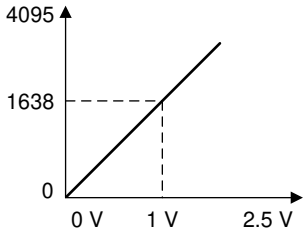


Figure 3-2. Input Signal to ADC Code

3.4 Selecting the Right Sampling and Conversion Time to Achieve the Target Conversion Rate

Sampling (sample-and-hold) time determines how long to sample a signal before digital conversion. During sample time, an internal switch allows the input capacitor to be charged. The required time to fully charge the capacitor is dependent on the external analog front-end (AFE) connected to the ADC input pin. Figure 3-3 shows a typical ADC model of an MSP430 MCU. The R_I and C_I values can be obtained from the device-specific data sheet.

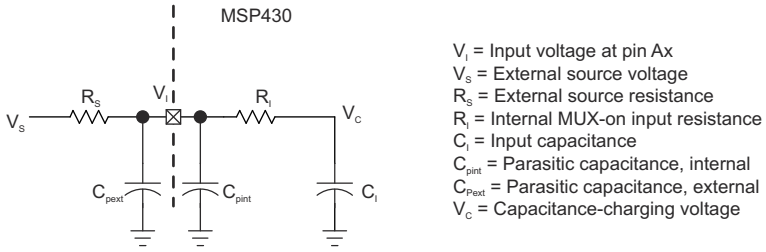


Figure 3-3. Analog Input Equivalent Circuit

It is critical to understand the AFE drive capability. If possible, model the AFE as shown in Figure 3-2. After this is known, calculate the minimum sampling time required to sample the signal. The resistance of the sources (R_S and R_I) affects t_{sample}. Equation 4 can be used to calculate a conservative value of the minimum sample time t_{sample} for an n-bit conversion.

$$t_{sample} \geq (R_S + R_I) \times \ln\left(2^{n+2}\right) \times \left(C_I + C_{pext} + C_{pint}\right) \quad (4)$$

More simple models can be adopted based on a common R_S assumption. According to the MSP430FR235x, MSP430FR215x data sheet, the sampling time of the ADC (t_{Sample}), which is the minimal value, should be calculated on (C_I + $C_{external}$) × (R_S + R_I) × Tau. The meaning of the "minimal value of sampling time" is the minimum time that is required to result in an error of less than ±0.5 LSB at the defined condition.

Table 3-1. ADC Timing Parameters of MSP430FR2355

PARAMETER		TEST CONDITIONS	DEVICE GRADE	V_{CC}	MIN	MAX	UNIT
f_{ADCCLK}	ADC clock frequency	ADC clock, 10-bit mode	T	2.4 V to 3.6 V		6.0	MHz
		ADC clock, 12-bit mode				4.4	
$t_{Settling}$	Turn-on settling time of the ADC(1)	The error in a conversion started after t_{ADCON} is less than ±0.5 LSB, Reference and input signal already settled	T			100	ns
t_{Sample}	Sampling time	R_S = 1000 Ω, R_I = 4000 Ω, C_I = 5.5 pF, $C_{external}$ = 8.0 pF, Approximately 7.62 Tau (t) are required for an error of less than ±0.5 LSB, 10-bit mode	T	2.4 V to 3.6 V	0.52		µs
		R_S = 1000 Ω, R_I = 4000 Ω, C_I = 5.5 pF, $C_{external}$ = 8.0 pF, Approximately 9.01 Tau (t) are required for an error of less than ±0.5 LSB, 12-bit mode	T	2.4 V to 3.6 V	0.61		

(1) This excludes the ADC conversion time. The ADC conversion time is specified as (N + 2) × 1/f_{ADCCLK}.

The sample-and-hold time depends on the mode (pulse sample mode or extended sample mode). The ADCSHTx bit controls the sample-and-hold time only in pulse sample mode. A timer can be used to control the sample-and-hold time in extended sample mode, providing more granular control.

Table 3-2. ADCCTL0 Register

15	14	13	12	11	10	9	8
Reserved				ADCSHTx			
r0	r0	r0	r0	rw-(0)	rw-(0)	rw-(0)	rw-(1)
7	6	5	4	3	2	1	0
ADCMSC	Reserved		ADCON	Reserved		ADCENC	ADCSC
rw-(0)	r0	r0	rw-(0)	r0	r0	rw-(0)	rw-(0)

Table 3-3. ADCCTL0 Register Description

Bit	Field	Type	Reset	Description
11-8	ADCSHTx	RW	1h(1)	ADC sample-and-hold time. These bits define the number of ADCCLK cycles in the sampling period for the ADC. Can be modified only when ADCENC = 0. Resetting ADCENC = 0 by software and changing these fields immediately shows an effect when a conversion is active. 0000b = 4 ADCCLK cycles 0001b = 8 ADCCLK cycles 0010b = 16 ADCCLK cycles 0011b = 32 ADCCLK cycles 0100b = 64 ADCCLK cycles 0101b = 96 ADCCLK cycles 0110b = 128 ADCCLK cycles 0111b = 192 ADCCLK cycles 1000b = 256 ADCCLK cycles 1001b = 384 ADCCLK cycles 1010b = 512 ADCCLK cycles 1011b = 768 ADCCLK cycles 1100b = 1024 ADCCLK cycles 1101b = 1024 ADCCLK cycles 1110b = 1024 ADCCLK cycles 1111b = 1024 ADCCLK cycles

(1) The default value for the 10-bit ADC is 0h, and the default value for the 12-bit ADC is 1h.

With the conditions of V_{CC} = 2.4 V to 3.6 V and resolution = 12 bits, the minimum ADC sampling time is Equation 5.

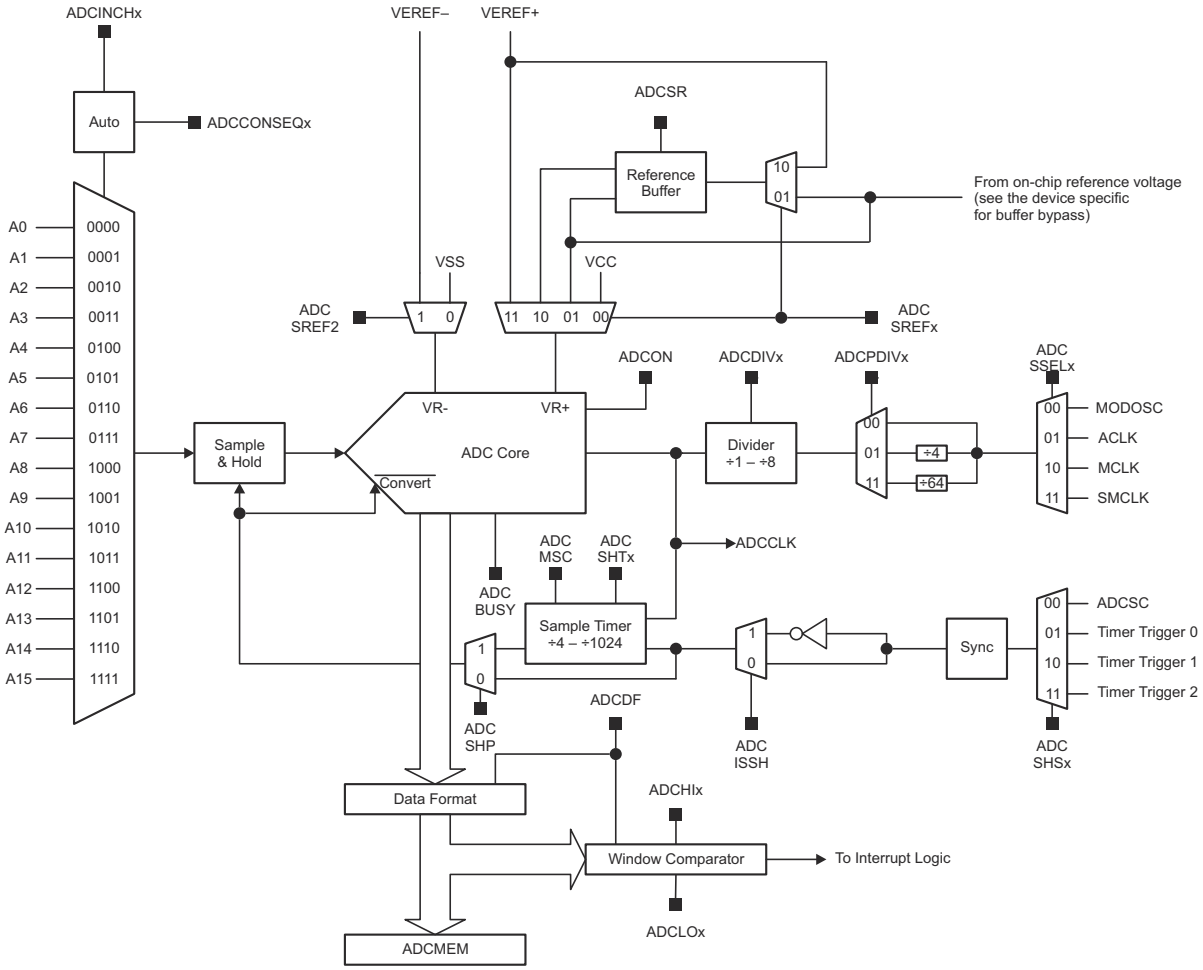
$$9.01\ (\text{Tau}) \times (1000 + 4000) \times (5.5 + 8.0) \times 10^{-12} = 0.61 \times 10^{-6}\ \text{s} = 0.61\ \mu\text{s} \quad (5)$$

In this formula, R_S = 1000 Ω and $C_{external}$ = 8.0 pF are the assumed values for the common case. 9.01 Tau, R_I = 4000 Ω, and C_I = 5.5 pF are known values from tests and calculations.

After the minimum sample-and-hold time is calculated, the appropriate settings for the ADC can be determined including selecting the correct ADC clock. The key goal is to optimize the sample-and-hold time in the application. If the sample-and-hold time is excessively longer than required, it is a waste of energy for the ADC to be operational during that time. The sample-and-hold time also limits the maximum sample rate. If your application requires a larger sample-and-hold time than the minimum, there is a tradeoff between performance and maximum sample rate.

3.5 Clock Selection

The ADC requires a clock source to convert the sampled analog input pin to an ADC code. The ADC conversion time is specified as (N + 2) × 1/f_{ADCCLK} in the device-specific data sheet. According to the MSP430FR4xx and MSP430FR2xx Family User's Guide, ADC clock can be selected from among MODOSC, ACLK, MCLK, and SMCLK as Figure 3-4 shows.



A. The MODCLK is part of the Clock System. See the Clock System chapter for more information.

B. When using ADCSHP = 0, no synchronisation of the trigger input is done.

Figure 3-4. ADC Block Diagram

The ADC clock frequency range and the MODOSC frequency are specified in the device-specific data sheet. According to the ADC timing parameters in the MSP430FR235x, MSP430FR215x data sheet, the ADC clock frequency for 12-bit mode should be less than or equal to 4.4 MHz, and the MODOSC frequency range is 3.0 to 4.6 MHz according to Table 3-4.

Table 3-4. MSP430FR2355 Module Oscillator (MODOSC) Parameters

PARAMETER		DEVICE GRADE	V_{CC}	MIN	TYP	MAX	UNIT
f_{MODOSC}	MODOSC frequency	T	3.0 V	3.0	3.8	4.6	MHz
f_{MODOSC}/dT	MODOSC frequency temperature drift(1)	T	3.0 V		0.102		%/°C
f_{MODOSC}/dV_{CC}	MODOSC frequency supply voltage drift	T	1.8 V to 3.6 V		1.17		%/V
$f_{MODOSC,DC}$	Duty cycle	T	3.0 V	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C) / (105°C – (–40°C))

The previous example is for the MSP430FR2355. If the ADC clock is set to 4 MHz with SMCLK, the ADC sample-and-hold time is set to 4 ADCCLK cycles by the ADCSHTx bits in the ADCCTL0 register. The ADC conversion time is specified as (N + 2) × $1/f_{ADCCLK}$. $t_{Settling}$ is 100 ns. Therefore, one complete ADC time would be 4 / 4 MHz + 14 / 4 MHz + 100 ns = 4.6 µs, and the ADC sample-and-hold rate is 217 ksps. If the ADC clock is set to MODOSC at approximately 3.8 MHz, the ADC sample-and-hold rate is 207 ksps, using the same calculation method.

4 Using the Window Comparator to Monitor a Signal Without CPU Intervention

The window comparator can set threshold levels and compare conversion results to the thresholds without any CPU intervention during low-power modes (LPM). The thresholds are set in LSB units and if a conversion result falls within the range of pre-set low and high threshold levels, an interrupt is triggered. Note that the same window comparator thresholds are shared among all channels, and conversion results from different channels are compared against the same threshold levels when the feature is enabled.

This feature is useful for saving power, because it allows the device to stay in a LPM until the ADC input reaches a specific threshold. All other conversion results are automatically discarded, and the CPU only wakes on threshold triggers.

5 Calibration of VREF and the Internal Temperature Sensor to Improve Performance

Calibration can be done to improve ADC performance. On-board calibration provides the best performance as it accounts for temperature drift and voltage dependencies based on the room temperature point provided by on-chip TLV data and the highest temperature point OR the lowest temperature point according to the application system level requirement, but it can require additional test time or hardware on the board to test the ADC code at high and low temperatures.

During production, measurements can be done specific to the application and those calibration values stored, and later used by the code to calibrate.

The device also contains some calibration values programmed by Texas Instruments that can be used to improve performance. These values are stored in the Device Descriptor Table (TLV). The device-specific data sheet shows the TLV calibration values available on the device and the correction equations are provided in the *Device Descriptor Table* section of the MSP430FR4xx and MSP430FR2xx Family User's Guide. To calibrate using TLV values, the code needs to implement the correction equations. The ADC has a gain factor and offset stored in TLV that is programmed on the device based on measurements using an external reference at room temperature. When the calibration equations are applied, gain and offset error are improved as well as total unadjusted error. At room temperature, gain and offset error are improved to ±0.5 LSB, and the total unadjusted error is improved to less than ±3 LSB.

6 FR2xx/FR4xx ADC Example Code and Resources

For more code examples and libraries using the FR2xx/FR4xx ADC, see the TI Cloud tools.

EnergyTrace++ technology offers an advance approach in debugging and optimizing your application power consumption by observing various aspects of the code and its power consumption. To use EnergyTrace™ technology, see the MSP430 Advanced Power Optimizations: ULP Advisor and EnergyTrace Technology application report.

For a complete online training workshop, see the MSP430FR4x/FR2x MCU Overview Workshop.

7 References

1. MSP430FR4xx and MSP430FR2xx Family User's Guide
2. MSP430FR235x,MSP430FR215x Mixed-Signal Microcontrollers data sheet
3. MSP430FR231x Mixed-Signal Microcontrollers data sheet
4. MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide
5. MSP430FR59xx, MSP430FR58xx Mixed-Signal Microcontrollers data sheet
6. Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC application report

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2019) to Revision A (August 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2

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