Enabling SPI-based flash memory expansion by using multiplexers

Field programmable gate array (FPGA) based designs need efficient memory storage to have the capacity to run a wide array of applications. Although the FPGA has internal storage, high-performance systems such as servers, Ethernet switches, SSDs, and hardware accelerators may require external memory to meet their minimum memory capacity. This external memory can be volatile or non-volatile, depending on whether the data needs to be stored when power is removed. Non-volatile memory, such as flash memory, is able to preserve data even when it is unpowered; making it ideal to store boot-up code and FPGA configuration data. The FPGA communicates to the external memory via serial peripheral interface (SPI) protocol, routed by a multiplexer (mux).

Figure 1 shows how a mux routes the SPI signal to give users multiple ways to access the flash memory, either through the FPGA or an external header. The header allows external access to the flash memory to debug boot-up code and to update other stored firmware.

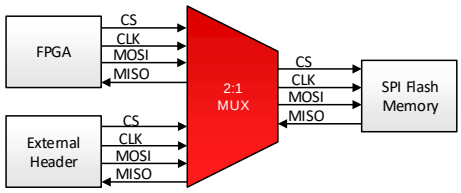

Figure 1. External access to flash memory

Figure 2 shows how the FPGA can access multiple external memories through the use of a mux for memory expansion. Although SPI protocol allows direct connection from the master to multiple slaves, the mux is essential in lowering bus capacitance and facilitating connection when there is only one master chip select bit. The bidirectional capability of the multiplexers enables the same mux to address both use-case scenarios in Figure 1 and Figure 2.

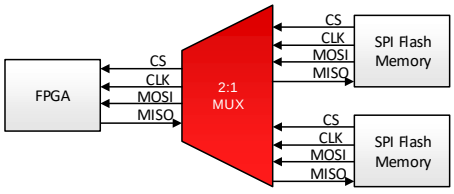

Figure 2. FPGA access to multiple flash memories

In addition to allowing an alternate path to the flash memory, powered-off protection muxes also provide isolation between the FPGA and external memory as seen in Figure 3, protecting the system from power sequencing issues. To learn more about this application, see how to eliminate power sequencing with powered-off protection signal switches.

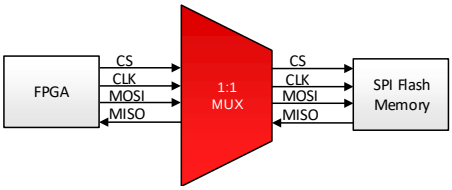

Figure 3. FPGA and external memory isolation

SPI Protocol

SPI is a synchronous serial interface used by FPGAs and MCUs to communicate to a variety of peripherals such as flash memories, sensors, ADCs, and SD cards over short distances. The SPI bus uses push-pull drivers which support higher clock frequencies (>75MHz) with lower power consumption (<1mA) compared to open drain drivers which are used for I2C or SMBus. The SPI protocol typically uses four channels (two data lines, one clock signal, and one chip select bit) compared to I2C, which uses two channels (one data lane, and one clock signal). To achieve higher throughput, quad SPI (four data lanes) and octal SPI (eight data lanes) protocols are becoming more prevalent in high-performance systems using external memories. For more information on the SPI bus, please see the Analog Engineer's Pocket Reference beginning on page 111.

Selecting the Right Mux for SPI Applications

The most critical mux parameters for SPI digital signaling are voltage, channel count, and bandwidth. To select the proper mux voltage, simply match the FPGA or MCU I/O voltage with the recommended mux I/O voltage. The mux channel count is defined by the SPI protocol; typical SPI protocol will require four channels (two data lines, one clock signal line, and one chip select line). The bandwidth is a simple way to account for the mux parasitic effects on a clock signal due to on-state capacitance (C_{ON}). For most systems, the calculation for sufficient mux bandwidth is to triple the maximum fundamental clock frequency. For example, if the maximum SPI clock signal is 75 MHz, a mux with three times the bandwidth (225 MHz) is recommended.

Recommended Mux Bandwidth = clock frequency x 3

Figure 4 shows how the SN74CBTLV3257 (200 MHz bandwidth) performs passing a 75 MHz SPI clock signal. The top waveform shows the clock signal for reference and the bottom waveform shows the output clock signal after passing through the mux. As the image shows, the parasitic mux C_{ON} slows down the clock rising and falling edges. Although this delay may not impact most SPI applications, it shows the effect that mux bandwidth can have on a SPI clock signal.

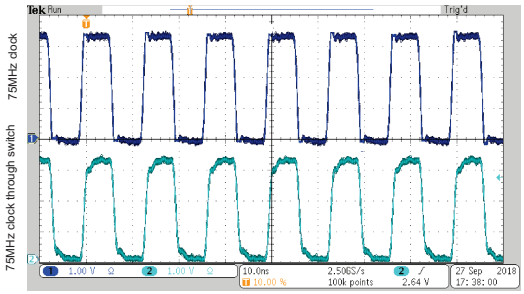

Figure 4. 75 MHz clock passing through SN74CBTLV3257

For sharper rise and fall times, the pin-to-pin TMUX1574 (2 GHz bandwidth) can be used in the same SPI application. Figure 5 shows how the TMUX1574 performs with the same 75 MHz SPI clock signal. As the bottom waveform shows, the mux has almost no impact on the output SPI clock signal. This is due to the C_{ON} that allow the 75 MHz clock signal to pass with almost no distortion. Using muxes with lower C_{ON} results in higher bandwidth which can be critical in systems where board layout or connectors add extra capacitance.

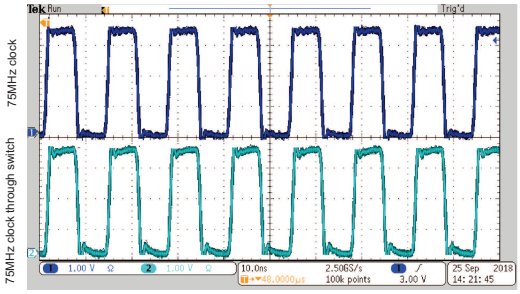

Figure 5. 75 MHz clock passing through TMUX1574

TI Solutions for SPI Muxes

In high-performance systems, FPGAs and MCUs may require external memory for expanded storage. This external memory can be non-volatile, such as flash memory, allowing data to be stored when power is lost. This functionality makes flash memories ideal to store boot-up code, FPGA configuration data, and media files. FPGAs and MCUs communicate to these flash memories via SPI protocol routed by a mux. This mux gives users multiple ways to access the flash memory, all while protecting the FPGA and MCU during power sequencing with powered-off protection. Choosing the right mux for your application will depend on the SPI protocol, signal voltage, and bandwidth requirements. To help support a wide variety of SPI applications, the TI portfolio of high-bandwidth muxes supports a wide range of signal voltages for ideal SPI performance.

Table 1. Alternative Device Recommendations

Device	Configuration	Key Features
TMUX1574	2:1, 4-channel	2GHz Bandwidth, Low Con (7.5pF), Low Ron (2Ω), Powered-off protection, 1.8V Logic Compatible
TMUX1511	1:1, 4-channel	3GHz Bandwidth, Low Con (3.3pF), Low Ron (2Ω), Powered-off protection, 1.8V Logic Compatible
SN74CB3Q3257	2:1, 4-channel	500MHz Bandwidth, Low Ron (4Ω), Powered-off protection
TS3A27518E	2:1, 6-channel	240MHz Bandwidth, Low Ron (4.4Ω), Powered-off protection, 1.8V Logic Compatible

Table 2. Adjacent Tech Notes

SLYW038	Texas Instruments Analog Engineer's Pocket Reference
SCDA015	Eliminate Power Sequencing with Powered-off Protection Signal Switches
SCAA128	Improve Stability Issues with Low C_{ON} Multiplexers
SCAA126	Simplifying Design with 1.8 V logic Muxes and Switches

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