TI TechNotes

Zero-crossover Amplifiers: Features and Benefits

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1 Introduction

Zero-crossover amplifiers employ a unique topology which eliminates the error induced by the crossover region that standard rail-to-rail amplifiers have. TI's zero-crossover topology assures high linearity across the entire common-mode voltage range and lowest distortion for precision and general applications. This tech note will explain the differences between standard rail-to-rail input and zero-crossover amplifiers.

Traditional rail-to-rail CMOS input

A traditional rail-to-rail input CMOS architecture has two differential pairs. Figure 1 highlights two differential pairs; one PMOS transistor pair (blue) and one NMOS transistor pair (red). PMOS transistors can operate in common-mode input voltages from VSS to (VDD-1.8V) and NMOS transistors can operate in common-mode input voltages from (VDD-1.8V) to VDD. The two input transistor pairs will have independent and uncorrelated input offset voltages, temperature coefficients and noise.

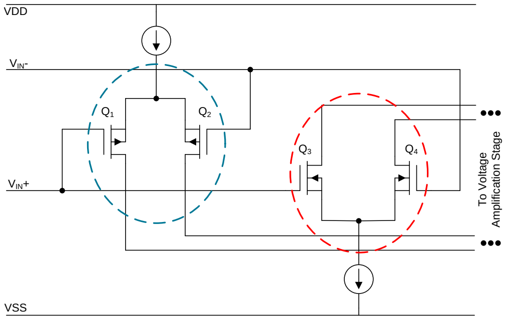

Figure 1. Simplified PMOS / NMOS Differential Pair

During the transition from the PMOS pair to the NMOS pair, and vice versa, there is a crossover region at ≈1.8V below the positive rail where both inputs are conducting (see Figure 2). Within this region, the DC input offset voltage can change – this is a source of distortion known as *input crossover distortion*. This offset error can be simulated using the TINA-TI SPICE tool (ti.com/tool/tina-ti).

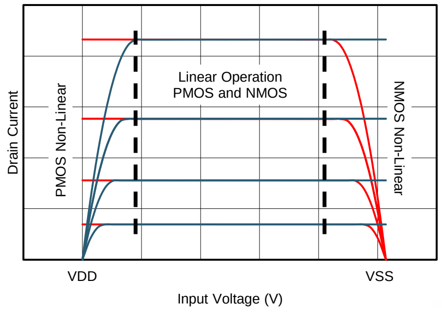

Figure 2. Transistor IV Curves

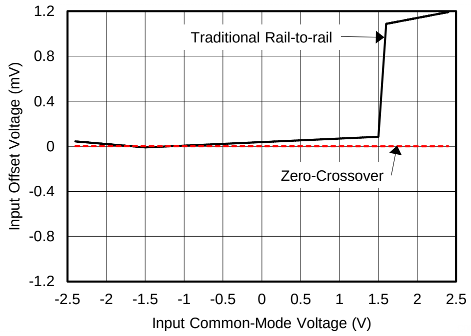

Figure 3. Simulated Crossover Performance

Figure 3 shows the simulated results of applying a [-2.4V, 2.4V] DC sweep to a traditional rail-to-rail CMOS input, buffer-configured op amp. The graph shows the *input offset voltage* abruptly shifts when the common-mode voltage is within the crossover region. If this error source is beyond the error budget, a zero-crossover amplifier will be needed.

How zero-crossover works

Zero-crossover topology uses a internal voltage charge pump to achieve linear operation with input voltages up to the rail with a single input transistor pair (PMOS or NMOS). This use of a single transistor pair allows true rail-to-rail operation without distortion over the entire input common-mode range since there is no crossover region. Zero-crossover amplifiers such as the OPA388 include an internal voltage charge pump. The charge pump boosts the input stage voltage ≈1.8V above VDD. This is enough to overcome the nonlinearity that occurs when the transistor enters triode operation at $V_{DS} < 1.8V$. Figure 4 shows a simplified representation of the charge pump topology used in zero-crossover amplifiers.

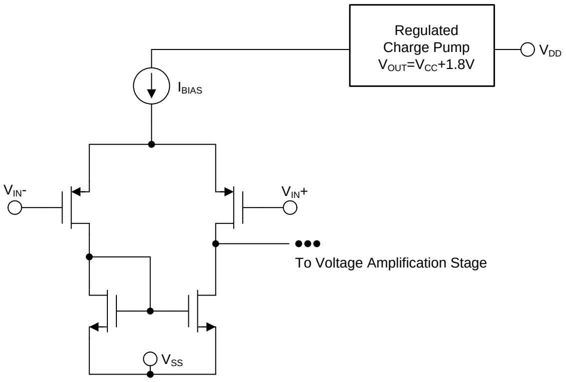

Figure 4. Simplified Zero-crossover Charge Pump Topology

Figure 3 also shows the simulated results of applying a [-2.4V, 2.4V] DC sweep on a buffer-configured OPA388. The *input offset voltage* trace in the graph shows no abrupt shift with input common-mode change because there is no crossover region. Figure 5 below contrasts the measured performance between a complementary rail-to-rail input and zero-crossover amplifier. Note the large variance in offset voltage across the input common-mode voltage.

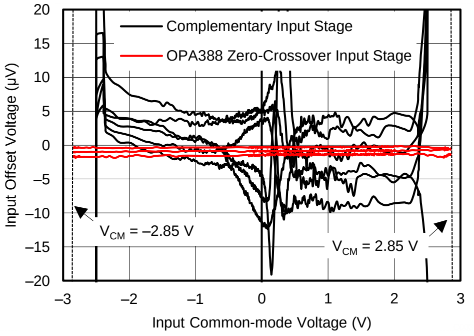

Figure 5. Measured Crossover Performance

Zero-crossover vs. rail-to-rail CMOS results

A zero-crossover and a standard rail-to-rail CMOS amplifier were used in identical, unity-gain buffer configurations. These amplifiers were both fed a pure sine wave with an amplitude of 2V ($4V_{PP}$). The outputs of these circuits were captured and the FFT was computed. Figure 6 illustrates the output voltage spectrum for the OPA388 (red) and a typical CMOS rail-to-rail amplifier (black). The output of the zero-crossover amplifier has very few spurs and harmonics compared to the typical rail-to-rail CMOS amplifier. This is the effect of eliminating the crossover region with zero-crossover topology.

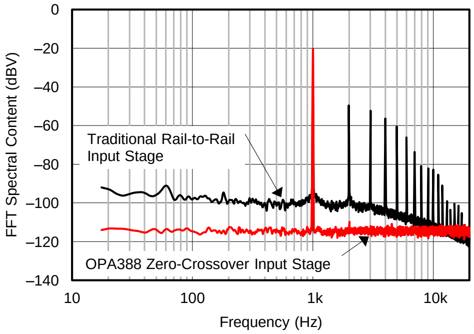

Figure 6. Buffer FFT Spectrum

Again, why zero-crossover?

Traditional rail-to-rail input CMOS op amps use two parallel differential input transistor pairs. When the common-mode is in the transition region (deadband), there is an abrupt shift in the input offset voltage which results in output voltage error and distortion. Zero-crossover op amps vastly reduce any changes in input offset voltage across the entire input common-mode range.

Additional Resources

Table 1 highlights some of TI's zero-crossover amplifiers. For a full list, see our parametric search tool results by visiting: ti.com/opamps.

Table 1. Alternative Device Recommendations

Device	Optimized Parameters
OPA388	Zero-drift, $V_{os(max)}$: 5µV, $dV_{os}/dT_{(max)}$: 0.05µV/°C, CMRR: 138dB, GBW: 10MHz, Noise: 7nV/√Hz
OPA320	$V_{os(max)}$: 150µV, CMRR: 114dB, $I_{B(max)}$: 0.9pA, 1.8V<Vs<5.5V, GBW: 20MHz, Noise: 7nV/√Hz
OPA2325	$V_{os(max)}$: 150µV, CMRR: 114dB, $I_{B(max)}$: 10pA, GBW: 10MHz, Noise: 9nV/√Hz
OPA365	$V_{os(max)}$: 200µV, CMRR: 120dB, GBW: 50MHz, Noise: 4.5nV/√Hz, Slew rate: 25V/µs, $1.8V<V_S<5.5V$
OPA322	$V_{os(max)}$: 2mV, CMRR: 100dB, GBW: 20MHz, Noise: 8.5nV/√Hz, Slew Rate: 10V/µs, $1.8V<V_S<5.5V$
OPA363/4	$V_{os(max)}$: 2.5mV, CMRR: 90dB, GBW: 7MHz, Noise: 17nV/√Hz, $I_{B(typ)}$: 1pA, $1.8V<V_S<5.5V$
OPA369	$V_{os(max)}$: 750µV, CMRR: 114dB, GBW: 12kHz, $I_{B(typ)}$: 10pA, $1.8V<V_S<5.5V$
LMV951	$V_{os(max)}$: 2.8mV, CMRR: 85dB, GBW: 2.8MHz, Noise: 25nV/√Hz, Slew Rate: 1.4V/µs, $0.9V<V_S<3V$

Table 2. Related Documentation

SBOA182	Zero-drift Amplifiers: Features and Benefits

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