

*User's Guide*

# ***J722S/TDA4VEN/TDA4AEN/AM67 Power Estimation Tool User's Guide***

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## 1 Abstract

The Excel-based tool allows users to estimate their thermal power based upon specified loadings for different components (compute cores and peripherals) of the system-on-chip (SoC). The tool allows the user to pre-populate the various fields (which components are used, and utilization of the major components) from a set of representative use cases. This gives a starting point from which a new use case can be customized to judge the power and loadings of their own use case. The tool provides a breakdown of thermal power at the junction temperature ( $T_j$ ) entered, and it also provides a table of power delivery network (PDN) currents computed for this defined use case at  $T_j = 125^\circ\text{C}$  or  $105^\circ\text{C}$ .<sup>1</sup>

The tool gives two power estimates:

### Thermal power estimate

- The time constant for heating or cooling an SoC is on the order of seconds or minutes. Because this is the primary use for the tool, the loadings should represent the average activity over a duration of seconds or minutes.

### Peak / PDN estimate

- The time constant for peak current (power) is on the order of a microsecond. Though a use case (on average) may utilize a given component for say 70%, for windows of time that component will be at 100% utilization. The tool's calculation for Peak / Power Delivery Network (PDN) estimates automatically increases the loading on key intellectual property (IP) that is enabled in order to create the PDN requirements.

## Table of Contents

<b>1 Abstract</b> .....	<b>2</b>
<b>2 Contributions to Power</b> .....	<b>3</b>
<b>3 How to Use the Tool</b> .....	<b>4</b>
3.1 Use Case.....	4
<b>4 Results Sheet</b> .....	<b>10</b>
4.1 Some Specific Pre-loaded Use Case Results.....	10
<b>5 Revision History</b> .....	<b>15</b>

## Trademarks

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<sup>1</sup> If the user selects a junction temperature less than or equal to  $105^\circ\text{C}$ , the Peak / PDN estimate is computed for  $105^\circ\text{C}$ . If the user-selected junction temperature is greater than  $105^\circ\text{C}$ , then the Peak / PDN estimate is carried out at  $125^\circ\text{C}$ .

## 2 Contributions to Power

The SoC power is typically considered to have two different components – dynamic power and leakage.<sup>2</sup>

- The dynamic power is computed based upon two numbers for the IP – max power and idle power (both scaled to the voltage). The dynamic power is computed as the weighted average of the max and idle power:  

$$P_{dyn} = P_{max} \times Utilization + P_{idle} \times (1 - Utilization)$$
  - For background: Dynamic power is typically computed as  $fCV^2$ . Consider a clock signal on a pcb that is driven from a CMOS output to a CMOS input. Dynamic power is computed based upon the (a) frequency of the signal –  $f$ ; (b) the capacitance of the input load and the pcb trace capacitance –  $C$ ; and (c) the voltage swing of the signal –  $V$ .
  - Within the tool, the user can select the frequency for some IP as well as the IP's utilization. The frequency and utilization are obviously linked; as the frequency decreases, the utilization will need to increase to maintain the same activity. Therefore, a function that requires 40% loading on an IP will have nearly the same power if the frequency is cut in half and the utilization doubles to 80%.
- The leakage power is computed based upon voltage, junction temperature, and manufacturing process variation. While the process and voltage have strong effects on the leakage power, the leakage power increases exponentially with  $T_j$ .
  - For background, a CMOS transistor is considered to have two states: (a) ON in which the channel between source and drain is conducting; and (b) OFF in which the channel is non-conductive between the source and the drain. Leakage power arises because the OFF state can allow a trickle of current to cross the channel.

<sup>2</sup> There is a third component of the SoC power – that is, analog or bias currents. These currents are not considered in this tool because in almost all cases the power contributed from these sources is negligible to the overall power.

### 3 How to Use the Tool

The tool has two pages:

1. Use Case (tab in the Excel workbook) contains many different components that the user can configure to represent their use case; the top portion of this worksheet is shown in [Figure 3-1](#). (The individual largest contributors to the power are in column E.) This sheet also contains 4 buttons that initialize different phases of the estimate.
2. Results is a blank sheet into which the results are populated.

J7225, TDA4VEN, TDA4AEN, AM67 Power Estimation Tool			Starting Use Case		Reset		Calculate		Status:	
Modifiable Field			Superset						Start Reset	
Descriptor									Done Reset	
									Load Use Case	
									Done Load Use Case	
					Populate Use Case		Save Current UC		Start Calculate	
									Done Calculate	

### Core Processor Utilization:

Processor Core Utilization (%)	
MAIN SMS 0	95%
MAIN (WKUP) R5FSS 0	95%
MAIN R5FSS 2	95%
MAIN A53SS 0: 0	91%
MAIN A53SS 0: 1	91%
MAIN A53SS 0: 2	91%
MAIN A53SS 0: 3	91%
MAIN C71SS 0: C71x	20%
MAIN C71SS 0: MMA	80%
MAIN C71SS 1: C71x	0%
MAIN C71SS 1: MMA	100%
MAIN VPAC 0	100%
MAIN DMPAC 0	61%
MAIN GPU 0	80%
MAIN Video Encoder/Decoder	100%
MCU R5FSS	95%

This block allows the user to assign a utilization to each major core IP.

- SMS 0 – Arm Cortex-M4F based Security Management Subsystem
- 3x R5F (single core) processors
- Quad-A53 MPU Subsystem
- 2x C71x DSP Subsystem that includes a Matrix Multiplication Accelerator (MMA) [up to 2TOP per subsystem]
- Vision Preprocessing Accelerator (VPAC)
- Depth and Motion Processing Accelerator (DMPAC)
- Graphics Processing Unit (GPU)
- Combination Video Encoder and Decoder

**Key IP Frequency selection:**

Key IP Frequency selection		Frequency [MHz]
MAIN PLL 15 HSDIV 0	MAIN SMS 0 Frequency [MHz]	400
MAIN PLL 15 HSDIV 2 MCU PLL 0 HSDIV 0	Domain Manager (WKUP) R5FSS 0 Frequency [MHz]	800
MAIN PLL 15 HSDIV 3	MAIN R5FSS 1 Frequency [MHz]	800
MCU PLL 0 HSDIV 3	MCU R5FSS 0 Frequency [MHz]	800
MAIN PLL 8 HSDIV 0	MAIN A53SS Frequency [MHz]	1400
MAIN PLL 7 HSDIV 0	MAIN C71SS 0 and 1 Frequency [MHz]	1000
MAIN PLL 5 HSDIV 0	MAIN VPAC 0 Frequency [MHz]	600
MAIN PLL 5 HSDIV 2	MAIN DMPAC 0 Frequency [MHz]	428
MAIN PLL 6 HSDIV 0	MAIN GPU 0 Frequency [MHz]	800
MAIN PLL 2 HSDIV 4	MAIN Video Encoder/Decoder 0 Frequency [MHz]	500
MAIN PLL 0 HSDIV 0 div 2	MAIN JPEG Encoder 0 Frequency [MHz]	250
MAIN PLL 12 HSDIV 0	LPDDR4 EMIF 0 [MT/s]	4000
MCU PLL 0 HSDIV 0	MCU SS / WKUP Modules CLK [MHz] (MCU SYSCLK)	400
MAIN PLL 0 HSDIV 0	MAIN Modules CLK [MHz] (SYSCLK)	500
MAIN PLL 15 HSDIV 0 MCU PLL 0 HSDIV 0	Device Manager Domain CLK [MHz]	400
MAIN PLL 15 HSDIV 0	HSM Domain CLK	400

This block allows the user to select the frequency for the key blocks in the core utilization block (+DDR).

**Memory Interfaces:**

Memory Interfaces	Mode	Utilization
DDRSS 0	lpddr4_4000_32	43%
GPMC / ELM	16b_133_MHz_3p3	30%

The AM67x device has a Double Data Rate (DDR) SDRAM controllers and associated physical layer interfaces (PHYs) as well as a General-Purpose Memory Controller (GPMC) with Error Location Module (ELM).

**PHYs:**

PHYs	Mode	Utilization	Instances
CSI2.0 D_PHY 4L Rx	2p5g4l	20%	4
CSI2.0 / DSI D_PHY 4L Tx	2p5g4l	27%	1
MAIN MMCSD0	hs400	25%	1
OLDI (2 Link)	oldi_dual_24b_m	100%	1

The AM67x device has several PHYs; for the PHYs with multiple instances, in addition to the mode and the utilization, the user should also select how many of the instances are used:

- 4x Camera Stream Interface (CSI) 2.0 Receive PHYs each with 4 Lanes
- CSI2.0 Transmit PHYs each with 4 Lanes
  - Display Subsystem Display Serial Interface (DSI) Transmit interface (using the CSI2.0 Tx PHY)
- Multi Media Card Interface (MMC) for eMMC only
- OLDI (Open LVDS Display Interface)

### High Speed Serial Interface:

High Speed Serial Interfaces	Mode	Utilization
<b>SerDes 0 (PCIE_3, PCIE_1, USB_0, Hyperlink_0)</b>		
Lane0	5g	30%
<b>SerDes 1 (CPSW3_0, PCIE_0, PCIE_2, n/a)</b>		
Lane0	8g	50%

There are two high speed serializing / deserializing (SerDes) interfaces on this device. Each SerDes has a single lane for which the mode, utilization, and IP should be selected.

- The IP loading (utilization) is required to be configured in the IP Utilization for High Speed IO
- Because the SerDes constantly transmits (e.g. SGMII sends /I1/ and /I2/ ordered sets when not sending data), the utilization should likely be set to 100%.

### IP Utilization for High Speed IO

IP for Complex IOs	Mode	Utilization	Instances
<b>CPSW3</b>			
1G SGMII SerDes ports	disable	0%	0
LVCMOS ports	rgmii_1000_3p3v	40%	2
<b>CSI (TX) / DSI D-PHY</b>			
CSI Tx ports	2p5g4l	27%	1
DSI Tx ports	ulps	0%	0
<b>PCIE</b>			
PCIE_0 (1 Lane)	8g	50%	1
<b>USB</b>			
3.0	5g	30%	1
2.0 (dedicated)	sleep	10%	1

The tool cannot determine the loading of the IP from the SerDes loading. Therefore, it is required that the user enter the IP loading in this table as well as entering the SerDes loading.

### Environmental:

Tj	125 C
SRAM_Voltage	0.85 V
CORE_Voltage	0.85 V
Process_Corner	strong
UC_Description	Add Test Description
UC Name	Add Test Name

The environmental section allows the user to define junction temperature (Tj), VDD\_CPU\_AVS voltage, VDD\_MCU voltage, the process corner, and a use case name and description.

- The PDN / Peak estimate will be run with Strong silicon and at either 105°C or 125°C; see Footnote 1.
- To save the use case, the user must supply a name for the use case.

## LVC MOS IOs

LVC MOS IO	Mode	Utilization	Instances
WKUP I2C	off	0%	0
WKUP UART	3p6m_1p8v	100%	1
MCU I2C	off	0%	0
MCU UART	3p6m_1p8v	100%	1
MCU McSPI	Controller_25_Mbaud_3p3v	100%	2
MCU MCAN	8mbs_3p3v	100%	2
MCU GPIO	off	0%	0
LVC MOS IO	Mode	Utilization	Instances
MAIN GPIO	off	0%	0
MAIN I2C	i2c_400k_3p3v	100%	4
MAIN UART	3p6m_1p8v	100%	7
MAIN McSPI	Controller_25_Mbaud_3p3v	100%	3
MAIN McASP	off	0%	0
MAIN ECAP	capture_in_1m_3p3v	100%	3
MAIN EPWM	off	0%	0
MAIN EQEP	off	0%	0
MAIN MCAN	8mbs_3p3v	100%	2
MAIN MMCSD1	unused	0%	0
MAIN DSS 0: DPI	Full_HD_ _1920x1080x60_fps_24b_ _3p3V	100%	1
MAIN FSS OSPI1 (QSPI)	off	0%	0
MAIN Ethernet	rgmii_1000_3p3v	40%	2

Like the PHY section, the user enters Mode, utilization, and instances for each LVC MOS.

There is only one mode and utilization allowed per IP (customization is not supported since the corresponding IP blocks do not contribute significantly to the overall power). If a system uses multiple modes for an IP type, the highest power mode should be used.

## Buttons:

						<b>Status:</b>		
Reset	Calculate					Start Reset	Done Reset	
						Load Use Case	Done Load Use Case	
						Start Calculate	Done Calculate	
Populate Use Case	Save Current UC							

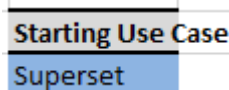
The buttons initialize different phases of the power estimation.

- Reset clears and resets the form as well as clearing Results
- Populate Use Case – It is recommended to start any power estimate by using one of the pre-configured representative use cases. This helps to highlight how the tool can be used in a reasonable way (i.e., it is usually not appropriate to enter 100% for all of the IP on the SoC).
- Calculate – once the form is completed, calculate in order to populate data into Results
- Save current UC – once the user gets a test case completed, it can be saved if a UC Name has been supplied. Once a use case is saved it will be part of the “Starting Use Case” list and be re-populated with the Populate use case button.



When each button is pushed, the cells underneath the button (H8:I11) record that it was started and then record when the step completes.

**Starting Use Case:**



This drop down selects the use case to pre-populate.

This set of use cases is supplemented when the user saves the current UC (with the buttons described above).

The pre-populated use cases are intended to provide TI-generated starting points for the customer's use case. In the final section of this user guide, some of the pre-populated use cases will be discussed.

## 4 Results Sheet

The Results sheet gives a lot of information based upon the use case entered.

Thermal power estimate:

- The primary output of the estimation is shown in cells A10 to D26; this table gives the total power of the device at various temperatures.
  - Since the leakage power is very nearly exponential, the leakage component can be interpolated between any two consecutive temperatures:  $P_{LKG} = 10^{mT_j + b}$
- Cells A1 to B8 contain reference information about the tool and the use case.
- Some users find it helpful to have the power breakdown by rail, and those results are provided in cell A30 to F77.
- Cells H42 to J79 provide information – utilization and frequencies -- on the use case estimated.
- Cells H22 to J40 show how the device's power domains<sup>3</sup> have been configured.
  - When possible, the tool powers OFF the power domain; if the user wants to keep the domain ON, it is recommended to load IP utilization within the domain at 0.1%
  - The user should configure their software to match the expectations defined in the power estimate.
- Cells H11 to I19 show a breakdown of power by block; power beyond what is accounted in this block should be treated as being present in the SoC backplane.

Peak / PDN power estimate:

- Cells M30 to R79 contain the by-rail Peak / PDN estimate; this estimate is derived from the entered use case.
  - Column U creates a label V\_G1 through V\_G18 (i.e. voltage group). These are just labels and can be modified by the user.
  - The same labels are present in cells N8 to N16; if the user modifies the labels in column U, the labels should also be modified in this range. Cells O2 to O19 sum the current for this voltage group.

### 4.1 Some Specific Pre-loaded Use Case Results

The three use cases below are intended to span the expected range of thermal power for this device; it is possible for a use case to fall outside of this range. (And the Peak / PDN power will certainly fall outside of this range.)

**Table 4-1. 125°C Thermal Power**

Use Case	Leakage [mW]	Dynamic [mW]	Total [mW]
ARM only	1650	2204	3454
3MP_FrontCamera	2785	4957	7342
Superset	3690	8479	11769

**Table 4-2. 105°C Thermal Power**

Use Case	Leakage [mW]	Dynamic [mW]	Total [mW]
ARM only	965	2204	2769
3MP_FrontCamera	1615	4957	6172
Superset	2157	8479	10236

<sup>3</sup> In the Environmental section of the Use Case tab, the user selects the voltage for configurable voltage domains. Within a voltage domain (e.g. VDD\_CORE), some circuitry is placed within a power domain (e.g. C7x\_0 and MMA are within PD\_C7\_0); the power domain can break the connection to the voltage domain if-and-only-if all of the IP within the power domain is unused. Circuitry within an off power domain, do not contribute power – leakage or dynamic – to the power budget. Within the power domain, IP is controlled by a local power sleep controller (LPSC) which controls the clock and reset to the IP. IP which is not clocked does not contribute dynamic power to the overall device power but it will contribute leakage power unless it resides in an unpowered power domain.

Note that a voltage domain typically has some IP that is within a power domain and other IP that is not within a power domain.

## Comments:

- As noted, the exponential behavior of the leakage with junction temperature causes a significant decrease in leakage between 125°C and 105°C.

**4.1.1 ARM Only**

A minimum use case for this class of processors relies upon using the A53 cores and the PCIe and ethernet switch.

The device loading is shown in the following table.

**Table 4-3. ARM-only Device Configuration (0.75V, VDD\_CORE)**

Core	Frequency	Utilization
A53 CPU	1250	70%
A53 CPU	1250	70%
A53 CPU	1250	70%
A53 CPU	1250	70%
C7x	912.5	0%
MMA	912.5	0%
C7x	912.5	0%
MMA	912.5	0%
R5F	800	25%
R5F	800	25%
R5F	800	0%
Double DSS7UL + DSI + OLDI wrap	320	0%
GPU BXS4-64-256KB DUST AM67	720	0%
GPU BXS4-64-256KB Rascal AM67	720	0%
GPU BXS4-64-256KB Wrap AM67	720	0%
VPAC3L	600	0%
DMPAC	428	0%
WAVE521CL Video Codec	500	0%
CSI_RX	720	0%
CSI_RX	720	0%
CSI_RX	720	0%
CSI_RX	720	0%
CSI_TX	720	0%
CPSW3x	250	25%
PCIE_G3 4L	500	25%
USB2 Controller	125	0%
USB3P0TCx1	125	0%
LP/DDR4-32 PHY 3733	933.25	44%
EMMC 4	250	0%
EMMC 4	250	0%
EMMC 8	250	0%
GPMC_ELM	166.67	0%
SerDes 10G Common	1PLL	100%
SerDes 10G Lane	8g	100%
SerDes 10G Common	disable	0%
SerDes 10G Lane	unused	0%

The thermal power for the device is shown in the following table.

**Table 4-4. ARM-only Thermal Power**

Tj	Leakage [mW]	Dynamic [mW]	Total [mW]
125	1650	2204	3454
120	1462	2204	3266
115	1265	2204	3069
110	1109	2204	2913
105	965	2204	2769
100	845	2204	2649
95	738	2204	2542
90	634	2204	2438
85	552	2204	2356
80	483	2204	2287
75	414	2204	2218
50	199	2204	2003
25	99	2204	1903
0	57	2204	1861
-20	37	2204	1841
-40	36	2204	1840

#### 4.1.2 Superset

On the other end of the spectrum is a superset use case in which A53s, Pulsars, C71x, and MMAs, GPU, DMPAC, and VPAC are effectively used. In this example, the SerDes is also loaded.

The device loading is shown in the following table.

**Table 4-5. Superset Device Configuration (0.85V, VDD\_CORE)**

Core	Frequency	Utilization
A53 CPU	1400	91%
A53 CPU	1400	91%
A53 CPU	1400	91%
A53 CPU	1400	91%
C7x	1000	20%
MMA	1000	80%
C7x	1000	0%
MMA	1000	100%
R5F	800	95%
R5F	800	95%
R5F	800	95%
Double DSS7UL + DSI + OLDI wrap	320	76%
GPU BXS4-64-256KB DUST AM67	800	80%
GPU BXS4-64-256KB Rascal AM67	800	80%
GPU BXS4-64-256KB Wrap AM67	800	80%
VPAC3L	600	100%
DMPAC	428	61%
WAVE521CL Video Codec	500	100%
CSI_RX	720	20%
CSI_RX	720	20%
CSI_RX	720	20%
CSI_RX	720	20%
CSI_TX	720	27%

**Table 4-5. Superset Device Configuration (0.85V, VDD\_CORE) (continued)**

Core	Frequency	Utilization
CPSW3x	250	40%
PCIE_G3 4L	500	50%
USB2 Controller	125	10%
USB3P0TCx1	125	30%
LP/DDR4-32 PHY 3733	1000	48%
EMMC 4	250	0%
EMMC 4	250	0%
EMMC 8	250	25%
GPMC_ELM	166.67	0%
SerDes 10G Common	1PLL	100%
SerDes 10G Lane	5g	100%
SerDes 10G Common	1PLL	100%
SerDes 10G Lane	8g	100%

The thermal power for the device is shown in the following table.

**Table 4-6. Superset Thermal Power**

Tj [C]	Leakage Power [mW]	Dynamic Power [mW]	Total Power [mW]
125	3690	8479	11769
120	3226	8479	11305
115	2832	8479	10911
110	2469	8479	10548
105	2157	8479	10236
100	1865	8479	9944
95	1613	8479	9692
90	1401	8479	9480
85	1220	8479	9299
80	1038	8479	9117
75	892	8479	8971
50	416	8479	8495
25	195	8479	8274
0	108	8479	8187
-20	76	8479	8155
-40	56	8479	8135

#### 4.1.3 3MegaPixel Front Camera

And finally, a use case representative of the vision analytics features of the device – front camera input run through deep learning algorithms.

The device loading is shown in the following table.

**Table 4-7. Compute Device Configuration**

Core	Frequency	Utilization
A53 CPU	1250	50%
A53 CPU	1250	50%
A53 CPU	1250	50%
A53 CPU	1250	50%
C7x	912.5	50%
MMA	912.5	50%

**Table 4-7. Compute Device Configuration (continued)**

Core	Frequency	Utilization
C7x	912.5	0%
MMA	912.5	100%
R5F	800	60%
R5F	800	40%
R5F	800	40%
Double DSS7UL + DSI + OLDI wrap	320	0%
GPU BXS4-64-256KB DUST AM67	720	0%
GPU BXS4-64-256KB Rascal AM67	720	0%
GPU BXS4-64-256KB Wrap AM67	720	0%
VPAC3L	600	90%
DMPAC	300	61%
WAVE521CL Video Codec	500	50%
CSI_RX	720	25%
CSI_RX	720	0%
CSI_RX	720	0%
CSI_RX	720	0%
CSI_TX	720	25%
CPSW3x	250	25%
PCIE_G3 4L	500	0%
USB2 Controller	125	0%
USB3P0TCx1	125	0%
LP/DDR4-32 PHY 3733	933.25	100%
EMMC 4	250	0%
EMMC 4	250	0%
EMMC 8	250	26%
GPMC_ELM	166.67	0%
SerDes 10G Common	disable	0%
SerDes 10G Lane	unused	0%
SerDes 10G Common	disable	0%
SerDes 10G Lane	unused	0%

The thermal power for the device is shown in the following table.

**Table 4-8. Compute Thermal Power**

Tj [C]	Leakage Power [mW]	Dynamic Power [mW]	Total Power [mW]
125	2785	4957	7342
120	2442	4957	6999
115	2129	4957	6686
110	1867	4957	6424
105	1615	4957	6172
100	1403	4957	5960
95	1231	4957	5788
90	1060	4957	5617
85	909	4957	5466
80	784	4957	5341
75	668	4957	5225
50	311	4957	4868

**Table 4-8. Compute Thermal Power (continued)**

T <sub>J</sub> [C]	Leakage Power [mW]	Dynamic Power [mW]	Total Power [mW]
25	144	4957	4701
0	78	4957	4635
-20	57	4957	4614
-40	46	4957	4603

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2024	*	Initial Release

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