Design Guide: TIDA-011008

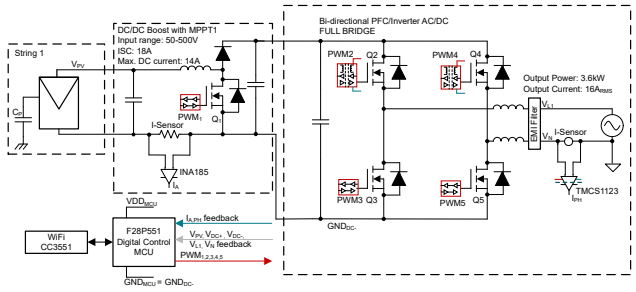
3.6kW, GaN-Based Single-Phase String Inverter Reference Design

Description

This reference design provides an overview into the implementation of a GaN-based single-phase string inverter. The design consists of one string input, able to handle up to 10 photovoltaic (PV) panels in series. The nominal rated power from string inputs to a single-phase grid connection at 230V is up to 3.6kW. Digital control of the three power stages is executed on a single C2000™ MCU. This board also features a WiFi® communication port to enable easy and remote monitor and control access.

Resources

TIDA-011008	Design Folder
LMG3660R025	Product Folder
TMCS1123	Product Folder
CC3551E	Product Folder
INA185	Product Folder
ISOTMP35	Product Folder
TMS320F28P551SG	Product Folder



Features

- Power stage with high power density makes solar inverters lighter and easier to install
- High switching frequency of 100kHz and high-efficiency design
- Cost-optimized with MCU GND referenced to V_{DC-}, allows use of non-isolated drive on all GaN devices connected to V_{DC-}
- Cost-optimized full-bridge topology: Implements an H-bridge bipolar modulation scheme to maintain low control complexity and robust grid injection
- Excellent power quality: Achieves less than 1.23% current THD with a grid emulator under high load conditions
- Wireless connectivity: Features the SimpleLink™ dual-band wireless MCU (CC3551E) for integrated Wi-Fi 6 and BLE communication

Applications

- String Inverter
- Power conversion system (PCS)

1 System Description

As the demand for residential solar power continues to rise, single-phase string inverters serve as a critical bridge facilitating clean energy delivery to the grid. Traditional silicon or IGBT designs hit efficiency and density bottlenecks due to limited switching speeds, requiring oversized magnetic filters and heavy thermal management. This reference design addresses these market challenges by deploying Gallium Nitride (GaN) power transistors. Running the system at a high frequency of 100kHz reduces total system bill of materials (BOM) cost by reducing the footprint of the filtering elements.

The system hardware layout is partitioned into a single localized board measuring 205mm × 205mm, which accommodates both distinct conversion stages:

DC/DC Stage: Single-channel PV input with a boost converter implementing maximum power point tracking (MPPT)

DC/AC Stage: 3.6kW Full-Bridge inverter running a bipolar modulation scheme

All the control, sampling and communication are done on a powerful but cost-effective MCU TMS320F28P551.

1.1 Key System Specifications

Table 1-1. Specifications

PARAMETERS	SPECIFICATIONS
PV Input Voltage Range	50V to 500V (up to 10 panels per string)
Max PV Short Circuit Current	18A
Maximum | Nominal DC Link Voltage	520V | 400V
Rated AC Output Voltage | Current	$230V_{RMS}$ | $16A_{RMS}$
Rated AC Output Power	3.6kW
Switching Frequency	100kHz
Frequency	50Hz – 60Hz
Ambient Temperature	–40°C to +60°C
Reference Design Dimensions	205mm × 205mm × 85mm (45mm without heatsink)

CAUTION

Do not leave the design powered when unattended.

WARNING

High voltage! *Accessible high voltages are present on the board.* Electric shock is possible. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property. For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

TI considers the user's responsibility to confirm that the voltages and isolation requirements are identified and understood before energizing the board or simulation. *When energized, do not touch the design or components connected to the design*.

WARNING

Hot surface! Contact can cause burns. Do not touch!

Some components can reach high temperatures > 55°C when the board is powered on. Do not touch the board at any point during operation or immediately after operating, as high temperatures can be present.

WARNING

TI intends this reference design to be operated in a ***lab environment only and does not consider the design as a finished product*** for general consumer use. The design is intended to be run at ambient room temperature and is not tested for operation under other ambient temperatures.

TI intends this reference design to be used only by ***qualified engineers and technicians*** familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

There are ***accessible high voltages present on the board*** . The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

2 System Overview

2.1 Block Diagram

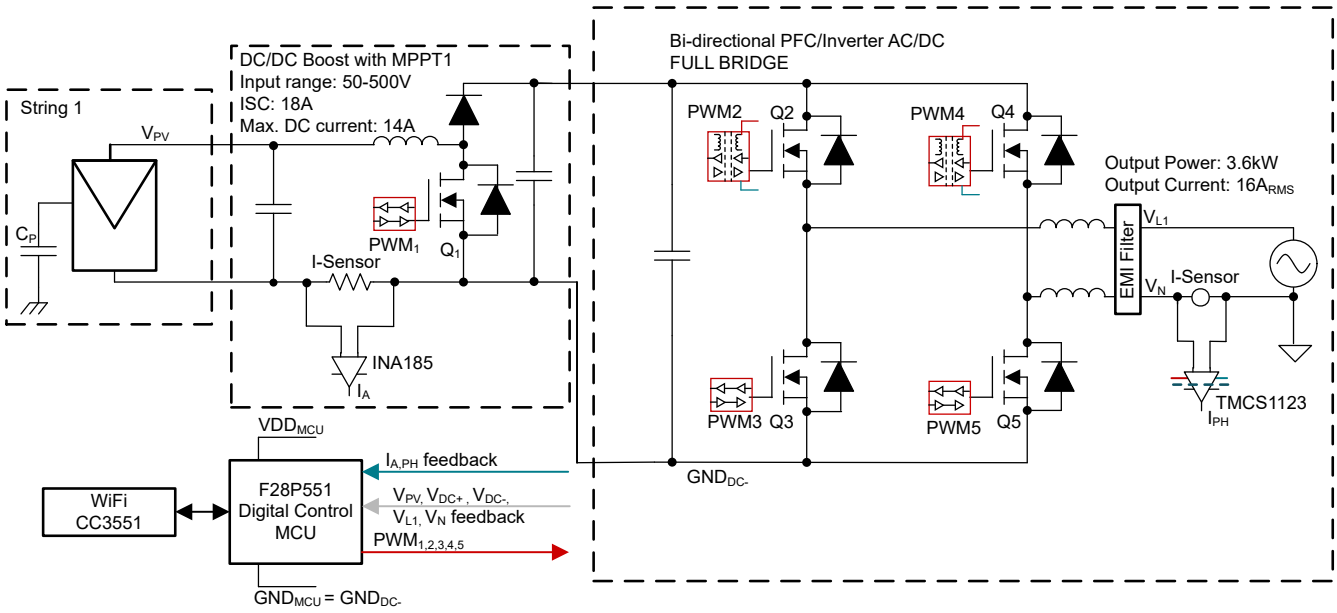


Figure 2-1. Block Diagram of the Reference Design

The board does not include any auxiliary power supply able to convert the power from HV down to 12V. An external bias power supply is required to run the board.

This topology is a good choice for transformer-less string inverter applications where there is no isolation available between the AC grid and the PV panels. The common-mode currents are a well-known challenge in PV applications due to PV surfaces exposed over grounded roof or other surfaces in the proximity. The large surface areas can lead to high values of stray capacitance between the PV panel and ground, which can go as high as 200nF / kWp in damp environments or on rainy days, as seen in Figure 2-2. This parasitic capacitance can cause high common-mode current flowing into the system when common-mode voltage of the converters is not well mitigated and can lead to EMI and issues such as grid current distortion.

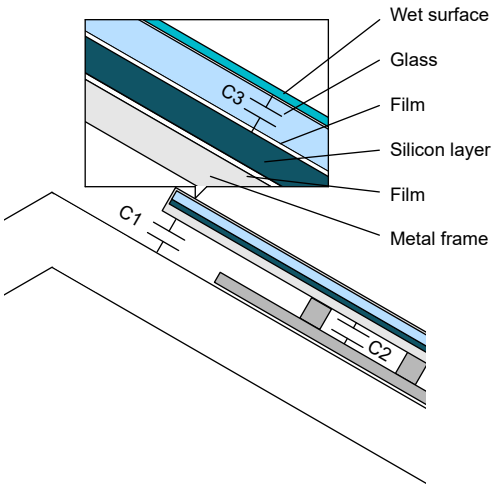


Figure 2-2. PV Panel Parasitic Capacitance

Microinverters containing transformers present high impedance return path for current, however, that is not the same case with cost-sensitive applications such as string inverters. String inverters usually present low impedance paths for return currents, hence leading to very high values of currents as shown in Figure 2-3.

The leakage currents to the ground thus constitute an important issue in transformer-less concepts. Special single-phase transformer-less topologies with reduced oscillations can be implemented for such purposes and is later discussed. In addition, the introduction of frame-less panels further contributed to the reduction of such problems.

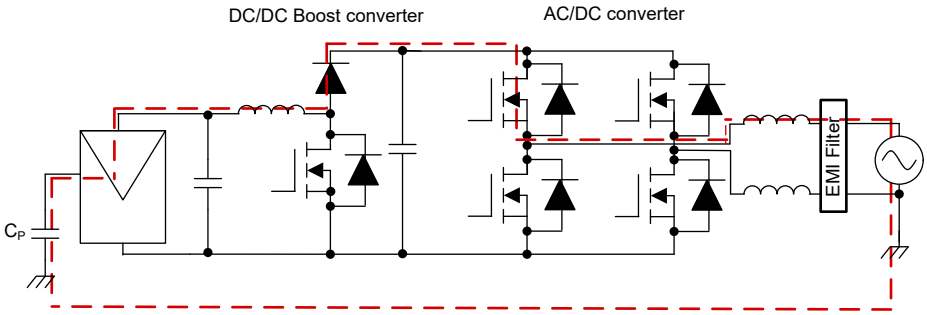


Figure 2-3. Common-Mode Noise

This DC/AC converter stage is operated at a high switching frequency for sinusoidal grid current control, thus allowing the EMI filter design to be compact. With the single-phase $230V_{RMS}$ grid, an output power of 3.6kW can be achieved with an output current of $16A_{RMS}$. The EMI filter is composed of a boost inductor split between both rails for better common-mode rejection capability, two common-mode chokes, C_x capacitors, and C_y capacitors. The EMI filter has been designed to attenuate both the differential-mode and common-mode noise injected into the grid. Additionally, electrolytic capacitors are present at the DC- link to compensate for the 100Hz power ripple present in such single-phase applications. Note that both of the half-bridges need to have a dead-time to avoid shoot-through. The current in the grid is measured and then controlled by the MCU using Proportional Resonant (PR) controllers. High-accuracy measurement of the current flowing in the Point of Common Coupling (PCC) is required to control active and reactive power. The current control requires the implementation of a Phase Locked Loop (PLL) which is synchronized with the grid voltage frequency. A DC-link voltage control loop is used to control the amplitude of the active current sink or source from the grid.

2.2 DC/DC Boost Converter

The variable low-voltage input coming from the PV solar string (50V-500V) must be boosted to a stable, regulated intermediate 400V DC-link bus. This step is managed via a non-synchronized boost stage driven by the C2000™ MCU.

2.2.1 Boost Inductor Design

In any power converter design, the inductor design is the most important part. The four important characteristics pertaining to the inductor design are namely the inductance value, ripple current, saturation current, and the DC resistance (DCR).

The lower the inductor value, the smaller the design size. Note that the inductor must always have a higher current rating than the maximum current calculated including the ripple current.

For a boost inductor used in solar application, following equation can be used as a starter:

$$L \geq \frac{V_{IN}*(V_{OUT} - V_{IN})}{\Delta I_L * V_{OUT} * f_{sw}} \quad (1)$$

Where:

- V_{IN} is the
- ΔI_L is the ripple current, normally is the 0.2 to 0.4 times of the nominal input current
- V_{out} is the output voltage
- f_{sw} is the switching frequency

2.2.2 Rectifier Diode Selection

SiC schottky diodes can be used to reduce system losses and improve efficiency. The conduction loss of the diode can be calculated, where I_F is the average forward current:

$$P_{DC} = I_F * V_F \quad (2)$$

The switching loss can be calculated as:

$$P_{SW} = 0.5 * I_{PK} * V_R * t_{rr} * f_{sw} = Q_r * V_R * f_{sw} \quad (3)$$

Where:

- I_{PK} is peak reverse current
- V_R is the reverse voltage in a steady state
- t_{rr} is the reverse recovery time
- f_{sw} is the switching frequency
- Q_{rr} is recovered charge

Total losses on rectifier diode can be calculated as:

$$P_D = P_{DC} + P_{SW} \quad (4)$$

2.2.3 Boost Cooling Concept

To optimize thermal performance and power density, a specialized hybrid cooling concept is used:

- The GaN FETs utilize a top-side cooled architecture. The GaN FETs couple directly to the aluminum heatsink through a thin 1mm thermal interface material (TIM), minimizing case-to-heatsink thermal resistance.
- The Silicon Carbide (SiC) power diodes use a bottom-side cooled configuration. They transfer heat through the PCB layer via copper thermal vias down to a 3mm TIM block before interfacing with the shared heatsink.

2.2.4 MPPT Operation

The power output from a PV panel depends on a few parameters, such as the irradiation received by the panel, panel voltage, panel temperature, and so forth. Correspondingly, the power output from a string of PV panels, depends on the individual conditions of the PV panels. The power output also varies continuously throughout the day as the conditions affecting the change. Figure 2-4 shows the I-V curve and the P-V curve of a single solar panel. The I-V curve represents the relationship between the panel output current and the output voltage. As the I-V curve in the figure shows, the panel current is at the maximum when the terminals are shorted and is at the lowest when the terminals are open and unloaded.

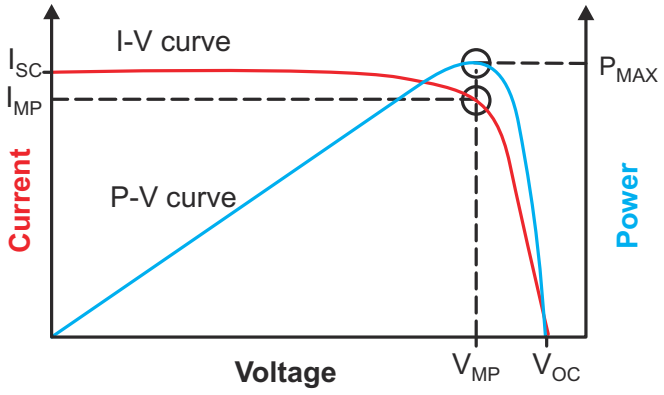


Figure 2-4. Solar Panel Characteristics I-V and P-V Curves

As shown, the maximum power obtained from the panel represented as P_{MAX} at a point when the product of the panel voltage and the panel current is at the maximum. This point is designated as the maximum power point (MPP). Figure 2-5 and Figure 2-6 show examples of how each of the various parameters affect the output power from the solar panel. The graphs also show the variation in the power output of a solar panel as a function

of irradiance. Observe in these graphs how the power output from a solar panel increases with the increase in irradiance and decreases with a decrease in irradiance. Also note that the panel voltage at which the MPP occurs also shifts with the change in irradiance. Similar concept can also be applied to a string inverter where the overall string voltage is monitored in addition to the string output current.

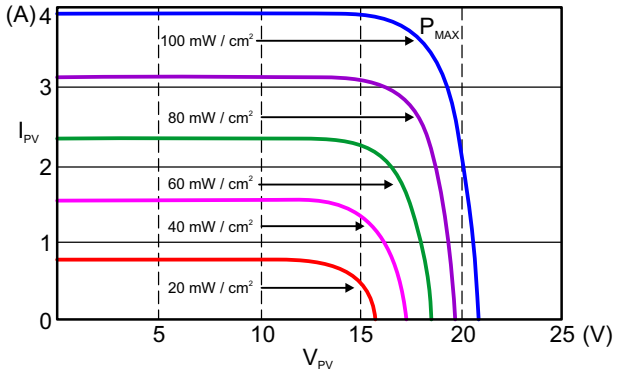


Figure 2-5. Solar Panel Output Power Variation Under Different Irradiation Conditions Graph A

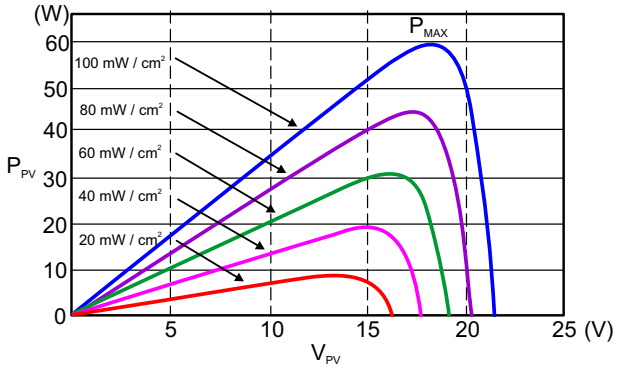


Figure 2-6. Solar Panel Output Power Variation Under Different Irradiation Conditions Graph B

The challenge of automatically identifying the MPP of the panel is typically performed by employing MPPT algorithms in the system. The MPPT algorithm tries to operate the string at the maximum power point and uses a switching power stage to supply the load with the power extracted from the panel. Perturb and Observe (PO) is one of the most popular MPPT algorithms used. The fundamental principle behind this algorithm is simple and easy to implement in a microcontroller based system. The process involves slightly increasing or decreasing (perturbing) the operating voltage of a panel. Perturbing the string voltage is accomplished by changing the duty cycle of the converter. Assuming that the string voltage has been slightly increased and that this leads to an increase in the panel power, then another perturbation in the same direction is performed. If the increase in the string voltage decreases the panel power, then a perturbation in the negative direction is done to slightly lower the string voltage. By performing the perturbations and observing the power output, the system begins to operate close to the MPP of the string with slight oscillations around the MPP. The size of the perturbations determines how close the system is operating to the MPP. Occasionally this algorithm can become stuck in the local maxima instead of the global maxims, but this problem can be solved with minor tweaks to the algorithm. The PO algorithm is easy to implement and effective, and was chosen for this design.

2.3 DC/AC Converter

The full bridge inverter translates the 400V DC-link voltage into an 230VRMS sinusoidal line output. This design opts for an H-Bridge Bipolar modulation scheme. While bipolar switching experiences higher voltage swings across the switching node compared to unipolar alternatives, it eliminates high-frequency common-mode voltages. This feature eliminates leakage currents passing through the parasitic capacitance of solar frames to ground without requiring transformer isolation.

2.3.1 Inverter Inductor Design

The inductor plays an important role in system efficiency, current ripple and overall size. The inductance value can be calculated as:

$$L \geq \frac{V_{DCBus}}{2 * \Delta I_{Lpk-pk} * f_{sw}} \quad (5)$$

Where:

- V_{DCBus} is the DC link voltage
- ΔI_{Lpk-pk} is the peak to peak ripple current
- f_{sw} is the switching frequency

Normally the peak to peak ripple current is less than 40% of the average inductor current of maximum output current. A smaller ripple current reduces the core losses in the inductor and EMI issue but need higher inductance. A bigger ripple current allows for smaller inductance and enables smaller inductor size and weight. Make sure the peak current does not exceed the inductor's saturation current.

Normally, in grid tied non-isolated inverter design, the inductor is split into two pieces, one installed on the live line, one installed on the neutral line. Each one is half the L value calculated. In this way, the common-mode noise can be suppressed to the maximum extent.

Figure 2-7 shows the common-mode noise spectrum simulation up to 500kHz with 100kHz switching stage. This can be seen from the graph that with split inductors on each line can reduce the common mode noise by >30dBµV.

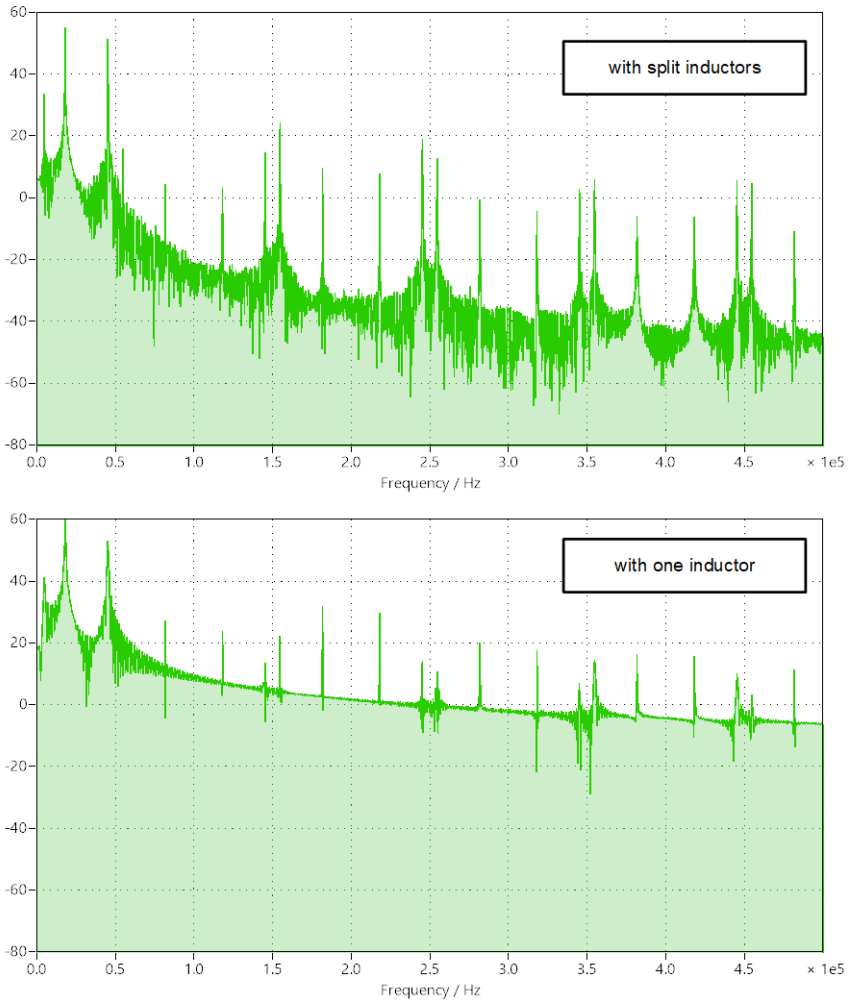


Figure 2-7. Common Mode Noise Spectrum In LISN

2.3.2 DC-Link Capacitor

DC-link capacitor is used to minimize the double line frequency voltage ripple, so the power transistor in the system does not have too much voltage stress due to voltage ripple. The DC-link capacitance can be calculated as:

$$C_{OUT} \geq \frac{P_{OUT}}{V_{DCBus} * 2\pi * \Delta V_{ripple} * f_{AC}} \quad (6)$$

Where:

- P_{OUT} is the output power
- V_{DCBus} is the DC link voltage
- ΔV_{ripple} is the peak to peak ripple voltage
- f_{AC} is the grid frequency

2.3.3 C_x Capacitance Selection

C_x are the capacitors connected between line-to-neutral. The aim of these capacitors is to attenuate the differential mode noise injected from the DC/AC into the grid. The value of these capacitors is a trade-off between reactive power delivered to the grid and the differential mode attenuation. By default, the reactive power injected into the grid is equal to:

$$Q = V_{LN}^2 * C_x * \omega \quad (7)$$

Where:

- C_x represent the equivalent capacitance connected between the line and the neutral
- ω is the grid electrical pulsation

Placing very high capacitance significantly reduces the injected noise, but leads to too much injected reactive power.

2.3.4 C_y Capacitance Selection

To detect small leakage current (typically 5-30mA) to prevent device damage or electrocution. Certain standards for the leakage current issue mention that PV systems with the transformer-less inverter must discontinue service if the leakage current value of 100mA can persist up to 0.04s.

The leakage current through the Y capacitors can be calculated with:

$$I_Y = V_{LN}^2 * C_Y * \omega \quad (8)$$

2.4 Highlighted Products

2.4.1 LMG366xR025 650V 25mΩ GaN FET With Integrated Driver and Protection

The LMG366xR025 GaN FET with integrated driver and protection is targeted at switch-mode power converters and enables designers to achieve new levels of power density and efficiency.

Adjustable gate driver strength allows the control of turn-on and maximum turn-off slew rates independently, which can be used to actively control EMI and optimize switching performance. Turn on slew rate varies from 10V/ns to 80V/ns, while the turn off slew rate control is available only in LMG3666R025 and LMG3667R025. The turn off slew rate can be limited from 10V/ns to a maximum based on the magnitude of load current.

Protection features include under-voltage lockout (UVLO), cycle-by-cycle overcurrent limit, and short-circuit and overtemperature protection. The LMG3661R025 provides a 5V LDO output on LDO5V pin that powers external digital isolators.

The LMG3666R025 includes the zero-voltage detection (ZVD) feature which provides a pulse output from the ZVD pin when zero-voltage switching is realized. The LMG3667R025 includes the zero-current detection (ZCD) feature that sets the ZCD pin high when the drain-to-source current is negative and transitions to low upon detecting the zero-crossing point.

2.4.2 TMS320F28P551 Real-Time Microcontrollers

The TMS320F28P55x (F28P55x) is a member of the C2000 real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high power density, high switching frequencies, and supporting the use of GaN and SiC technologies.

The real-time control subsystem is based on TI's 32-bit C28x DSP core, which provides 160MHz of signal processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the Floating-Point Unit (FPU), Trigonometric Math Unit (TMU), and VCRC

(Cyclical Redundancy Check) extended instruction sets, speeding up common algorithms key to real-time control systems.

The CLA allows significant offloading of common tasks from the main C28x CPU. The CLA is an independent 32-bit floating-point math accelerator that executes in parallel with the CPU. Additionally, the CLA has dedicated memory resources and can directly access the key peripherals that are required in a typical control system. Support of a subset of ANSI C is standard, as are key features like hardware breakpoints and hardware task-switching.

The F28P55x supports up to 576KB of flash memory divided into two 256KB banks plus one 64KB bank, which enable programming one bank and execution in another bank in parallel. Up to 101KB of on-chip SRAM is also available to supplement the flash memory.

2.4.2.1 Hardware Features

The TMDSCNCD28P55X hardware features follow:

- Onboard 6-pin JTAG debug connector enables real-time in-system programming and debugging, isolated debugger is need for safety.
- Analog I/O, digital I/O, and JTAG signals at interface

2.4.2.2 Software Features

The TMDSCNCD28P55X software features include:

- TI Code Composer Studio IDE - integrated development environment for TI microcontrollers and embedded processors
- Software development kits (SDK)
- C2000Ware - low-level device drivers and examples
- DigitalPower SDK - digital power system development for various AC-DC, DC-DC and DC-AC power supply applications

2.4.3 TMCS1123 - Precision 250kHz Hall-Effect Current Sensor With Reinforced Isolation

The TMCS1123 is a galvanically isolated Hall-effect current sensor with industry leading isolation and accuracy. An output voltage proportional to the input current is provided with excellent linearity and low drift at all sensitivity options. Precision signal conditioning circuitry with built-in drift compensation is capable of less than 1.4% maximum sensitivity error over temperature 1.4% and lifetime with no system level calibration, or less than 0.9% maximum sensitivity error including both lifetime and temperature drift with a one-time calibration at room temperature.

AC or DC input current flows through an internal conductor generating a magnetic field measured by integrated, on-chip, Hall-effect sensors. Core-less construction eliminates the need for magnetic concentrators. Differential Hall sensors reject interference from stray external magnetic fields. Low conductor resistance increases measurable current ranges up to ±96A while minimizing power loss and easing thermal dissipation requirements. Insulation capable of withstanding 5kVRMS, coupled with a minimum of 8mm creepage and clearance, provides high levels of reliable lifetime reinforced working voltage.

Integrated shielding enables excellent common-mode rejection and transient immunity. Fixed sensitivity allows the device to operate from a single 3V to 5.5V power supply, eliminating ratiometry errors and improving supply noise rejection.

2.4.4 INA185 26V, 350kHz, Bidirectional, High-Precision Current Sense Amplifier in Ultra Small (SOT-563) Package

The INA185 current sense amplifier is designed for use in cost-sensitive space constrained applications. This device is a bidirectional, current-sense amplifier (also called a current-shunt monitor) that senses the voltage drop across a current-sense resistor at common-mode voltages from –0.2V to +26V, independent of the supply voltage. The INA185 integrates a matched resistor gain network in four, fixed-gain device options: 20V/V, 50V/V, 100V/V, or 200V/V. This matched gain resistor network minimizes gain error and reduces the temperature drift.

The INA185 operates from a single 2.7V to 5.5V power supply. The device draws a maximum supply current of 260µA and features high slew rate and bandwidth making this device an excellent choice for many power-supply and motor-control applications.

The INA185 is available in an industry standard SC70 package and low profile 6-pin, SOT-563 package. The SOT-563 package has a body size of size of only 2.56mm2, including the device pins. All device options are specified over the extended operating temperature range of –40°C to +125°C.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

The Device under Test (DUT) in this design is set up and operated in several pieces:

- One TIDA-011008 board, heatsink and thermal interface material (T-Work8000).
- 4-pin or 6-pin isolated JATG debugger like XDS110ISO-EVM
- Power adapter with 12V output and 2A rating
- Laptop
- Oscilloscope, current and voltage probes.
- Thermal camera
- Adjustable high power AC resistor (4 kW Rated)
- 3.6kVA bidirectional AC grid emulator (230 VAC)
- 3.6kW solar panel emulator (600 VDC)
- 3.6kW DC load (400V)

3.2 Test Setup

3.2.1 Testing TIDA-011008

In this test condition, the system is configured to operate in a close-loop control mode. The control is executed by the TMS320F28P551. The MCU is implementing current control loops able to synchronize with the grid voltages of the AC source emulator. The synchronization with the grid is happening by means of PLL. At the same time, the peak current reference of the three current loops is generated by the voltage control loop. The peak current is responsible for controlling the active power flowing between the DC and the AC.

On the DC side, the Solar Panel Emulator controls the power flowing from the DC input to the DC link.

In above operating conditions, efficiency versus power were measured.

3.3 Test Results

3.3.1 Testing TIDA-011008 Boost Stage

To run this test, the board needs to be connected as shown in 3.2.1.

In this test, the boost stage is tested with the common mode choke shorted, and one of the DC link capacitor is removed for the DC Load connection as shown in Figure 3-1, the testing results are shown below.

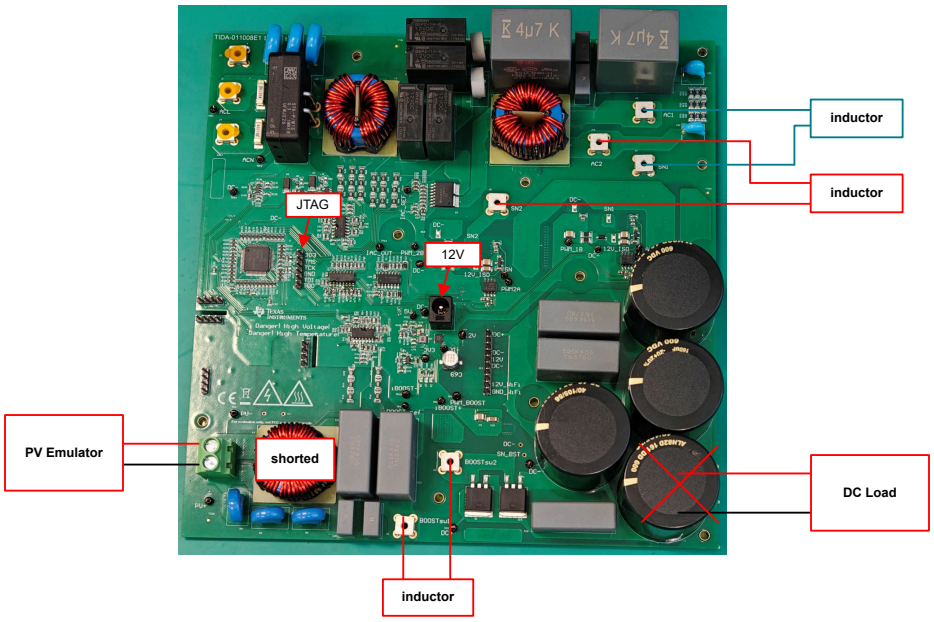


Figure 3-1. Connections for testing Boost Stage

The switching node waveform as shown in Figure 3-2 has no big overshoot or ringing even with >40V/ns V_{ds} slew rate, indicating the GaN power stage has a clean power loop and good integrated driver circuit.

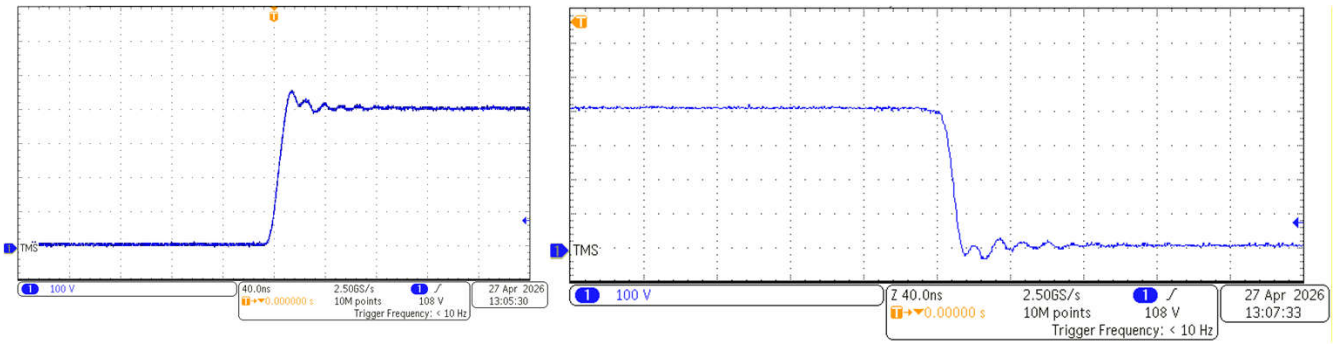


Figure 3-2. Boost Switching Node Waveform

As can be seen in Figure 3-3, the high load maximum efficiency is ~99.2%, the full load efficiency is ~99.1%.

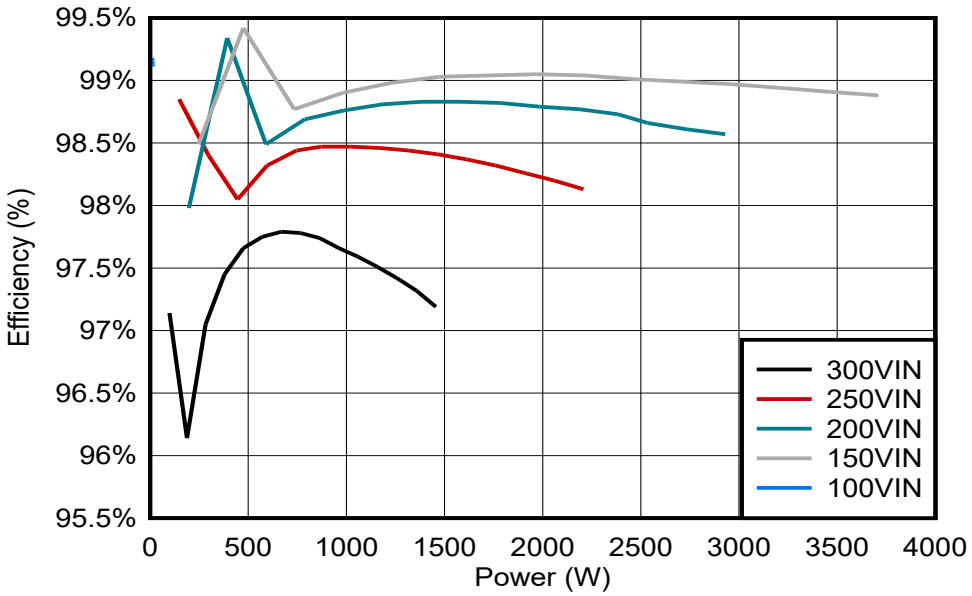


Figure 3-3. Boost Stage Efficiency with Different Input Voltage

Can be noticed on the low load condition, there are several high efficiency points where the current on the boost inductor goes to 0 and boost is in DCM mode. In this condition, the turning-on voltage on the GaN device is quite low, which achieve almost ZVS, improves the efficiency a lot.

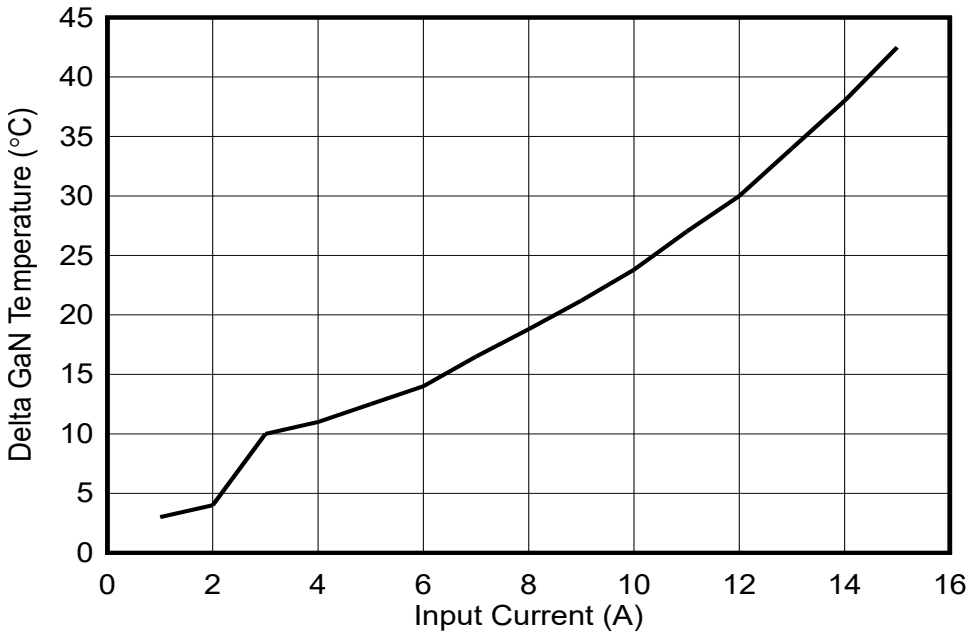


Figure 3-4. Boost Stage GaN Temperature Rise

As can be seen in Figure 3-4, the temperature rise of GaN at maximum output power is ~43°C. The temperature is measure on the other side of PCB since the top side of GaN is attached with heatsink. The test condition is input voltage 250VDC, output voltage 400VDC.

3.3.2 Testing TIDA-011008 DC/AC Stage

To run this test, the board needs to be connected as shown in Figure 3-5. The DC input is 400V, the AC output is connected to a 230Vrms AC voltage.

In this test, the DC/AC stage is tested with the common mode choke shorted, and one of the DC link capacitor is removed for the DC source connection, the testing results are shown below.

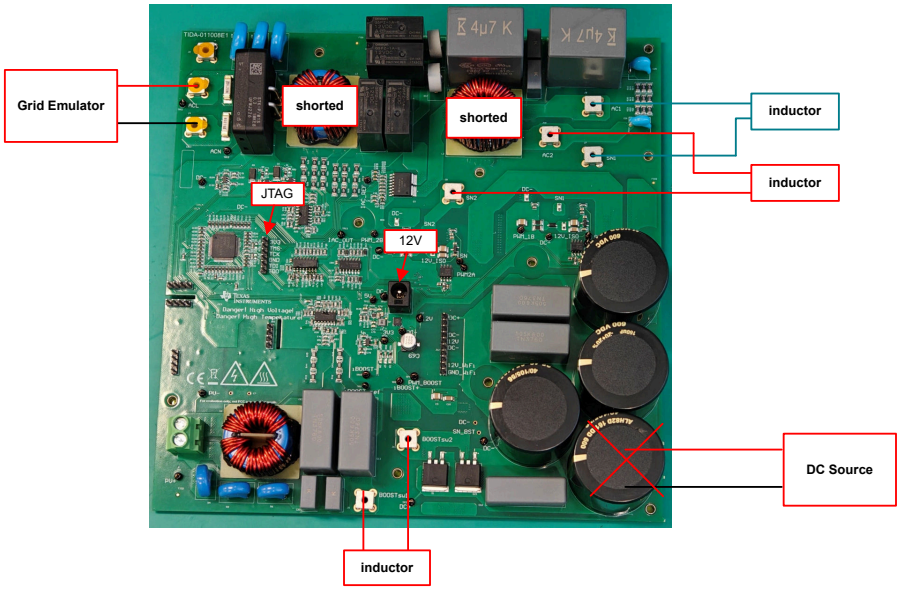


Figure 3-5. Connections for testing DC/AC Stage

The switching node waveform as shown in Figure 3-6 has no big overshoot or ringing even with >40V/ns V_{ds} slew rate, indicating the GaN power stage has a clean power loop and good integrated driver circuit.

Channel 1 waveform is one leg switching node, Channel 2 waveform is another leg switching node waveform. Channel 4 waveform is the AC output current.

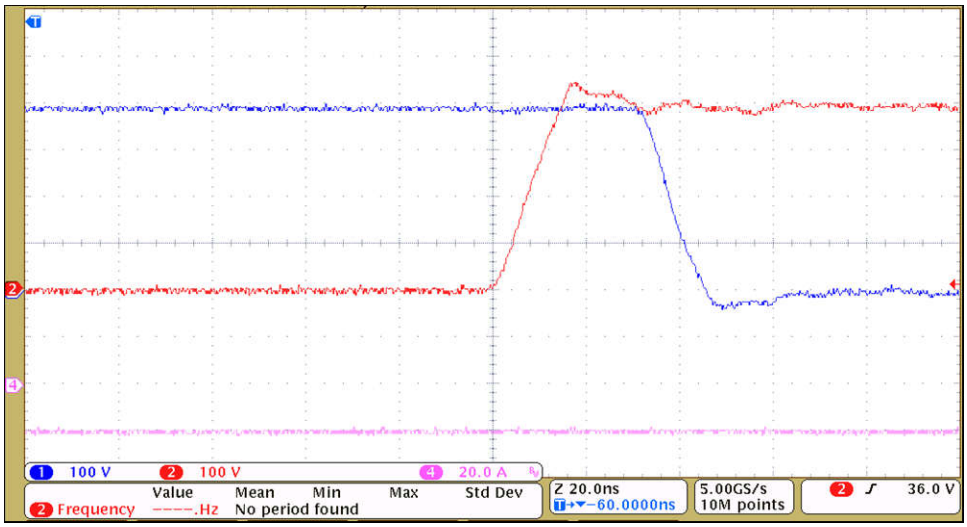


Figure 3-6. DC/AC Switching Node Waveform

As can be seen in Figure 3-7, the peak efficiency of the DC/AC stage is ~98.4%. The full-load efficiency is ~98%.

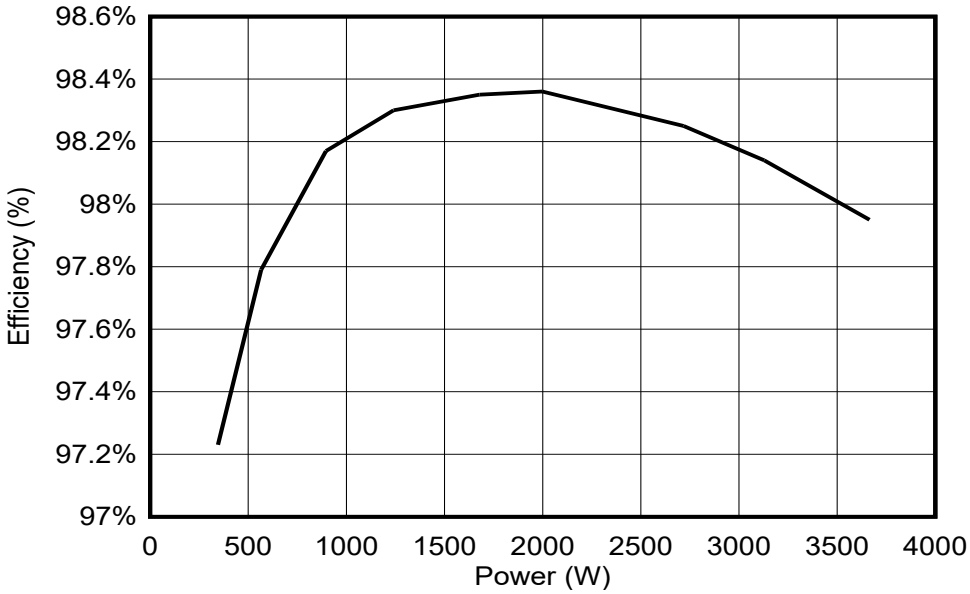


Figure 3-7. DC/AC Stage Efficiency with 400VDC Input

In this test, the heatsink is heated up to 40°C before testing, the ambient temperature is ~30°C, as can be seen in Figure 3-8, the temperature of GaN at maximum output power is ~80°C, the temperature rise of GaN is ~50°C. The temperature is measure on the other side of PCB since the top side of GaN is attached with heatsink.

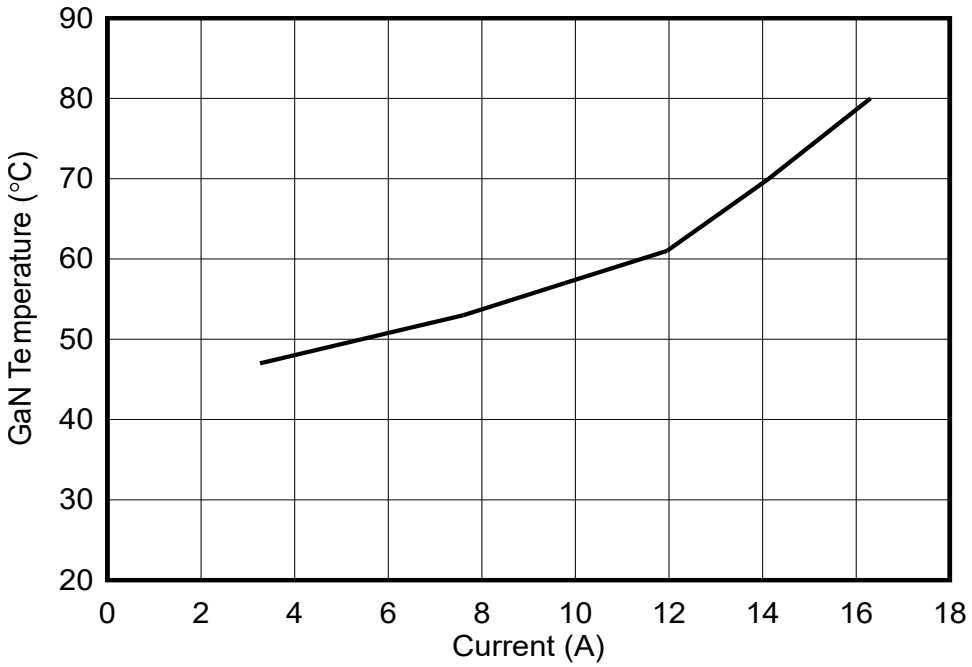


Figure 3-8. DC/AC Stage GaN Temperature

3.3.3 Total System Testing

In this chapter, the two stages are tested together to verify the system efficiency.

To run this test, the board needs to be connected as shown in Figure 3-9. The three common mode choke is installed on the board. The testing results are shown below.

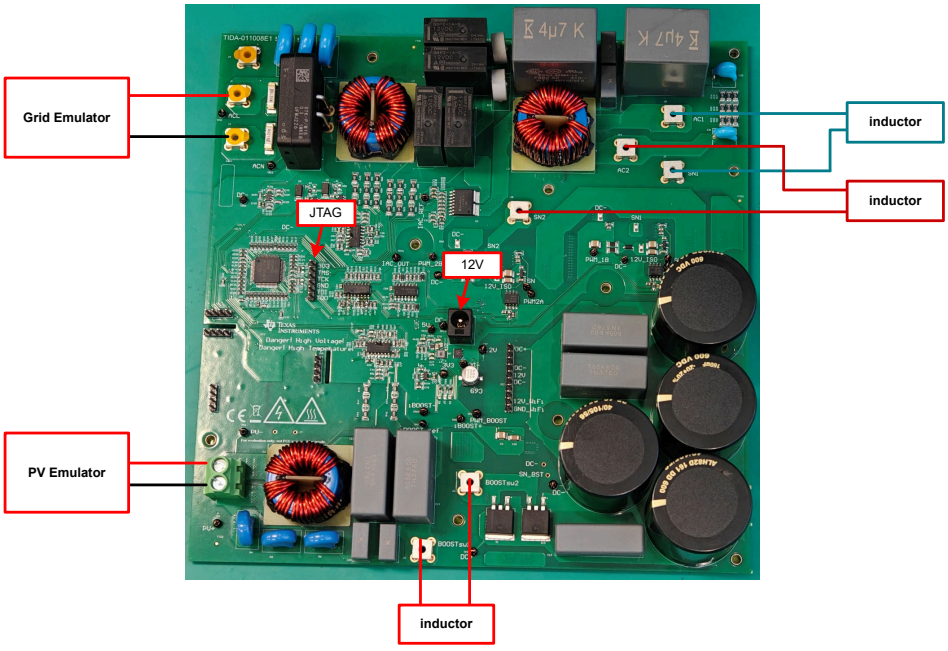


Figure 3-9. Connections for Testing the Whole Board

As can be seen from Figure 3-10, the output AC current has very low THD (1.23%). CH1 is boost inductor current, CH2 is DC link voltage, CH3 is grid voltage, CH4 is grid current.

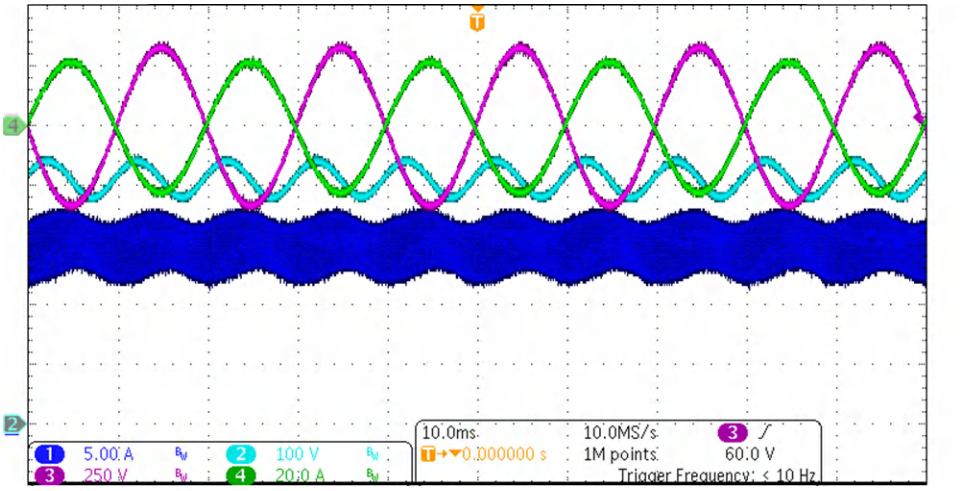


Figure 3-10. Whole Board Testing Waveform Connected With Grid Emulator

As can be seen from Figure 3-11, even connected with real grid (with 4.2% THD AC voltage), the output current THD is still pretty low (3.5%).

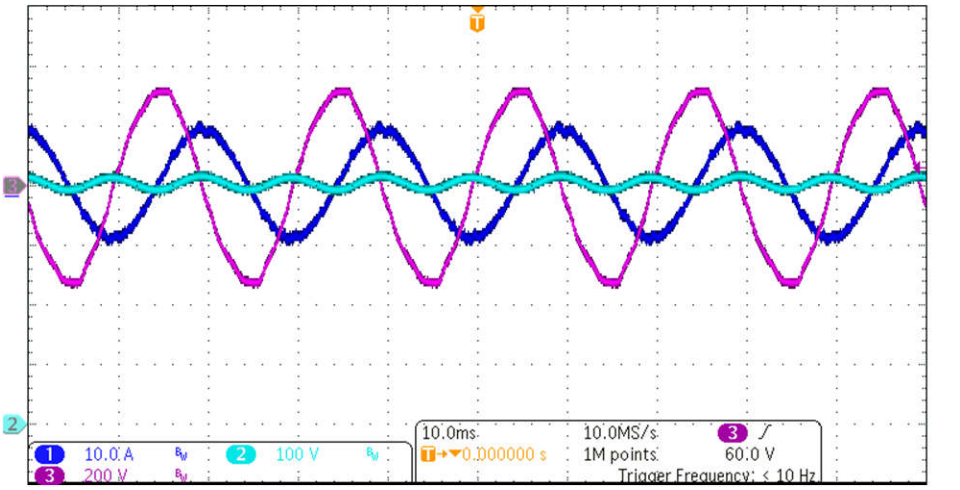


Figure 3-11. Whole Board Testing Waveform Connected With Real Grid

The whole system efficiency at full load, with both Boost and DC/AC stage switching at 100kHz is 96.7%, CEC weighted efficiency is 96.4% as shown in Figure 3-12. The DC input is 250V, the AC output is connected to a 230Vrms AC voltage.

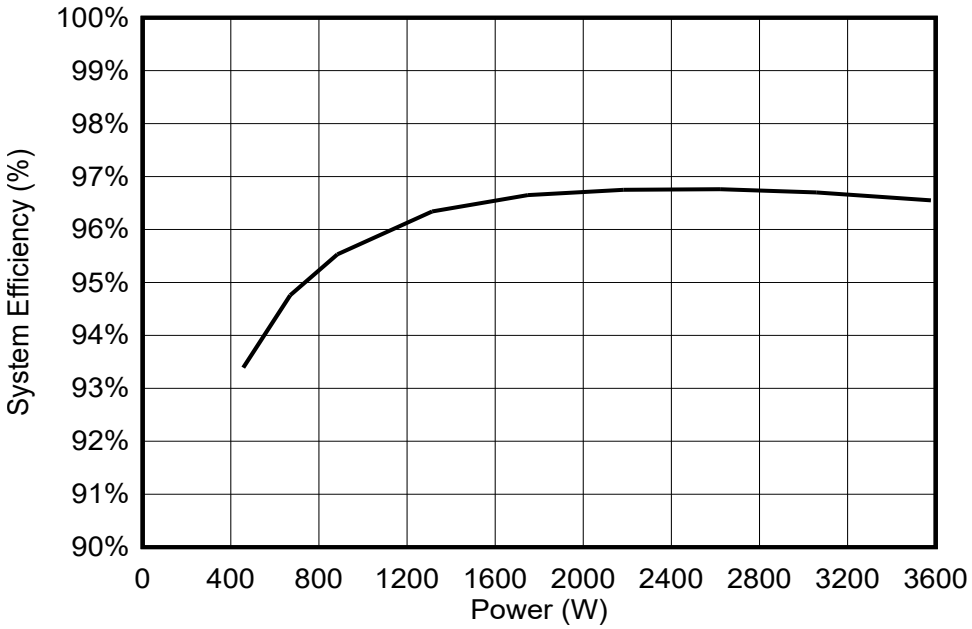


Figure 3-12. Whole Board Testing Efficiency With Both Stages Switching

The whole system efficiency at full load, with Boost stage not switching and DC/AC stage switching at 100kHz is 97.4%, CEC weighted efficiency is 97.3% as shown in Figure 3-13. The DC input is 400V, the AC output is connected to a 230Vrms AC voltage.

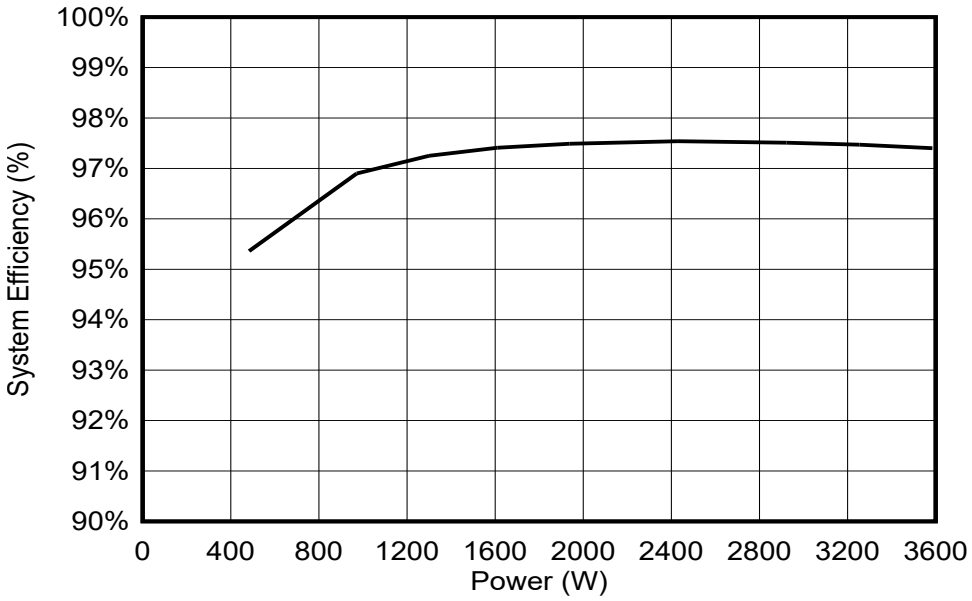


Figure 3-13. Whole Board Testing Efficiency With Boost Stage Not Switching

4 Design and Documentation Support

4.1 Design Files

To download the design files, see the design files at TIDA-011008.

4.1.1 Schematics

To download the schematics, see the design files at TIDA-011008.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-011008.

4.2 Tools and Software

TMDSCNCD28P55X Real-Time Microcontrollers.

4.3 Documentation Support

1. Texas Instruments, *Basic Calculation of a Boost Converter's Power Stage* application note.

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

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