Design Guide: TIDA-010985

Resistive-Bridge Insulation Monitoring Device for 800V DC Systems With Large Y Cap Reference Design

Description

This reference design features a resistive-bridge insulation monitoring device (IMD). The design accurately detects symmetrical and asymmetrical isolation resistance faults. The reference design also measures capacitance for high-voltage DC systems with large Y-capacitances (Y caps). The design meets response time requirements per UL standards.

Resources

TIDA-010985	Design Folder
LP-MSPM0G3507	Tool Folder
TPSI2240-Q1	Product Folder
RES60A-Q1, TLV9002-Q1	Product Folder
ISOW1044, TPSM33620-Q1	Product Folder
TPS7A20, TSM24CA	Product Folder

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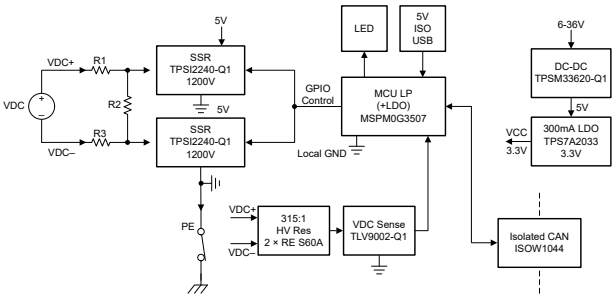
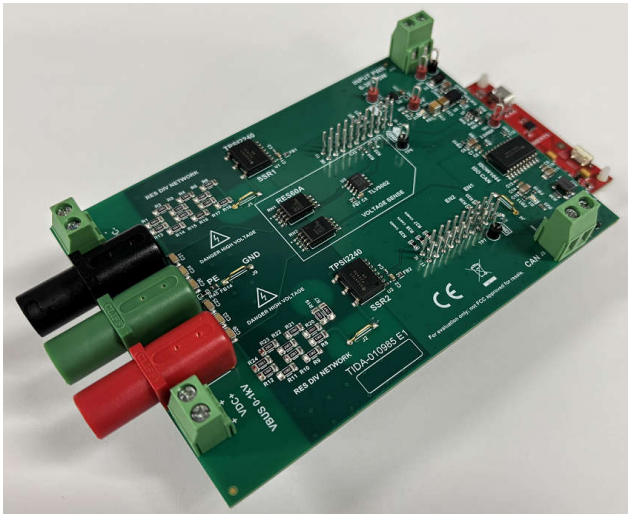


Features

- Large Y-cap support (up to 9µF total)
- Low-computation predictive algorithm to shorten response time
- Low voltage variation on Y caps (±10% with regard to protective earth)
- Provides both symmetrical and asymmetrical fault detection
- ±5% resistance and ±15% capacitance measurement errors (±3σ)
- Supports UL 2231-2 ±15% accuracy and 10s response time
- Supports up to 1kV bus voltage
- Isolated Controller Area Network (CAN) 2.0 for communication

Applications

- High-voltage battery system
- ESS – Battery management system (BMS)
- String inverter
- DC fast charging power module



1 System Description

High-voltage (HV) DC systems show accelerated adoption across multiple end equipment applications including energy storage systems, data centers, solar inverters, and DC fast chargers. The typical DC voltage for these applications ranges from 150V to 1000V. Larger energy storage systems operate at voltages up to 1500V.

User protection represents an important design consideration in these HV DC systems. All HV parts of the system receive electrical isolation from PE through high-omic paths (typically in the high MΩ range). The insulation limits the maximum leakage current. International standards (for example, UL 2231-2, IEC 61851-23 for EV charging) require that leakage current remain limited to 10mA (that is, 100Ω/V) to avoid personal injury from contact with the system. IEC 61851-23 specifies a safe isolation rating when the leakage measures less than 2mA (500Ω/V). Table 1-1 shows the insulation monitoring device (IMD) key thresholds. Figure 1-1 shows that the IMD monitors insulation resistance and reports faults to the main controller when the insulation resistance becomes insufficient. The main system controller initiates a safe shutdown sequence following a fault. These IMDs operate continuously at a low frequency of 1Hz to 2Hz because insulation changes occur slowly.

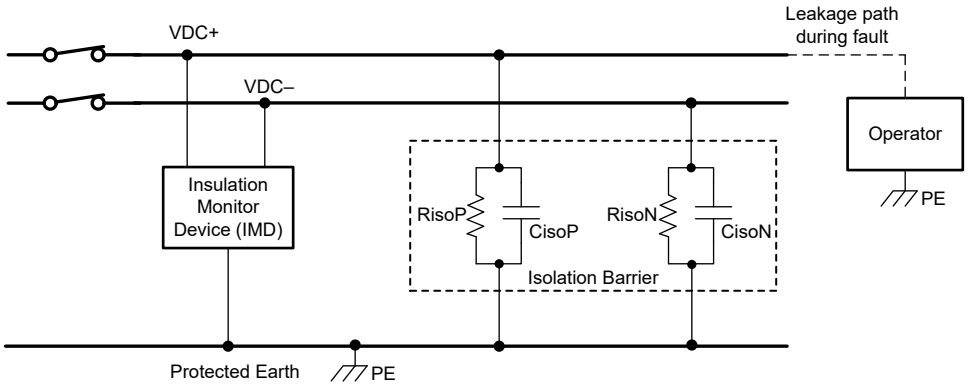


Figure 1-1. Insulation Monitoring Device in DC Unearthed Distribution Systems

Table 1-1. IMD Key Thresholds from IEC and UL Standards

STATUS	Ω/V	LEAKAGE CURRENT	800V VBus	1000V VBus
Warning	500	2mA	400kΩ	500kΩ
Fault	100	10mA	80kΩ	100kΩ

1.1 Insulation Monitoring

There are a number of methods for measuring insulation. However, the two most common methods are AC current injection and resistive bridge. In general, the AC current injection method is flexible for various operation conditions and is widely used in DC charging but has higher complexity and cost compared to the resistive bridge method. Regardless of the method, the approach has to meet the standard requirements such as accuracy, response time, and operating voltage limits. One of the key challenges associated with the resistive bridge method is dealing with a large RC time constant. Some systems such as megawatt chargers require very large Y-capacitances (for example, 4µF). This reference design, TIDA-010985, implements the resistive-bridge approach, and is specially designed to deal with large Y-capacitances by employing a novel predictive algorithm to shorten the measurement time without requiring heavy computation such as floating-point operations. In addition, this new design topology limits the voltage variation on the Y caps. Table 1-2 shows a comparison overview of the various methods.

Table 1-2. Comparison of Various IMD Methods

METHOD	ADVANTAGES	DISADVANTAGES
AC current injection • Typically sold as a standalone module	• Can measure energized and non-energized lines • No reduction in insulation resistance during measurement • Supports UL 2231-2 including large Y caps	• High hardware complexity and cost • High software complexity (AC signal processing, floating point math)
Resistive Bridge • TIDA-01513, BQ79731 EVM • TIDA-010232 (MCU on isolated GND)	• Easy implementation – both hardware and software • Low cost • Low calculation effort	• Does not support UL 2231-2 for large Y caps (> 100nF) • Does not support IEC 61851-23 due to high voltage swings relative to PE during measurement. Limits applications to < 500 Vbus • Only capable of measuring energized lines • Slightly reduces insulation resistance during measurement
Balanced Resistive Bridge + Prediction Algorithm • TIDA-010985 (MCU on Earth GND)	• Easy implementation – both hardware and software • Low cost and computationally light • Limited voltage swings relative to PE during measurement, supporting IEC 61851-23 • Supports UL 2231-2 including large Y caps	• Only capable of measuring energized lines • Slightly reduces insulation resistance during measurement

1.2 Key System Specifications

Table 1-3. Key UL 2231-2 , IEC 61851-23 Specifications

PARAMETER	UL 2231-2 / IEC 61851-23 SPECIFICATION	TIDA-010985
Trip Accuracy (symmetrical and asymmetrical faults)	15%	5%
Response time	<10 seconds	< 2 seconds (Ciso = 4µF, Riso = 1MΩ)
Line to PE Voltage Variation % of VDC	10%	10% (that is, 50V for 1kV bus)

Table 1-4. Key Electrical Specifications

PARAMETER	SPECIFICATION	Unit
Riso Measurement Range (maximum tested)	2	MΩ
Riso Measurement Error (3σ)	±5	%
Ciso Measurement Range (maximum tested)	9	µF
Ciso Measurement Error (3σ)	±15	%
Isolation Measurement Cycle Time (configurable)	2	s
HV Bus Voltage (maximum)	1000	V
ADC Full Scale Input	3.3	V
Voltage Divider Resistance	12.5 ±15%	MΩ
IMD Leakage Current (maximum, active)	2	mA
IMD Leakage Current (maximum, inactive)	100	µA
Resistive Bridge Power Dissipation (maximum)	0.85	W
Power Supply	6-36 or Isolated USB to LP	V
Power Consumption (maximum)	2	W
Operating Temperature	-40 to 85	°C
Interface	CAN 2.0	N/A

2 System Overview

2.1 Block Diagram

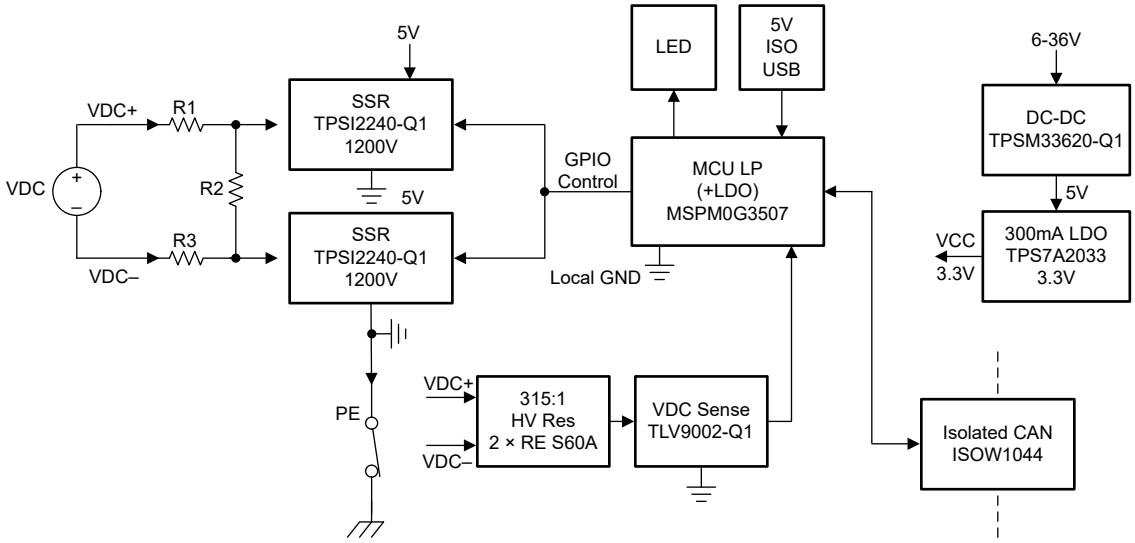


Figure 2-1. System Block Diagram

2.2 Design Considerations

2.2.1 TIDA-010985 Overview

Figure 2-2 shows the TIDA-010985 analog front end (AFE) key system components as mentioned in the following list:

1. Mechanical connectors to DC+, DC– and Protected Earth (PE)
2. The quasi-balanced resistive network providing multiple test resistance combinations (Rsn, R1, Rsp).
3. TPSI2240 bidirectional solid-state switches (SW1, SW2) to alternate the resistive network
4. Single-supply inverting amplifier for voltage sensing of VDC– relative to PE. Voltage is scaled down to ADC level (Vn). Required to calculate RisoN and RisoP.
5. Single-supply voltage buffer for voltage sensing of VDC+ relative to PE. Voltage is scaled down to ADC level (Vp). Required to calculate RisoN and RisoP.
6. A microcontroller is used to control these switches, sample the analog outputs (simultaneously), and calculate the insulation resistances.

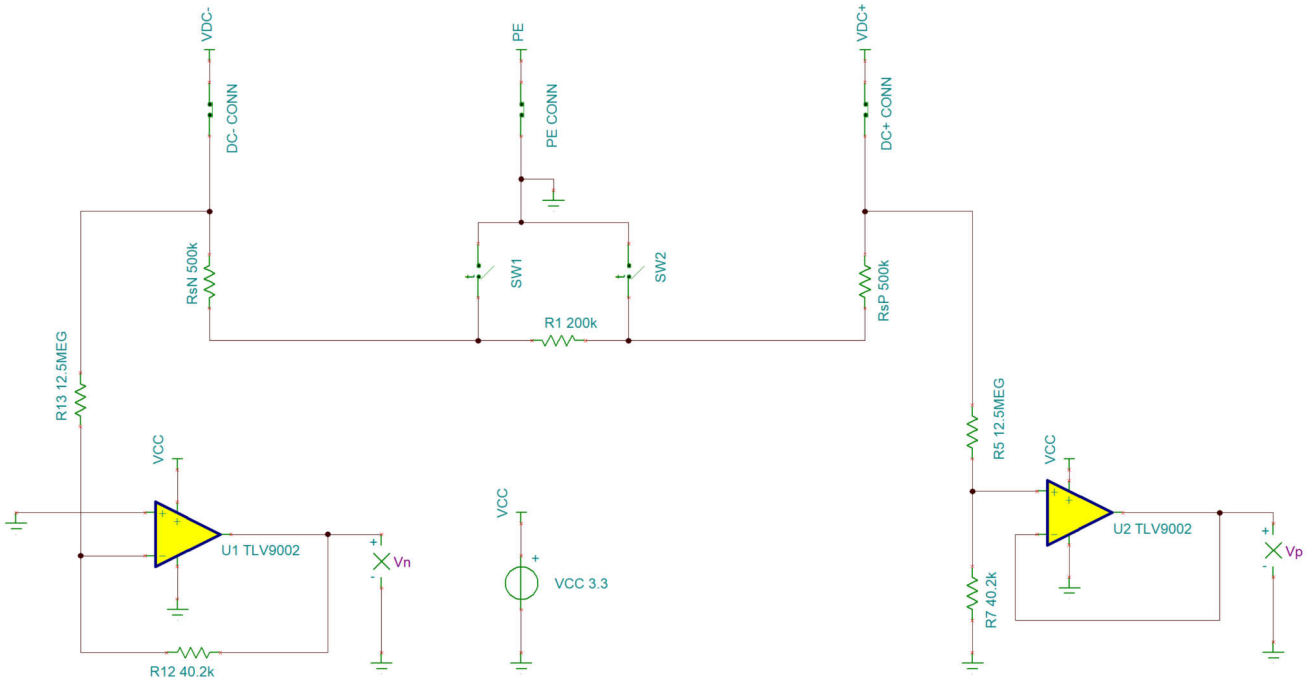


Figure 2-2. TIDA-010985 Simplified Schematic Without Target System Connected

Figure 2-3 shows the simplified schematic with the target system connected. The IMD must determine all Riso and Ciso passive values.

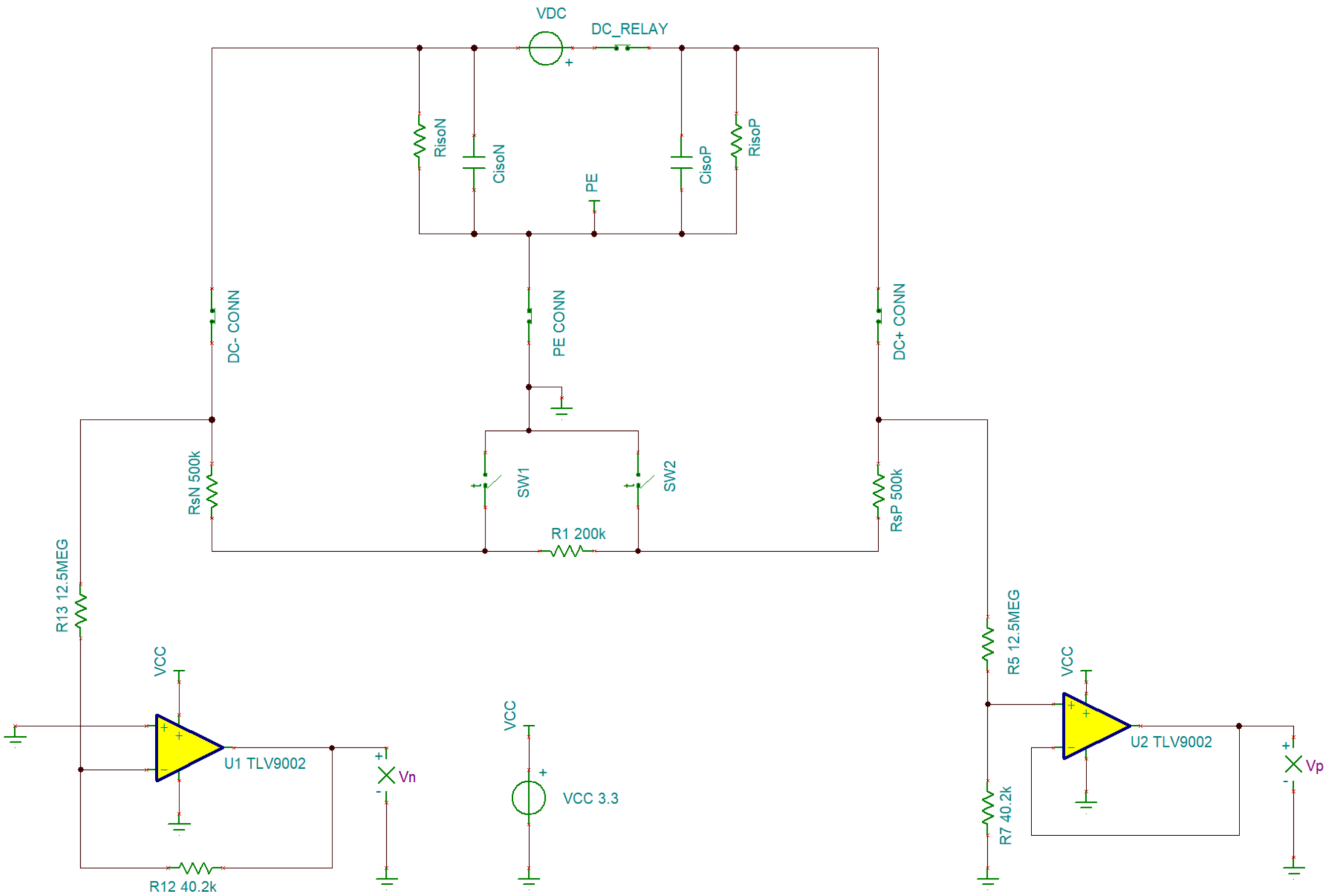


Figure 2-3. Simplified Design Schematic With Target System Connected

2.2.2 Solving for the Unknown Isolation Resistances

Two switches enable multiple resistive bridge test ratios using RsP, RsN, and R1. This configuration provides detection capability for any given RisoP to RisoN ratio. The system detects both asymmetric and symmetric faults. Table 2-1 shows the possible switching states for TIDA-010985 and corresponding equations. Only two switching states (except D) are required to solve for RisoP and RisoN. Two equations solve for two unknowns.

Table 2-1. All Possible Switching States for TIDA-010985

STATE	SW1	SW2	RsP:RsN RATIO	STEADY STATE EQUATION
A	ON	OFF	7:5	$\frac{Vp}{Vn} = \frac{-RisoP \mid\mid (7R)}{RisoN \mid\mid (5R)}$
B	OFF	ON	5:7	$\frac{Vp}{Vn} = \frac{-RisoP \mid\mid (5R)}{RisoN \mid\mid (7R)}$
C	ON	ON	5:5	$\frac{Vp}{Vn} = \frac{-RisoP \mid\mid (5R)}{RisoN \mid\mid (5R)}$
D	OFF	OFF	N/A	N/A

In theory, designers can choose any two combinations of A, B, and C switching states. This reference design uses switching states A and B to solve for the isolation resistances. This AB combination maximizes the signal to noise ratio (SNR) by generating the greatest voltage difference between the switching states while limiting voltage variation under IEC requirements. With this selection, the two relevant equations are:

$$\frac{Vp1}{Vn1} = \frac{-RisoP \mid\mid (7R)}{RisoN \mid\mid (5R)} \quad (1)$$

$$\frac{Vp2}{Vn2} = \frac{-RisoP \mid\mid (5R)}{RisoN \mid\mid (7R)} \quad (2)$$

where

- Vp1 is the voltage of first DC+ measurement (Switch state A)
- Vn1 is the voltage of first DC– measurement (Switch state A)
- Vp2 is the voltage of second DC+ measurement (Switch state B)
- Vn2 is the voltage of second DC– measurement (Switch state B)

Using two equations solves for the two unknowns (RisoP and RisoN). MATLAB® helped solve the equations.

```
% solve for two equations with two unknowns assuming settled voltages
clc
syms rp rn vp1 vp2 vn1 vn2 rs
% change the sign if we're using inverting op amp for the vn sense
eq1 = vp1/vn1 == (rp*7*rs/(rp+7*rs)) / (rn*5*rs/(rn+5*rs));
eq2 = vp2/vn2 == (rp*5*rs/(rp+5*rs)) / (rn*7*rs/(rn+7*rs));
eq3 = rs > 0 & vp1 > 0 & vn1 > 0;
eqns = [eq1, eq2, eq3];
%
[srna, srpa, parametersa, conditionsa] = solve(eqns,[rn, rp],ReturnConditions=true)
%
```

The calculation for this yields:

$$RisoN = \frac{-(35 \times Vn1 \times Vp2 - 35 \times Vn2 \times Vp1) \times RS}{(7 \times Vn1 \times Vp2 - 5 \times Vn2 \times Vp1 + 2 \times Vp1 \times Vp2)} \quad (3)$$

$$RisoP = \frac{-(35 \times Vn1 \times Vp2 - 35 \times Vn2 \times Vp1) \times RS}{(2 \times Vn1 \times Vn2 + 7 \times Vn1 \times Vp2 - 5 \times Vn2 \times Vp1)} \quad (4)$$

Note the RS constant is defined as 100kΩ. If users use a different ratio, the MATLAB script can be modified to solve for the new chosen ratio.

Figure 2-4 shows an example voltage waveform with the AB combination. In this example, each switching state lasts for one second. One IMD measurement cycle takes two seconds since measurement for the two states is required. Vp1 and Vn1 are measured simultaneously within the first second, and Vp2 and Vn2 are measured simultaneously in the following second. Note that simultaneous ADC measurement of Vp and Vn rejects noise disturbances on the HV bus. The Riso answer depends on the difference in ratios of Vp to Vn (not the individual absolute Vp and Vn).

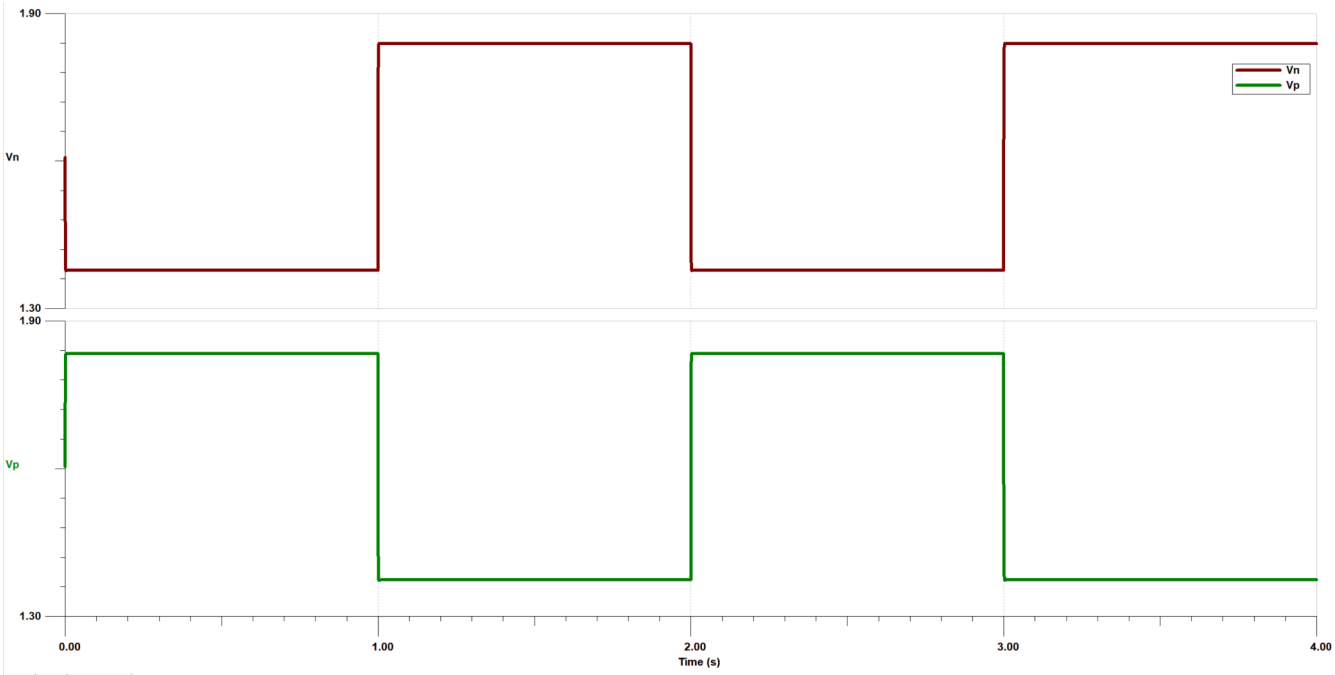


Figure 2-4. Example AB Switch Toggling Mode Waveform

2.2.3 Addressing Large Time Constant Cases

In the previous example, no significant RC settling time before the ADC measures Vp and Vn is assumed. In some conditions, such as the example in Figure 2-5, the time constant can be quite long. Without a workaround, the system can need to wait for a significant amount of time for the voltage to settle and thus fail to meet the standard response time requirements (for example, UL 2231-2 is 10s).

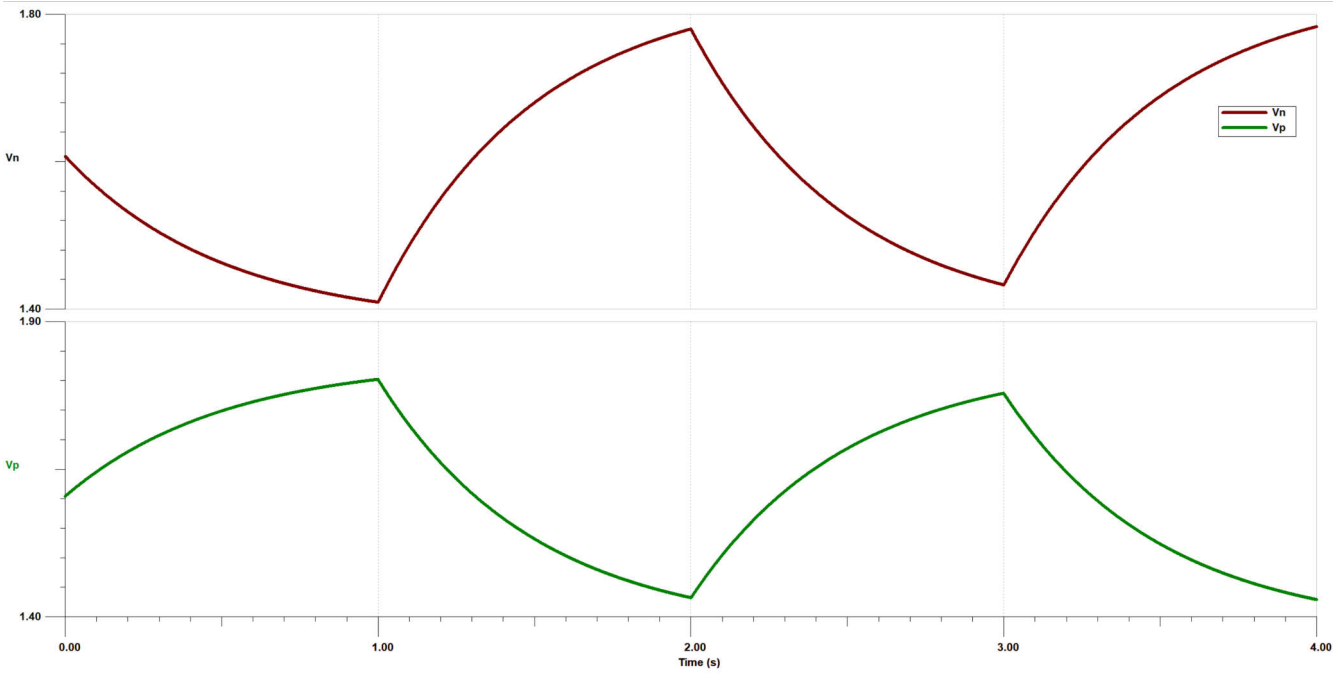


Figure 2-5. Example Waveforms With Large Time Constant

The time constant τ when SW1 is ON and SW2 is OFF:

$$\tau = (\mathrm{RisoP}\,||\,\mathrm{RisoN}\,||\,\mathrm{RsP} + \mathrm{R1}\,||\,\mathrm{RsN}) \times (\mathrm{CisoP} + \mathrm{CisoN}) \quad (5)$$

There are a number of ways to address the larger time constant cases (that is, large Y caps in the µF range):

- Use lower Rsp and Rsn values at the expense of increased power dissipation and leakage current. This approach is often not practical, since higher leakage currents violate standard requirements.
- Increase the cycle time (for example, from 2s to 3s) to account for the added settling time. This is often not practical with the UL response time limit.
- Use multiple measurements and an algorithm to predict the final settling voltage. When done correctly, this can help extend the IMD operating range without increasing power and time. This topic is discussed in Section 2.2.4.

2.2.4 Prediction Algorithms

When SW2 is ON, the response follows the exponential decay equation:

$$V(t) = V_{inf} + V_o e^{\frac{-t}{\tau}} \quad (6)$$

where

- V_{inf} is the final settled voltage (t = infinity)
- V_o is the difference between the initial voltage at time zero, $V(t_0)$, and V_{inf}.

See Figure 2-6 for a better understanding of the concept.

The settling voltage, V_{inf}, is of specific interest. The three unknowns in this equation are V_{inf}, τ, and V_o. If the ADC measures three sample voltages at three different times, a system of three equations is created:

$$V(t_0) = V_{inf} + V_o \quad (7)$$

$$V(t_1) = V_{inf} + V_o e^{\frac{-t_1}{\tau}} \quad (8)$$

$$V(t_2) = V_{inf} + V_o e^{\frac{-t_2}{\tau}} \quad (9)$$

By using $t_2 = 2 \times t_1$, the calculation for V_{inf} is heavily simplified:

$$V_{inf} = \frac{V(t_0) \times V(t_2) - V(t_1)^2}{V(t_0) - 2V(t_1) + V(t_2)} \quad (10)$$

- Note that only four-function arithmetic is needed to compute the V_{inf}. Once V_{inf} is calculated, V_o can be calculated by subtracting V_{inf} from $V(t_0)$.
- In theory, the location of t_0 on the decay curve does not matter as long as t_1 and t_2 are spaced appropriately relative to each other. Specifically, users must keep the same time difference between the three samples. For longer time constants, the voltage settling curve can be relatively flat for the same cycle time. In noisy conditions, increasing the time spacing between the three samples increases SNR and thus improves the prediction algorithm performance.

The MATLAB script used to solve for the system of equations is:

```
%% solution for exponential decay
clc
syms vt0 vt1 vt2 vinf v0 x
eq1 = vt0 == vinf+v0;
eq2 = vt1 == vinf+v0*x;
eq3 = vt2 == vinf+v0*x*x;
eq4 = vt0 ~= vt1;
eqns = [eq1, eq2, eq3, eq4];
[vinf, v0, x, para, conditions] = solve(eqns,[vinf, v0, x],ReturnConditions=true)
```

In the TIDA-010985 default code, the time spacing between the three samples is 330ms. This keeps the total IMD measurement cycle time under 2s while making the fixed-point computation straightforward. To change the default cycle time, users can do one of the following:

- Change the E1 #define in IMD.c. For example, changing E1 #define from 990 to 600 (ms) decreases the IMD cycle time from about 2s to about 1.2s. The exact time depends on a few milliseconds (ms) of computation (about 2ms) after the data acquisition period. If the user wants to increase the cycle time for some reason, the data buffer "SamplesSize" must be changed accordingly in addition to E1 #define. Without changing the default ADC sampling period, increasing the data buffer can be limited due to available SRAM (32kB total):

```
#define SamplesSize 2000 // ADC buffer size
#define E1 990 // total time for Riso measurement is 2xE1 in ms
```

- Change the ADC sampling interval by changing the TIMER_0 period in syscfg (for example, from 1ms to 0.5ms). This requires some changes to the rest of the code since the code assumes the default 1ms ADC sampling period.

The time constant is calculated with the following equation:

$$\tau = \frac{-V_o}{V'(t_0)} \quad (11)$$

For isolation resistance, only V_{inf} is necessary. For the total system Y cap (CisoP + CisoN), approximate V'(t) at t_0 with two adjacent ADC measurements. Then Ciso is:

$$Ciso = \frac{\tau}{RisoP \,||\, RisoN \,||\, RsP + R1 \,||\, RsN} \quad (12)$$

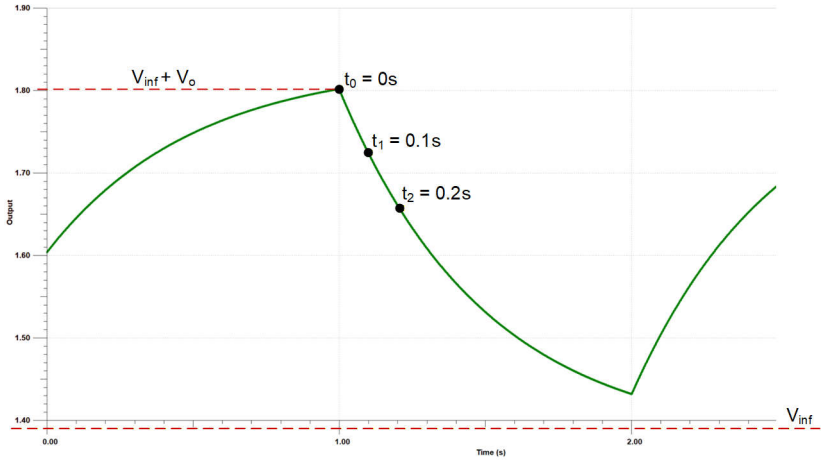


Figure 2-6. Example Voltage Decay Curve With ADC Samples Used for Prediction Algorithm

A similar analysis can be done for the charging curve. The calculation for the final steady state voltage V_{inf} is:

$$V_{inf} = V(t_0) + \frac{V(t_0)^2 - 2 \times V(t_0) \times V(t_1) + V(t_1)^2}{-V(t_0) + 2 \times V(t_1) - V(t_2)} \quad (13)$$

The MATLAB script used to solve for the system of equations is:

```
%% charging solution
clc
syms vt0 vt1 vt2 vi v0 x
eq1 = vt0 == vi;
eq2 = vt1 == vi+ v0×(1-x);
eq3 = vt2 == vi+ v0×(1-xxx);
eq4 = vt0 ~= vt1;
eqns = [eq1, eq2, eq3, eq4];
%
[svi, sv0, sx, para, conditions] = solve(eqns,[vi, v0, x],ReturnConditions=true)
```

One important consideration is knowing when to apply the prediction algorithm. If the voltage has a fast settling time, avoid using the prediction algorithm. Waiting a little longer in time before solving for Riso or Ciso is more practical. Currently, the software does some basic checks based on the voltage time derivative (normalized by the Vbus voltage) to set a threshold for prediction mode. This method does require some tuning with known loads to provide a reliable operation. These are the possible operating modes in the code:

- **#define** SETTLED_MODE
- **#define** DECAY_MODE
- **#define** CHARGE_MODE
- **#define** OUT_OF_RANGE_MODE

2.2.5 Understanding Error Sources

The MSPM0G3507 only supports fixed-point math, and thus some consideration of number overflow is required to minimize error and loss of precision. The current code is optimized to maintain precision and accuracy where most important, near the fault and warning thresholds. Users can avoid this challenge by switching to an MCU with floating-point math support.

Component tolerances are specifically chosen to meet the design target accuracy. Some passives such as the RES60A resistors have a maximum absolute tolerance of 15%, affecting measurement accuracy when the Riso is in the MΩ range. However, this is not important since the highest accuracy closer to the fault trip point of 100Ω/V is desired. For a 1kV bus, that is 100kΩ. At this level, the RES60A tolerance is not significant for a 5% accuracy target. However, the equivalent resistance reading must be compensated for the paralleling of RES60A and other resistances.

So far, the IMD is assumed to work under exceptional conditions without noise, providing a good place to start understanding the fundamental concepts. In practice, TIDA-010985 performance is heavily dependent on how well noise is controlled. These are the steps to help mitigate noise for this design:

- Hardware filtering to limit input noise
- Follow PCB layout guidelines to optimize SNR
- ADC hardware averaging (default is set to 128)
- Software averaging of multiple ADC readings or predictions to estimate the steady-state voltage. For non-prediction-based IMD calculations, the software averages 50 adjacent ADC samples to estimate the settled voltage.
- For prediction-based IMD calculations, the software averages 330 predictions to estimate the settled voltage (that is, Vp1, Vn1, Vp2, Vn2). Longer time constants create flatter voltage settling curves and decrease prediction accuracy under noisy conditions. As mentioned previously, increasing the time spacing between the three samples can help improve prediction performance.

2.3 Highlighted Products

2.3.1 LP-MSPM0G3507

The LP-MSPM0G3507 LaunchPad™ development kit is an easy-to-use evaluation module (EVM) based on the MSPM0G3507. The device contains everything needed to start developing on the MSPM0G3507 M0+ MCU platform, including onboard debug probe for programming, debugging, and energy measurements. The board includes three buttons, two LEDs (one is an RGB LED) and an analog temperature sensor and light sensor. The device also has a external buffer to show high-speed ADC performance at 4MSPS.

2.3.2 TPSI2240-Q1

The TPSI2240-Q1 is an isolated solid-state relay designed for high-voltage automotive and industrial applications. The TPSI2240-Q1 uses TI's high reliability capacitive reinforced isolation technology in combination with internal back-to-back MOSFETs to form an integrated approach requiring no secondary side power supply.

2.3.3 RES60A-Q1

The RES60A-Q1 is a matched resistive divider, implemented in thin-film SiCr with Texas Instruments' modern, high-performance, analog wafer process. A high-quality SiO2 insulative layer encapsulates the resistors and enables usage at extremely high voltages, up to 1400VDC for sustained operation or 4000VDC for HiPOT testing (60s). The device has a nominal input resistance of RHV = 12.5MΩ, and is available in several nominal ratios to meet a wide array of system needs.

2.3.4 TLV9002-Q1

The TLV900x-Q1 family includes single (TLV9001-Q1), dual (TLV9002-Q1), and quad-channel (TLV9004-Q1) low-voltage (1.8V to 5.5V) operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. These op amps provide a cost-effective option for space-constrained automotive applications such as infotainment and lighting where low-voltage operation and high capacitive-load drive are required. The capacitive-load drive of the TLV900x-Q1 family is 500pF, and the resistive open-loop output impedance makes stabilization easier with much higher capacitive loads. These op amps are designed specifically for low-voltage operation (1.8V to 5.5V) with performance specifications similar to the TLV600x-Q1 devices.

2.3.5 TPSM33620-Q1

The TPSM336xx-Q1 is a 0.6A, 1A, or 2A, 36V input, automotive, synchronous step-down DC/DC power module that combines flip-chip on lead packaging, integrated power MOSFETs, AEC-Q100 qualified inductor and boot capacitor in a compact and easy-to-use package. The small HotRod QFN package enhances the thermal performance, enabling high ambient temperature operation. The spread spectrum helps achieve excellent EMI performance. The device is available in two fixed output voltage options supporting 3.3V and 5V. The devices can be configured for 1V up to 7V output with a feedback divider and operated in auto or forced PWM mode through the MODE/SYNC pin. The device only requires four external components for a 3.3V and 5V fixed output design simplifying PCB layout and design.

2.3.6 TPS7A2033

The TPS7A20 is an ultra-small, low-dropout (LDO) linear regulator that can source 300mA of output current. The TPS7A20 is designed to provide low noise, high PSRR, and excellent load and line transient performance that can meet the requirements of radio frequency and other sensitive analog circuits. Using design techniques, the TPS7A20 offers an ultra-low noise performance without the addition of a noise bypass capacitor. The TPS7A20 also provides the advantage of low quiescent current for battery-powered applications. With an input voltage range of 1.6V to 6.0V and an output range of 0.8V to 5.5V, the TPS7A20 can be used for a wide variety of applications. The device uses a precision reference circuit to provide a maximum accuracy of 1.5% over load, line, and temperature variations.

2.3.7 ISOW1044

The ISOW1044 device is a galvanically-isolated controller area network (CAN) transceiver with a built-in isolated DC-DC converter that eliminates the need for a separate isolated power supply in space-constrained isolated designs. The low-emissions, isolated DC-DC meets CISPR 32 radiated emissions Class B standard with just two ferrite beads on a simple two-layer PCB. Additional 20mA output current can be used to power other circuits on the board. An integrated 10Mbps GPIO channel is available and can help remove an additional digital isolator or optocoupler for diagnostics, LED indication or supply monitoring.

2.3.8 TSM24CA

The TSM24CA is a low-capacitance TVS diode and is part of TI's surge protection device family. The TSM24CA robustly shunts up to 30A of IEC 61000-4-5 (8µs to 20µs) fault current to protect systems from high power transients or lightning strikes. The device offers an answer to the common industrial signal line EMC requirement to survive up to 1kV IEC 61000-4-5 open circuit voltage coupled through a 42Ω impedance, clamping that surge at 40V (IPP = 24A). The TSM24CA also has a very low line capacitance of 12pF allowing protection of common automotive communication networks like CAN from surges in EV charging applications.

2.3.9 TLV431B

The TLV431 device is a low-voltage, 3-terminal adjustable voltage reference with specified thermal stability over applicable industrial and commercial temperature ranges. Output voltage can be set to any value between VREF (1.24V) and 6V with two external resistors. These devices operate from a lower voltage (1.24V) than the widely used TL431 and TL1431 shunt-regulator references.

Note

This voltage reference is optional for the operation of the reference design. By default, the ADC uses VDD as the voltage reference, which is not an issue since the result depends on the ratios of Vp to Vn.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

The hardware used for evaluating this reference design is composed of the following:

- TIDA-010985
- LP-MSPM0G3507
- USB Type-C® cable
- USB isolator (to power the LP and protect the laptop). USB powering the entire system is the default method to evaluate the reference design.
- Laptop
- Four-channel oscilloscope
- Two high-voltage differential probes rated for voltages higher than 1kV
- Two single-ended probes for low-voltage signal measurements (TPP0500B)
- A logic analyzer (Saleae logic 16) for debugging digital signals (optional)
- HV DC power supply SL1250-1.2/UI+LXI
- An interlocked safety box for HV testing safety
- Optional 12V DC lab power supply (5W) if an external power supply is desired instead of the USB source of the LP for power (default option)

3.2 Software

Code Composer Studio™ (CCS) software is required to evaluate the reference design. The example code is found in the TIDA-010985 tool folder. CCS version 12.8.1.00005 is used for this design. When first installing CCS, be sure to check the MSP package during installation.

- MSPM0-SDK version 2.7.0.05 is used for this design. If the SDK is not installed from the CCS installation step, download and install the SDK. An example installation path is: C:\ti\mspm0_sdk_2_07_00_05. Make sure that the linked resource path variables of the project include this SDK path. Configure these settings under Project → Properties → Resources → Linked Resources.

3.3 Test Setup

3.3.1 Hardware Test Setup

Figure 3-1 shows the basic test setup.

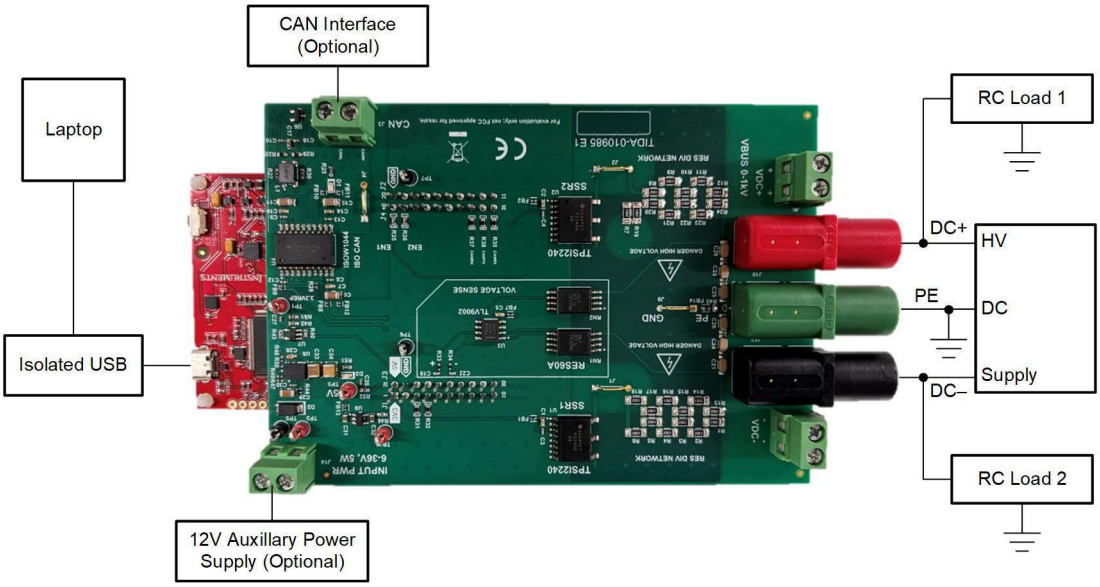


Figure 3-1. Hardware Test Setup

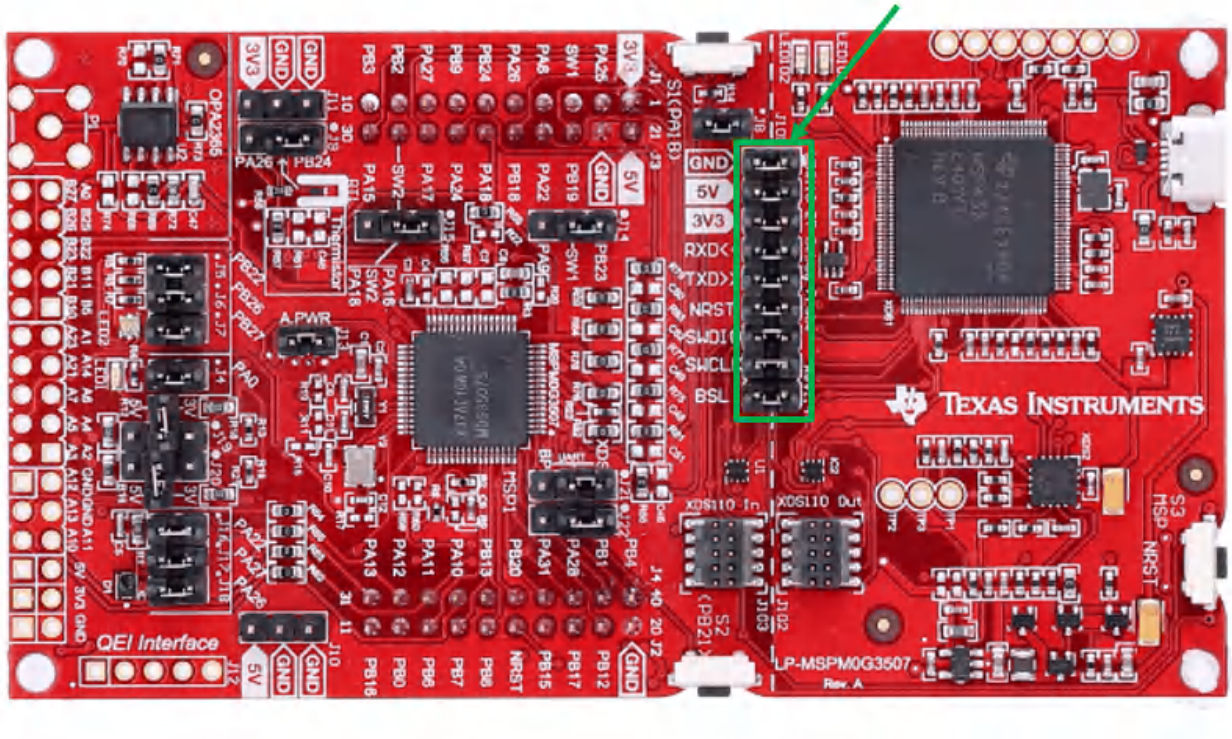


Figure 3-2. LaunchPad™ J101 Default Jumper Configuration

1. Make all required hardware connections as shown in Figure 3-1. Do not energize the HV supply until all connections are secured and placed properly inside the safety box.
2. Connect the target test RC load to the HV connectors. There are a few convenient options for users:
   a. J6 or TP11 for VDC+ connection
   b. J7 or TP10 for VDC– connection
   c. J9 for protected earth (PE) ground. Note that the system ground is tied to the PE.
3. Connect the oscilloscope probes to the desired SW_EN pins (J13 pins 39 and 40) and ADC input pins (J5 pins 25 and 27) to debug the board
4. Connect the HV differential probes to the HV connectors for debugging, if needed
5. Import the demonstration project and start CCS software debug mode
6. Turn on the HV power supply and observe the waveforms and the calculated resistance and capacitance values

Note

To use the external DC power supply (input to J14 of the TIDA-010985 board) to power the reference design, R52 and R46 must be shorted, and the jumpers on J101 the LP device must be removed (all except for GND, SWDIO, and SWCLK for the debugger to work).

3.3.2 Software Test Setup

1. The example demonstration project is found on the TIDA-010985 tool folder. CCS Version: 12.8.1.00005 is used for this design. Install CCS and MSPM0 SDK, if not already done.
2. Download and import the demonstration project
3. Start CCS software debug mode
4. Check the continuous refresh option for the CCS watch window
5. Add variables to the watch window to observe measurements, for example, gRn, gRp. gRn and gRp are compensated values based on the two 12.5MΩ RES60A resistors in parallel with RP and RN. For the effective RP and RN, add "rn" and "rp" to the watch window.

6. If changing the default settings of the ADC such as the timing and hardware averaging is desired, modify the syscfg file in the project. By default, the two ADCs (ADC0 and ADC1) sampling periods are set to 1ms, and the number of hardware averages is set to 128 conversions (Figure 3-3 through Figure 3-5). Note that the hardware averaging helps with reducing the noise effect on measurement. For more information on how to properly change the IMD cycling time, see the *Prediction Algorithms* section.

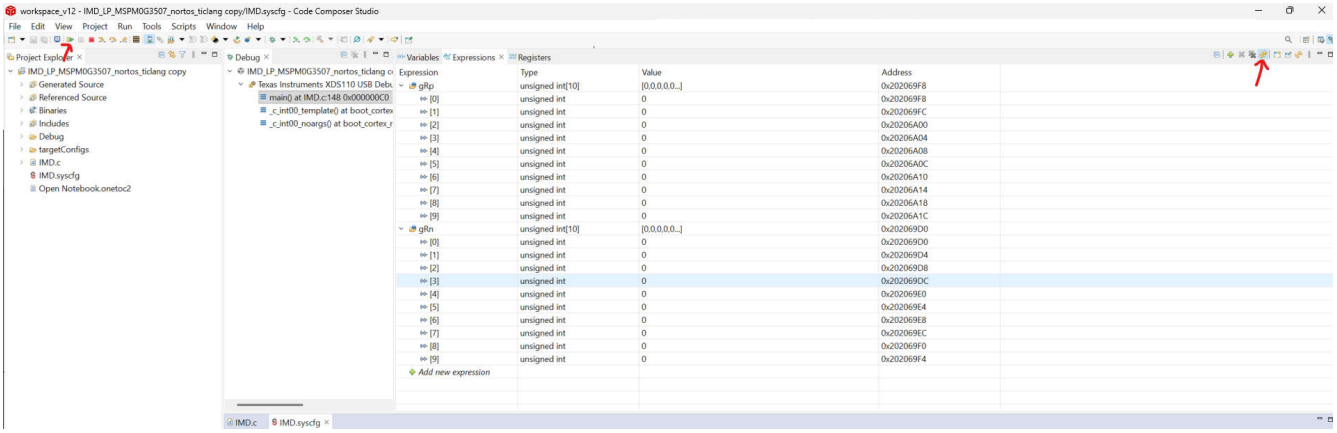


Figure 3-3. CCS Expression Watch Window Running on Continuous Refresh Mode During a Debug Session

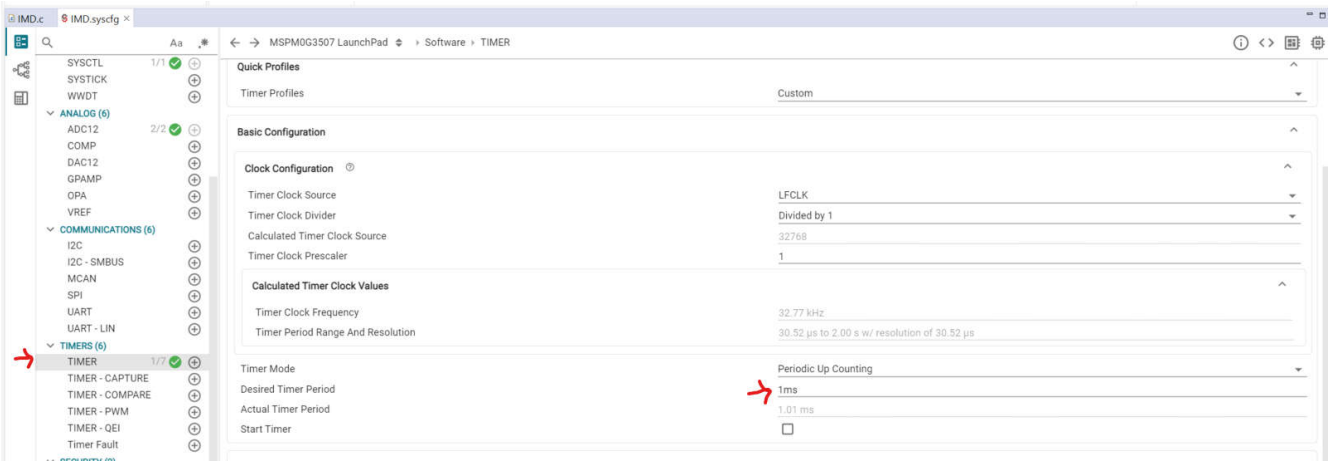


Figure 3-4. syscfg Timer Period Setting

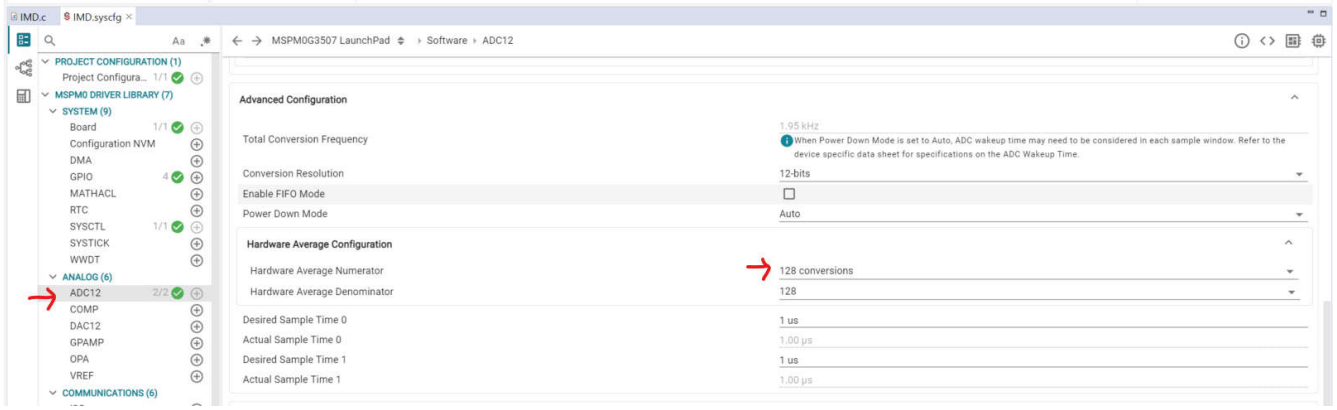


Figure 3-5. syscfg ADC Hardware Averaging Setting

3.4 Test Results

Each test condition includes ten IMD measurements for statistical analysis (mean and standard deviation). Fixed-point math error is significant in some cases. Overall, the measurement errors and response time are well below the UL 2231-2 requirements (±15%, 10 seconds).

In Figure 3-6, for asymmetric faults, the error displayed is the Riso in the fault condition. The "1MΩ-1MΩ" case requires a 3s cycle to resolve due to a very large time constant.

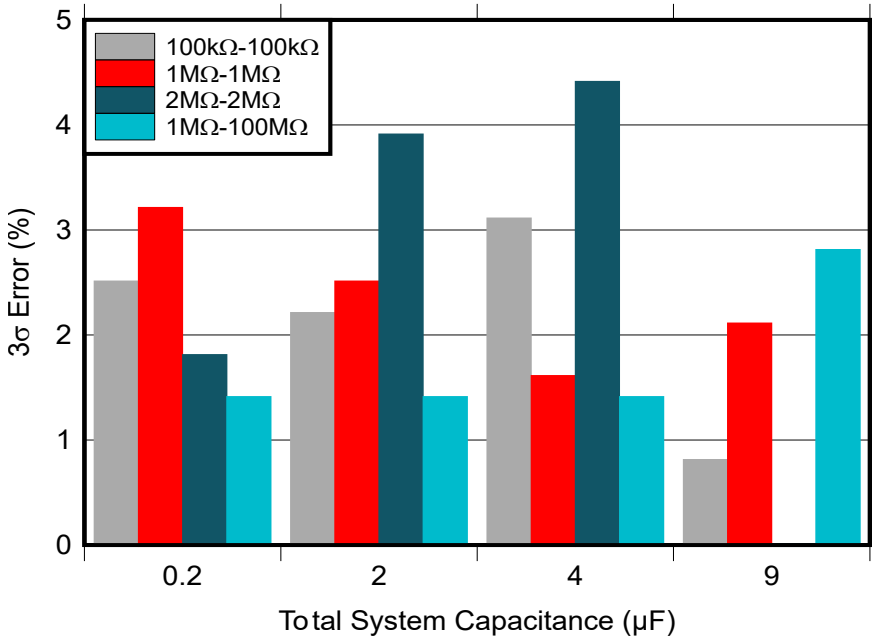


Figure 3-6. IMD Riso Measurement Error, 1000VDC, 2s Cycle

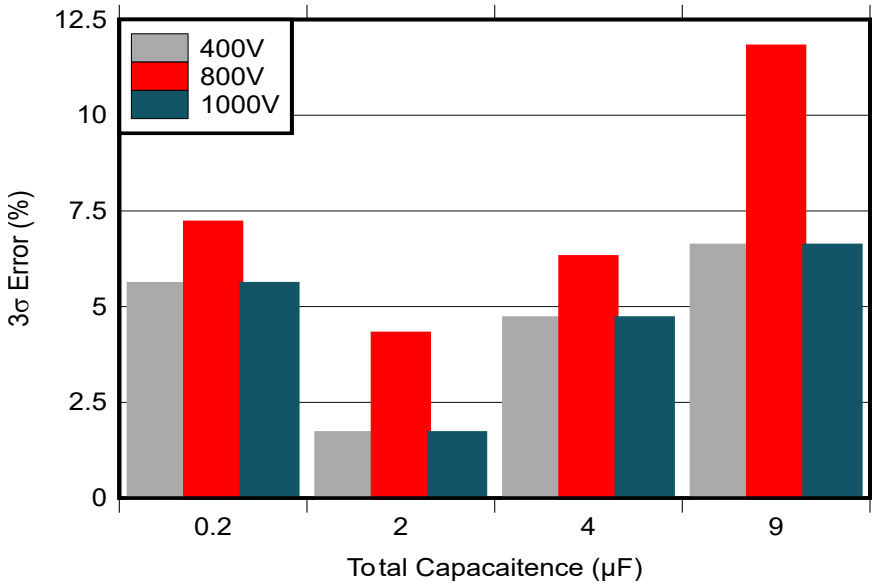


Figure 3-7. IMD Ciso Error, 1MΩ to 100kΩ, 2s Cycle

In Figure 3-8, the relatively short time constant means that prediction for the final steady-state voltages is not necessary.

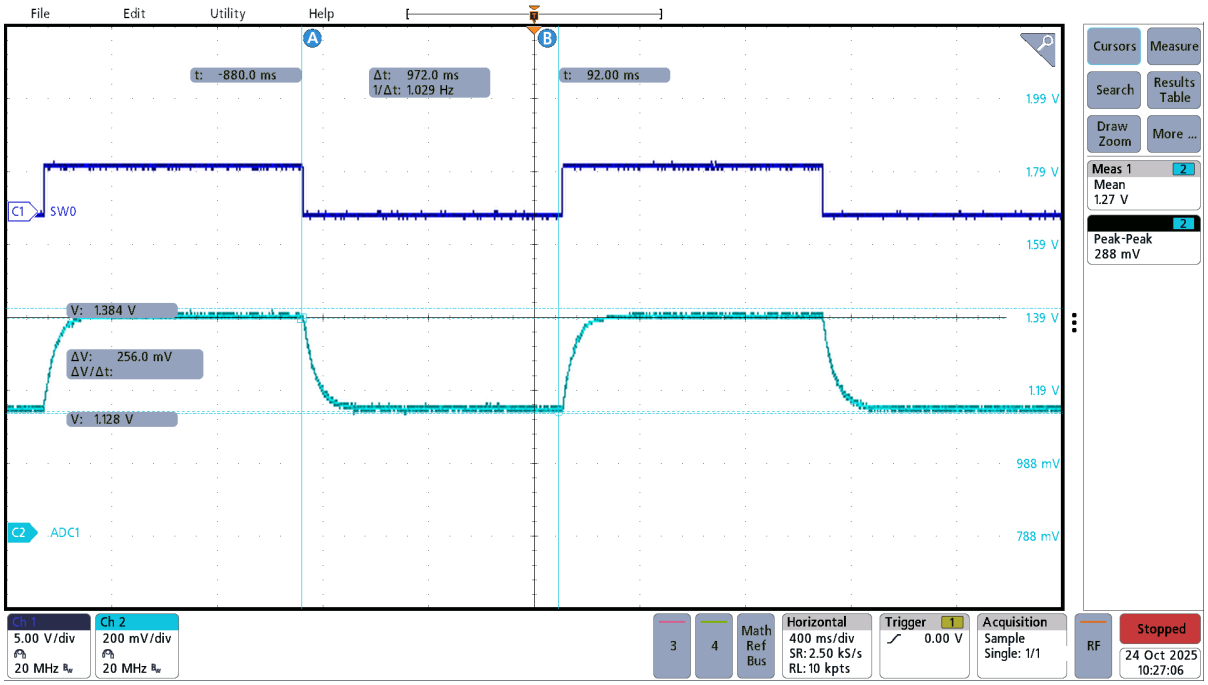


Figure 3-8. Switching Waveform Capture for 800VDC, 0.1µF, 1MΩ Symmetrical Condition

In Figure 3-9, the relatively long time constant means that prediction for the final steady-state voltages is necessary.

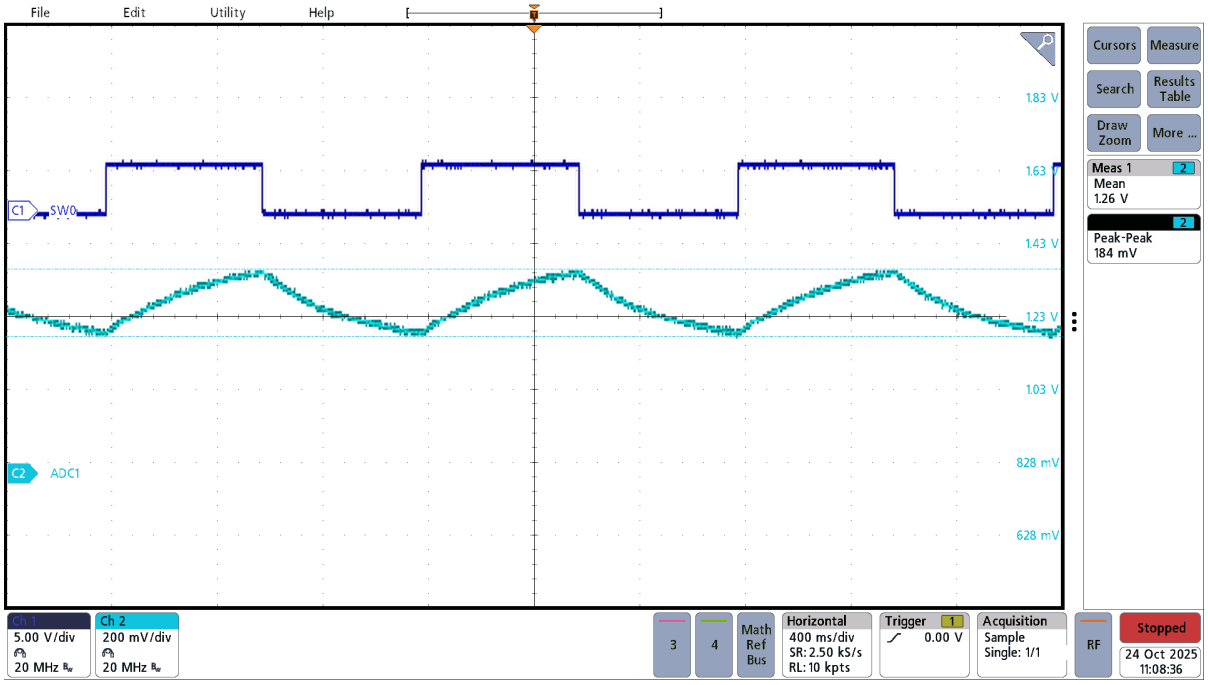


Figure 3-9. Switching Waveform Capture for 800VDC, 1µF, 1MΩ Symmetrical Condition

Figure 3-10 shows the switching timing diagram. Note that each switch state stays on for about 980ms. The ADC sampling period is about 1ms. The computation time after the ADC acquisition period is about 1.98ms.

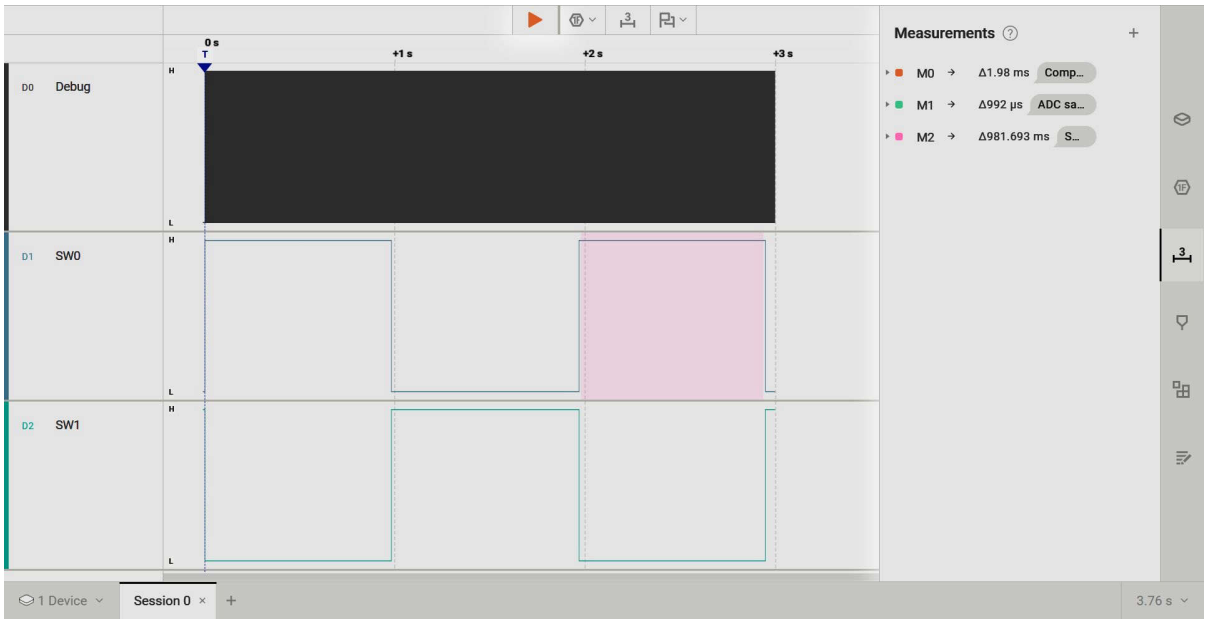


Figure 3-10. Switching Timing Diagram

Figure 3-11 shows a computation time of about 2ms, which includes all of the math computations such as prediction and solving for the unknowns.

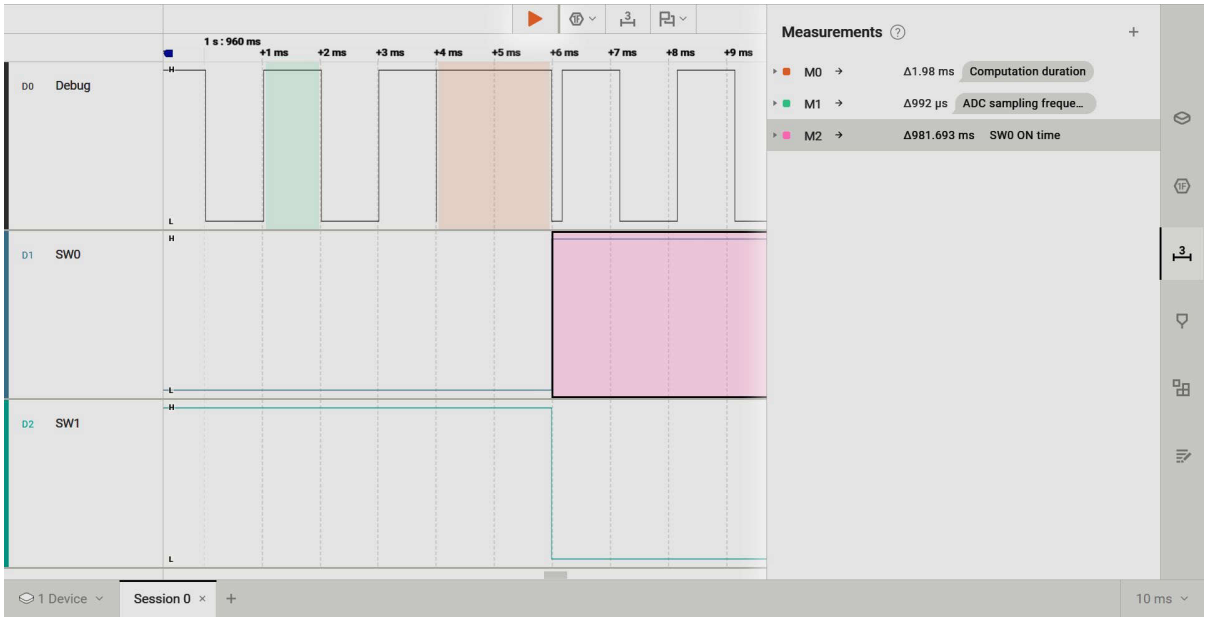


Figure 3-11. Zoomed-in Timing Diagram

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010985.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010985.

4.1.3 PCB Layout Recommendations

The PCB layout can vary depending on specific design requirements such as the isolation rating and the components selected for the design.

- In general, reference the individual device guidelines in the datasheet for device-specific layout recommendations.
- For HV system designs, clearance and creepage rules are an important factor when laying out the PCB. Pollution degree, working voltage, material properties, and other environmental factors (for example, altitude, and humidity) can affect the specific design creepage and clearance requirements. These are typically specified in standards such as IEC-61851-1 and UL-2202.
- To minimize noise coupling, avoid routing digital and analog signals close together. Having proper ground planes, shields, minimal signal loop areas, and filters can help keep noise under control.
- TIDA-010985 is an example AFE reference design that works with a TI LaunchPad in the spirit of modularity. In the best circumstances, place the MCU ADC on the same PCB as the AFE to minimize trace length, which improves the performance of the system.

4.1.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010985.

4.2 Tools and Software {Required Topic}

Tools

CCSTUDIO	Code Composer Studio™ integrated development environment (IDE)
MSPM0-SDK	MSPM0 software development kit (SDK)

Software {if applicable}

Software	Descriptive text

4.3 Documentation Support

1. Texas Instruments, *AFE for Insulation Monitoring in High-Voltage EV Charging and Solar Energy Reference Design Guide*
2. Texas Instruments, *TPSI2240-Q1 1200V, 50mA, Automotive Reinforced Solid-State Relay With Avalanche Protection Data Sheet*
3. Texas Instruments, *RES60A-Q1 Automotive, 1400V_{DC}, Precision Resistive Divider Data Sheet*
4. Texas Instruments, *MSPM0G3507 LaunchPad Development Kit (LP-MSPM0G3507) User's Guide*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2025) to Revision A (January 2026)	Page
• Updated block diagram to support TPSI2240-Q1 device	1
• Updated *Insulation Monitoring Device in DC Unearthed Distribution Systems*	2
• Updated *Block Diagram* to support TPSI2240-Q1 device	5

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Last updated 10/2025