Design Guide: TIDA-010237

AC and DC Residual Current Fault Detection Reference Design

Description

This reference design detects milliampere-level AC and DC ground fault currents for residual current detection (RCD) and ground fault current interrupters (GFCI), targeted to meet timing and accuracy requirements for UL2331-2 and IEC62752. A DRV8220 H-bridge that drives the magnetic core in and out of saturation created an auto-oscillation circuit. An active filter circuit identifies fault current signal and level. A set of resistor-adjustable window comparators provide a digital fault output.

Resources

TIDA-010237	Design Folder
DRV8220	Product Folder
INA600	Product Folder
OPA4383	Product Folder
INA293	Product Folder
SN74LVC2G74	Product Folder
TLV7011	Product Folder
TLV9022L	Product Folder

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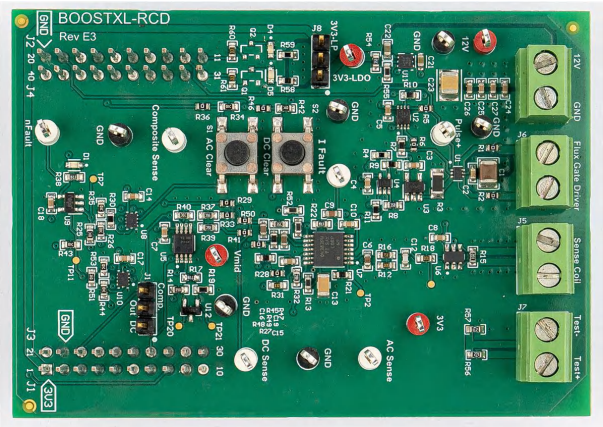
Features

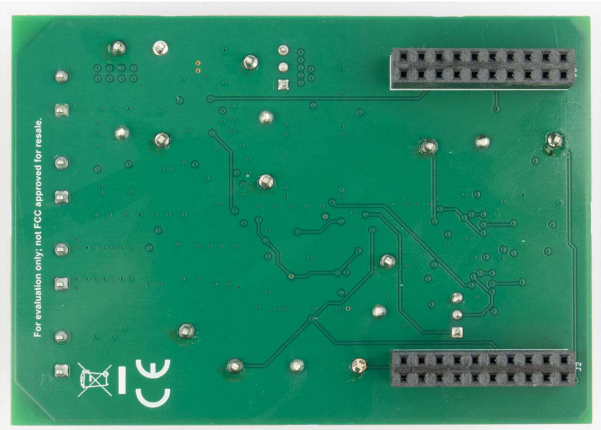
- Low-cost discrete AC and DC ground fault detection circuit
- leakage current sensing thresholds of 6mA to 30mA DC, and $5mA_{RMS}$ to $30mA_{RMS}$ AC to enable testing to UL2231, IEC62752 and IEC62955
- Detection-to-response time of 3-50ms (not including relay delay time)
- Adjustable AC and DC trip thresholds
- Auto-oscillation feedback circuit can drive different magnetic core materials with minimal changes to hardware
- Active low-pass filter optimized to attenuate auto-oscillation frequency and amplify fault current signal

Applications

- AC charging (pile) station
- DC fast charging station
- Onboard charger
- GFCI/RCD circuit breaker
- Central inverter



Top of Board



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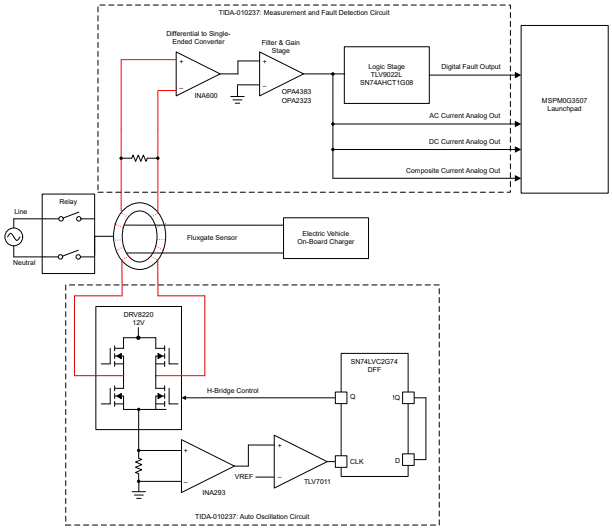

Block Diagram

1 System Description

Electric vehicles (EVs) receive energy from the electrical grid through electric vehicle supply equipment (EVSE), more commonly known as EV chargers. To facilitate power delivery to the vehicle, the EVSE sits between the grid and the vehicle.

If a ground fault occurs, the EVSE must respond and trip a relay to disconnect power from the grid. The primary requirement in providing protection during EV charging is the ability to detect AC and DC residual currents and mitigate the risk of electrical shock. This system implements residual current detection (RCD) by monitoring the phase lines and neutral wires through a fluxgate sensor. During normal operation without a fault condition, the sum of currents equals zero. During a ground fault condition, the sum of currents is not equal to zero. This residual current indicates a system short which can be an issue at 6mA DC and 30mA$_{RMS}$ according to IEC62752 and IEC62955.

The need to measure AC and DC residual currents extends beyond EVs. Solar, smart circuit breakers, and other applications where there are DC loads or supplies can require residual current detection.

1.1 Key System Specifications

PARAMETER	NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT	DETAILS
INPUT CHARACTERISTICS						
Line Frequency	Line through fluxgate sensor		60, 50		Hz	
Phase Line Voltages			Universal		V	
Phase Line Current			Universal		A	
TRIP THRESHOLDS						
Residual DC Current Threshold			6		mA	Adjustable through the resistors
Residual AC Current Threshold			30		mA$_{RMS}$	Adjustable through the resistors
POINT-OF-LOAD CHARACTERISTICS						
Board positive supply voltage			+12		V	Provided by external power supply
Fluxgate sensor drive voltage	DRV8220		+12		V	H-bridge voltage to drive fluxgate sensor into saturation

2 System Overview

2.1 Block Diagram

Figure 2-1 shows an overview of connections between the fluxgate sensor, filtering circuit, fault detection circuit, and auto-oscillation circuit.

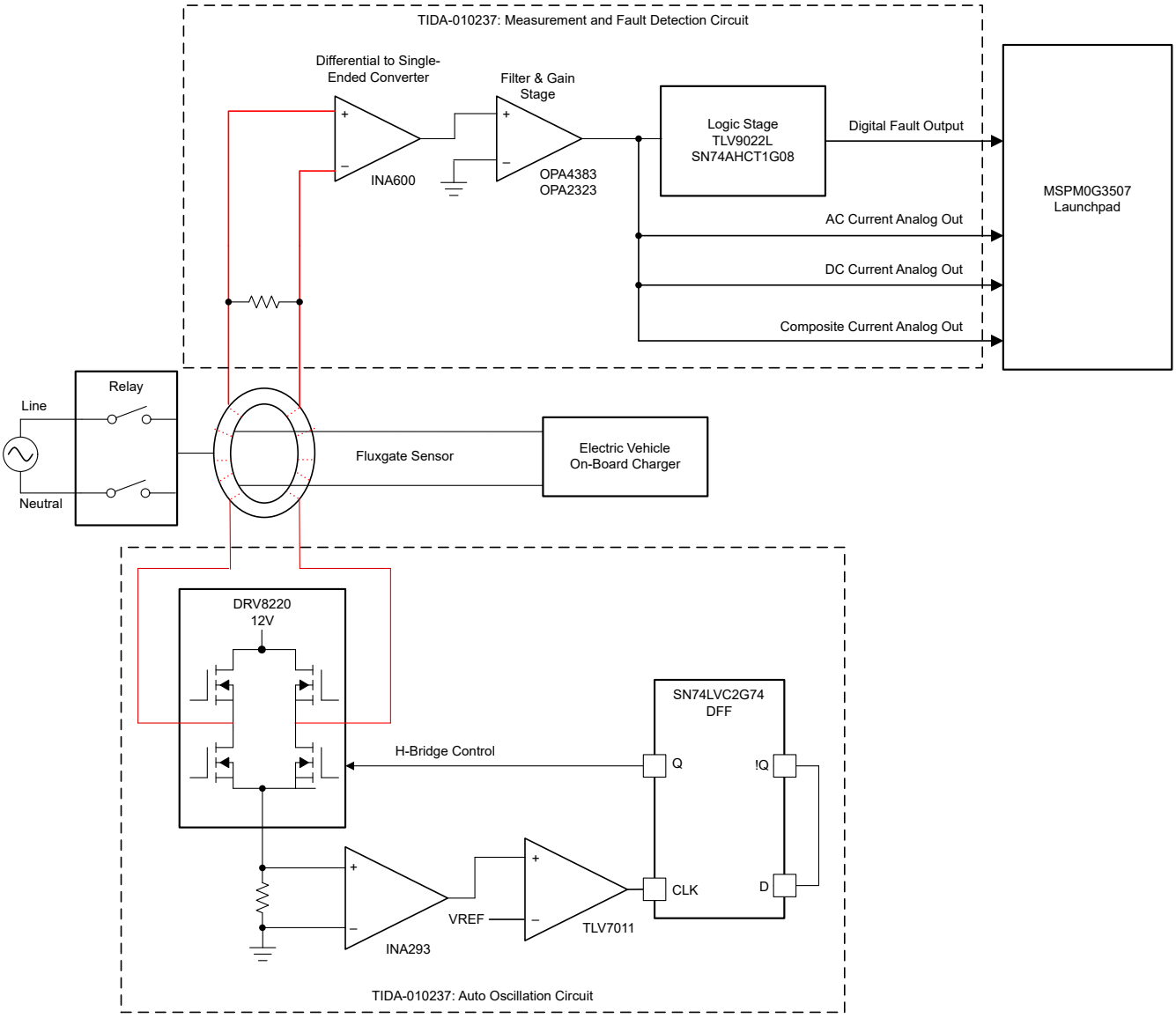

Figure 2-1. Block Diagram

2.2 System Design Theory

2.2.1 Detection Principals

If the current leaving the grid does not equal the current returning, there is a ground fault. This current is traveling somewhere unintended; therefore, risking fires or shock.

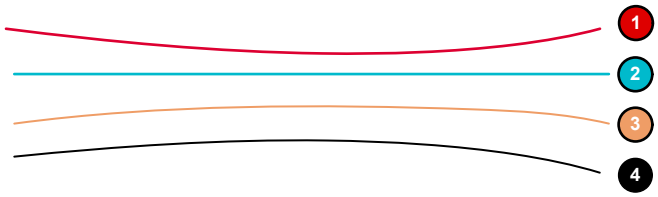

Figure 2-2. Phase Lines and Neutral

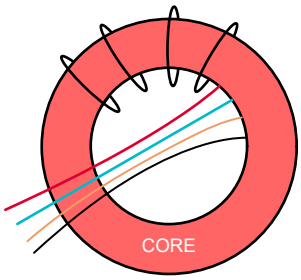

Figure 2-3. Fluxgate Sensor Frontal View

Under normal conditions:

$I_{TOTAL} = I_1 + I_2 + I_3 + I_4 = 0A$

During a ground fault condition:

$I_{TOTAL} = I_1 + I_2 + I_3 + I_4 \neq 0A$

For a DC fault condition: $|I_{TOTAL}| > 6mA$

For an AC fault condition: $|I_{TOTAL}| > 30mA_{RMS}$

Note

The threshold values of 6mA and $30mA_{RMS}$ are adjustable through resistors.

2.2.2 Saturation

Saturation is a state reached when an increase in applied magnetizing *field H* cannot increase the magnetization of the material further, so the total magnetic *field B* levels off. As the H field increases, the B field approaches a maximum value asymptotically, the saturation level for the substance. The magnetic field represents the existing current through a conductor. From this idea, the excited saturable inductor is able to measure current.

The saturation point of ferromagnetic materials depends on magnetic permeability and the amount of current. The core permeability changes both by an external field and an excitation current through the coils wrapping the sensor.

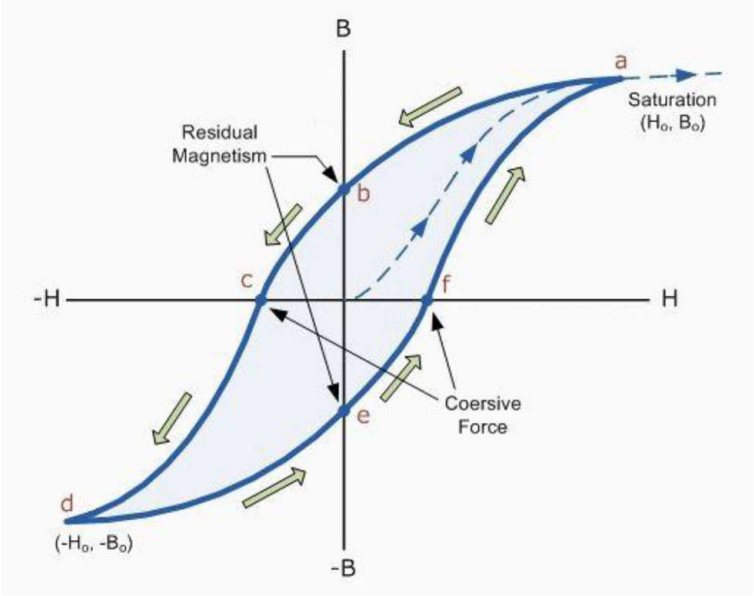

Figure 2-4. Magnetization Curve and B-H Curve

2.2.3 General Mode of Operation

Current through a wire produces a magnetic field. Explained in Detection Principals section, a ground fault produces a magnetic field. Average voltage across the fluxgate burden resistor changes proportional to the ground fault magnetic field. This average voltage is filtered and read to determine if there is a ground fault.

The core is driven into saturation with a driver circuit. Once reaching saturation, the driver circuit switches the direction of the current until the core reaches saturation again. The drive circuit continuously switches the drive current direction every time the core reaches saturation. Prior to saturation, the ambient field is channeled through the core producing a high flux due to the high permeability. At the point of saturation, the core permeability falls away to the vacuum. During the next half cycle of excitation drive current, the core recovers from saturation, and the flux due to the ambient field is once again at a high level until the core saturates in the opposite direction; the cycle then repeats.

2.3 Highlighted Products

2.3.1 DRV8220

The DRV8220 is an integrated H-bridge driver with multiple control interface options: PWM (IN1, IN2) interface, PH, EN,or half-bridge interface. To reduce area and external components on a printed circuit board, the device integrates a charge pump regulator and the capacitors.

The integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), overcurrent protection (OCP), and overtemperature shutdown (TSD).

2.3.2 TLV7011

The TLV701x and TLV702x devices are single-channel, micro-power comparators with push-pull and open-drain outputs. Operating down to 1.6V and consuming only 5µA, the TLV701x and TLV702x are designed for portable and industrial applications. The comparators are available in leadless and leaded packages to offer significant board space savings in space-challenged designs.

2.3.3 INA293

The INA293 is a high- or low-side current-sense amplifier that offers a wide common-mode range, precision zero-drift topology, excellent common-mode rejection ratio (CMRR), high bandwidth, and fast slew rate. Different gain versions are available to optimize the output dynamic range based on the application. The device is designed using a transconductance architecture with a current-feedback amplifier that enables low bias currents of 20µA with a common-mode voltage of 110V.

2.3.4 SN74LVC1G74

This single positive-edge-triggered D-type flip-flop is designed for 1.65V to 5.5V V_{CC} operation.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully-specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when powered down.

2.3.5 OPAx383

The OPA383, OPA2383, and OPA4383 (OPAx383) family of precision amplifiers offers state-of-the-art performance. With zero-drift technology, the OPAx383 offset voltage and offset drift provide unparalleled long-term stability. With a ultra-low 65µA of quiescent current, the OPAx383 are able to achieve 2.5MHz of bandwidth, a broadband noise of 32nV/√Hz, and a 1/f noise at 650nVPP. These specifications are crucial to achieve extremely-high precision and no degradation of linearity in 16-bit to 24-bit analog to digital converters (ADCs). The OPAx383 feature flat bias current over temperature; therefore, little to no calibration is needed in high input impedance applications over temperature.

2.3.6 INA600

The INA600 is a voltage-sensing difference amplifier with precision matched resistors that offer attenuating gain options. The precision matched integrated resistors saves BOM costs and board space by removing the need for precise and low tolerance external resistors.

The INA600 offers high input impedance of >1MΩ and low quiescent current of 65µA. The device can handle up to –40V to +85V of input voltage, attenuate the voltage down with great accuracy, and interface the voltage to the low voltage ADC while rejecting any common-mode errors such as ground bounce, switching ripples, AC mains and so forth. The device achieves a maximum gain error of ±0.05%, and a maximum gain drift of 5ppm/°C along with 89dB of minimum common-mode rejection ratio (G = 1/5).

2.3.7 TLV9022L

The TLV902xL and TLV903xL are a family of single and dual channel latching comparators. The family also offers low input offset voltage, power on reset (POR), and fault-tolerant rail-to-rail inputs. These devices have an excellent speed-to-power combination with a propagation delay of 110ns with a quiescent supply current of only 22µA per channel.

The unique feature of the TLV90xxL is the output latching capability. The output latches upon the first threshold crossing, allowing capture of an event or error condition without the full attention of a system controller. This feature allows events to be captured at start up while the system controller is still initializing or busy with other tasks. The falling-edge triggered clear input allows system controller to reset the latch after performing any needed tasks and meets safety-critical requirements. The L1 and L2 options define power-up latching behavior.

These comparators also feature fault-tolerant inputs that can go up to 6V without damage with no output phase inversion. This feature makes this family of comparators designed for precision voltage monitoring in harsh, noisy environments.

The TLV902xL have an open-drain output that can be pulled up below or beyond the supply voltage, designed for ORing multiple outputs or level translation. Latching occurs on the high to low output transition. The TLV903xL have a push-pull output stage capable of sinking and sourcing up to 85mA to drive a capacitive load such as a MOSFET gate. Latching occurs on the low to high output transition.

2.3.8 TLV431B

The TLV431 device is a low-voltage 3-terminal adjustable voltage reference with specified thermal stability over applicable industrial and commercial temperature ranges. Output voltage can be set to any value between VREF (1.24V) and 6V with two external resistors. These devices operate from a lower voltage (1.24V) than the widely used TL431 and TL1431 shunt-regulator references.

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware

3.1.1 Board Overview

The TIDA-010237 is in a BoosterPack™ Plug-in Module form factor to connect to a MSPM0 LaunchPad™ Development Kit. Figure 3-1 shows the top side of the reference design board, measuring 6cm × 8.5cm, and highlights the AC/DC detection and oscillator subsystems.

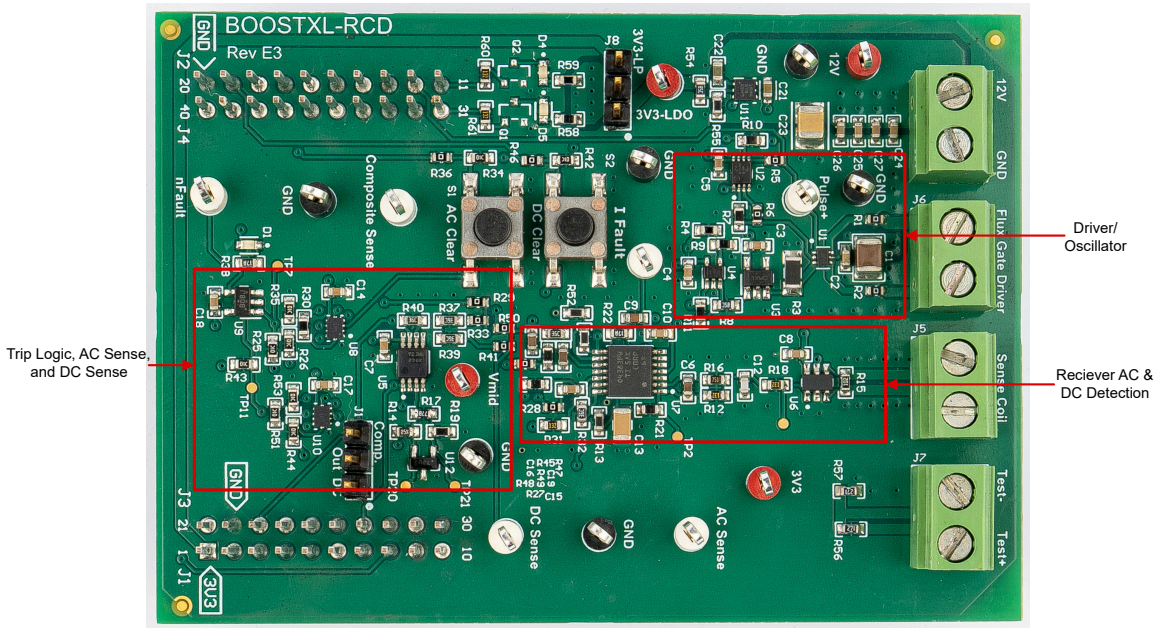

Figure 3-1. Subsystem Location on Board Hardware

Figure 3-2 highlights the connections for both the power supply, sensor, and test inputs to the board. The terminal header J4 is a connection for an external +12V and GND power supply.

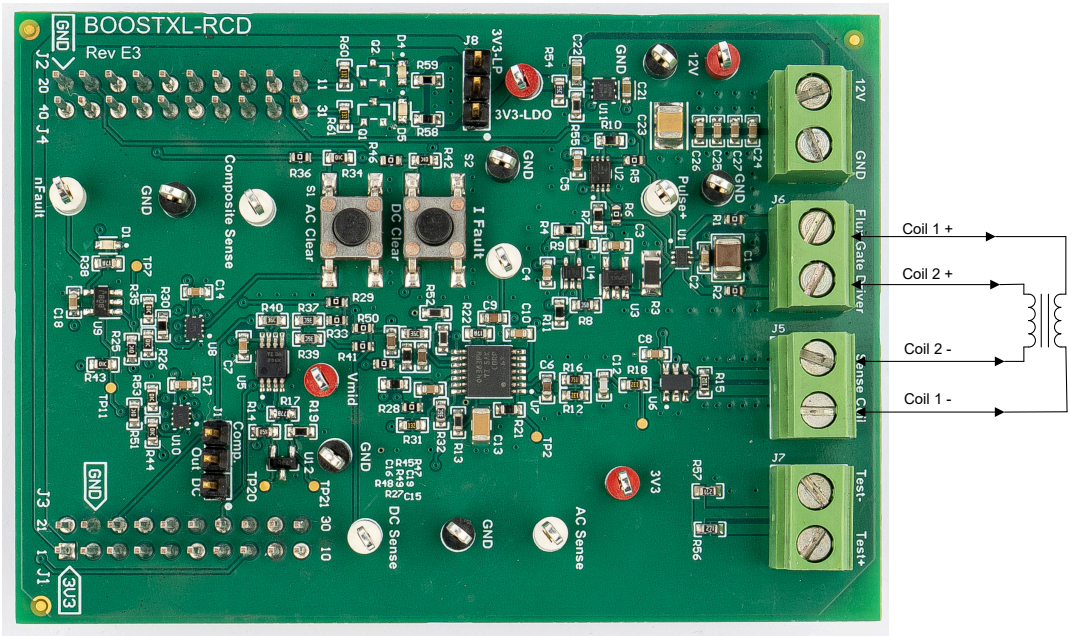

Figure 3-2. Power Supply and Sensor Board Connections

Connector J5 and J6 are for connecting the driving coil on the nanocrystalline core fluxgate sensor. J6 connects one side of the two drive coils to the DRV8220 outputs. J5 connects the other side of the drive coil to a 1kΩ sense resistor of the receive detection circuit. J7 connects to the test inputs. Test+ has a resistor to Test– that can be used for AC testing. Test– also has a resistor to ground for DC testing.

3.1.2 Filter Stage

The goals of filter stage are to gain the ground fault detection signal for both AC and DC and filter out the noise created by the auto-oscillation circuit.

Noise in the signal path needs to be filtered. Too much noise can trigger false trips. The major source of noise is switching caused by the auto-oscillation circuit generating switching of the DRV8220. The auto-oscillation switching frequency changes with fluxgate sensor permeability, burden resistance, or adjusting the saturation detection circuit. The nanocrystalline cores used for testing ranged from 600Hz to 800Hz with a 1kΩ burden resistor and two sets of 100 turns.

During a fault, the filter stage outputs a detectable signal that can be read by an ADC. There are three different filtered outputs. One for AC ground faults, one for DC ground faults, and a combined output with the AC and DC ground fault signals added together. The combined output is a weighted combination of AC and DC signals to enable composite trip levels as defined in UL2332-2.

There is a window comparator to provide a digital fault output when the AC, DC, or composite fault signals passes a predetermined threshold. There are two window comparators, one for AC and another that can be for DC or composite depending on the position of the jumper on J1. Window comparator faults are latching, so the design also includes buttons to clear the fault and retest without powering down the board. The outputs of each window comparator are inputs to an AND gate. The output of this AND gate is high with no fault, and low with a fault present.

In this design, a DC fault of 6mA outputs a 130mV offset. An AC fault of 30mA$_{RMS}$ outputs a peak-to-peak of 2.86V centered at 1.65V. The gain can be increased, make sure the trip threshold is below the rail of op amps.

Filter stage is designed to gain the fault signal and attenuate frequencies above 70Hz. Figure 3-3 highlights the receiver circuit that consists of a differential to single-ended converter, active low-pass filter, and active high-pass filter.

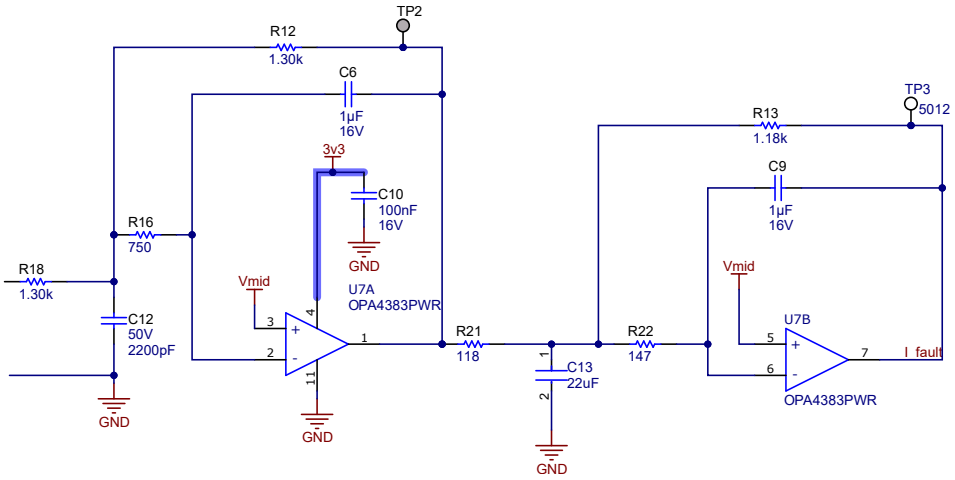

Figure 3-3. Filter Stage Schematic

The filter topology used is the MFB topology (sometimes called infinite gain or Rauch) and is often preferred due to low sensitivity to component variations. The MFB topology creates an inverting second-order stage. This inversion can be a concern in the filter application. The MFB filter circuit can be configured as a low-pass filter, high-pass filter, or band-pass filter based on the component selection. For this application, a fourth-order low-pass filter with a Butterworth response was used.

3.1.3 Differential to Single-Ended Converter

The first part of the signal chain performs the differential to single-end conversion. The INA600 attenuating difference amplifier converts the differential signal across the fluxgate burden resistor to a single-ended signal. This conversion simplifies later signal conditioning and allows an ADC to read a ground referenced signal. R15 is the burden resistor across the coils of the fluxgate sensor.

Impedance matching to op amp inputs is important to minimize error. Mismatched impedance adds error to the fault detection signal. Use similar trace from R15 to U6 to reduce error.

A higher impedance relative to the burden resistor (R22) gives a higher ground fault signal due to the resistor divider effect. The INA600 has an input impedance of >1MΩ.

The first filter stage in Figure 3-4 is used to convert the differential signal across the burden resistor to a single-ended signal. These interface between the burden resistor (R22) of the fluxgate sensor and the TIDA-010237.

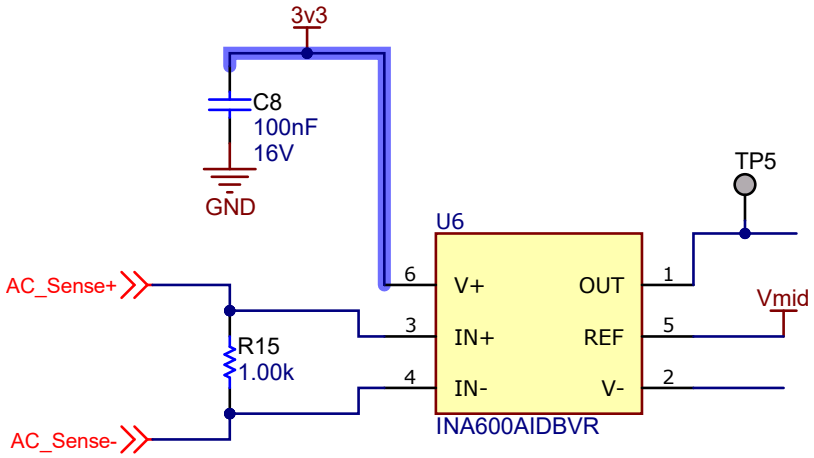

Figure 3-4. Differential to Single-Ended Schematic

3.1.4 Low-Pass Filters

The low-pass filter is optimized to attenuate auto-oscillation frequencies. The goal is to reduce noise to prevent false trips. For DC signal, TI's Webench™ Filter Designer was used to create a single ended Sallen and Key lowpass filter with butterworth response. The gain can be adjusted with R47 and R52. The cutoff frequency is 10Hz. The attenuation is –50dB at 600Hz.

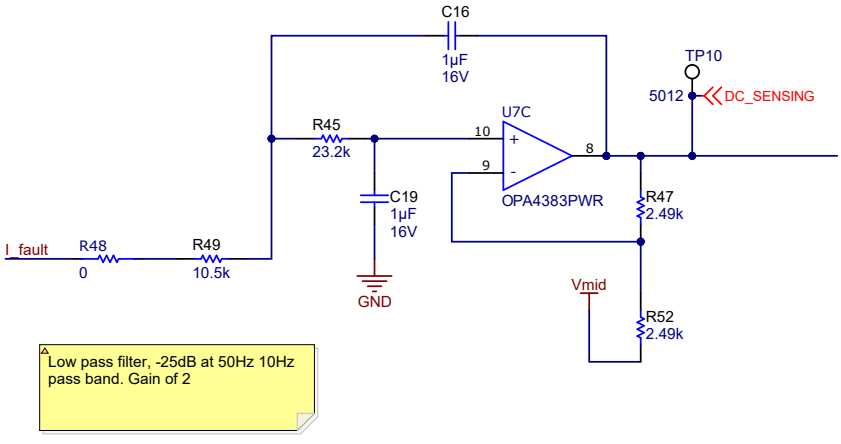

Figure 3-5. Low Pass Filter

The AC signal is AC coupled with a high pass filter to isolate the signal from the DC offset. Also, an adjustable gain and single pole low pass filter with 70Hz cutoff for reducing the auto oscillation ripple is included.

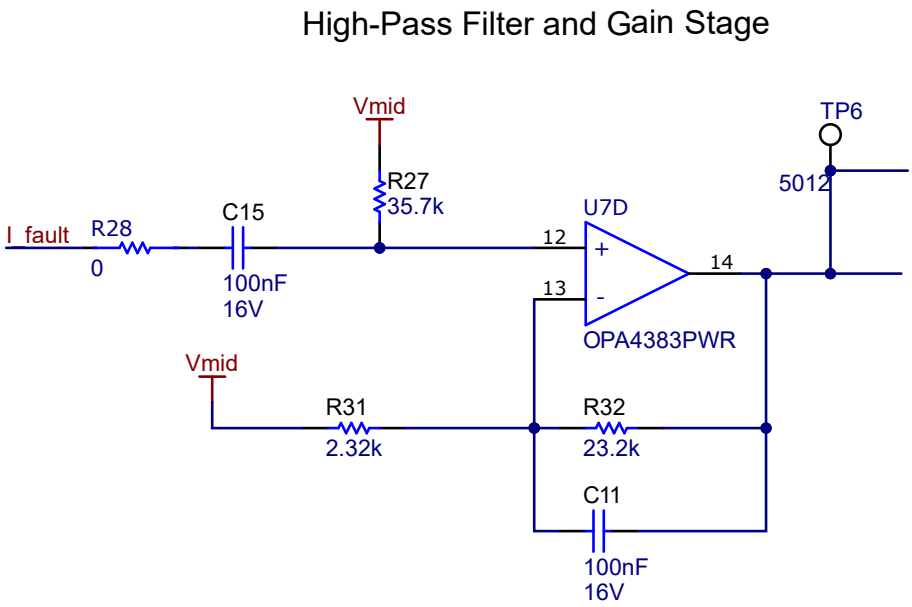

Figure 3-6. High-Pass Filter Schematic

3.1.5 Auto-Oscillation Circuit

The Auto-Oscillation sub-circuit detects when the fluxgate sensor reaches saturation then reverses the current direction. When saturation is reached, current sense voltage exceeds the comparator threshold, which causes the D-type flip-flop to flip control signals to the DRV8220 H-bridge. This flipping drives the fluxgate sensor core to saturation in the opposite direction.

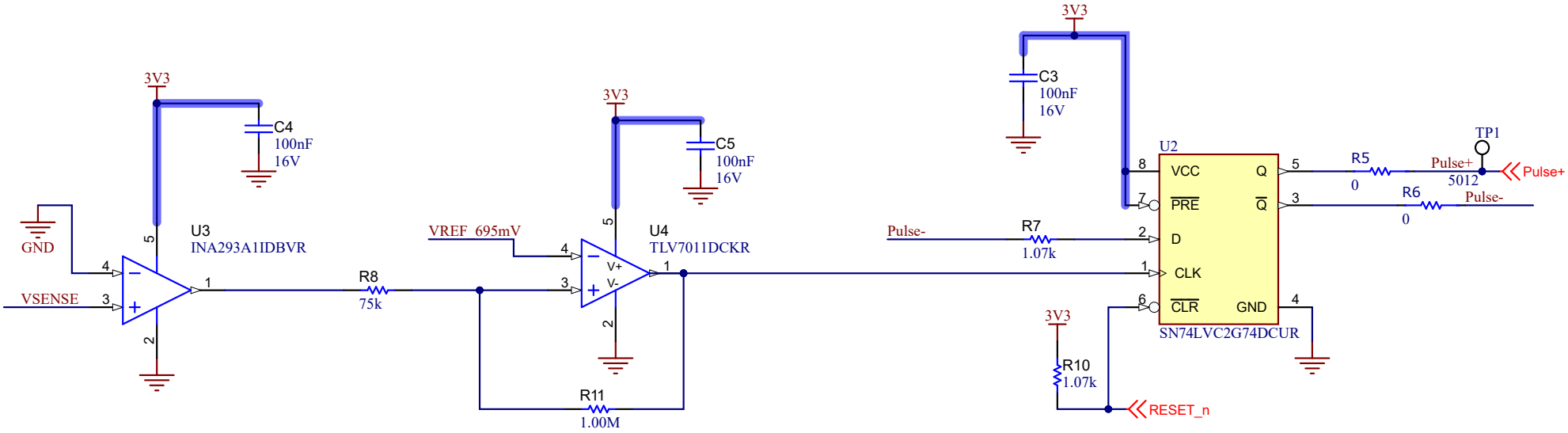

Figure 3-7. Auto-Oscillation Circuit Schematic

This circuit monitors the current flowing through the fluxgate and reverses drive current direction once saturation is reached. The auto-oscillation circuit is needed to detect DC faults.

The phase lines and neutral wires go through a fluxgate sensor. During normal operation without a fault condition, the sum of currents equals zero.

During a ground fault condition, the sum of currents is not equal to zero. During a DC fault, there is an imbalance of current flowing through the line and current returning through the neutral wire. The fluxgate is blind to steady DC current. An oscillating drive current is pushed through the fluxgate sensor coil. This DC fault current produces a magnetic field which opposes fluxgate drive in one direction, and assists fluxgate drive in the opposite direction; resulting in a duty cycle shift. Under normal conditions, the duty cycle of the switching is 50%. During a DC fault, the duty cycle shifts.

The oscillation frequency depends on the signal chain between R3 to pin 1 of the DFF. Match the current sense amplifier gain and VREF voltage to make sure the core is driven to saturation. Driving the core deeper into saturation reduces noise, removing the need for degaussing. When the core is fully saturated, all material within the core is magnetically aligned. When all material is aligned, there are no stray fields within the material to contribute noise.

3.1.6 DRV8220 H-Bridge

The DRV8220 drives current through the magnetic core to saturate the core. This device is the smallest, most cost-effective device capable of driving enough current.

The DRV8220 is an integrated motor driver with four N-channel power FETs, charge pump regulator, and protection circuitry. The device can supply up to 1.76A of output current, operating on a supply voltage from 4.5V to 18V. The driver offers robust internal protection including undervoltage lockout, output overcurrent, and device overtemperature.

The low-side current sense resistor (R3) detects current through the DRV8220. The current spikes when the core reaches saturation, which the saturation detection circuit can read.

The output of the DRV8220 is controlled by pins 1 and 2. The state of these pins determines which direction current flows through the magnetic coil. When the saturation detection circuit threshold is passed, the control signals to pins 1 and 2 flip, which flips the DRV8220 output.

DRV8220 output 1 and 2 are used to drive the fluxgate sensor coil to saturation. The saturation detection circuit uses the low-side current sense resistor to know when saturation is reached.

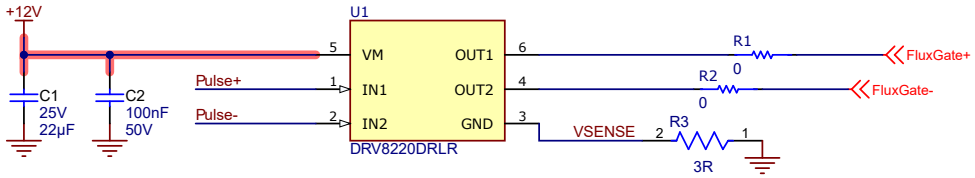

Figure 3-8. DRV8220 Schematic

The current through VSENSE peaks when the core reaches saturation.

3.1.7 Saturation Detection Circuit

The saturation detection circuit is made of the low-side current sense resistor (R3), current sense amplifier INA293, and comparator TLV7011. The comparator outputs high when the fluxgate sensor coil saturation is reached.

This circuit is used to determine when the fluxgate sensor has reached saturation.

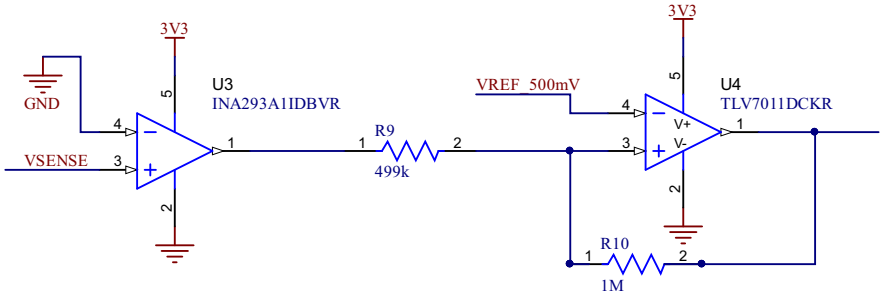

Figure 3-9. Saturation Detection Schematic

V_{SENSE} is read from the low-side shunt resistor of the DRV8220. V_{SENSE} gives the current through the fluxgate sensor coil. This signal is gained by current sense amplifier INA293, with a fixed gain of 20V/V. The gained signal is compared to a reference voltage V_{REF} of 695mV which is sourced from a resistor divider. When the current sense signal passes the V_{REF} voltage, the core has saturated and the DRV8220 must swap output directions. The output of comparator TLV7011 feeds into a DFF. For a longer explanation, see H-Bridge Controlled by DFF.

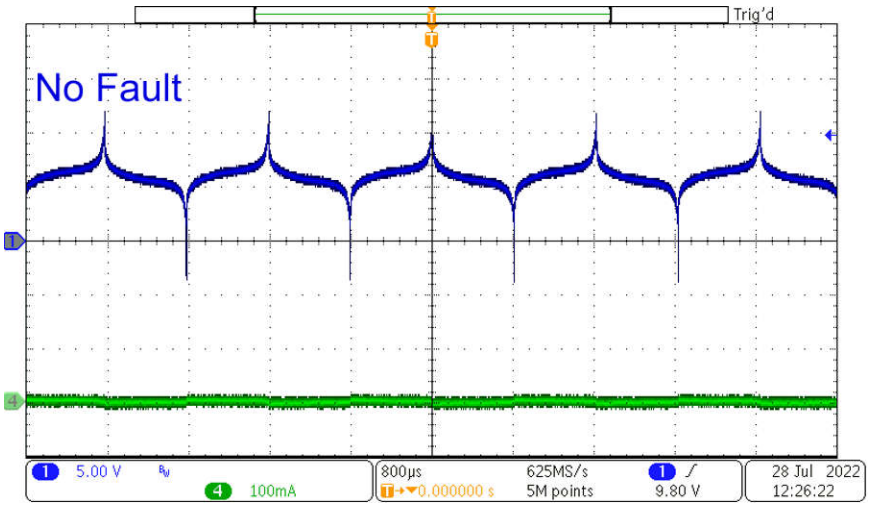

Figure 3-10. Burden Resistor Going Into Saturation

3.1.8 H-Bridge Controlled by DFF

The digital flip-flop uses the output logic to control the DRV8220 output current direction. The flip-flop circuit changes output Q with each positive CLK edge. The status of the auto-oscillation circuit can be monitored by confirming that the output Q continues to flip at less than 20mS. Reset the circuit by pulling reset_n low.

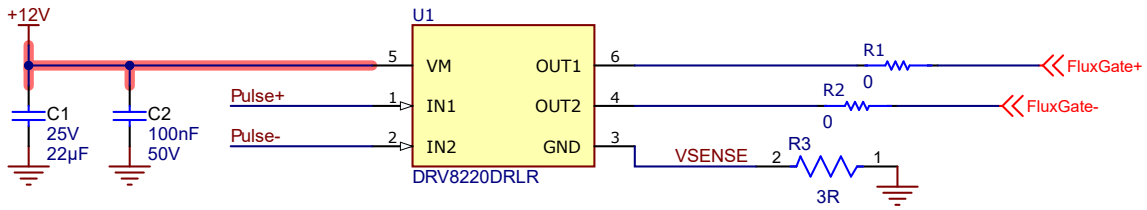

Figure 3-11. DFF SN74LVC2G74 Circuit

Inverted output !Q is connected to input data D, so each positive clock edge inverts the outputs.

3.1.9 Move Away From Timer Capture

Timer capture is a method to read the DC fault by reading duty cycle shifts from the auto-oscillation circuit. This is a common measurement technique in RCD modules. With a DC fault condition, the duty cycle of the DRV8220 shifts as the B-H curve or magnetization curve loop shifts. The DC fault current through the core causes saturation slightly quicker in one direction than the other. This difference translates into a measurable shift in duty cycle.

This approach was sensitive to noise in components, oscillators, and magnetic cores. This approach is found to require more expensive components with less delay, and faster MCU clock speeds. There was a large inconsistency of duty cycle shift dependent on which magnetic core was used. In many cases, the jitter caused by noise blinded the signal, causing false trips.

Reading a digital fault output from the window comparators or the analog signal using an ADC resulted in a lower cost BoM and more accurate readings over a broader selection of fluxgate sensor material types.

3.1.10 Fluxgate Sensor

Fluxgate sensors measure magnetic fields by periodically saturating a piece of ferromagnetic core material in alternating directions. When an external magnetic field is present, the periodic saturation is offset and measured. Intrinsic magnetic noise from the core as the core saturates limits fluxgate performance.

A ground fault creates a magnetic field due to the imbalance of current through line and return current through neutral.

Current going through a wire creates magnetic fields. When equal current flows in opposite directions, the sum of magnetic fields cancels out. To detect milliampere (mA) levels of fault current, use a soft magnetic material that has a high permittivity and low coercivity. The Hitachi core used for this design is FT-3K70T F2520C which is a nanocrystalline core. The core is wound with two sets of 100 and turns a 34-gauge magnet wire. Magnetics CMC020012008h is another nanocrystalline core option.

3.2 Test Setup

3.2.1 Ground-Fault Simulation

Faults were simulated with an additional wire running through the magnetic toroidal core with the three-phase and neutral line. The additional wire was connected to a separate power supply and controllable load to control the fault current amplitude and confirm circuit trip levels of 6mA DC or 30mA$_{RMS}$. In addition to threshold testing, the output of the nFault AND gate was measured to confirm when the system detected a fault and determine system response time.

3.3 Test Results

3.3.1 Linearity Over Temperature

The design was tested from –40°C to 110°C, and measurements were taken at the analog DC output to measure output voltage versus fault current. The fault current input range was tested –50mA to +50mA. Figure 3-12 shows the output voltage –8mA to 8mA of the active filters versus the fault current at different temperatures. The temperature drift is at a worst case of 432mV which is ±0.26mA.

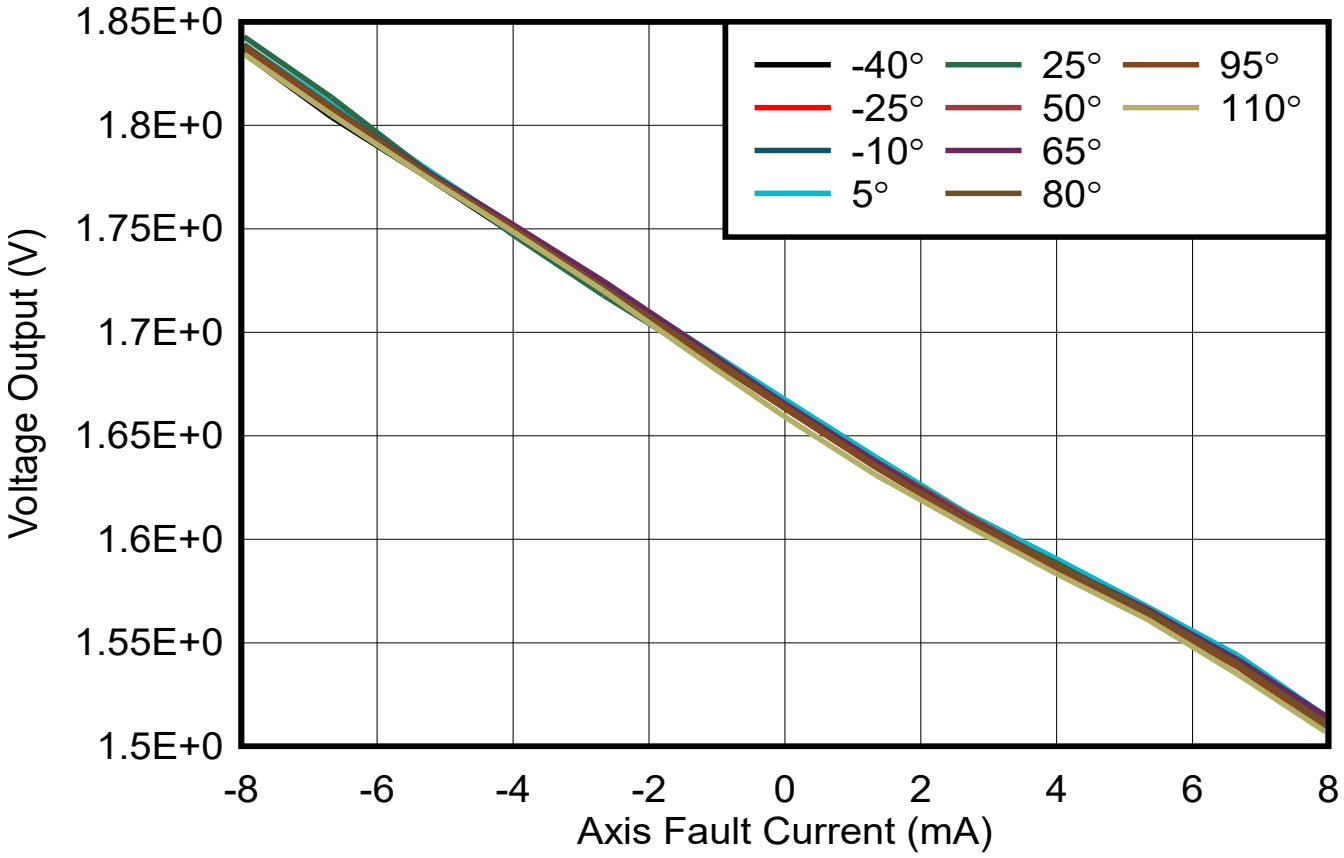

Figure 3-12. Filter Output versus Fault Current

3.4 Fault Response Results

Response time was measured for both AC and DC faulty currents. In Figure 3-13, the TIDA-010237 is sensing a 30mA$_{RMS}$ and resulted in a response time of approximately 11ms.

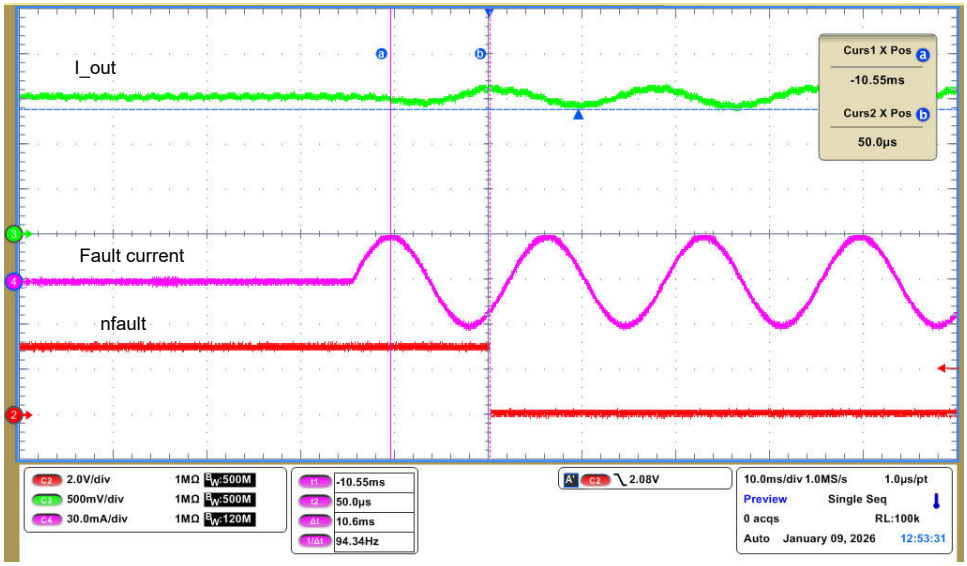

Figure 3-13. System Response to 30mA$_{RMS}$ Fault Current

In Figure 3-14, the TIDA-010237 is sensing a 50mA DC fault and resulted in a response time of 2.47ms

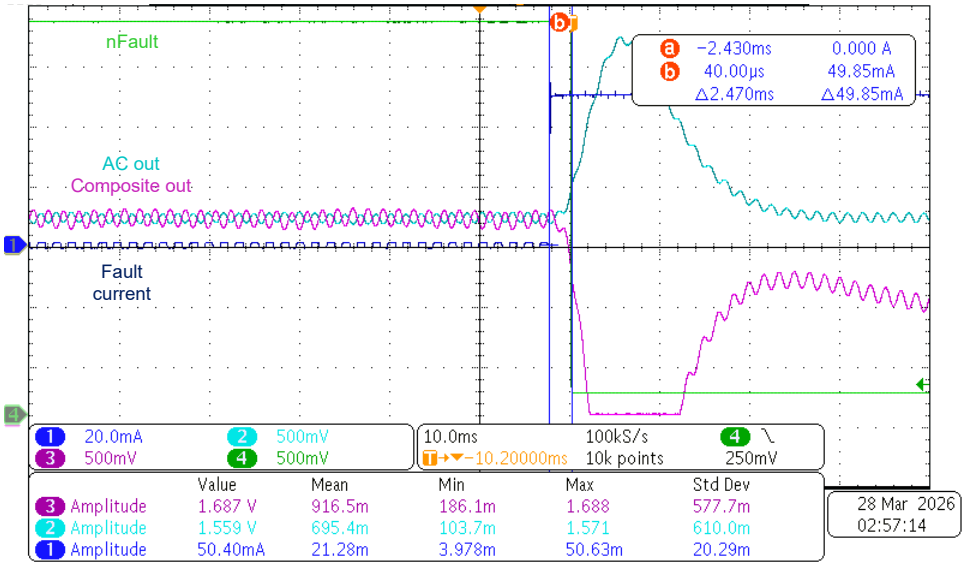

Figure 3-14. 50mA DC Fault

In Figure 3-15, the TIDA-010237 is sensing 6mA and resulted in a response time of approximately 47ms.

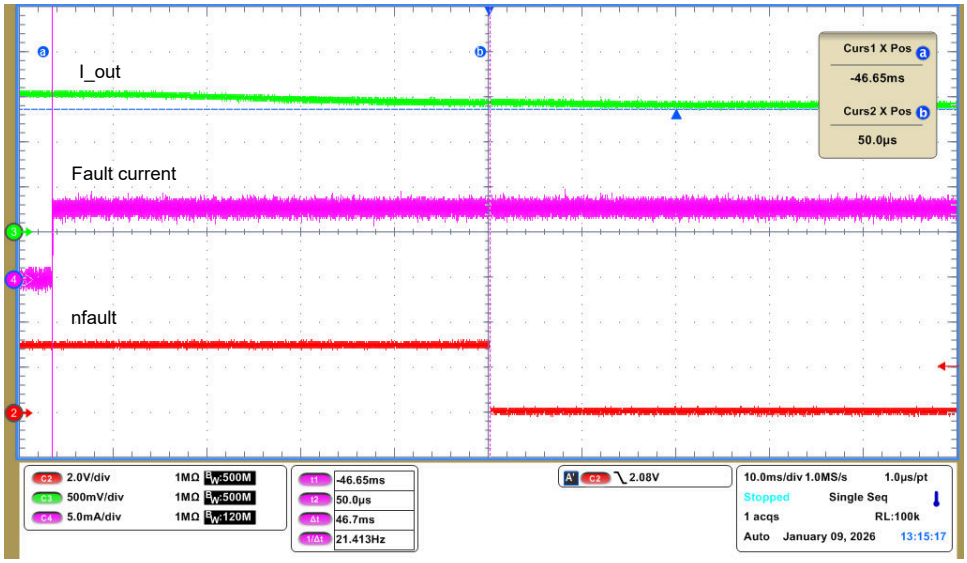

Figure 3-15. System Response to 6mA Fault Current

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010237.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010237.

4.2 Documentation Support

1. Texas Instruments, *DRV8220 18-V H-Bridge Motor Driver with PWM, PH/EN, and Half-Bridge Control Interfaces and Low-Power Sleep Mode* datasheet
2. Texas Instruments, *INA186 Bidirectional, Low-Power, Zero-Drift, Wide Dynamic Range, Current-Sense Amplifier With Enable* datasheet
3. Texas Instruments, *OPAx323 20MHz High Bandwidth, 114dB CMRR, Low Voltage (1.7V to 5.5V), RRIO Zero-Cross Operational Amplifier* datasheet
4. Texas Instruments, *TLV902xL and TLV903xL Precision, Self-Latching Comparator Family* datasheet
5. Texas Instruments, *INA293 –4 V to 110 V, 1.3-MHz, Ultra-Precise Current Sense Amplifier* datasheet
6. Texas Instruments, *SN74LVC1G74 Single Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset* datasheet
7. Texas Instruments, *TLV701x and TLV702x Small-Size, Low-Power, Low-Voltage Comparators* datasheet
8. Texas Instruments, *TLV767 1-A, 16-V Precision Linear Voltage Regulator* datasheet

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2022) to Revision A (April 2026)	Page
• Updates to receiving front-end and added comparator-based digital fault output	1
• Added UL2231 Reference	1
• Updated the *Top of Board* figure, *Bottom of Board* figure, *Block Diagram* figure, figure 2-1, figures 3-1 through 3-9, and figures 3-11 through 3-15	1
• Updated diagram to include AC output, DC output, and digital fault	3
• Removed MSPM430 Reference	8
• Added information about DC and AC filters	10
• Added second core option	14

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