TI Designs: TIDA-01456

Compact, Non-Isolated, Three-Phase Inverter Reference Design for 200- to 480-V AC Industrial Drives

Description

This reference design realizes a three-phase inverter subsystem for variable frequency AC inverter drives and servo drives. This design is particularly suited for drive architectures in which the microcontroller ground and the inverter ground are non-isolated. Basic isolated gate driver UCC5320S is used for driving the high-side inverter switches, and the small and compact six-pin UCC27531 low-side gate driver is used for driving the bottom switches. The reinforced isolation is moved to the UART communication channel. Current sensing in the inverter half-bridge leg is done in two phases using shunt resistors and the dual operational amplifier TLV9062. This drive architecture results in reduced number of reinforced isolated channels and enables a cost optimized compact solution. The design is controlled by a C2000™ microcontroller.

Resources

TIDA-01456	Design Folder
UCC5320	Product Folder
UCC27531	Product Folder
TLV9062	Product Folder
TLV431	Product Folder
ISO7741	Product Folder
SN6501	Product Folder
TLV702	Product Folder
TLV6001	Product Folder
TL331	Product Folder
TMDSCNCD28379D	Tool Folder

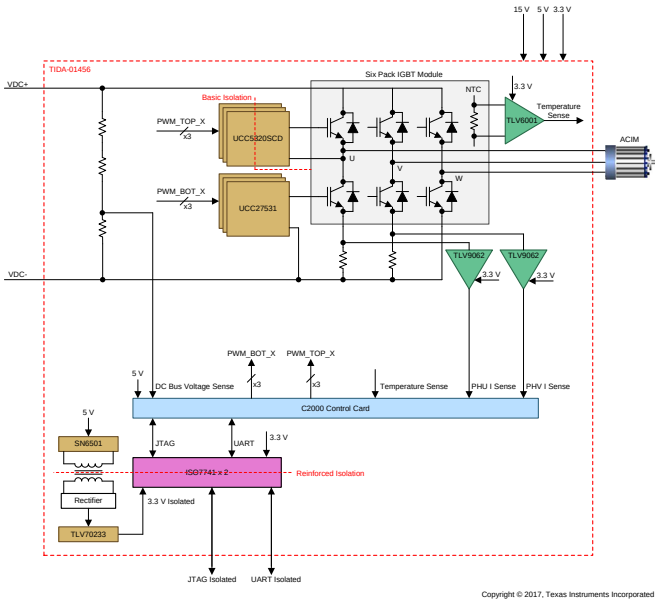
TI E2E™ Community — ASK Our E2E Experts

Features

- Three-Phase Inverter Power Stage Suited for 200- to 480-V AC Powered Drives With Continuous Current Rating up to 10 A_{RMS}
- Compact, Cost-Optimized Solution Due to:
  - Movement of Reinforced Isolation From Power Stage to Interprocessor Communication Channel Resulting in Reduction of Number of Reinforced Isolated Devices From 9 to 1
  - Use of Small Low-Side Gate Drivers (SOT23: 2.9 mm × 1.6 mm) and Basic Isolated High-Side Gate Drivers (SOIC8: 4 mm × 5 mm)
  - Single (15 V) Power Supply Rail Powering All Gate Drivers Through Bootstrap Technique
  - High-Side Gate Drivers With Basic Isolation in Power Stages Minimizes Creepage Distances
- Low Propagation Delay (< 75 ns) of Gate Drivers Enable Decreasing Dead Time, Which Improves Inverter Efficiency and Reduces Distortions
- Robust Solution Due to Gate Drivers With Enhanced Immunity Against Miller dV/dt Turnon Events, Negative Input Voltage Handling and UVLO
- Low-Side Shunt-Based Current Sensing for Two Inverter Legs Using Dual Operational Amplifiers
- Reinforced Isolated JTAG for Controller Debug and UART for Communication
- Provision for IGBT Module Temperature Measurement Using NTC Integrated Inside Module

Applications

- AC Inverter and VF Drives
- Servo CNC and Robotics



An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Description

Three-phase inverter power stages are the fundamental building blocks in industrial motor drive applications like pumps, compressors, robotics, machine tools, and CNC machines. The inverter converts a DC voltage into a variable frequency and power AC output to drive the motor.

The generic motor control blocks are shown in Figure 1. The inner most control loop controls the torque applied by the motor. The torque applied by the motor is directly proportional to the motor current. The current can be sensed either in the motor phase, the inverter half-bridge legs, or in the DC link. Each of these available methods have pros and cons, and a specific sensing technology is selected depending on the drive architecture and control performance required. The sensed current is then controlled to the loop current set point by varying the inverter duty cycle applied to the motor. The current loop exists inside the speed loop. The speed of the motor can be detected with sensors like the resolver and encoder, which are mounted on the motor shaft or the speed can also be calculated without sensors. The choice of speed detection is again dependent on drive performance and architecture. The speed loop provides the current setpoint to the current control loop. The setpoint is a function of the error between the actual speed and the required speed. The speed loop exists inside a position control loop. The position control loop provides a speed setpoint, which is a function of the actual position and the required position. The required position setpoint can come from further external control loops, human machine interface, or from a motion control profiler.

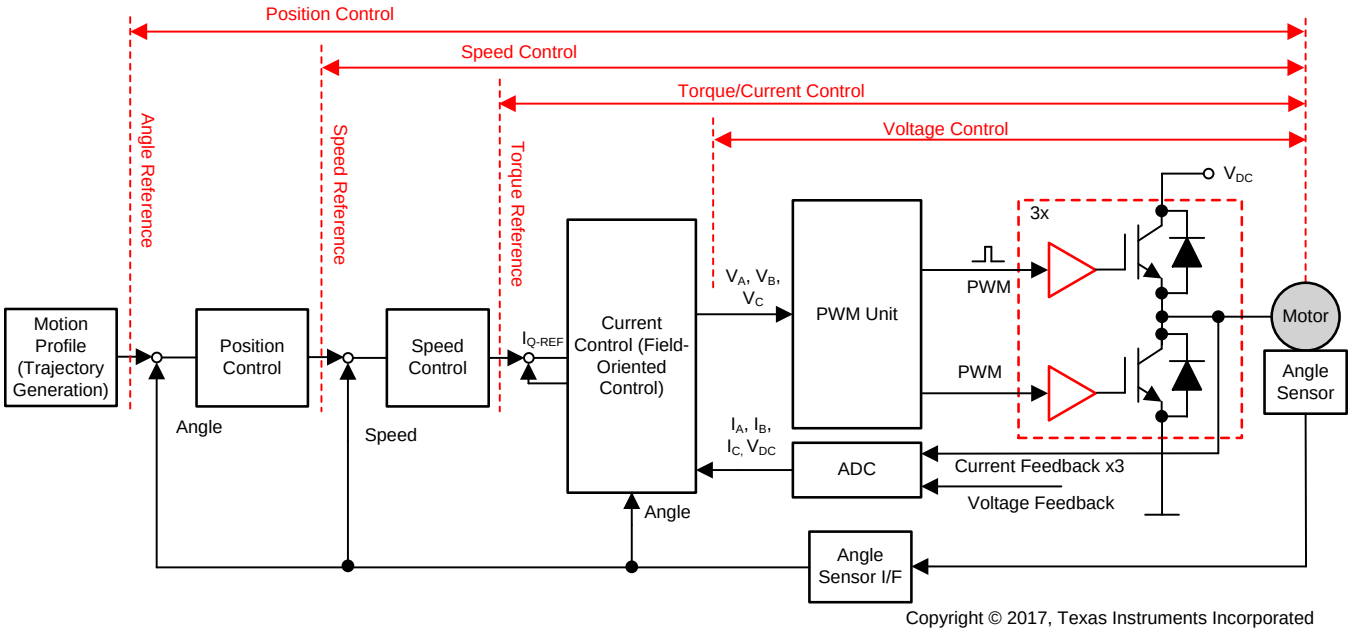


Figure 1. Generic Motor Control Block

The control blocks can be implemented inside a single controller or shared across multiple controllers. Reinforced isolation is required between the power stage and the user interface for safety. The reinforced isolation can be placed between the controller and the power stage, such a control architecture is called cold side control, or the torque and current control can be implemented inside a single motor controller and the position and speed control, communications, and human machine interface functions inside another application controller. The reinforced isolation can be placed in the communication channel between the two controllers. The IC used for motor current controller shares the ground with the inverter in such an architecture, which is called hot-side control.

Figure 2 shows the hot- and cold-side control architectures implemented inside a drive. For the cold-side control, reinforced isolation is required on the six gate drivers, current sensors, and DC-link voltage sensing. For hot-side control, isolation is only required on the high-side gate drivers as the safety isolation is moved to the communication channel. This enables the use of compact basic isolated high-side gate drivers. Small, low-cost, non-isolated gate drivers are used for low-side switches; current sensing is done in the inverter phase legs using shunt resistors and op amps; and DC-link voltage sensing using voltage dividers and temperature sensing using op amps. Reducing the number of reinforced isolation channels saves cost and results in a small form factor power stage. The hot-side control architecture is generally suited for low-power drives in the range of around 5 kW. For higher power drives, ground bouncing starts to become significant, making it more difficult to share ground between controller and power stage.

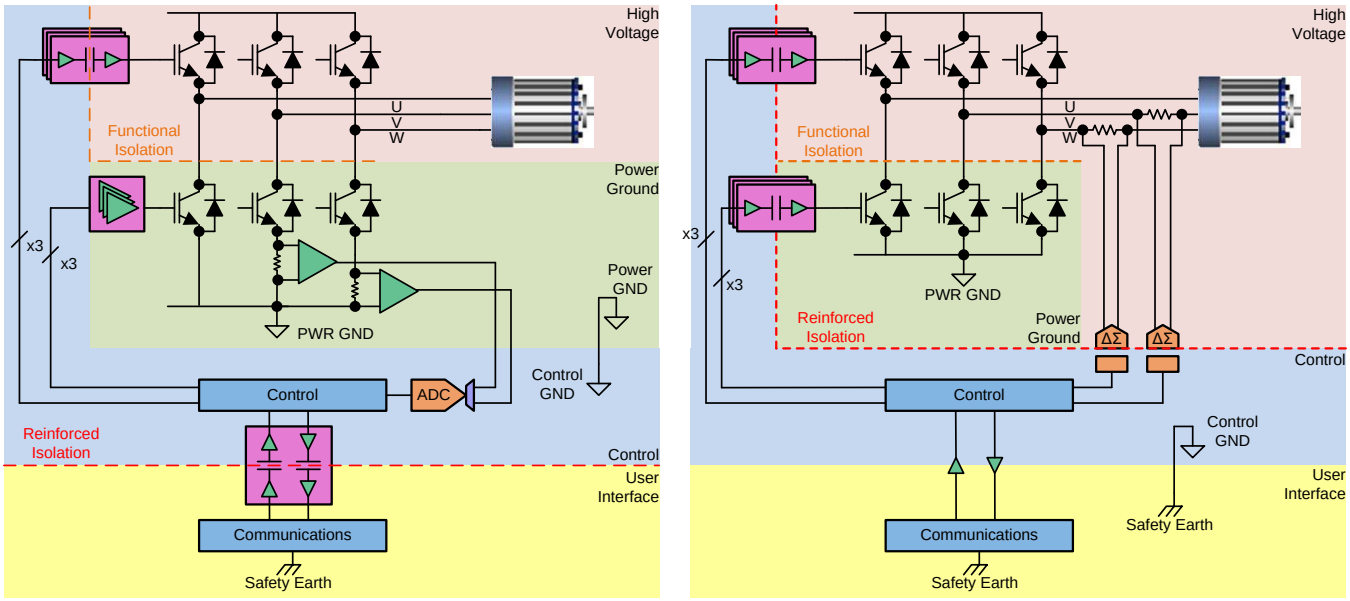


Figure 2. Hot-Side and Cold-Side Motor Control Architectures

This reference design shows the functionality of the three-phase inverter using the hot-side control architecture implemented with TI's non-isolated low-side gate drivers, basic isolated high-side gate drivers, and op amps for current sensing. The design is used to demonstrate the robustness of the architecture in an actual system. The following test results are shown:

- UVLO functionality of gate drivers
- PWM propagation delay
- Gate source and sink currents, gate voltages, and switch node voltage waveforms at hard and soft switching conditions
- Bootstrap power supply ripple

1.1 Key System Specifications

Table 1. Key System Specifications

SUBSECTION	PARAMETER	SPECIFICATIONS	COMMENT
Inverter	DC bus input voltage	200- to 900-V DC	—
	Continuous output current rating	10 A_{RMS}	—
	Output frequency	0 to 100 Hz	—
	PWM switching frequency	4 to 16 kHz	Inverter tested with specified range
	PWM dead band	800 ns	Inverter tested with 800-ns deadband; can be varied as long as there is no overlap between V_{GE} signals of top and bottom IGBT switches
	Power switch used	1200-V, 35-A, six-pack inverter IGBT module with integrated NTC and open emitter for low-side switches	Part number: SK35GD126ET
Current sensing	Measurement range	20 A_{PK}	Shunt resistor used is 4 mΩ with an difference amplifier gain of 20.1
Feedback	Measured variables	U and V phase leg currents, module temperature, DC-link voltage	Feedbacks required for motor control and protection
Protection	DC bus voltage	Overvoltage and undervoltage detection	User software implementation
	Module temperature	Overtemperature shutdown	User software implementation
	Isolation	Reinforced isolation	Reinforced digital isolators are used for JTAG and UART signals; 8-mm creepage between the hot and cold sides
Operating conditions	Temperature range	0ºC to 85ºC	Components selected support the industrial temperature range of 85ºC
Interface connectors	Microcontroller (MCU) interface	180-pin dual in line edge connector socket for C2000 control cards	See schematic for pin assignments on the connector
	Power	15 V, 100 mA	For powering the low side gate drivers and generating the bootstrapped power supplies for the secondary side of high side gate drivers
		5 V, 500 mA	For powering the C2000 control card and SN6501 based push pull isolated power supply.
		3.3 V, 100 mA	For powering the current sense amplifier, primary side of high-side gate drivers, NTC buffer, high-voltage LED indicator comparator circuit, hot side of digital isolators, and reference generator for current sense amplifier level shifting
	Communication	Isolated JTAG	14-pin header with key for connecting debug probe
		Isolated UART	3-pin header
PCB information	PCB layer stack	4 layer, 2-oz copper	35-micron copper
	Laminate	FR4, high Tg	—
	PCB thickness	1.6 mm	—
	PCB size	95 mm × 110 mm	—

2 System Overview

2.1 Block Diagram

Figure 3 shows the system level block diagram for this reference design.

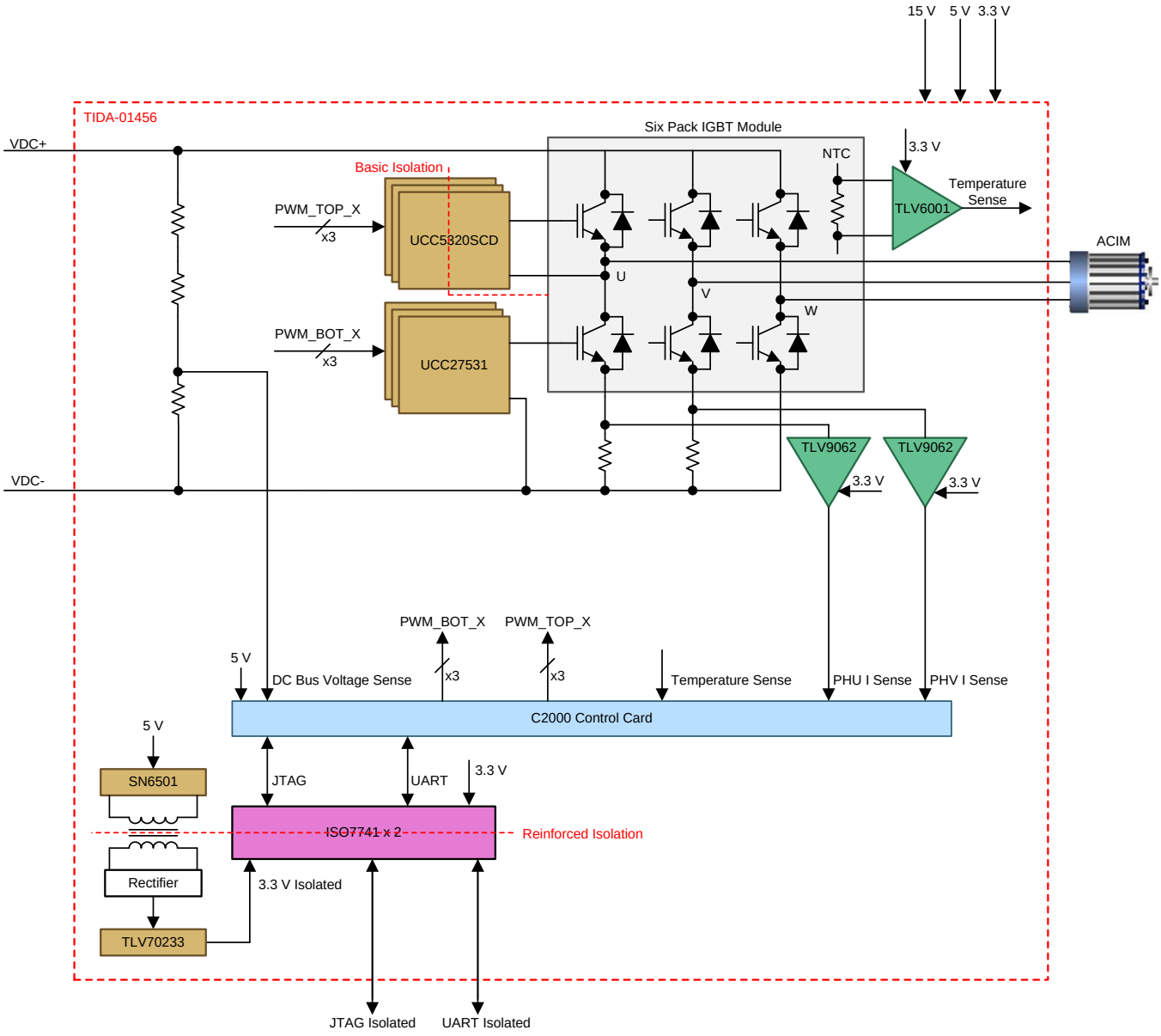


Figure 3. TIDA-01456 Block Diagram

The inverter section is implemented using a six-pack IGBT power module. The power module is composed of three half bridges. The emitter of each of the low-side IGBTs is open inside the module and brought out to a pin. This allows adding a shunt resistor on the phase legs for low-side current sensing. The low-side IGBTs are controlled by the low-side gate driver UCC27531. The device is available in the 6-pin SOT-23 package, which enables a compact solution. Basic isolated UCC5320S in the SOIC8 package is used for the high-side gate drivers. Six PWM signals are routed from the controller to the gate drivers. The DC-link voltage is applied to the board through a terminal block. The maximum DC-link voltage that can be applied is 900 V. The motor is connected to the inverter through a terminal block.

As the controller ground is common with the inverter, low-side current sensing is done using shunt resistors in the phase legs and non-isolated op amp. In this design, the cost-optimized dual op amp TLV9062 is used in the difference amplifier configuration. A single 3.3-V power supply is used by the op amp. For bidirectional current sensing, a reference voltage is required for level shifting the shunt voltage. The TLV431 is used for generating a 1.65-V reference from 3.3 V to the difference amplifier.

The inverter power stage has been designed to be protected against DC bus under- and overvoltage and IGBT module overtemperature. The DC-link voltage is sensed using a high-impedance voltage divider. The scaled voltage is directly connected to the ADC inside the controller. For module temperature monitoring, the negative temperature coefficient resistor integrated inside the module is used. A voltage divider is implemented using the NTC and an external resistor. The voltage drop across the NTC is buffered by a single, cost-effective op amp TLV6001, which drives the ADC inside the controller. The actual temperature is derived from the voltage drop by software implemented in the controller.

The reinforced isolation on the PCB board is on the communication channels. The communication interfaces on the board are JTAG and UART. The JTAG signal is used to debug the controller and the UART signal can be used for communication to an external serial interface. The JTAG and UART signals are reinforced isolated through two ISO7741 digital isolators before being taken out of the board.

The TIDA-01456 PCB requires three additional external power supplies other than the DC-link voltage. 15 V is required for the low- and high-side gate drivers. The secondary side of the high-side gate drivers is powered by bootstrapping the low-side power supplies. 5 V is required by the C2000 control card, and 3.3 V is required by the primary side of the high-side gate drivers, the current and temperature sensing op amps, and the hot side of the digital isolators. The secondary side of the isolators require reinforced isolated power supply, which is generated by the SN6501 push-pull transformer driver, reinforced isolated center tap transformer, and rectifier diodes on the isolated side. The SN6501 converts 5 V into an isolated mid-voltage rail. The TLV70233 LDO converts the mid-voltage rail into 3.3 V for the isolator cold side.

2.2 Highlighted Products

2.2.1 UCC5320S

The UCC5320S is a compact, single-channel, basic isolated gate driver available in an 8-pin SOIC package. This package has a creepage and clearance of 4 mm and can support isolation voltage up to 3 kV_{RMS}. The driver has a split output with a minimum source current rating of 2.4 A and a minimum sink current rating of 2.2 A that is used to control the rise and fall times of the IGBT switch independently. The 11-V UVLO feature prevents the operation of the IGBT in the linear region incase there is a fault in the gate drive power supply.

When compared to an optocoupler, the UCC5320S has lower part to part skew, lower propagation delay, higher operating temperature, and higher CMTI. The low propagation delay enables reducing dead time, and the high temperature range and CMTI make the gate drive solution more robust.

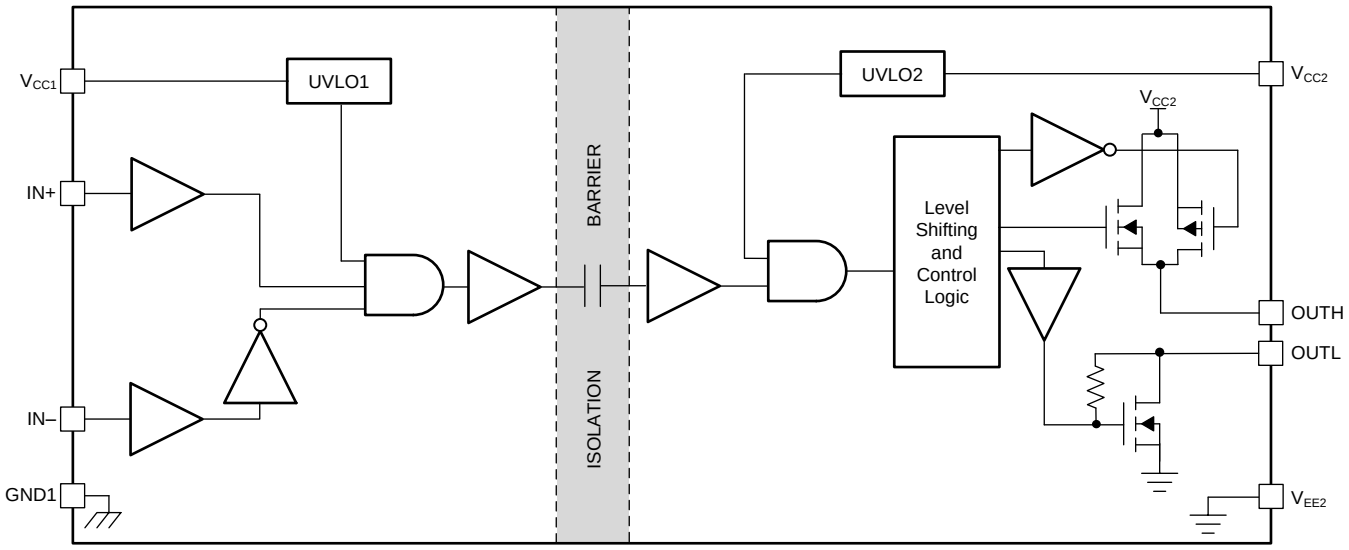


Figure 4. Functional Block Diagram of UCC5320S

2.2.2 UCC27531

The UCC27531 is a single-channel, high-speed gate driver that can source up to 2.5 A and sink up to 5 A through split outputs. The split outputs and strong asymmetrical drive boost the devices immunity against parasitic Miller turnon effect and can help reduce ground debouncing. The extremely small propagation delay (17 ns typical) helps reduce dead time and the small 6-pin SOT-23 package enables a low-cost compact solution.

When compared to a discrete transistor pair solution, the UCC27531 provides easy interface with the controller, reduces BOM components, and has integrated features like UVLO detection on the power supply of the gate drive.

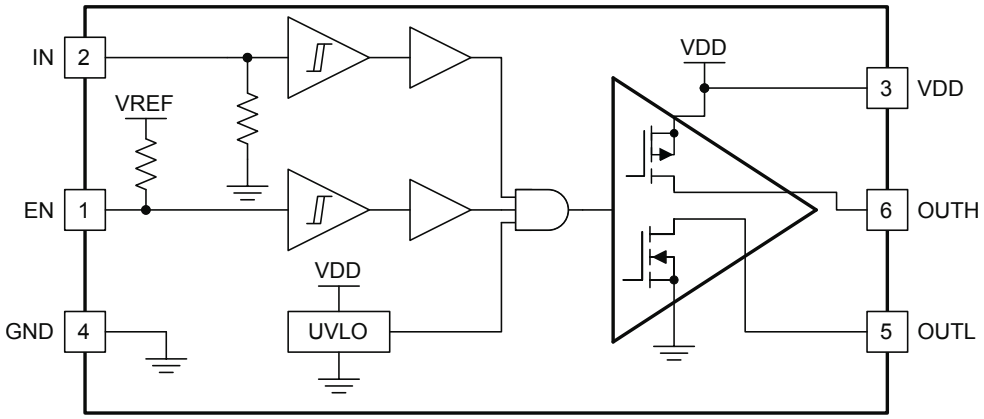


Figure 5. Functional Block Diagram of UCC27531

2.2.3 TLV9062

The TLV9062 is a cost-effective, dual low-voltage op amp with rail-to-rail input and output swing capabilities. The device has a unity gain bandwidth product of 10 MHz and an output slew rate of 6.5 V/µs. The RFI and EMI rejection filter are integrated inside the device. These features make the TLV9062 an excellent device for low-side current sensing in the inverter half-bridge phase legs.

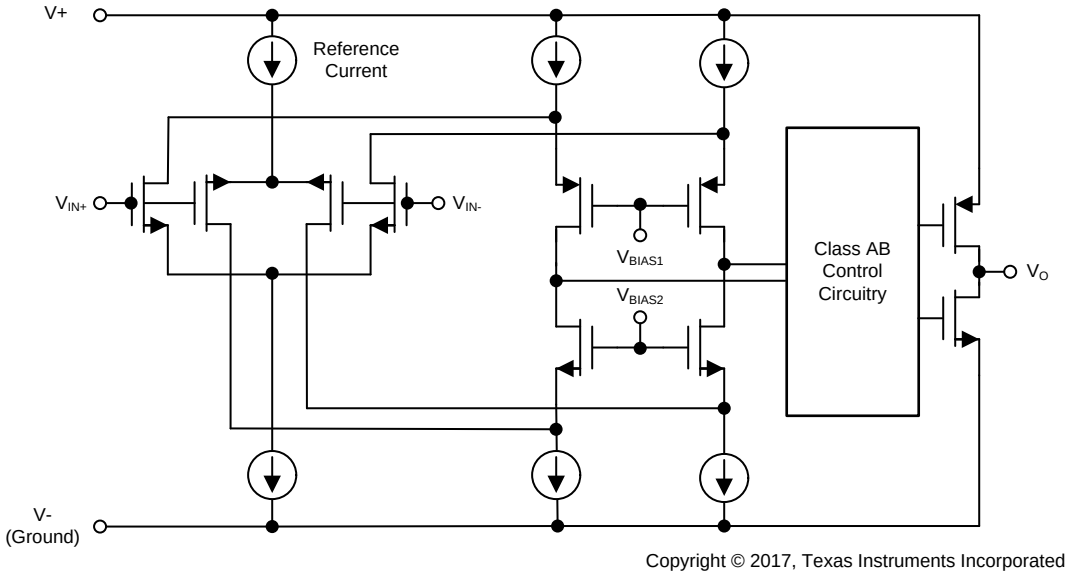


Figure 6. Functional Block Diagram of TLV9062

2.2.4 TLV431

The TLV431 is a low-voltage, three-terminal, adjustable voltage reference with specified thermal stability over industrial temperature range. The output voltage can be set to any value between V_{REF} (1.24 V) and 6 V with two external resistors. The low operational cathode current of 80 µA (typ) with active output circuitry and precise output voltage regulation makes the TLV431 excellent replacement for low-voltage Zener diodes. In this design, the device is used to provide a 1.65-V reference for level shifting the outputs of the current sense amplifier.

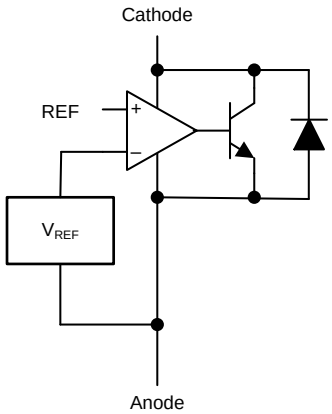


Figure 7. Functional Block Diagram of TLV431

2.2.5 ISO7741

The ISO7741 is a high-performance, quad-channel digital isolator with a 5000-V_{RMS} (DW package) isolation rating as per UL 1577. The device is reinforced isolated as per VDE, CSA, TUV, and CQC. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO7741 device has been significantly enhanced to ease system level ESD, EFT, surge, and emissions compliance. This enables a robust digital isolation solution. In this design, the part is used for isolating the JTAG and UART signals from the MCU, which is placed on the hot side.

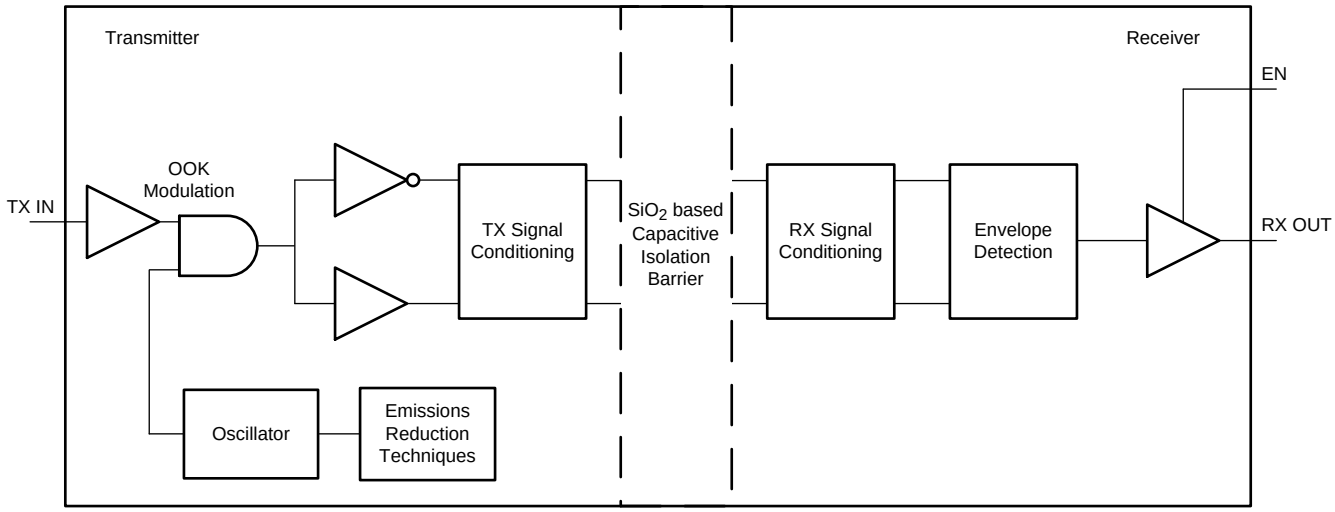


Figure 8. Functional Block Diagram of a Channel of ISO7741

2.2.6 SN6501

The SN6501 is a push-pull transformer driver in a small 5-pin SOT-23 package. The monolithic oscillator and power driver is specifically designed for small form factor isolated power supplies in isolated interface applications. In this design, the device along with a reinforced isolated center tapped transformer generates an isolated 3.3-V power supply for the isolated UART and JTAG signals.

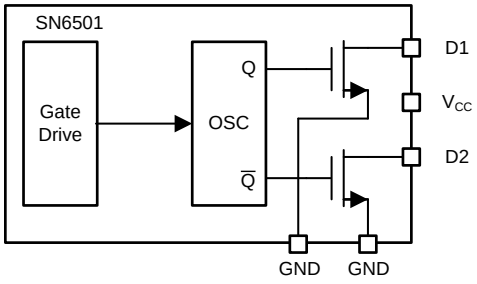


Figure 9. Functional Block Diagram of SN6501

2.2.7 TLV702

The TLV702 series of low dropout linear regulators are low quiescent current devices with excellent line and transient performance. All device versions have thermal shutdown and current limit for safety. The devices are stable with an effective output capacitance of only 0.1 µF. This enables the use of cost effective capacitors that have higher bias voltages and temperature derating. The 3.3-V output version of the device is used for powering the cold side of the digital isolators, which isolate the JTAG and UART signals.

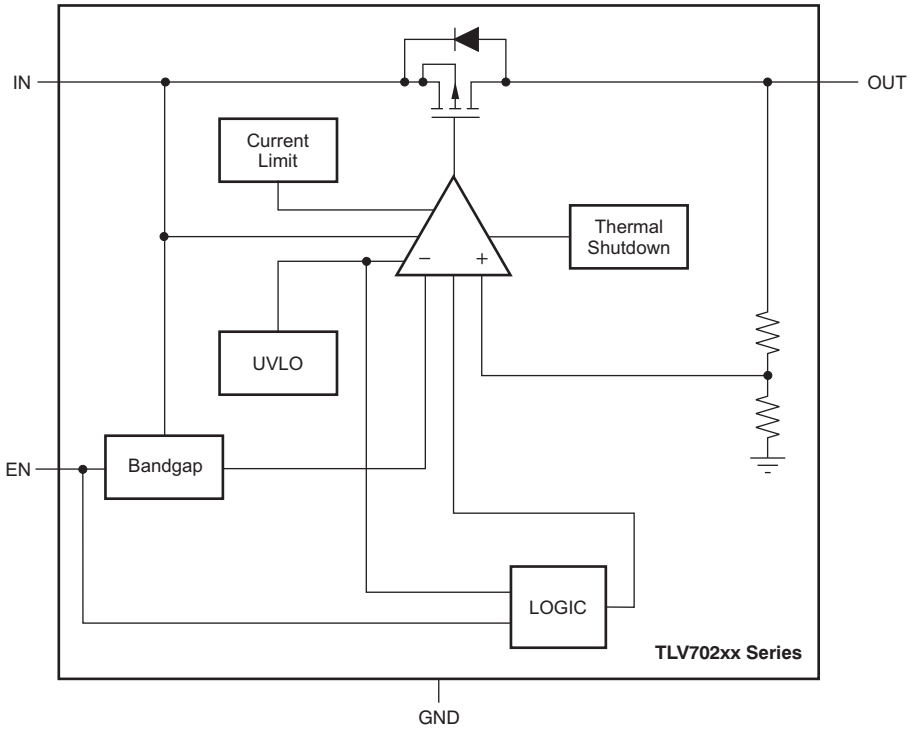


Figure 10. Functional Block Diagram of TLV702

2.2.8 TLV6001

The device is a single-channel op amp with rail-to-rail input and output swings, low quiescent current (75 µA typ), wide bandwidth (1 MHz), and low noise. The device has internal RF and EMI filters and is unity gain stable with capacitive loads up to 150 pF. The device is specifically designed to be low cost. In this design, the part is used in voltage follower configuration to buffer the output of the NTC integrated inside the IGBT module to the MCU.

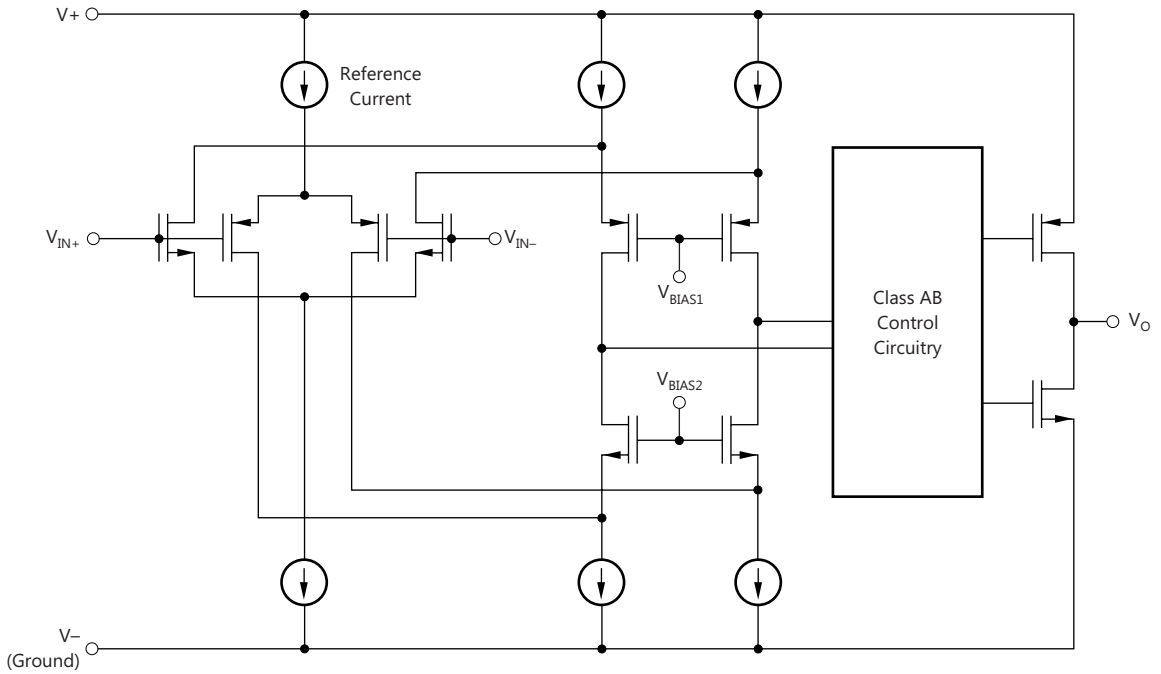
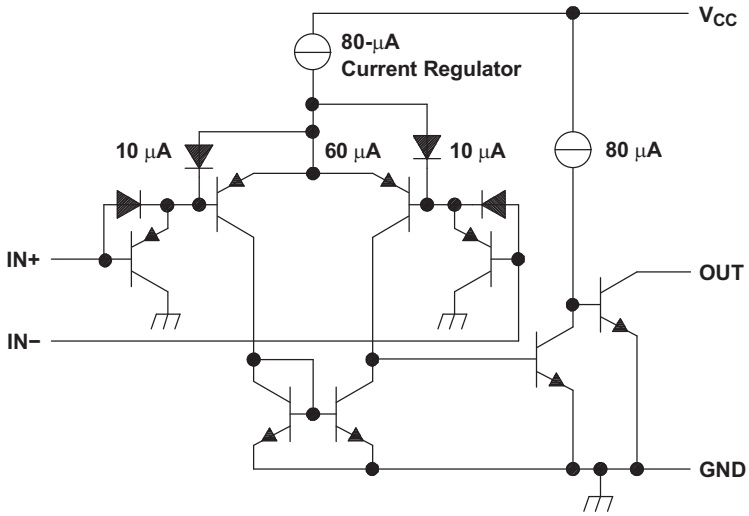


Figure 11. Functional Block Diagram of TLV6001

2.2.9 TL331

The TL331 is a single voltage comparator designed to operate from a single power supply over a wide range of voltages. The current drain is independent of the supply voltage and the output of the comparator is open collector. In this design, the comparator is used to drive an LED that indicates whether the DC bus voltage is energized more than 50 V.



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	1
Transistors	20

Current values shown are nominal.

Figure 12. Functional Block Diagram of TL331

2.3 System Design Theory

2.3.1 DC Bus Voltage Input

This reference design is designed to operate from a DC bus voltage of up to 900-V DC at maximum, which covers most of the low-voltage drives with grid voltage input up to 480-V AC as shown in Table 2.

Table 2. Maximum DC Bus Voltage for Different Grid Voltages

THREE-PHASE GRID VOLTAGE	MAXIMUM DC-LINK VOLTAGE	IGBT BLOCKING VOLTAGE
208-, 220-, 230-, 240-V AC	400-V DC	600 or 650 V_{PK}
380-, 400-, 415-, 480-V AC	900-V DC	1200 V_{PK}
690-V AC	1200-V DC	1700 V_{PK}

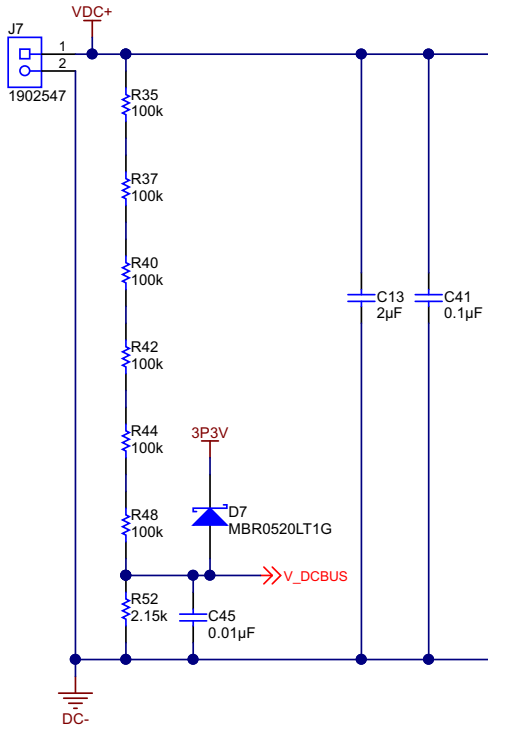


Figure 13. DC Bus Input

The DC bus voltage is applied to connector J7. The bulk capacitors are not placed on the PCB and have to be connected externally or a current limited high-voltage DC source has to be used. A 2-µF, 1100-V film capacitor is placed close to the IGBT DC bus inputs and a 0.1-µF, 1000-V ceramic capacitor is connected in parallel. These capacitors minimize the loop area for the high-frequency switching currents. This helps minimize switch node overshoots and high frequency ringing, which in turn help reduce EMI.

2.3.1.1 DC Bus Voltage Sensing

The resistor network comprising of R35, R37, R40, R42, R44, R48, and R52 form a high impedance voltage divider. The attenuated voltage is routed to the ADC integrated inside the controller. This voltage is used for DC bus undervoltage and overvoltage protection. It is also used for estimating the output voltage applied to the motor.

$$V_{DCBUS} = (VDC+) \times \left(\frac{R52}{R52 + R35 + R37 + R40 + R42 + R44 + R48} \right) = 0.00357(VDC+) \quad (1)$$

The 0- to 900-V DC range is converted to 0 to 3.213 V. The maximum voltage across each resistor is 150 V (at 900-V DC). The maximum power that can be dissipated in the divider is 1.345 W (at 900-V DC). The maximum dissipation per resistor is 0.224 W. Therefore, 200-V rated, 0.25-W, 1206 package resistors are selected for the resistor divider network.

In case there is failure in resistor R52 and it gets open, there is a possibility of high voltage getting connected to the controller. D7 is used to clamp the voltage to 3.3 V in such a case. A 0.01-µF ceramic capacitor is used for low pass filtering.

2.3.1.2 DC Bus Energized LED Indication

When the input to the DC bus is disconnected; the film capacitor still holds stored charge which discharges slowly over time by leakage mechanism. This may cause an electrical shock hazard for anyone touching the board even though the input is disconnected. This reference design uses comparator TL331 with open collector output for indicating that the DC bus is energized. The comparator drives an LED which lights up as soon as the DC bus voltage increases above 50-V DC. For 50-V DC, the threshold is 50 × 0.00357 = 0.1785 V, which is set by the divider network R56 and R39.

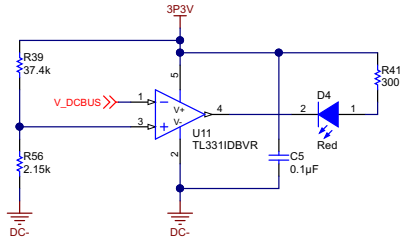


Figure 14. DC Bus Energized LED Indication

2.3.2 Inverter IGBT Module Selection

The inverter stage converts the DC bus input voltage into variable frequency AC voltage for driving the motor. It comprises of the six-pack inverter IGBT module and the gate drivers. This reference design has a nominal output current rating of 10 A_{RMS} and can be powered with grid voltages up to 480-V AC. Table 2 shows that an IGBT module with a blocking voltage range of 1200 V_{PK} is required for drives powered with grid voltages up to 480-V AC.

A 1200-V Semikron IGBT module SK35GD126ET is selected for the inverter. This module has a maximum collector current rating of 32 A and inverse diode current rating of 23 A at case temperature of 80 ºC. The module also has an NTC integrated inside the module for module temperature measurement. All the emitter pins of the low-side IGBTs are open and accessible. This allows insertion of shunt resistors between the emitter and the DC– allowing for low-side current sensing in the phase half bridge.

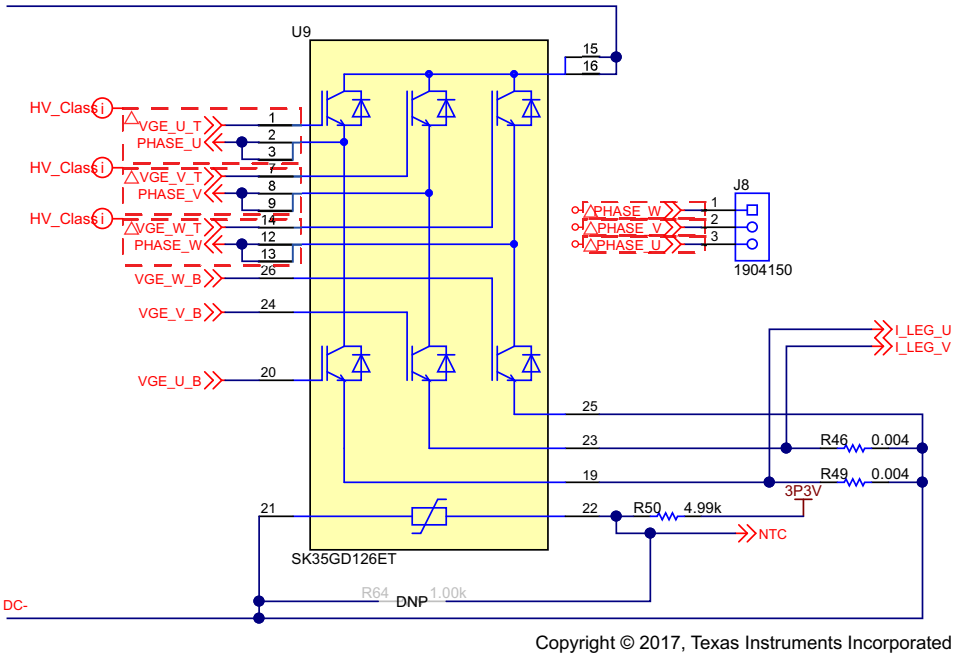


Figure 15. Three-Phase Inverter Stage

2.3.3 Low-Side IGBT Gate Driver

NOTE: This section describes the IGBT gate driver for one phase. The gate drivers for the other two phases are similar.

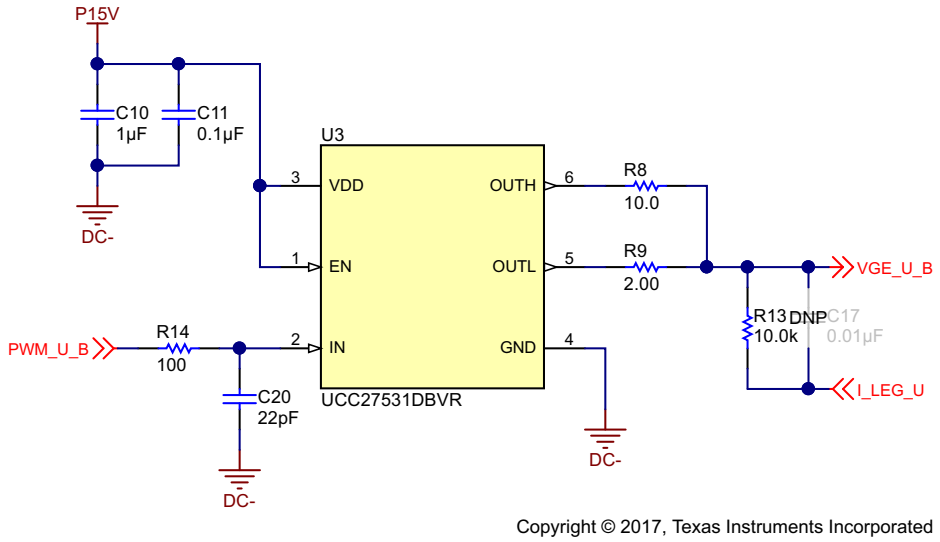


Figure 16. Low-Side Gate Driver Phase U

In this reference design, the controller is placed on the hot side and thus shares the ground with the inverter. This enables driving the low-side IGBT gate without isolation resulting in the use of low-cost, compact, non-isolated, low-side gate drivers. The UC27531 in the SOT23 6-pin package is used in this design. The UCC27531 has a VDD voltage range of 10 to 35 V, enabling its use with IGBTs that require a 15-V gate voltage for IGBT turnon.

2.3.3.1 Gate Driver Supply

The UCC27531 has a single supply for both the gate driver internal circuit biasing as well as the drive output stage. In this design, it is powered with a 15-V supply. A 1-µF bulk capacitor C10 is placed on the VDD pin of the gate driver. This provides the IGBT gate currents and helps minimize the parasitic inductance due to gate current loops allowing for faster switching. A 0.1-µF noise decoupling capacitor C11 is also used to filter the power input.

2.3.3.2 PWM Input

The PWM inputs to the gate driver are provided by the controller PWM output peripheral. The signal is single ended and is filtered by an RC low-pass filter comprising of R14 and C20 before connecting to the gate driver input. The filter attenuates high-frequency noise and prevents overshoot and undershoot on the PWM inputs due to longer tracks from the controller to the gate driver. In the PCB layout, take care that the input PWM signal return does not crisscross the IGBT inverter DC– current paths to avoid ground bouncing issues.

2.3.3.3 Gate Drive Enable

In this design, the EN pin of the gate driver is hardwired to the VDD pin. This results in the gate driver being always enabled as long as the VDD voltage is above the UVLO threshold limits.

2.3.3.4 Gate Driver Output Stage

The UCC27531 has split outputs, which allow for controlling the turnon rise time and turnoff fall time of the IGBT individually. A 10-Ω gate resistor R8 is used for IGBT turnon. A 2-Ω IGBT turnoff resistor R9 allows for strong turnoff, helping reduce turnoff losses. The low value of the turnoff resistor also increases the immunity of the gate drive circuit to Miller induced parasitic turnon effects. A 10-kΩ resistor R13 is connected across the IGBT gate to emitter pins close to the IGBT module. This is to ensure that the IGBT remains in the off state in case the gate driver gets disconnected from the IGBT due to faults.

2.3.4 High-Side IGBT Gate Driver

This reference design has the controller on the hot side and the reinforced safety isolation is placed on the communication link. This enables the use of basic isolated UCC5320SD gate driver in SOIC 8 package, which has a creepage and clearance distance of 4 mm.

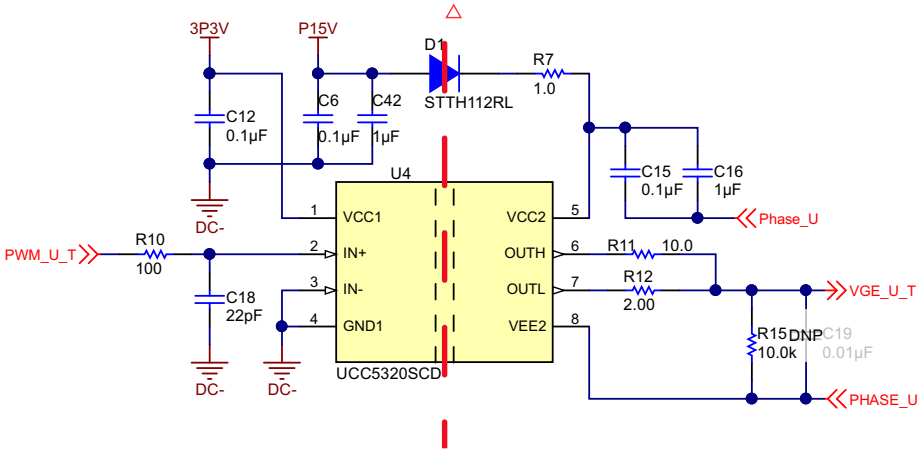


Figure 17. High-Side Gate Driver Phase U

2.3.4.1 Primary-Side Supply

The UCC5320S primary side is powered by a 3.3-V rail. A 0.1-µF ceramic capacitor is placed close to the VCC1 pin for noise decoupling. The positive going UVLO threshold on the supply is 2.6 V and the negative going threshold is 2.5 V.

2.3.4.2 Secondary-Side Supply

The 15-V secondary-side power supply is used for driving the IGBT gate. It is generated by bootstrapping the low-side gate driver power supply using D1, R7, and C16. C15 (0.1 µF) is a high-frequency noise decoupling capacitor. C16 (1 µF) is a bulk capacitor that provides the IGBT gate drive source current. Using bootstrap power supply is a simple, cost-effective method of generating floating power supply for the high-side gate driver. The positive going UVLO threshold on the supply is 12 V and the negative going threshold is 11 V.

2.3.4.3 PWM Input

The PWM input to the gate driver is provided by the controller PWM output peripheral. Dead time must be inserted between the low-side and high-side PWM signals to prevent both switches turning on at the same time. The signal is single ended and is filtered by RC low pass filter comprising of R10 and C18 before connecting to the gate driver input. The filter attenuates high frequency noise and prevents overshoot and undershoot on the PWM inputs due to longer tracks from the controller to the gate driver. The inverting PWM input IN– is not used in the design and is connected to primary side ground.

2.3.4.4 Gate Driver Output Stage

The UCC5320S has split outputs that allows for controlling the turnon rise time and turnoff fall time of the IGBT individually. A 10-Ω gate resistor R11 is used for IGBT turnon. A 2-Ω IGBT turnoff resistor R12 allows for strong turn off helping reduce turn off losses. The low value of the turnoff resistor also increases the immunity of the gate drive circuit to Miller induced parasitic turnon effects. A 10-kΩ resistor R15 is connected across the IGBT gate to emitter pins close to the IGBT module. This is to ensure that the IGBT remains in the off state in case the gate driver gets disconnected from the IGBT due to faults.

2.3.5 Low-Side Current Sensing

Accurate speed and torque control of a motor requires precise control of the inverter output current. The current is then used for calculation of output PWM pattern. In this design, inexpensive shunt resistors are used for current sensing. Current sensing can either be done in the half bridge leg or in-phase with the motor terminals. Low side leg current sensing is used in this design providing the following benefits:

- As the MCU is on the hot side, isolation is not necessary to measure current
- Use of cost effective non-isolated op amps for amplifying the measured current signal

As shown in Figure 15, a shunt resistor R49 is inserted into the motor phase half-bridge leg. The value of this shunt resistor is decided based on the maximum current value to be measured and the maximum input voltage range of the ADC. In this design, the TLV9062 dual op amp is used in the difference amplifier configuration to monitor current in two phase legs.

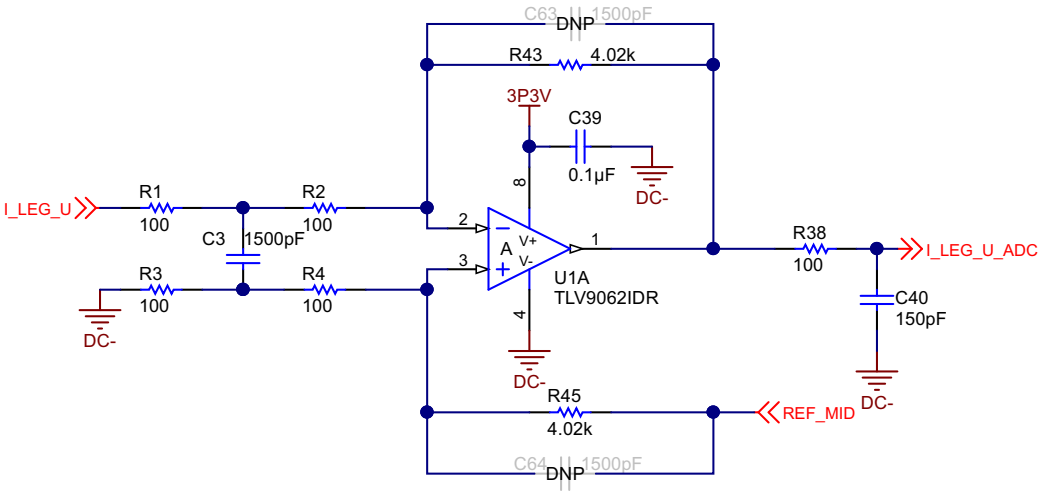


Figure 18. Low-Side Current Sense Difference Amplifier for Phase U

The typical input voltage range of an ADC integrated inside an MCU is 3.3 V.

The gain of the difference amplifier = R43 / (R1 + R2) = 20.1

The op amp U1 is powered by a unipolar power supply of 3.3 V, but the current to be measured is bidirectional. A 1.65-V reference signal REF_MID is used to level shift the bidirectional input voltage of the difference amplifier to the 0- to 3.3-V range. A 50-mV margin is provided on the op amp output from both the power and GND rails of the op amp. This results in a useful measurement range of 3.2 V.

The input voltage range of op amp = 3.2 / 20.1 = 0.1592 V

A 4-mΩ shunt resistor is used for measuring current.

The current measurement range = 0.1592 / 4 m = 39.8 A_{PP} = 14.07 A_{RMS}

This allows for measurement of the nominal inverter output current rating of 10 A_{RMS} with ≈ 40 % margin for short term overloading of the inverter.

Maximum power dissipated in shunt resistor = $(14.07)^2 \times 0.004 = 0.79$ W

The difference amplifier input is low-pass filtered using R1, C3, and R3. A single-ended low-pass RC filter comprising of R38 and C40 is placed near the input to the control card to filter any noise pickup on the op amp output PCB track.

The 1.65-V reference for the level shifter is generated using the TLV431 shunt regulator as shown in Figure 19. A 300-Ω resistor R63 is used to limit the current into the shunt regulator. The voltage divider for setting the reference voltage is calculated using Equation 2.

$$REF\_MID = \left(1 + \frac{R54}{R59}\right) V_{REF} \quad (2)$$

R59 is selected to be 10 kΩ. V_{REF} is 1.24 V. R54 is calculated to be 3.3 kΩ.

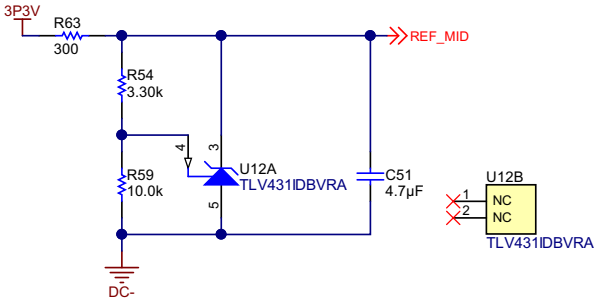


Figure 19. Level Shifting Reference Generation for Difference Amplifier

A 4.7-µF bulk capacitor is used on the output for stability according to Figure 20.

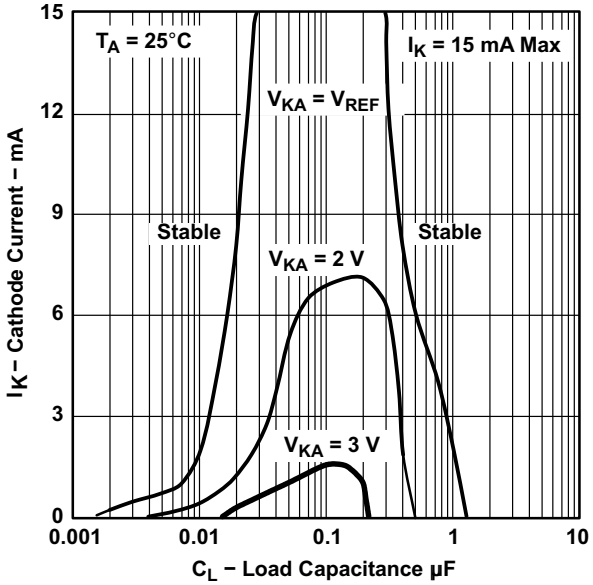


Figure 20. TLV431 Stability Boundary Condition

2.3.6 IGBT Module Temperature Sensing

Temperature feedback of the IGBT power module is necessary for overtemperature shutdown as well as derating the output of the inverter at higher temperatures. Module temperature is measured using the NTC integrated inside the module. The NTC is the standard "KG3B" temperature sensor with a nominal resistance value of 5 kΩ ± 5% at 25ºC.

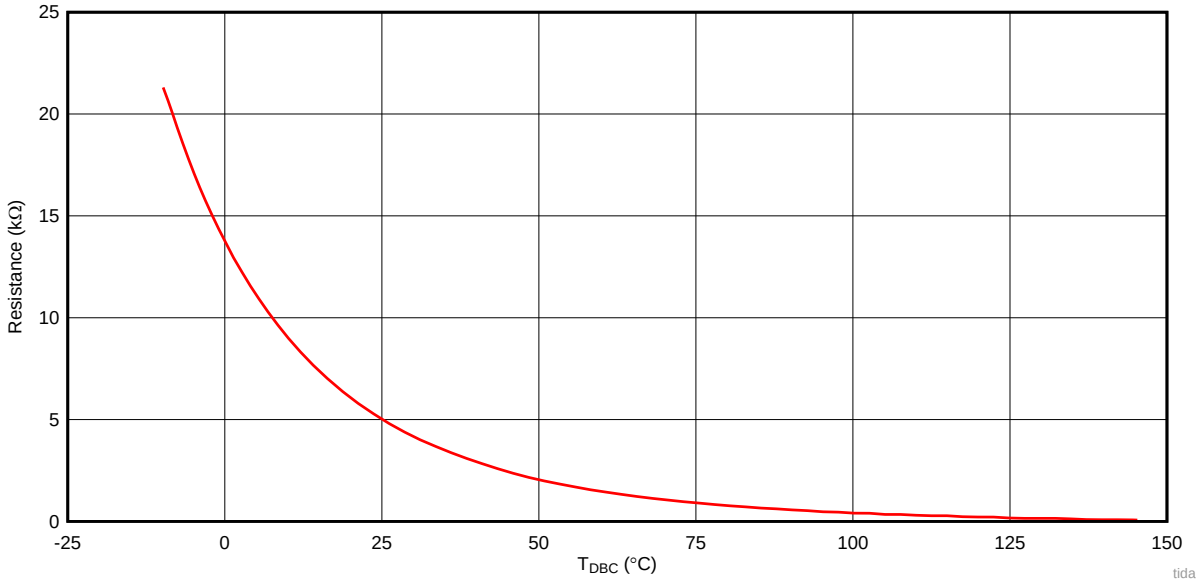


Figure 21. NTC Characteristics

The resistor divider is formed using R50 and the NTC resistor as shown in Figure 22. R64, which is not populated, can be connected in parallel to the NTC to improve the linearity of the NTC measurement.

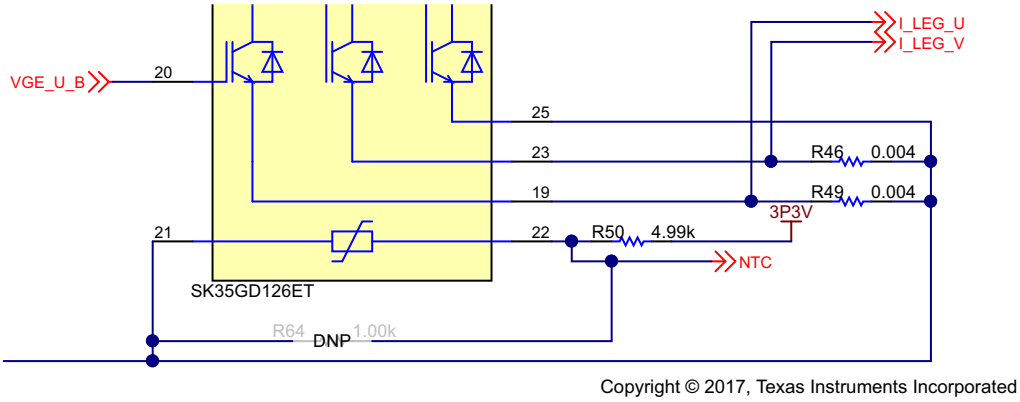


Figure 22. Temperature Sensing Using IGBT Module Integrated NTC

The voltage across the NTC resistor is buffered using U10 (TLV6001) in the voltage follower configuration (see Figure 23) and then filtered with a low-pass RC filter comprising of R55 and C49 before connecting it to the controller. The temperature can be calculated in software using Equation 3 and Equation 4.

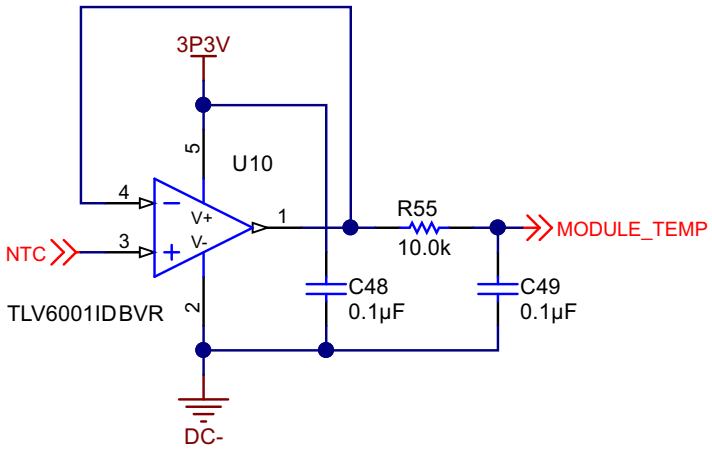


Figure 23. NTC Voltage Sense Buffer

$$R_{NTC}(T) = R50\left(\frac{Module\_temp}{3.3 - Module\_temp}\right) \quad (3)$$

$$T = \frac{1}{\left[\frac{\ln\left(\frac{R_{NTC}(T)}{R_{25}}\right)}{B_{(25/85)}} + \frac{1}{25}\right]} \quad (4)$$

where:

- T is the temperature of the IGBT module direct bonded copper substrate
- $R_{NTC}(T)$ is the NTC resistance at temperature T calculated from the voltage drop across the NTC
- R_{25} is the NTC resistance at 25ºC available from the IGBT module datasheet
- $B_{(25/85)}$ is the B-constant of the NTC resistor

2.3.7 Reinforced Isolated Communication

In this reference design, the safety isolation has been moved to the communication link between the hot-side MCU and the external communication interface. JTAG interface is provided for the real-time debug of the controller and UART interface for serial communication. Reinforced isolated wide body (8-mm creepage and clearance) digital isolators ISO7741 are used to isolate the JTAG and UART signals as shown in Figure 24. The primary- and secondary-side enable signals are connected to their respective power supply rails. The isolator channels are always enabled.

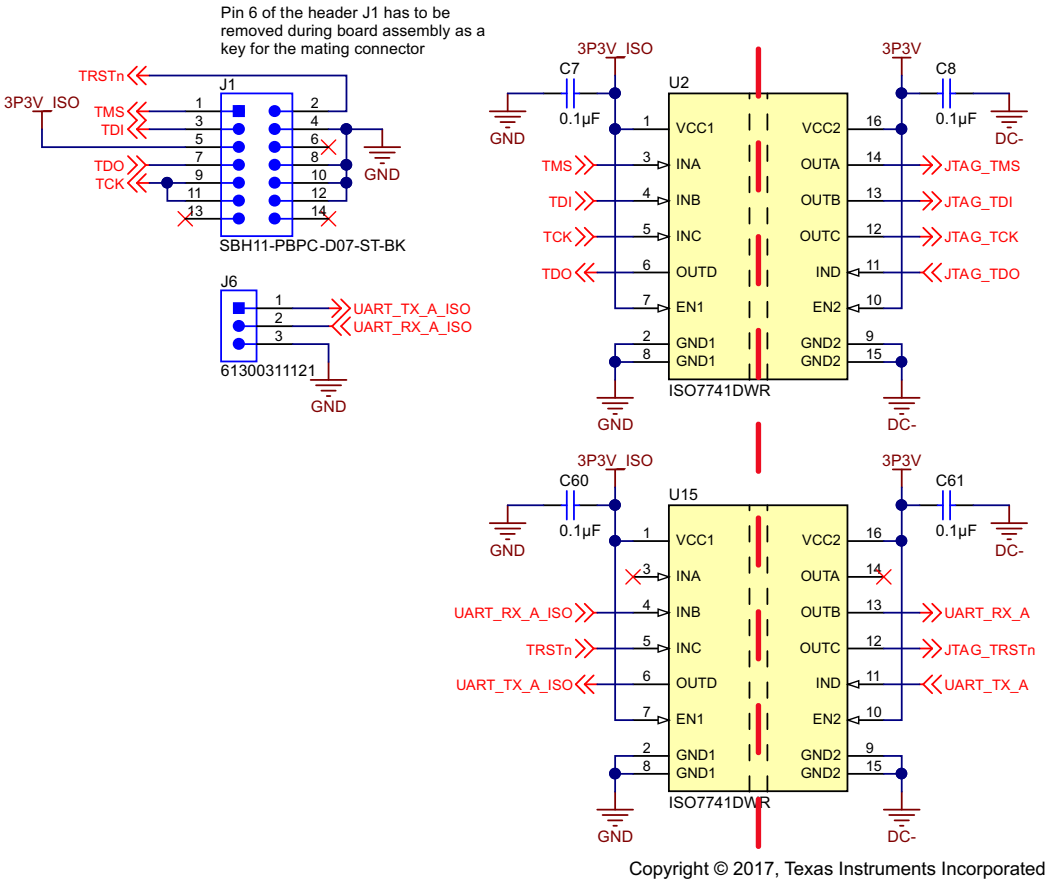


Figure 24. Reinforced Isolated JTAG and UART Interface

Each of the digital isolators have four channels with three channels in forward direction and one channel in the reverse direction. The JTAG signals from an external debug probe are connected to the standard 14 pin JTAG interface header J1. The JTAG signals TMS, TDI, TCK, TDO, and TRSTn are isolated. The UART transmit and receive signals UART_TX and UART_RX are isolated and connected to header J6.

2.3.8 Reinforced Isolated Power Supply Generation

A reinforced isolated 3.3-V power supply is required for the cold side of the digital isolators and for the JTAG interface. The SN6501 is a push-pull transformer driver that helps in generating isolated power rails from the 5-V input supply in this design. A 1-µF bulk capacitor C58 is placed near the transformer hot-side center tap to minimize switching loops. The transformer used has a 1.3:1 turns ratio and has a dielectric isolation rating of 5000 V_{RMS} for 1 minute. The creepage and clearance distance between the primary and the secondary of the transformer is 8 mm. On the cold side of the transformer, diodes D5 and D6 rectify the transformer output onto 1-µF bulk capacitor C57. An LDO TLV70233 is used to generate a 3.3-V rail for the isolated side.

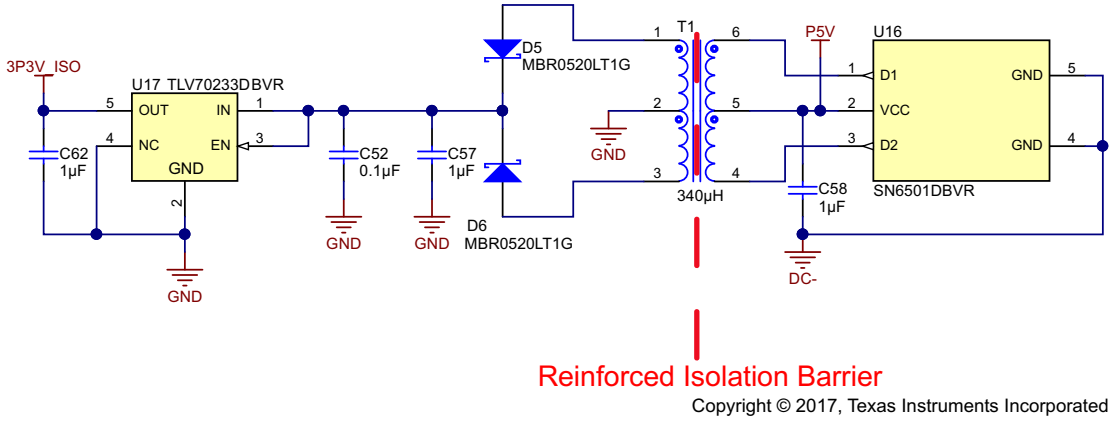


Figure 25. Isolated 3.3-V Power Supply Generation

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

Figure 26 shows the top view of the PCB. The DC bus input connector J7 and the three-phase motor output connector J8 are indicated. The 15-V gate driver power supply, 5-V control card supply, and 3.3-V low-voltage sense circuit supply are to be connected to J5 in the order shown in Figure 26. A dual in-line edge connector socket is used for the 180-pin C2000 control card. The dual core Delfino™ F28379D control card is used for testing this design. J6 is the 3-pin header for connecting the reinforced isolated UART signals. J1 is the 14-pin reinforced isolated interface for connecting the JTAG debug probe. Note that the pin 6 of the header J1 has to be removed as a key for the JTAG debug probe connector. The red LED indicator shown lights up as soon as the DC-link voltage is above 50 V. The LED acts as a warning that the board is energized and must not be touched.

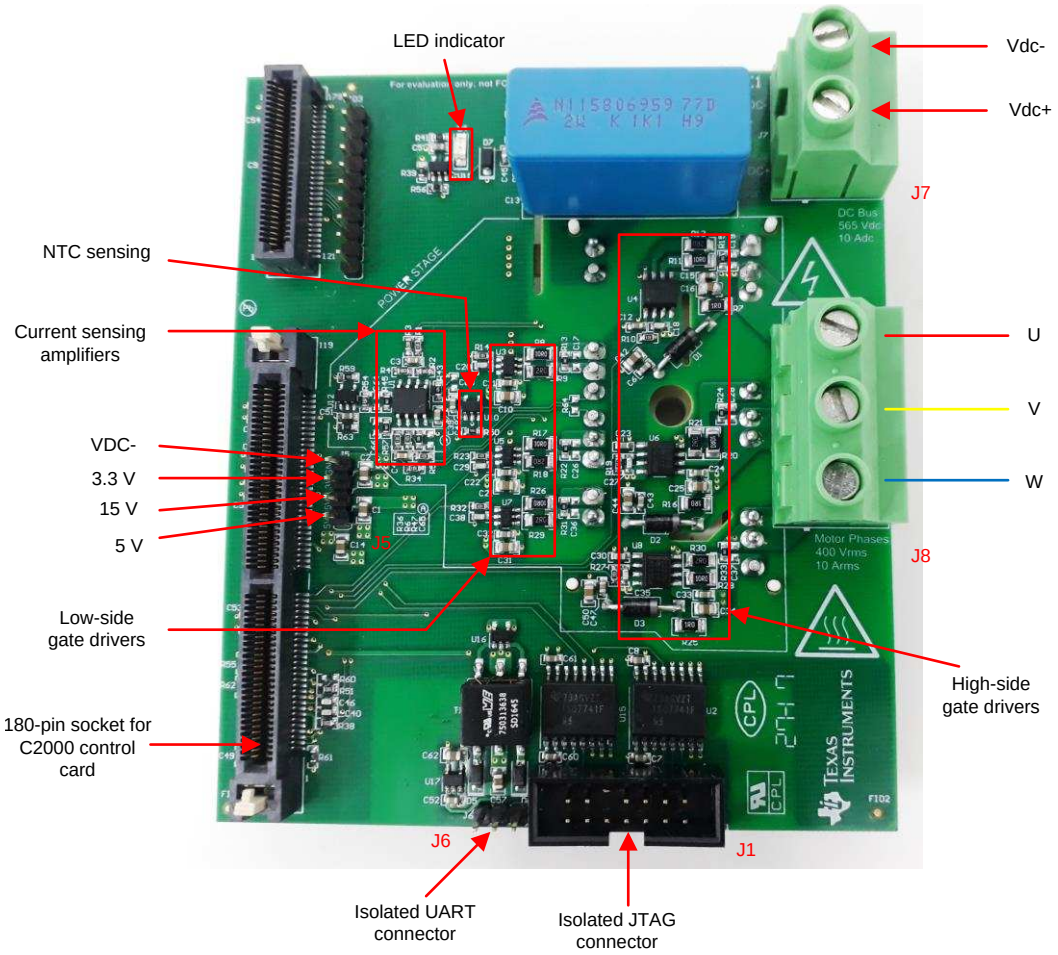


Figure 26. Top View of TIDA-01456 PCB

Figure 27 shows the high-voltage hot side highlighted in red and the low-voltage cold side highlighted in yellow with the reinforced isolation barrier in between. The creepage and clearance distance across the barrier is 8 mm. The digital isolators are placed across the isolation barrier.

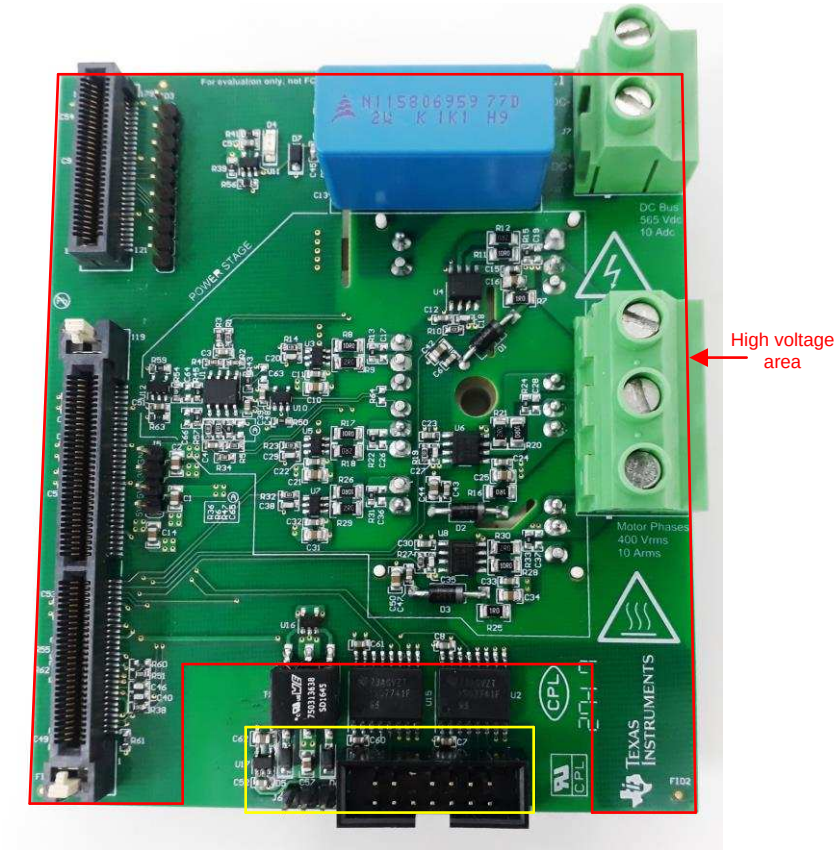


Figure 27. High-Voltage Hot Side, Isolated Low-Voltage Cold Side, and Isolation Barrier

Figure 28 shows the bottom view of the PCB. The current sense shunt resistors are indicated on the bottom side. The IGBT module pad has to be connected to the heat sink. Thermal compound has to be used between the pad and the heat sink and the module tightly coupled to the heat sink with a single screw as shown in Figure 29. Choose an appropriate heat sink based on the maximum continuous power to be dissipated.

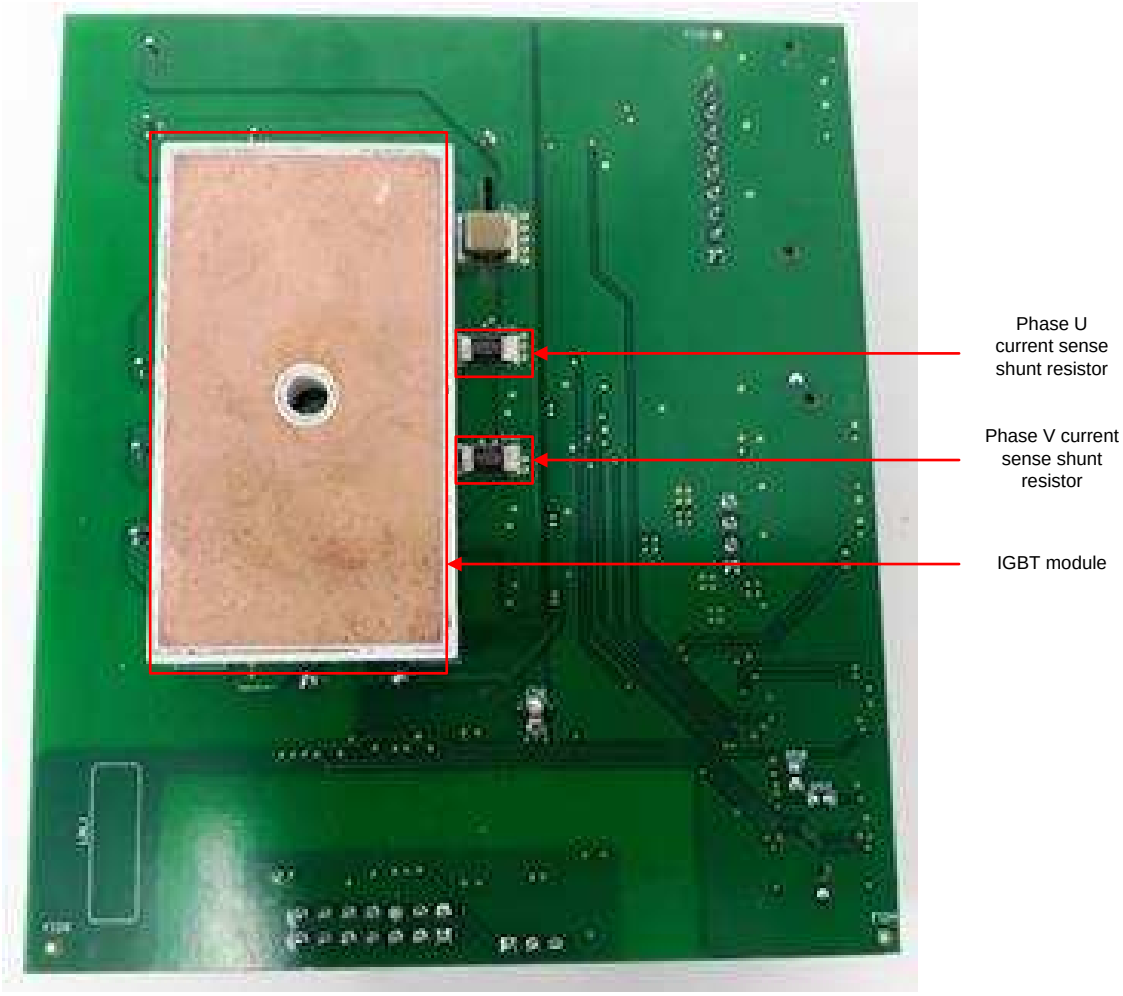


Figure 28. Bottom View of TIDA-01456

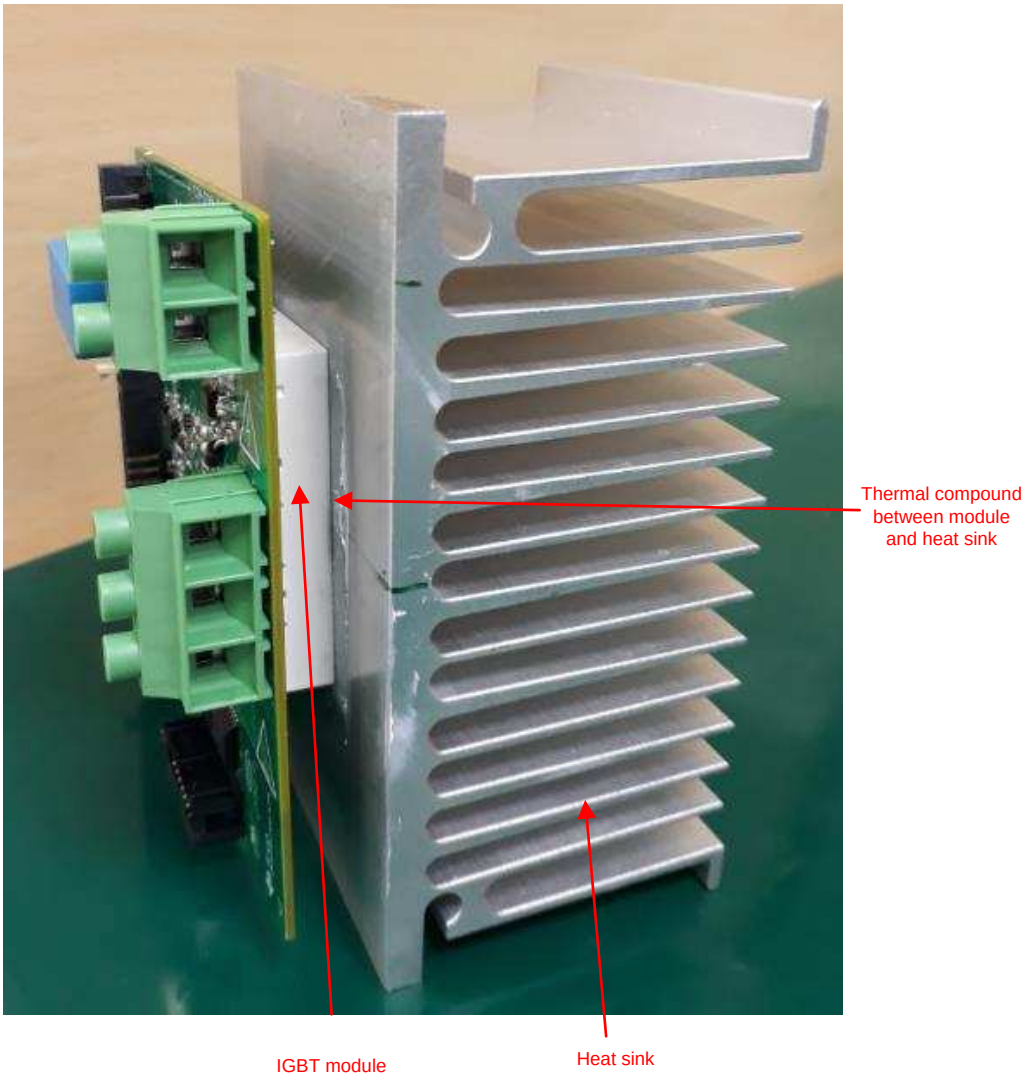


Figure 29. TIDA-01456 Connected to Heat Sink

3.1.2 Controller Interface Socket

The 180-pin control card is mounted in the dual in-line socket J3 and J2 as shown in Figure 30. The pin functions used on this PCB are described in Table 3.

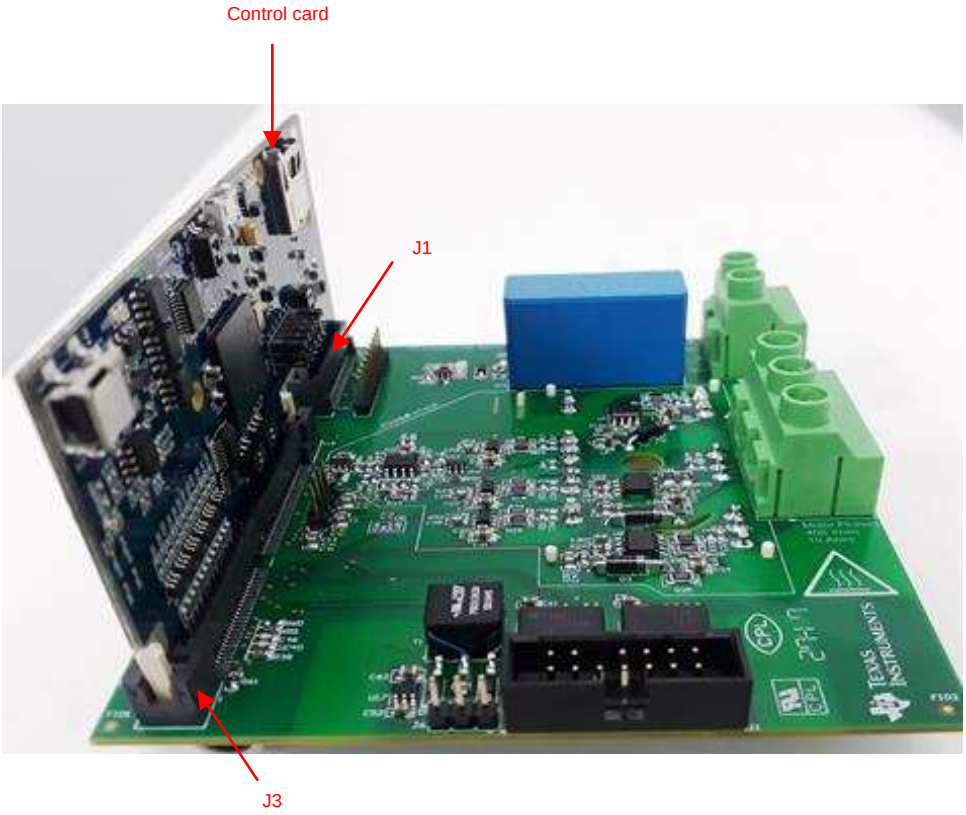


Figure 30. Control Card Connection to TIDA-01456

Table 3. TIDA-01456 Interface to Control Card

TIDA-01456 PINOUT	C2000 CONTROL CARD PINOUT	PIN NO		C2000 CONTROL CARD PINOUT	TIDA-01456 PINOUT
3P3V	JTAG-EMU1	1	2	JTAG-EMU0	3P3V
JTAG_TMS	JTAG_TMS	3	4	JTAG-TRSTN	JTAG_TRStn
JTAG_TCK	JTAG_TCK	5	6	JTAG-TDO	JTAG_TDO
DC-	GND	7	8	JTAG-TDI	JTAG_TDI
—	ADC1 (and/or DACA)	9	10	GND	DC-
—	ADC1 (and/or DACB)	11	12	ADC2	—
DC-	GND	13	14	ADC2	—
I_LEG_U_ADC	ADC1 (and/or CMPIN+)	15	16	GND	DC-
I_LEG_V_ADC	ADC1	17	18	ADC2	I_LEG_U_ADC
DC-	GND	19	20	ADC2	—
I_LEG_V_ADC	ADC1 (and/or CMPIN+)	21	22	GND	DC-
—	ADC1	23	24	ADC2	MODULE_TEMP
I_LEG_V_ADC	ADC (and/or CMPIN+)	25	26	ADC2	—
—	ADC	27	28	ADC	—
DC-	GND	29	30	ADC	—
—	ADC	31	32	Rsv	—
—	ADC	33	34	ADC	—
DC-	GND	35	36	ADC	—

Table 3. TIDA-01456 Interface to Control Card (continued)

TIDA-01456 PINOUT	C2000 CONTROL CARD PINOUT	PIN NO		C2000 CONTROL CARD PINOUT	TIDA-01456 PINOUT
—	ADC	37	38	GND	DC-
V_DCBUS	ADC	39	40	ADC	—
—	Rsv	41	42	ADC	—
—	VREFLO on certain MCU	43	44	Rsv	—
—	VREFHI on certain MCU	45	46	GND	DC-
DC-	GND	47	48	5V0	P5V
PWM_U_T	PWM1A	49	50	PWM3A	PWM_W_T
PWM_U_B	PWM1B	51	52	PWM3B	PWM_W_B
PWM_V_T	PWM2A	53	54	PWM4A	—
PWM_V_B	PWM2B	55	56	PWM4B	—
—	PWM5A	57	58	PWM7A or TZ1	—
—	PWM5B	59	60	PWM7B or TZ2	—
—	PWM6A	61	62	PWM8A or TZ3	—
—	PWM6B	63	64	PWM8B or TZ4	—
DC-	GND	65	66	Rsv	—
—	SPISIMOA	67	68	QEP1A (McBSP-MDXA)	—
—	SPISOMIA	69	70	QEP1B (McBSP-MDRA)	—
—	SPICLKA	71	72	QEP1S (McBSP-MFSXA)	—
—	SPISTEA	73	74	QEP1I (McBSP-MCLKXA)	—
—	CAP1 or SPISIMOB	75	76	SCIRXA/UARTRXA	UART_RX_A
—	CAP2 or SPISOMIB	77	78	SCITXA/UARTTXA	UART_TX_A
—	CAP3 or SPICLKB	79	80	CANRXA	—
—	CAP4 or SPISTEB	81	82	CANTXA	—
DC-	gnd	83	84	5V0	P5V
—	I2CSDAA	85	86	GPIO	—
—	I2CSCLA	87	88	GPIO	—
—	GPIO	89	90	GPIO	—
—	GPIO	91	92	GPIO	—
—	GPIO	93	94	GPIO	—
—	GPIO	95	96	GPIO	—
DC-	GND	97	98	5V0	P5V
—	SD-D1	99	100	QEP2A or GPIO	—
—	SD-C1	101	102	QEP2B or GPIO	—
—	SD-D2	103	104	QEP2S or GPIO	—
—	SD-C2	105	106	QEP2I or GPIO	—
—	SD-D3	107	108	GPIO (McBSP-MCLKRA)	—
—	SD-C3	109	110	GPIO (McBSP-MFSRA)	—
DC-	GND	111	112	5V0	P5V
—	Rsv	113	114	Rsv	—
—	Rsv	115	116	Rsv	—
—	Rsv	117	118	Rsv	—
—	Rsv	119	120	Device Reset (Active low)	—
—	GPIO	121	122	GPIO	—
—	GPIO	123	124	GPIO	—
—	GPIO	125	126	GPIO	—
—	GPIO	127	128	GPIO	—
—	GPIO	129	130	GPIO	—

Table 3. TIDA-01456 Interface to Control Card (continued)

TIDA-01456 PINOUT	C2000 CONTROL CARD PINOUT	PIN NO		C2000 CONTROL CARD PINOUT	TIDA-01456 PINOUT
—	GPIO	131	132	GPIO	—
—	GPIO	133	134	GPIO	—
DC-	GND	135	136	Rsv	—
—	GPIO	137	138	Rsv	—
—	GPIO	139	140	Rsv	—
GPIO-74	GPIO	141	142	Rsv	—
GPIO-76	GPIO	143	144	Rsv	—
GPIO-78	GPIO	145	146	Rsv	—
GPIO-80	GPIO	147	148	Rsv	—
GPIO-82	GPIO	149	150	Rsv	—
GPIO-84	GPIO	151	152	Rsv	—
GPIO-86	GPIO	153	154	Rsv	—
GPIO-88	GPIO	155	156	Rsv	—
DC-	GND	157	158	5V0	P5V
—	GPIO	159	160	GPIO	—
—	GPIO	161	162	GPIO	—
—	GPIO	163	164	GPIO	—
—	GPIO	165	166	GPIO	—
—	GPIO	167	168	GPIO	—
—	GPIO	169	170	GPIO	—
—	Rsv	171	172	Rsv	—
—	Rsv	173	174	Rsv	—
—	Rsv	175	176	Rsv	—
—	Rsv	177	178	Rsv	—
DC-	GND	179	180	5V0	P5V

3.1.3 Software

This reference design is tested using software modified from the application report *Sensorless Field Oriented Control of 3-Phase Permanent Magnet Synchronous Motors Using TMS320F2833x*. The incremental build level 2 from the application report is modified as shown in Figure 31. A switch is added to connect either the OUT signal coming from the RG MACRO or the angle variable to the sine cos block. Connecting OUT enables the design to pump sinusoidal current into the motor. Connecting the angle variable, which is made zero, enables driving DC current into the motor. Maximum DC current of ±8 A into a phase switching node is used for showing the switching behavior of the inverter and the gate drive waveforms.

NOTE: DC current is used for ease of triggering the scope and for pumping a high current into the motor without loading the motor shaft.

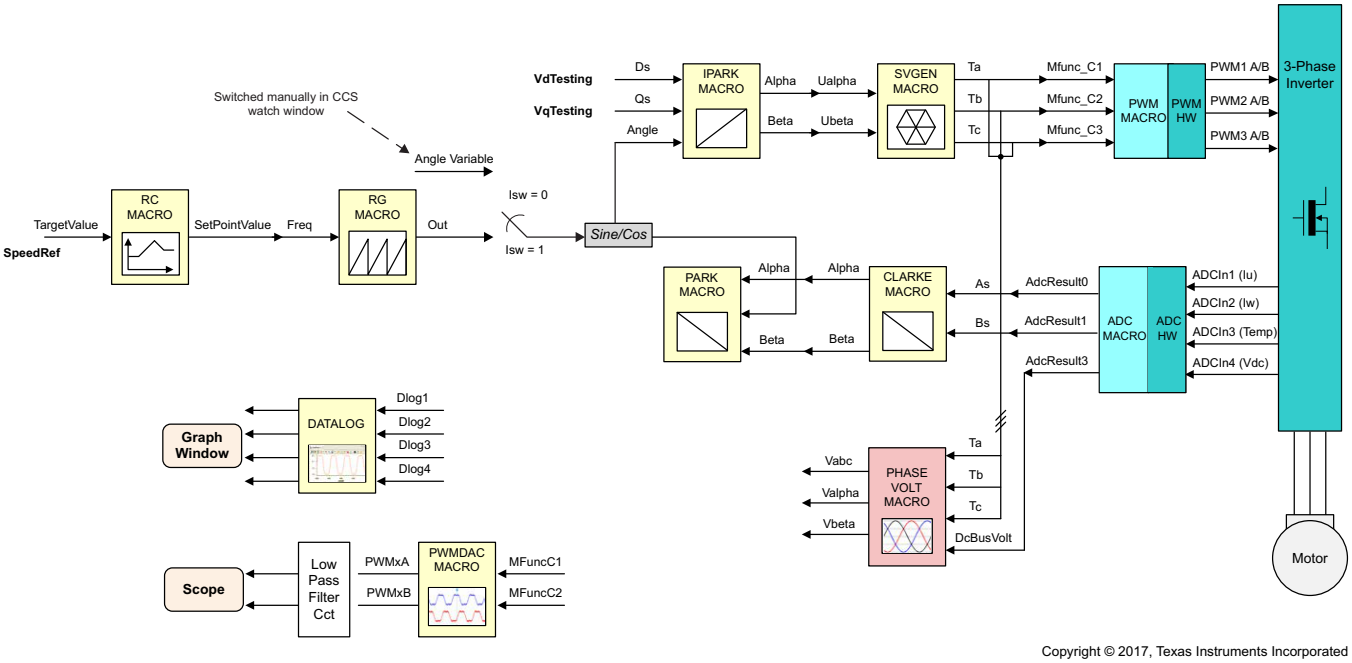


Figure 31. PWM Control Software

3.2 Testing and Results

The focus of the tests is to evaluate the functionality and performance of the gate drive subsystem for the three-phase inverter using the UCC27531 for the low-side switches and the UCC5320SD for the high-side switches.

3.2.1 Test Setup

Figure 32 shows the test setup and Table 4 lists the key test equipment used. The F28379D 180-pin control card is mounted in the socket on the TIDA-01456 board. External DC supplies are used to power 3.3-, 5-, and 15-V DC rails. A high-voltage DC supply is connected to the design DC bus. The motor terminals are connected to the PCB through screw terminal blocks. The controller is debugged through reinforced isolated JTAG channel, which is connected to the laptop through external XDS110 debug probe. Isolated oscilloscope and high-voltage differential probes are used to take most of the scope plots.

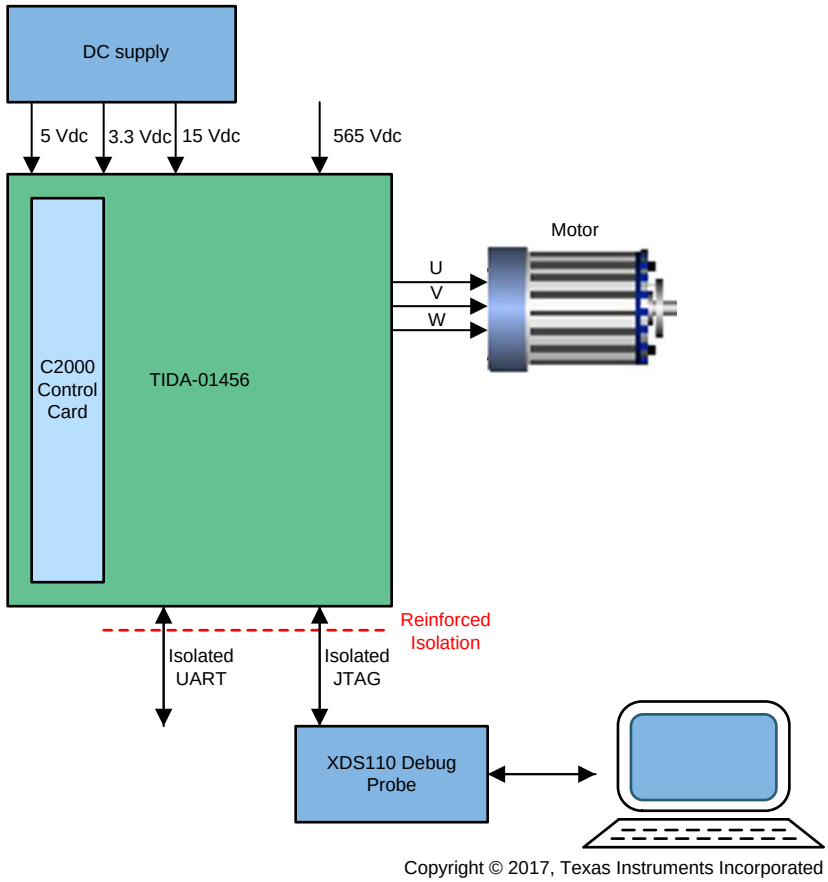


Figure 32. Test Setup

Table 4. Test Equipment Used

DESCRIPTION	PART NUMBER
Isolated oscilloscope	Tektronix TPS2014B
Single-ended probes	Tektronix TPP0200
Differential probe	Tektronix P5200A
Current probe	Keysight N2783B
Current probe amplifier	Agilent N2779A
High-voltage power supply	Ametek SGI 1000/5
Power supply	Keithley 2230G-30-1
Power supply	Agilent E3631A
AC induction motor	3.7 kW, 1460 rpm (0.5 to 100 Hz), 415 V_{RMS} ± 10%, η = 83 %, cosΦ = 0.74, 8.4 A_{MAX}

3.2.2 Test Results

3.2.2.1 UVLO Feature of Gate Drivers

An IGBT requires sufficient ON gate voltage to ensure that it is operating in the saturation region. If due to fault conditions the gate power supply voltage reduces, then there is the risk that the IGBT operates in the linear region. Operation in linear region increases power losses in the IGBT resulting in overheating of the switch and possibly damaging it. This can be avoided by the UVLO feature of the gate drivers. As soon as the gate voltage falls below a threshold, the gate driver output shuts down and prevent the IGBT from operation in linear region.

- Channel 1 (Blue) - Input PWM signal
- Channel 2 (Red) - Gate drive power supply
- Channel 3 (Green) - Output PWM signal

Figure 33 shows the UVLO turnoff threshold for the high-side gate driver to be 11.6 V and Figure 34 the turnon threshold to be 12.4 V. The hysteresis in the threshold levels is 0.8 V.

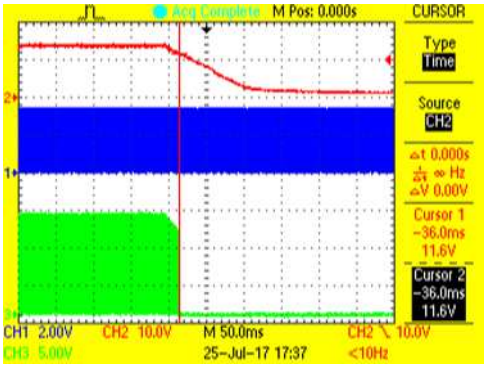


Figure 33. High-Side Gate Driver (UCC5320S) UVLO Turnoff

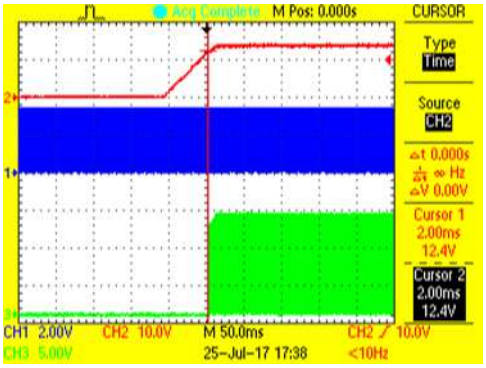


Figure 34. High-Side Gate Driver (UCC5320S) UVLO Turnon

3.2.2.2 PWM Propagation Delay

The propagation delay from the input of the gate driver to the output of the gate driver as shown in Figure 35 is an important parameter in setting the dead time between the high-side and low-side switches.

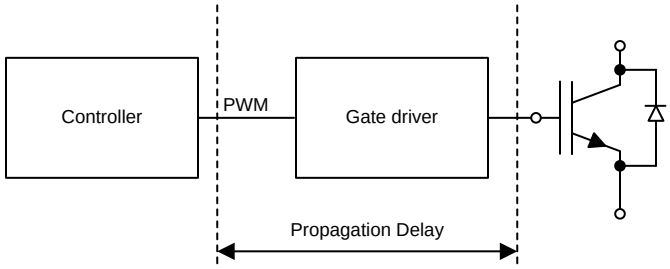


Figure 35. PWM Propagation Delay

Lower variation in the propagation delay difference between the high-side and low-side gate drivers enable setting a lower dead time. Lower dead time provides the following benefits:

- Reduced dead time distortions
- More efficient operation (harmonic losses are reduced)
- Less torque ripple resulting in smoother running motors with less audible noise

3.2.2.2.1 Low-Side Gate Driver Propagation Delay

The propagation delay waveforms for the low-side gate drivers of this reference design are shown in Figure 37 to Figure 42. The delay waveforms are taken according to the datasheet specifications shown in Figure 36. For turnon, the delay is from the V_{IH} threshold of the input PWM waveform to 10% of the rising edge of the output PWM waveform. For turnoff, the delay is measured from the V_{IL} threshold of the input PWM waveform to 90% of the falling edge of the output PWM waveform. The delay variations between all three gate drivers is measured to be less than 1 ns.

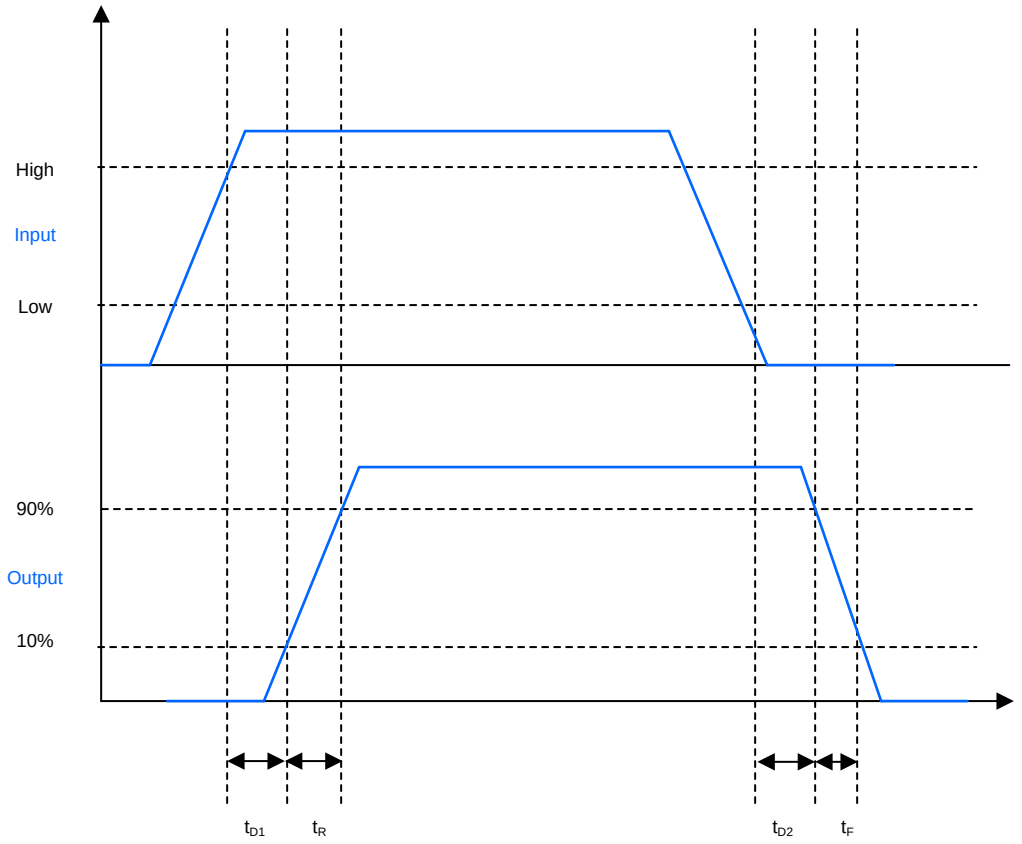


Figure 36. UCC27531 Propagation Delay Specification

- Channel 1 (Blue): Input PWM signal
- Channel 3 (Green): Output PWM signal

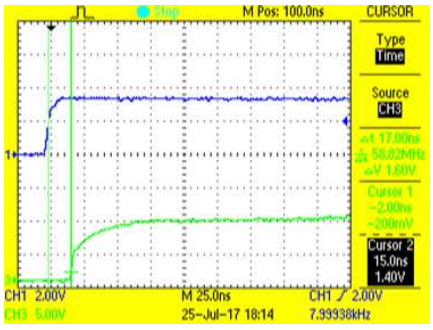


Figure 37. Low-Side Phase U Turnon Propagation Delay (17 ns)

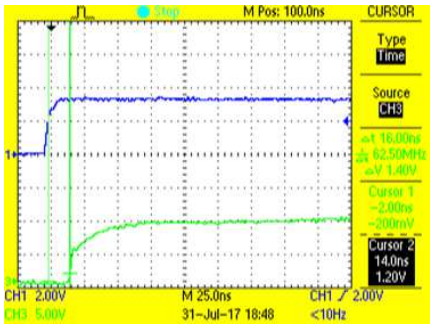


Figure 38. Low-Side Phase V Turnon Propagation Delay (16 ns)

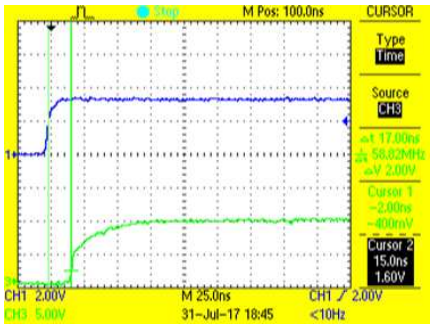


Figure 39. Low-Side Phase W Turnon Propagation Delay (17 ns)

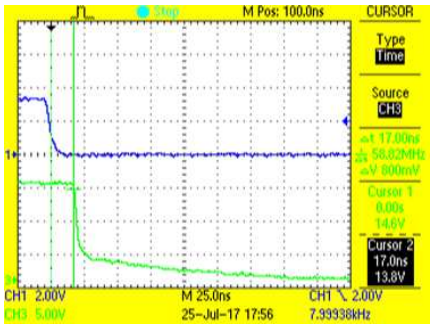


Figure 40. Low-Side Phase U Turnoff Propagation Delay (17 ns)

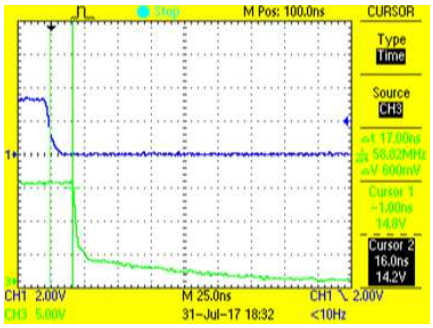


Figure 41. Low-Side Phase V Turnoff Propagation Delay (17 ns)

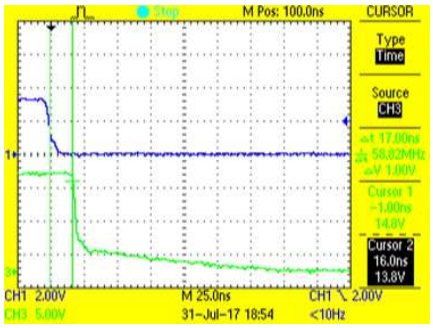


Figure 42. Low-Side Phase W Propagation Delay (17 ns)

3.2.2.2.2 High-Side Gate Driver Propagation Delay

The propagation delay waveforms for the high-side gate drivers are shown in Figure 44 to Figure 49. The delay waveforms are taken according to the datasheet specifications shown in Figure 43. For turnon, the delay is from 50% of the input PWM rising edge to 10% of the output PWM rising edge. For turnoff, the delay is measured from 50% of the input PWM falling edge to 90% of the output PWM falling edge. The delay variations measured between all three gate drivers is less than 2 ns.

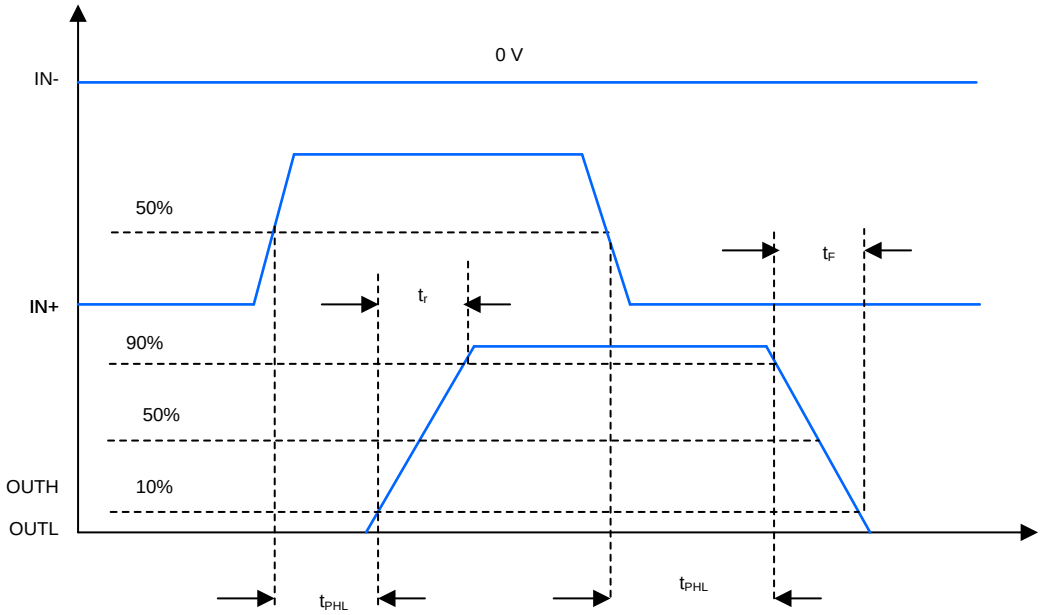


Figure 43. UCC5320S Propagation Delay Specification

- Channel 1 (Blue) input PWM signal
- Channel 2 (Green) output PWM signal

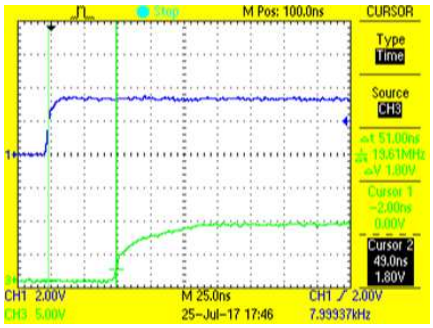


Figure 44. High-Side Phase U Turnon Propagation Delay (51 ns)

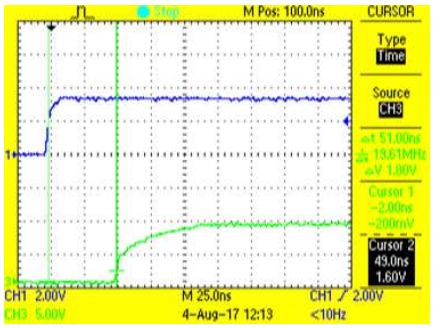


Figure 45. High-Side Phase V Turnon Propagation Delay (51 ns)

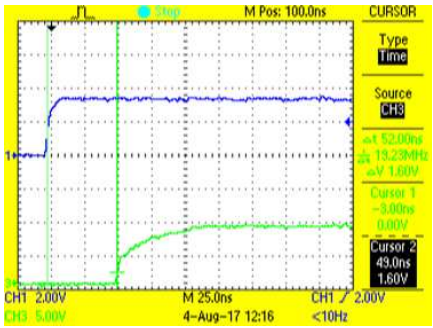


Figure 46. High-Side Phase W Turnon Propagation Delay (52 ns)

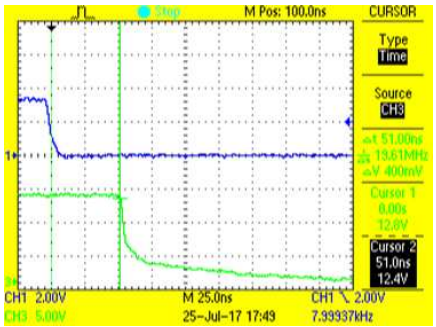


Figure 47. High-Side Phase U Turnoff Propagation Delay (51 ns)

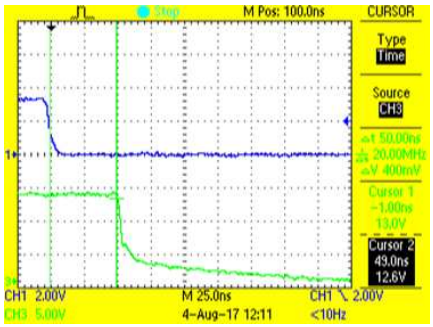


Figure 48. High-Side Phase V Turnoff Propagation Delay (50 ns)

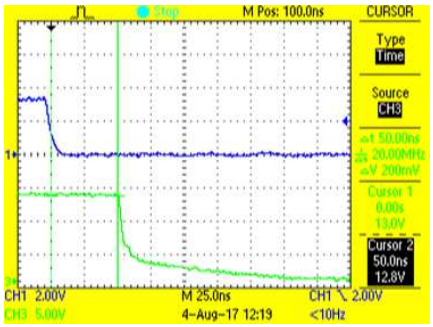


Figure 49. High-Side Phase W Propagation Delay (50 ns)

3.2.2.3 Bootstrap Power Supply Ripple

This reference design uses the bootstrap power supply technique for generating the floating high-side gate driver power supplies from the DC– referenced low side gate driver power supply. The high-side gate voltage ripple is dependent on the low-side switch duty cycle as well as on the phase current amplitude and direction. It is important to ensure that the floating high-side gate voltages do not drop by a magnitude such that it drives the IGBT switch into the linear region or increases the saturation voltage.

For this reference design, the ripple voltage is captured at 10% and 90% duty cycles, ±8-A DC phase current as well as sinusoidal phase current to ensure that the voltage across the bootstrap capacitor does not decrease much. For measuring the worst case ripple voltage waveforms, the minimum inverter switching frequency of 4 kHz is used.

- Channel 1 (Blue): Phase U bootstrapped power supply

NOTE: The DC coupled waveform is on the left side and the AC coupled waveform is on the right side.

- Channel 2 (Red): Phase U current
- Channel 3 (Green): Phase U low-side PWM signal

3.2.2.3.1 Inverter Operated Without Load

The PWM duty cycle is varied from 10% to 90% to capture the maximum and minimum ripple voltage.

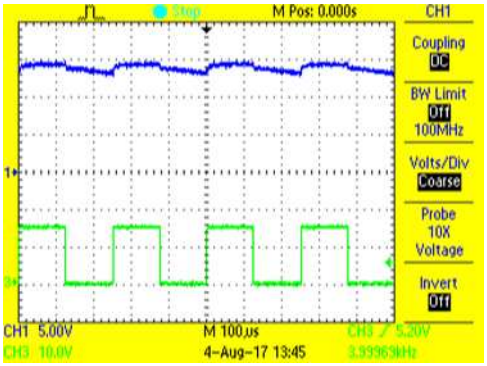


Figure 50. 50% Duty Cycle DC Coupled

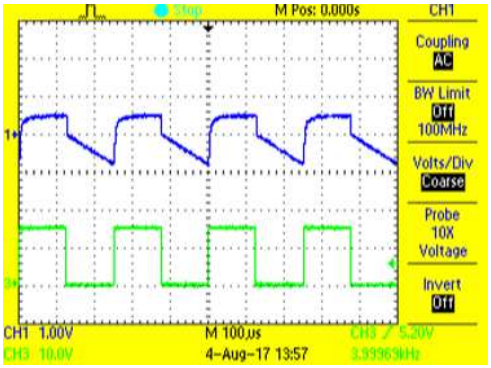


Figure 51. 50% Duty Cycle AC Coupled

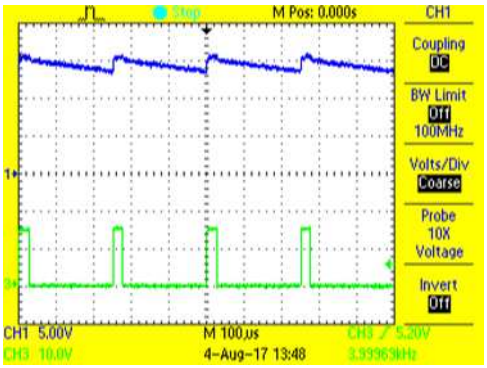


Figure 52. 10% Duty Cycle DC Coupled

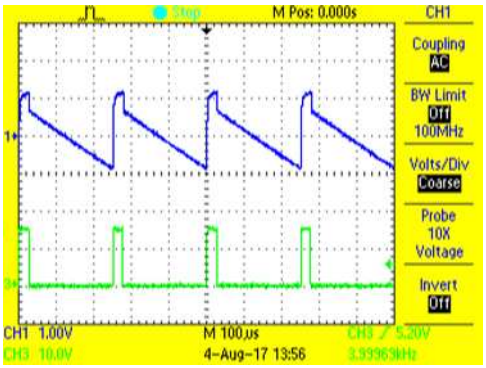


Figure 53. 10% Duty Cycle AC Coupled

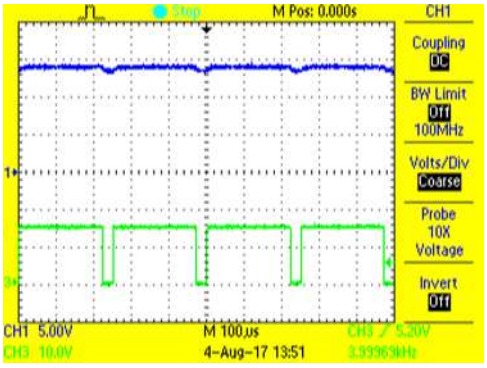


Figure 54. 90% Duty Cycle DC Coupled

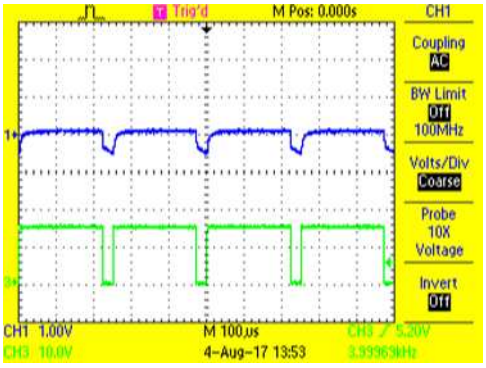


Figure 55. 90% Duty Cycle AC Coupled

3.2.2.3.2 Inverter Operated With DC Load

Figure 56 to Figure 59 show the effect of phase current on the ripple voltage.

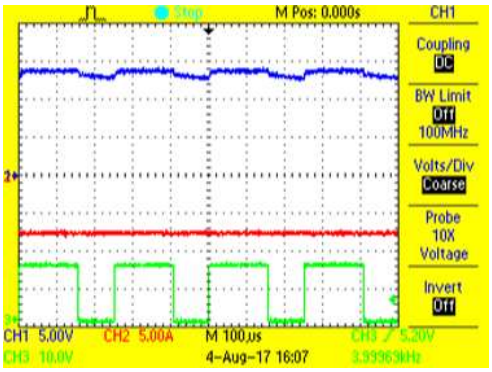


Figure 56. –8-A DC Current in Phase U DC Coupled

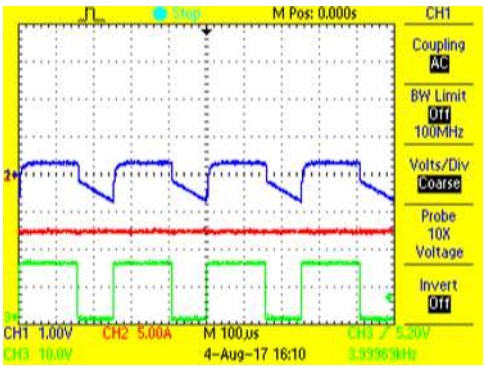


Figure 57. –8-A DC Current in Phase U AC Coupled

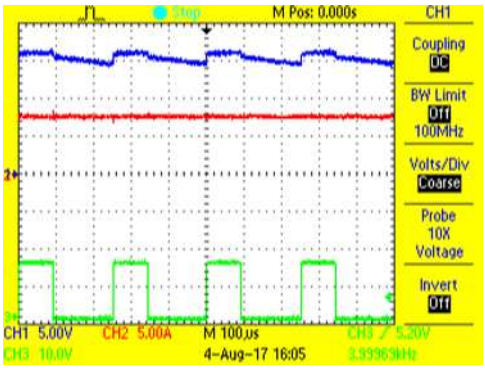


Figure 58. 8-A DC Current in Phase U DC Coupled

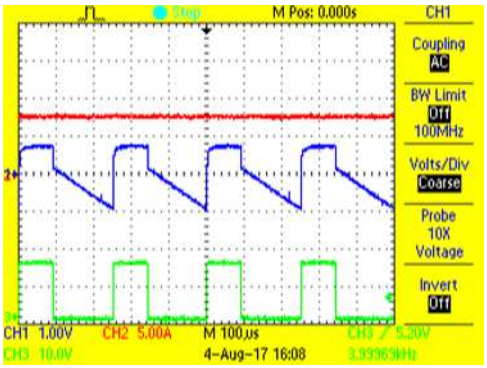


Figure 59. 8-A DC Current in Phase U AC Coupled

3.2.2.3.3 Inverter Operated With Sinusoidal Loading

Figure 60 shows that when the phase current is negative, the bootstrap voltage is lower. This is because the IGBT ON saturation voltage is subtracted from the bootstrap capacitor charge voltage. When the current is positive, the bootstrap voltage is higher. This is because the freewheeling diode of the low-side switch conducts when the current is positive and the diode forward drop gets added to the bootstrap capacitor charge voltage.

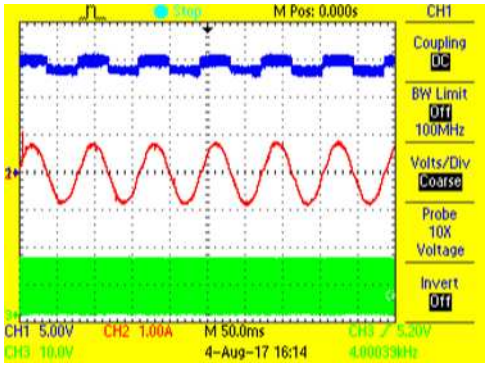


Figure 60. Sinusoidal Current in Phase U

3.2.2.4 Gate Source/Sink Current, Gate Voltages, and Switch Node Voltage Waveforms at Hard and Soft Switching Conditions

This section shows the inverter functional switching waveforms. A positive current (current flowing out of phase node) of 8 A is used for showing the soft switching behavior of the low-side switch and hard switching of the high-side switch. Negative current (current flowing into phase node) of –8 A is used for showing the soft switching behavior of the high-side switch and hard switching of the low-side switch. For all the waveforms, a DC bus voltage of 565-V DC is used.

3.2.2.4.1 Low-Side IGBT Switching Waveforms

Figure 61 to Figure 64 show the turnon and turnoff behavior of the low-side switch:

- Channel 1 (Blue): Low-side IGBT gate to emitter voltage for phase U
- Channel 2 (Red): Gate current for the low-side IGBT for phase U

NOTE: The Channel 2 waveform is measured across the gate resistors and therefore shown in volts. To convert from voltage to current, the ON current waveform is to be divided by an ON resistor of 10 Ω and the OFF current waveform is to be divided by an OFF resistor of 2 Ω.

- Channel 3 (Green): Phase U switch node with respect to DC–

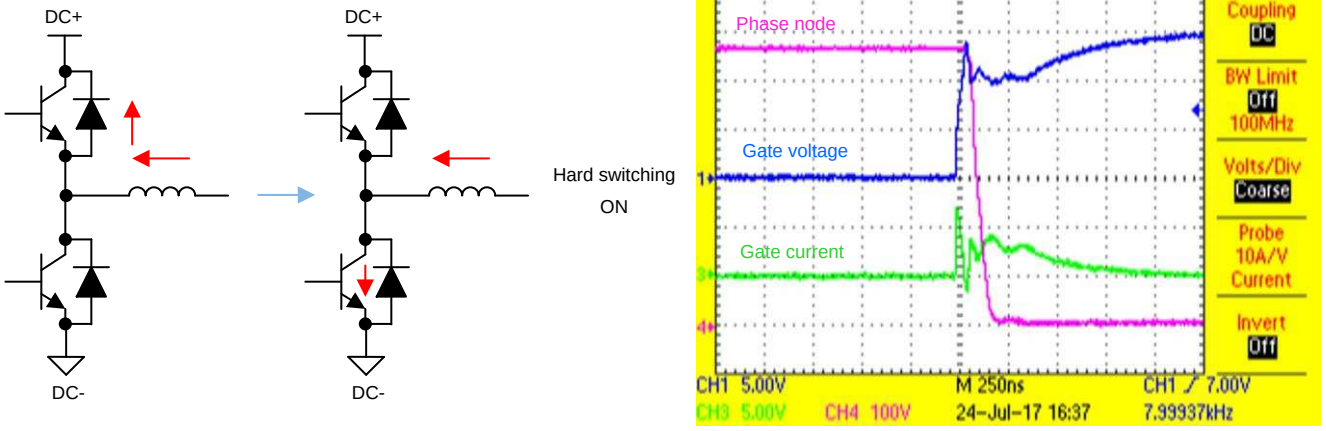


Figure 61. Hard Switch Turnon (Low Side)

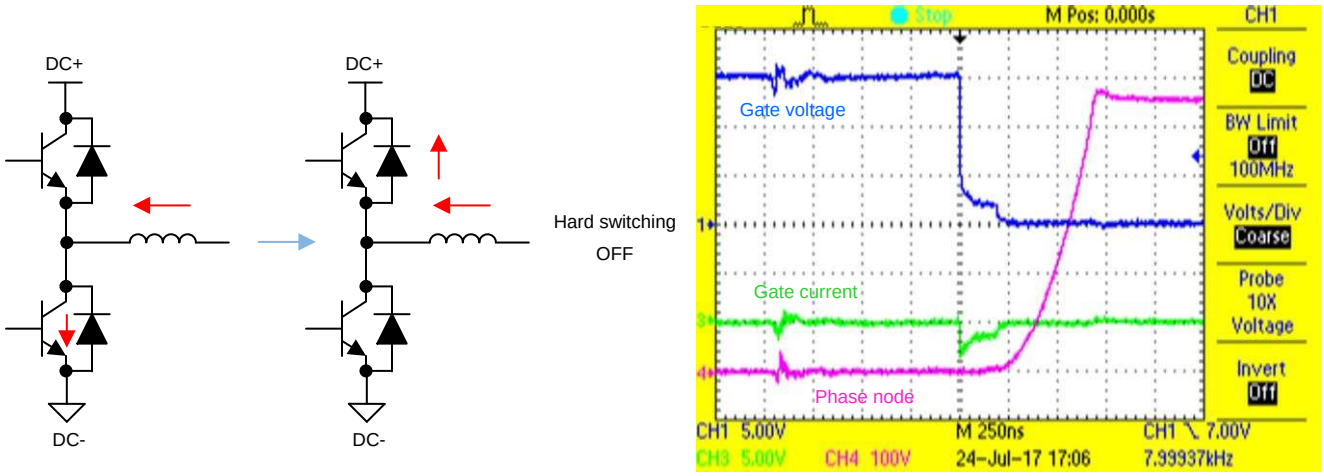


Figure 62. Hard Switch Turnoff (Low Side)

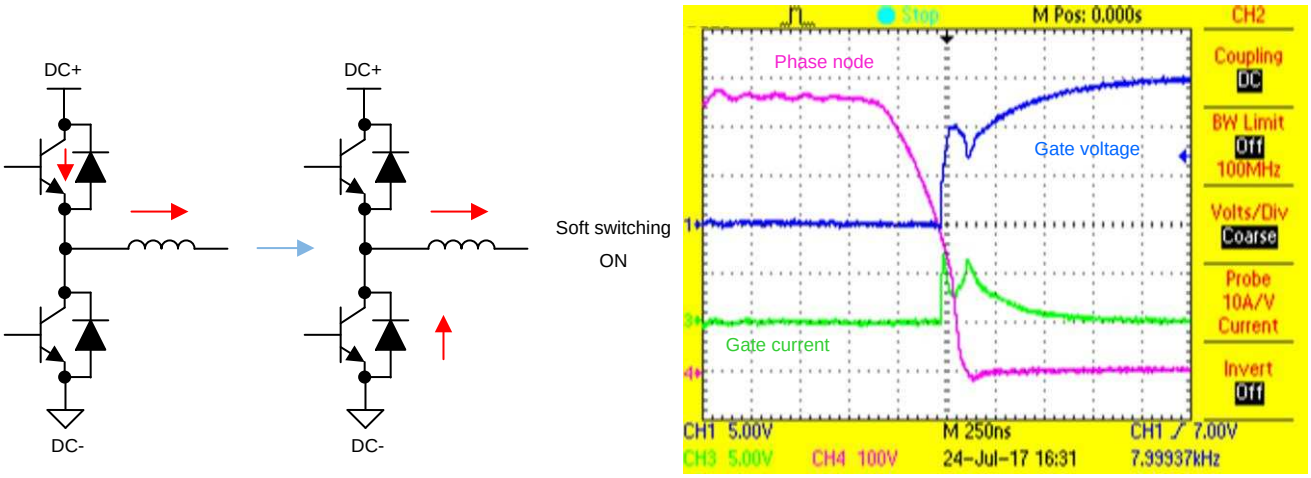


Figure 63. Soft Switch Turnon (Low Side)

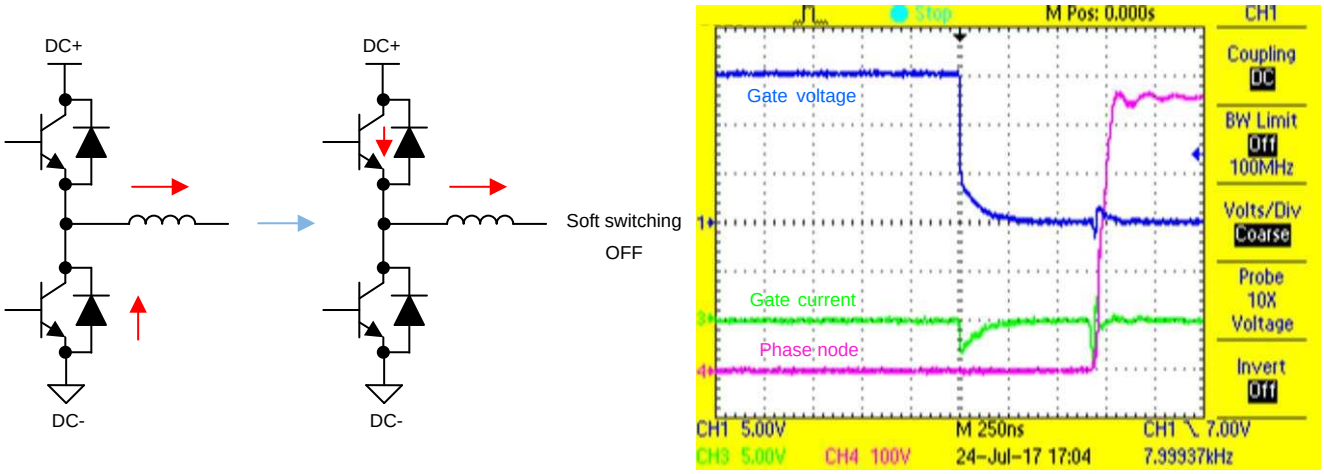


Figure 64. Soft Switch Turnoff (Low Side)

3.2.2.4.2 High-Side IGBT Switching Waveforms

Figure 65 to Figure 68 show the turnon and turnoff behavior of the high-side switch:

- Channel 1 (Blue): High-side IGBT gate to emitter voltage for phase U
- Channel 2 (Red): Gate current for the high-side IGBT for phase U

NOTE: The Channel 2 waveform is measured across the gate resistors and therefore shown in volts. To convert from voltage to current, the ON current waveform is to be divided by an ON resistor of 10 Ω and the OFF current waveform is to be divided by an OFF resistor of 2 Ω.

- Channel 3 (Green): Phase U switch node with respect to DC–

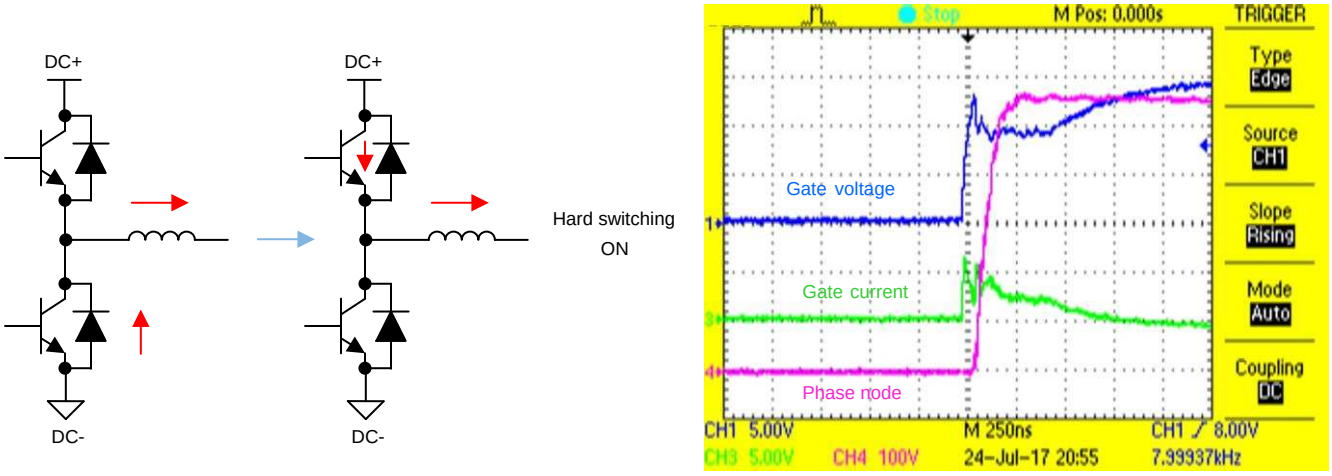


Figure 65. Hard Switch Turnon (High Side)

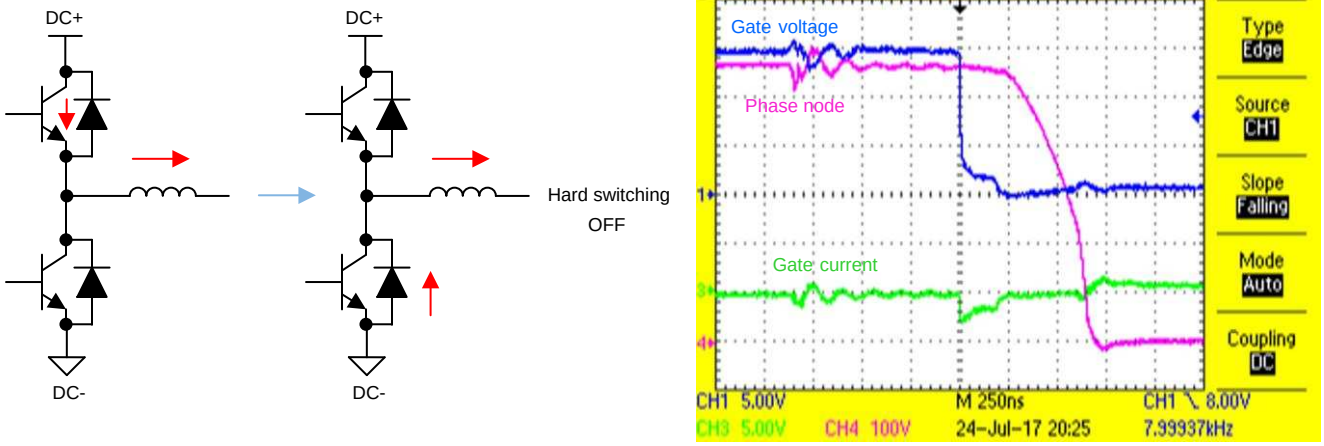


Figure 66. Hard Switch Turnoff (High Side)

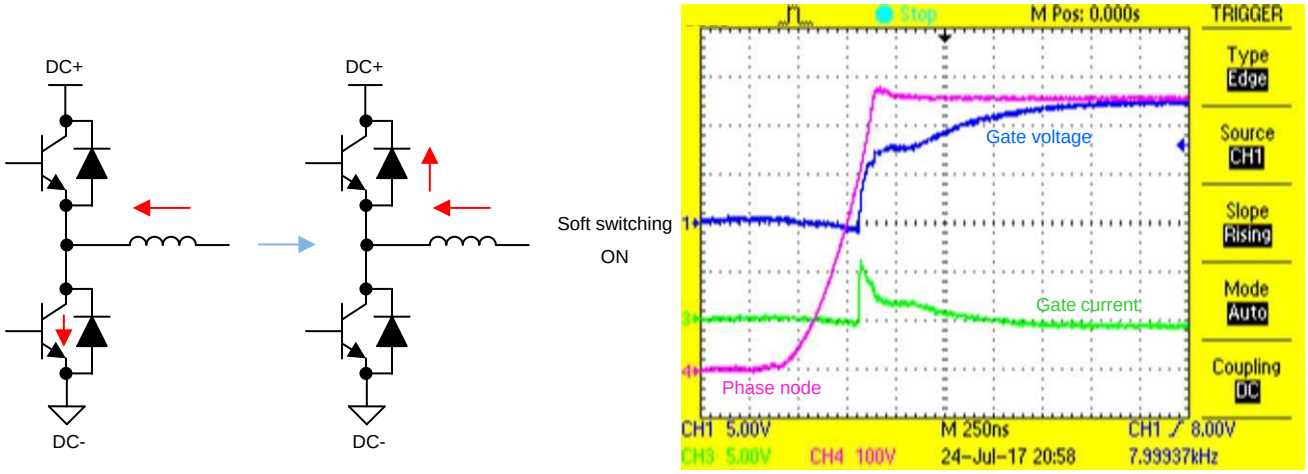


Figure 67. Soft Switch Turnon (High Side)

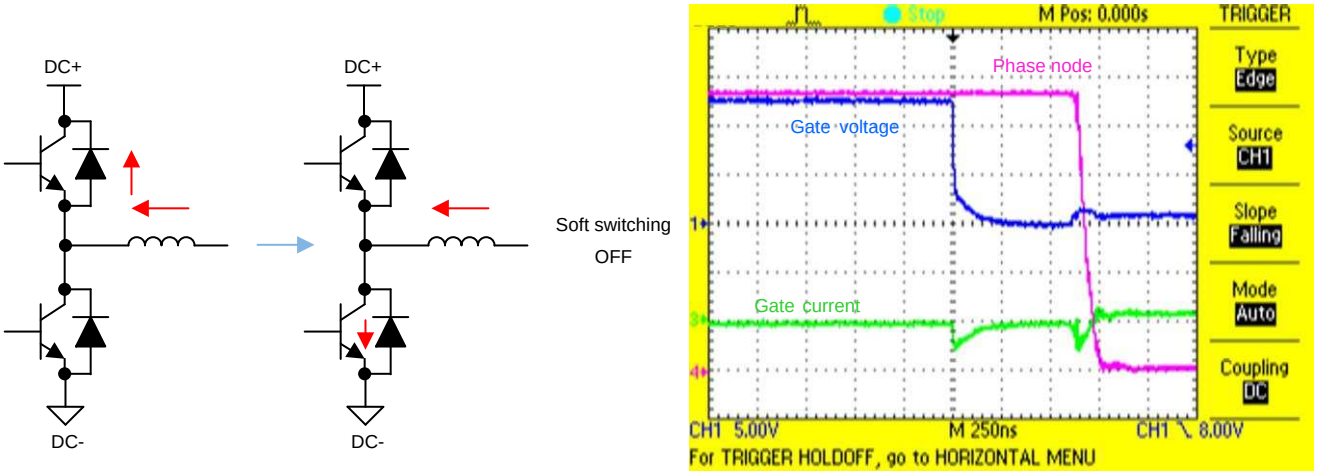


Figure 68. Soft Switch Turnoff (High Side)

3.2.2.5 Temperature of Gate Drivers

An infrared picture of the board is taken to measure the temperature rise of the gate drivers. The DC bus voltage is made zero to capture only the temperature rise due to the gate driver switching. The drivers are operated at 16 kHz (maximum tested inverter switching frequency) for 30 min to bring the gate driver package temperature rise into equilibrium. Figure 69 shows that the self heating of the gate drivers is only ≈ 4°C (22.7°C ambient room temperature).

NOTE: HS_U means high-side gate driver for phase U and LS_U means low-side gate driver for phase U (similarly for the remaining two phases).

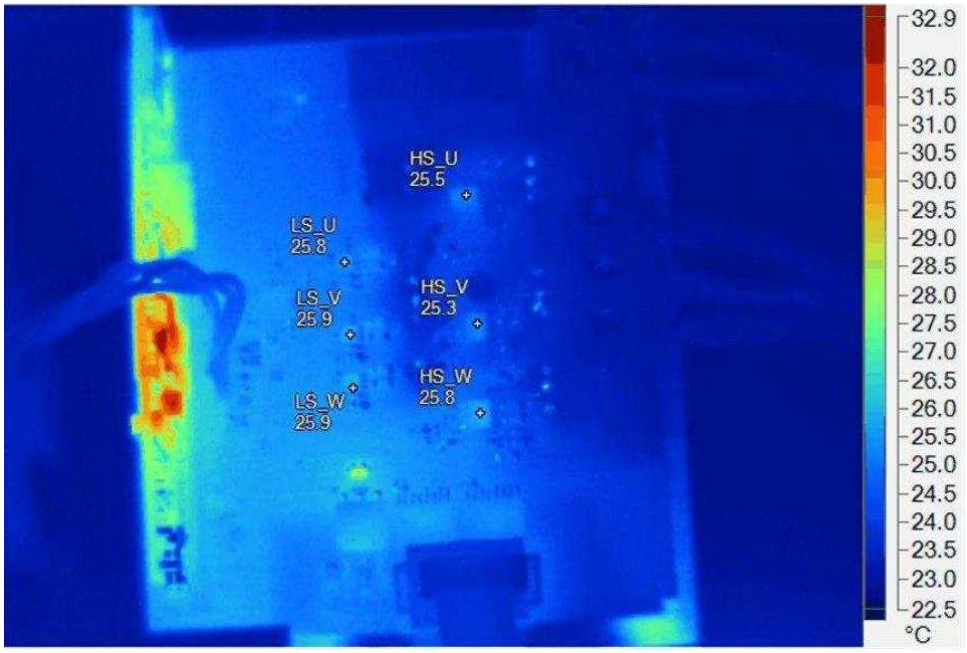


Figure 69. Measurement of Operational Temperature Rise of Gate Drivers

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01456.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01456.

4.3 PCB Layout Recommendations

Layout is very important for proper and reliable operation of the circuit. The layout guidelines are provided in the following sections.

4.3.1 Reinforced Isolation Barrier

Figure 70 shows the isolation barrier and the ground split. The hot-side (high-voltage power side) and the cold-side (isolated low-voltage JTAG and UART communication) copper tracks are separated from each other by a reinforced isolated barrier. The wide body package of the digital isolators are placed across the isolation barrier. The creepage spacing between the hot- and cold-side copper tracks is maintained at a minimum of 8 mm.

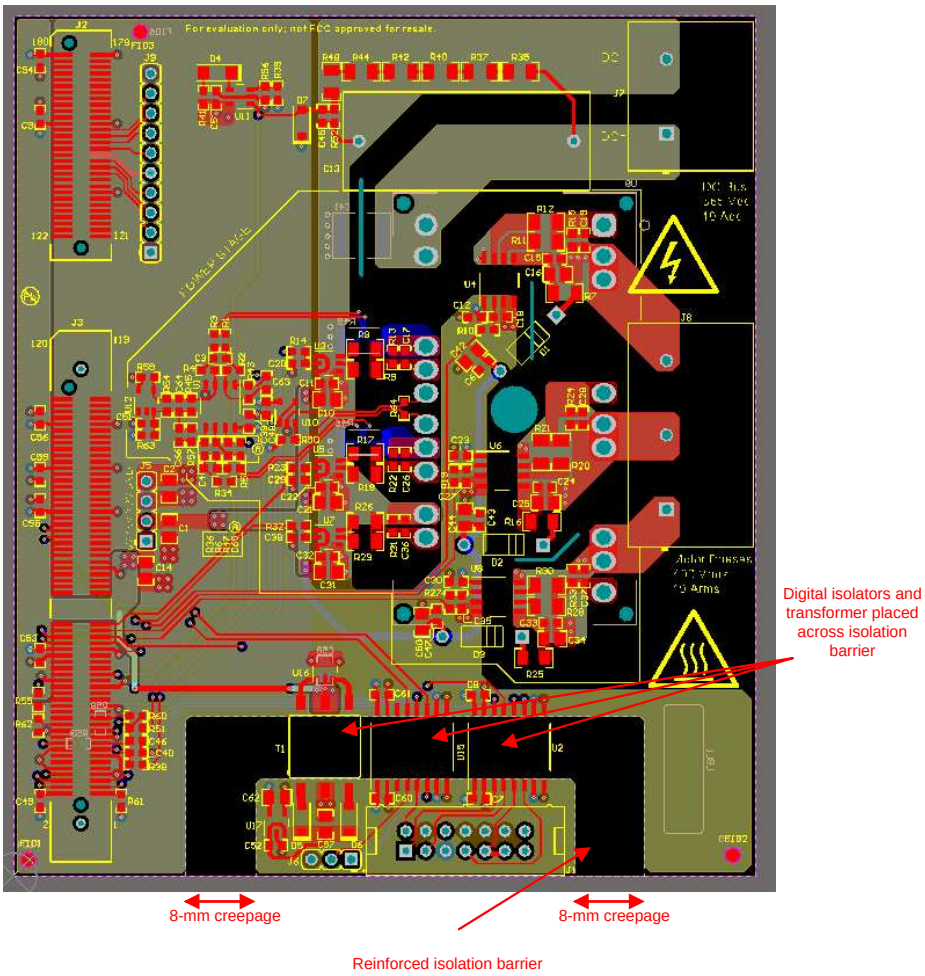


Figure 70. Reinforced Isolation Barrier and Creepage Spacing

4.3.2 Low-Side Gate Driver

- Place the 0.1-µF high-frequency noise decoupling capacitor C11 and the 1-µF bulk capacitor C10 close to the power supply pin of the device.
- Keep the IGBT gate turnon and turnoff loop areas to a minimum. Figure 71 shows the gate current sourcing path and Figure 72 shows the gate current sinking path. Gate tracks are made wide to reduce parasitic track inductance, which may slow down the switching speed of the IGBT.
- R14 and C20 is the low-pass RC filter on the PWM input, and it has to be kept close to the PWM IN+ pin.

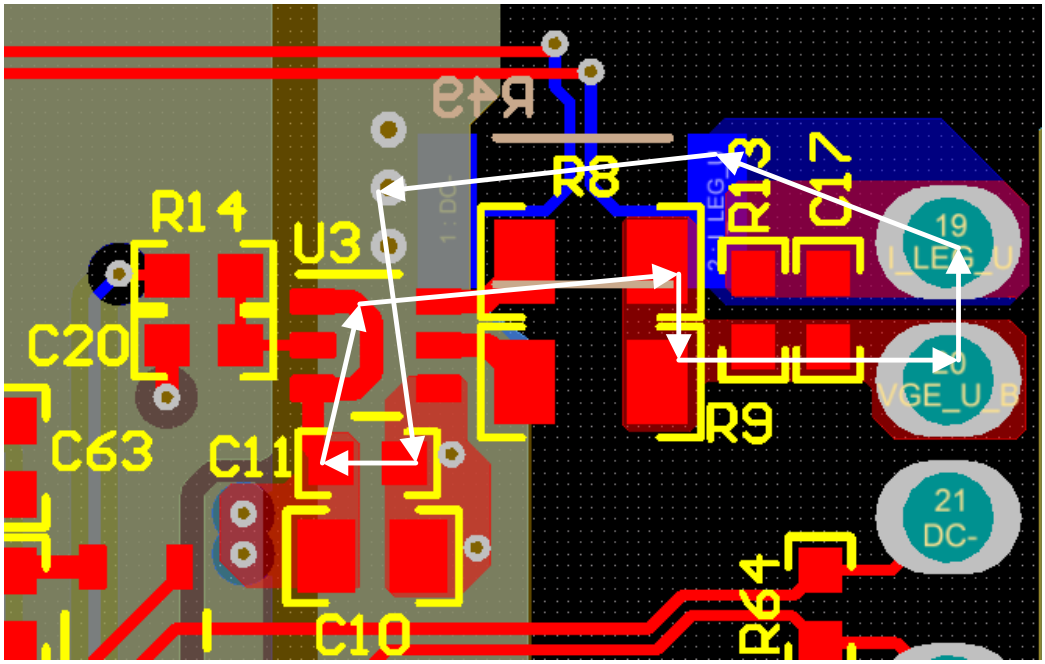


Figure 71. Low-Side Gate Driver Turnon Loop

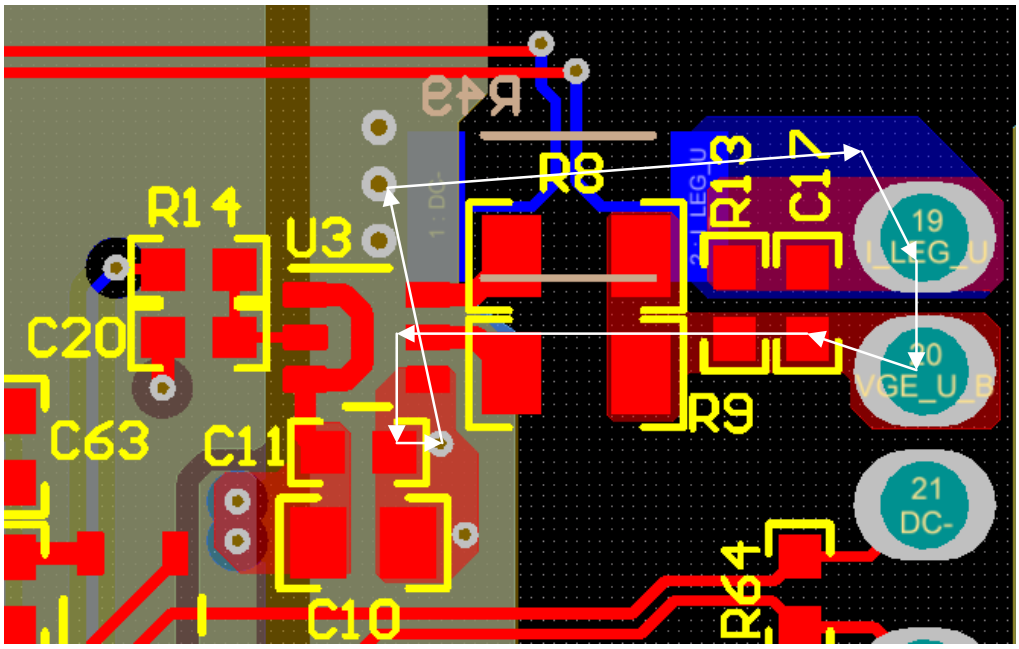


Figure 72. Low-Side Gate Driver Turnoff Loop

4.3.3 High-Side Gate Driver

- Place the primary-side 0.1-µF noise decoupling capacitor C23 close to the primary side power pin.
- Place the RC filter on the PWM input comprising of R19 and C27 close to the IC for good low-pass filtering.
- C44 and C43 form the local 15-V bulk capacitors for the bootstrap circuit.
- D2 is the bootstrap diode and R16 is the inrush current limiting resistor.
- 1-µF bulk capacitor C25 and 0.1-µF high-frequency noise decoupling capacitor C24 are used on the secondary-side power supplies and must be placed close to the IC power pin to minimize switching current loops.
- Keep the IGBT gate source and sink current loop areas to a minimum and the tracks wide to reduce parasitic inductances.

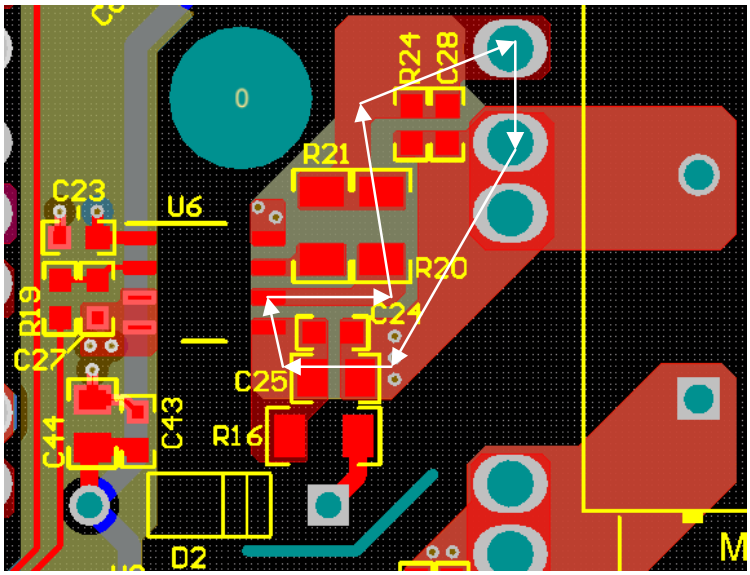


Figure 73. High-Side Gate Turnon Loop

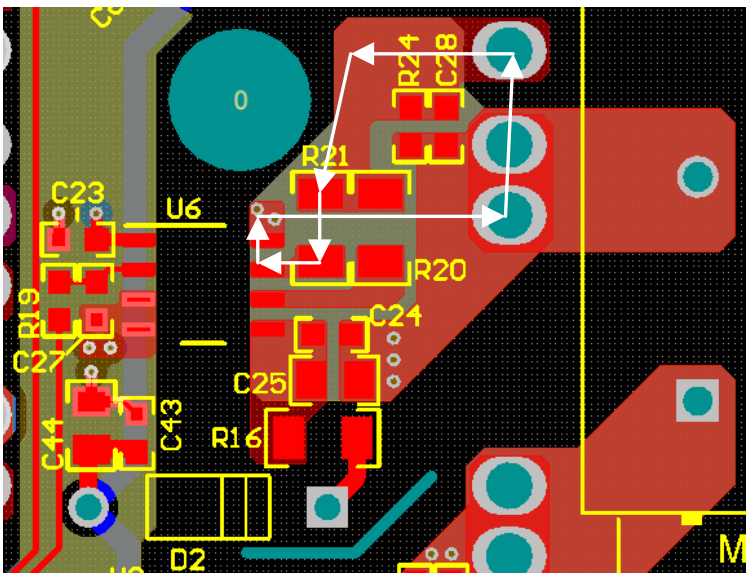


Figure 74. High-Side Gate Turnoff Loop

4.3.4 Creepage and Clearance Between High-Voltage Nets

For overvoltage category 3 equipment operating in a pollution degree 2 environment, a minimum clearance of 3 mm and creepage spacing of 4 mm is required for basic isolation according to IEC 61800-5-1 (Adjustable speed electrical power drive systems: Safety requirements – Electrical, thermal and energy). For reinforced isolation, a clearance of 5.5 mm and creepage of double the basic isolation (meaning 8 mm is required). In this reference design, the reinforced isolation is moved towards the communication channels, thus reducing the creepage and clearance required in the power stage as shown in Figure 75. This leads to a compact lower cost power stage. Wherever a creepage of 4 mm is not possible, a slot is placed inside the board to increase the creepage distance.

The power stage size in this design including the current sensing is ≈ 65 mm × 65 mm.

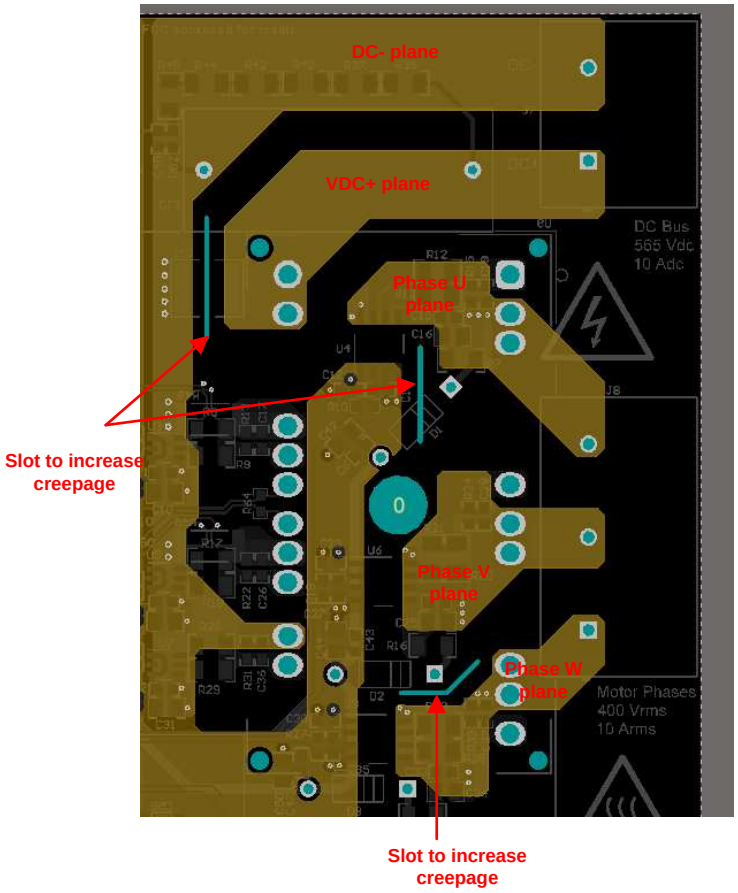


Figure 75. Creepage and Clearance Spacing Within Power Stage

4.3.5 Layout Prints

To download the layer plots, see the design files at TIDA-01456.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01456.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01456.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01456.

5 Related Documentation

1. Texas Instruments, *Sensorless Field Oriented Control of 3-Phase Permanent Magnet Synchronous Motors Using TMS320F2833x*, Application Report (SPRABQ4)
2. Texas Instruments, *Reinforced Isolated Phase Current Sense Reference Design with Small Delta Sigma Modulators*, TIDA-00914 Design Guide (TIDUD07)
3. Texas Instruments, *Reference Design for Reinforced Isolation 3-Phase Inverter with Current, Voltage and Temp Protection*, TIDA-00366 Design Guide (TIDUBX1)
4. Texas Instruments, *Isolated IGBT Gate Driver Evaluation Platform for 3-Phase Inverter System Reference Design* , TIDA-00195 Design Guide (TIDUA15)
5. Semikron, Technical Explanation SEMITOP®

5.1 Trademarks

6 Terminology

IGBT— Insulated gate bipolar transistor

ACIM— AC induction motor

PWM— Pulse width modulation

UVLO— Undervoltage lockout

DNP— Do not populate

NTC— Negative temperature coefficient

7 About the Author

PAWAN NAYAK is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the Motor Drive segment within Industrial Systems.

7.1 Recognition

The author would like to recognize the excellent contributions from **MARTIN STAEBLER** and **NELSON ALEXANDER** during the design, test, and documentation of the design.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265