TI Designs

18-V, 400-W, 98% Efficient Compact Brushless DC Motor Drive With Stall Current Limit Reference Design

Description

The TIDA-00772 is an 18-A_{RMS} drive for a three-phase brushless DC (BLDC) motor in power tools. The device operates off of a 5-cell Li-Ion battery with a voltage of up to 21 V. The design is a 45-mm × 50-mm compact drive that implements sensor-based trapezoidal control. The design uses a discrete, compact MOSFET-based three-phase inverter that delivers an 18 A_{RMS} continuous (60-A peak for 1 s) winding current without external cooling or heat sink. The slew-rate control and triple charge pump of the gate drive ensures maximum inverter efficiency and optimum EMI performance. The cycle-by-cycle overcurrent protection feature protects the power stage from large currents, and the board can work up to 55°C ambient temperature. For a 10.8-V, 250-W (3-cell Li-Ion) drive, refer to TIDA-00771.

Resources

TIDA-00772	Design Folder
CSD18502Q5B	Product Folder
DRV8305	Product Folder
MSP430G2553	Product Folder
SN74LVC126A	Product Folder
LMT87	Product Folder
TPD1E10B06	Product Folder
DRV5013	Product Folder

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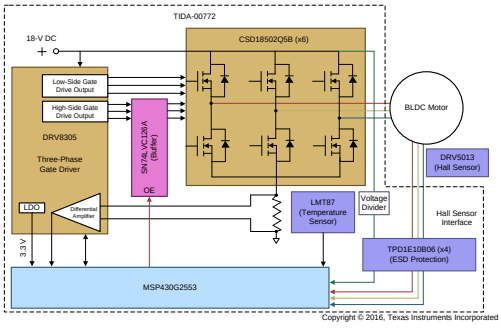
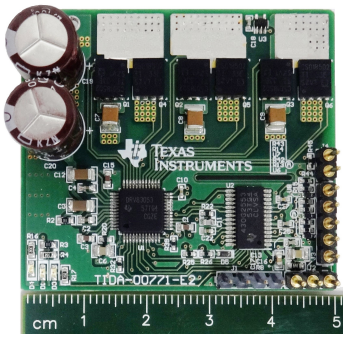
Features

- 400-W Drive for BLDC Motor Supporting Sensor-Based Trapezoidal Control
- Designed to Operate From 5-Cell Li-Ion Battery Voltage Ranging From 5 V to 21 V
- Delivers up to 18-A_{RMS} Continuous Motor Current Without Heat Sink or Airflow
- 60-A Peak Current Capability for 1 Second
- Small PCB Form Factor of 45 mm × 50 mm Using 40-V, 400-A_{PEAK},1.8-mΩ R_{DS_ON}, SON5×6 Package MOSFETs
- Optimum Inverter Efficiency and EMI Performance Using Slew Rate Control of Gate Driver
- Three-Phase Gate Driver With Internal Charge Pump Ensures Maximum Inverter Efficiency Even at 5-V DC
- Cycle-by-Cycle Overcurrent and Motor Stall Current Non-Latching Limit
- Short-Circuit Latch Protection by V_{DS} Sensing
- Shoot-Through, Undervoltage, Over-Temperature, and Blocked Rotor Protection
- Operating Ambient Temperature: –20°C to +55°C

Applications

- Power Tools
- Garden Tools
- Mower Robots
- Vacuum Cleaner Robots





1 System Overview

1.1 System Description

Power tools are used in various industrial and household applications such as drilling, grinding, cutting, polishing, driving fasteners, various garden tools, and more. The most common types of power tools use electric motors while some use internal combustion engines, steam engines, or compressed air. Power tools can be either corded or cordless (battery powered). Corded power tools use the mains power (the grid power) to power up the AC or DC motors. The cordless tools use battery power to drive DC motors.

Most of the cordless tools use lithium-ion batteries, the most advanced in the industry. Lithium-ion batteries have high energy density, low weight, and greater life. These batteries have relatively low self-discharge (less than half that of nickel-based batteries) and can provide a very high current for applications like power tools.

Cordless tools use brushed or BLDC motors. The brushless motors are more efficient and have less maintenance, low noise, and a longer life. Power tools have requirements on form factor and thermal performance, therefore, high-efficient power stages with a compact size are required to drive the power tool motor. The small form factor of the power stage enables flexible mounting, better PCB layout performance, and a low-cost design. High efficiency provides maximum battery duration and reduces cooling efforts. The high-efficiency requirement must have switching devices with a low drain-to-source resistance (R_{DS_ON}). The power stage should also take care of protections like motor stall or any other chances of high current.

This design uses the CSD18502Q5B NexFETs, featuring a low R_{DS_ON} of 1.8 mΩ in a SON5×6 SMD package that results in a small form factor of 45 mm × 50 mm. The three-phase gate-driver DRV8305 is used to drive the three-phase MOSFET bridge, which can operate from 4.5 V to 45 V and support a programmable gate current with a maximum setting of 1.25-A sink and 1-A source. The DRV8305 includes three current shunt amplifiers for accurate current measurements that support bi-directional current sensing with an adjustable gain. The DRV8305 has an integrated voltage regulator and controller to support a microcontroller (MCU) or additional system power needs. The SPI provides detailed fault reporting and flexible parameter settings such as gain options for the current shunt amplifier, slew rate control of the gate drivers, and various protection features.

The MSP430G2553 MCU implements the control algorithm in this design. The cycle-by-cycle (CBC) overcurrent protection uses the internal comparator of the MSP430G2553 and external buffer.

The test report shows the RMS current capability, peak current capability, and thermal performance of the board and overcurrent protection features such as cycle-by-cycle control and latch control of the DRV8305. The test results also show the improved RMS current capability of the board with a different air flow.

1.2 System Design Theory

Compared to their brushed-motor counterpart, permanent magnet brushless motors are gaining importance because of their high efficiency, high torque-to-weight ratio, low maintenance, high reliability, low rotor inertia, and more. A brushless permanent-magnet synchronous motor (PMSM) has a wound stator and a permanent magnet rotor assembly. These motors generally use internal or external devices to sense the rotor position. The sensing devices provide position information for electronically switching the stator windings in the proper sequence to maintain rotation of the magnet assembly. The electronic drive is required to control the stator currents in a brushless permanent magnet motor. The electronic drive has the following parts:

- Power stage with a three-phase inverter that has the required power capability
- MCU to implement the motor-control algorithm
- Position sensor for accurate motor-current commutation
- Gate driver for driving the three-phase inverter
- Power supply to power the MCU

1.2.1 Brushless Permanent Magnet Motors

Permanent magnet motors can be classified according to Back-EMF (BEMF) profiles: a BLDC motor and a PMSM. Both BLDC motors and PMSMs have permanent magnets on the rotor but have different flux distributions and BEMF profiles. In a BLDC motor the BEMF that is induced in the stator is trapezoidal, and in a PMSM the BEMF that is induced in the stator is sinusoidal. Implementing an appropriate control strategy is required to obtain the maximum performance from each type of motor.

The BLDC motor or the trapezoidal BEMF motor has the ampere conductor distribution of the stator, which should remain constant and fixed in space for a fixed interval (commutation interval). For a three-phase winding, the commutation interval is 60° electrical. At the end of each commutation interval, the ampere conductors are commutated to the next position. These motors use a two-phase ON control, where two phases of the motor energize at a time and the third winding will open. The principle of the BLDC motor is, at all times, to energize the phase pair that can produce the highest torque. The combination of a direct current with a trapezoidal BEMF makes it theoretically possible to produce a constant torque. In practice, the current cannot be established instantaneously in a motor phase; because of this, the torque ripple is present at each 60° phase commutation. Figure 1 shows the electrical waveforms in the BLDC motor in the two phases ON operation.

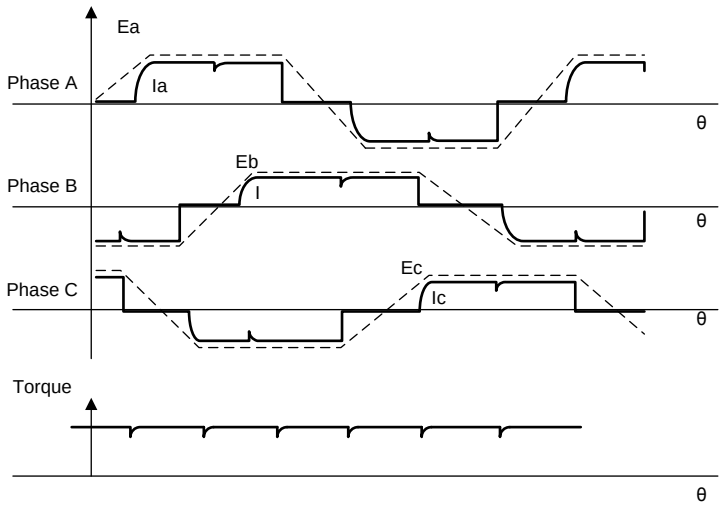


Figure 1. Electrical Waveforms in Two-Phase ON Control of BLDC Motor and Torque Ripple

A trapezoidal control has the following advantages:

- Only one current at a time needs to be controlled.
- Only one current sensor is required (or none for speed loop only).
- The positioning of the current sensor allows the use of low-cost sensors as a shunt.

For more details about trapezoidal control, see the application report ([1]).

1.2.2 Power Stage Design – Battery-Power Input to Board

The battery-power input schematic is shown in Figure 2. The input bulk-aluminum electrolytic capacitors (C19 and C20) provide the ripple current and the voltage rating is derated by 50% for better life. These capacitors are rated to carry high ripple current. Capacitors C21 and C24 are used as bypass capacitors to GND. D2 is the transient voltage suppression (TVS) that has a breakdown voltage of 30 V and a maximum supply voltage of 30 V.

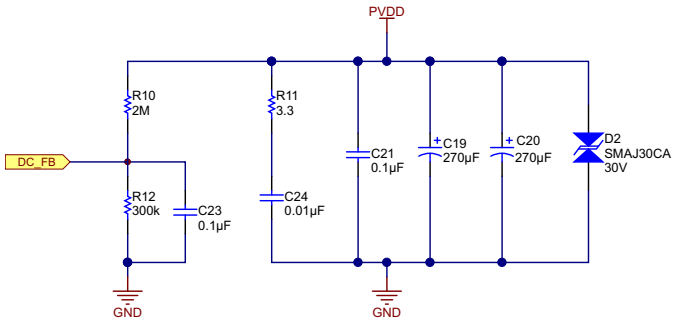


Figure 2. Schematic of Battery-Power Input Section

The input supply voltage (PVDD) is scaled using the resistive divider network that consists of R10, R12, C23, and is fed to the MCU. Considering the maximum voltage for the MCU ADC input is 3.3 V. The maximum measurable amount of DC input voltage is calculated by using Equation 1.

$$V_{DC}^{Max} = V_{ADC\_DC}^{Max} \times \frac{(300\ k\Omega + 2000\ k\Omega)}{300\ k\Omega} = 3.3 \times \frac{(300\ k\Omega + 2000\ k\Omega)}{300\ k\Omega} = 25.3\ V \quad (1)$$

Considering a 20% headroom for this value according to Equation 1, the maximum recommended voltage input to the system is 25.3 × 0.8 = 20.25. For a power stage with a maximum operating voltage of 21 V, this voltage feedback-resistor divider is ideal. Also, this choice of feedback-resistor values gives optimal ADC resolution for a system operating from 5 V to 21 V.

1.2.3 Power Stage Design – Three-Phase Inverter

The three-phase inverter circuit is shown in Figure 3. The current-sensor resistors (R5 and R18) mounted on the DC bus return path measure the DC bus current. The voltage across the sense resistor is fed to the MCU through the current-shunt amplifiers. Capacitors C7, C8, and C9 are the decoupling capacitors that are connected across each inverter leg.

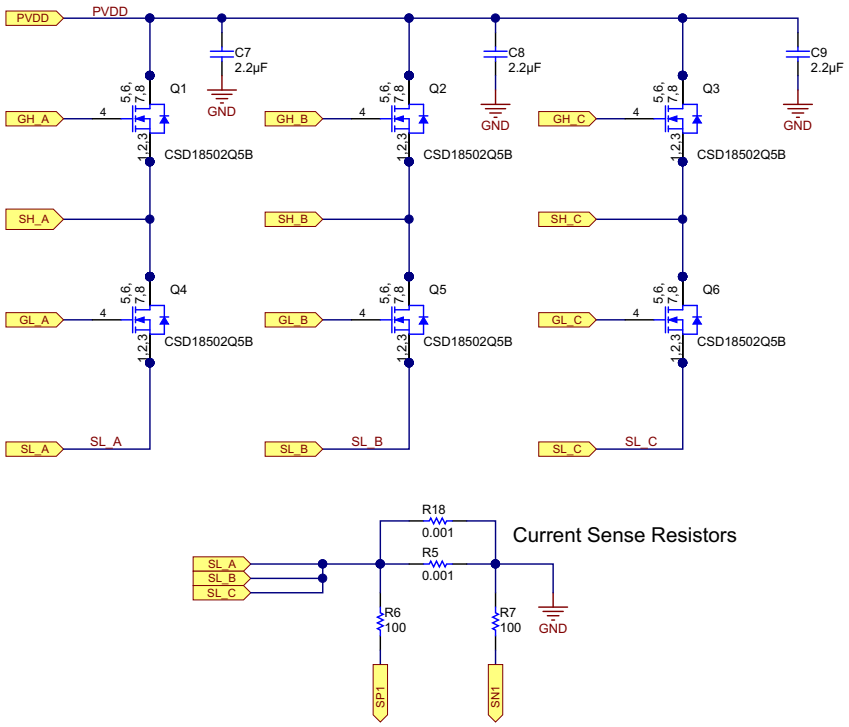


Figure 3. Schematic of Three-Phase MOSFET Inverter and Current Sense Resistors

NOTE: Connect the decoupling capacitors close to the corresponding MOSFET legs for better decoupling (see Section 4.3). An improper layout or position of the decoupling capacitors can cause undesired V_{DS} switching voltage spikes.

1.2.3.1 MOSFET

The board is designed to operate from a 5-cell Li-Ion battery voltage up to 21 V (the maximum input DC voltage in the application is 21 V). Considering the safety factor and switching spikes a MOSFET with a voltage rating that is greater than or equal to 40 V is suitable for this application.

The current rating of the MOSFET depends on the peak winding current. The power stage must provide an 18-A_{RMS} nominal continuous current to the motor winding and a 60-A peak current for 1 second. Considering the peak current capability with enough margin, a MOSFET with a 100-A continuous rating may be selected. The package size of the MOSFET must be small to design a small form-factor PCB.

For better thermal performance, select the MOSFETs with low R_{DS_ON}. In the reference design, TI uses the MOSFET CSD18502Q5B; this device is a N-channel NexFET with a low R_{DS_ON} of 1.8 mΩ and requires a low total gate charge. The device also has a continuous drain current capacity (package limited) of 100 A and a peak current capacity of 400 A. The MOSFET is available at a small package size of 5 mm × 6 mm.

1.2.3.2 Sense Resistor

Power dissipation in sense resistors and the input-offset error voltage of the op amps are important in selecting the sense-resistance values. The sense resistors carry a total nominal RMS current of 18 A with a peak current of 60 A for 1 second. A high sense resistance value increases the power loss in the resistors. If the current-sense amplifier is used without offset calibration, select the sense resistor so the sense voltage across the resistor is sufficiently higher than the offset error voltage to reduce the effect of the offset error.

Select a 0.5-mΩ resistor as the sense resistor and use Equation 2 to calculate the power loss in the resistor at 18 A_{RMS}.

$$\text{Power loss in the resistor} = I_{RMS}^2 \times R_{SENSE} = 18^2 \times 0.0005 = 0.162 \text{ W} \quad (2)$$

Use a 60-A peak current and Equation 2 to calculate the power loss in the resistor (= 1.8 W for one second). In this design, two 1-mΩ, 3-W resistors are used in parallel.

1.2.4 Power Stage Design – DRV8305 Gate Driver

Capacitors C1 and C3 are the AVDD and DVDD decoupling capacitors that must be placed close to the IC. PVDD is the DC supply input; in this case, it is the battery voltage of 10.8 V. A 4.7-µF capacitor (C5) is the PVDD capacitor in this design.

Capacitors C12 and C15 are charge pump capacitors for the high-side and low-side gate drivers. The EN_GATE pin of DRV8305 is connected to the MCU and is pulled down by R32. The MCU can enable or disable the gate drive outputs of the DRV8305.

Capacitors C2 and C4 are the flying capacitors for charge pumps. See [4] for the voltage rating selection of C2 and C4.

The WAKE pin of the DRV8305 is tied to 3.3 V. To control the WAKE pin through the MCU, connect the pin to any digital I/O of the MCU.

Figure 4 shows the schematic of the DRV8305 gate driver.

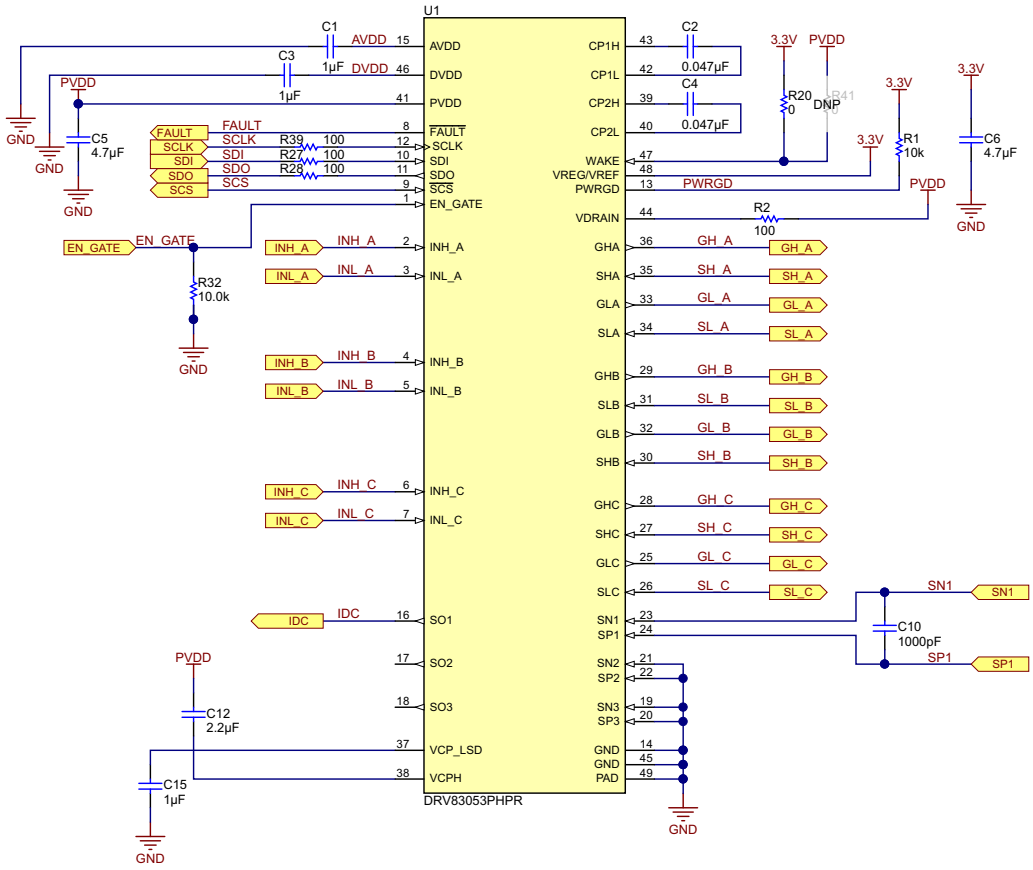


Figure 4. Schematic of DRV8305 Gate Driver

1.2.4.1 Gate Drive Features of DRV8305

The DRV8305 gate driver uses a complimentary push-pull topology for the high-side and the low-side gate drivers. The high side (GHx to SHx) and the low side (GLx to SLx) are floating gate drivers that tolerate switching transients from the half-bridges.

IDRIVE – Gate Driver Output Current

The gate drive architecture implements adjustable current control for the gates of the external power MOSFETs. Adjustable current control allows the gate driver to control the V_{DS} slew rate of the MOSFETs by adjusting the gate drive current. The DRV8305 provides 12 adjustable source and sink current levels for the high-side (the high sides of all three phases share the same setting) and low-side gate drivers (the low sides of all three phases share the same settings). The gate drive levels are adjustable through the SPI registers in the standby and operating states. This flexibility enables the system designer to use software to tune the performance of the driver for different operating conditions.

The current source architecture helps to eliminate the temperature, process, and load-dependent variations associated with internal and external series limiting resistors. Also, internal switches are adjusted to create the desired settings up to the 1.25-A (sink) or 1-A (source) settings.

Control of the gate current during the MOSFET Miller region is a key component for adjusting the MOSFET V_{DS} rise and fall times. MOSFET V_{DS} slew rates are a critical parameter for optimizing emitted radiations, energy and duration of diode recovery spikes, slew rate (dV/dt) related turnon leading to shoot-through, and voltage transients related to parasitics.

TDRIVE – Gate Driver State Machine

The DRV8305 gate driver uses an integrated state machine (TDRIVE) in the gate driver to protect against excessive current on the gate drive outputs, shoot-through in the external MOSFET, and dV/dt turn on as a result of switching on the phase nodes. The TDRIVE state machine allows for the design of a robust and efficient motor drive system with minimal overhead.

The state machine incorporates internal handshaking when switching from the low-side to the high-side external MOSFET or vice-versa. The handshaking prevents the external MOSFETs from entering a period of cross conduction, also known as shoot-through. The internal handshaking uses the V_{GS} monitors of the DRV8305 to determine when one MOSFET has been disabled and the other can be enabled. Internal handshaking allows the gate driver to insert an optimized dead time into the system without the risk of cross conduction. Any dead time that is externally added through the MCU or SPI register will be inserted after the handshake process.

The state machine also incorporates a gate drive timer to ensure that under abnormal circumstances, such as a short on the MOSFET gate or the unintentional turnon of a MOSFET V_{GS} clamp, the high peak current through the DRV8305 and MOSFET is limited to a fixed duration. Select a t_{DRIVE} time that is longer than the time needed to charge or discharge the gate capacitances of the external MOSFETs. The TDRIVE SPI registers must be configured so the MOSFET gates are charged completely within t_{DRIVE} during normal operation. If t_{DRIVE} is too low for a given MOSFET, then the MOSFET may not turn on completely. Tune these values in-system with the required external MOSFETs to determine the best possible setting for the application. A good starting value is a t_{DRIVE} period that is 2x the expected rise or fall times of the external MOSFET gates. Note that TDRIVE does not increase the PWM time and terminates if a PWM command is received while it is active.

VCPH Charge Pump – High-Side Gate Supply

The DRV8305 uses a charge pump to generate the proper gate to source voltage bias for the high-side N channel MOSFETs. Similar to the commonly used bootstrap architecture, the charge pump generates a floating supply voltage that enables the MOSFET.

To support low-voltage operation, a regulated triple charge pump scheme is used to create a sufficient V_{GS} to drive standard and logic level MOSFETs during the low-voltage transient. The charge pump regulates the voltage in a tripler mode from 4.4 V to 18 V. Beyond 18 V and up to the maximum operating voltage, the charge pump switches over to a doubler mode to improve efficiency. The charge pump is continuously monitored for undervoltage and overvoltage conditions to prevent underdriven or overdriven MOSFET scenarios.

VCP_LSD LDO – Low-Side Gate Supply

The DRV8305 uses a linear regulator to generate the proper gate-to-source voltage for the low side N-channel MOSFETs. The Linear regulator generates a fixed 10-V supply voltage with respect to GND. To support low-voltage operation, the input voltage for the VCP_LSD linear regulator is taken from the VCPH charge pump; this allows the DRV8305 to provide a sufficient V_{GS} to drive standard and logic level MOSFETs during the low-voltage transient. The VCP_LSD regulator is continuously monitored fo under-voltage conditions.

1.2.4.2 Current Shunt Amplifier in DRV8305

The DRV8305 includes three high-performance, low-side current-shunt amplifiers for accurate current measurement using low-side shunt resistors in the external half-bridges. The current-shunt amplifiers are commonly used to measure the motor phase current to implement overcurrent protection, external torque control, or external commutation control through the application MCU.

The current shunt amplifiers have the following features:

- Can be programmed and calibrated independently
- Can provide output bias up to 2.5 V to support bidirectional current sensing
- May be used for either individual or total current shunt sensing
- Four programmable gain settings through SPI registers (10, 20, 40, and 80 V/V)
- Programmable output bias scaling. The scaling factor k can be programmed through SPI registers (1/2 or 1/4)
- Programmable blanking time of the amplifier outputs
- Minimizes DC offset and drift through temperature with DC calibrating through SPI register.
- Calculate the output of the current-shunt amplifier by using Equation 3

$$V_O = \frac{V_{REF}}{k} - G \times (SN_X - SP_X) \quad (3)$$

where

- V_{REF} is the reference voltage from the VREG pin
- G is the gain setting of the amplifier
- k = 2 or 4
- SN_X and SP_X are the inputs of channel x

Figure 5 shows the current amplifier simplified block diagram.

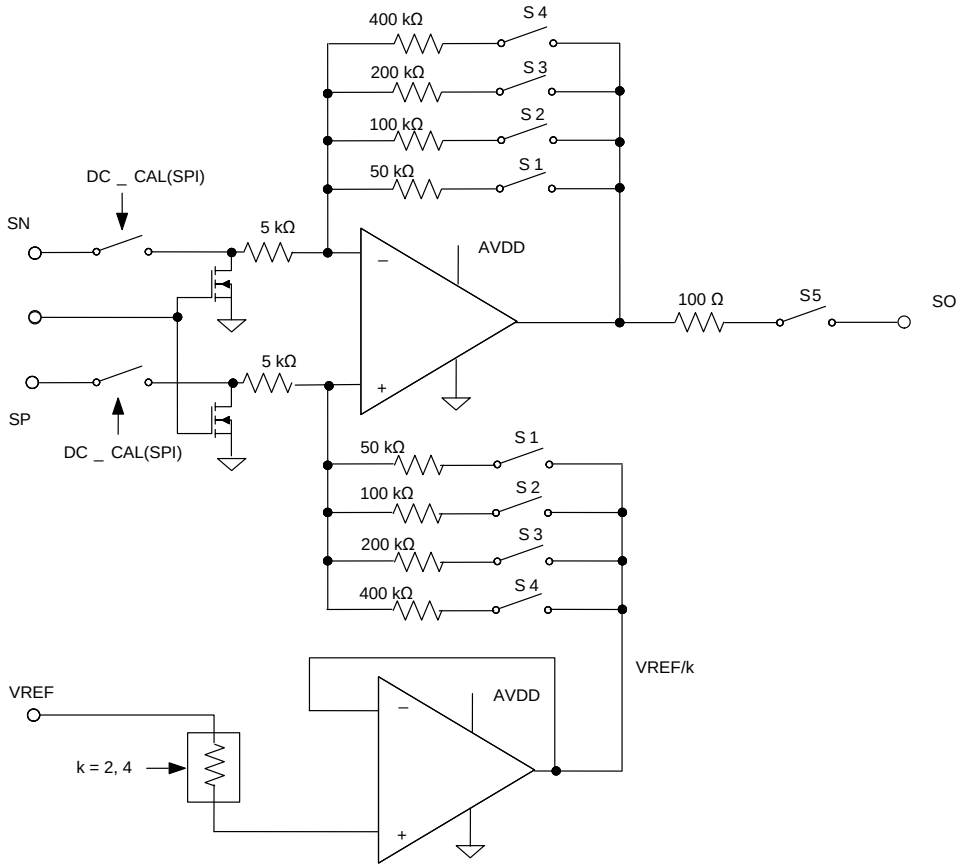


Figure 5. DRV8305 Current Shunt Amplifier Simplified Block Diagram

1.2.4.3 Protection Features in DRV8305

MOSFET Shoot-Through Protection (TDRIVE)

The DRV8305 integrates analog handshaking and digital dead time to prevent shoot-through in the external MOSFETs.

- An internal handshake through analog comparators is performed between each high-side and low-side MOSFET switching transition to avoid cross conduction.
- A minimum dead time (digital) of 40 ns is always inserted after each successful handshake. This digital dead time is programmable through the DEAD_TIME SPI register setting in addition to the time taken for the analog handshake.

MOSFET Overcurrent Protection (VDS_OCP)

To protect the system and external MOSFET from damage because of high current events, V_{DS} overcurrent monitors are implemented in the DRV8305. The V_{DS} sensing is implemented for both the high-side and low-side MOSFETs through the following pins:

- High-side MOSFET: V_{DS} measured between VDRAIN and SHx pins
- Low-side MOSFET: V_{DS} measured between SHx and SLx pins

Based on the R_{DS_ON} of the power MOSFETs and the maximum allowed I_{DS} a voltage threshold can be calculated and, when exceeded, triggers the V_{DS} overcurrent protection feature. The voltage threshold level is programmable through the SPI VDS_LEVEL setting.

The V_{DS} overcurrent monitors implement adjustable blanking and deglitching times to prevent false trips because of switching voltage transients. The different V_{DS} sensing protection modes are:

- V_{DS} Latched Shutdown Mode: When a V_{DS} overcurrent event occurs, the device pulls all gate drive outputs low and reports through nFAULT and SPI registers.
- V_{DS} Report Only Mode: When the overcurrent event is detected, the device does not take action related to the gate drivers and reports through nFAULT and SPI registers.
- V_{DS} Disabled Mode: The device ignores V_{DS} overcurrent-event detections and does not report them.

MOSFET dV/dt Turnon Protection (TDRIVE)

Parasitic dV/dt turnon can occur when a charge couples into the gate of the low-side MOSFET during a switching event. If the charge induces enough voltage to cross the threshold of the low-side MOSFET, shoot-through can occur in the half-bridge. To prevent shoot-through, the TDRIVE state machine turns on a strong pulldown during switching. After the switching event has completed, the gate driver switches back to a lower holdoff pull down to improve efficiency.

MOSFET Gate Drive Protection (GDF)

The DRV8305 uses a multilevel scheme to protect the external MOSFET from V_{GS} voltages that could damage it.

The first stage uses integrated V_{GS} clamps that will turn on when the GHx voltage exceeds the SHx voltage by a value that could be damaging to the external MOSFETs.

The second stage relies on the TDRIVE state machine to detect when abnormal conditions are present on the gate driver outputs. After the TDRIVE timer has expired, the gate driver performs a check of the gate driver outputs against the commanded input. If the two do not match, a gate drive fault is reported. This feature can be used to detect a gate short-to-ground or gate short-to-supply event.

The third stage uses undervoltage monitors for the low-side gate drive regulator (VCP_LSD_UVLO2), the high-side gate drive charge pump (VCPH_UVLO2), and an overvoltage monitor for the high-side charge pump (VCPH_OVLO). These monitors detect if any of the power supplies to the gate drivers have encountered an abnormal condition.

Low-Side Source Monitors (SNS_OCP)

The DRV8305 directly monitors the voltage on the SLx pins with respect to ground. If high-current events, such as phase shorts, cause the SLx pin voltage to exceed 2 V, the DRV8305 shuts down the gate driver, puts the external MOSFETs into a high impedance state, and reports a SNS_OCP fault error on the nFAULT pin and corresponding SPI status bit.

Undervoltage Warning (UVFL), Unvervoltage Lockout (UVLO), and Overvoltage Protection

Undervoltage is monitored for on the PVDD, AVDD, VREF, VCPH, and VCP_LSD power supplies. Overvoltage is monitored for on the PVDD and VCPH power supplies.

Overtemperature Warning (OTW) and Overtemperature Shutdown (OTSD) Protection

A multilevel overtemperature detection is implemented in the DRV8305.

MCU Watchdog

The DRV8305 has an MCU watchdog function to ensure that the external controller that is instructing the device is active and not in an unknown state.

V_{REG} Undervoltage (VREG_UV)

The DRV8305 has an undervoltage monitor on the V_{REG} output regulator to ensure the external controller does not experience a brownout condition. The V_{REG} undervoltage level can be set through the SPI setting.

For more details on the protections and SPI monitoring, see [4].

1.2.5 Power Stage Design – Microcontroller MSP430™

Figure 6 shows the schematic for configuring the MSP430G2553 MCU. Capacitors C16 and C17 are the decoupling capacitors. Resistor R8 is used to limit the dv/dt at the supply pin of the MSP430G2553. TI recommends using a 4.7-µF capacitor (minimum) at the DVCC pin. The TIDA-00772 reference design uses a 10-µF capacitor at the DVCC pin. A 0.1-µF capacitor has been added to obtain the best performance at a high frequency.

Timer A of the MCU is used for PWM generation. The TA1.2 instance of the timer and the corresponding pins are mapped to the high-side switch PWM. The TA1.1 instance of the timer and the corresponding pins are mapped to the low-side switch PWM. The TIDA-00772 reference design uses unipolar, trapezoidal BLDC control where the high-side switches switching at a high frequency. The low side switches at the electrical frequency of the motor current that is much lower, and the same side switches at a high frequency (complimentary to high-side switch) during the freewheeling period to enable active freewheeling and low losses. All of the feedback signal voltages including the DC bus voltage, current sense amplifier output, potentiometer voltage for speed control, and temperature sensor output are interfaced to the 10-bit successive approximation (SAR) ADC channels of the MCU. The current sense amplifier output is also connected to the comparator input. An external reference is used to set the comparator reference using resistors R23 and R24.

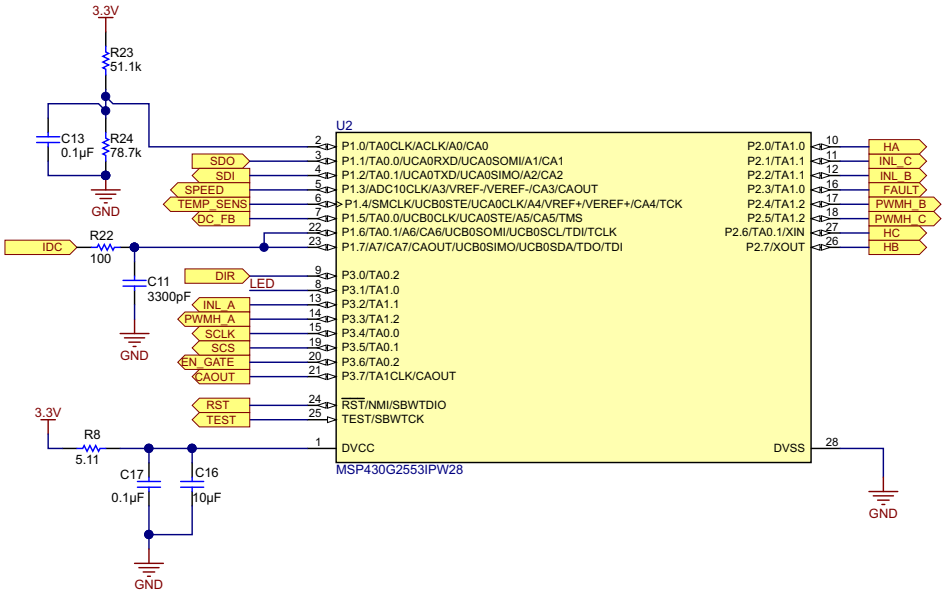


Figure 6. MSP430G2553 Schematic

1.2.6 Power Stage Design – Cycle-by-Cycle Overcurrent Protection

The cycle-by-cycle overcurrent protection is implemented by using the current sense amplifier in the DRV8305, comparator A+ in the MSP430G2553, and the buffer SN74LVC126A. The overcurrent protection circuit is shown in Figure 7.

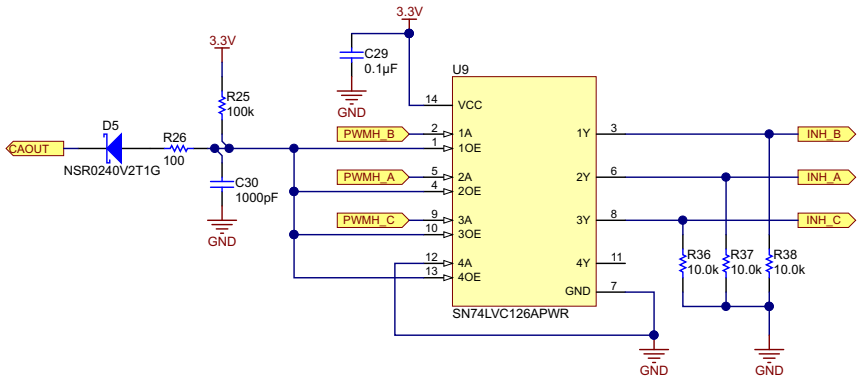


Figure 7. Cycle-by-Cycle Overcurrent Protection Using SN74LVC126A

1.2.6.1 Comparator_A+

The Comparator_A+ module is an analog voltage comparator that has the following features:

- Inverting and non-inverting terminal input multiplexer
- Software selectable RC-filter for the comparator output
- Interrupt capability
- Selectable reference voltage generator
- Comparator and reference generator can be powered down
- Input multiplexer

The comparator compares the analog voltages at the non-inverting (+) and inverting (–) input terminals. If the non-inverting terminal is more positive than the inverting terminal, the comparator output CBOUT is high. The comparator can be switched on or off using the control bit CBON.

The output of the comparator can be used with or without internal filtering. When control bit CBF is set, the output is filtered with an on-chip RC filter. The delay of the filter can be adjusted in four different steps. Selecting the output filter can reduce errors associated with comparator oscillation.

The comparator can be used with internal or external reference voltages. TIDA-00772 uses external reference.

1.2.6.2 PWM Shutoff Using SN74LVC126A

The SN74LVC126A, a quadruple bus buffer gate, features independent line drivers with three state outputs. Each output is disabled when the associated output enable (OE) input is low. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver. Inputs can be driven from either 3.3-V or 5-V devices.

In the TIDA-00772 design, all of the high-side PWM signals are connected through the buffer. Whenever a current limit happens, all of the high-side PWMs shut off by pulling down the OE of the buffer. The OE of the buffer is connected to the comparator output through a diode (D5) and the current limiting resistor (R26). When the DC bus current reaches the set current limit reference, the comparator output goes low and causes capacitor C30 to discharge through resistor R26 and D5. Once the capacitor discharges below the V_{IL} of buffer, all the buffer outputs will tristate. This means all the high-side PWMs are off and the current falls down. As the current goes below the overcurrent reference threshold, the comparator output goes high (3.3 V), and as the OE voltage is lower, diode D5 will be reverse biased. Next, capacitor C30 charges through resistor R25. When capacitor C30 reaches the V_{IH} of the buffer, the buffer output enables and the high-side PWMs go high. The value of C30 and R25 are designed so the next enable occurs after approximately 50 μs once the OE is disabled. The value of C30 has to be low to ensure that C30 discharges immediately through R26, and this affects the response time of the current limit action.

1.2.7 Power Stage Design – Hall Sensor Interface

Figure 8 shows the Hall sensor interface from the motor to the board. The 3.3 V that is generated by the DRV8305 is used as the power supply for the Hall sensor. Usually, the Hall sensors have an open drain or open collector configuration. Resistors R13, R14, and R15 are used as the pullup resistors. Resistors R42, R43, and R44 along with capacitors C14, C26, and C27 form noise filters at the Hall sensor input.

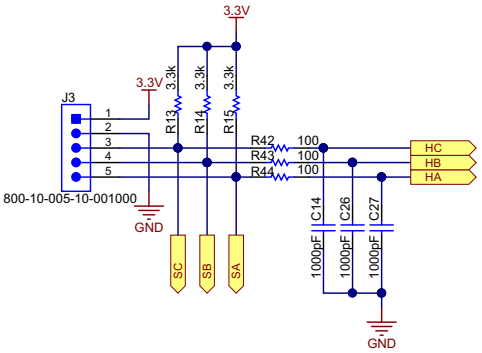


Figure 8. Hall Sensor Connector Schematic

NOTE: The Hall sensor connection must match with the winding connection for proper operation of the BLDC motor.

1.2.8 Power Stage Design – External Interface Options and Indications

1.2.8.1 ESD Protection

The DC-bus voltage lines and the hall sensor signal interfaces are externally protected using ESD devices (see Figure 9). The TPD1E10B06 diode is used for ESD protection. The TPD1E10B06 is a single-channel, ESD, transient-voltage-suppression (TVS) diode that offers ±30-kV contact ESD, ±30-kV IEC air-gap protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bidirectional signal support.

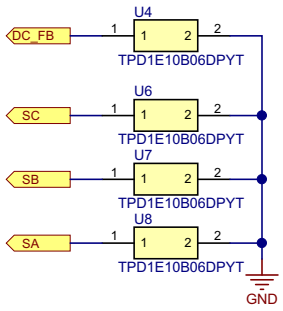


Figure 9. ESD Protection Schematic

1.2.8.2 Speed Control of Motor

The speed control is configured by using a potentiometer (POT), and the POT voltage is fed to the ADC of the MSP430G2553. The circuit is shown in Figure 10. The POT is supplied from the 3.3 V that is generated by the DRV8305. A 20-k POT can be connected externally to jumper J2. Connect the fixed terminals of the POT to terminal 1 and 3 of J2 and connect the mid-point to terminal 2 of J2.

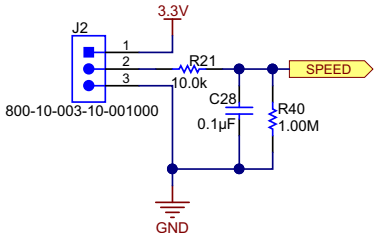


Figure 10. Potentiometer Connection for Speed Control Schematic

Resistor R40 is used to ensure that the speed control reference is zero if the POT terminal is open.

1.2.8.3 Direction of Rotation – Digital Input

Jumper J4 (see Figure 11) is used to set the direction of rotation of the motor. Close or open the jumper to change the direction of rotation.

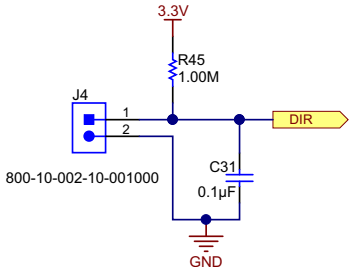


Figure 11. Digital Input to Change Direction of Rotation

1.2.8.4 Temperature Sensing

Figure 12 shows the temperature sensor circuit used to measure the PCB temperature. The LMT87 is an analog output temperature sensor. The temperature sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage, providing a low-impedance output source. The average output sensor gain is 13.6 mV/°C.

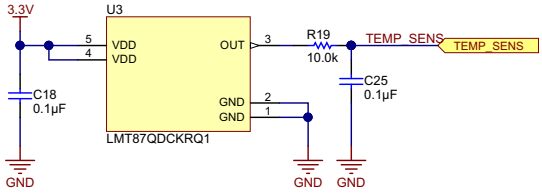


Figure 12. Temperature Sensor Schematic

1.2.8.5 LED Indications

Figure 13 shows the LED indications provided in the board. LED D4 indicates the 3.3 V in the board, D1 is tied to FAULT signal from the DRV8305, and D3 is driven by a digital I/O in the MSP430G2553.

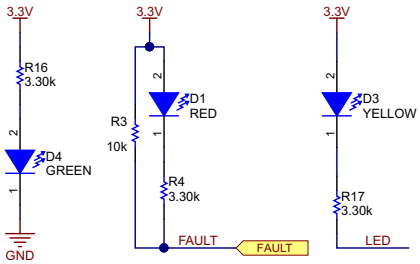


Figure 13. LED Indications Schematic

1.3 Key System Specifications

Table 1 shows the key system specifications.

Table 1. Key System Specifications

PARAMETERS	SPECIFICATIONS
Input voltage	18-V DC (5-V Min to 21-V Max), 5-Cell Li-Ion
Rated input power	400 W
RMS winding current	18 A
Peak winding current	60 A (for 1 second)
Control method	Sensor-based trapezoidal
Inverter switching frequency	20 kHz (adjustable from 5 k – 100 k)
Motor electrical frequency	300 Hz max (for example, a motor with 9000 RPM and 4 poles)
Feedback signals	DC bus voltage, hall sensor, low-side DC bus current
Protections	Cycle-by-cycle overcurrent, input undervoltage, overtemperature, and blocked rotor
Cooling	Natural cooling only, no heat sink
Operating ambient	–20°C to +55°C
Board specification	45 mm x 50 mm, 4-layer, 2-Oz copper
Efficiency	> 98%

1.4 Block Diagram

Figure 14 shows the block diagram.

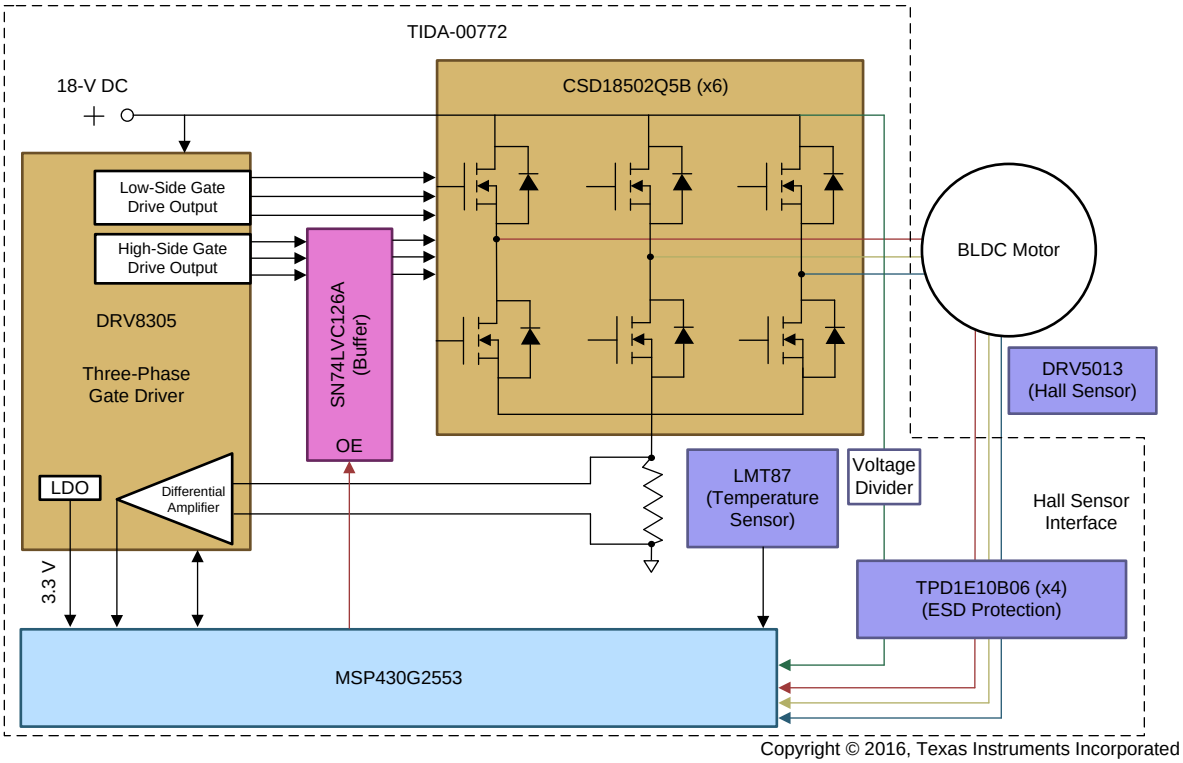


Figure 14. Block Diagram

1.5 Highlighted Products

1.5.1 CSD18502Q5B

The CSD18502Q5B is a 40-V, N-channel NexFET Power MOSFET with a low R_{DS_ON} of 1.8 mΩ. The device has a low total gate-charge requirement. The CSD18502Q5B is available in a small SON 5-mm × 6-mm package with a peak current rating of 400 A.

1.5.2 DRV8305

The DRV8305 is a gate driver IC for three-phase motor drive applications. The device provides three high-accuracy trimmed and temperature compensated half-bridge drivers, and each driver is capable of driving a high-side and low-side N-type MOSFET. The DRV8305 includes three current-shunt amplifiers for accurate current measurements, supports 100% duty cycle, and has multiple levels of protection. The gate driver is programmable through SPI.

1.5.3 MSP430G2553

The TI MSP430™ family of ultra-low-power MCUs consists of several devices that feature different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is achieves an extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active modes in less than 1 µs.

The MSP430G2x13 and MSP430G2x53 series are ultra-low-power mixed-signal MCUs with built-in 16-bit timers, up to 24 I/O capacitive-touch enabled pins, a versatile analog comparator, and a built-in communication capability using the universal serial communication interface. Also, the parts in the MSP430G2x53 family have a 10-bit analog-to-digital (A/D) converter.

1.5.4 SN74LVC126A

The SN74LVC126A is a quadruple-bus buffer gate that is designed for 1.65- to 3.6-V V_{CC} operation. The SN74LVC126A features independent line drivers with 3-state outputs. Each output is disabled when the associated OE input is low. Inputs can be driven from 3.3-V or 5-V devices.

1.5.5 LMT87

The LMT87 device is a precision CMOS integrated-circuit temperature sensor with an analog output voltage (V_{OUT}) that is linearly and inversely proportional to temperature. The device can operate down to a 2.7-V supply with a 5.4-µA power consumption. Package options, including a through-hole TO-92 package, allows the LMT87 to be mounted onboard, off-board, to a heat sink, or on multiple unique locations. The LMT87 has accuracy specified in the operating range of −50°C to +150°C.

1.5.6 TPD1E10B06D

The TPD1E10B06 device is a single-channel electrostatic discharge (ESD) TVS diode in a small 0402 package. This TVS protection product offers ±30-kV contact ESD, ±30-kV IEC air-gap protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bi-directional signal support.

2 Getting Started Hardware and Firmware

2.1 Hardware

2.1.1 Connector Configuration of TIDA-00772

Figure 15 shows the TIDA-00772 connector configuration, and the following list details the configuration.

- Two-terminal input for power supply: This pin is used to connect the input DC supply from the battery. The positive and negative terminals can be identified (see Figure 15).
- Three-terminal output for motor winding connection: The phase output connections for connecting to the three-phase BLDC motor winding are PHASE U, PHASE V, and PHASE W (see Figure 15).
- Four-pin connector J1: This is the programming connector for the MSP430G2553 MCU. The two-wire Spy-Bi-Wire protocol is used to program the MSP430G2553 MCU.
- Three-pin connector J2: This connector can be used to interface an external potentiometer for speed reference. The two fixed terminals of the potentiometer must be connected to the 3V3 and GND pins. The mid-point of the potentiometer must be connected to the POT pin of the connector.
- Five-pin connector J3: This is the interface for connecting the Hall position sensors from the motor.
- Two-pin connector J4: This connector is used for the motor direction change. Externally shorting or opening this connector changes the direction of rotation of the motor.

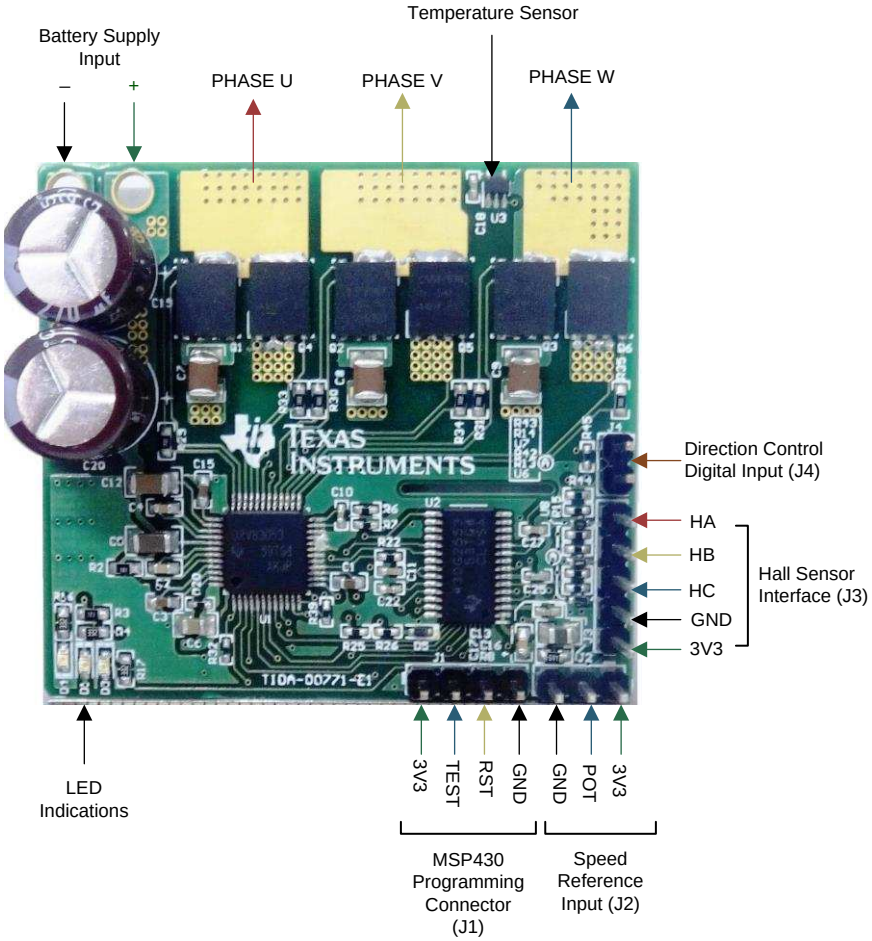


Figure 15. TIDA-00772 PCB Connectors

2.1.2 Programming of MSP430™

Use the two-wire Spy-Bi-Wire protocol to program the MSP430G2553 MCU. Figure 16 shows the four-pin programming connector provided in the TIDA-00772 board.

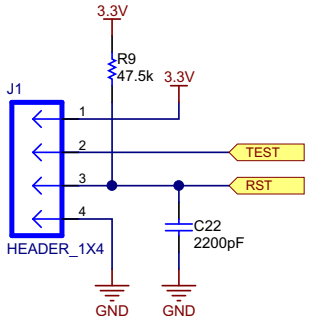


Figure 16. MSP430G2553 Programming Connector

See [4] for the programming options with an external JTAG interface.

Use the following steps to program the MSP430G2553 MCU when the programming supply voltage is provided by the board:

1. Remove the motor connections from the board and power on the input DC supply. Ensure that a minimum of 5-V DC input is applied and 3.3 V is generated in the board.
2. Connect the programmer to the board.
3. Open the CCS software and then build and debug the code to program the MSP430G2553.

2.1.3 Board Bring-up and Testing Procedure

Use the following steps to bring up and test the board:

1. Remove the motor connections from the board and power on the input DC supply. Ensure that a minimum of a 5-V DC input is applied and the 3.3 V is generated in the board.
2. Program the MCU as detailed in Section 2.1.2
3. Remove the programmer, and switch off the DC input supply.
4. Connect the inverter output to the motor winding terminals. Connect the position Hall sensor inputs to J3 and ensure that the winding connection and Hall sensor connections match.
5. Connect the POT at the interface J2 and set the speed reference.
6. Use a DC power supply with current limit protection and apply 5-V DC to the board. If the Hall sensors and winding are connected properly in the matching sequence the motor will begin rotating at a speed set by the POT.

   If the motor is not rotating and takes high current or rotates and draw distorted peak winding current waveform (proper waveform shape is as shown in Figure 36), then check the winding and Hall sensor connection matching and, if wrong, correct it.
7. Adjust the POT voltage for change in speed.
8. Switch off the DC input, close jumper J4, and switch on the DC input to change direction.

2.2 Firmware

2.2.1 System Features

The TIDA-00772 firmware offers the following features and user controllable parameters:

- Trapezoidal control of BLDC motors using digital position Hall sensor feedback
- Overcurrent protection using the internal comparator of the MSP430G2553 MCU
- Latch protection using the V_{DS} sensing feature of the DRV8305

Table 2 shows the TIDA-00772 firmware system components.

Table 2. System Components

SYSTEM COMPONENT		DESCRIPTION
Development and emulation		Code Composer Studio™ v5.5
Target controller		MSP430G2553
PWM frequency		20-kHz PWM (default), programmable for higher and lower frequencies
PWM mode		Asymmetrical
Interrupts		Port 2 interrupt for Hall sensor change
		CPU Timer A – implements 20-kHz ISR execution rate
		ADC interrupt
Peripherals	PWM generation timer configuration	High Side PWM- TIMER A1.2, Clock-16MHz, OUTMOD[2:0]= 2,PWM frequency set for 20 kHz
		Low Side PWM- TIMER A1.1, Clock-16MHz, OUTMOD[2:0]= 6,PWM frequency set for 20 kHz
	Position feedback Hall sensor signals	P2.0 → HA
		P2.7 → HB
		P2.6 → HC
	Comparator configuration for overcurrent protection	CA0/P1.0 → VREF (+ve input of comparator)
		CA7/P1.7 → CSA output (–ve input of comparator)
		CAOUT/P3.7 → comparator output
	ADC channel assignment	A3 → Speed reference from the external potentiometer
		A4 → PCB or FET temperature feedback
		A5 → DC bus voltage sensing
		A6 → Low-side DC bus current sensing
	DRV8305 – SPI programming pins connection	P1.1 → SDO
		P1.2 → SDI
		P3.4 → SCLK
		P3.5 → SCS
	DRV8305 digital I/Os	P3.6 → EN_GATE
		P2.3 → FAULT
	MCU digital I/O	P3.0 → Direction of motor rotation
		P3.1 → LED3

2.2.2 Customizing Reference Code

To modify the firmware, the end user must have CCS and the MSP430G2553 configuration files installed. Section 2.2.2.1, Section 2.2.2.2, and Section 2.2.2.3 detail the different user-adjustable parameters and how to select an optimized value for a specific application.

Open CCS and load the reference project *TIDA-00772_Firmware _V1.0*.

NOTE: If the project is in a .zip or .rar compressed format, the user must extract this file.

2.2.2.1 Customizing Reference Code in MSP430™

Select the main.c file. Paramaters at the beginning of the file can be optimized and are included as the configuration variables. The following code shows these parameters.

```
#define     PWM_PERIOD              400  //PWM Frequency (Hz) = 16MHz/((2*PWM_PERIOD)-1)
#define     MAX_DUTYCYCLE           400  //relative to PWM_PERIOD
#define     MIN_DUTYCYCLE           50   //relative to PWM_PERIOD
#define     ACCEL_RATE              500  // Ramp up time to full scale duty cycle =
                                           (Full scale duty cycle) * ACCEL_RATE * PWM_PERIOD/PWM_Frequency
#define     DEAD_TIME               1    // Dead time from MSP430 = DEAD_TIME* 0.0625 uS (for 16MHz clock)
#define     Block_Rotor_Duration    800  //Blocked_rotor shut off time(s) =
                                           Block_Rotor_Duration*30000/clock frequency
```

PWM_PERIOD

The PWM_PERIOD parameter sets the value in capture and compare register 0 of Timer_A. Timer_A is initialized to operate at 16 MHz (see Equation 4 to calculate the PWM frequency). The TIMER_A PWM is configured in up-down mode.

$$\text{PWM Frequency (Hz)} = \frac{16\ \text{MHz}}{((2 \times \text{PWM\_PERIOD}) - 1)} \tag{4}$$

For example, if the PWM_PERIOD = 400, then PWM frequency = 20 kHz (see Equation 5).

$$\text{PWM Frequency (Hz)} = \frac{16\ \text{MHz}}{((2 \times 400) - 1)} \approx 20\ \text{kHz} \tag{5}$$

MAX_DUTYCYCLE

The MAX_DUTYCYCLE parameter sets the maximum duty cycle that the user can set. The duty cycle input command is compared to MAX_DUTYCYCLE. If the duty cycle input command exceeds MAX_DUTYCYCLE, the target duty cycle is set to MAX_DUTYCYCLE.

MIN_DUTYCYCLE

The MIN_DUTYCYCLE parameter sets the minimum duty cycle that can be applied to the motor. This number is relative to PWM_PERIOD.

ACCEL_RATE

The ACCEL_RATE parameter defines how fast the motor accelerates. For a motor with greater inertia or a motor that requires more time to accelerate, set ACCEL_RATE to a high value (such as 2000). Motors that can quickly ramp up can use a smaller ACCEL_RATE to decrease the startup time.

Calculate the start ramp-up time and the required ACCEL_RATE by using Equation 6 and Equation 7.

$$\text{Ramp-up time to full-scale duty cycle} = \frac{\text{Full-scale duty cycle} \times \text{ACCEL\_RATE} \times \text{PWM\_PERIOD}}{\text{PWM Frequency}} \quad (6)$$

$$\text{ACCEL\_RATE} = \frac{\text{Ramp-up time to full-scale duty cycle} \times \text{PWM Frequency}}{\text{Full-scale duty cycle} \times \text{PWM\_PERIOD}} \quad (7)$$

For example, to ramp up from 0% to 100% duty cycle in 10 s with a PWM frequency of 20 kHz, the ACCEL_RATE would be 500 (see Equation 8).

$$\text{ACCEL\_RATE} = \frac{10\ \text{s} \times 20\ \text{kHz}}{1 \times 400} = 500 \quad (8)$$

Block_Rotor_Duration

The Block_Rotor_Duration parameter defines the time duration in which the motor blocked rotor condition is allowed before the controller turns off all of the PWMs. The time taken to turn off all of the PWMs when the motor is blocked can be calculated by using Equation 9.

$$\text{Blocked rotor PWM turnoff time (s)} = \frac{\text{Block\_Rotor\_Duration} \times 30000}{16\ \text{MHz}} \quad (9)$$

where

- 16 MHz is the TIMER_A clock frequency

For example, if the user wants to turn off the motor if a blocked rotor condition is observed for 1.5 s, then:

Block_Rotor_Duration = 1.5 × (30000 ÷ 16 MHz) = 800

2.2.2.2 Configuring DRV8305 Registers

The register settings of the DRV8305 can be modified by selecting and modifying the drv8305.c file. See the function *drv8305_init()* to initialize the DRV8305 with modified values. See the following code snippet of the function:

```
void drv8305_init(void)
{
    //setup drv8305 via SPI commands
    WriteRegister(0x05, (TDRIVEN_2000NS + IDRIVEN_HS_1000MA + IDRIVEP_HS_1000MA));

    delay_1ms(1);
    WriteRegister(0x06, (TDRIVEP_2000NS + IDRIVEN_LS_1000MA + IDRIVEP_LS_1000MA));

    delay_1ms(1);
    WriteRegister(0x07, (COMM_OPTION_ACTIVE_FW + PWM_MODE_6_INDEPENDENT + DEAD_TIME_40NS +
    TBLANK_0US + TVDS_2US));

    delay_1ms(1);
    WriteRegister(0x09, (FLIP_OTS_ENABLE + DIS_VPVDD_UVLO2_DISABLE + DIS_GDRV_FAULT_ENABLE +
    EN_SNS_CLAMP_ENABLE + WD_DLY_20MS + DIS_SNS_OCP_ENABLE + WD_EN_DISABLE + SLEEP_AWAKE +
    CLR_FLTS_NORMAL + SET_VCPH_UV_4D9V));

    delay_1ms(1);
    WriteRegister(0x0A, (DC_CAL_CH3_NORMAL + DC_CAL_CH2_NORMAL + DC_CAL_CH1_NORMAL + CS_BLANK_0NS
    + GAIN_CS3_10VV + GAIN_CS2_10VV + GAIN_CS1_10VV));

    delay_1ms(1);
    WriteRegister(0x0B, (VREF_SCALING_K4 + SLEEP_DLY_10US + VREG_UV_LEVEL_10P));

    delay_1ms(1);
    WriteRegister(0x0C, (VDS_LEVEL_0D175V + VDS_MODE_REPORT));
}
```

The function *WriteRegister(unit8_t, unit16_t)* is used to write to the DRV8305 registers, and the function *ReadRegister(unit8_t)* is used to read the DRV8305 register content. See [3] for a detailed description of register settings.

2.2.2.3 Initialiazing SPI Communication Between DRV8305 and MSP430™

The register initialization for the DRV8305 is achieved by using SPI communication. The SPI communication pins are connected to the ports of the MSP430. See the drv8305.h file to assign and initialize the ports of MSP430 for SPI communication. The TIDA-00772 reference design uses port connections, shown in Table 3.

Table 3. SPI Communication Interface

DRV8305 PIN	MSP430G2553 PIN
SDO	P1.1
SDI	P1.2
SCLK	P3.4
SCS	P3.5

Modify the SPI GPIO settings according to the hardware mapping. For the TIDA-00772, the mapping is shown in the following code snippet.

```
#define CPU_FREQ_MHZ    (16)

/*****************************************************************************
 * SPI GPIO Settings (Modify according to hardware mapping)
 *****************************************************************************/
#define M1_SCLK_HIGH        (P3OUT |= BIT4)
#define M1_SCLK_LOW         (P3OUT &= ~BIT4)

#define M1_SDI_HIGH         (P1OUT |= BIT2)
#define M1_SDI_LOW          (P1OUT &= ~BIT2)

#define M1_SDO_LEVEL        ((P1IN &= BIT1)?(1):(0))

#define M1_nSCS_HIGH        (P3OUT |= BIT5)
#define M1_nSCS_LOW         (P3OUT &= ~BIT5)
/*****************************************************************************/
```

2.2.3 Running Project in Code Composer Studio™

Use the following steps to run the project in CCS.

1. Install Code Composer Studio.
2. Import the project titled *TIDA-00772_Firmware_V1.0*.
3. Read through Section 2.2.2.1 to customize the code.
4. Power up the board with an external supply (see Section 2.1.2) and connect the programmer.
5. Build and debug the modified project to download the code to the MSP430G2553.

3 Testing and Results

3.1 Test Setup

Figure 17 shows the load setup that is used to test the motor. the load is an electrodynamometer type load where the load torque that is applied to the motor is controllable.

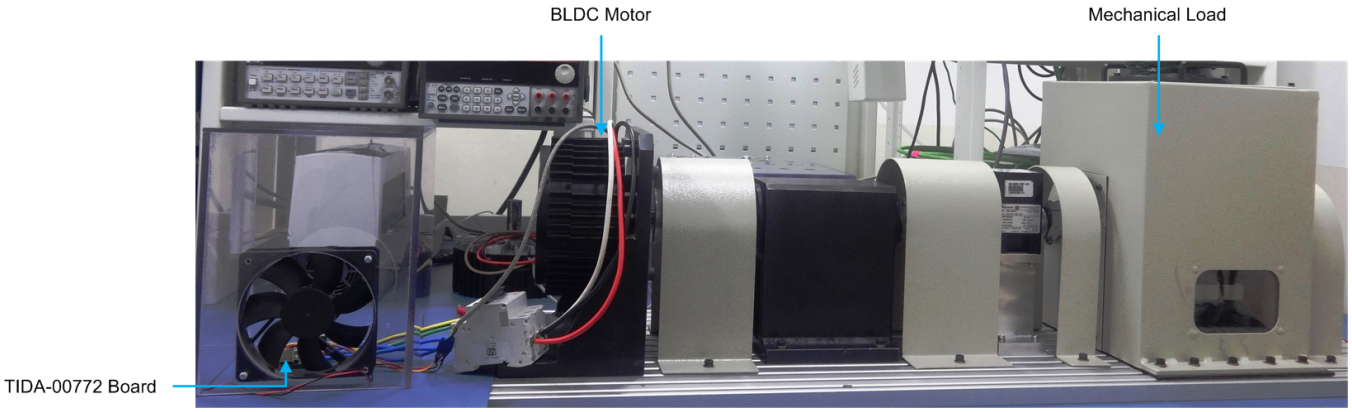


Figure 17. Board and Motor Test Setup

3.2 Test Data

3.2.1 Functional Tests

3.2.1.1 3.3-V Power Supply from DRV8305

The internal low-dropout (LDO) of the DRV8305 generates the 3.3 V over a wide DC supply input voltage down to 4.5 V. Figure 18 shows the 3.3 V generated from the DRV8305 at a DC input voltage of 18 V.

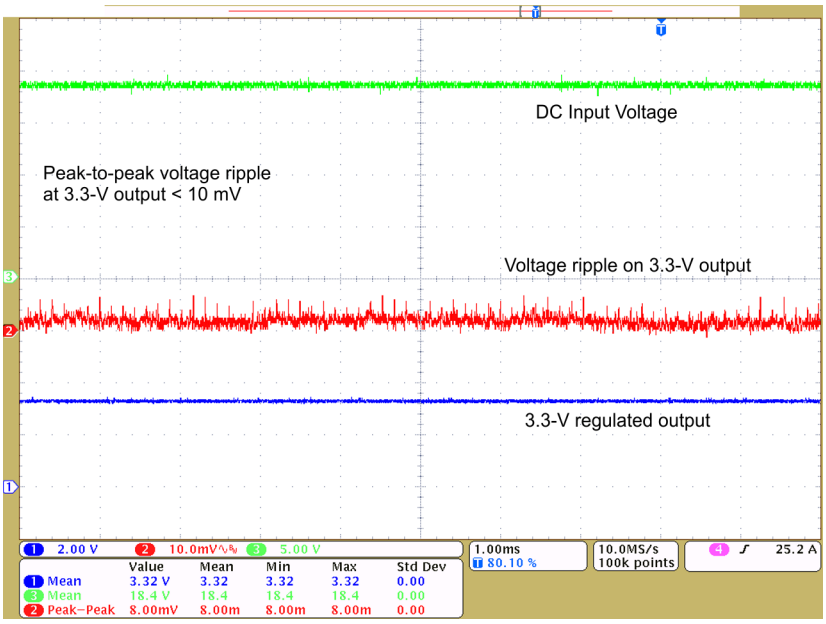


Figure 18. 3.3-V Regulator Output at 18-V DC Input

Figure 19 and Figure 20 show the AVDD and DVDD voltage generated by the DRV8305.

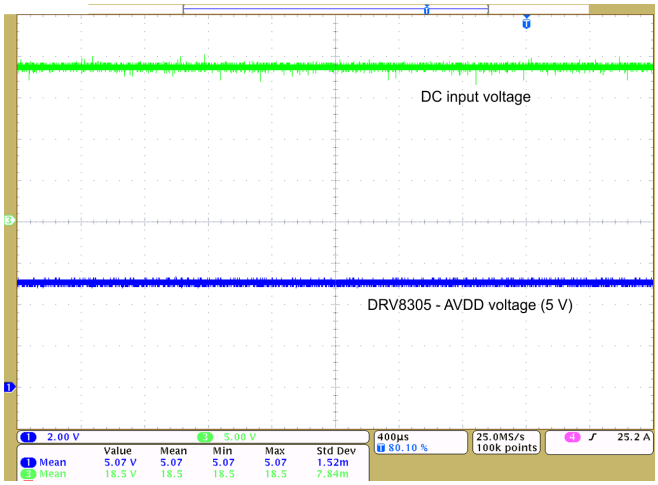


Figure 19. Voltage Generated by DRV8305 at 18-V DC Input – AVDD

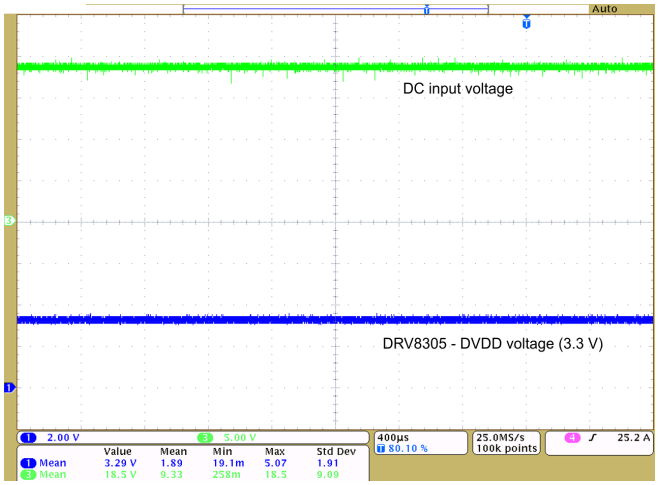


Figure 20. Voltage Generated by DRV8305 at 18-V DC Input – DVDD

Figure 21 and Figure 22 show the gate driver regulator voltages.

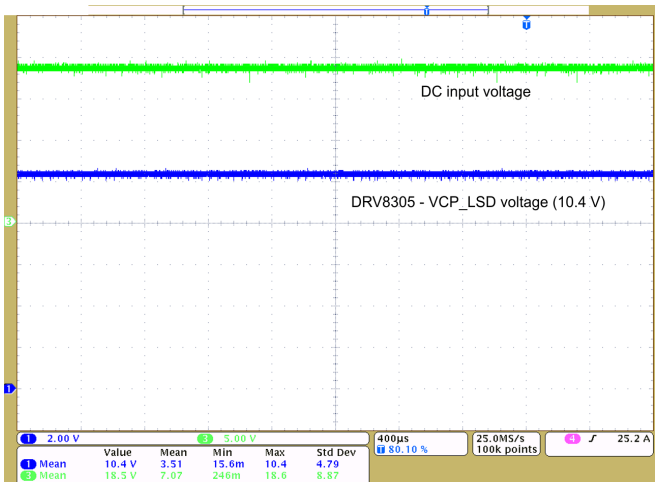


Figure 21. Low-Side Gate Driver Regulator Voltages From DRV8305 at 18-V DC Input – VCP_LSD

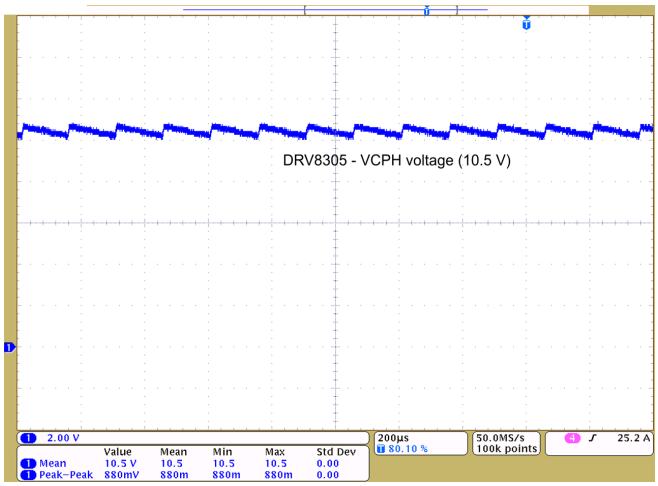


Figure 22. High-Side Gate Driver Regulator Voltages From DRV8305 at 18-V DC Input – VCP_LSD

3.2.1.2 PWM Signal From MCU and Gate Drive Output From DRV8305

Figure 23 shows the high-side and low-side PWM signals from the MSP430 and the corresponding gate drive output waveforms from DRV8305 at a DC input voltage of 18 V. The gate drive output voltage is approximately 10 V.

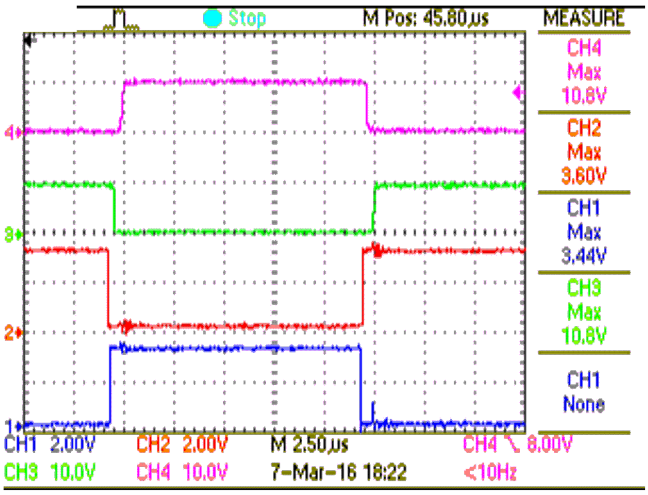


Figure 23. PWM Signals From MSP430™ and Gate Drive Output From DRV8305

3.2.1.3 Dead Time From DRV8305

Figure 24 shows the high-side and low-side gate source voltage from the DRV8305.

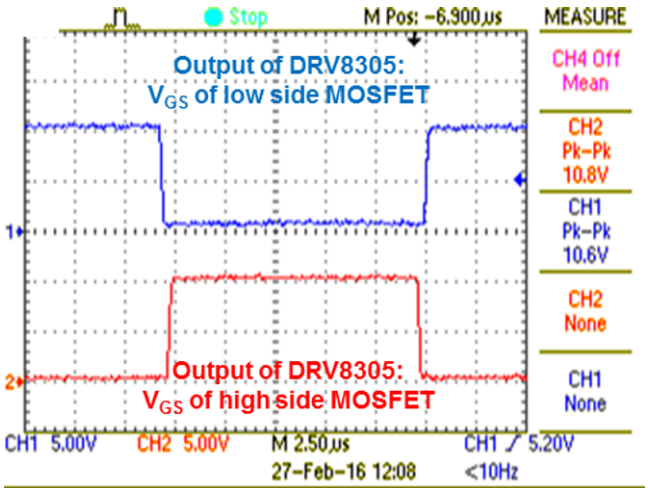


Figure 24. High-Side and Low-Side Gate Source Voltage

Figure 25 and Figure 26 show the dead time inserted by the DRV8305 at both edges of the PWM. The minimum dead time after hand shaking (td_min) from the DRV8305 is 280 ns. The dead time in addition to td_min is set by using the register bit DEAD_TIME. The waveform is taken with DEAD_TIME bits set for 35 ns; the total dead time is 280 ns + 35 ns = 315 ns.

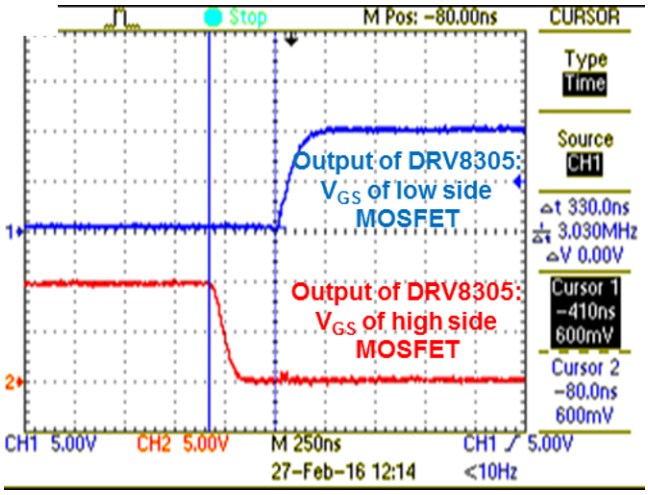


Figure 25. Dead Time Provided by DRV8305 at Rising Edge of Low-Side PWM

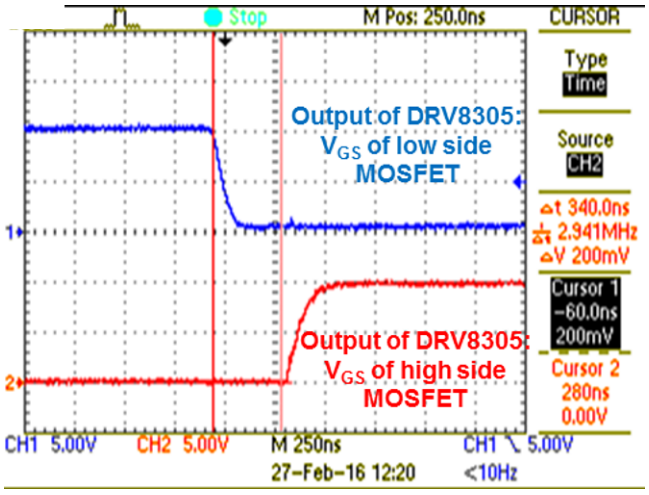


Figure 26. Dead Time Provided by DRV8305 at Falling Edge of Low-Side PWM

3.2.1.4 *Maximum Gate Drive Voltage From DRV8305 Ensures High-Efficiency Inverter*

Figure 27 shows the gate drive output waveforms from the DRV8305 when the input DC supply voltage is 5 V. The low-side gate drive output voltage is approximately 10 V, and the high-side gate drive output voltage is approximately 7.5 V. The internal triple-charge pump of the DRV8305 ensures the availability of a higher gate drive output voltage that improves the efficiency of the inverter. When the available gate drive voltage (V_{GS}) increases, the R_{DS_ON} of the FETs decreases, and hence efficiency improves.

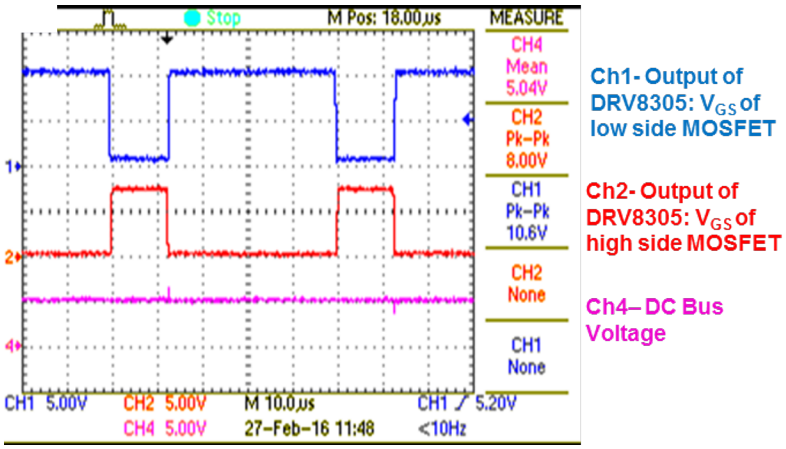


Figure 27. High-Side and Low-Side Gate Drive Output

3.2.1.5 MOSFET Switching Waveforms

Figure 28, Figure 29, Figure 30 and Figure 31 show the V_{DS} and V_{GS} waveforms of the low-side and high-side MOSFETs when the gate current of the DRV8305 (I_{DRIVE}) is set at 250-mA sink and 125-mA source.

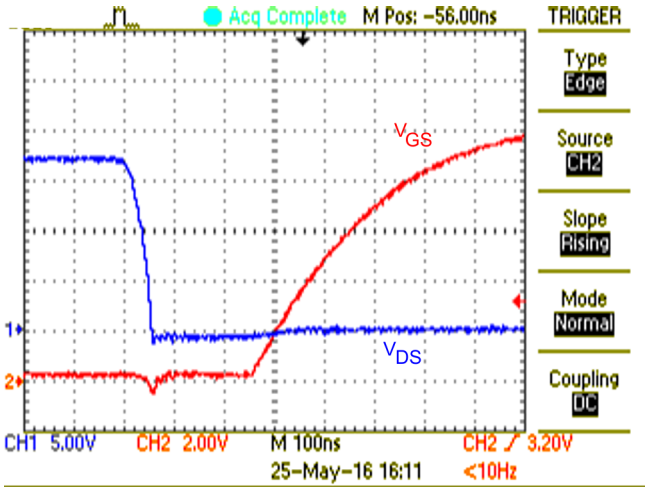


Figure 28. Low-Side FET Turnon Waveforms

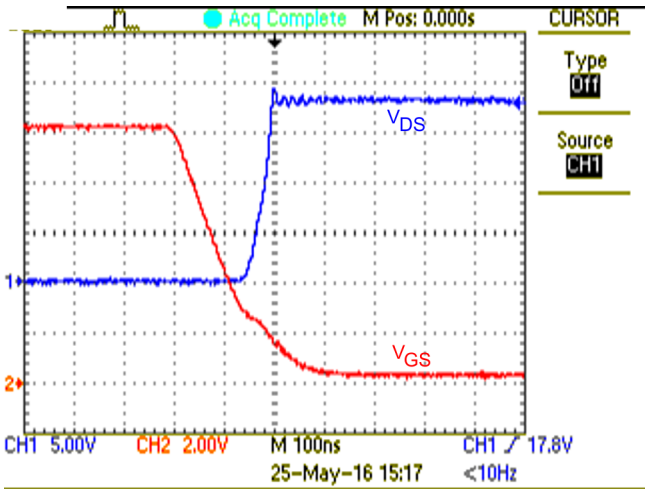


Figure 29. Low-Side FET Turnoff Waveforms

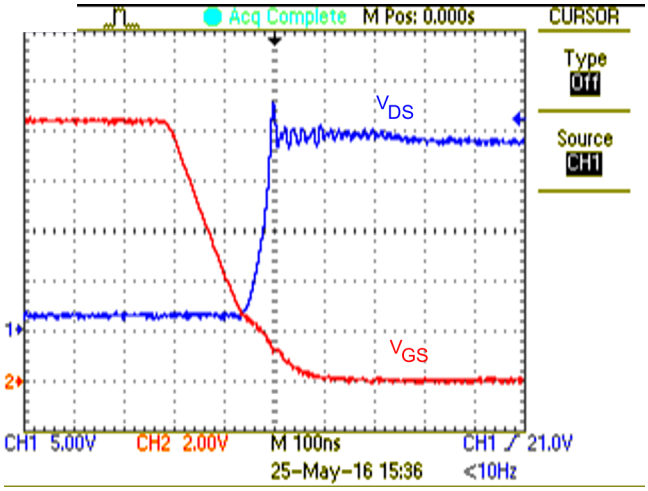


Figure 30. High-Side FET Turnon Waveforms

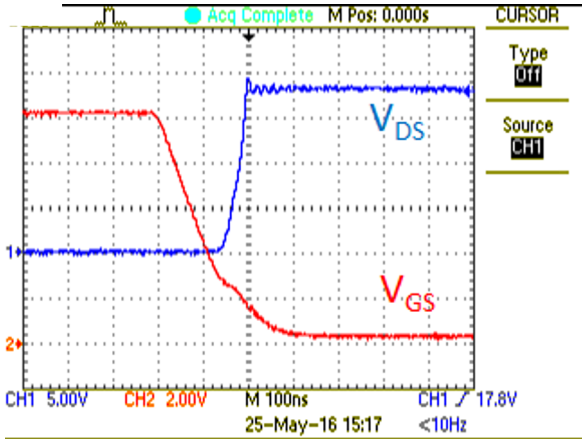


Figure 31. High-Side FET Turnoff Waveforms

Figure 32 and Figure 33 shows the effect of the I_{DRIVE} feature of the DRV8305 on the performance of the inverter stage. Figure 32 shows the V_{DS} and V_{GS} waveforms with a 500-mA sink current setting. Figure 33 shows the V_{DS} and V_{GS} waveforms with a 250-mA sink current setting. The dv/dt of the V_{DS} rise waveform is controlled with a different gate sink-current setting.

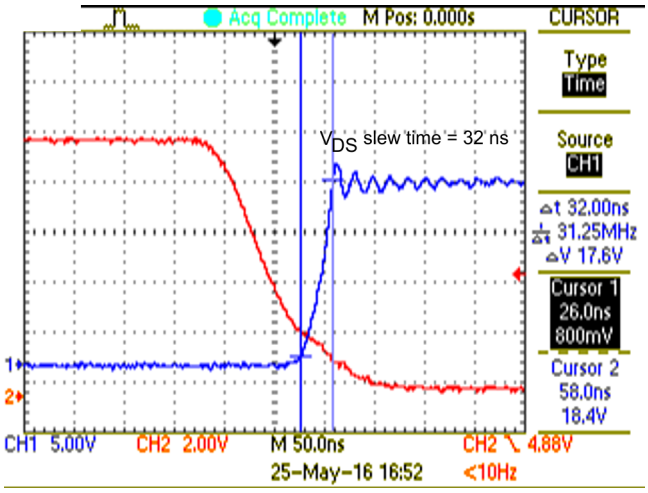


Figure 32. 500-mA Sink Current

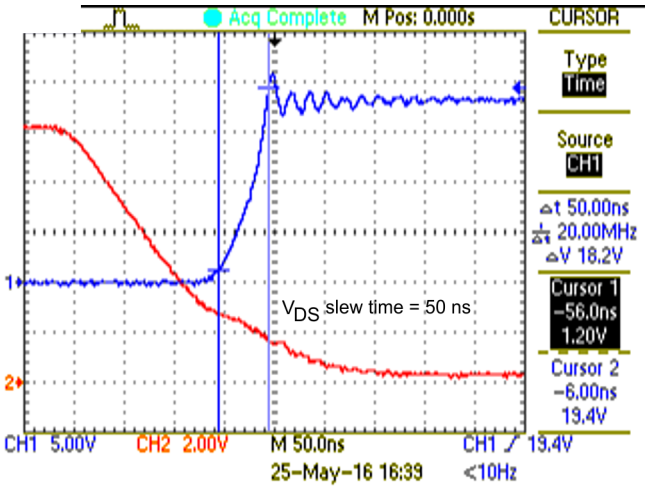


Figure 33. 250-mA Sink Current

3.2.2 Load Test

TI tested the TIDA-00772 board with an external BLDC motor and load using the test set up in Figure 17.

Figure 34 shows the motor winding current and winding voltage waveforms at 18-V DC input and 18-A_{RMS} winding current. The testing is done at 100% duty cycle. Figure 35 shows the steady-state thermal image of the board at the same condition, captured after 15 minutes of continuous operation. The maximum FET temperature observed was 79.2 °C.

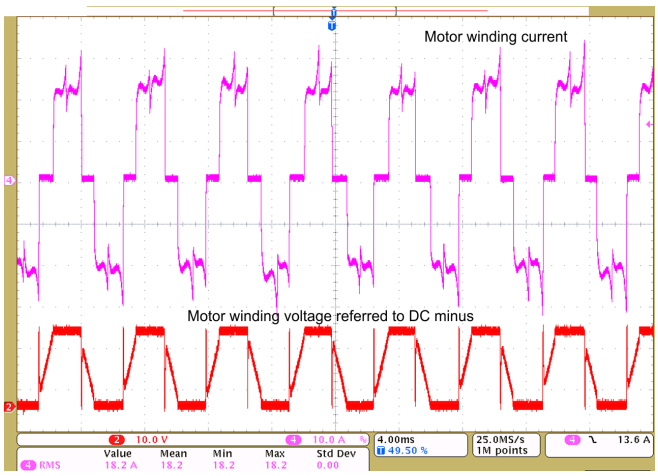


Figure 34. Load Test Results 1

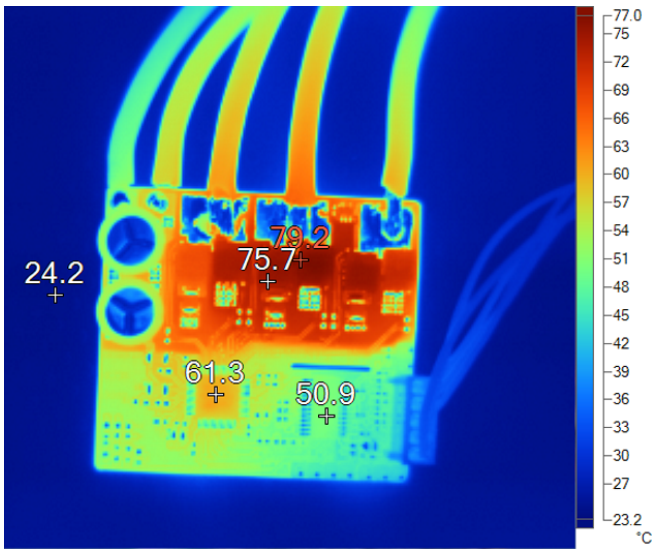


Figure 35. Thermal Image 1

TI Also tested the board at a DC input voltage of 21 V; this voltage is the maximum voltage available from a 5-cell Li-Ion battery (4.2 V maximum per cell). Figure 36 shows the motor winding current and winding voltage waveforms at 21-V DC input and 18.2-A_{RMS} winding current. The testing is done at 100% duty cycle. Figure 37 shows the steady state thermal image of the board at the same condition, captured after 15 minutes of continuous operation. The maximum FET temperature observed was 81.3 °C.

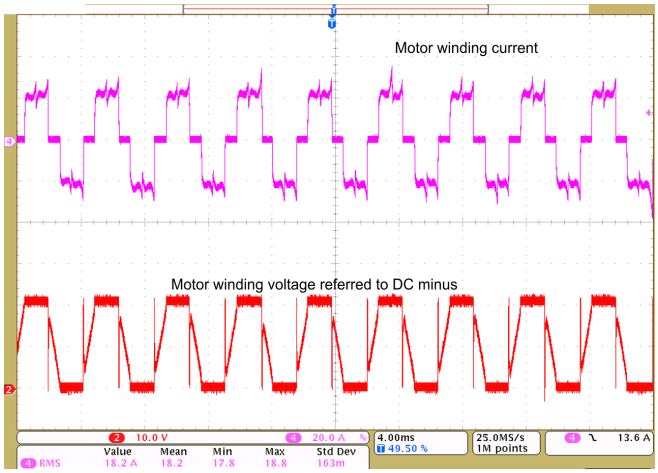


Figure 36. Load Test Results 2

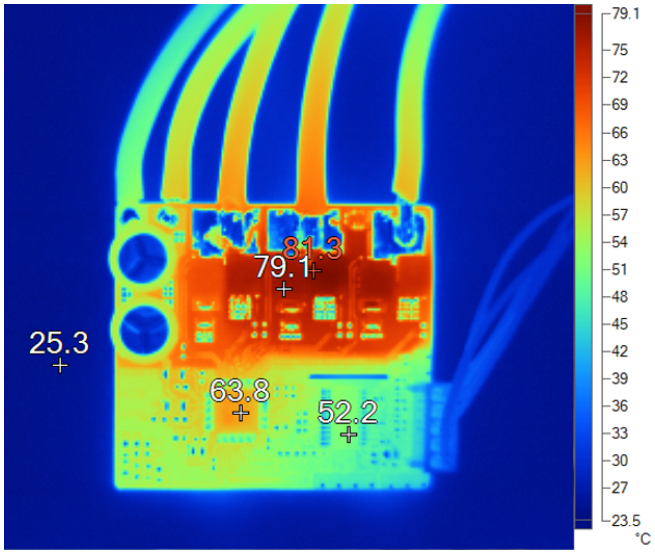


Figure 37. Thermal Image 2

Figure 38 shows the motor winding current and winding voltage waveforms at a 21-V DC input and 18.2-A_{RMS} winding current at 75% duty cycle. Figure 39 shows the steady-state thermal image of the board at the same condition, captured after 15 minutes of continuous operation. The maximum FET temperature observed was 86.6°C (observed on a low-side FET). The maximum temperature observed on the high-side FET was 75.1°C. The PWM is configured as an active, freewheeling, unipolar PWM.

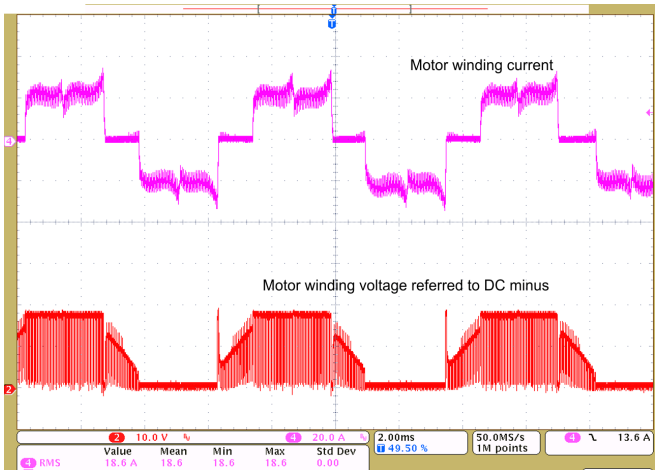


Figure 38. Load Test Results 3

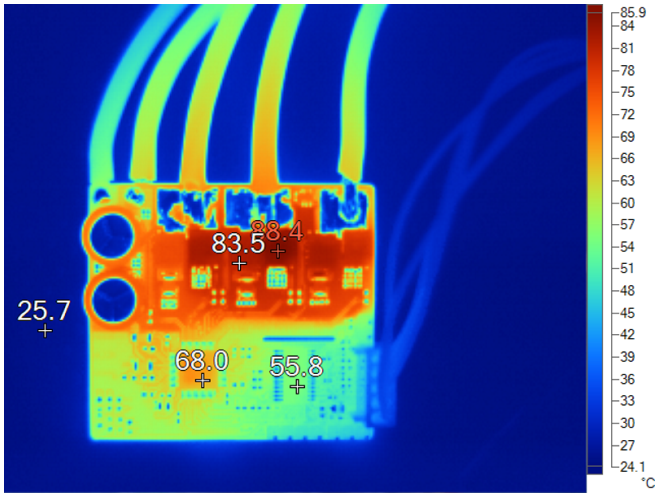


Figure 39. Thermal Image 3

The TIDA-00772 board was also tested for higher currents. Figure 40 shows the test results when the board is delivering a 24-A_{RMS} current to the motor winding.

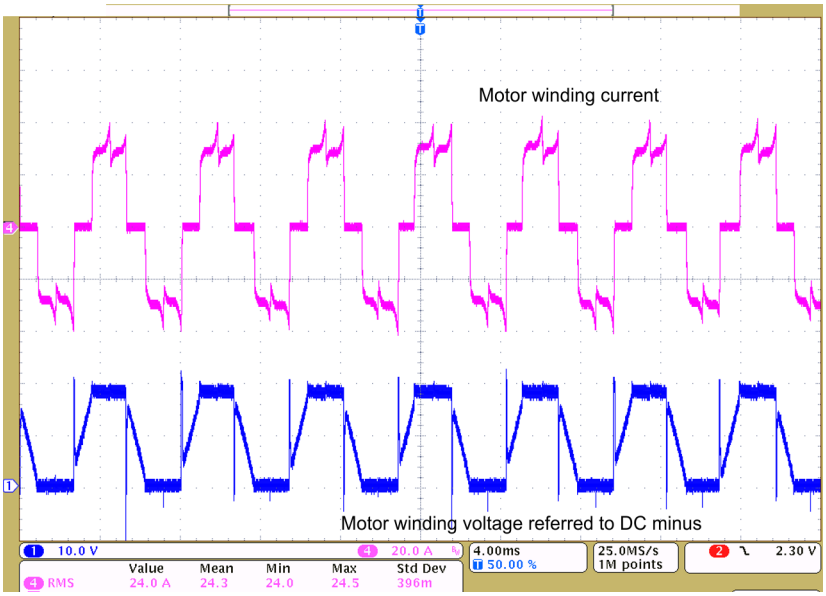


Figure 40. Load Test Results 4

3.2.3 Inverter Efficiency Test

Table 4 shows the test results with 100% duty cycle. The inverter efficiency is experimentally tested with a load setup (see Figure 17).

Table 4. Inverter Efficiency Test Results at 100% Duty Cycle

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY (%)
18.05	7.38	6.029	130.72	129.381	98.98
17.985	8.7151	7.135	155	153.419	98.98
17.918	11.196	9.198	199.32	197.284	98.98
17.919	13.688	11.278	244.08	241.599	98.98
17.937	16.193	13.368	289.14	285.91	98.88
17.888	18.668	15.437	332.32	328.44	98.83
17.939	21.191	17.553	378.1	373.12	98.68
17.994	22.858	18.961	408.9	403.39	98.65

Figure 41 shows the efficiency variation with inverter output.

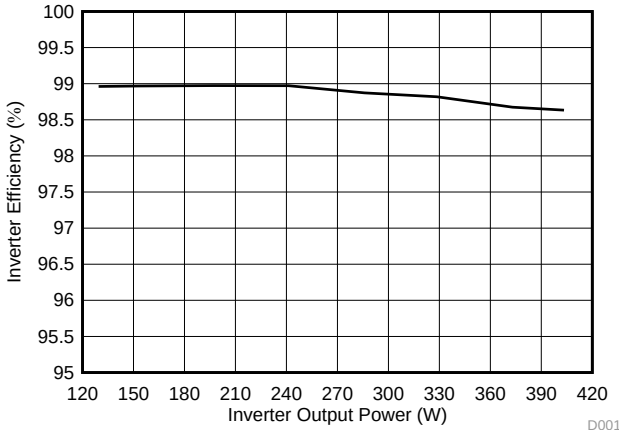


Figure 41. Inverter Efficiency Versus Output Power – 100% Duty Cycle

The test results with 90% duty cycle are shown in Table 5 and the efficiency variation with inverter output is shown in Figure 42.

Table 5. Inverter Efficiency Test Results at 90% Duty Cycle

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY (%)
18.054	5.795	5.192	102.03	99.50	97.52
17.972	7.688	6.933	136.56	133.75	97.94
17.986	9.915	8.985	177.18	173.85	98.12
17.982	12.146	11.041	217.36	213.31	98.14
17.945	14.339	13.073	256.18	251.29	98.09
17.985	16.594	15.166	297.02	291.27	98.06
17.97	18.842	17.253	336.67	330.09	98.05
17.995	20.325	18.656	363.12	355.90	98.01

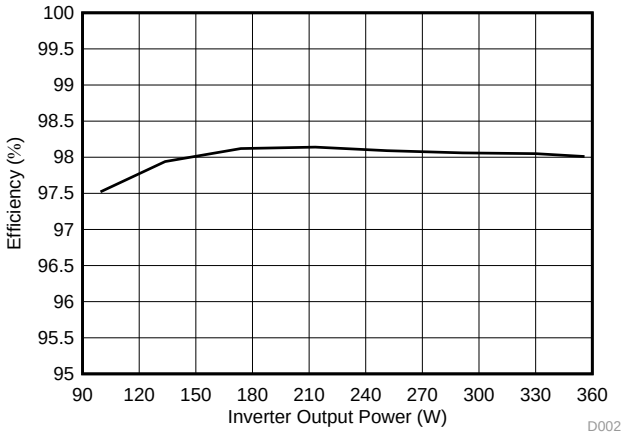


Figure 42. Inverter Efficiency Versus Output Power – 90% Duty Cycle

3.2.4 Temperature Rise Test

The power stage must provide high current to the motor for a small duration of time (a few hundred milliseconds), enabling the motor to deliver peak torque in power-tool applications. Figure 43 shows the temperature rise of the MOSFETs over time when the board is delivering 20 A_{RMS} to the motor winding. The results are taken at an ambient temperature of 22°C. The curve shows that the steady-state absolute temperature observed on the FET is 80°C, meaning the board can deliver 20 A_{RMS} continuously, even at an ambient temperature of 55°C and the MOSFET junction temperature will be in the safe operating limit.

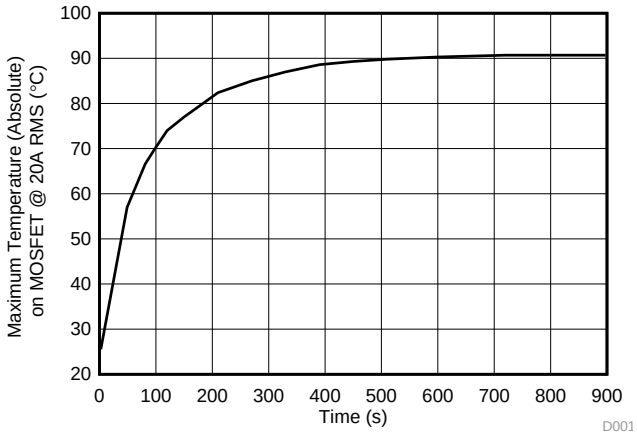


Figure 43. Load Test Results 5

Figure 44 shows the temperature rise of the MOSFETs over time when the board is delivering 25 A_{RMS} to the winding. The results are taken at an ambient temperature of 22°C. The results show that the board can deliver 25 A_{RMS} for 60 s, even at an ambient of temperature of 55°C.

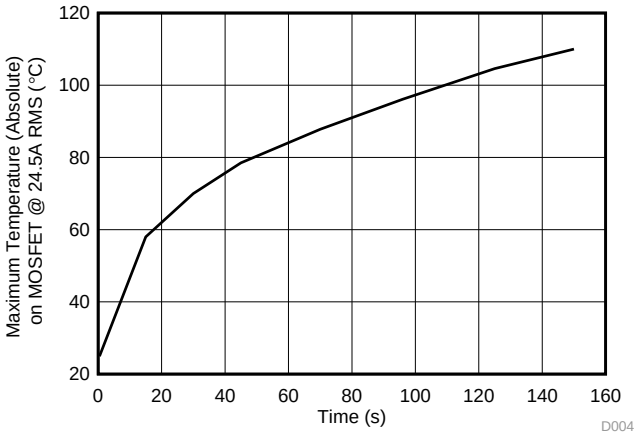


Figure 44. Load Test Results 6

3.2.5 Overcurrent and Short-Circuit Protection Test

3.2.5.1 Effect of Amplifier Blanking Time in Current Sensing

In BLDC motor current sensing using shunt resistors, the sense-resistor voltage may have transient noise voltage because of:

- Inductive coupled noise when the MOSFETs are switching
- The voltage drop across the small inductance of the sense resistors because of high di/dt during switching

The DRV8305 current-sense amplifiers have a programmable blanking time (delay) at the amplifier outputs. The blanking time is implemented from any rising or falling edge of the gate drive outputs. The blanking time is applied to all three current sense amplifiers equally. If the current sense amplifiers are already being blanked when another gate driver rising or falling edge is seen, the blanking interval restarts at the edge.

NOTE: The blanking time options do not include delays from internal amplifier loading or delays from the trace or component loads on the amplifier output. The programmable blanking time may be overridden to have no delay (default value).

Figure 45 and Figure 46 show the noise rejection in current sense amplifiers by using the blanking time feature of DRV8305 current sense amplifier.

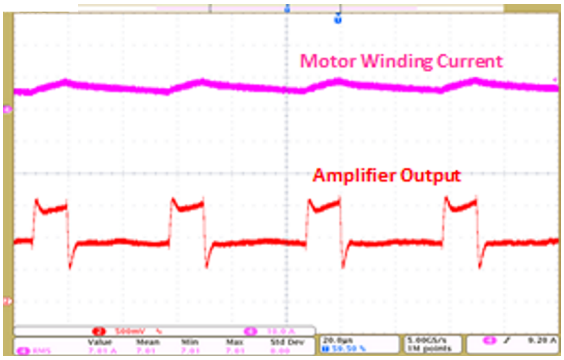


Figure 45. Effect of Blanking Time on Amplifier Output – Without Blanking

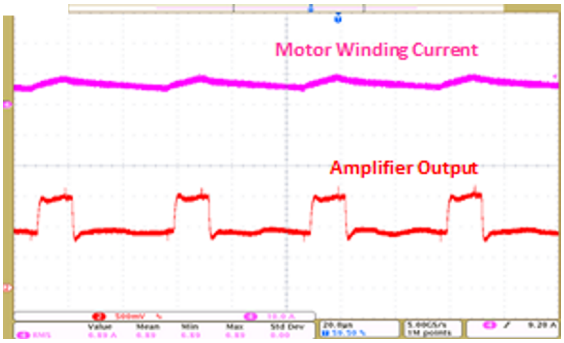


Figure 46. Effect of Blanking Time on Amplifier Output – With 500-ns Blanking

3.2.5.2 Cycle-by-Cycle Overcurrent Protection

Figure 47 and Figure 48 show the overcurrent test results when the motor is loaded to draw high current and with the following configurations:

- Amplifier gain (G) = 40 V/V
- Amplifier blanking time = 500 ns
- Offset reference in the DRV8305 ($V_{REF} \div k$) = 0.825 V
- Comparator reference (V_{COMP_REF}) = 1.6 V
- Shunt resistance (R_{SENSE}) = 0.5 mΩ

Use Equation 10 to calculate the theoretical current limit.

$$I_{CL} = \frac{\left(V_{COMP\_REF} - \left(V_{REF} \div k\right)\right)}{R_{SENSE} \times G} \tag{10}$$

$$I_{CL} = \frac{1.6 - 0.825}{0.0005 \times 40} = 38.75 \text{ A}$$

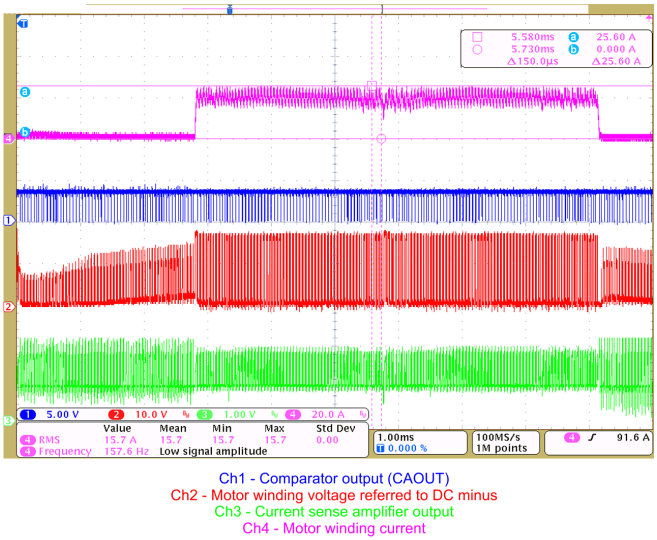


Figure 47. Cycle-by-Cycle Overcurrent Protection With Overloading

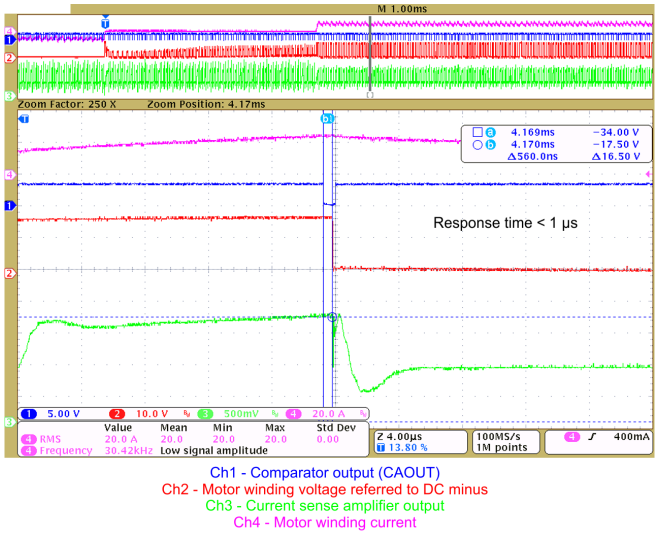


Figure 48. Response Time of Cycle-by-Cycle Overcurrent Protection

For low-inductance BLDC motors (typically from a few microhenries [µH] to tens of millihenries [mH]) a high winding resistance-to-inductance ratio leads to a high rate of winding current rise. The current-limit protection must be fast (below 1 µs) and act in every PWM cycle to avoid any short current spikes.

Figure 48 is a zoomed view of Figure 47. When the comparator output goes low, the buffer turns off the high-side PWM even though the PWM signal is high at the output of the MCU. The delay (beginning when the comparator output goes low and the turnoff of the high-side switch) is less than 1 µs.

3.2.5.3 Cycle-by-Cycle Stall Current Protection

Figure 49 shows the test setup to simulate a stall current when the motor is rotating. S1 is a single-throw, double-pole switch that is connected between the motor terminals. This test setup is used to create a motor winding to a winding short.

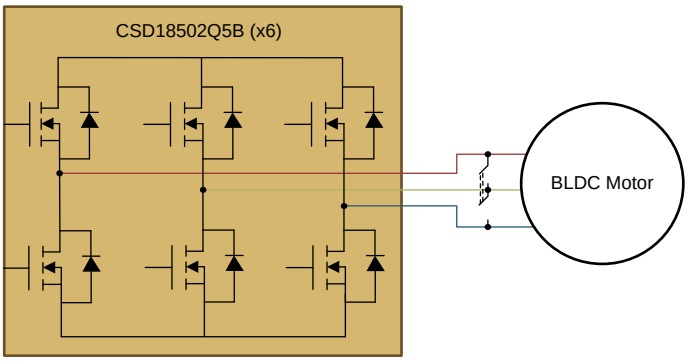


Figure 49. Test Setup to Simulate Stall Current

Before S1 is closed, the motor rotates at a steady speed. Figure 50 and Figure 51 show the waveforms obtained when the switch S1 is closed. When S1 is closed, S1 carries the short-circuit current. During this condition the motor stops, causing the Hall state to continue at the current commutation state; the controller continues to generate the PWM corresponding to this commutation state. The test results in Figure 50 and Figure 51 have the following configurations:

- Amplifier gain = 40 V/V
- Amplifier blanking time = 500 ns
- Offset reference in the DRV8305 = 0.825 V
- Comparator reference = 1.6 V
- Shunt resistance = 0.5 mΩ

See Equation 10 for the theoretical overcurrent limit.

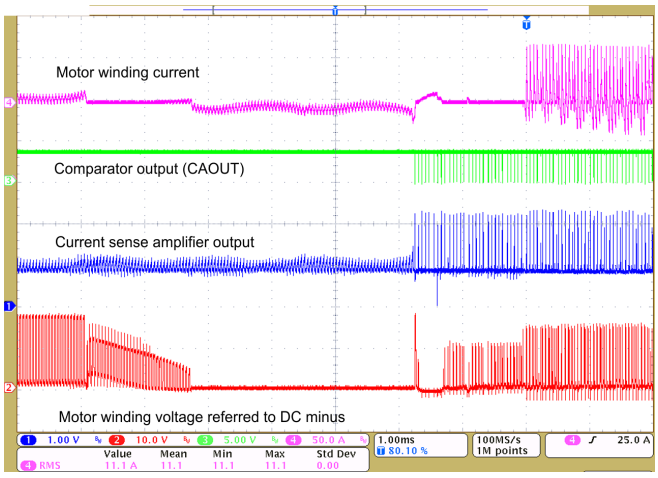


Figure 50. Cycle-by-Cycle Overcurrent Protection with Motor Stall

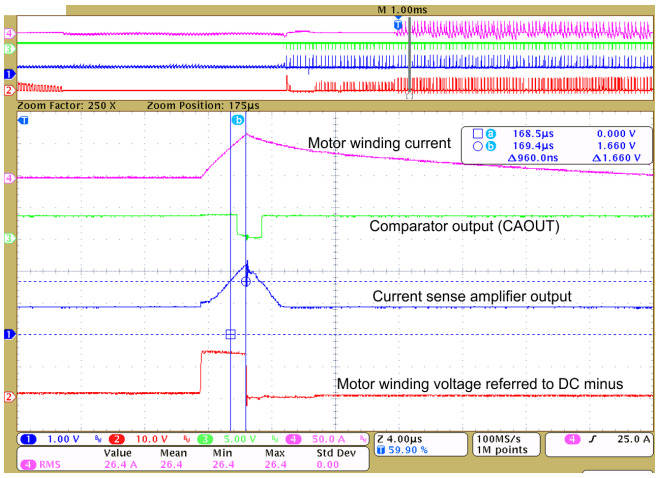


Figure 51. Zoomed View of Cycle-by-Cycle Overcurrent Protection with Motor Stall

Figure 51 is a zoomed view of Figure 50. When the amplifier output reaches 1.6 V, the comparator output goes low and the buffer turns off the high-side PWM. The delay (beginning when the comparator output goes low and the turnoff of the high-side switch) is less than 1 µs.

NOTE: Under a short-circuit condition the rate of change of current is very high. In this case (from the current waveform) the current is raising to 60 A in approximately 2.8 µs. The inductance of the sense resistor creates additional voltage across the sense resistor at such high di/dt and affects the op amp output. Calculate the reference threshold for current limit by considering the inductance of the sense resistor.

3.2.5.4 Stall-Current Latch Protection by DRV8305 V_{DS} Sensing

The same test setup in Figure 49 is used for the stall-current protection. The V_{DS} reference used is 0.109 V by writing in the register of the DRV8305 (see the following code). The latch protection acted at 65 A.

```
WriteRegister(0x0C, (VDS_LEVEL_0D109V + VDS_MODE_LATCH));
```

Figure 52 and Figure 53 show the test results with latch protection by V_{DS} sensing. When a V_{DS} overcurrent event occurs, the device pulls all gate drive outputs low to put all six external MOSFETs into high-impedance mode. This overcurrent event reports on the nFAULT pin. The SPI status registers report which MOSFET the overcurrent event was detected on.

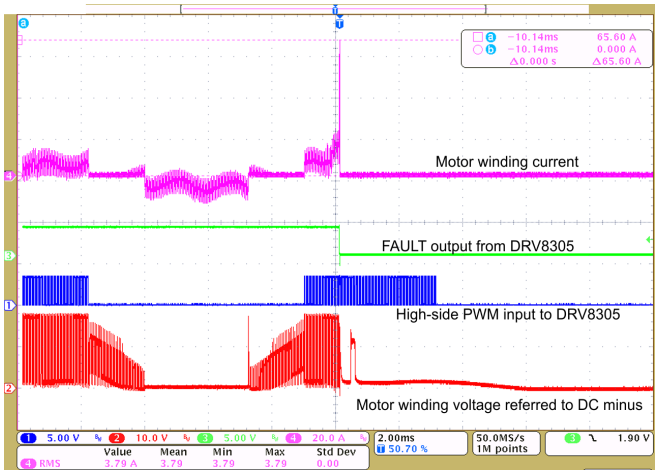


Figure 52. Overcurrent Latch Protection With Motor Stall by V_{DS} Sensing

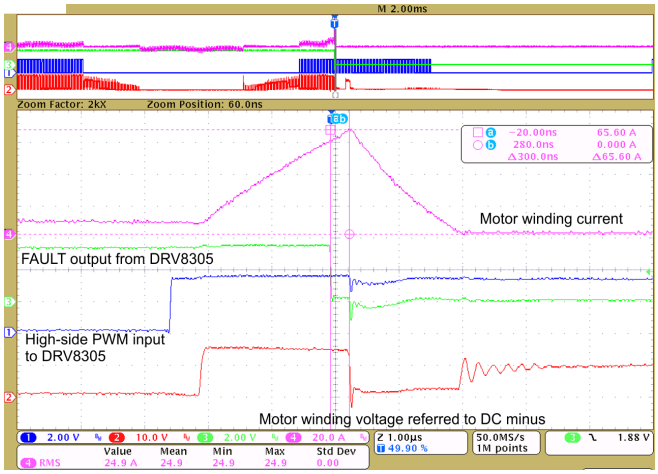


Figure 53. Zoomed View of Figure 52

Figure 54 shows the test results of a latch protection when the inverter output is shorted. The same test setup in Figure 49 is used for the short-circuit simulation. The V_{DS} reference used is 0.109 V by writing in the register of the DRV8305. The latch protection acted at 46 A.

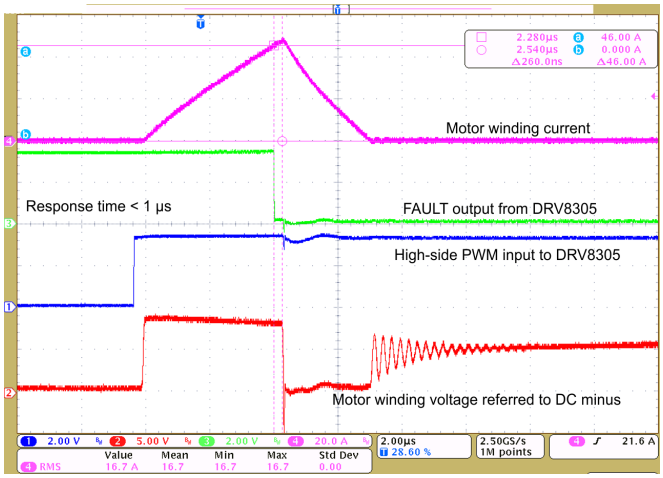


Figure 54. Overcurrent Latch Protection With Inverter Output Shorted

3.2.6 Testing With External Airflow

The test setup with external airflow is shown in Figure 55. The maximum temperature ovserved on the MOSFETs at different winding currents is shown in Figure 56. The testing is done at 200 LFM. The board can continuously deliver 25 A_{RMS} at a 200-LFM airflow and the steady state maximum temperature on the MOSFET is approximately 82°C. The testing is done at an ambient temperature of 23°C.

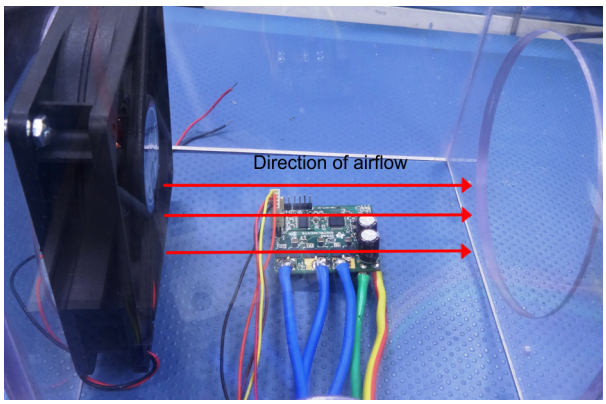


Figure 55. Test Setup and Direction of Airflow

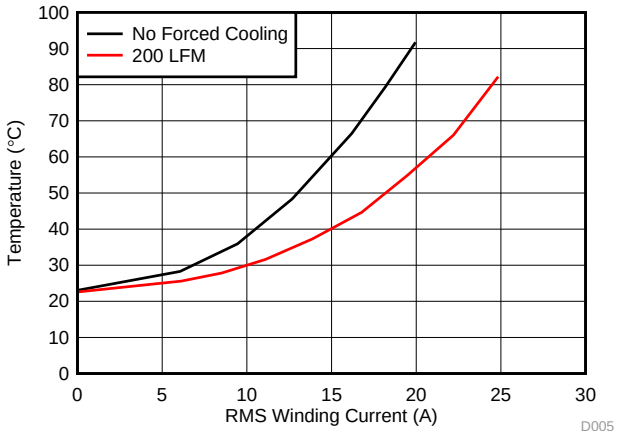


Figure 56. Maximum Steady-State Temperature on MOSFETs With Different Airflow

3.2.7 Testing for Peak Current Capability

The board is tested with a 60-A peak current for 1 s. Figure 57 shows the winding current of 66.8 A when the motor is stalled for 1.1 s. Figure 58 shows the thermal image of the board after 1.1 s. The high peak current capability ensures that the power stage aids the motor to deliver high peak torque in power-tool applications. Overtemperature protection or blocked rotor protection shuts off the system if the stall current continues to be high.

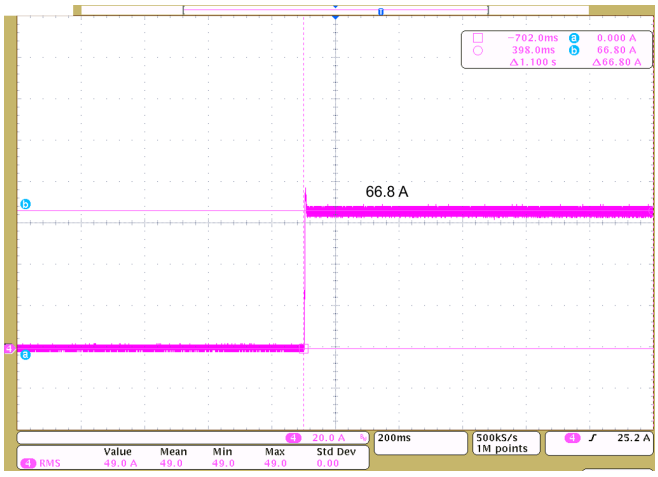


Figure 57. Peak Current of 66.8 A in Motor Winding During Motor Stall

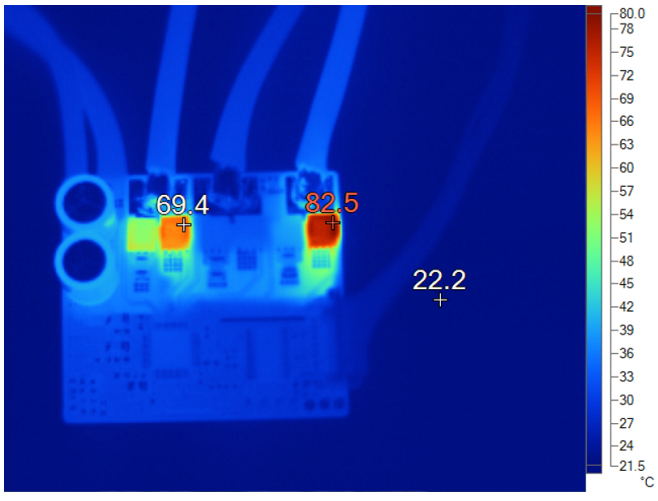


Figure 58. Thermal Image of Board After 1.1 s

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00772.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00772.

4.3 PCB Layout Recommendations

Use the following recommendations when designing a PCB for the DRV8305. See Figure 59 for an example layout.

- Connect the DVDD and AVDD 1-µF bypass capacitors directly to the adjacent GND pin to minimize loop impedance for the bypass capacitor.
- Place the CP1 and CP2 0.047-µF flying capacitors next to the DRV8305 charge-pump pins.
- Place the VCPH 2.2-µF and VCP_LSD 1-µ bypass capacitors close to the corresponding pins with a direct path back to the DRV8305 GND net.
- Place the PVDD 4.7-µF bypass capacitor as close as possible to the DRV8305 PVDD supply pin.

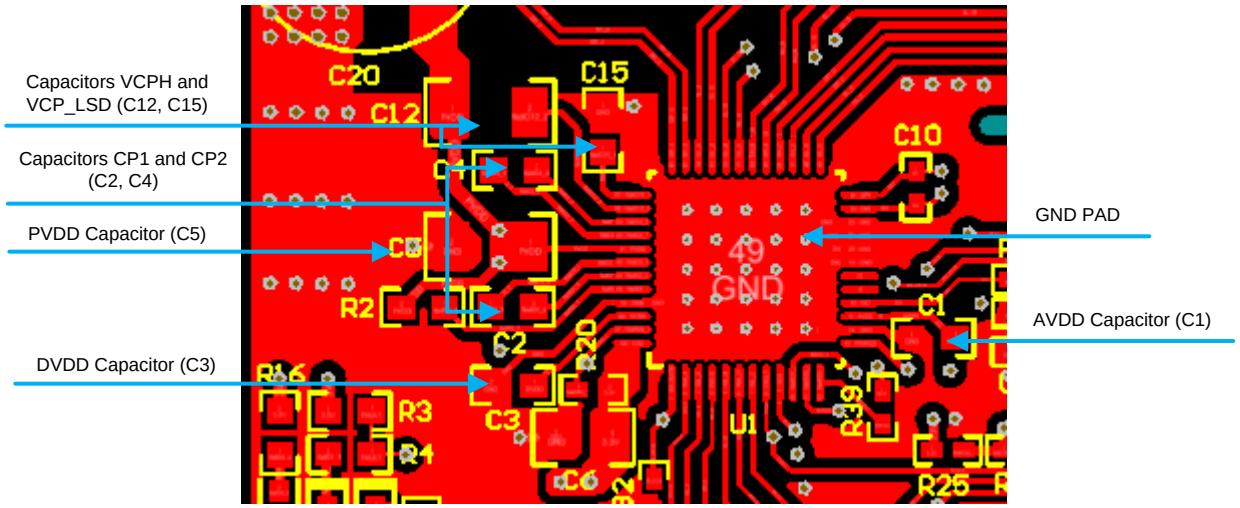


Figure 59. Layout Recommendations for Decoupling Capacitors

- Minimize the loop length for the high-side and low-side gate drivers. the high-side loop is from the DRV8305 GH_X to the power MOSFET and returns through SH_X. The low-side loop is from the DRV8305 GL_X to the power MOSFET and returns through SL_X. See Figure 60 for an example layout.

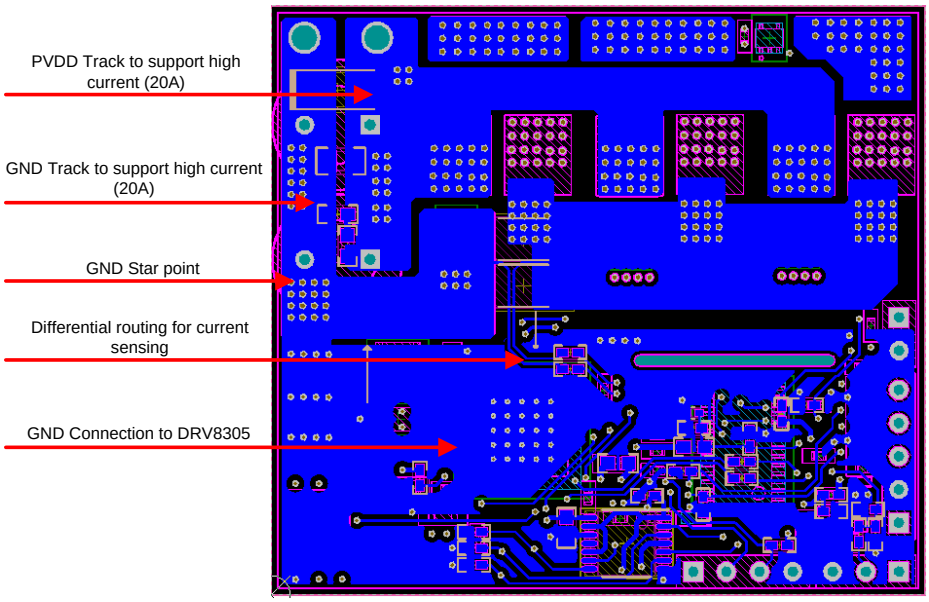


Figure 60. Gate Drive Connection From DRV8305

- Route the track for sensing the V_{DS} of the MOSFET as a differential track.

In the reference design the PCB is a four-layer layout with 2-Oz (70-micron) copper thickness in each layer. The power tracks are wide to carry a high current. Figure 61 shows the current carrying track from the power input point. The tracks are repeated in different layers and are connected by arrays of stitching vias.

A GND star point is defined in the PCB where the GND path for the DRV8305 and other signal circuits in the board is tapped.

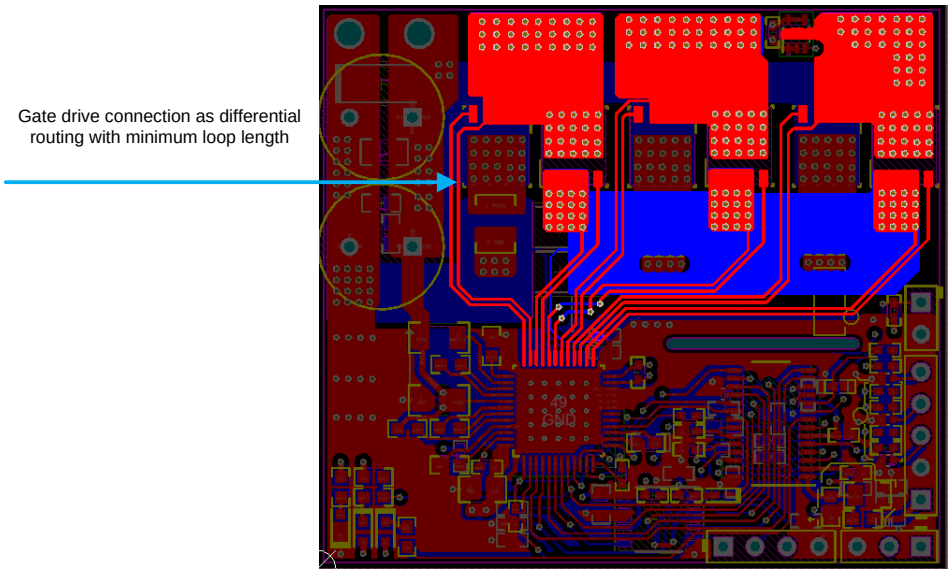


Figure 61. Bottom Layer of PCB – Power Tracks and GND Star Connection

- Increase the copper area around the MOSFET pad as much as possible to improve thermal dissipation from the MOSFET to the PCB. Use arrays of vias under the drain pad of the MOSFET to help spread heat to the bottom surface copper area. Add a small heat sink or copper bars to the bottom surface of the PCB to improve heat dissipation.
- Consider the placement of the decoupling capacitors so the V_{DS} sensing protection of the DRV8305 functions properly. Place these capacitors near each MOSFET. The return path of the decoupling capacitor must be through a thick track, and the return-path length must be short to improve decoupling.
- Use the slot that is provided in the PCB above the MCU to limit the theat spread to the MCU (see Figure 62).

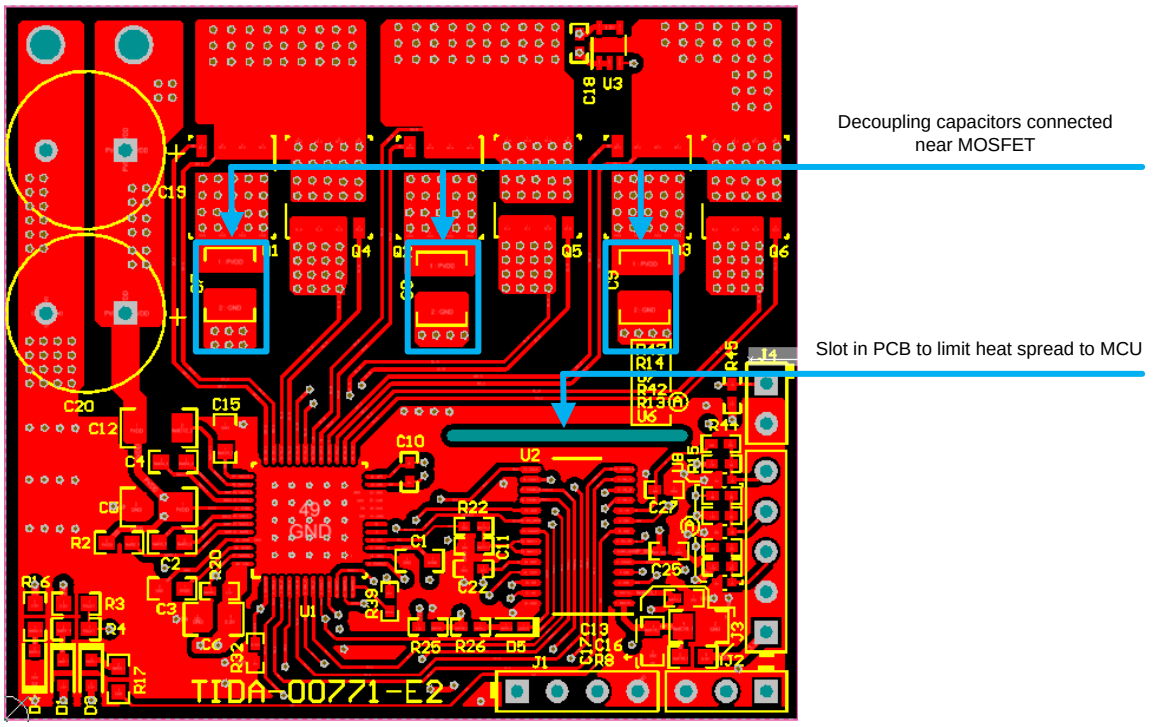


Figure 62. Placement of Decoupling Capacitors for Inverter Legs

The board has the provision for the bottom-side heat sink. Use a thermally conductive and electrically-insulated thermal pad between the PCB bottom side and the heat sink. Figure 63 shows the space for the bottom-side heat sink.

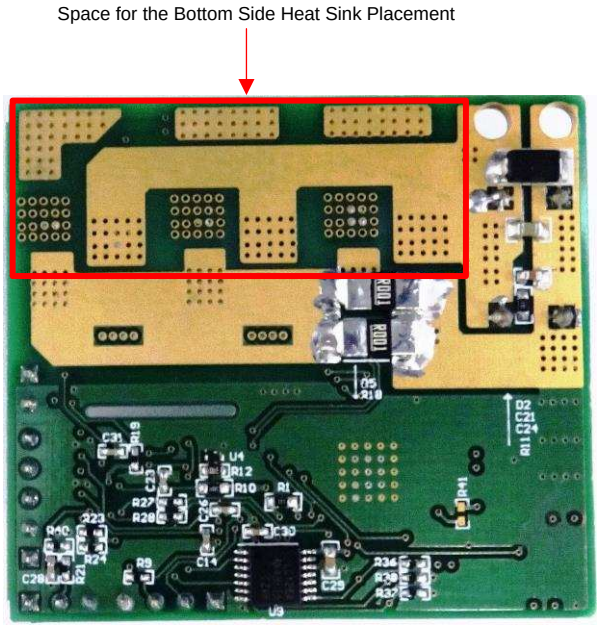


Figure 63. Space for Bottom-Side Heat Sink

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00772.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-00772.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00772.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00772.

5 Software Files

To download the software files, see the design files at TIDA-00772.

6 References

1. Texas Instruments, *Sensored 3-Phase BLDC Motor Control Using MSP430*, Application Report (SLAA503)
2. Texas Instruments, *Understanding IDRIVE and TDRIVE in TI Motor Gate Drivers*, Application Report (SLVA714)
3. Texas Instruments, *DRV8305 Three Phase Gate Driver With Current Shunt Amplifiers and Voltage Regulator*, Data Sheet (SLVSCX2)
4. Texas Instruments, *MSP430G2x53, MSP430G2x13 Mixed Signal Microcontroller*, Development Tools (MSP430)

7 Terminology

BLDC— Brushless DC motor

ESD— Electrostatic discharge

FET— Field-effect transistor

MOSFET— Metal-oxide semiconductor field-effect transistor

PWM— Pulse width modulation

RMS— Root mean square

RPM— Rotation per minute

SPI— Serial peripheral interface

8 About the Author

MANU BALAKRISHNAN is a systems engineer at Texas Instruments where he is responsible for developing subsystem design solutions for Industrial Systems. Manu brings his experience in power electronics and analog and mixed signal designs to this role. He has system level product design experience in permanent magnet motor drives. Manu earned his Bachelor of Technology in Electrical and Electronics Engineering from the University of Kerala, and his Master of Technology in Power Electronics from the National Institute of Technology Calicut, India.

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