*Errata*

# *CC2340R5-Q1 SimpleLink™ Wireless MCU Device Revision B*


**ABSTRACT**

This document describes the known exceptions to functional specifications (advisories) to the CC2340R5-Q1 and CC2340R53-Q1 SimpleLink™ devices.


## Table of Contents



## Trademarks

# 1 Advisories Matrix

Table 1-1 lists all advisories, modules affected, and the applicable silicon revisions.

**Table 1-1. Advisories Matrix**

| MODULE | DESCRIPTION | SILICON REVISIONS AFFECTED | |
|---|---|---|---|
| | | CC2340R5-Q1 | CC2340R53-Q1 |
| | | Revision Affected | |
| SPI | Advisory SPI_04—Hang scenario with SPI waiting for CPU intervention forever | B | B |
| ADC | Advisory ADC_08—ADC BUSY bit not cleared in repeat single, sequence and repeat sequence conversion modes. | B | B |
| ADC | Advisory ADC_09—ADC can have random conversion errors. | B | B |
| BATMON | Advisory BATMON_01—Incorrect temperature measurement | B | B |
| BATMON | Advisory BATMON_02—Spurious temperature update interrupts from BATMON in standby | B | B |
| CKM | Advisory CKM_01—Tracking loop issues during standby-wake | Not Affected | B |
| CKM | Advisory CLK_01—Bluetooth Low Energy link may not be maintained when using LFOSC only | B | B |
| I2C | Advisory I2C_02—SDA and SCL open-drain output buffer issue | B | B |
| GPIO | Advisory GPIO_01—Open-drain configuration can drive a short high pulse | B | B |
| PMU | Advisory PMU_01—Slow Transition Across Brown-Out Detect (BOD) Threshold Might Cause the Device to Hang | B | B |
| UART | Advisory UART_01—UART might issue spurious µDMA write burst requests | B | B |

**Table 1-2. Latest Revision by Part Number**

| Part Number | Revision |
|---|---|
| CC2340R5-Q1 | B |
| CC2340R53-Q1 | B |

# 2 Nomenclature, Package Symbolization, and Revision Identification

## 2.1 Device and Development Support-Tool Nomenclature

To designate the stages in the product development cycle, Texas Instruments™ stage identifiers for all devices and support tools. Devices are assigned one of two designators: X or P, to indicate non-production versions of the silicon die (for example, CC2340Q/R53/TI X). Fully qualified production versions carry no designator. Texas Instruments recommends two possible designators for its support tools: TMDX and TMDS. These designators represent evolutionary stages of product development from engineering prototypes (X/TMDX) through fully qualified production devices/tools (TMDS).

Device development evolutionary flow:

**X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow

**P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications

**no designator** Production version of the silicon die that is fully qualified

Support tool development evolutionary flow:

**TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing

**TMDS** Fully-qualified development-support product

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Prototype devices (marked with X or P) have a greater failure rate than fully qualified production devices. Texas Instruments advises against their use in production systems, as their long-term reliability has not been fully characterized. Only fully qualified production devices should be used in end products.

### 2.2 Devices Supported

This document supports the following device:

- CC2340R5-Q1
- CC2340R53-Q1

### 2.3 Package Symbolization and Revision Identification

Figure 2-1 and Table 2-1 describe package symbolization and the device revision code.

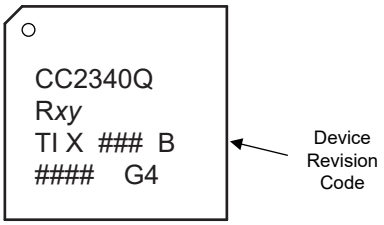


**Figure 2-1. Package Symbolization**

***xy*** Denotes the flash and RAM specifications

**Table 2-1. Revision Identification**

| Device Revision Code | Silicon Revision |
|---|---|
| B | PG2.0 |

## 3 Advisories

**SPI_04** ***Hang scenario with SPI waiting for CPU intervention forever***

**Revisions Affected** B

**Details** When the CPU is reading or writing the SPI FIFO using FIFO level triggers to generate interrupts, the system can hang. After the first interrupt is serviced, the FIFO level can permanently be below or above the configured threshold and not generate a subsequent CPU interrupt. This can lead to a hang scenario with SPI waiting for CPU intervention forever.

**Workaround**

1. Use polling of FIFO status within SPI and do not rely on FIFO level configured interrupts, or
2. Use only empty/overflow interrupts and do not use FIFO level configured interrupts, or
3. Use FIFO level configured interrupts along with empty (for TXFIFO) and overflow (for RXFIFO) as a failsafe to avoid hang scenarios.

**ADC_08** ***ADC BUSY bit not cleared in repeat single, sequence, and repeat sequence conversion modes***

**Revisions Affected** B

**Description** When the ADC is configured in repeat single, sequence, or repeat sequence conversion modes with trigger policy as trigger next in the MEMCTLx register, software attempting to

**ADC_08** (continued) ***ADC BUSY bit not cleared in repeat single, sequence, and repeat sequence conversion modes***

stop the conversion sequence by clearing the ENC bit does not clear the BUSY bit in the STATUS register. In the case of sequence conversion mode with trigger next policy, the BUSY bit is cleared at the end of the conversion sequence.

**Workaround**

To stop the conversions and to clear the BUSY bit in the above-mentioned ADC operating scenario, the following software sequence can be followed.

1. Write CTL0.ENC = 0
2. Change CTL1.TRIGSRC to SOFTWARE
3. Write CTL1.SC=1

**ADC_09** ***ADC can have random conversion errors***

**Revisions Affected**

B

**Description**

ADC can have errors at a rate as high as 1 in 400 million ADC conversions. When a conversion error occurs, the error results in a jump in the digital output of the ADC without a corresponding change in the ADC input voltage, otherwise known as a ‘sparkle code’. The magnitude of the jump is 64 LSBs higher or lower than the expected ADC output when the ADC is used in 12-bit resolution setting. The magnitude of the jump decreases to ±16 LSBs for 10-bit resolution and ±4 LSBs when set to 8-bit resolution.

**Workaround**

The error rate can be reduced to 1 error in 100 billion ADC conversions by setting ADC.DEBUG1:CTRL[10:9] bits high.

Other software workarounds, like a best-out-of-three, where out of three consecutive samples the one with the highest standard deviation is discarded and the other two averaged to generate the ADC output, can also be considered.

Software averaging of 16 consecutive ADC outputs decreases the deviation of the ADC output to ±4 LSBs when set to 12-bit resolution.

These workarounds would be incorporated into future releases of SimpleLink™ Low Power F3 software development kit (SDK).

## BATMON_01 *Incorrect temperature measurement*

**Revisions Affected**

B

**Description**

BATMON can report incorrect temperatures when hysteresis is enabled. To prevent potential incorrect temperature reports, the user must always disable BATMON hysteresis.

**Workaround**

Hysteresis is controlled by the PMUD.CLT[2] HYST_EN bit.

Hysteresis is enabled by default (reset value = 1) and, therefore, must actively be disabled during boot.

Hysteresis can be disabled by clearing the PMUD.CLT[2] HYST_EN bit using the following command:

HWREG( PMUD_BASE + PMUD_O_CTL ) = ( PMUD_CTL_CALC_EN | PMUD_CTL_MEAS_EN )

This workaround is incorporated into the SimpleLink™ Low Power F3 software development kit (SDK) version 8.10 and newer.

## BATMON_02 *Spurious temperature update interrupts from BATMON in standby*

**Revisions Affected**

B

**Description**

BATMON can issue spurious temperature update interrupts when PMUD.EVENT.TEMP_UPDATE is used as a wake-up source from standby.

**Workaround**

Instead of using PMUD.EVENT.TEMP_UPDATE as the wake-up source, PMUD.EVENT.TEMP_OVER_UL (current temperature over a set upper limit) or PMUD.EVENT.TEMP_BELOW_LL (current temperature below a set lower limit) shall be considered.

When using PMUD.EVENT.TEMP_OVER_UL or PMUD.EVENT.TEMP_BELOW_LL as wake-up interrupts, these are the other settings that have to be enabled:

- Select GLDO as the source for VDDR regulation by setting PMCTL.VDDRCTL.SELECT to 0x0.

**Note**

**This causes a slight increase in standby power consumption. Please check the ‘Power Consumption – Power Modes’ section of the data sheet for exact details.**

- Set SYS0.TMUTE4.RECHCOMPREFLVL to 0x2
- Set SYS0.TMUTE5.GLDOISSET to 0x1E

This workaround would be incorporated into future releases of SimpleLink™ Low Power F3 software development kit (SDK).

| CKM_01 | *Tracking loop issues during standby-wake* |
|---|---|
| **Revisions Affected** | CC2340R53-Q1 Rev B |
| **Details** | In a few corner cases, the HFOSC tracking loop stops working out of standby, with TRACKREFLOSS getting set, indicating that the selected reference clock of the tracking loop is lost. |
| **Workaround** | The standby entry sequence includes disabling software override and clearing CKM LDO control bits. These writes have to be sequenced such that the software override is cleared first, and then the LDOCTL bits are all set to zero.<br>If these settings occur in parallel, the tracking loop is seen to get stuck in a few cases.<br>The workaround has been implemented within the power drivers and is a part of the 9.10 SDK release. |

| CLK_01 | *The Bluetooth Low Energy link cannot be maintained when using LFOSC only.* |
|---|---|
| **Revisions Affected** | B |
| **Description** | A small percentage of devices do not maintain a Bluetooth Low Energy link if LFOSC is used as a sleep clock due to random timing error above 500 PPM. |
| **Workaround** | A software workaround are available in the SimpleLink F3 SDK >= 8.10.xx to allow devices to operate in the broadcaster, observer and peripheral roles when using LFOSC only. When the software workaround is used, the device can see short periods of operation with reduced throughput and increased power consumption when the timing error occurs. This software workaround does not support the central role. To completely avoid the consequences of increased power consumption and connection throughput or support the Central role, TI recommends using an external 32.768kHz crystal. |

## I2C_01 *SDA and SCL Open-Drain Output Buffer Issue*

**Revisions Affected** B

**Description**

The SDA and SCL outputs are implemented with push-pull 3-state output buffers rather than open-drain output buffers as required by $I^2C$. While it is possible for the push-pull 3-state output buffers to behave as open-drain outputs, an internal timing skew issue causes the outputs to drive a logic-high for a duration of approximately 1ns–2ns before the outputs are disabled. The unexpected high-level pulse only occurs when the SCL or SDA outputs transition from a driven low state to a high-impedance state.

This short high-level pulse injects energy in the $I^2C$ signal traces, which causes the $I^2C$ signals to sustain a period of ringing as a result of multiple transmission line reflections. This ringing should not cause an issue on the SDA signal because it only occurs at times when SDA is expected to be changing logic levels, and the ringing will have time to damp before data is latched by the receiving device. The ringing can have enough amplitude to cross the SCL input buffer switching threshold several times during the first few nanoseconds of this ringing period, which can cause clock glitches. This ringing should not cause a problem if the amplitude is damped within the first 50ns because $I^2C$ devices are required to filter the SCL inputs to remove clock glitches. Therefore, it is important to design the PCB signal traces to limit the duration of the ringing to less than 50ns. One possible way to reduce the ringing is to insert series termination resistors near the SCL and SDA terminals to attenuate transmission line reflections.

This issue may also cause the SDA output to be in contention with the target SDA output for the duration of the unexpected high-level pulse when the target begins an ACK cycle. This occurs because the target may already be driving SDA low before the unexpected high-level pulse occurs. The glitch that occurs on SDA as a result of this short period of contention does not cause any $I^2C$ protocol issue, but the peak current applies unwanted stress to both $I^2C$ devices and potentially increases power supply noise. Therefore, a series termination resistor located near the respective SDA terminal is required to limit the current during the short period of contention.

A similar contention problem can occur on SCL when connected to $I^2C$ target devices that support clock stretching. This occurs because the target is driving SCL low before the unexpected high-level pulse occurs. The glitch that occurs on SCL as a result of this short period of contention does not cause any $I^2C$ protocol issue because $I^2C$ devices are required to apply a glitch filter to their SCL inputs. However, the peak current applies unwanted stress to both $I^2C$ devices and potentially increases power supply noise. Therefore, a series termination resistor located near the respective SCL terminal is required to limit the current during the short period of contention.

If another controller is connected, the unexpected high-level pulses on the SCL and SDA outputs can cause contention during clock synchronization and arbitration. The series termination resistors described above also limit the contention current in this use case without creating any $I^2C$ protocol issue.

**Workaround**

Insert series termination resistors on the SCL and SDA signals and locate them near the SCL and SDA terminals, along with the SCL and SDA pullup resistors.

The ringing can also be reduced by controlling the output to use minimum drive strength and a reduced slew rate. These options are only configurable on pins that support high drive output. Standard drive pins have no configuration options.

## GPIO_01 *Open-Drain Configuration Can Drive a Short High Pulse*

**Revisions Affected** B

**Description**

Each DIO can be configured to an open-drain mode using the IOCx register.

However, an internal device timing issue may cause the GPIO to drive a logic-high for approximately 1ns–2ns during the transition into or out of the high-impedance state. This undesired high-level can cause the GPIO to be in contention with another open-drain driver on the line if the other driver is simultaneously driving low. The contention is undesirable because it applies stress to both devices and results in a brief intermediate voltage level on the signal. This intermediate voltage level may be incorrectly interpreted as a high level if there is not sufficient logic filtering present in the receiver logic to filter this brief pulse.

**Workaround**

If contention is a concern, do not use the open-drain functionality of the GPIOs; instead, emulate open-drain mode in software. Open-drain emulation can be achieved by setting the GPIO data (DOUT31_0.DIOx) to a static 0 and driving the GPIO output enable (DOE31_0.DIOx) to enable or disable the drive low. For an example implementation, see the code below.

```
#include <ti/devices/cc23x0r5/driverlib/gpio.h>
    /* Call driver init functions */
    GPIO_init();

    //Set GPIO data (DOUT31_0.DIOx) to static 0
    GPIOClearDio(CONFIG_GPIO_LED_0);
    while(1) //loop below toggles the LED on and off every 1 second
    {
    GPIOSetOutputEnableDio(CONFIG_GPIO_LED_0, 1);
    sleep(1);
    GPIOSetOutputEnableDio(CONFIG_GPIO_LED_0, 0);
    sleep(1);
    }
```

## PMU_01 *Slow Transition Across Brown-Out Detect (BOD) Threshold Might Cause the Device to Hang*

**Revisions Affected**

B

**Details**

If the VDDS supply voltage is held in the BOD threshold region (approximately 1.68V), the device might, on rare occasions, enter a lock-up state. In this state, the device draws approximately 2.25mA of current and will not recover even if the VDDS supply voltage is subsequently increased above the BOD threshold. Recovery from this state requires either a pin reset or reducing the VDDS supply voltage below the power-on reset (POR) threshold (1.0V), thereby triggering a POR reset.

The lock-up state is triggered if a brown-out-detect (BOD) event occurs during specific stages of boot code execution. There are two critical narrow time windows, each of approximately 10 ns duration, and both of these time windows occur within 100 µs to 1 ms after the reset event that initiates the boot code. The issue typically arises when the supply voltage ramps slowly across the BOD threshold. In such cases, supply resistance in combination with device startup current may cause the VDDS voltage to repeatedly dip below the BOD threshold as the device resets, increasing the likelihood of entering the lock-up state.

For Li-Ion and NiMH rechargeable batteries, a first-level protection disconnecting the chip VDDS supply would typically prevent the device from entering this state during battery discharge as the device power supply would fall below the POR threshold.

Even with non-rechargeable (primary) batteries, this issue may still occur, particularly as the battery approaches end-of-life and the voltage slowly decreases. In these cases, a workaround may not always be necessary, as the device will eventually require battery replacement, which would also trigger a power-on reset. However, the risk of lock-up cannot be ruled out.

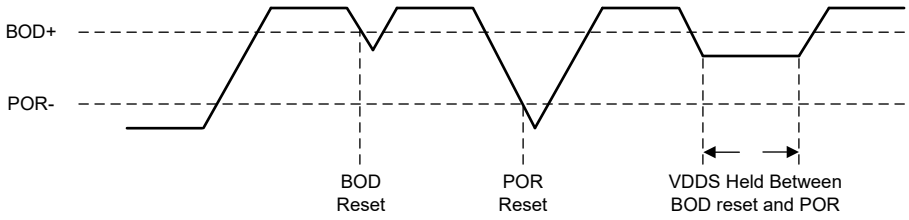


**Figure 3-1. Diagram showing occurrence**

**Workaround**

The following workarounds must be implemented:

The specified operating supply voltage range for the device is 1.72V to 3.8 V. When using rechargeable batteries, the battery protection system must ensure one of the following:

- The device supply voltage remains at or above the minimum operating supply voltage (1.72V) once powered on, or
- If the device supply is discharged below the minimum operating supply voltage (1.72V), the device must be reset (pin or power-on reset) when the supply is charged above the minimum operating supply voltage (1.72V) again.

| UART_01 | *UART might issue spurious µDMA write burst requests* |
|---|---|
| **Revisions Affected** | B |
| **Details** | UART issues a µDMA burst write request when the number of entries in the FIFO is less than or equal to the configured burst FIFO threshold. A subsequent µDMA write burst request is issued, if the total FIFO entries are still below the configured threshold. UART takes one additional SVT clock cycle to update the internal FIFO level, when compared to µDMA signaling an end to its burst active state. In corner cases, dependent on initial UART FIFO level, configured FIFO threshold for burst request, interconnect latencies, and so on, this additional clock latency within UART can cause a spurious write burst request to be generated towards µDMA, which might cause the last write(s) by µDMA responding to this to get missed. This is not seen on UART read burst requests as µDMA waits for the read to complete before signaling an end of read burst. |
| **Workaround** | When used along with UART, µDMA SETBURST must be configured for burst requests.<br>µDMA arbitration size must be 2.<br>TX FIFO level trigger must be set to ≤ 1/4 empty for the write burst trigger |

# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from September 30, 2024 to July 16, 2025 (from Revision A (September 2024) to Revision B (July 2025))** **Page**



**Changes from December 1, 2023 to September 30, 2024 (from Revision * (December 2023) to Revision A (September 2024))** **Page**

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265